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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

VELLFIRE

2020.06.05

21-OCT-2002		
DATE	CHANGE NO.	REV.

DESIGN / DRAWER		XXX	DATE		21-OCT-2002	TITLE MODEL,PROJECT,FUNCTION MAIN BOARD					
CHECK						SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0			REV X01
APPROVAL FILE NAME											
PCB RN		S6vxxxxxxxxxx	PCB VER		YYY	SHEET 1 of 130					

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FOR 17 SMALL BOARD1&2

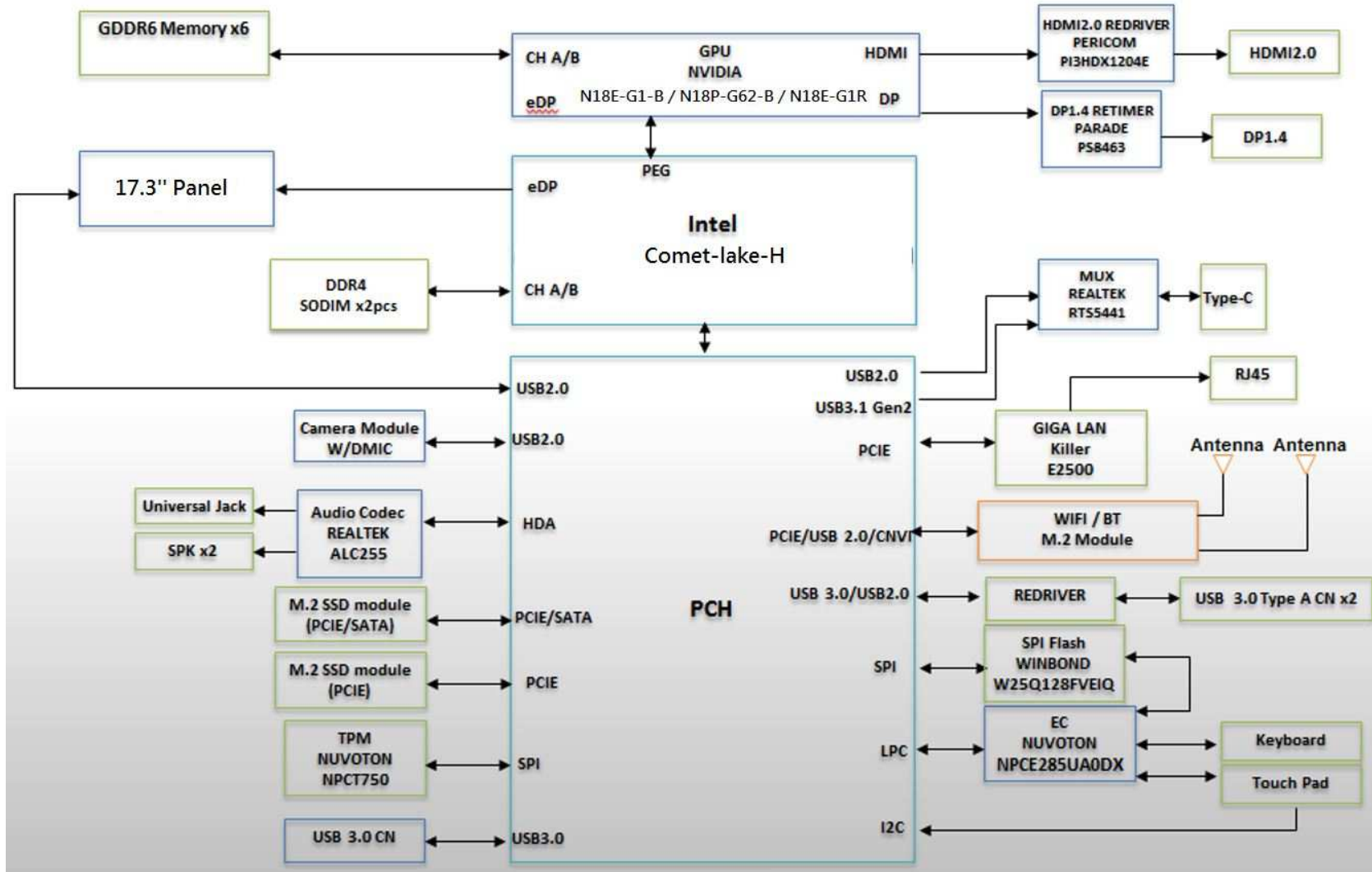
129.KB_BL
130.KB

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INVENTEC

TITLE			
MODEL PROJECT FUNCTION TABLE OF THE CONTENT			
SIZE	CODE	DOC.NUMBER	REV
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SHEET 2 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX



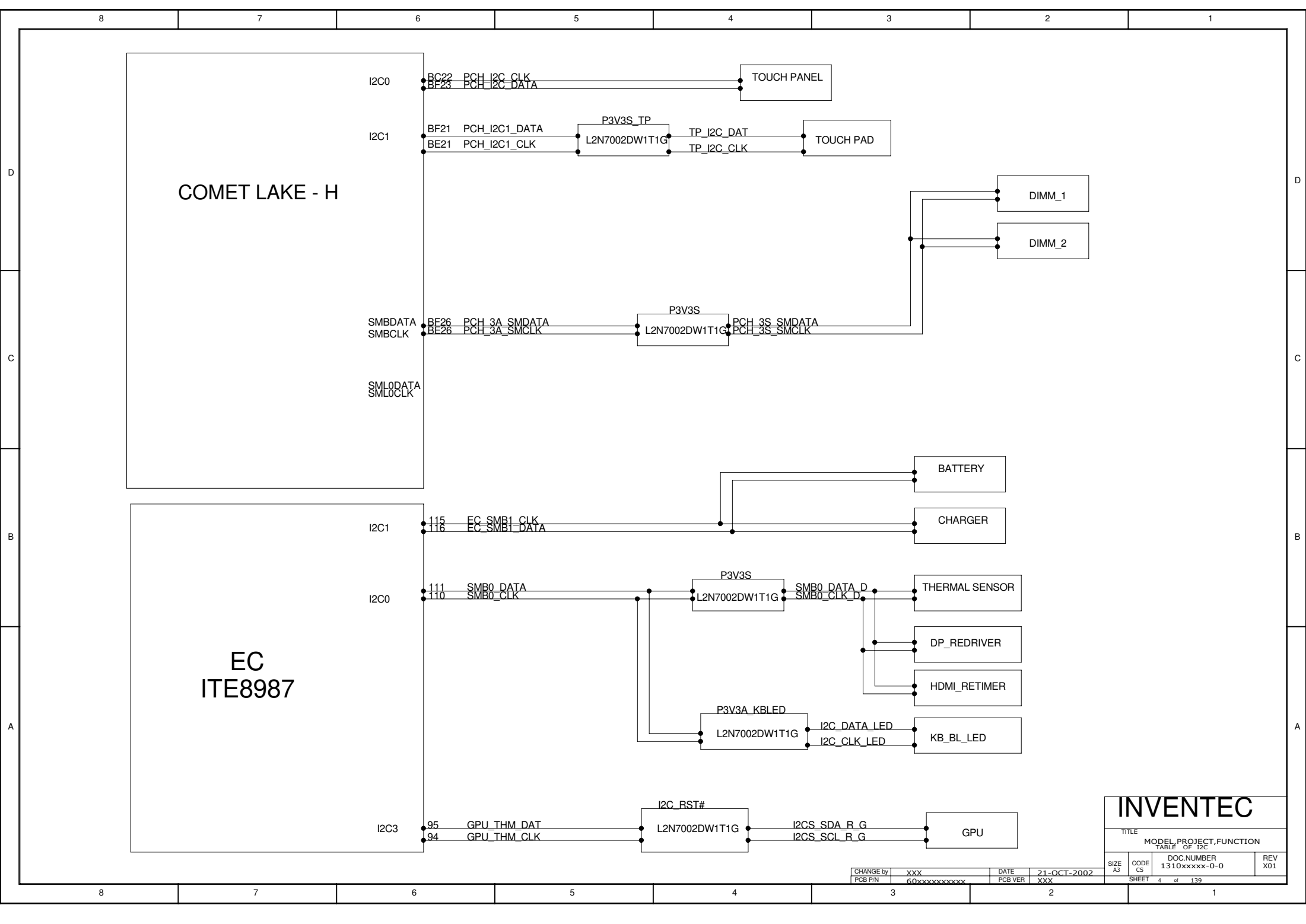
INVENTEC

TITLE MODEL PROJECT FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

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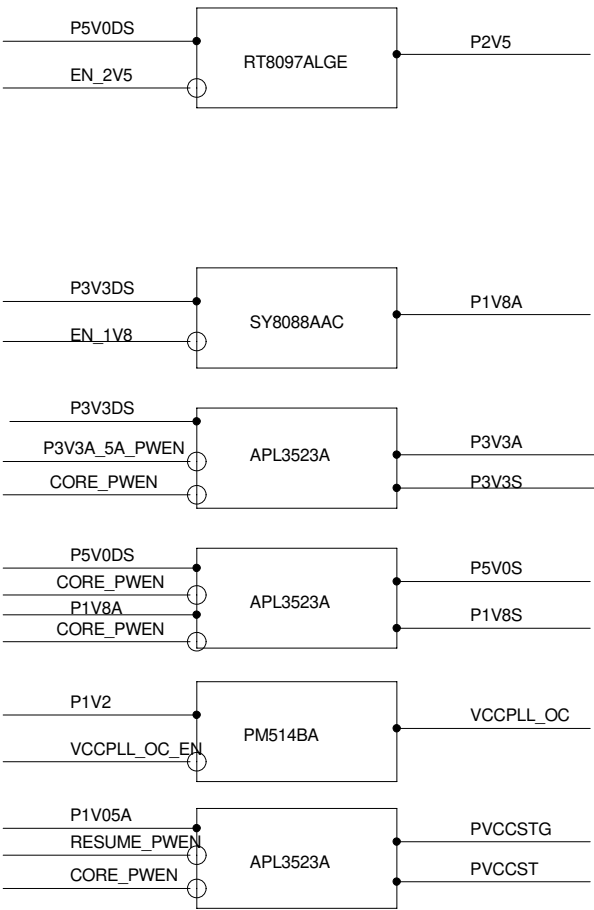
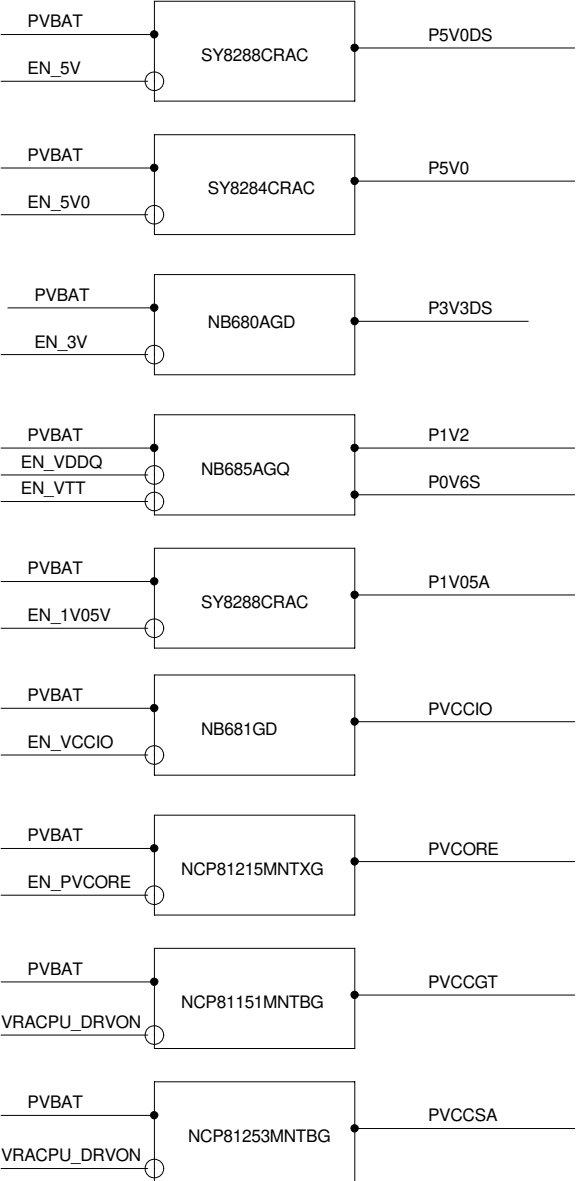
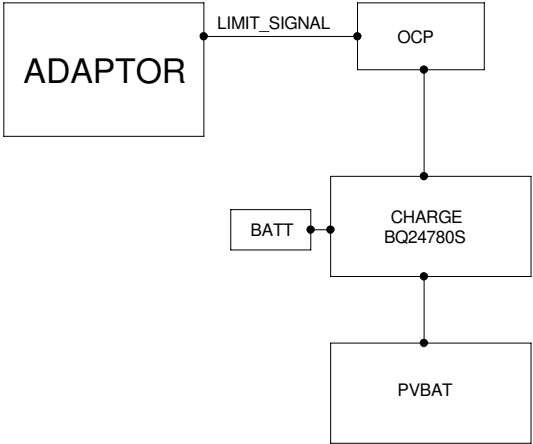


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TITLE MODEL PROJECT,FUNCTION TABLE OF I2C			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

POWER BLOCK

IN/EN OUT IN/EN OUT

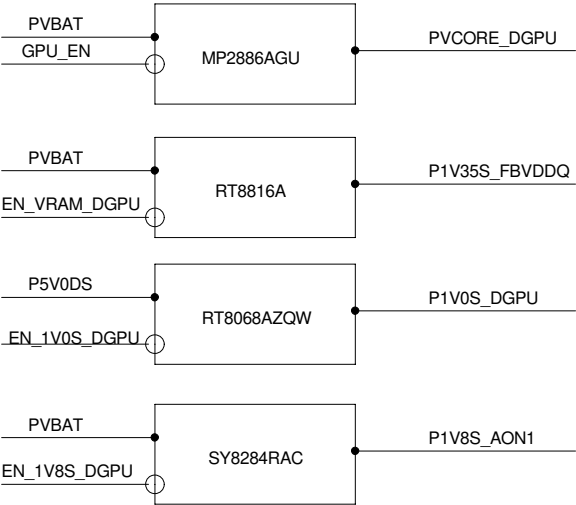


INVENTEC

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	5	of	139				

GPU POWER BLOCK

IN/EN OUT

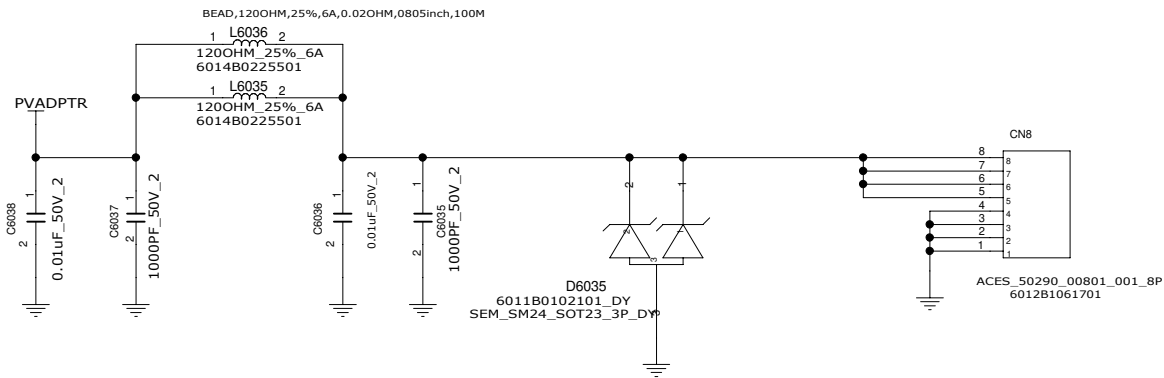


INVENTEC

TITLE
MODEL PROJECT, FUNCTION
TABLE OF 12C

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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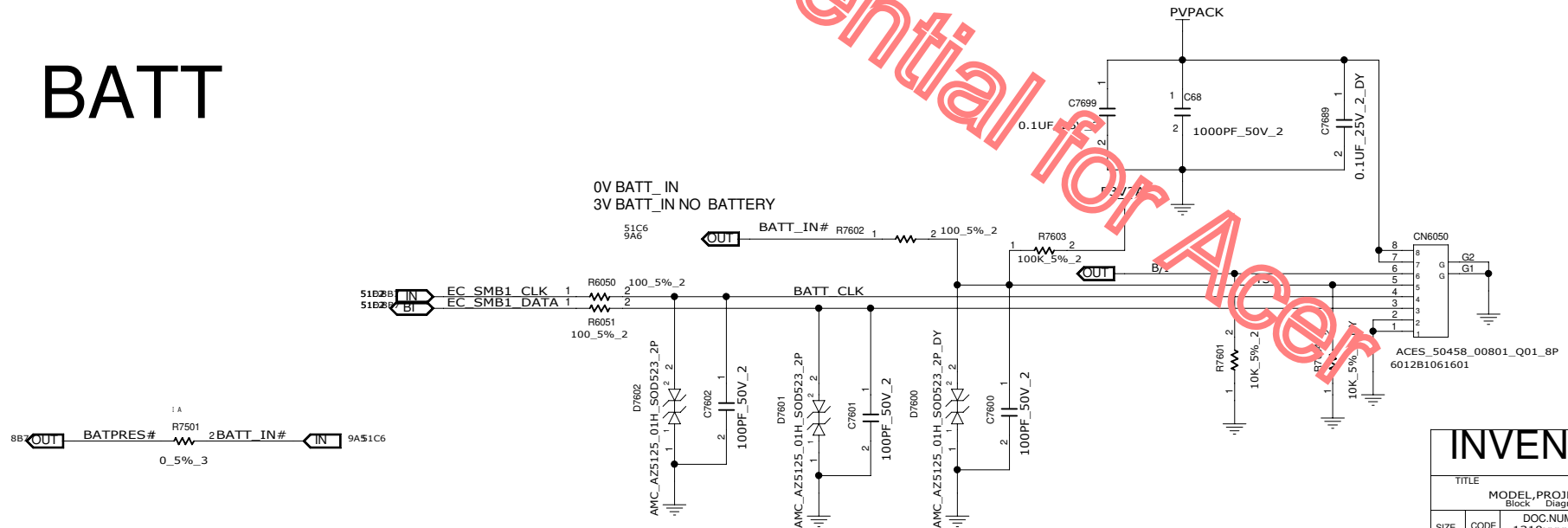
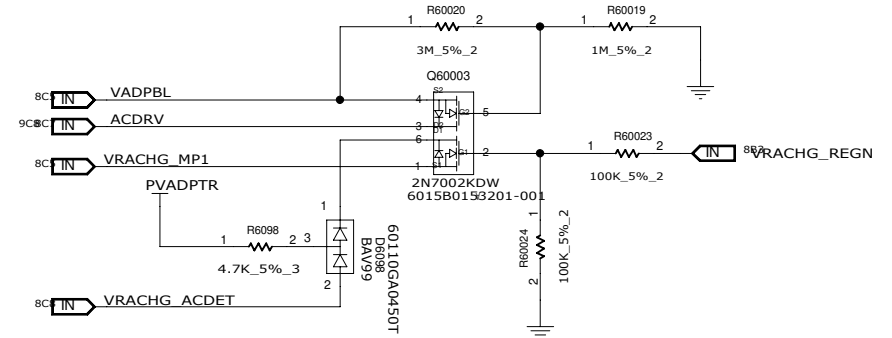
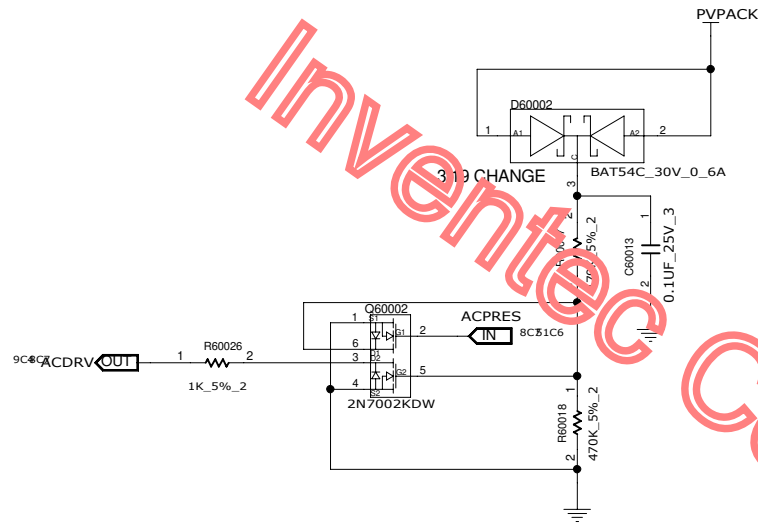
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

FOR CHARGER

SCP

ARP

BATT



INVENTEC

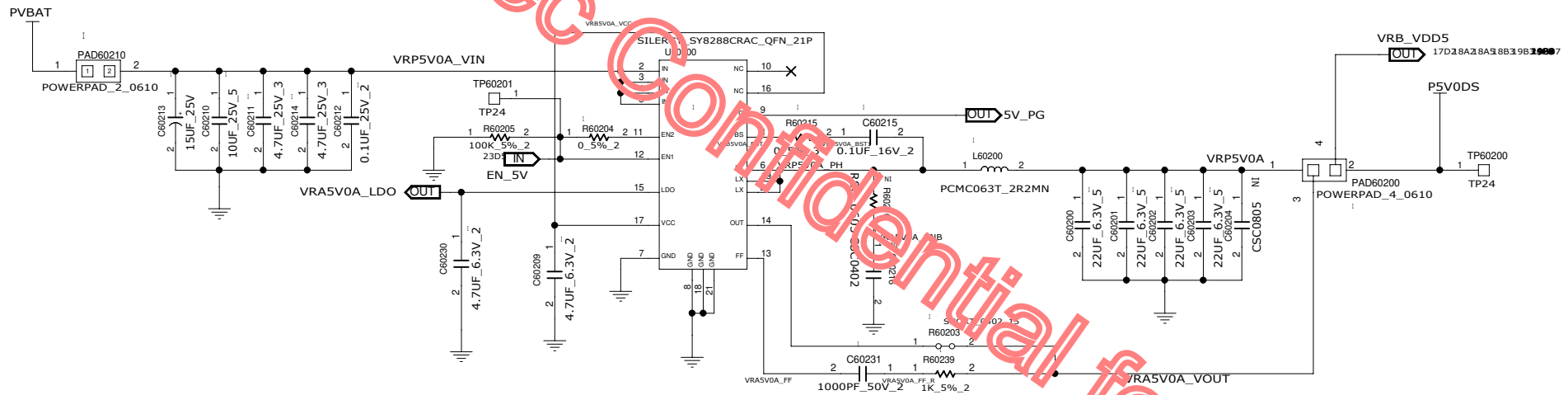
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MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS 1310xxxx-0-0 REV X01
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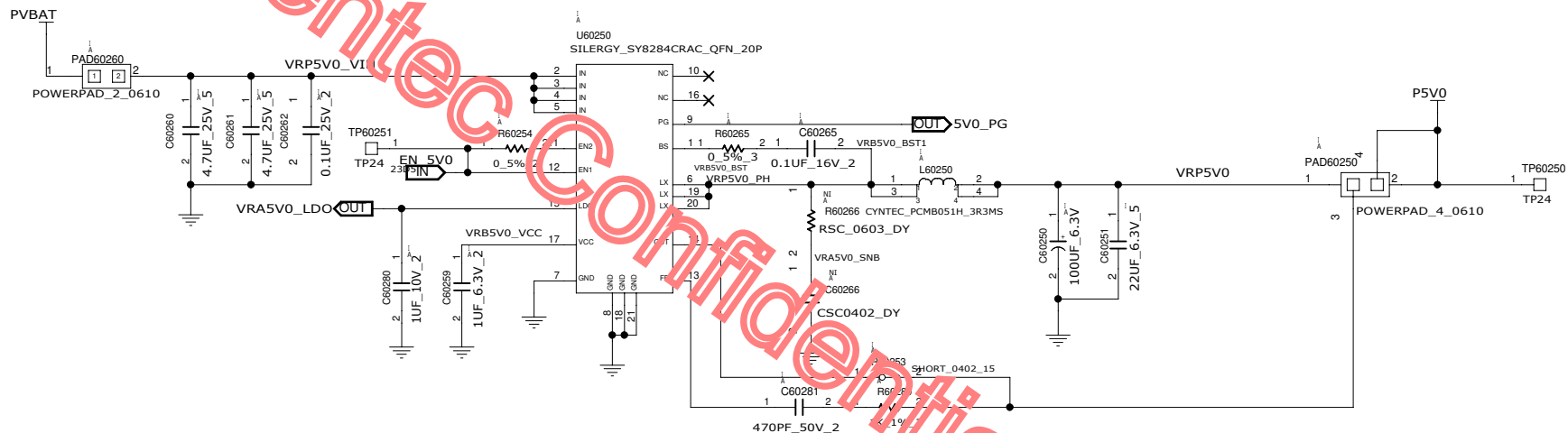
CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

Inventec Confidential for Acer

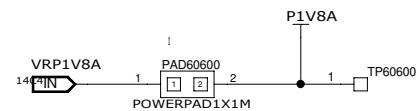


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TITLE MODEL PROJECT,FUNCTION PSV0DS				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
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INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC. NUMBER		REV
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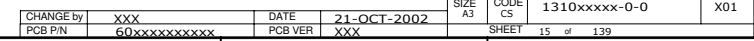
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



$$V_{OUT} = 0.6 * (1 + (R_{60600} / R_{60601}))$$

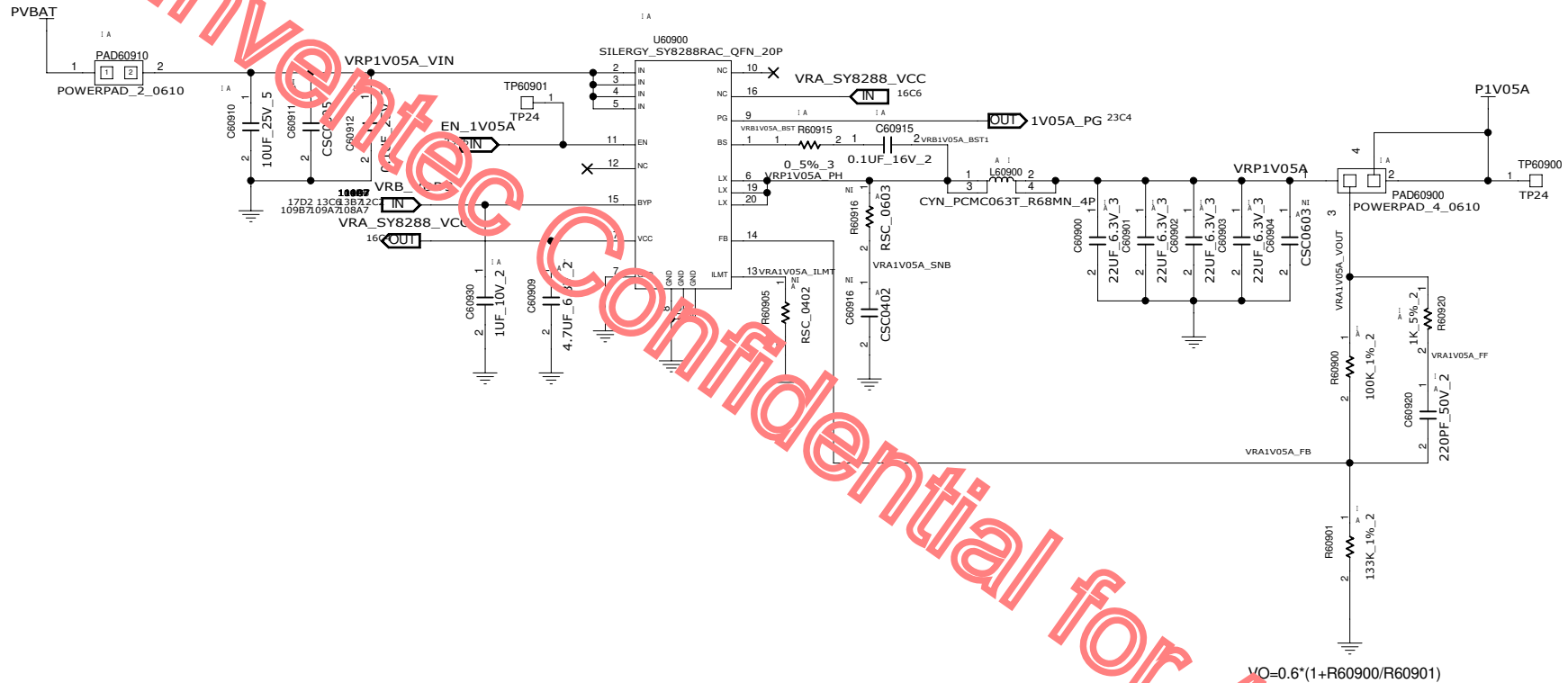
AS	CS	
SHEET		14 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



TITLE	MODEL,PROJECT,FUNCTION
	P2V5

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
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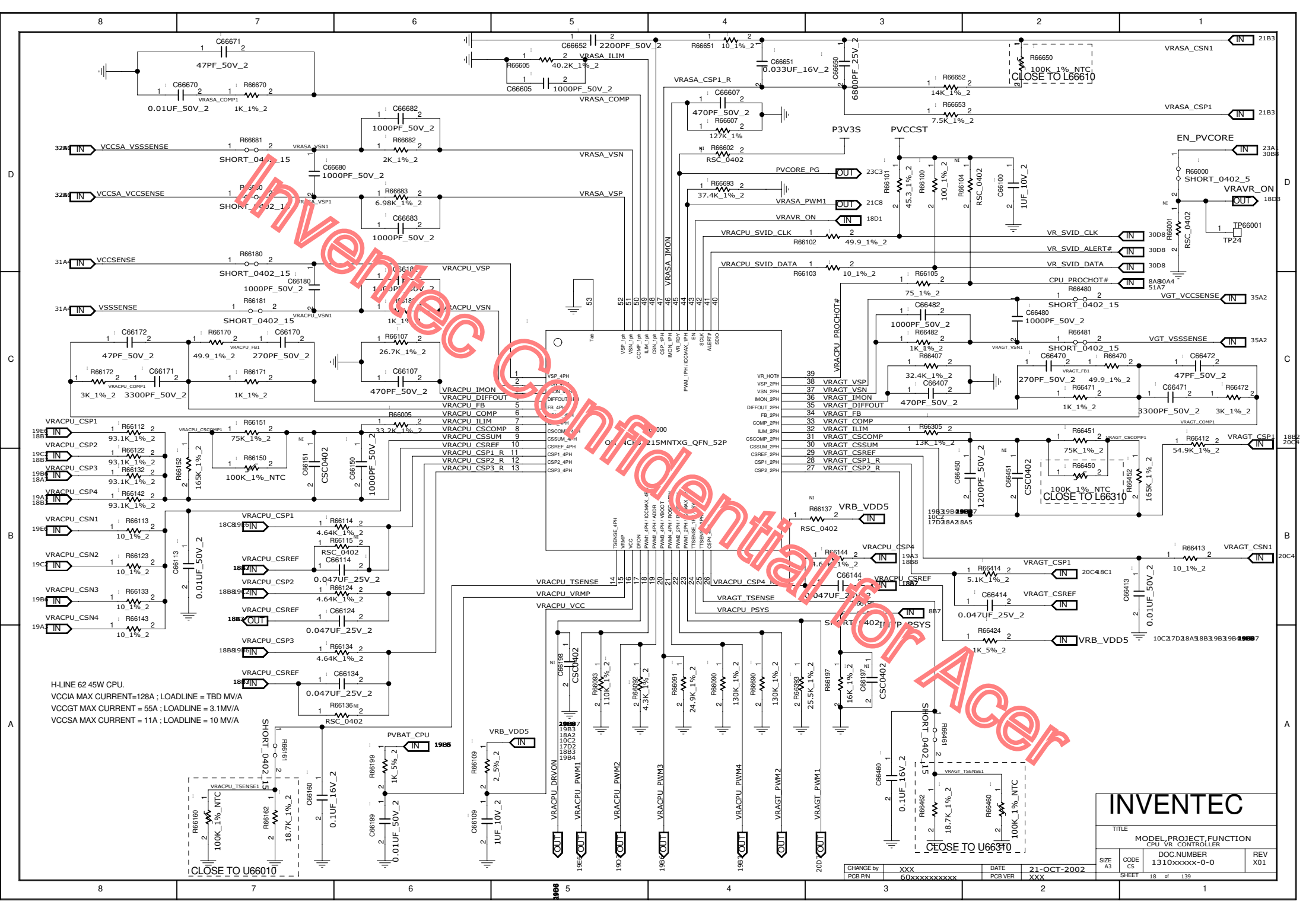


$$VO=0.6 \cdot (1 + R60900/R60901)$$

INVENTEC

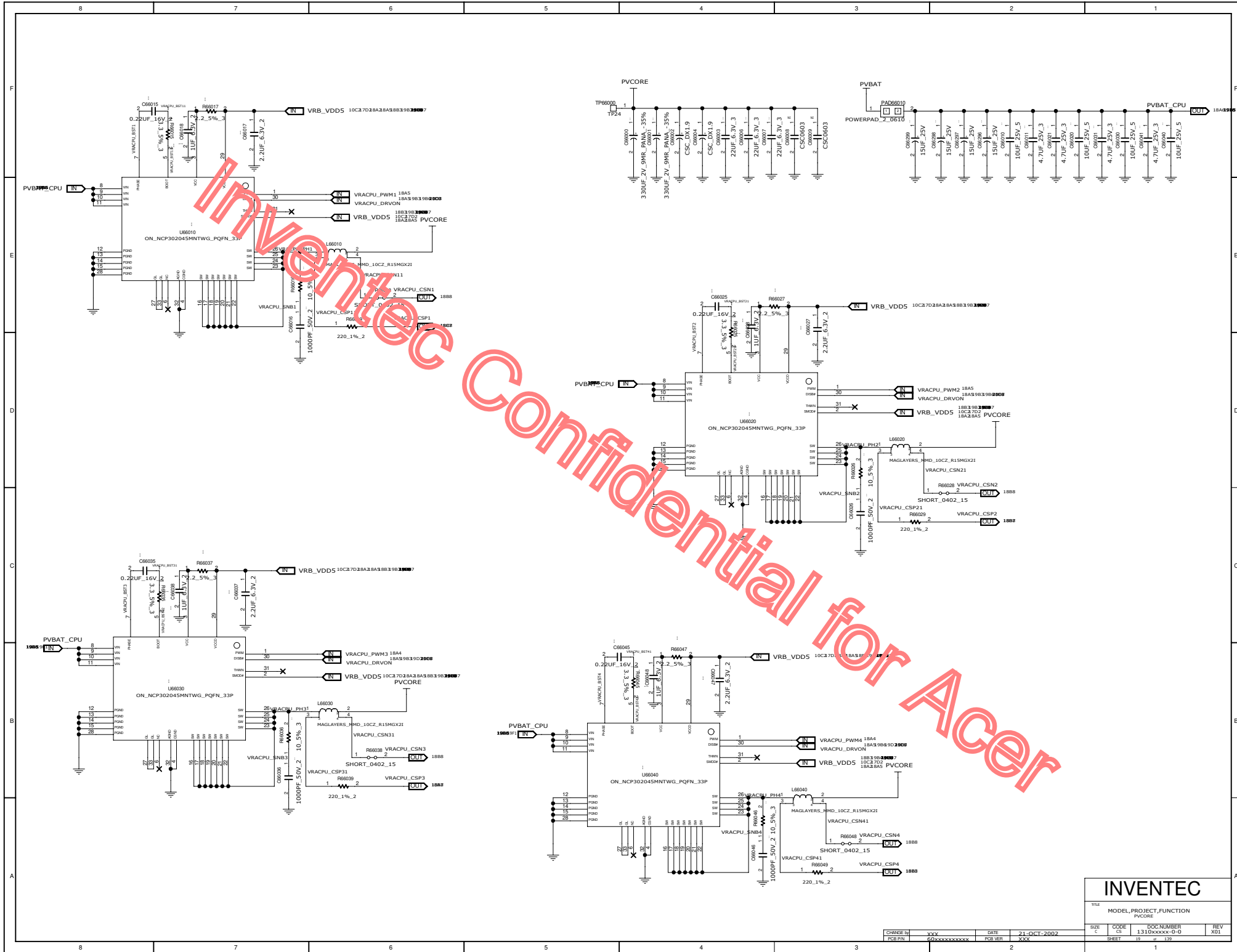
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MODEL PROJECT, FUNCTION			
P1V0A			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



H-LINE 62 45W CPU.
VCCIA MAX CURRENT=128A; LOADLINE = TBD MV/A
VCCGT MAX CURRENT = 55A; LOADLINE = 3.1MV/A
VCCSA MAX CURRENT = 11A; LOADLINE = 10 MV/A

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION CPU VR CONTROLLER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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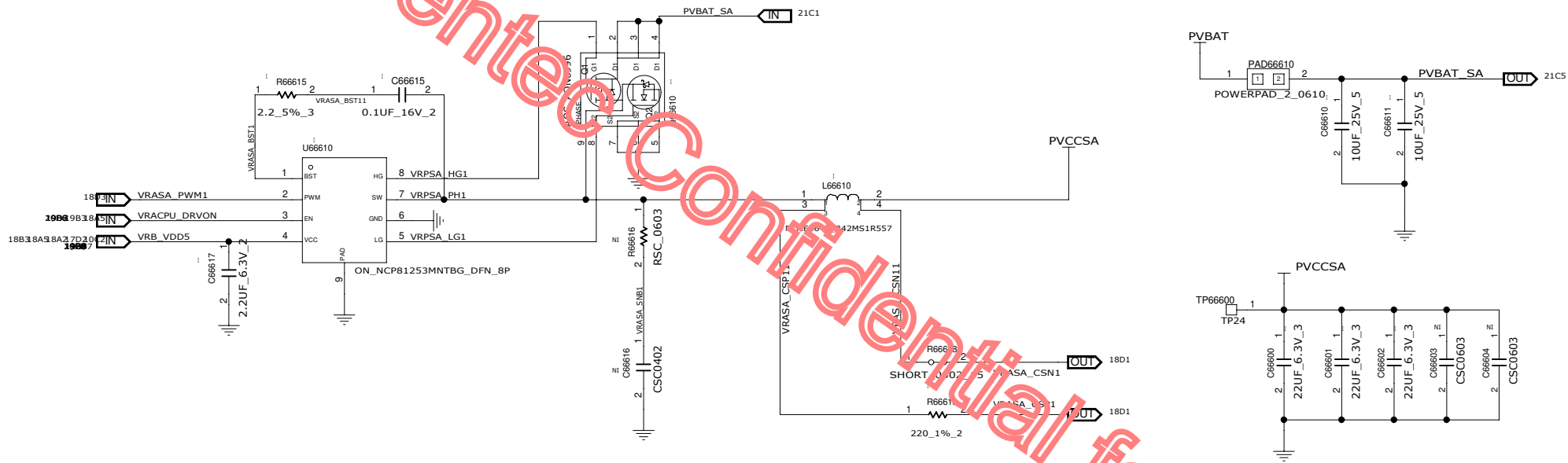
INVENTEC

TITLE		MODEL, PROJECT, FUNCTION	
SIZE	C	CODE	CS
DOC NUMBER	1310xxxxx-0-0		
REV	X01		

CHANGE D	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxx	PCB VER	XXX

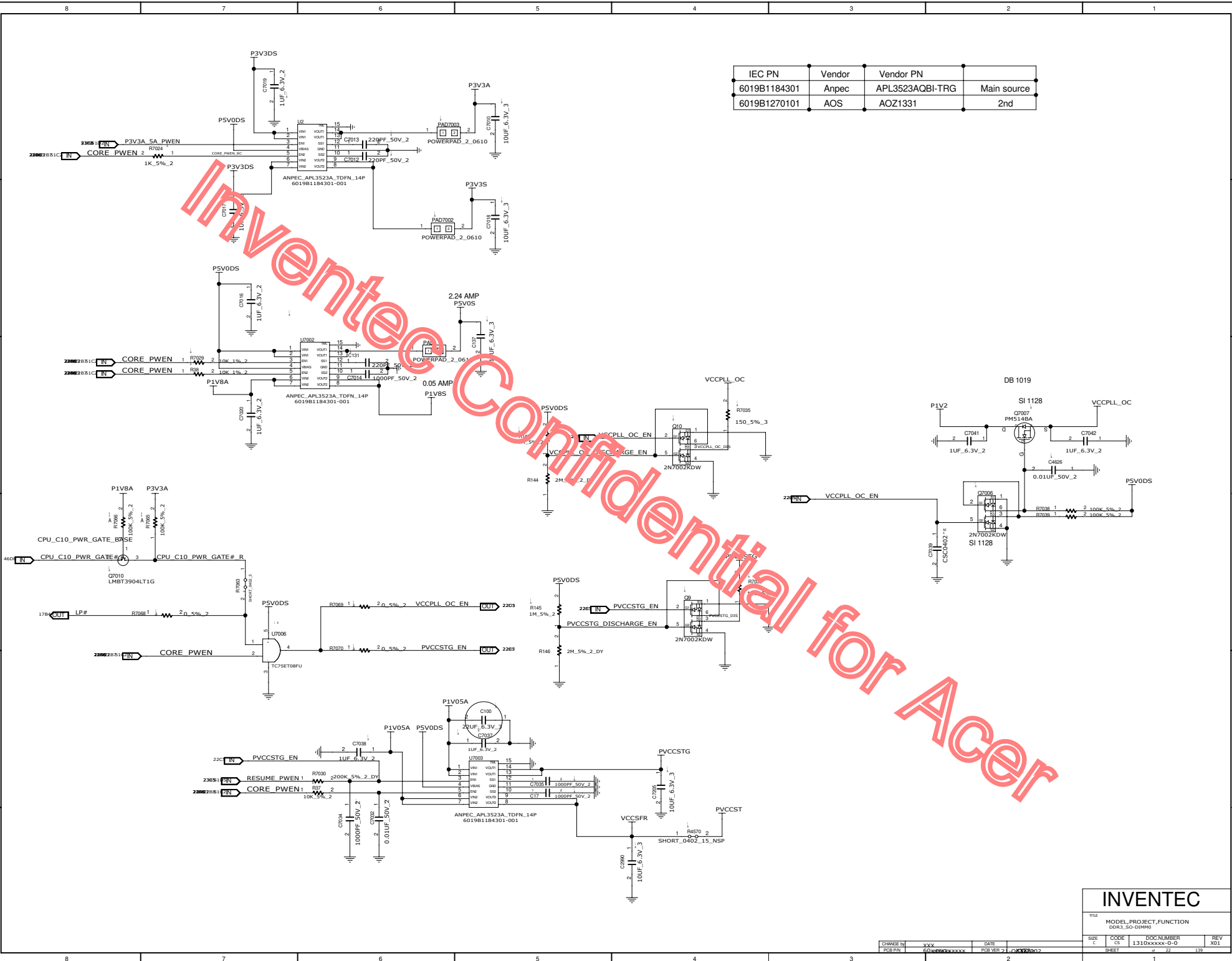
SHEET 19 of 139

Inventec Confidential for Acer



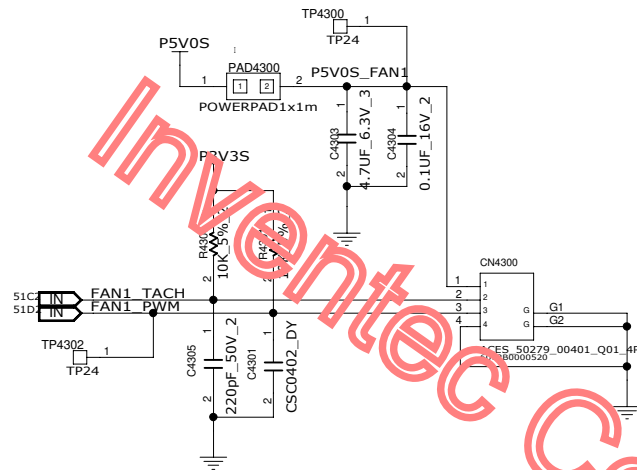
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MODEL,PROJECT,FUNCTION				
PVCCSA				
SIZE	CODE	DOC NUMBER	REV	
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

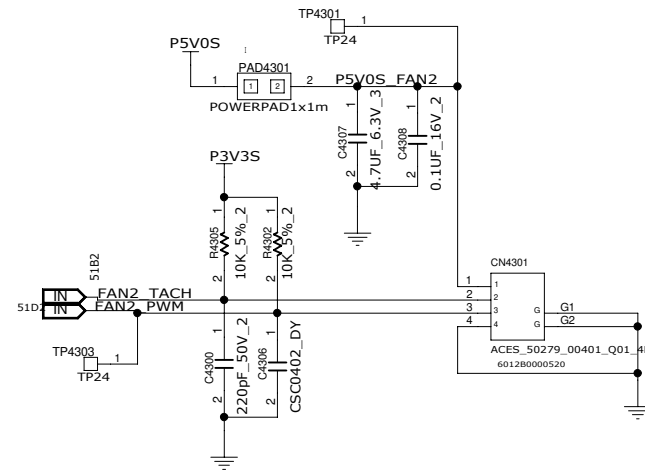


IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

INVENTEC

TITLE			
MODEL		PROJECT	FUNCTION
FAN		THERMAL	
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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REFERENCE 0~49(PCB SCREW)

X 1 FIX1
FIX_MASK
X 1 FIX2
FIX_MASK
X 1 FIX3
FIX_MASK
X 1 FIX4
FIX_MASK

X 1 FIX5
FIX_MASK
X 1 FIX6
FIX_MASK
X 1 FIX7
FIX_MASK
X 1 FIX8
FIX_MASK

1 S35
SCREW280_900_700_1P
1 S18
SCREW280_700_1P
1 S19
SCREW280_700_1P
1 S20
SCREW280_700_1P
1 S21
SCREW280_700_1P
1 S22
SCREW280_700_1P
1 S23
SCREW280_700_1P
1 S24
SCREW280_700_1P

1 S27
SCREW390_850_700_1P
1 S25
SCREW390_850_700_1P
1 S26
SCREW390_1160_850_1P
1 S11
SCREW280_900_550_NP_1P
1 S10
SCREW280_850_700_1P
1 S16
SCREW280_850_700_1P
1 S17
SCREW280_700_1P

PCB

1 S2
SCREW420_700_1P
1 S3
SCREW420_700_1P
1 S4
SCREW420_700_1P
1 S5
SCREW420_700_1P
1 S6
SCREW420_700_1P
1 S7
SCREW420_700_1P
1 S8
SCREW420_700_1P

INVENTEC

TITLE
MODEL PROJECT FUNCTION
XDP & ME CONN.

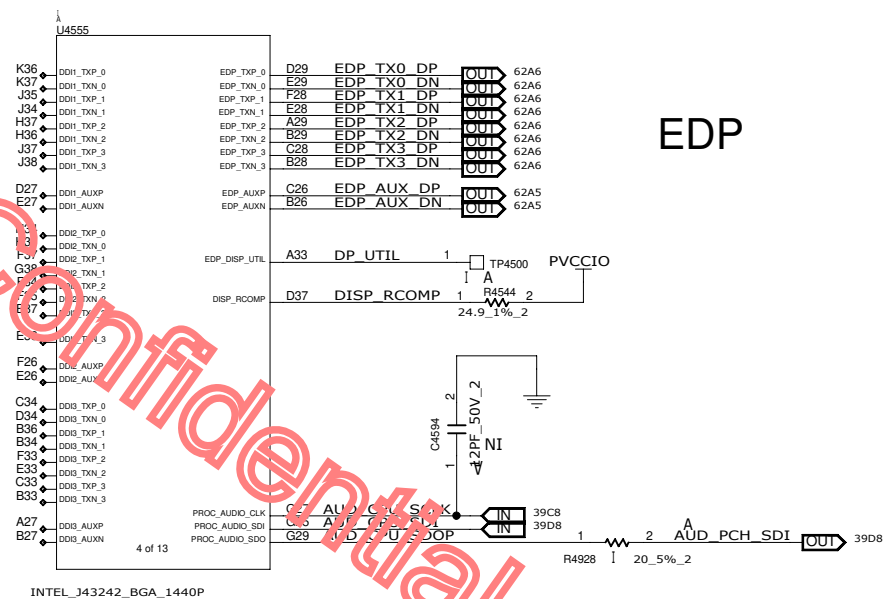
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A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

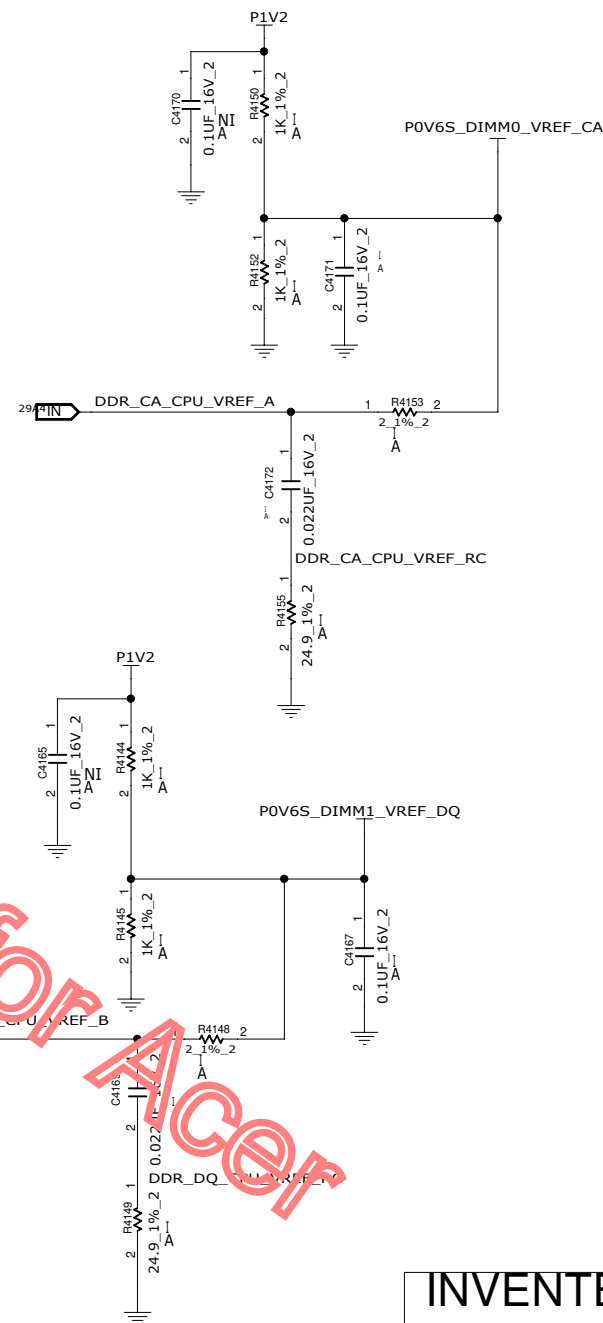
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1

	8	7	6	5	4	3	2	1
D								



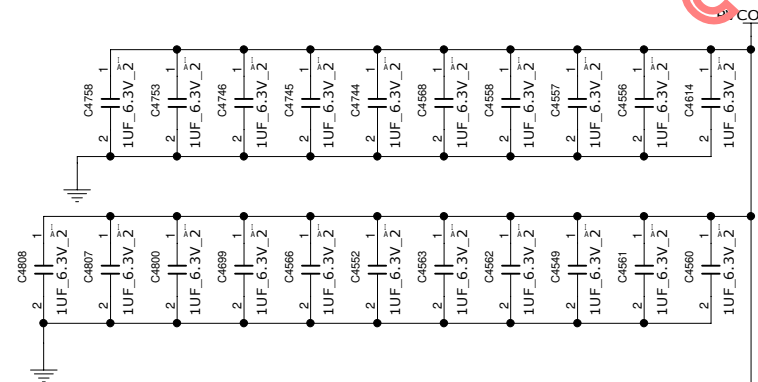
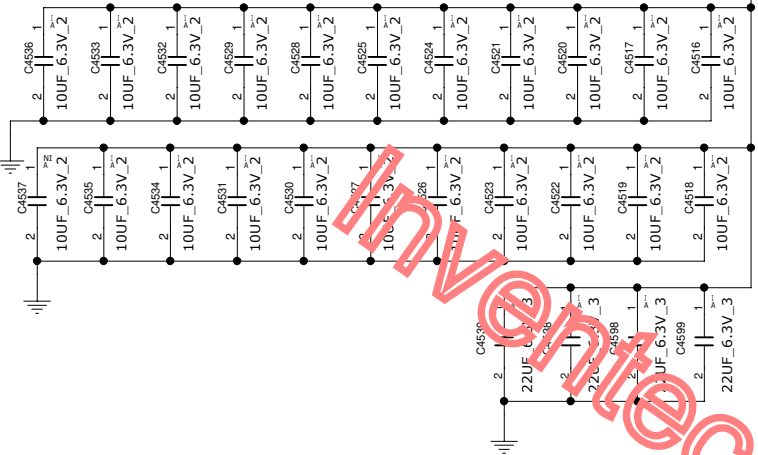
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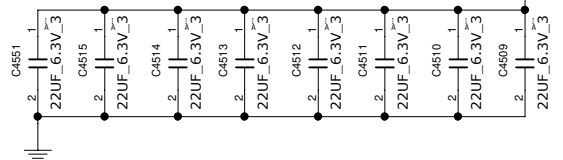
CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 29 of 139			

PLACE IN BACK SIDE

PVCORE



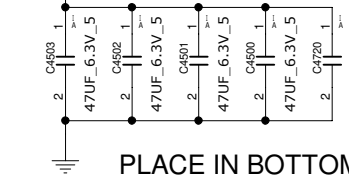
PVCORE



EDS VER0.7

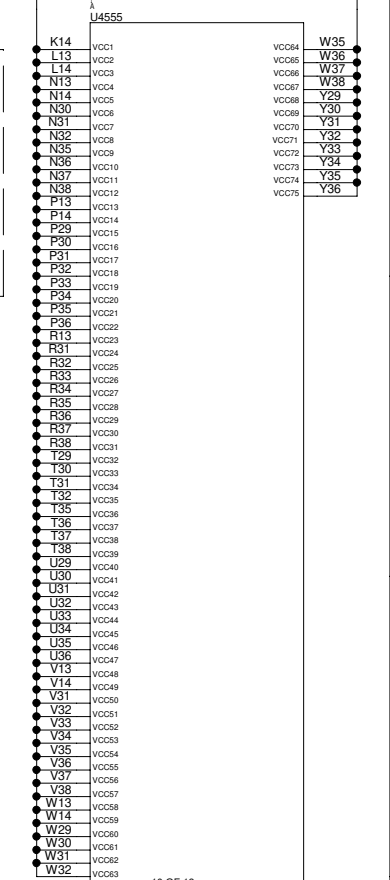
PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24

PVCORE



PLACE IN BOTTOM SIDE

PVCORE



10 OF 13

INTEL_J43242_BGA_1440P

INTEL_J43242_BGA_1440P

9 OF 13

VCC_SENSE
VSS_SENSE

AG37 VCCSENSE
AG38 VSSSENSE

18D8
18C8

INVENTEC

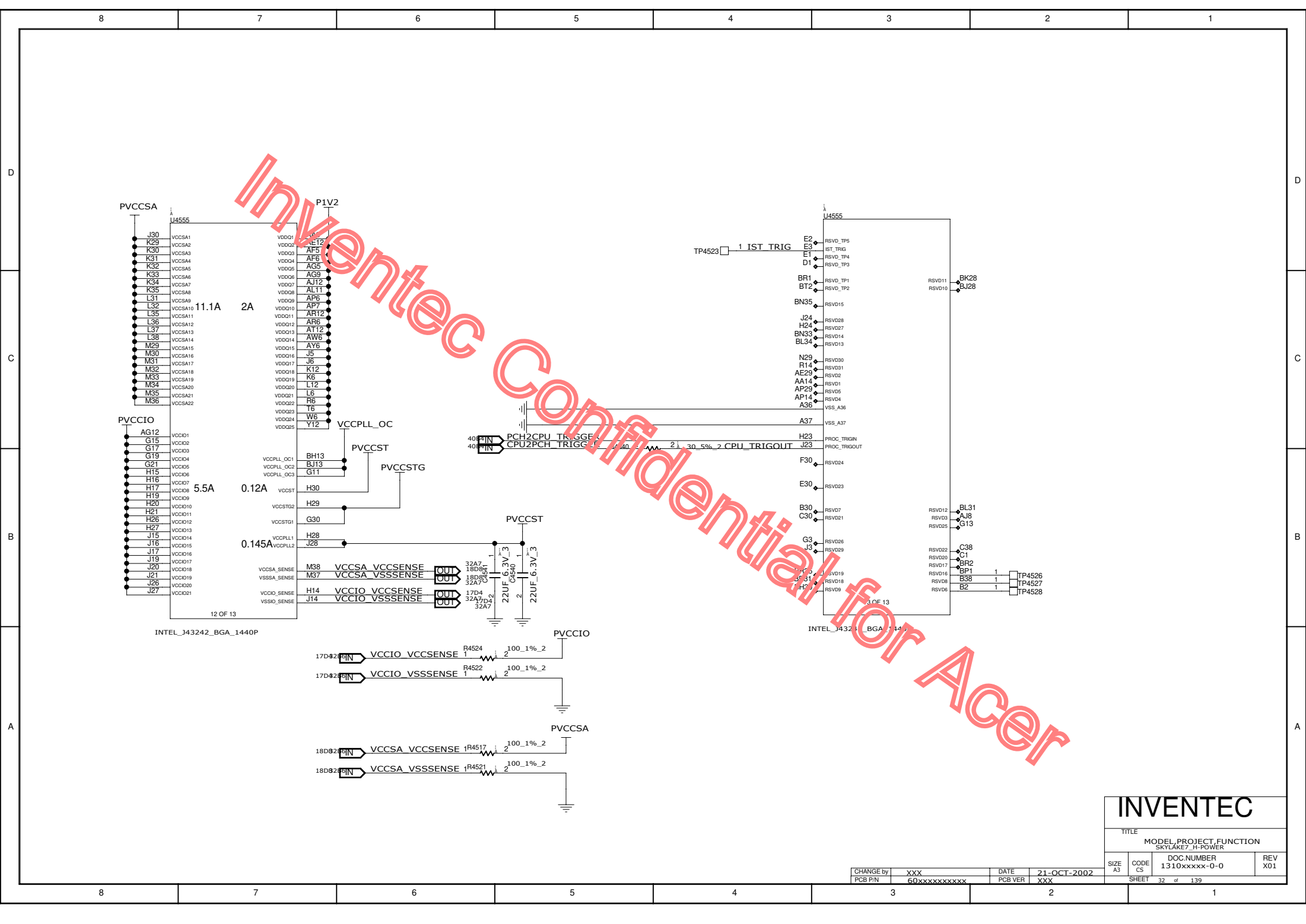
TITLE
MODEL PROJECT FUNCTION
SKYLAKES_HI-POWER

SIZE A3 CODE CS
DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

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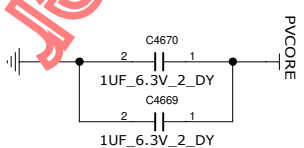
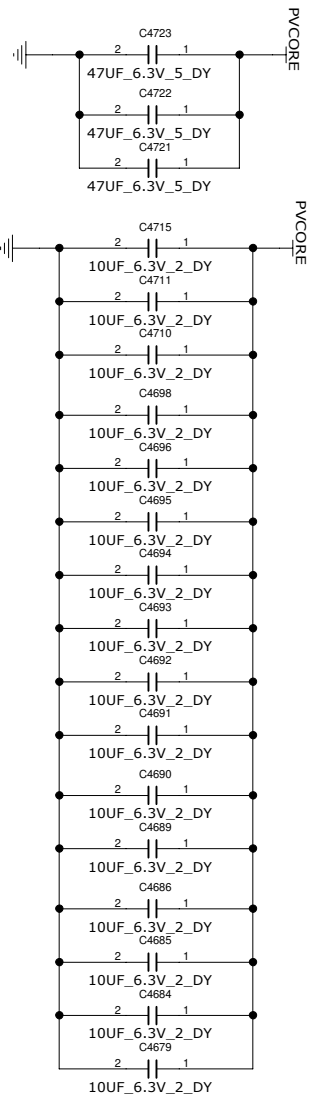
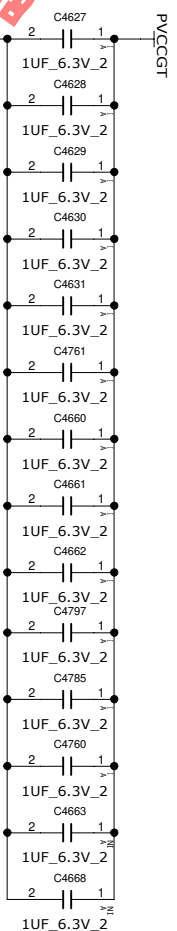
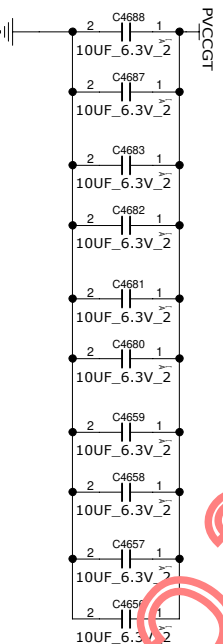
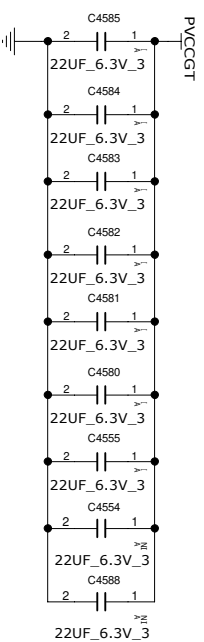


INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
SKYLAKE7_H-POWER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EDS VER0.7
PVC0GT
47UF X 3 22UF X 7
10UF X 10 1UF X 12

PLACE IN TOP SIDE

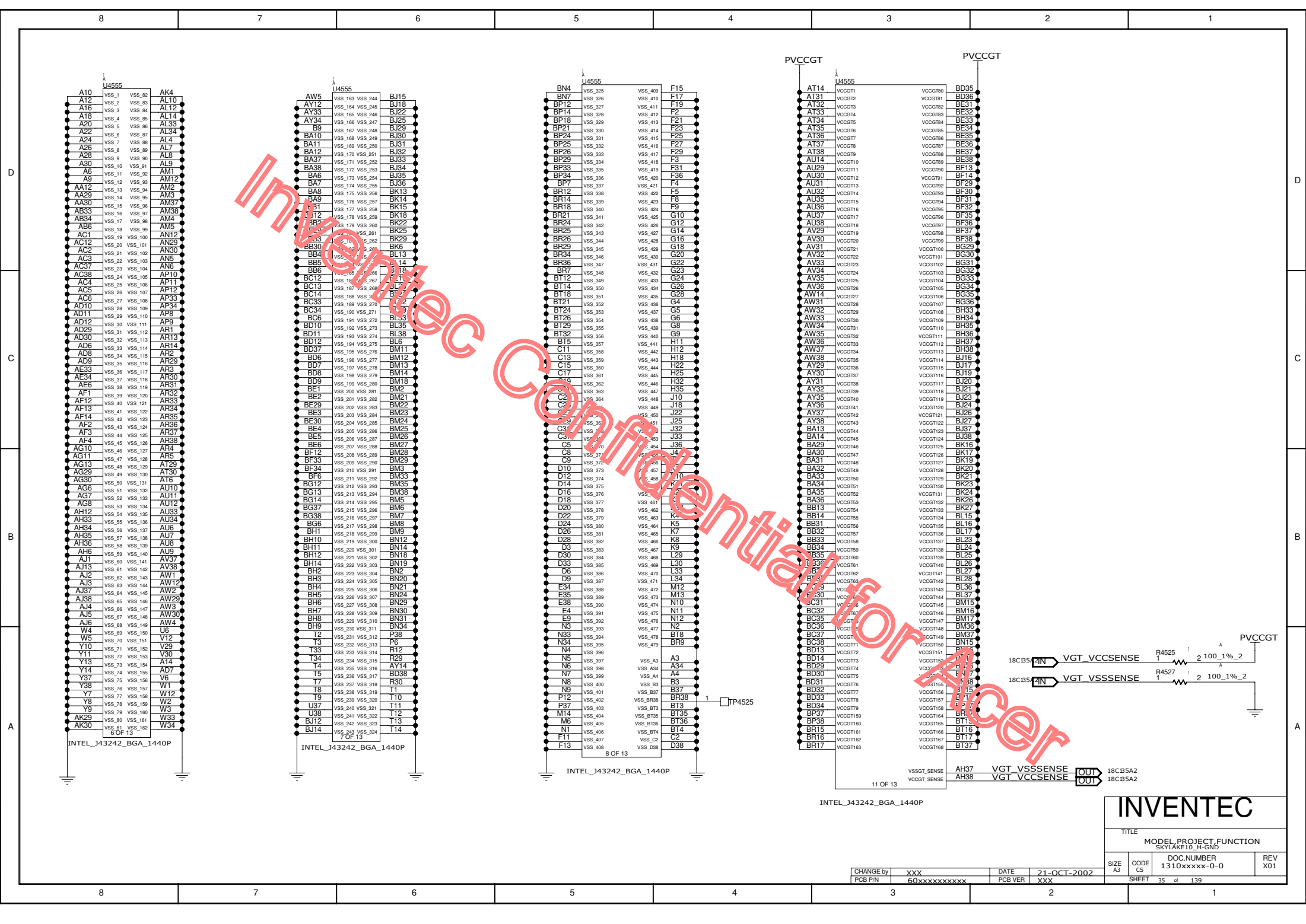


H82 CPU

INVENTEC

CHANGE BY	DATE	PCB VER	REV
XXX	21-OCT-2002	XXX	X01

TITLE	MODEL/PROJECT/FUNCTION	SIZE	CODE	SHEET	34	139
MODEL/PROJECT/FUNCTION	SKETCHES	A3	C5	1310XXXX-0-0		



INVENTEC

TITLE
MODEL PROJECT FUNCTION
SKYLAKE H-G

SIZE CODE
A3 CS

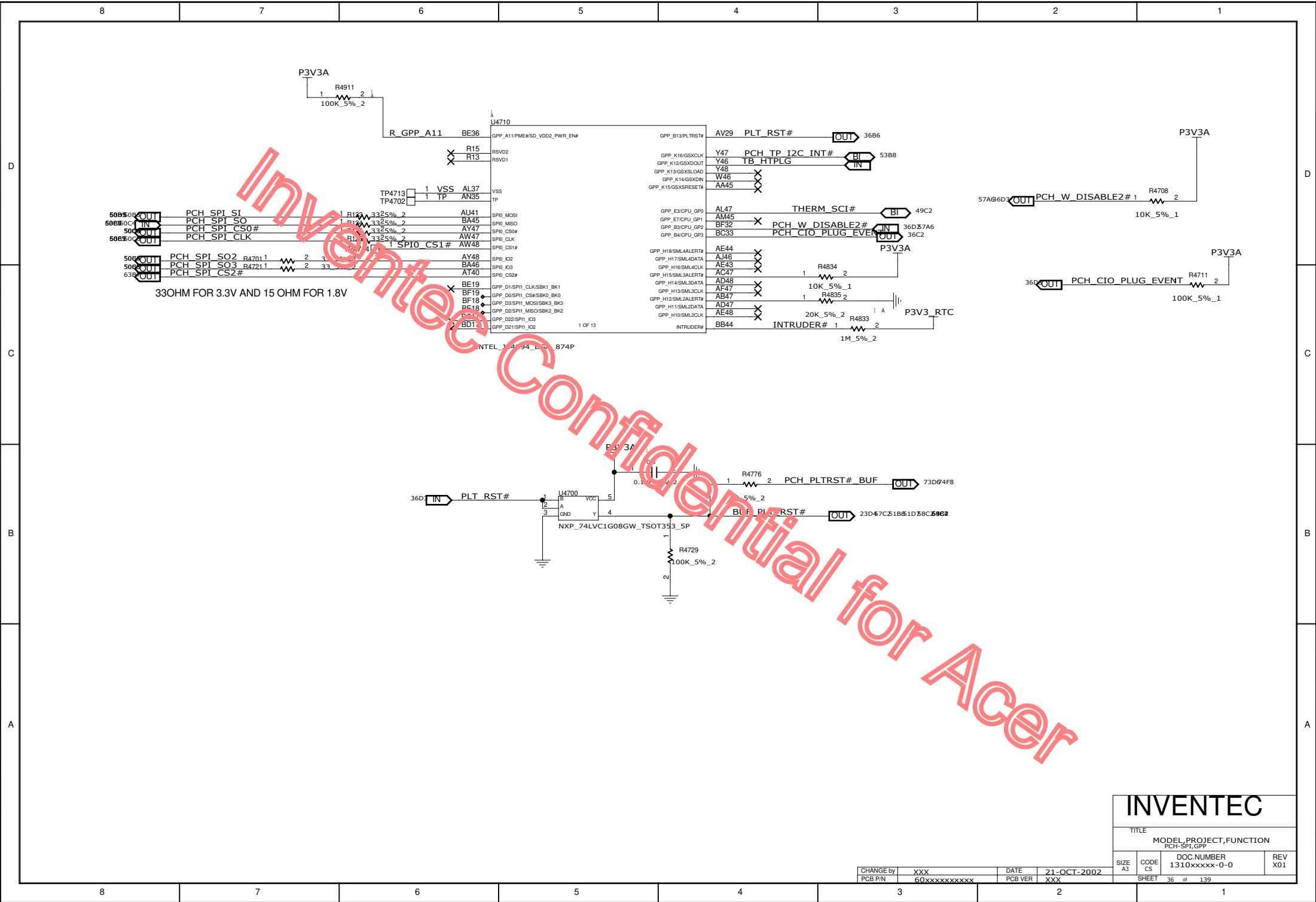
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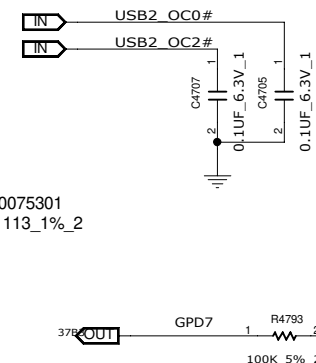
REV
X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

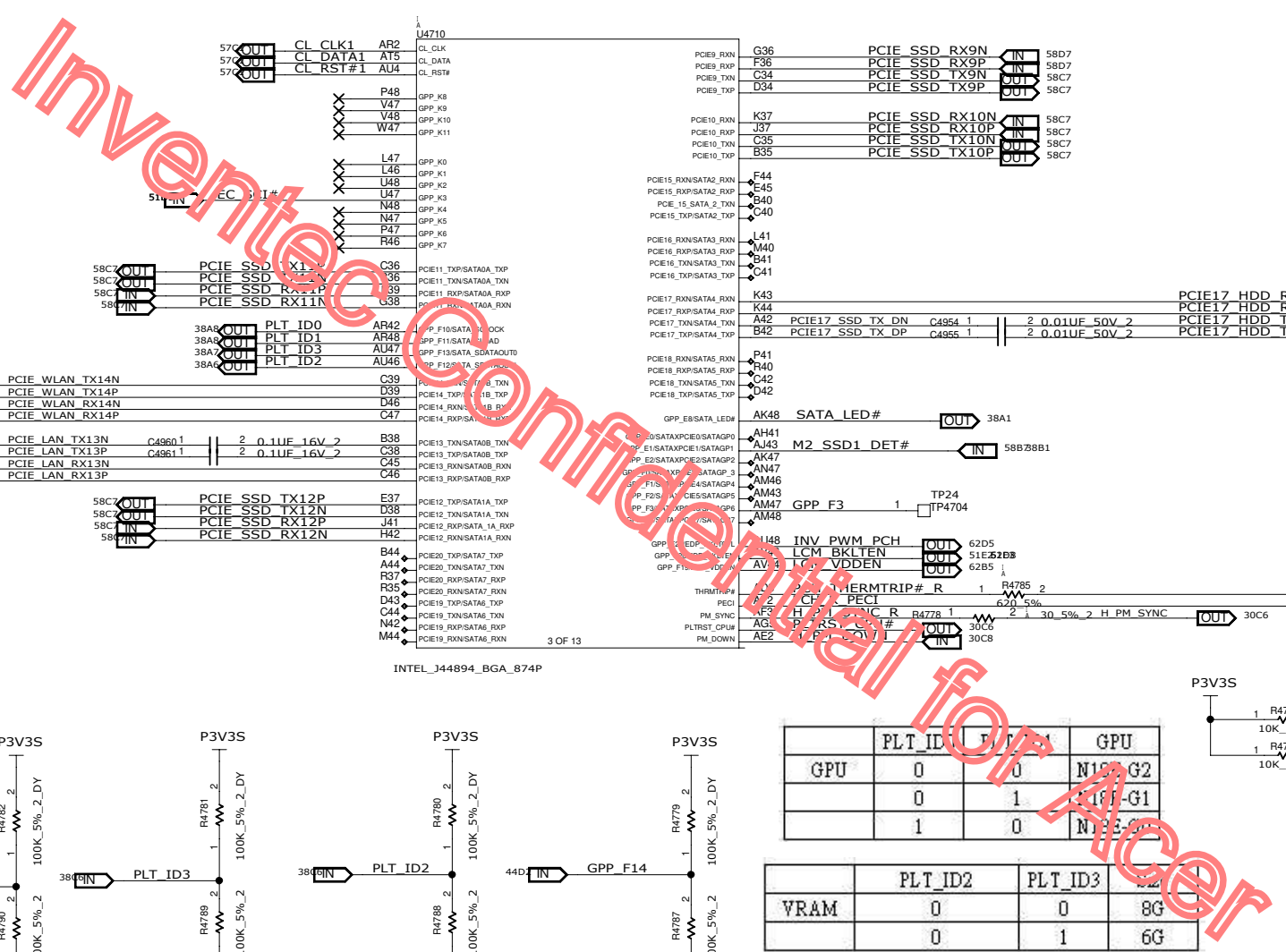
DATE 21-OCT-2002
PCB VER XXX

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SSD2



	PLT_ID1	PLT_ID2	GPU
GPU	0	0	N19 G2
	0	1	N19 G1
	1	0	N19 G0

	PLT_ID2	PLT_ID3	VRAM
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

INVENTEC

TITLEMODEL PROJECT FUNCTIONPCH-CLK/FAN/PCIe/SATA/HOST

SIZE A3CODE CS1310xxxxx-0-0REV X01

CHANGE by XXXDATE 21-OCT-2002PCB P/N 60xxxxxxxxxxPCB VER XXX

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D

C

B

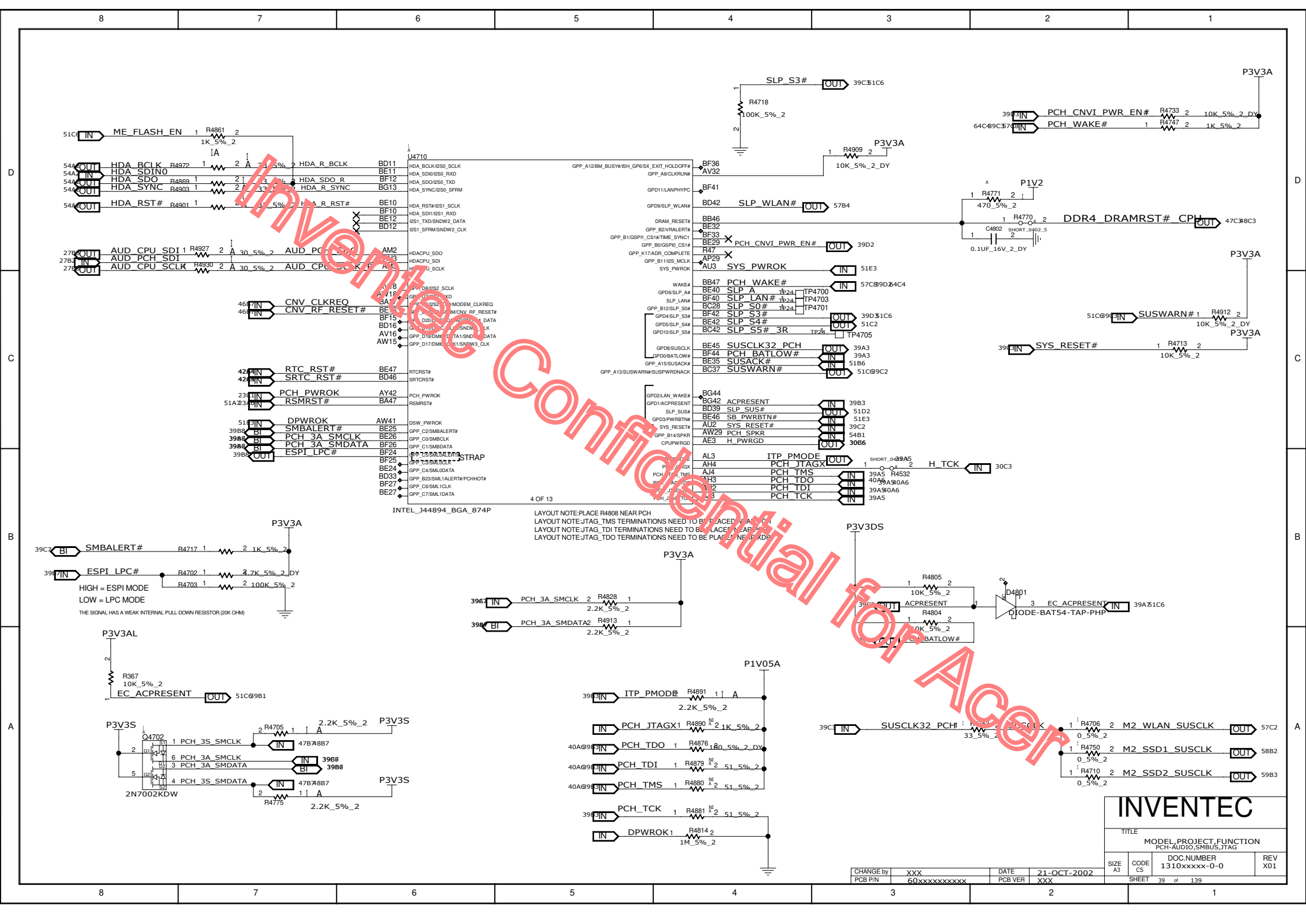
A

D

C

B

A

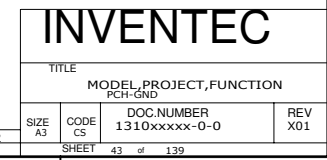


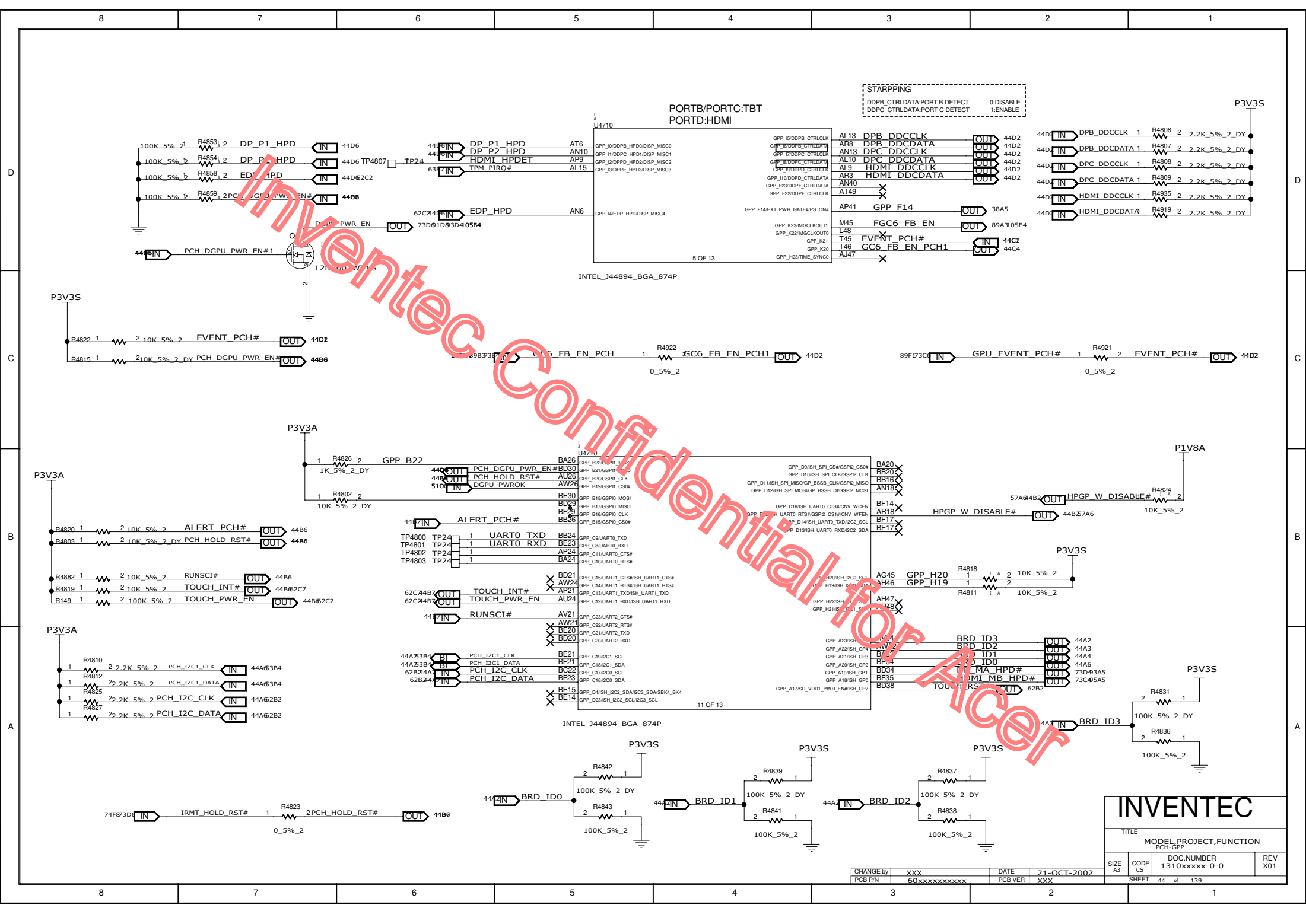
LAYOUT NOTE: PLACE R4808 NEAR PCH
LAYOUT NOTE: JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR PCH

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
PCH AUDIO, SMBUS, JTAG			
SIZE A3		DOC NUMBER	REV
CODE CS		1310xxxxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX





STARPPING

DDPB_CTRLDATA:PORT B DETECT	0:DISABLE
DDPC_CTRLDATA:PORT C DETECT	1:ENABLE

PORTB/PORTC:TBTT
PORTD:HDMI

INTEL_J44894_BGA_874P

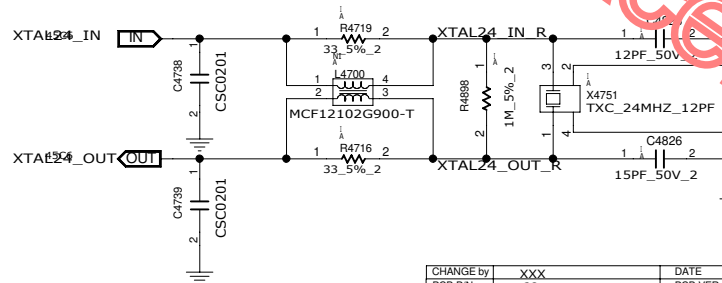
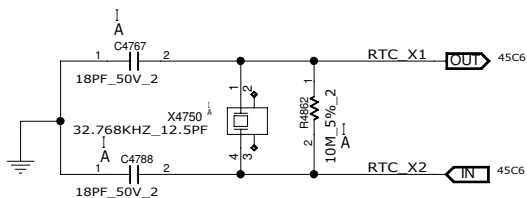
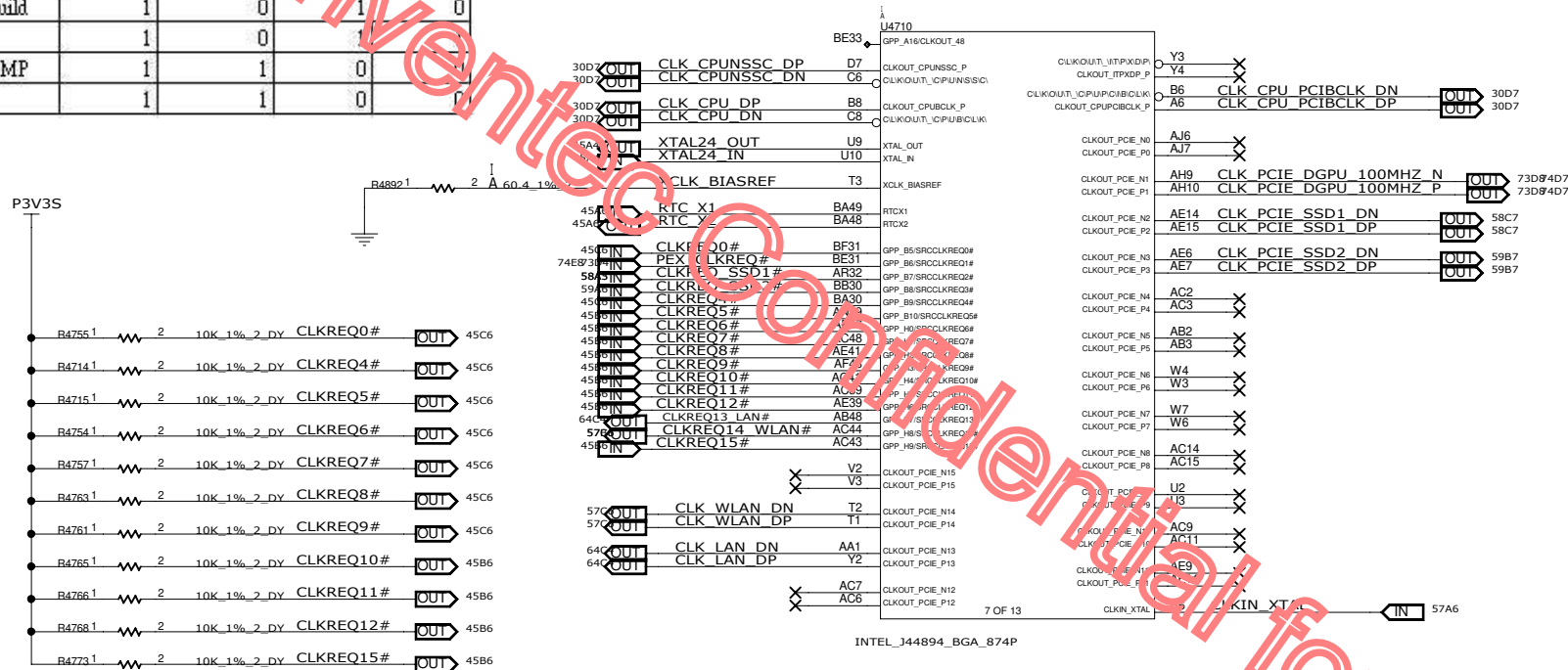
INTEL_J44894_BGA_874P

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
PCH/GPP			
SIZE		DOC NUMBER	
A3		1310xxxxx-0-0	
CODE		REV	
CS		X01	
SHEET		44 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	1	1
D build	1	0	1	0
	1	0		
Pre-MP	1	1	0	
MP	1	1	0	

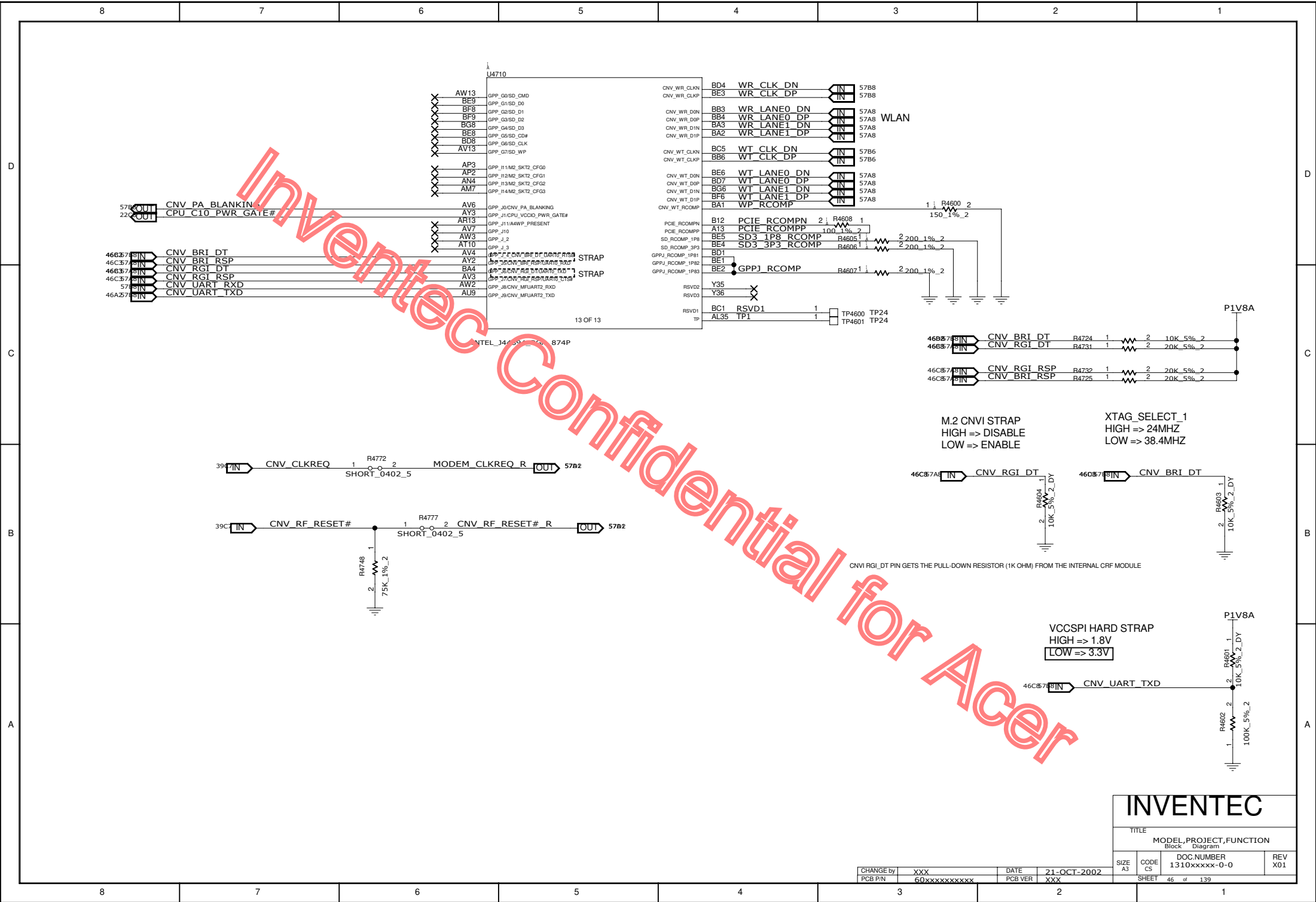
1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
 - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
 - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs



CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

INVENTEC			
TITLE MODEL PROJECT FUNCTION PCH-GPP,CLKOUT			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 45 of 139			



INVENTEC

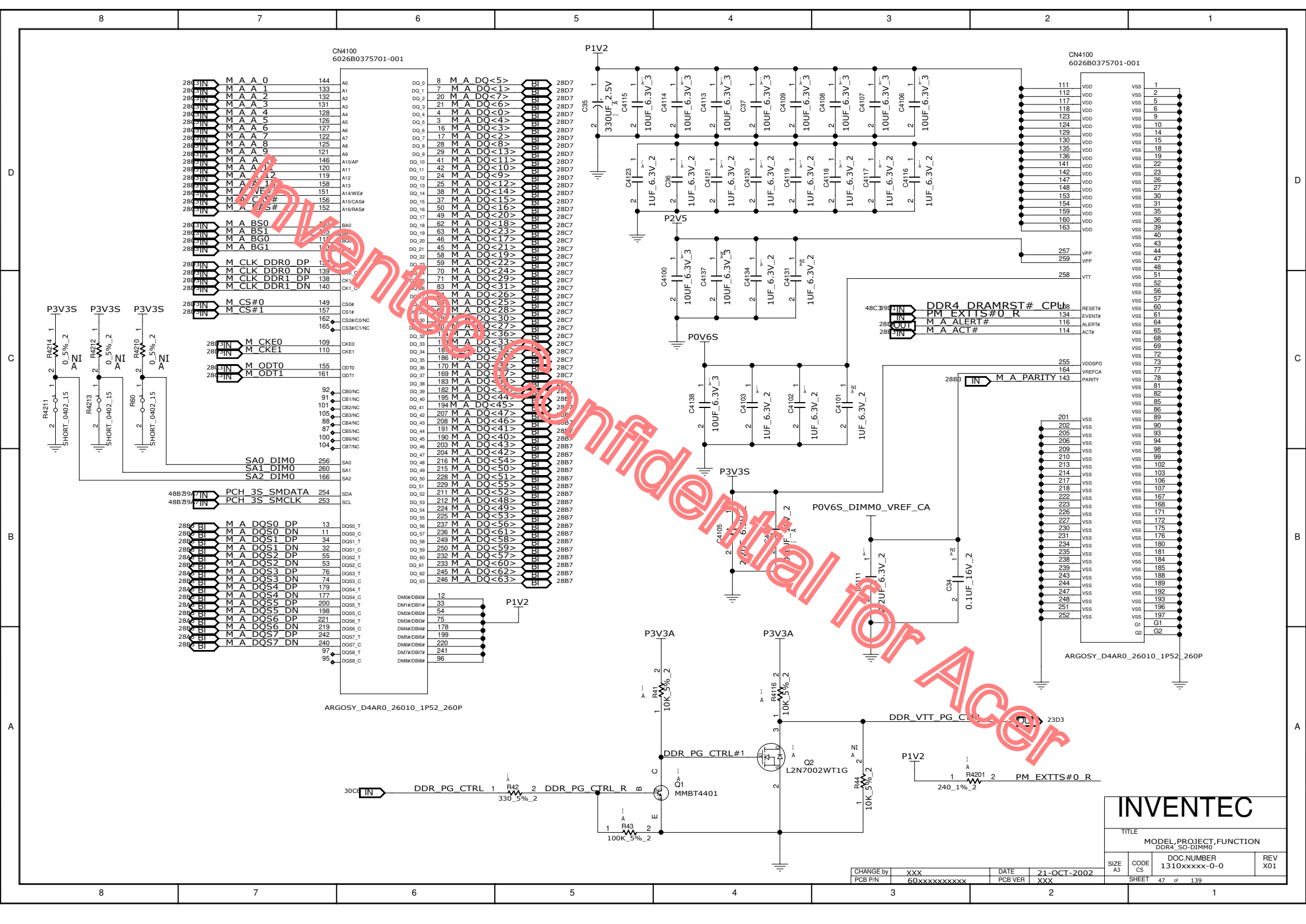
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3
CODE 1310xxxxx-0-0
SHEET 46 of 139

REV X01

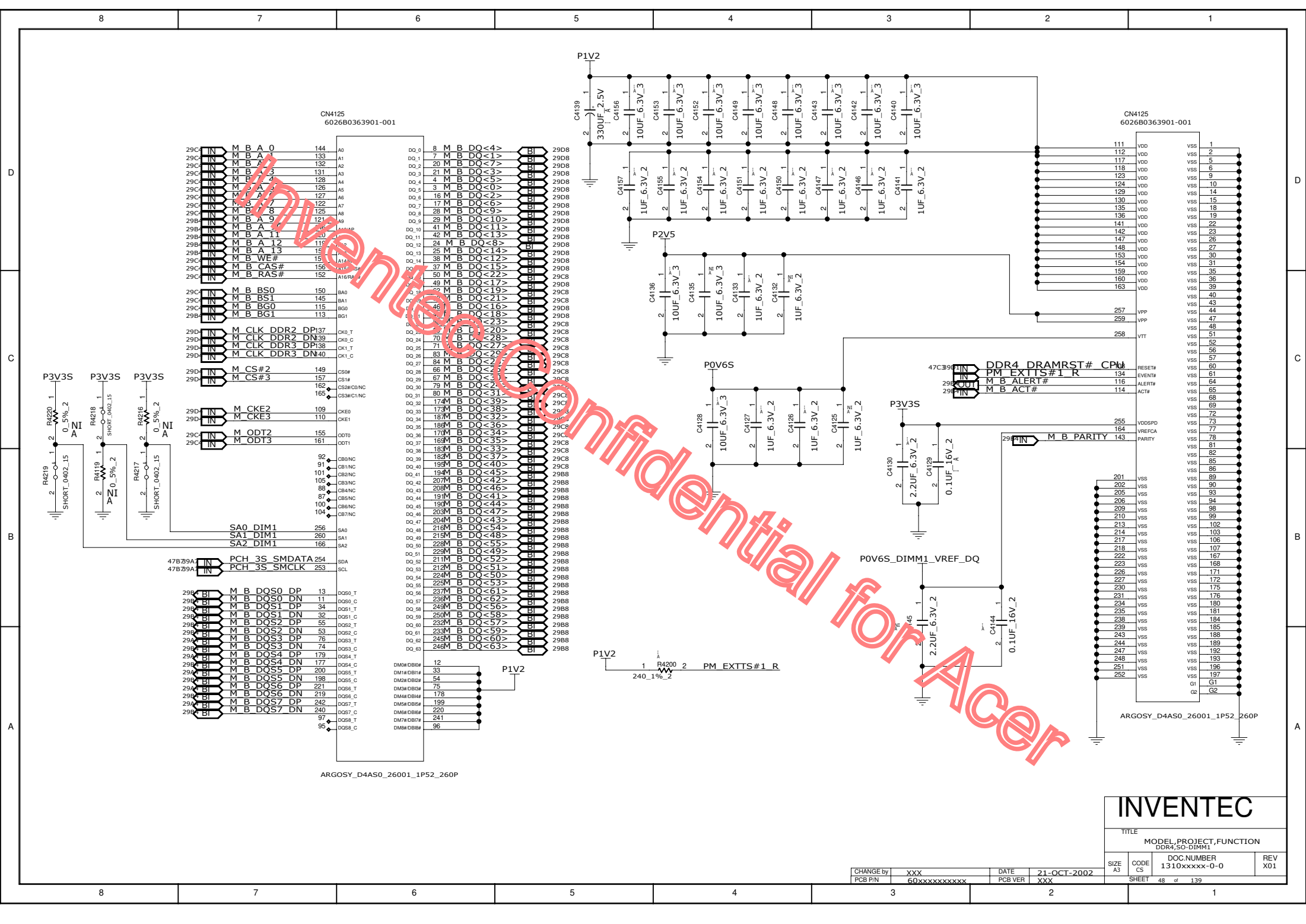
CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX



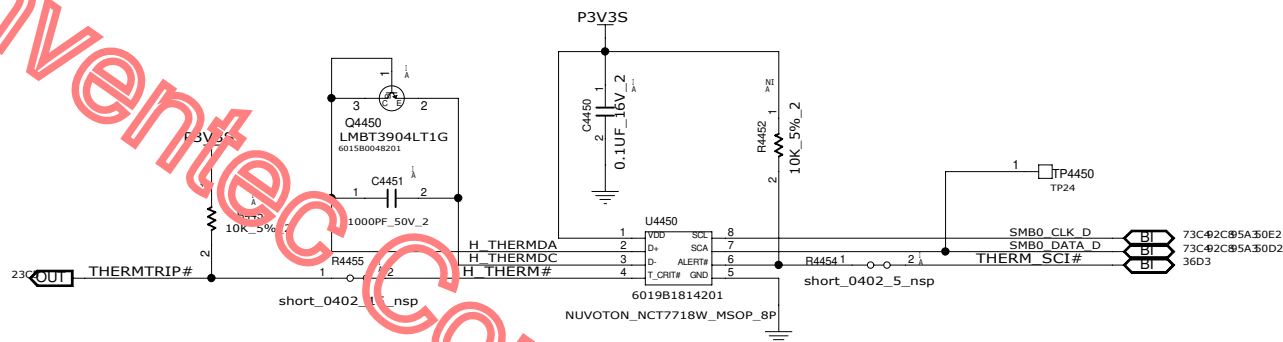
INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION		DDR4 SODIMM	
SIZE A3		DOC NUMBER	REV
CODE CS		1310xxxx-0-0	X01
SHEET		47 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
DDR4,SO DIMM1			
SIZE A3		DOC NUMBER	REV
CODE CS		1310xxxxx-0-0	X01
SHEET		48 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



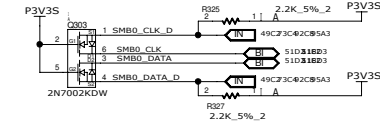
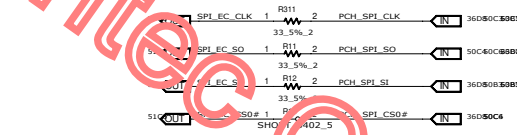
INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

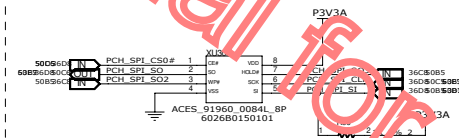
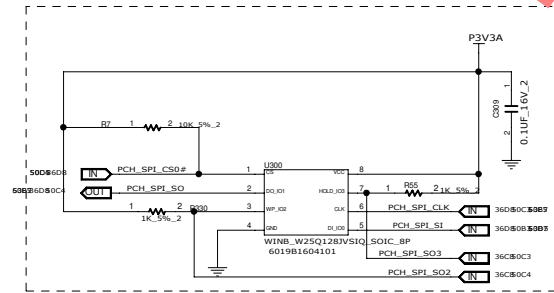
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 49 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

REFERENCE 300~389(KBC)



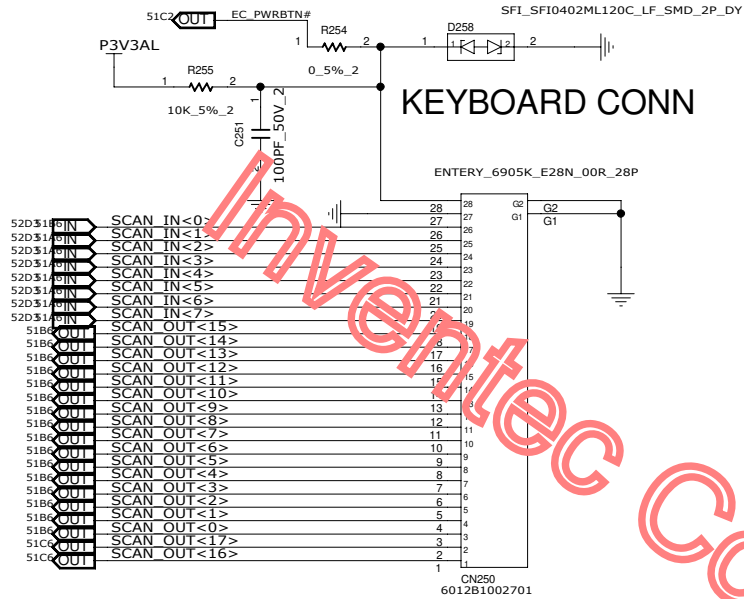
THERMAL SENSOR
HDMI
DP



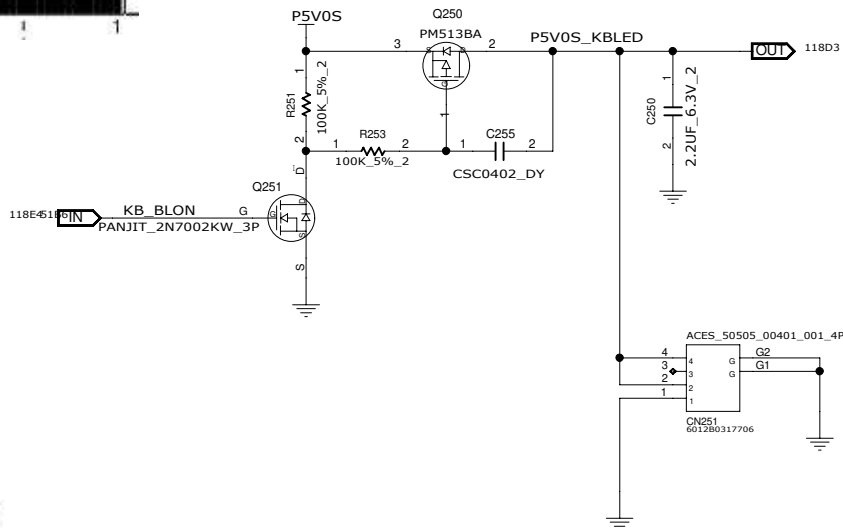
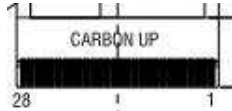
R390 FOR INTEL DEBUG

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
CHANGE D	xxx	DATE	21-OCT-2002
PCH P/N	60xxxxxxx	PCB VER	xxx
SIZE A3	CODE CS	DOC NUMBER	1310xxxxx-0-0
SHEET	50	of	139
		REV	X01

REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



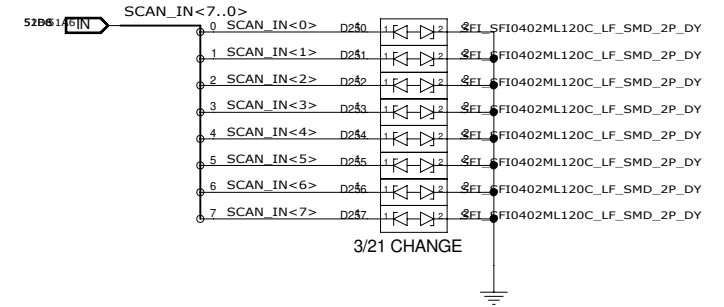
NEE TO CHANGE 6012B1002701
5/2 REVERSE



VCC : 45V
LED W : 2.9~3.5V

	Min(LED W : 3.5V)	Max(LED W : 2.9V)
Power consumption	228.71mA	320.2mA

	14*
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



INVENTEC

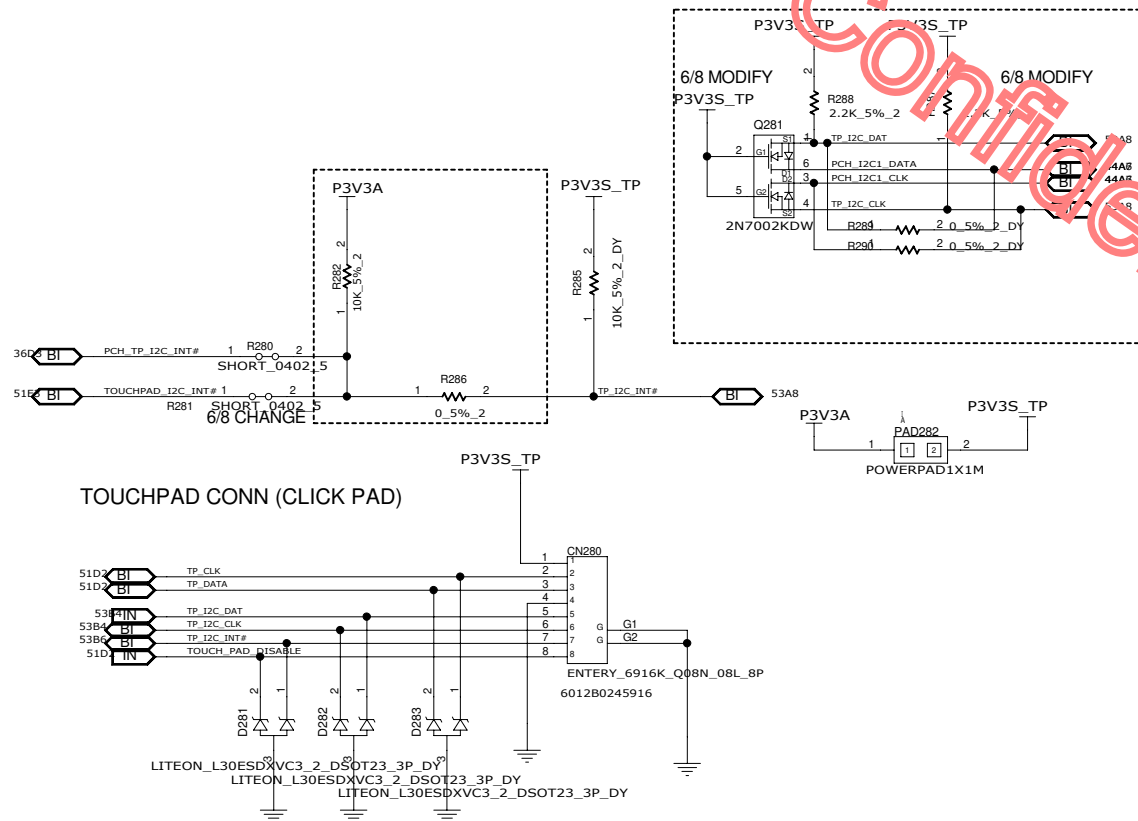
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS 1310xxxx-0-0 REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

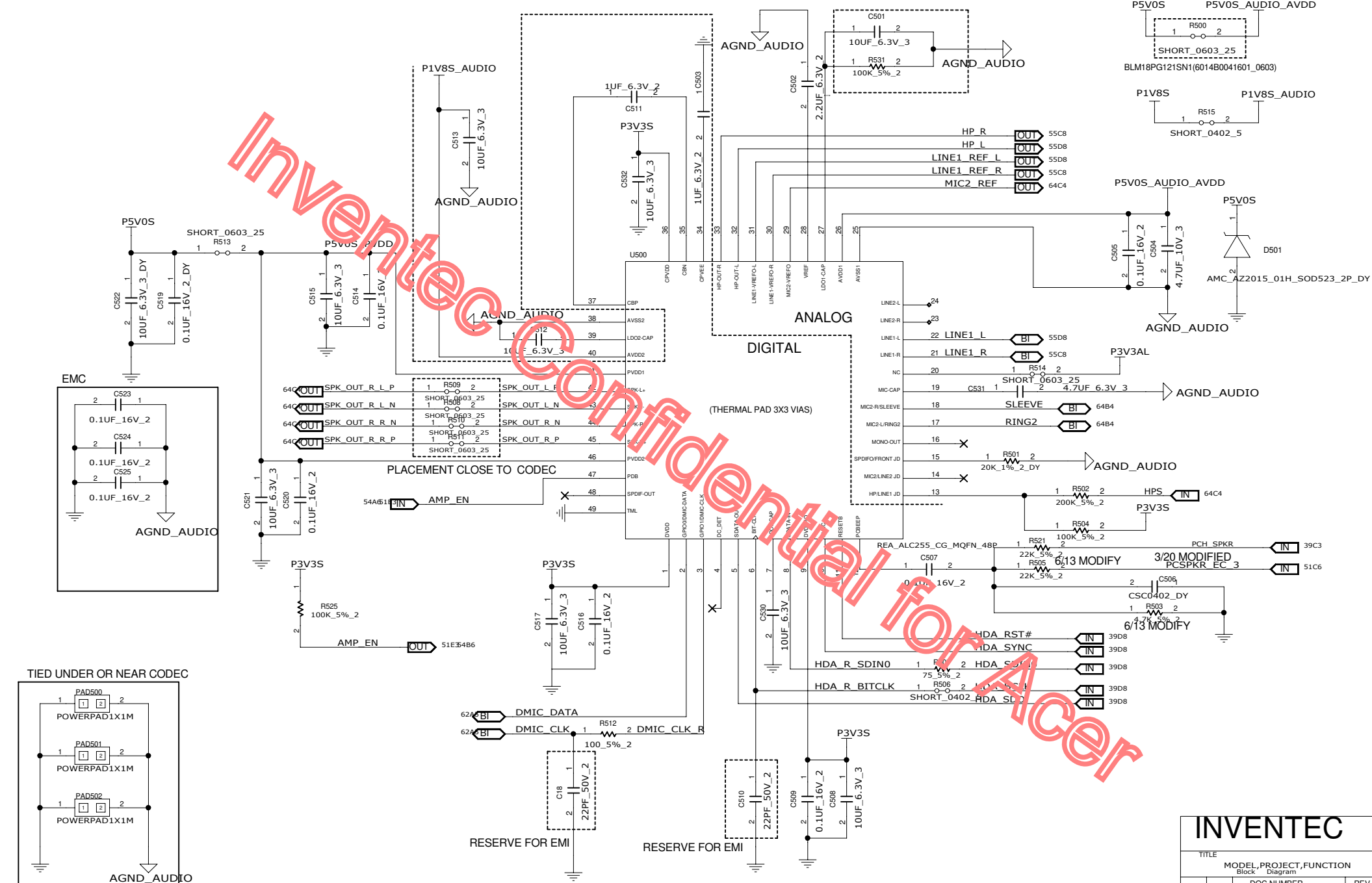
SHEET 52 of 139



CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		SHEET	53 of 139	

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 53 of 139			

REFERENCE 500~549(AUDIO CODEC)

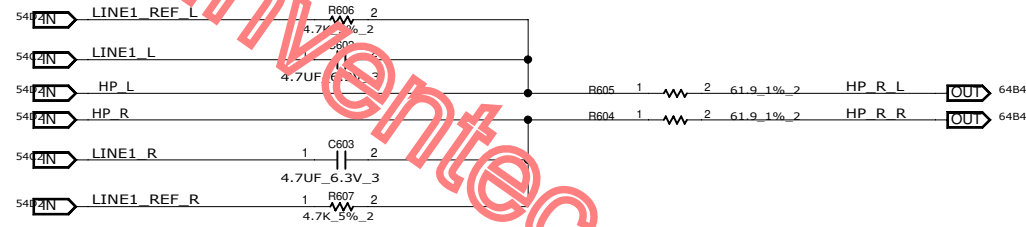


INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 54 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

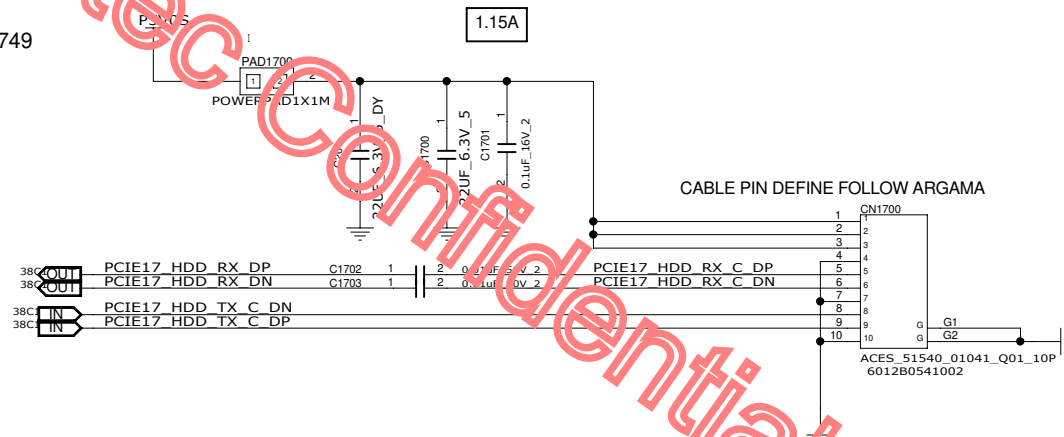
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 55 of 139

SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749

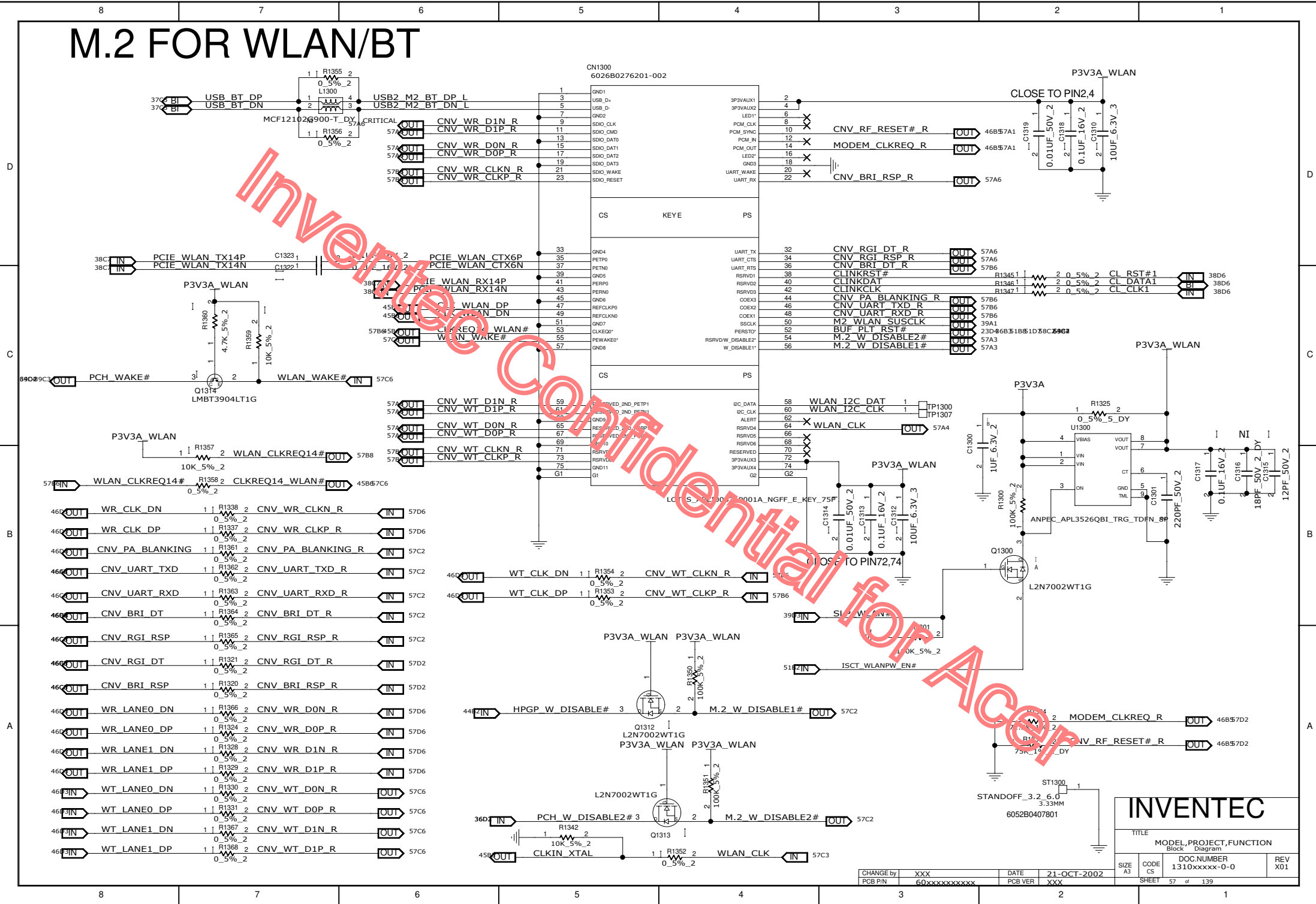


INVENTEC

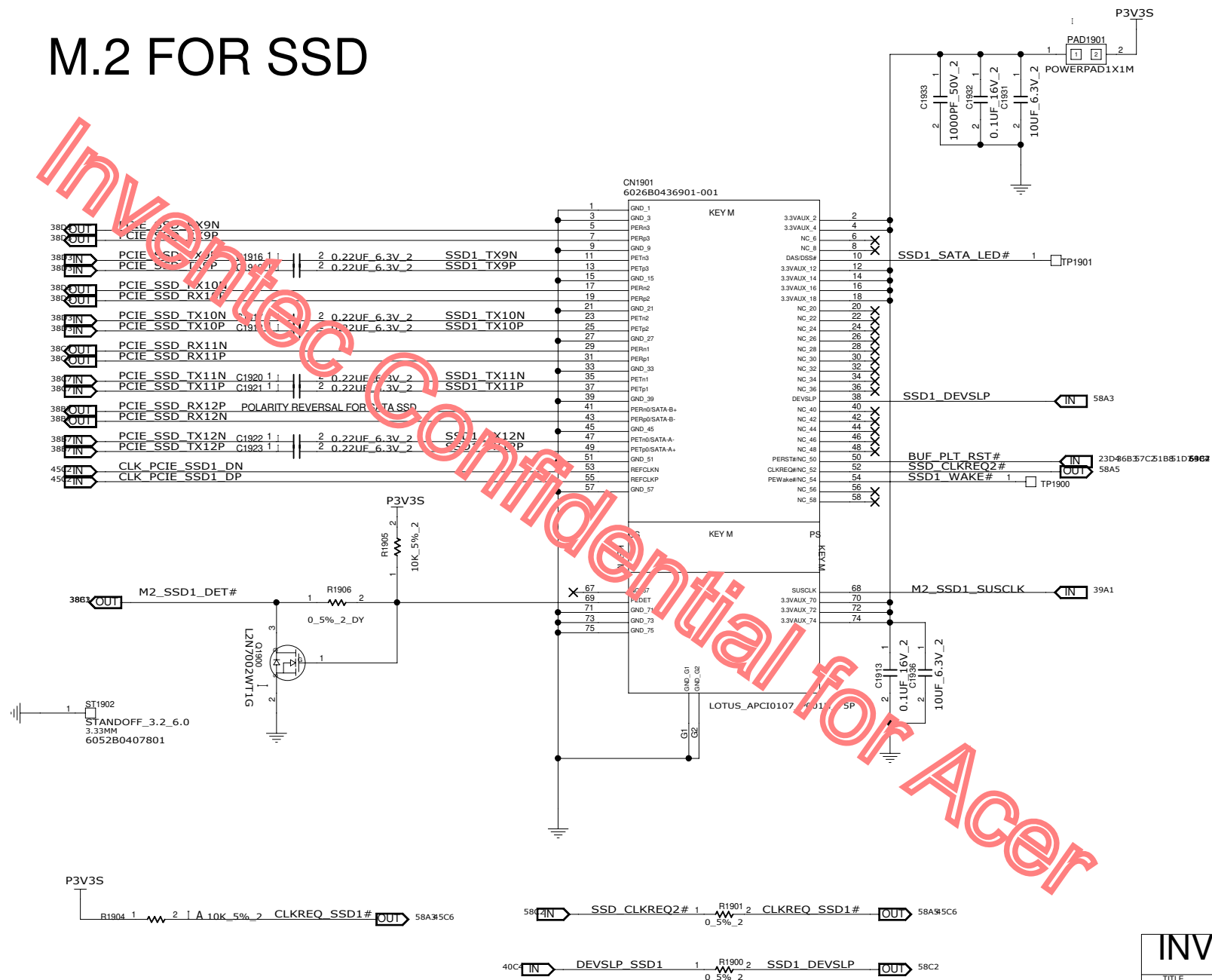
TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 56 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



M.2 FOR SSD



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 58 of 139			

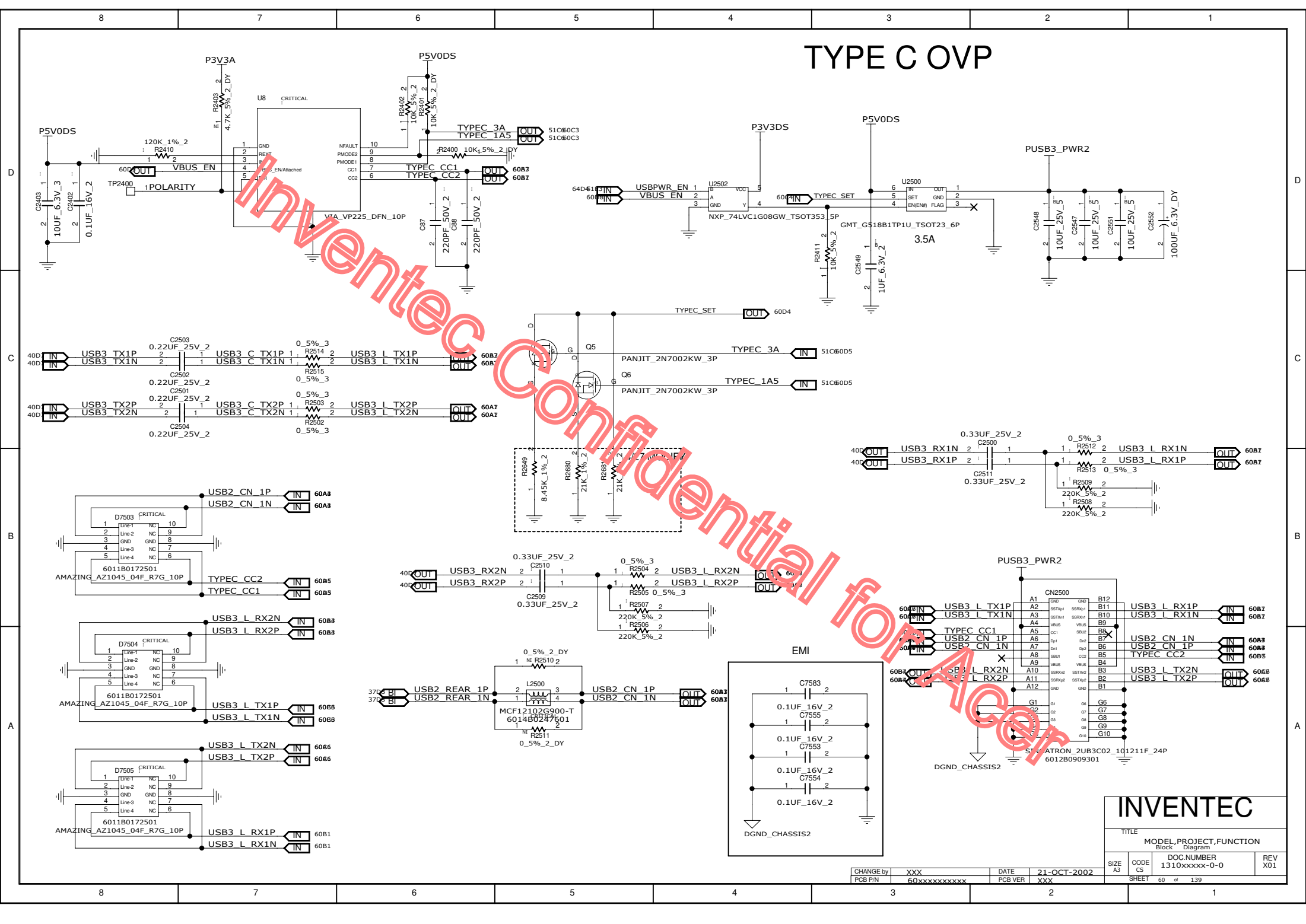
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
----------------------	----------------------	-----------------	--------------------

The schematic diagram illustrates the electrical connections for the SSD2 SATA LED# and SSD2 WAKE# signals. The central component is the CN1900 6026B0436901-001, which is connected to the SSD2 SATA LED# signal via the ITP1902 component. The SSD2 WAKE# signal is connected to the ITP1903 component. The diagram also shows the connection of the SSD2 WAKE# signal to the ITP1903 component. The diagram includes a large red watermark 'Inventec Confidential for Acer'.

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION SATA HDD CONN.			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 59 of 139			

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET	59	of	139

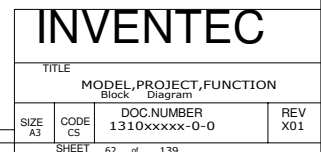
TYPE C OVP



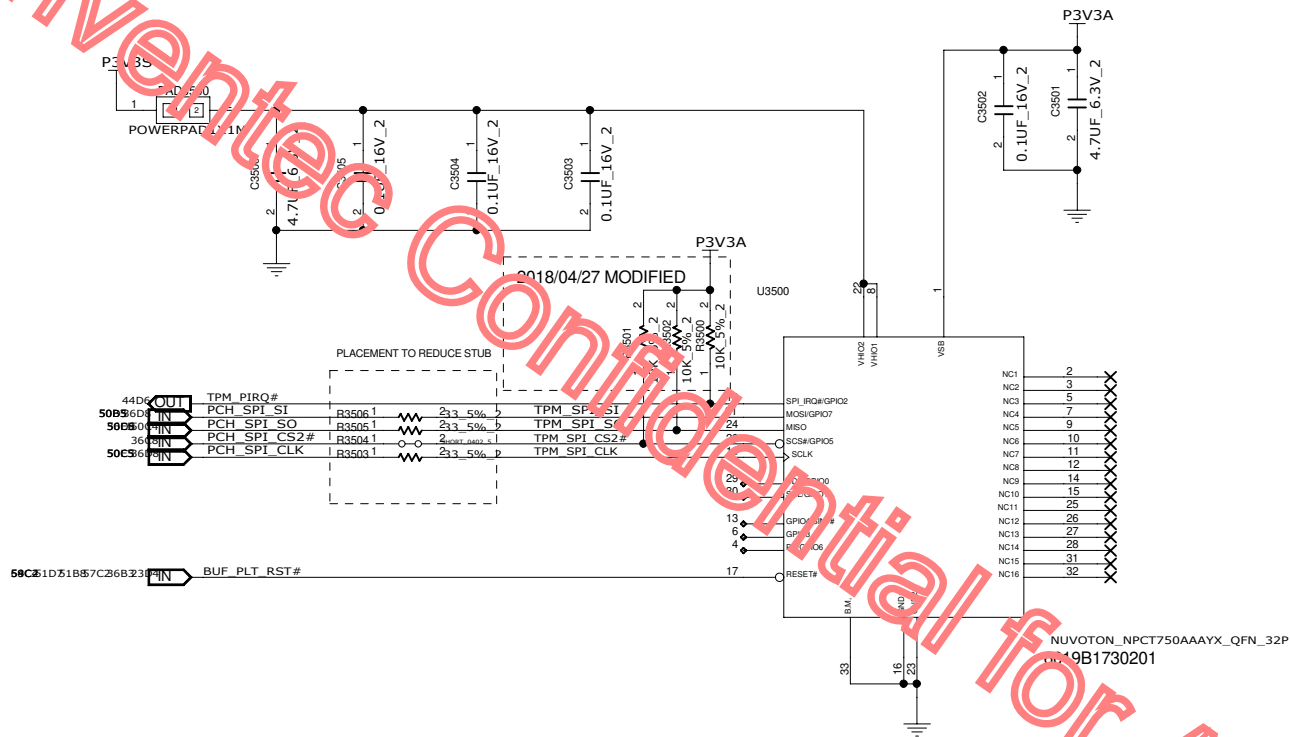
CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxx	PCB VER	XXX	SHEET	60	of	139				

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

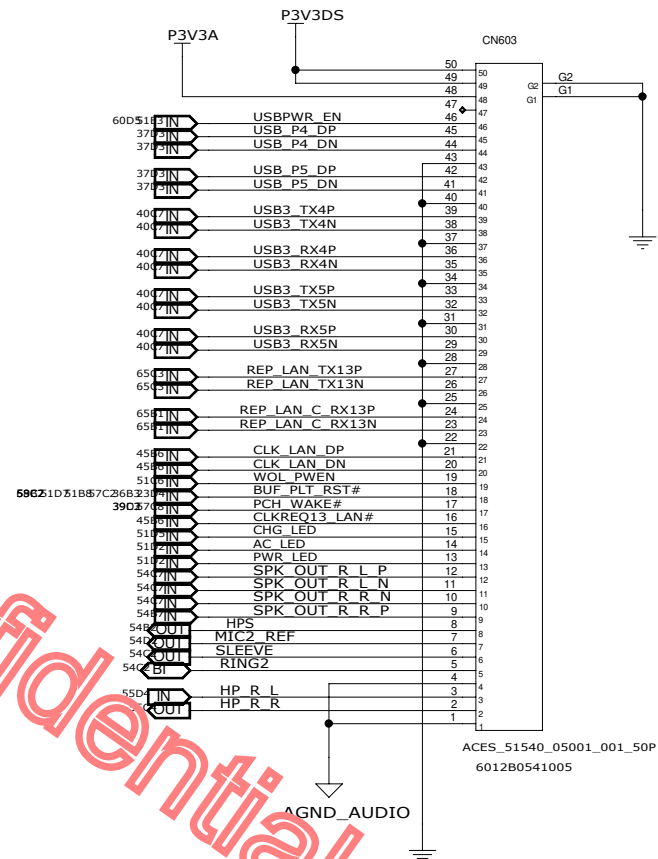
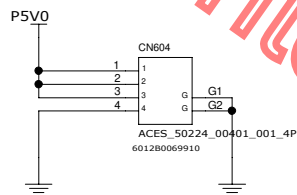


Inventory Confidential for Acer



INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		63 of 139	1	

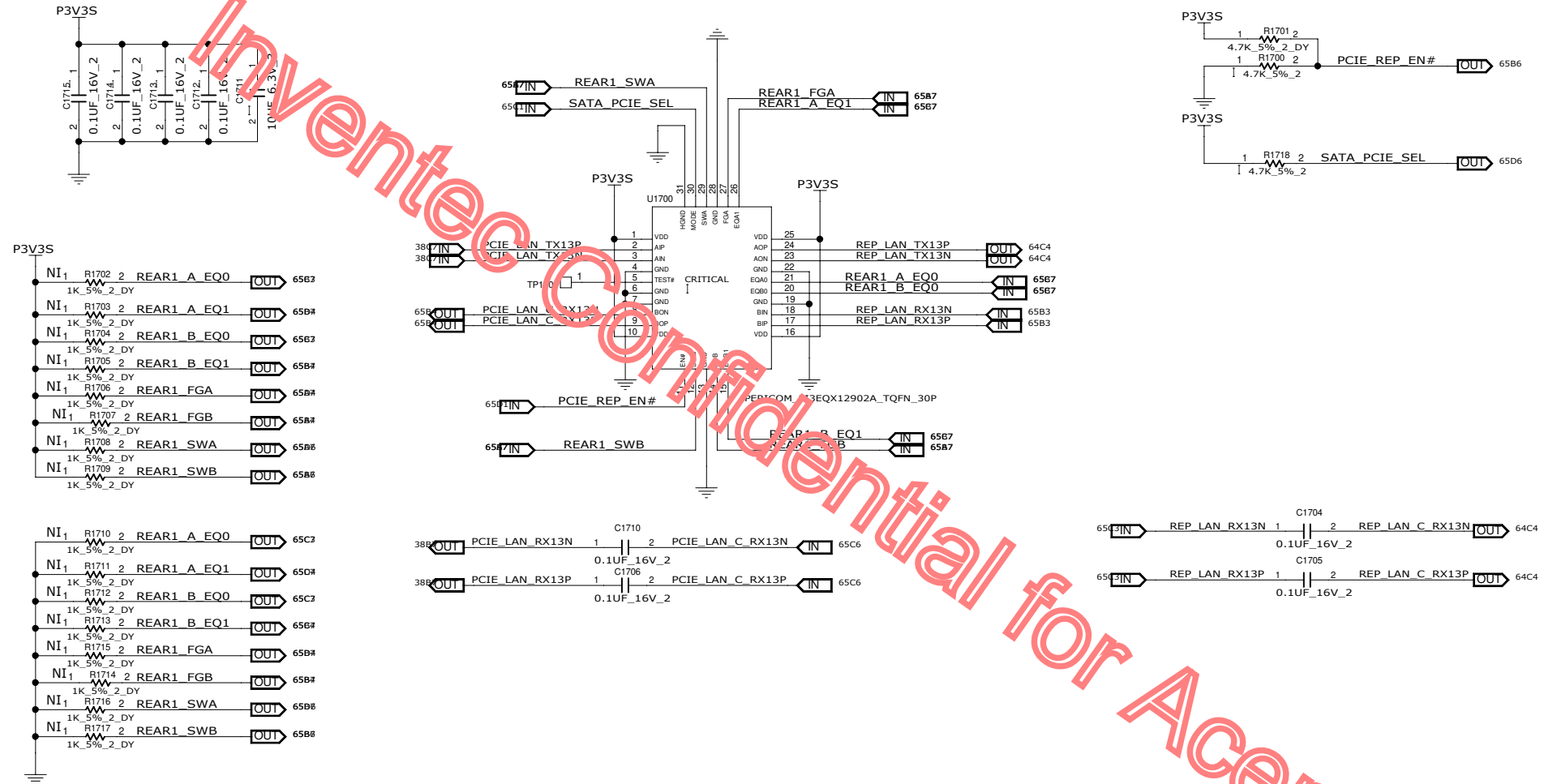
Inventec Confidential for Acer



ACES_51540_05001_001_50P
6012B0541005

INVENTEC				
TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX	SHEET 64 of 139

PCIE REPEATER



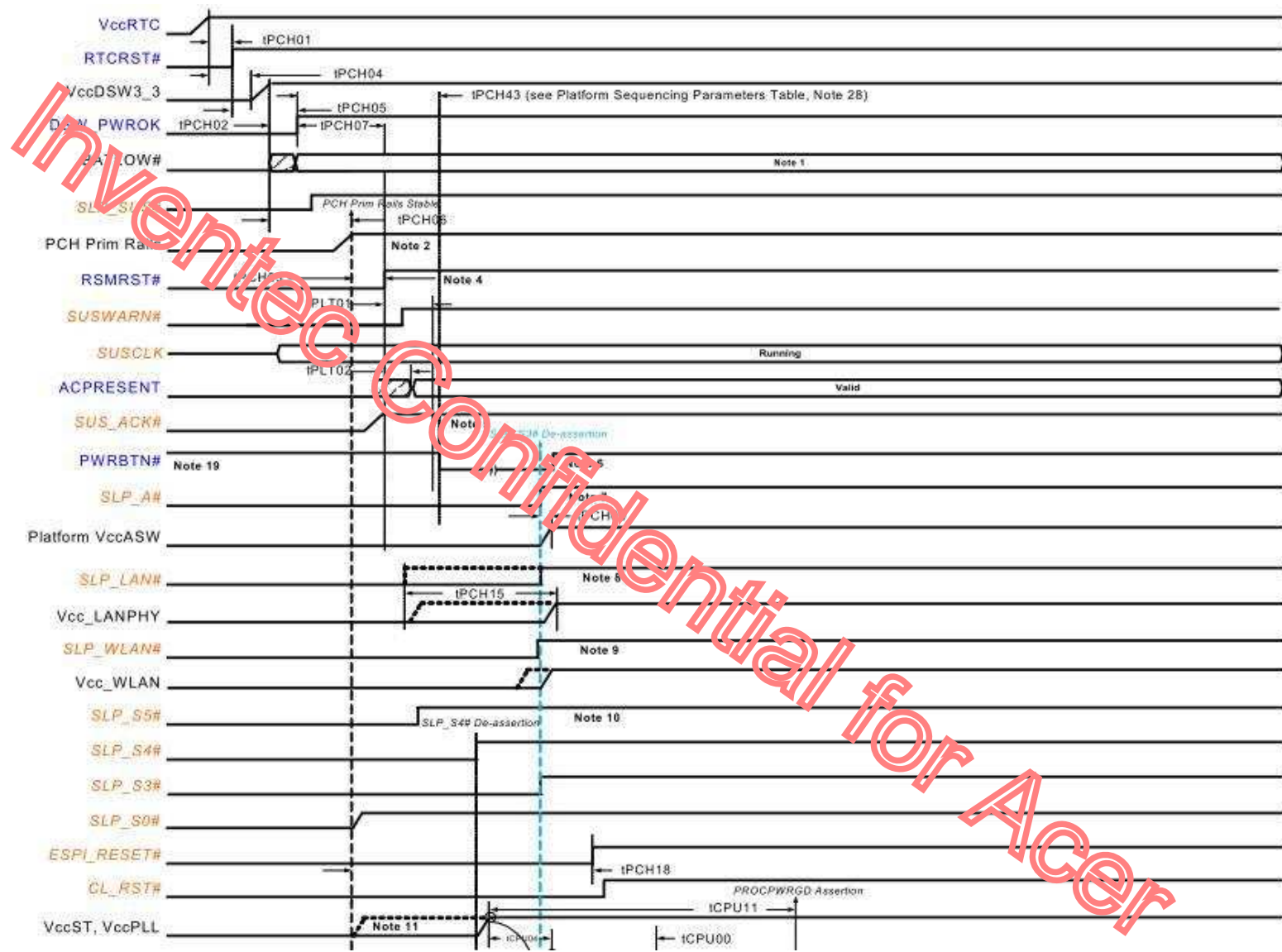
INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

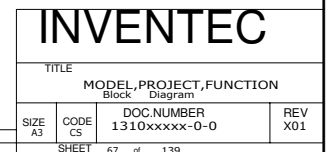
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SHEET 65 of 139



INVENTEC			
TITLE MODEL PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
60xxxxxxxxxx		SHEET 66 of 139	



8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 68 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 69 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 70 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

N18E-G0
N18E-G1
N18E-G2 MAX-Q
8GB DDR5 256M X 16 X 2 X6

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 71 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

PCA CODE NAME : N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001

G1 : 6019B1849201

G2 MAXQ:6019B1849301

PCB VERSION : X01

BOARD SIZE:

SCH P/N:

PCB P/N:

PCA P/N:

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL

NI: NON-INSTALL

DY: NON-INSTALL

MP: PRODUCTION

PROTO: PRE-PRODUCTION

CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14

6019B1847701

MICRON MT61K256M32JE-14:A

6019B1847701

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MONITOR BOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (MP86941_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (MP86941_1P)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (R18158A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOs	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
93	GPU DP CONNECTOR	123	
94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OV-R	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	72	of	139				

CONNECTION TO MAINBOARD

D

C

B

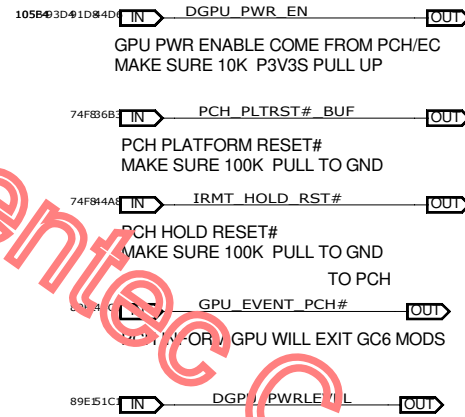
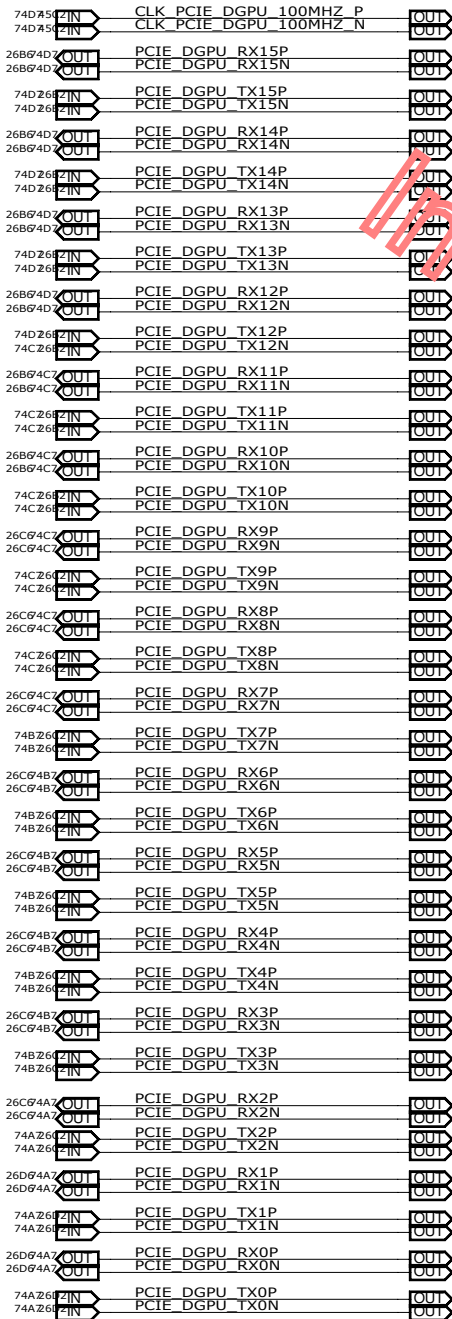
A

D

C

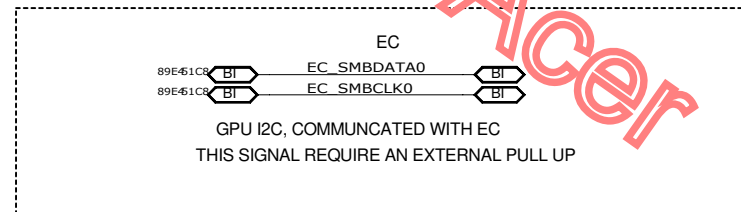
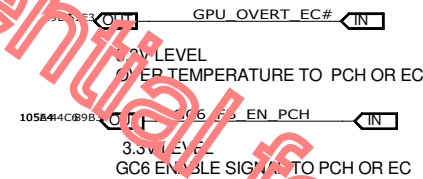
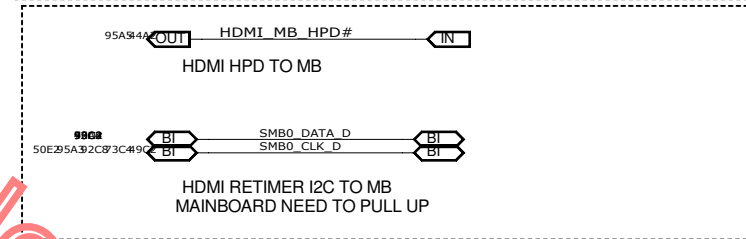
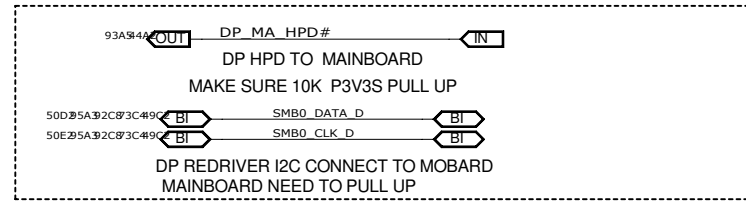
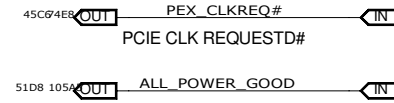
B

A



15.3.2 PWR_LEVEL* (GPIO12)

The **PWR_LEVEL** input signal triggers an immediate low-to-high or slow-to-high transition followed by the driver capping the GPU power state to the appropriate limit. There are a few events that can trigger this signal assertion: AC to battery power transition, total system power overdraw event.

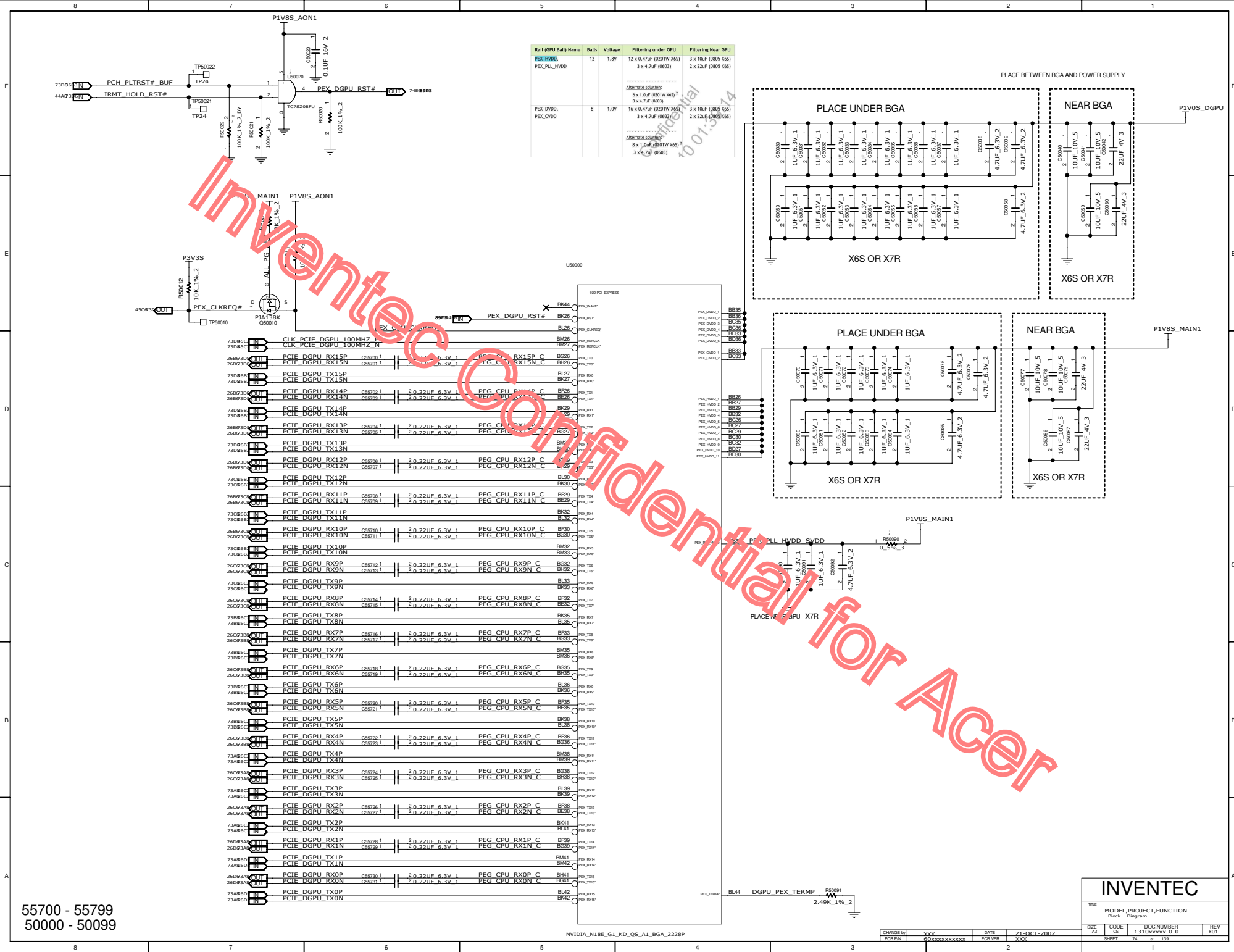


INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 73	of 139		

CHANGE by XXX	DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx	PCB VER XXX

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD, PEX_PL_HVDD	12	1.8V	12 x 0.47uF (0201W X65) 3 x 4.7uF (0603)	3 x 10uF (0805 X65) 2 x 22uF (0805 X65)
PEX_DVDD, PEX_CVDD	8	1.0V	16 x 0.47uF (0201W X65) 3 x 4.7uF (0603) Alternate solution: 8 x 1.0uF (0201W X65) 3 x 4.7uF (0603)	3 x 10uF (0805 X65) 2 x 22uF (0805 X65)



55700 - 55799
50000 - 50099

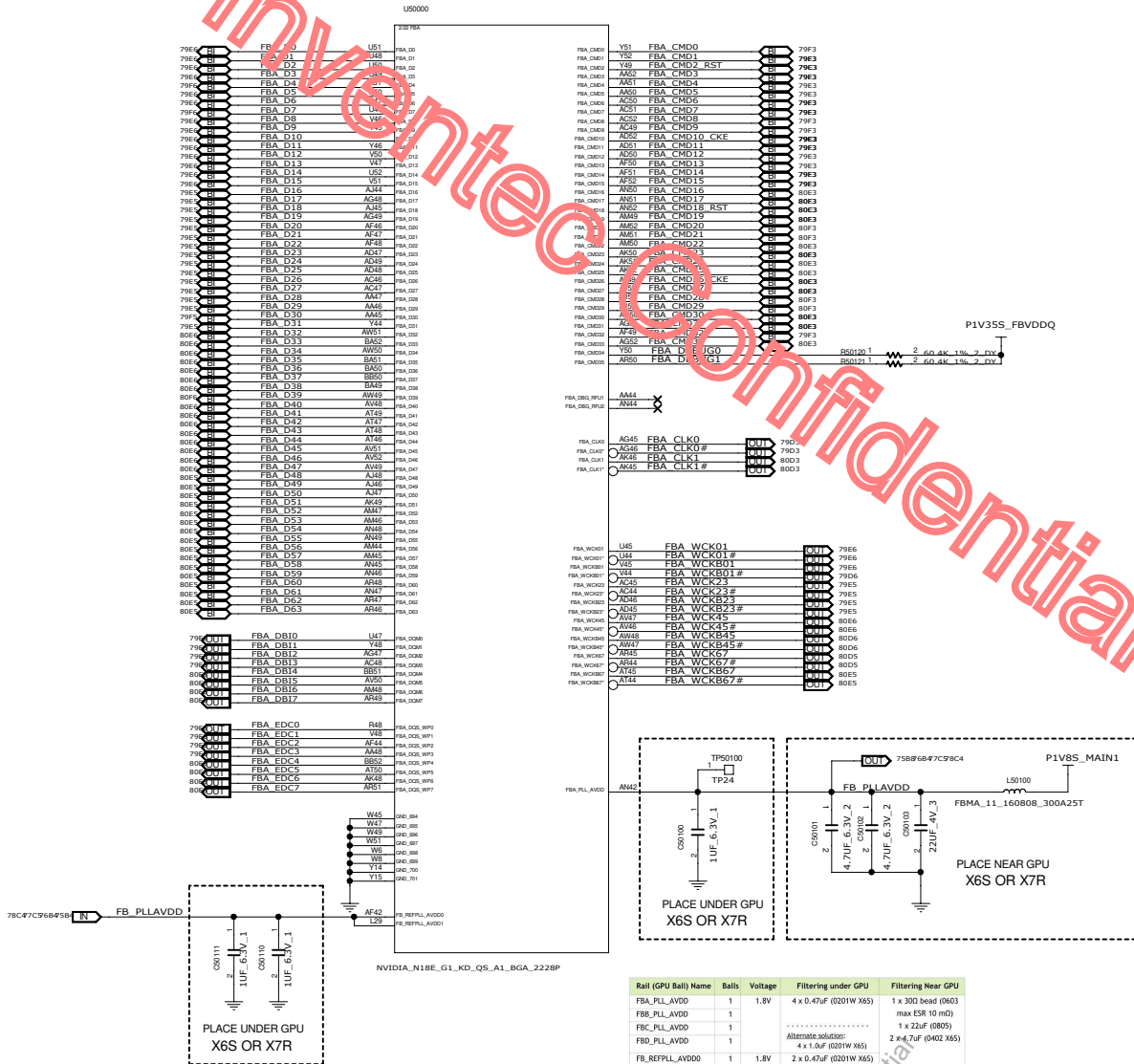
NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

CHANGE D	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310XXXX-0-0	REV X01
SHEET 24		139	

GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1			2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1			2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	

50100 - 50199

INVENTEC

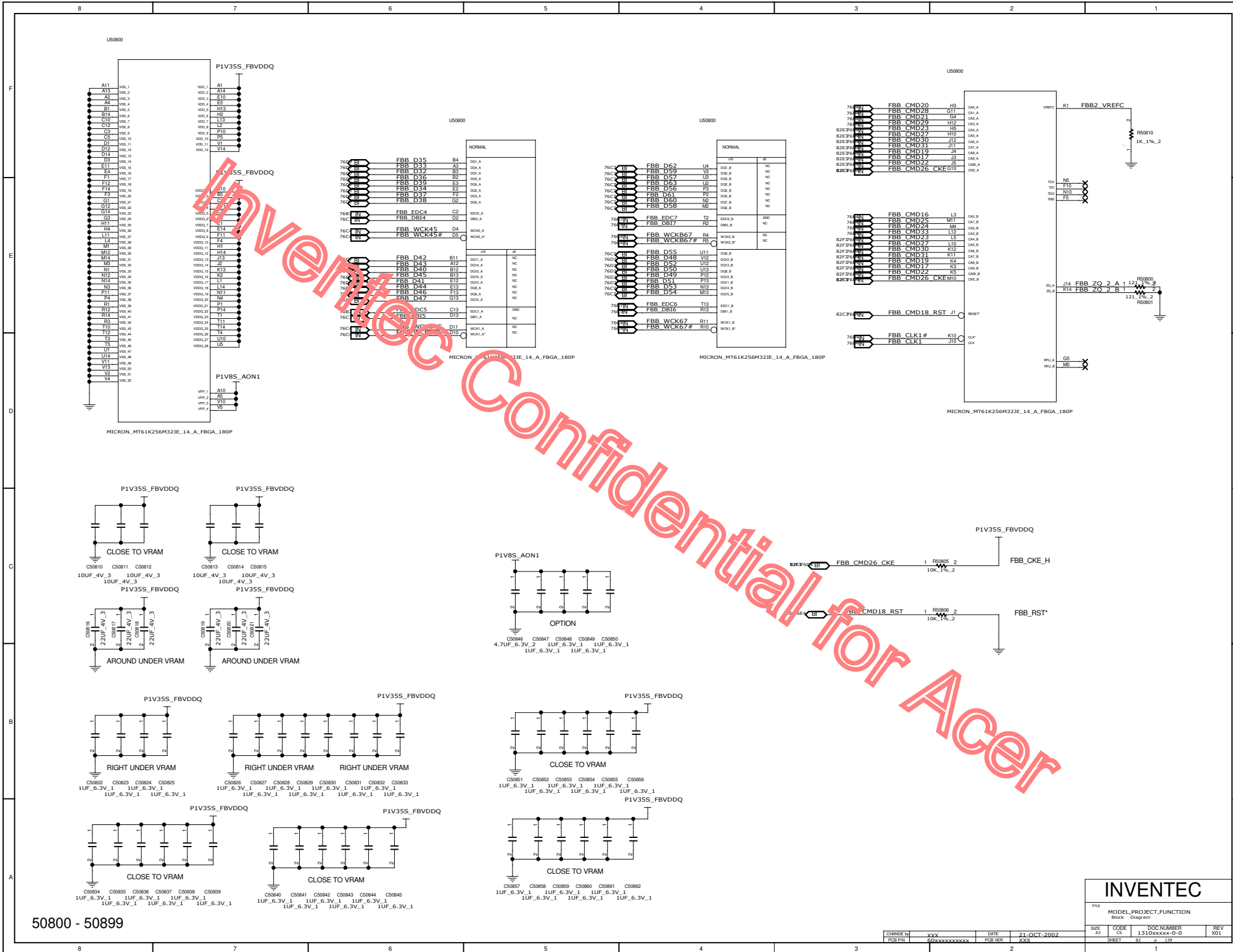
MODEL, PROJECT, FUNCTION			
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SHEET	75	of 139	1

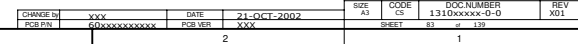
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PCB P/N	60xxxxxxx	PCB VER	XXX

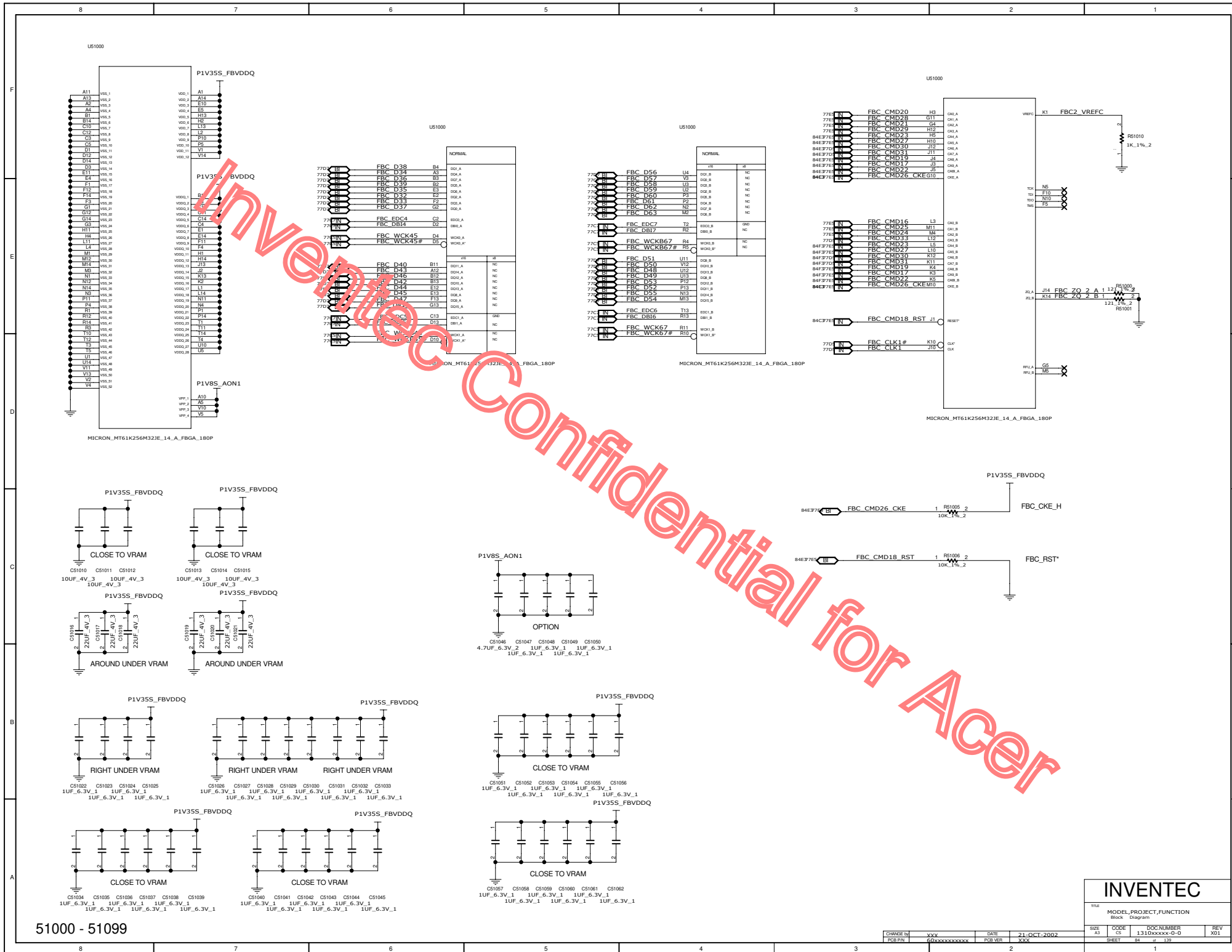
A	B	C	D	E	F
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[illegible]

[illegible][illegible]







27 MHZ XTAL

$$CL = 2 \cdot 10 - (5 + 3) = 12$$

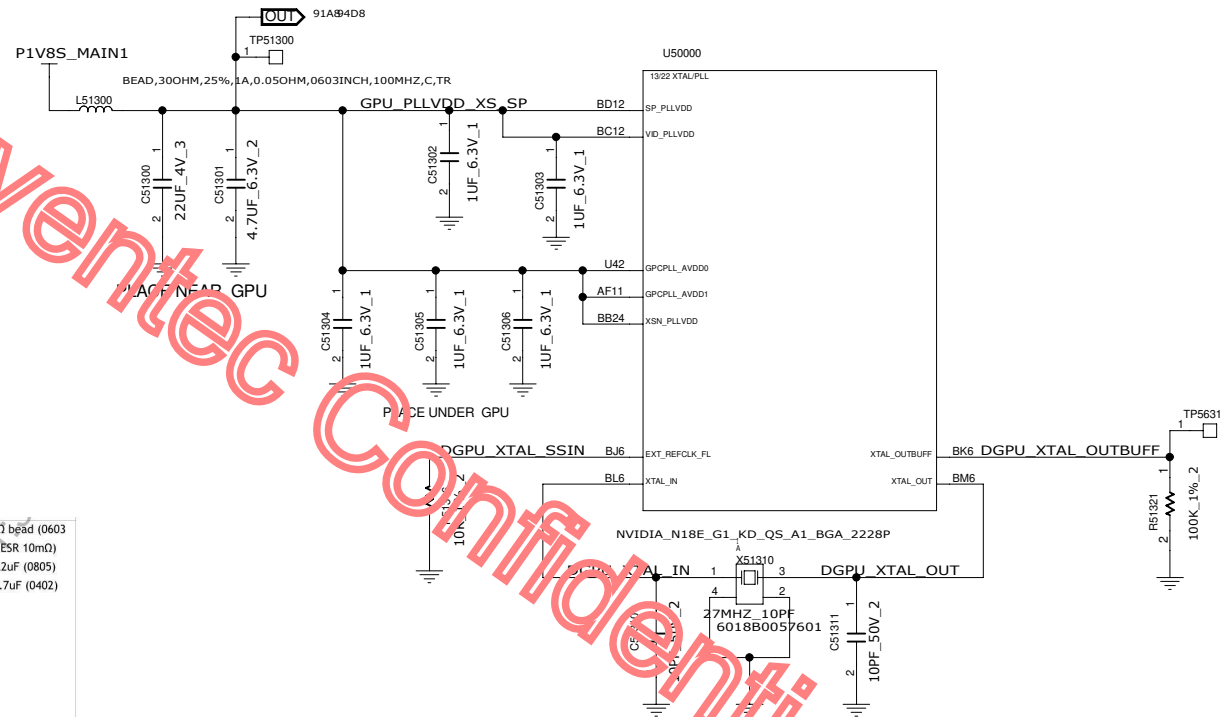
$$CL_{trim} = 2 \times CLoad - (C_{stray} + C_i)$$

Where:

- ▶ C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- ▶ C_{stray} is $\sim 3\text{pF}$ (Stray capacitance of XTAL pads and any significant trace routing)
- ▶ C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S)	1 x 300 bead (0603)
IFPCD_PLLVDD	1			max ESR 10mΩ
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X6S)	1 x 22uF (0805)
				1 x 4.7uF (0402)
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S)	
			Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1.0uF (0201W X6S)	



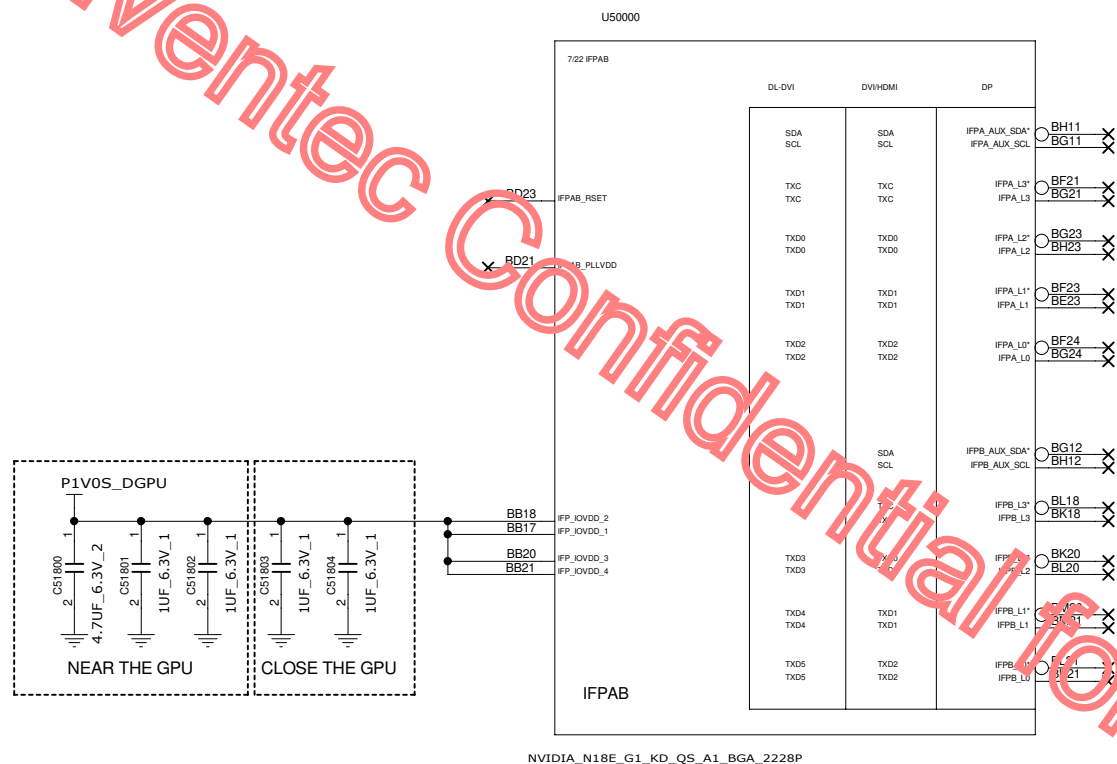
51300 - 51399

INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

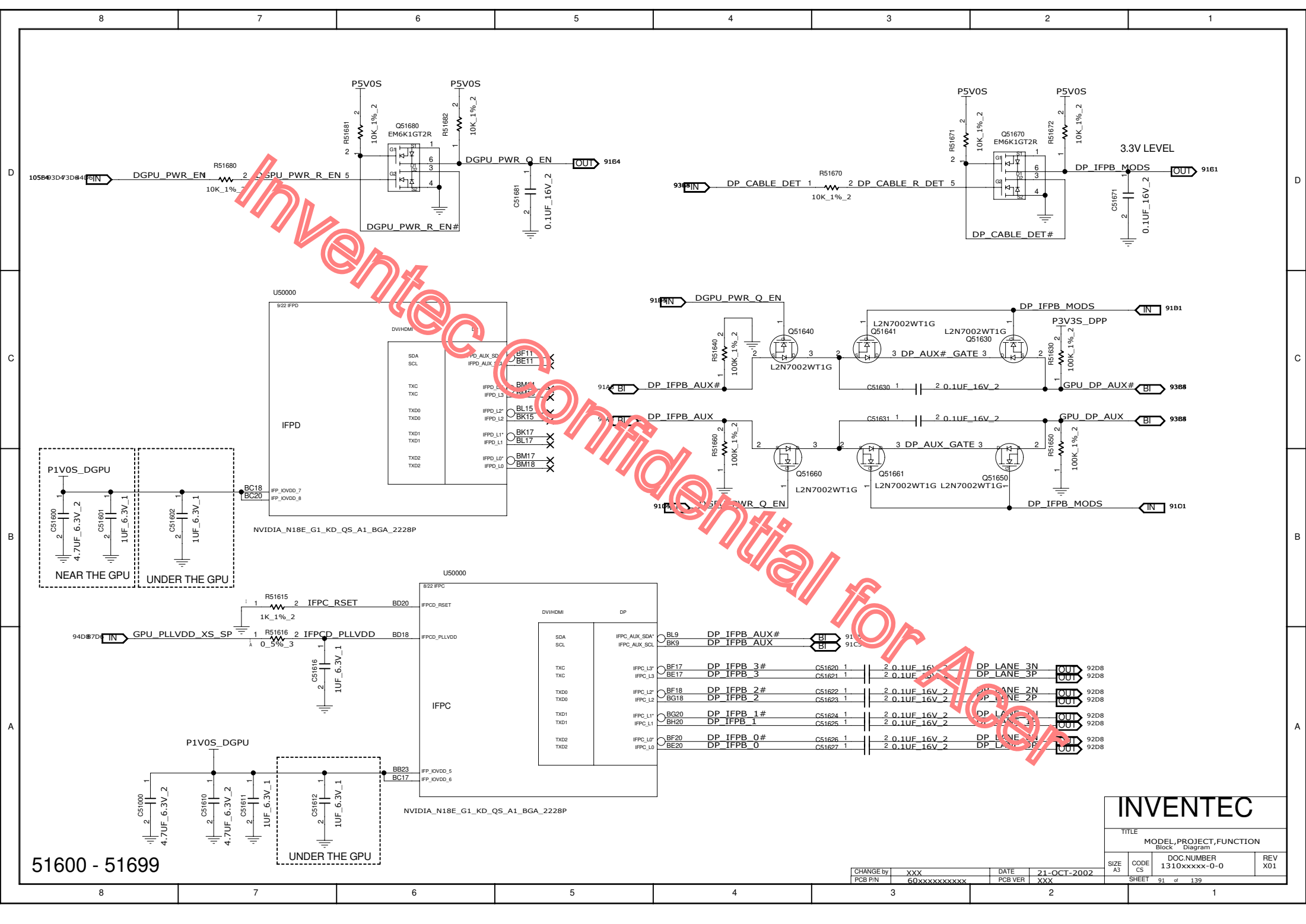
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 87 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



51800 - 51899

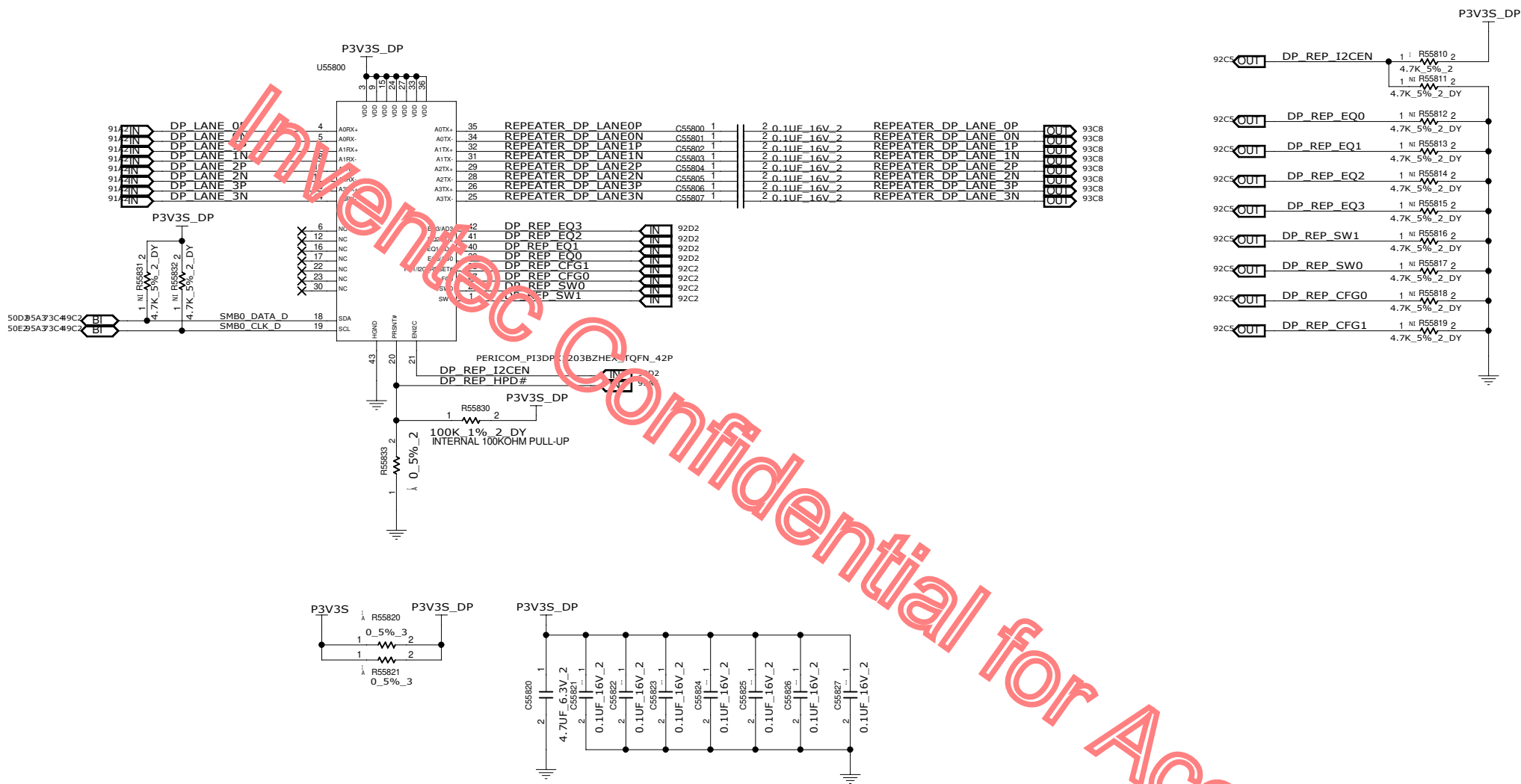
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	A3	CS		
				SHEET	90 of 139		



51600 - 51699

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
60xxxxxxxxxxx				
SHEET		91 of 139		

DP REDRIVER



55800 - 55999 56000 - 56199

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET 92 of 139			

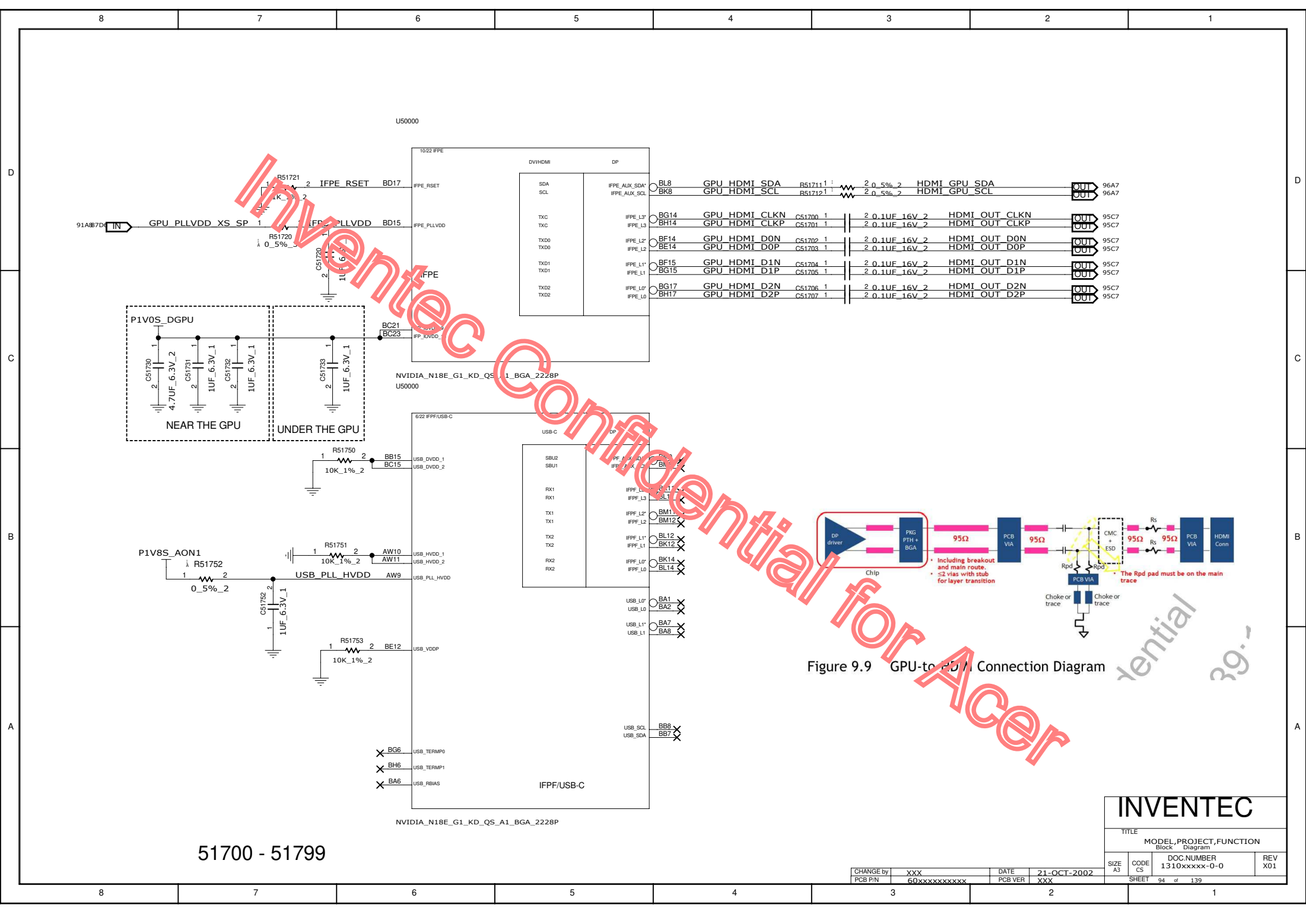
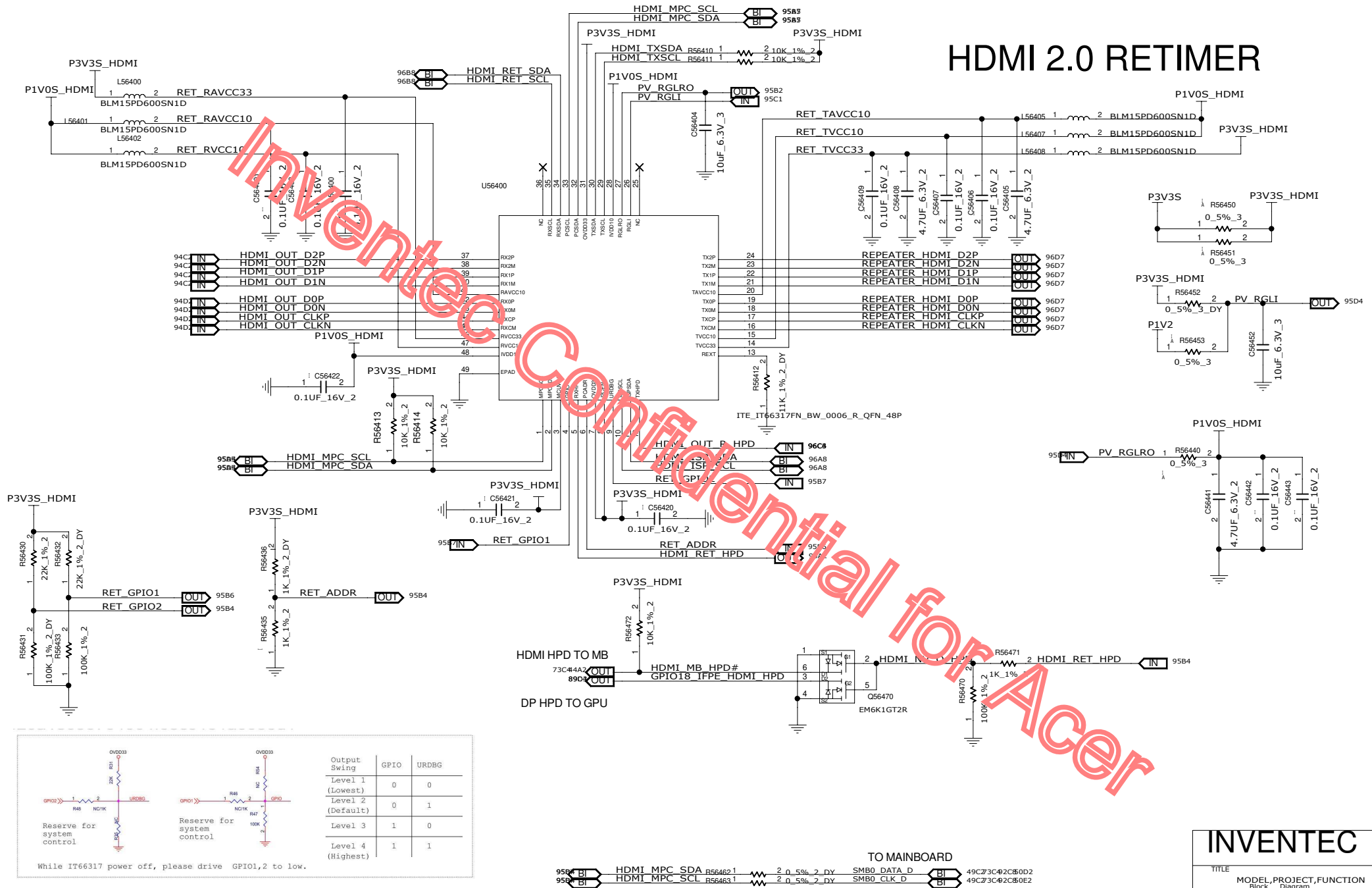


Figure 9.9 GPU-to-PD/A Connection Diagram

51700 - 51799

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
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PCB P/N		PCB VER	XXX	
SHEET		94 of 139	1	

HDMI 2.0 RETIMER



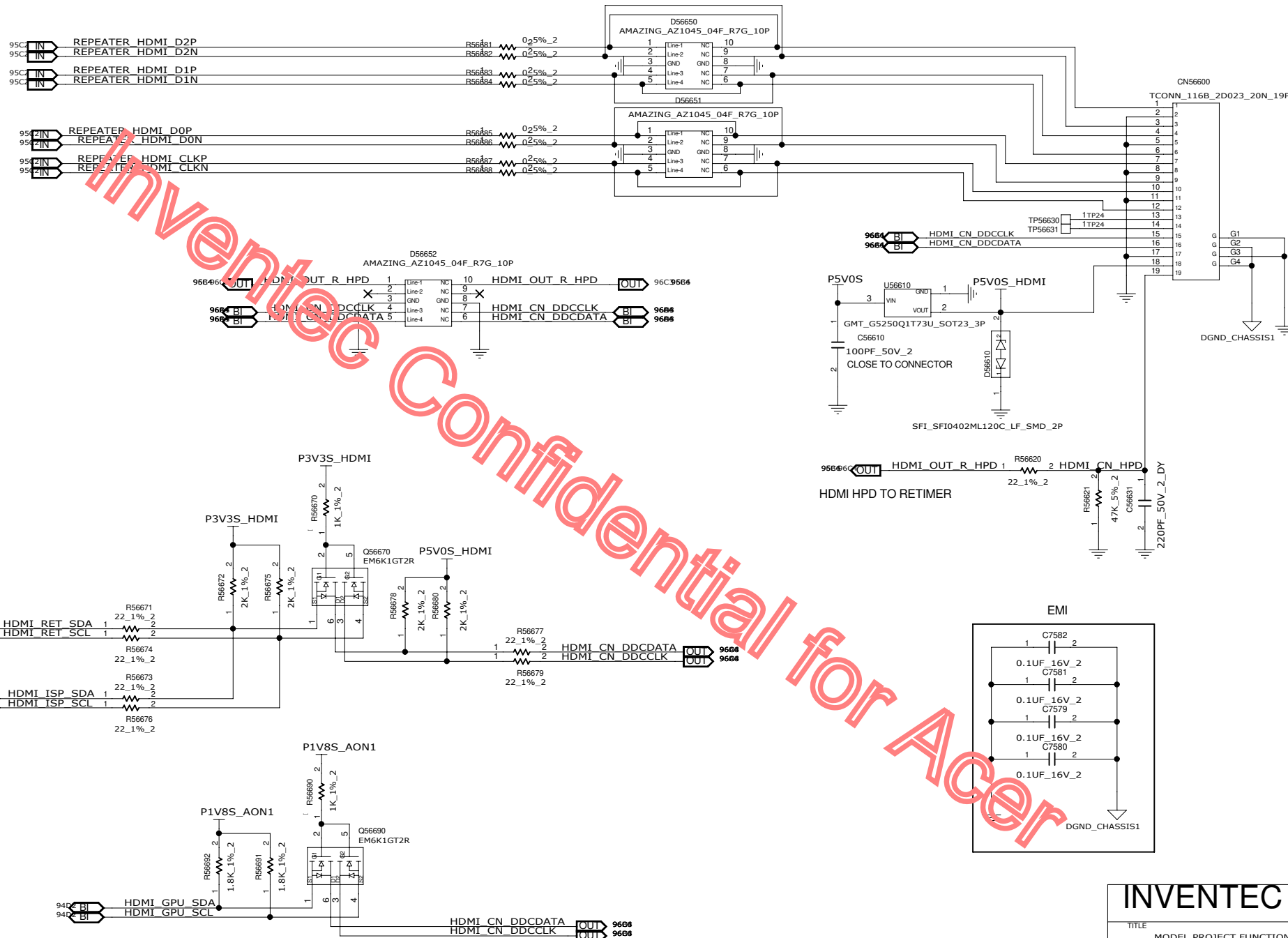
56400 - 56599

TO MAINBOARD

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
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SHEET 95 of 139			

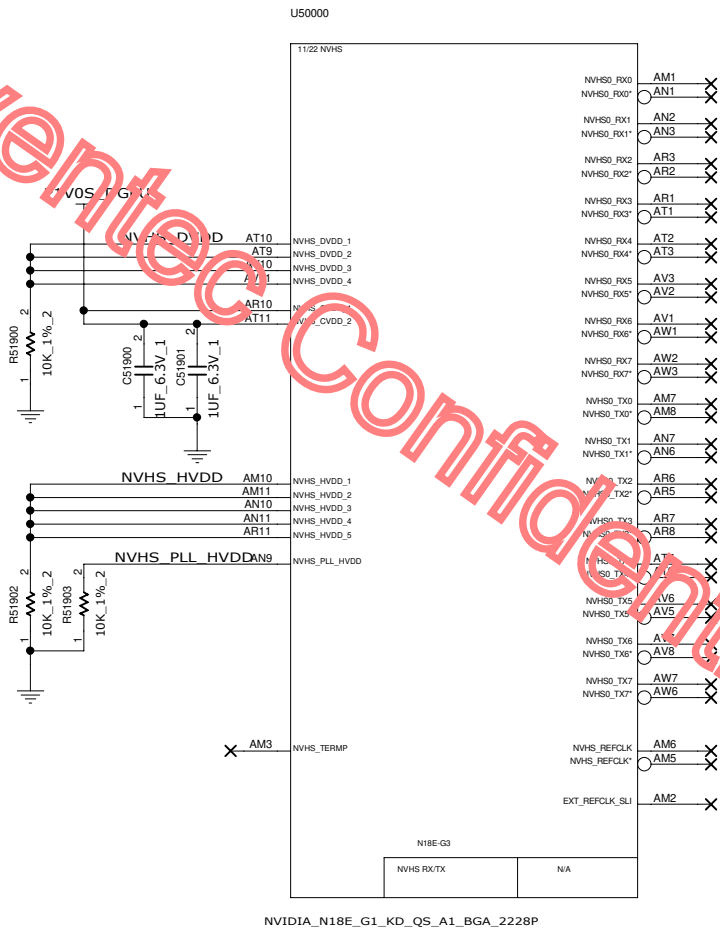
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX



56600 - 56799

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	96	of	139				

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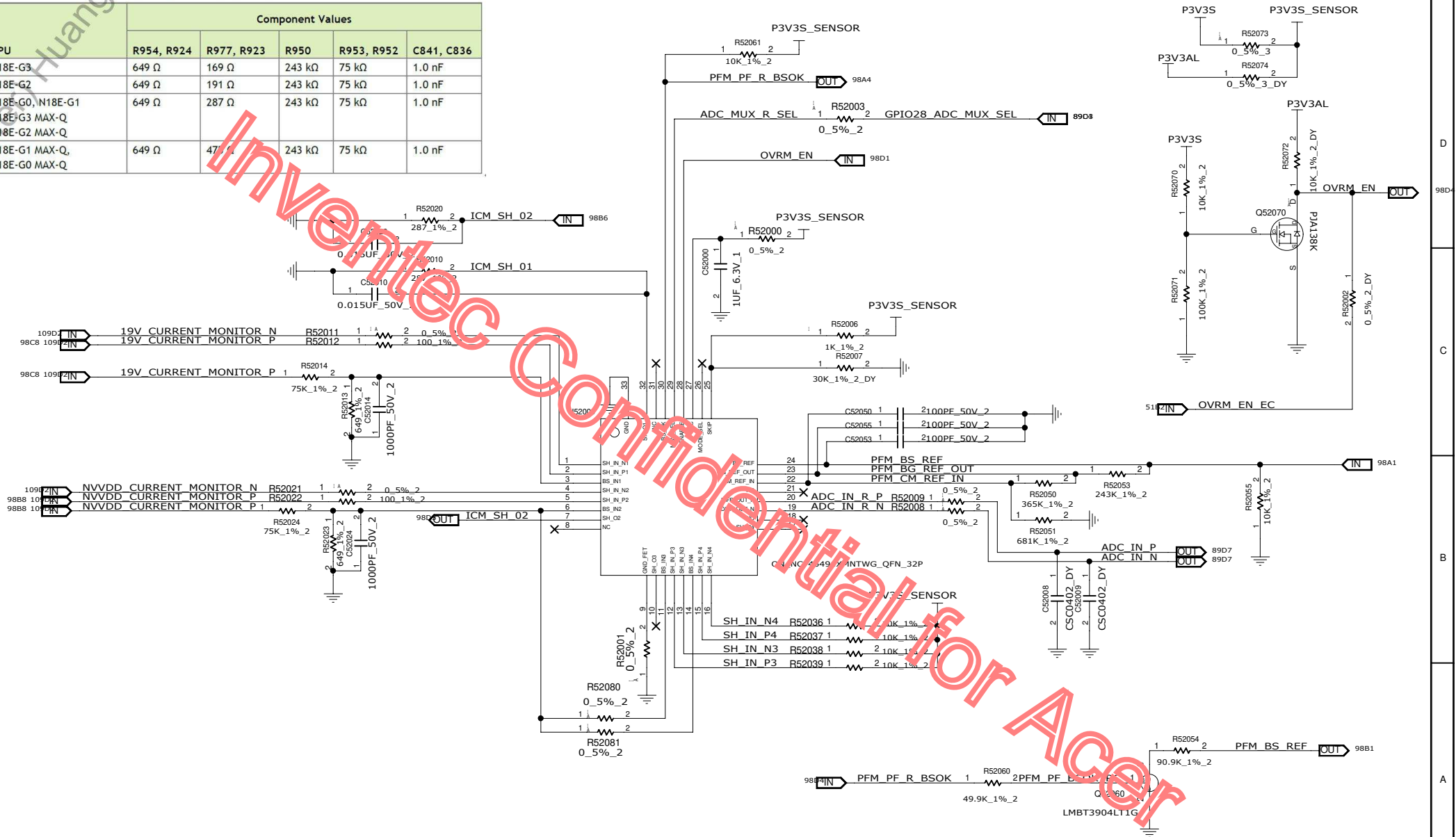


51900 - 51999

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
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A3	CS	1310xxxxx-0-0	X01	
CHANGE by	XXX	DATE	21-OCT-2002	
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	
SHEET		97 of 139		

Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G2	649 Ω	191 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G0, N18E-G1	649 Ω	287 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G3 MAX-Q					
N18E-G2 MAX-Q					
N18E-G1 MAX-Q	649 Ω	471 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G0 MAX-Q					



52000 - 52099

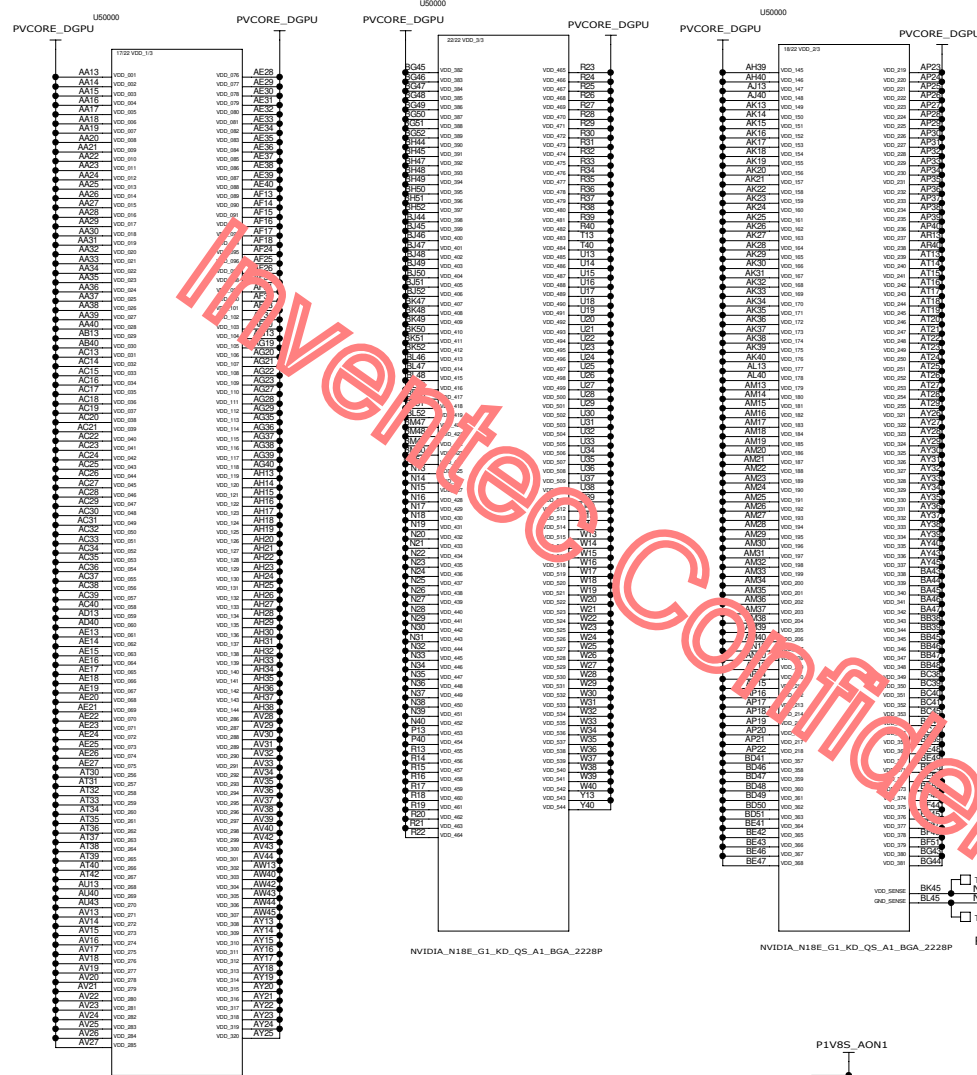
INVENTEC

TITLE MODEL, PROJECT, FUNCTION
Block Diagram

SIZE CODE DOC. NUMBER REV
A3 C5 1310xxxxx-0-0 X01

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxx PCB VER: XXX

SHEET 98 of 139



The required subcircuit is shown in detail in Figure 15.6.

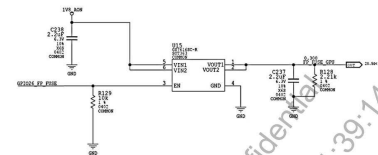
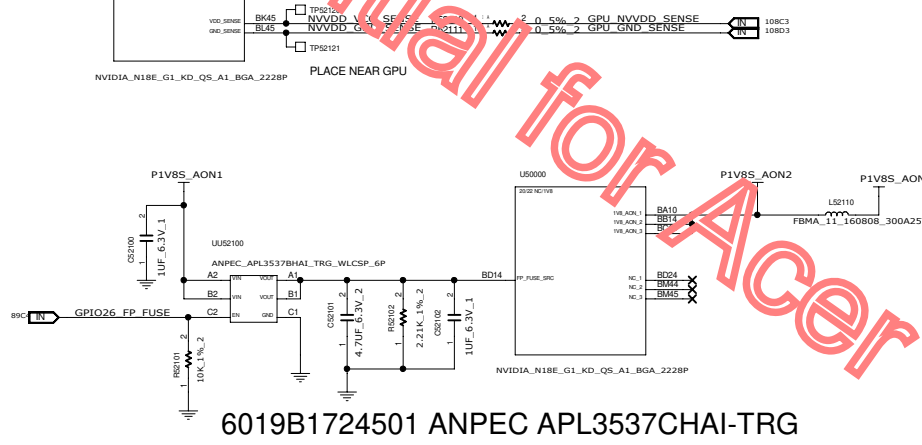
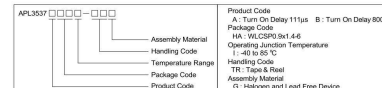


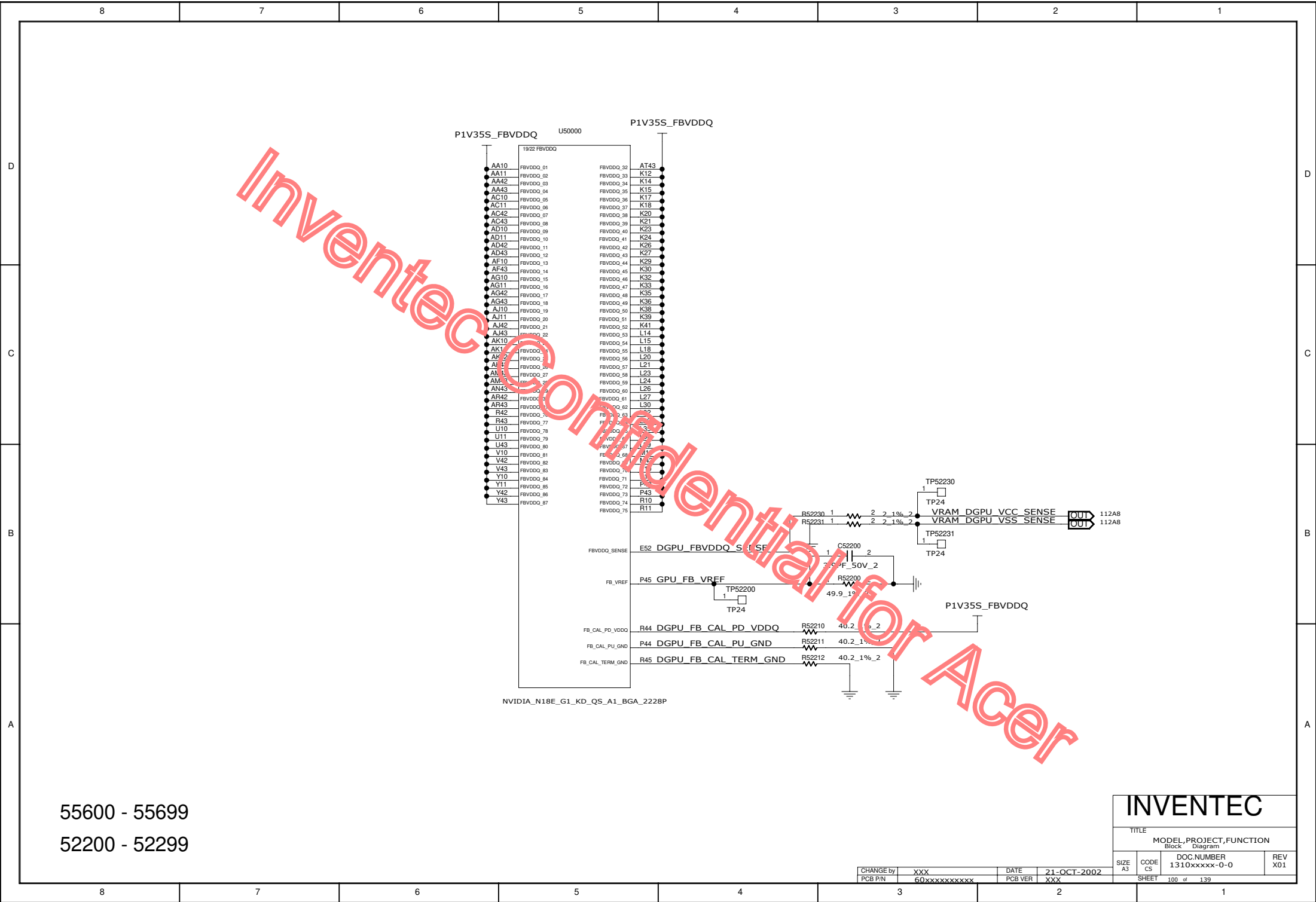
Figure 15.6 Subcircuit Schematic

- In Figure 15.6, the component labeled "U15" is an active switch; devices equivalent to the GS7616SC-R are acceptable as long as they meet the following requirements:
- ▶ The active switch must be capable of driving 100mA or more.
 - ▶ The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100ms or less.
 - ▶ There must be no glitch during power up or GPGCC-Off entry or exit.
 - ▶ The FP_FUSE_GPU output trace width must be 0.25 mm (10 mil) or greater.



6019B1724501 ANPEC APL3537CHAI-TRG

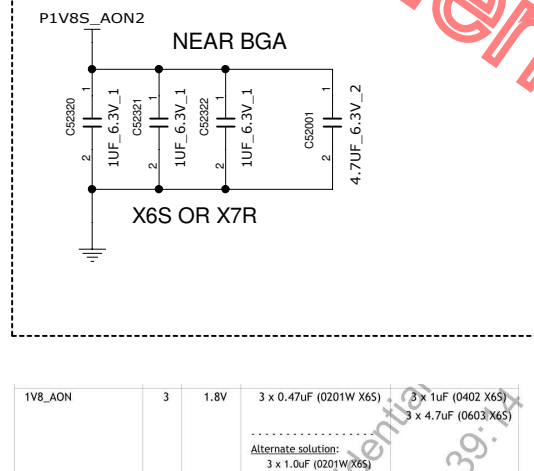
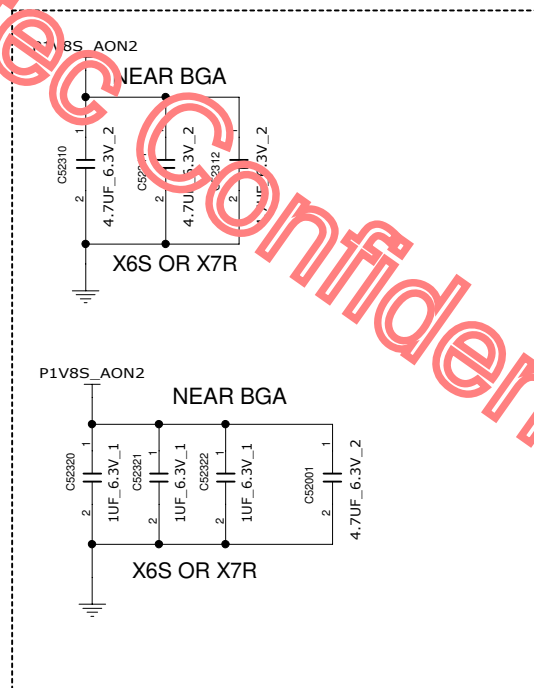
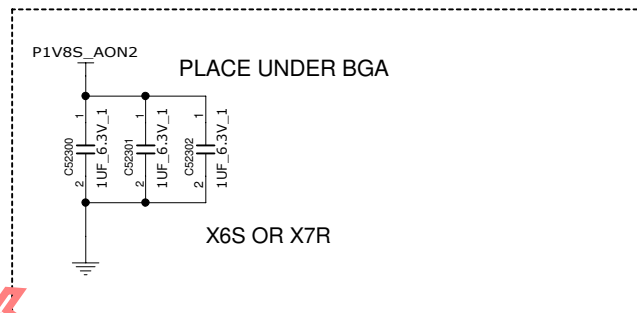




55600 - 55699
52200 - 52299

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	100	of	139				

GPU 1V8_AON DECOUPLING



1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S)	3 x 1uF (0402 X6S)
			Alternate solution:	3 x 4.7uF (0603 X6S)
			3 x 1.0uF (0201W X6S)	

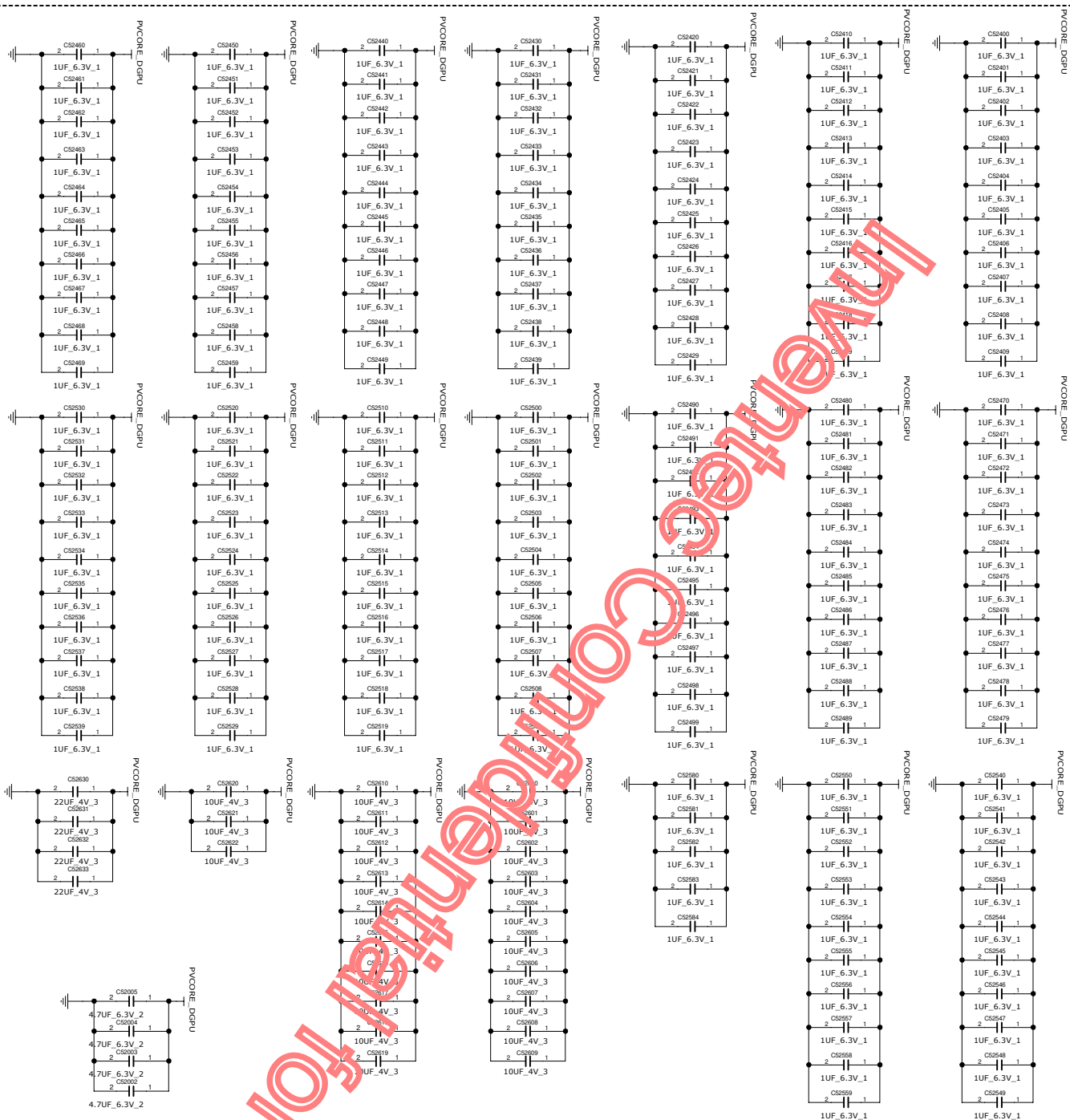
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

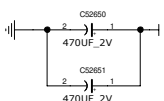
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET	101 of 139
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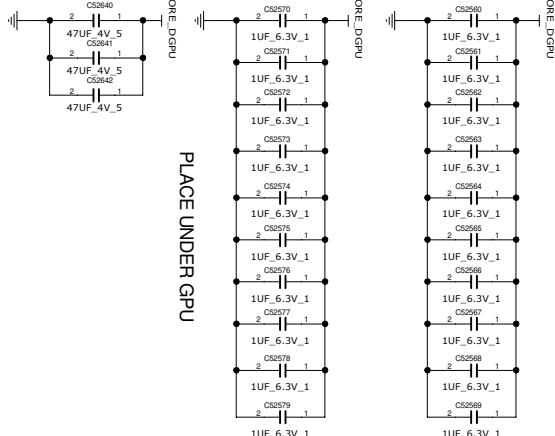
INVENTEC



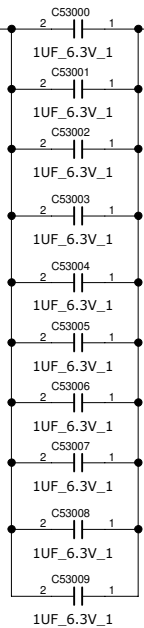
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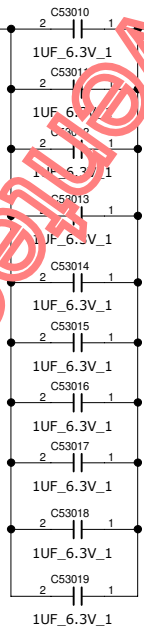
PLACE UNDER GPL

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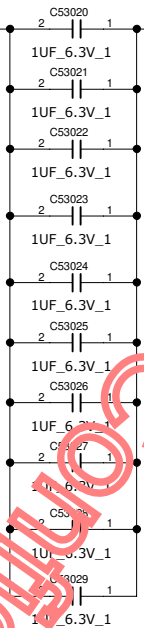
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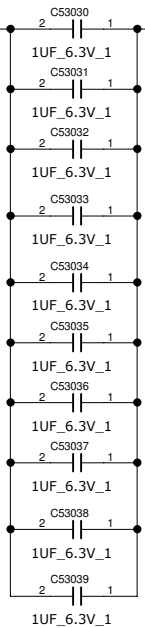
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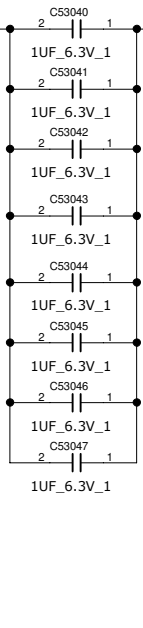
P1V35S_FBVDQ



P1V35S_FBVDQ

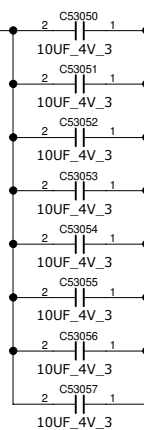


P1V35S_FBVDQ



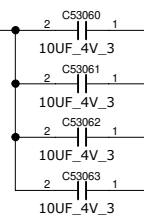
PLACE UNDER GPU

P1V35S_FBVDQ



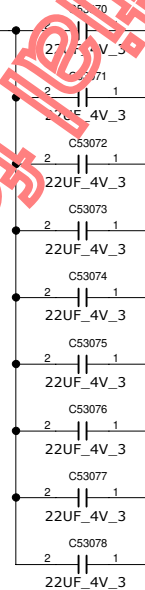
PLACE UNDER GPU

P1V35S_FBVDQ



PLACE NEAR GPU

P1V35S_FBVDQ



Herbert
tec Net

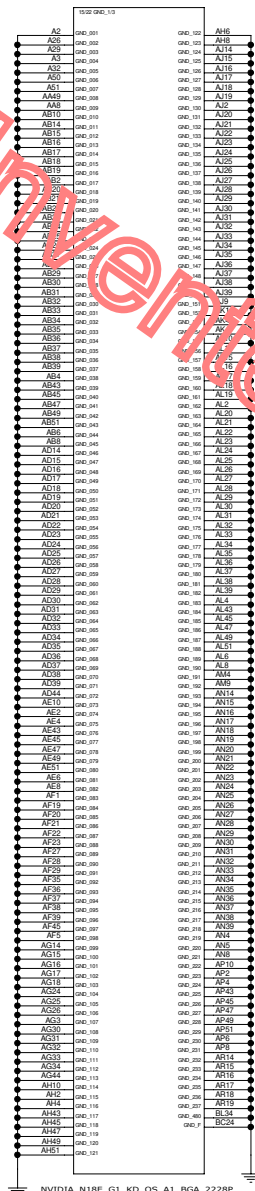
FBVDQ (GPU side)
25V
48 x 0.47uF (0201W X65)
8 x 10uF (0603 X65)
4 x 10uF (0603 X65)
9 x 22uF (0603 X65)
generate solution:
24 x 1.0uF (0201W X65) 2
8 x 10uF (0603 X65)

INVENTEC

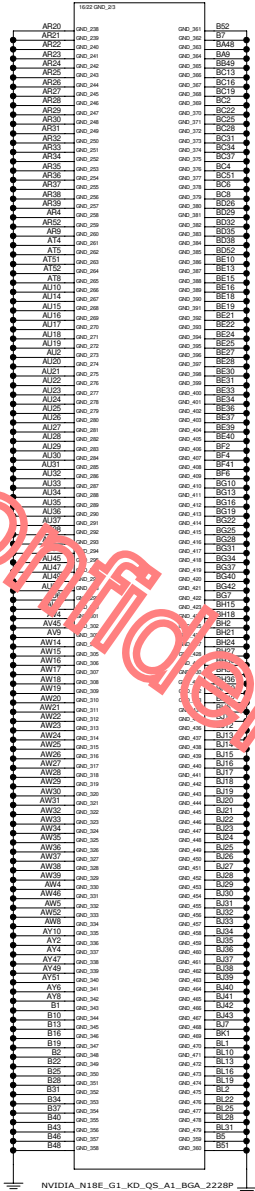
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GND

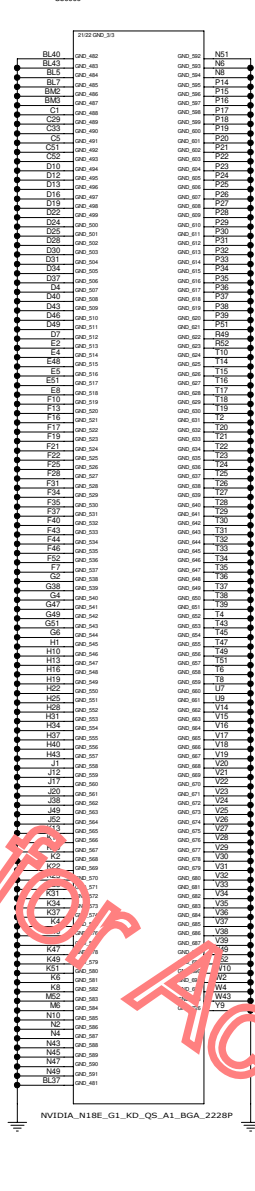
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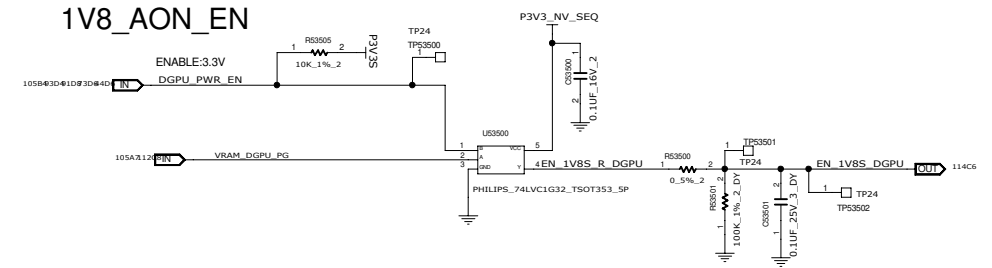
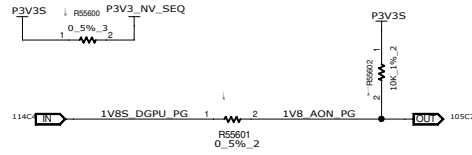
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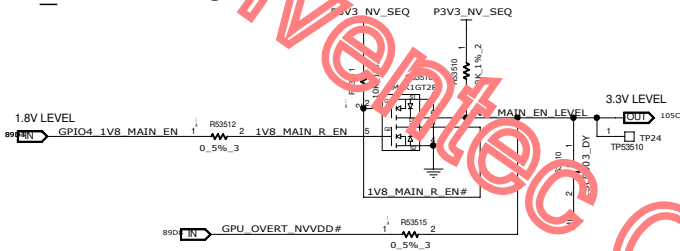
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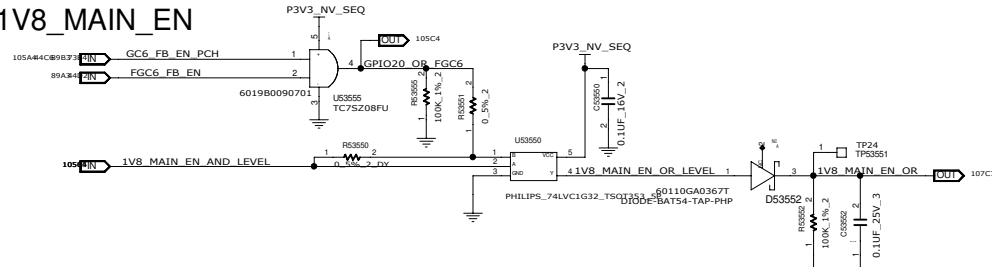
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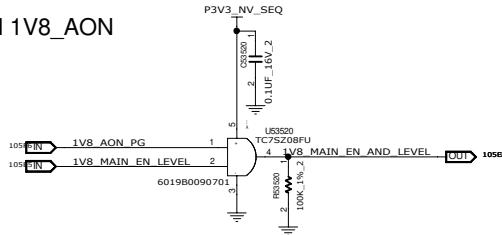
1V8_MAIN_EN LEVEL SHIFT



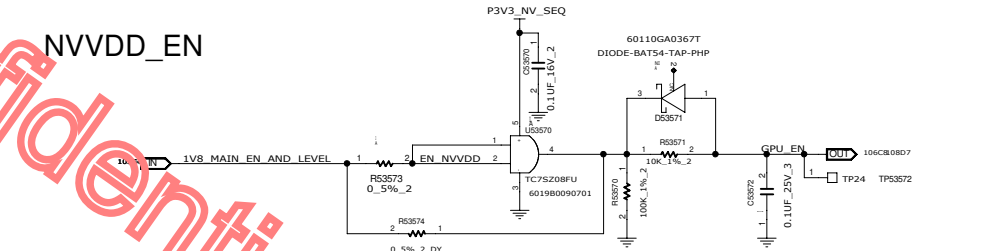
1V8_MAIN_EN



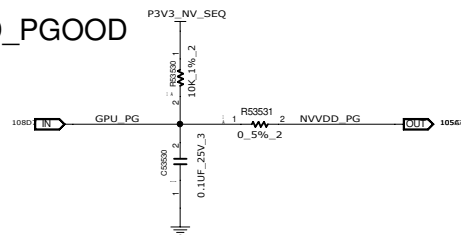
1V8_MAIN_EN AND WITH 1V8_AON



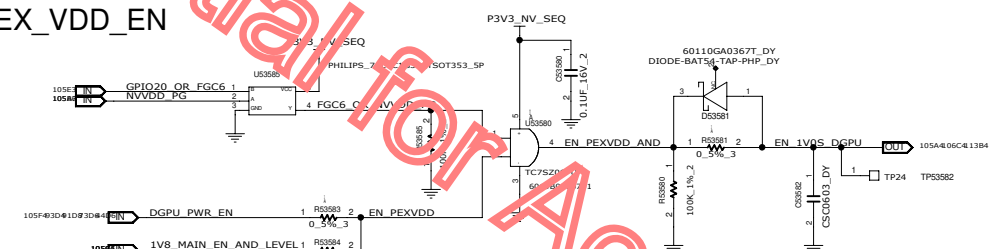
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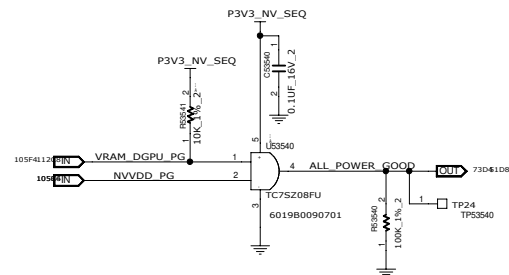
NVVDD_PGOOD



PEX_VDD_EN

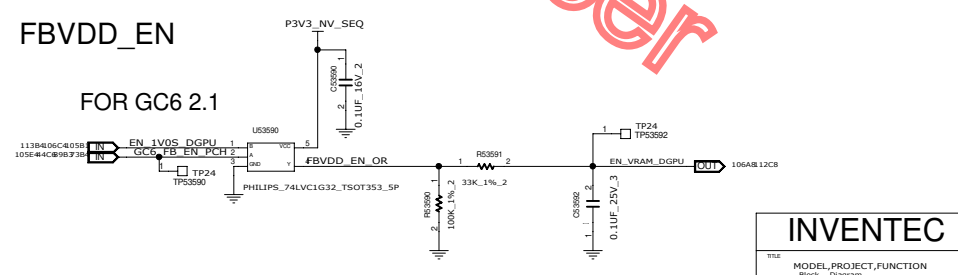


ALL POWER GOOD



FBVDD_EN

FOR GC6 2.1



55600 - 55699

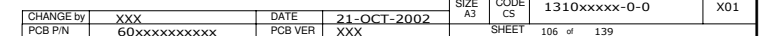
53500 - 53899

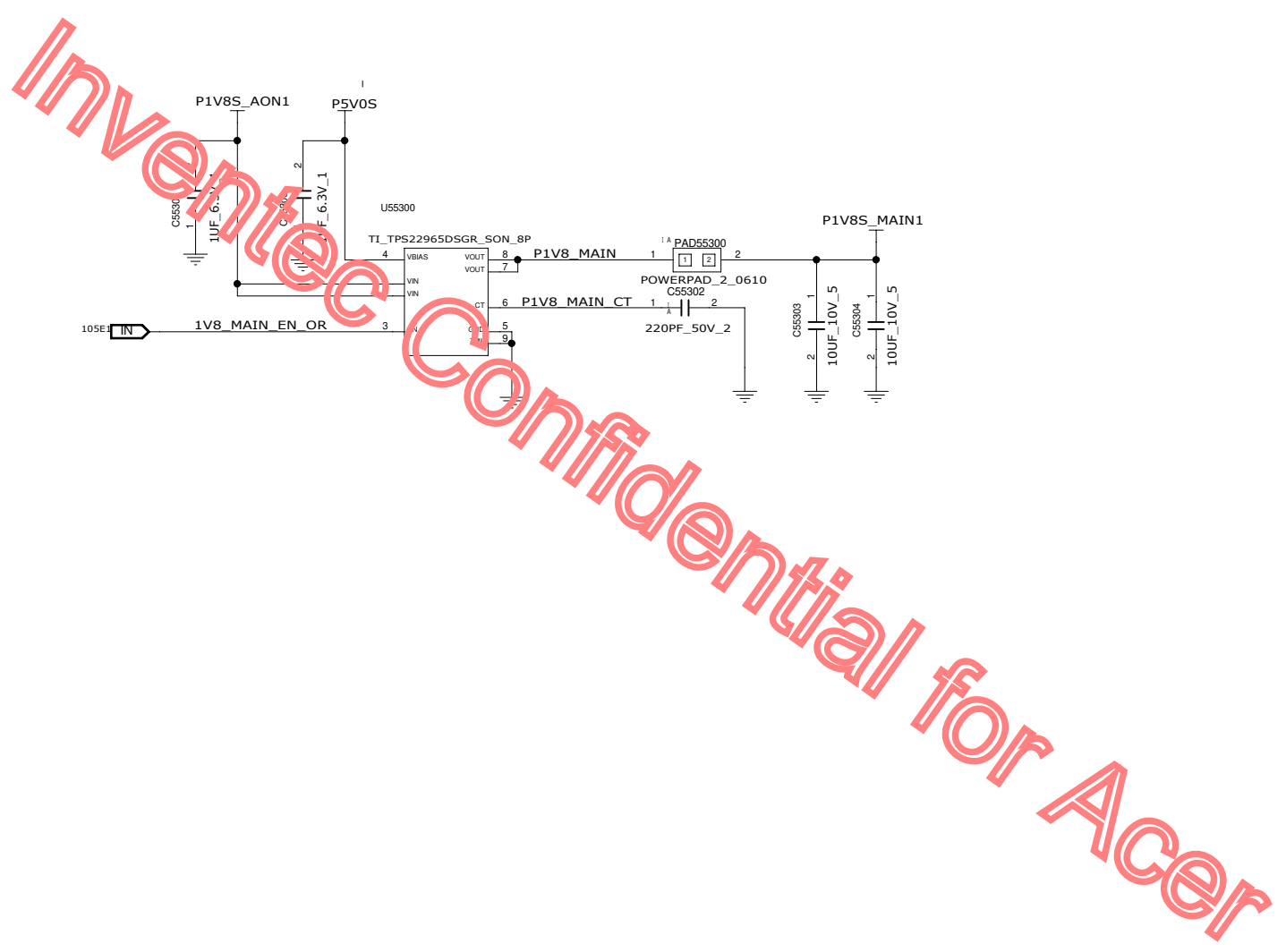
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SHEET 105 of 139			

CHANGE D	XXXX	DATE	21-OCT-2002
PCH PIN	XXXXXXXXXXXX	PCH VER	XXX

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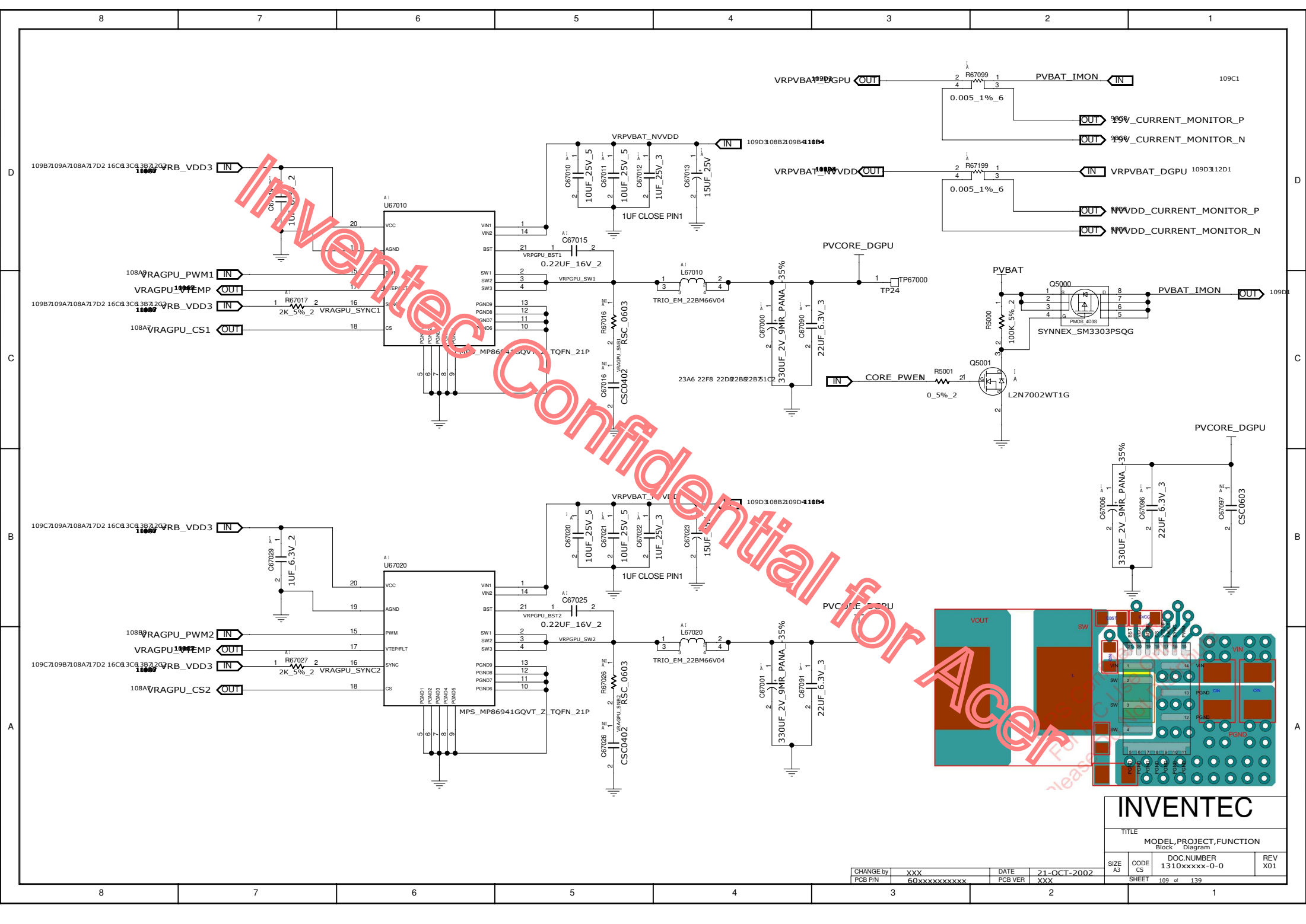


[illegible][illegible][illegible][illegible]

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The schematic diagram illustrates the P1V8 power supply circuit. It begins with a 10SE IN signal connected to the 1V8 MAIN_EN_OR pin (pin 3) of the TI_TPS22965DSGR_SON_8P (U55300). The U55300's VIN pins (pins 4 and 5) are connected to the P1V8S_AON1 node, which also includes a C55300 capacitor (10UF_6.3V_1) and a P5V0S connection. The VBIAS pin (pin 7) is connected to the P1V8S_AON1 node. The VOUT pin (pin 8) is connected to the P1V8 MAIN node. The CT pin (pin 6) is connected to the P1V8 MAIN CT node, which includes a C55302 capacitor (220PF_50V_2). The P1V8 MAIN node is connected to the PAD55300 (POWERPAD_2_0610), which has a 1A current rating. The PAD55300's output (pin 2) is connected to the P1V8S_MAIN1 node, which also includes a C55303 capacitor (10UF_10V_5) and a C55304 capacitor (10UF_10V_5).

[illegible]



INVENTEC

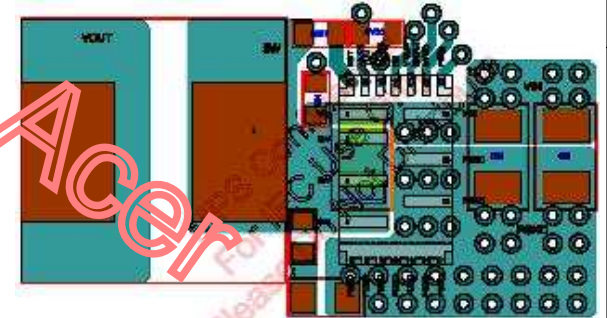
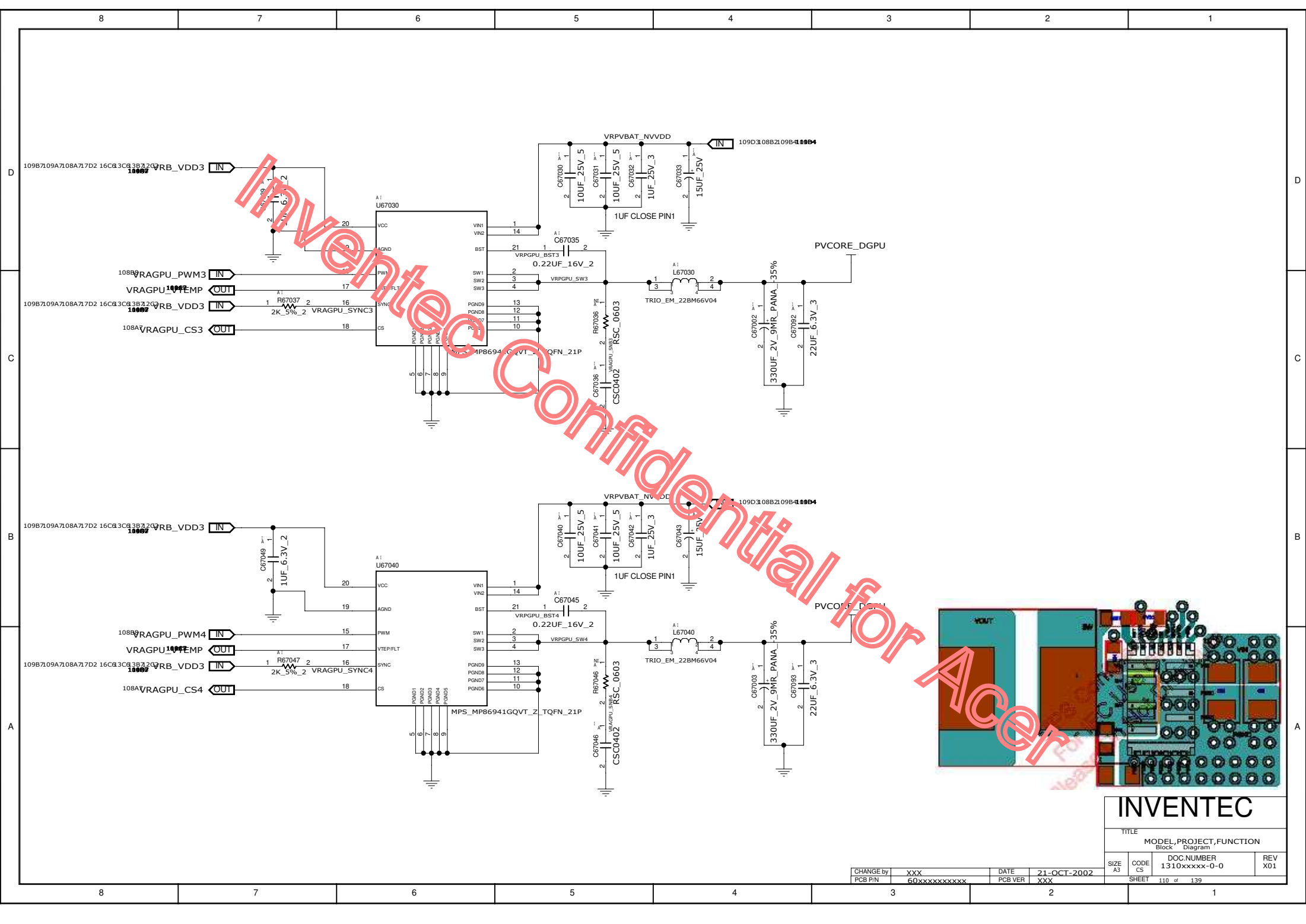
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MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS
SHEET 109 of 139

DOC NUMBER
1310xxxxx-0-0

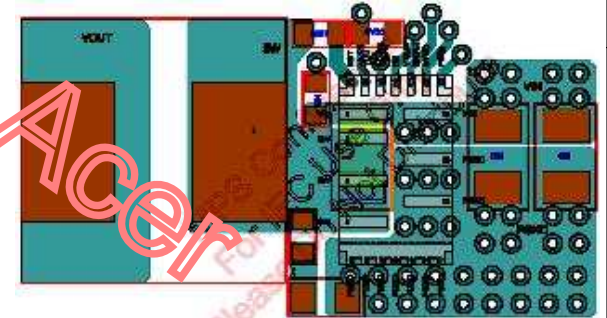
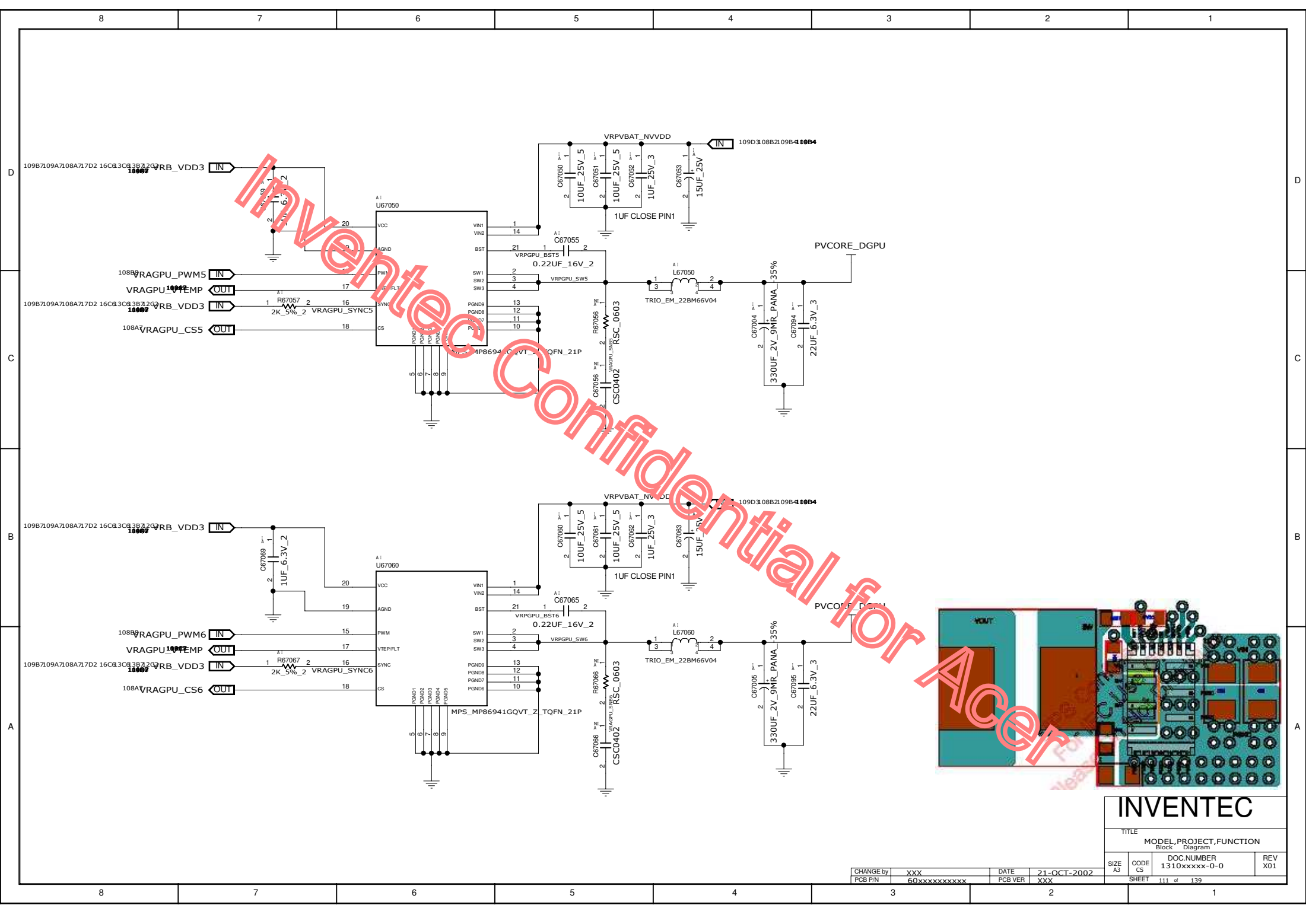
REV
X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



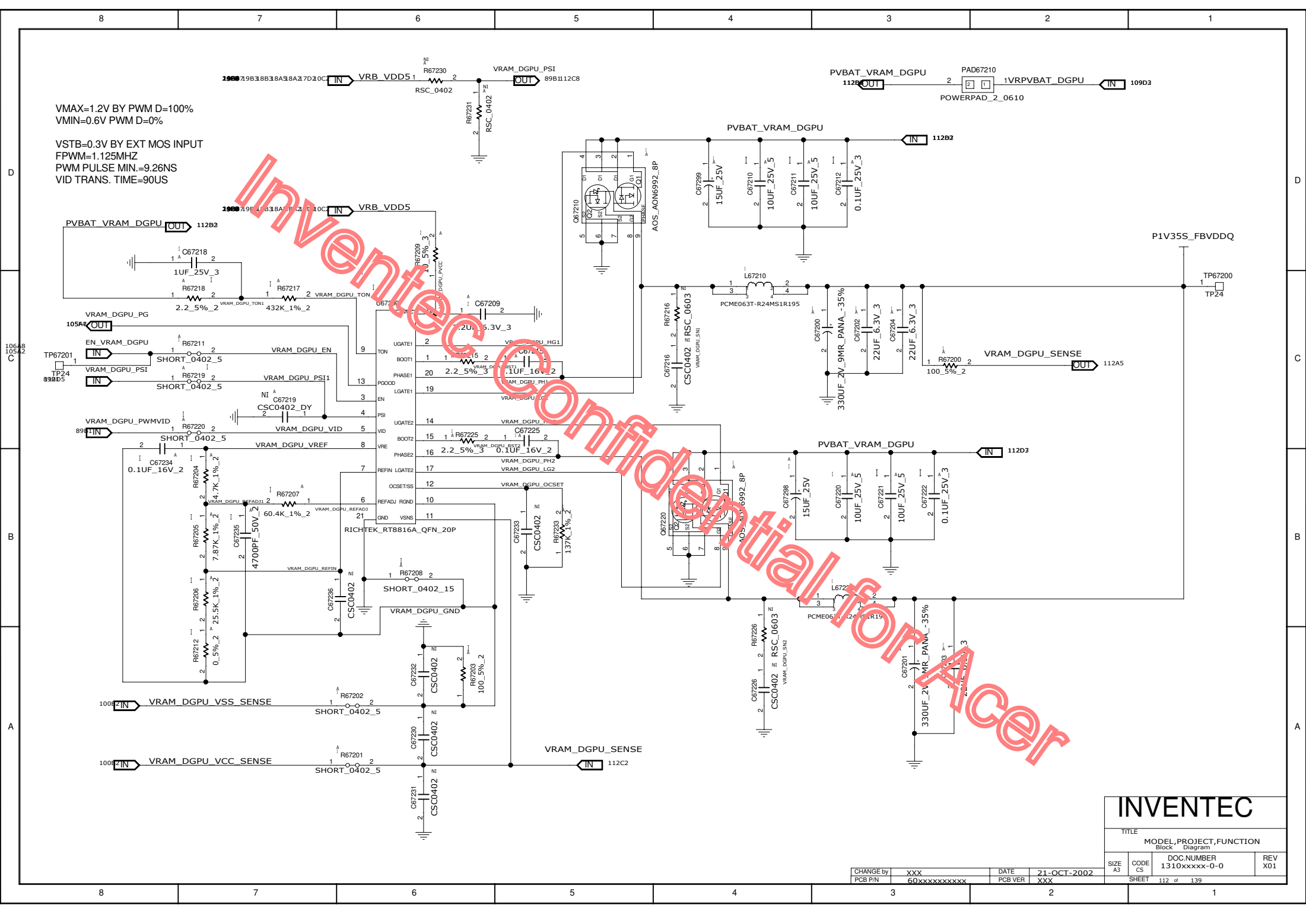
INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 110 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



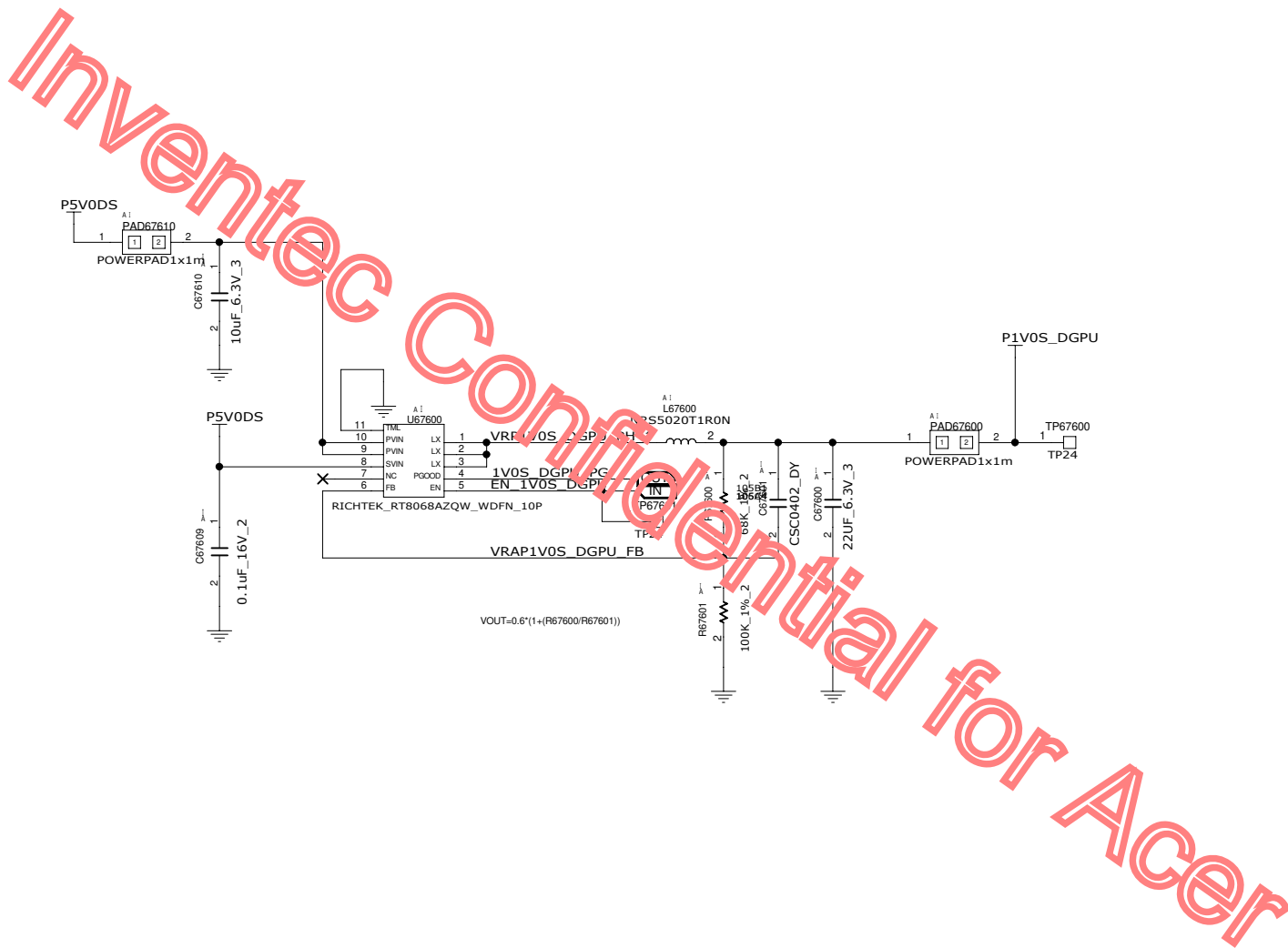
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TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		111 of	139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D=0%
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US

INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		112 of 139		



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		113 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

Table 12. Output EDP-Continuous

		NVVD	FB TOTAL ⁵	1.0V Total ¹	1.8V Total ²
Product	(W)	(A)	(A)	(A)	(A)
N18E-G3	150	142	46	1.6	2.3
	160	150			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

		NVVD	FB TOTAL ⁴	1.0V Total ¹	1.8V Total ²
Product	(W)	(A)	(A)	(A)	(A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms) ² (A)	Input EDPp (5ms) ² (A)	Input EDPc (1sec) ¹ (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$\text{Input EDPc Current (A)} = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$\text{Input EDPp (A) at } V_{\text{new}} = \text{Input EDPp (A) at } 19V \times \frac{19V}{V_{\text{new}}(V)}$$

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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 115 of 139

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

HISTORY

SCHEMATIC MODIFY HISTORY

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INVENTEC

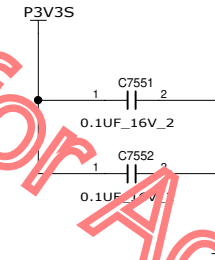
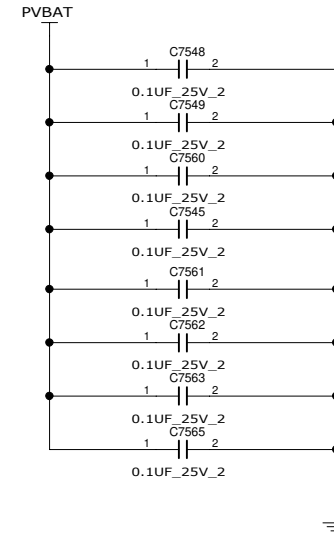
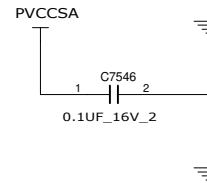
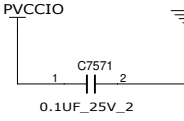
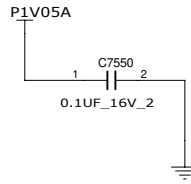
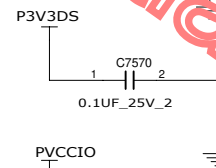
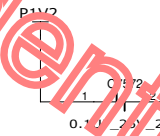
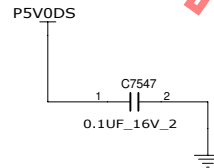
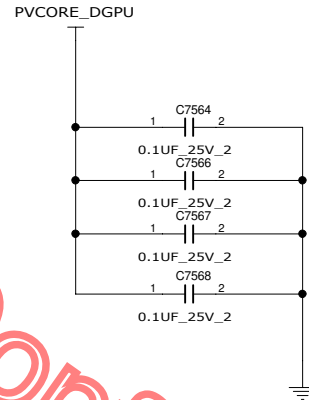
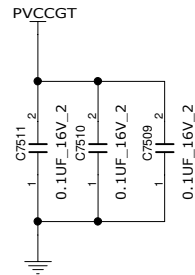
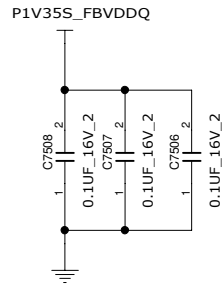
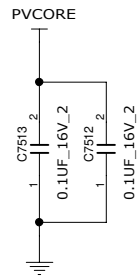
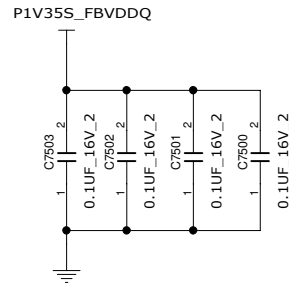
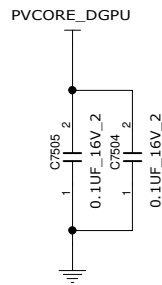
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	xxx 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 xxx
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SHEET 116 of 139

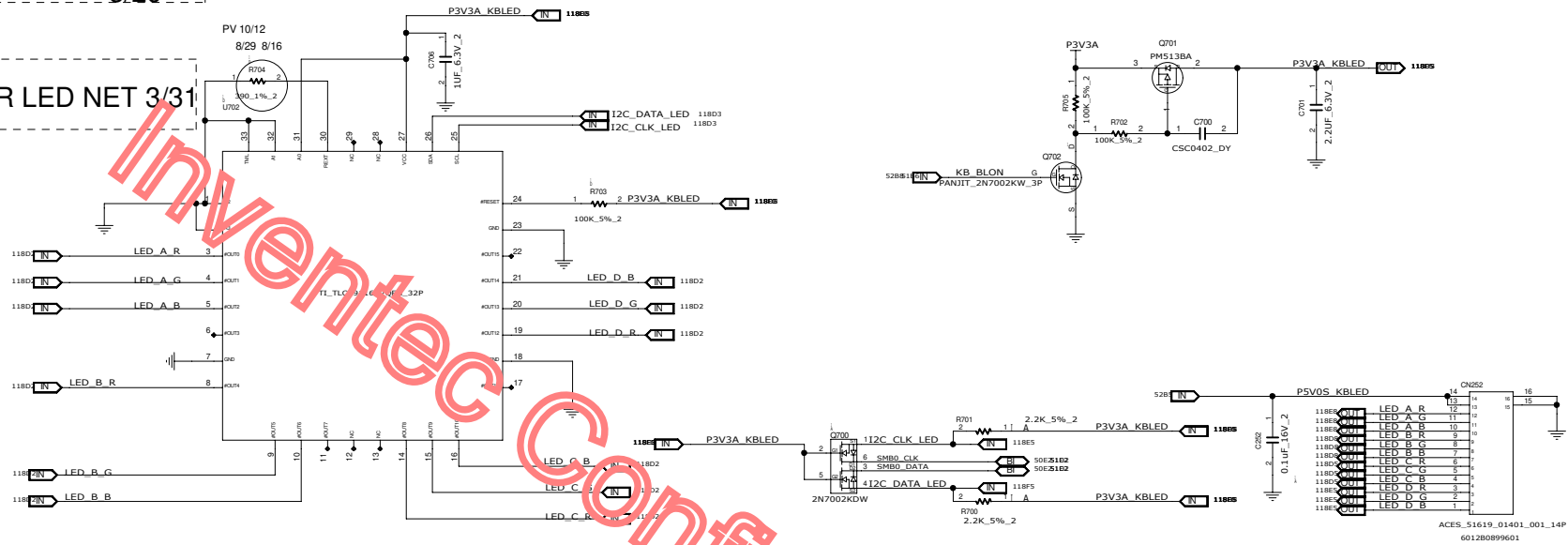
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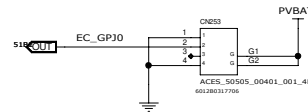
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION NFC CNNN.			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 117 of 139			

ADJUST LED RES 8/16
8/29

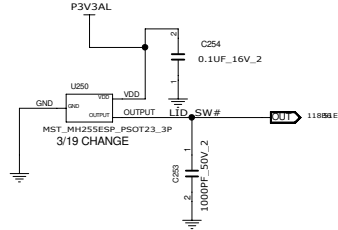
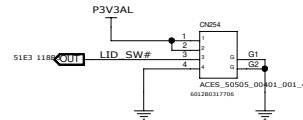
RE-ORDER LED NET 3/31



TURBO#



HALL_SENSOR



REFERENCE NUMBER:700~800

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	C5	1310xxxxx-0-0	X01
SHEET	118	of 139	

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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TURBO# BOARD

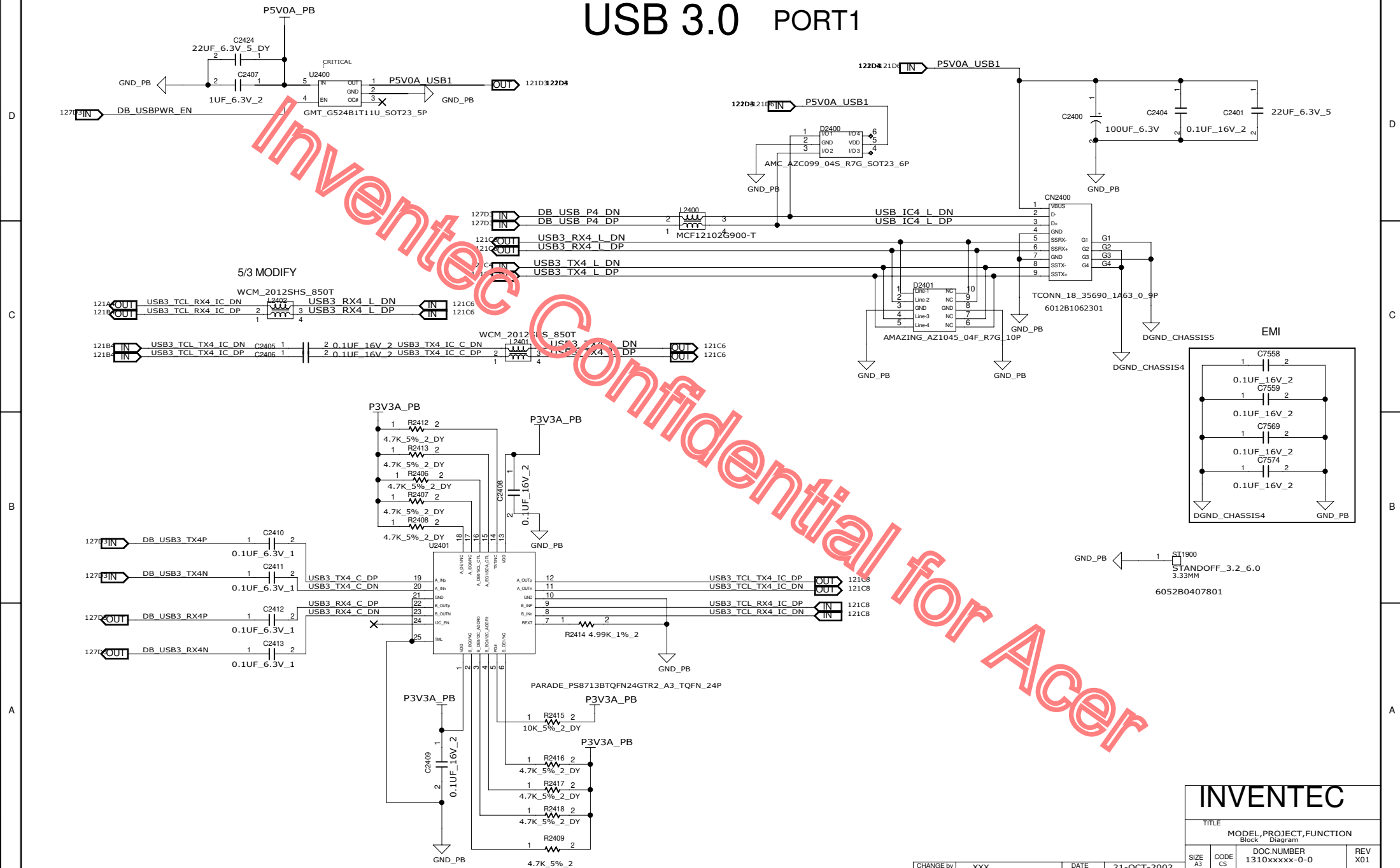
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TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET

XXX	21-OCT-2002
60xxxxxxxxxx	XXX

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 120 of 139			

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC NUMBER

1310xxxxx-0-0

REV

X01

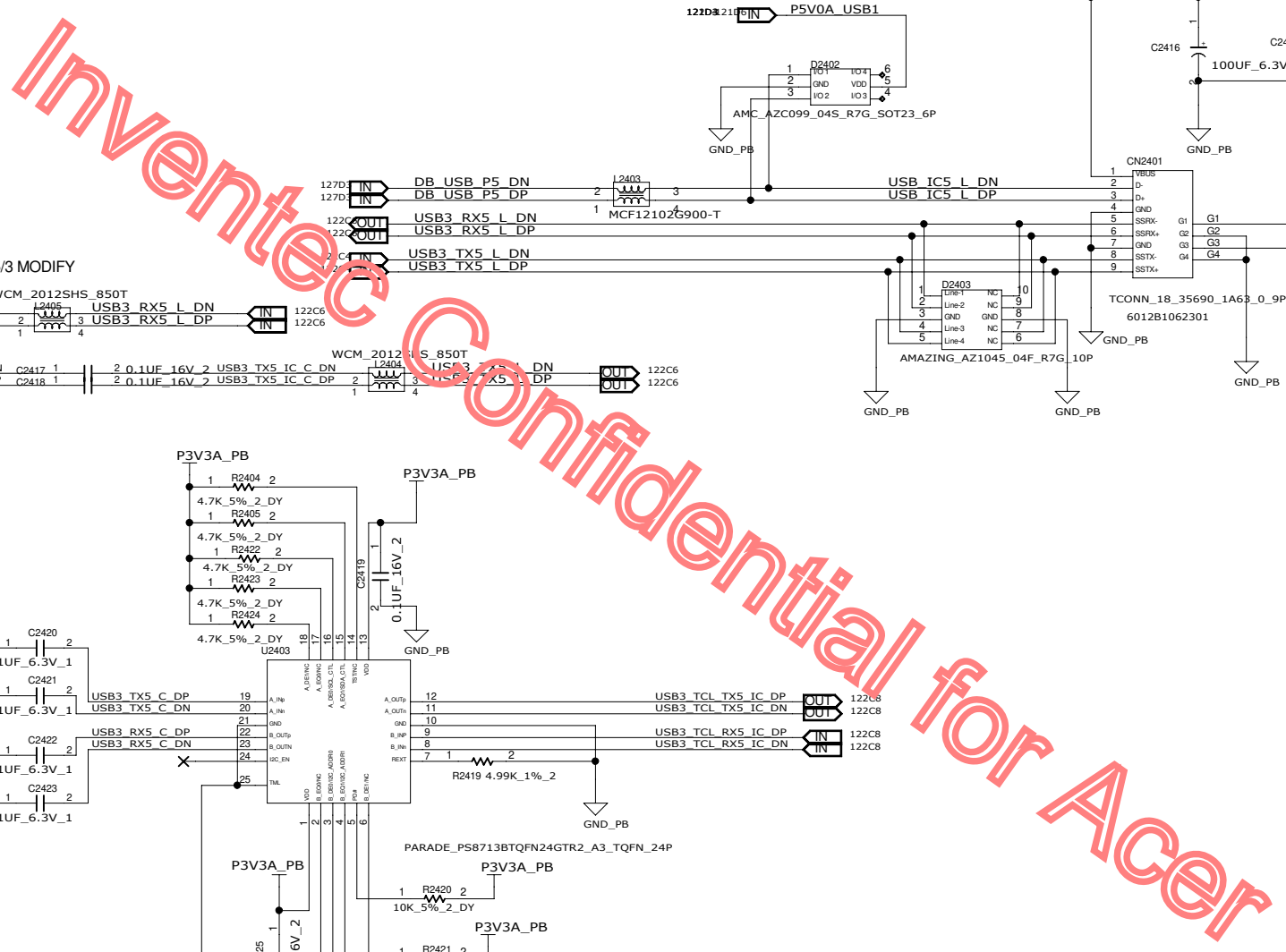
CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

SHEET 121 of 139

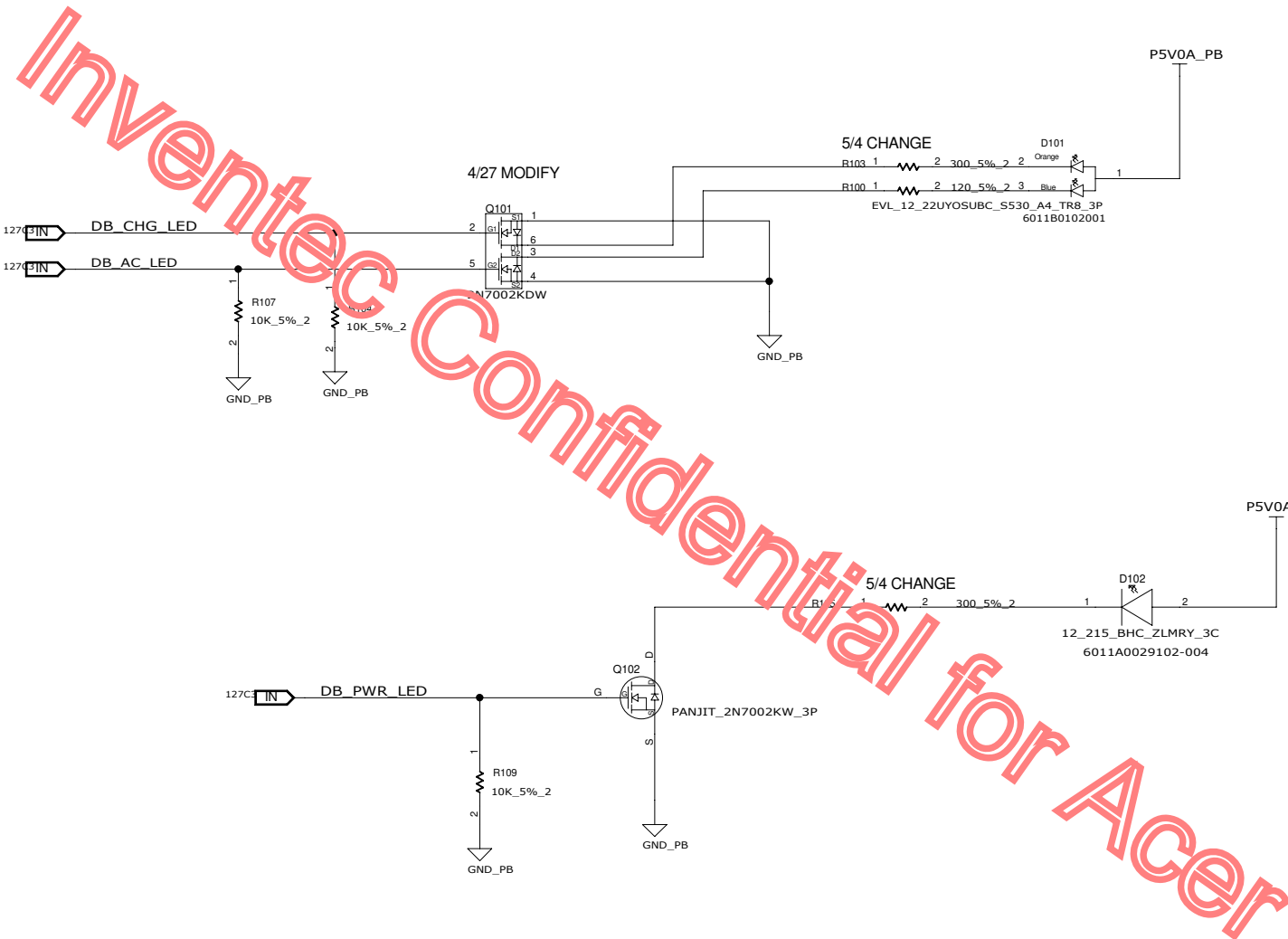
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8	7	6	5	4	3	2	1
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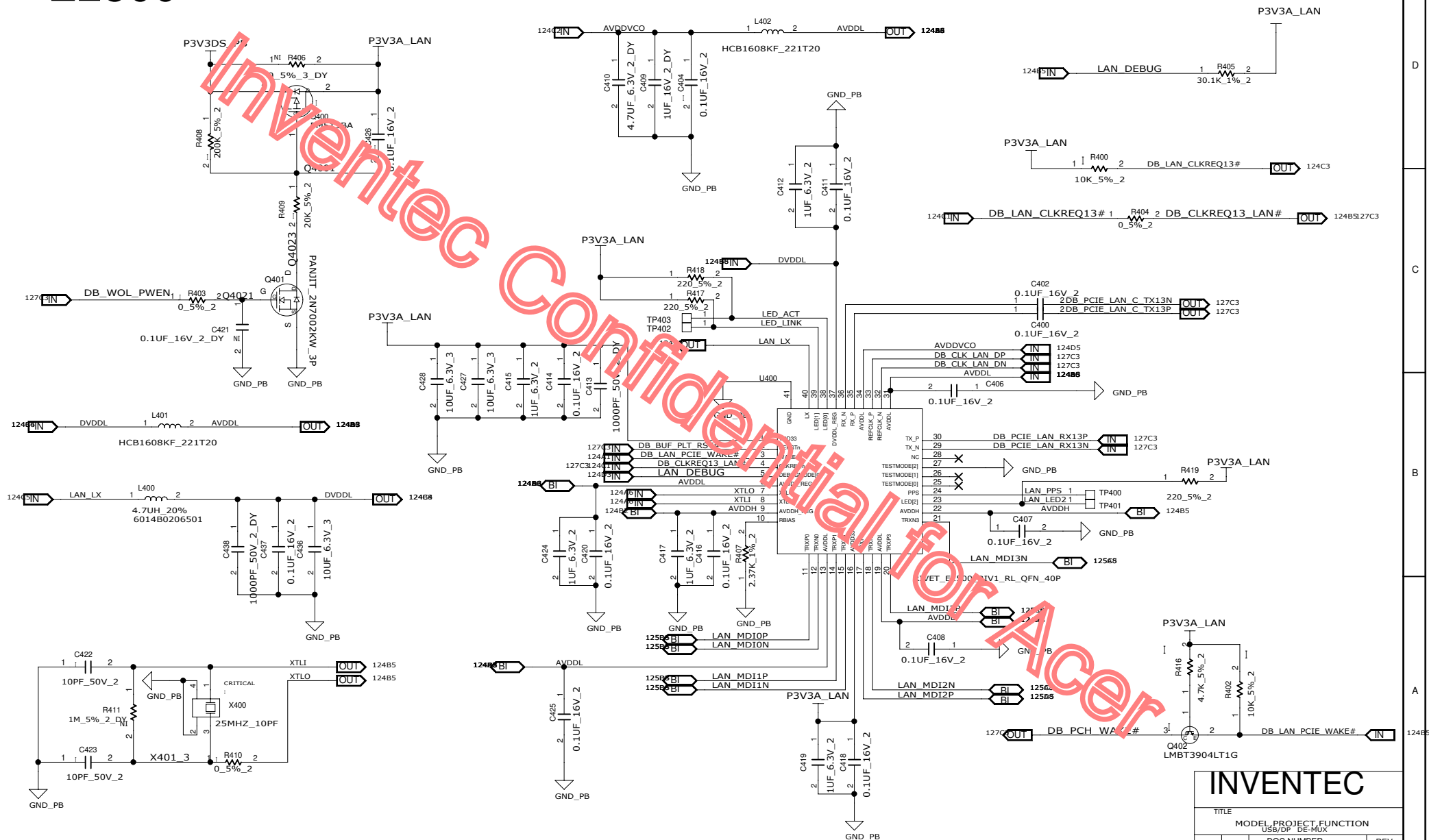
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SHEET		122 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
SHEET		123 of	139

LAN (CONTROLLER) E2500



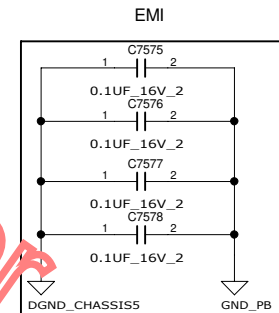
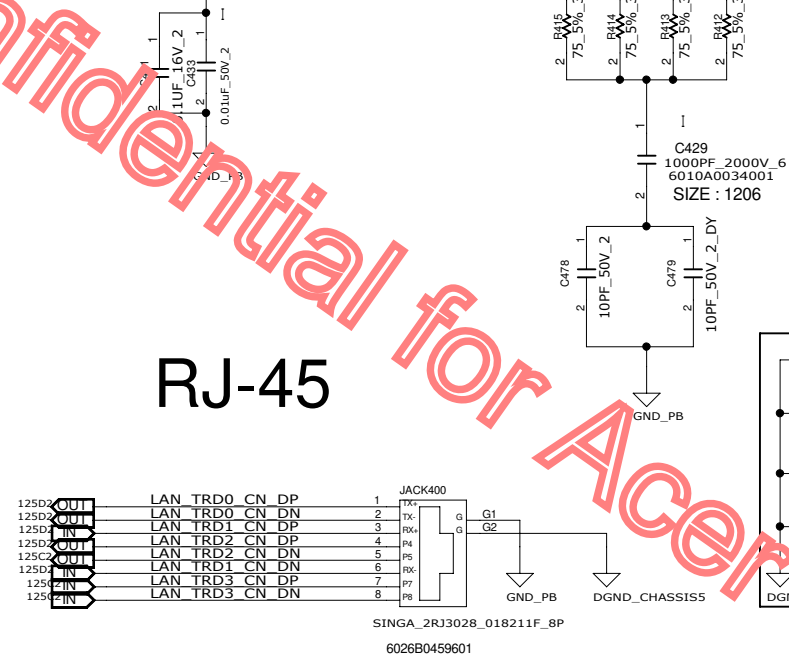
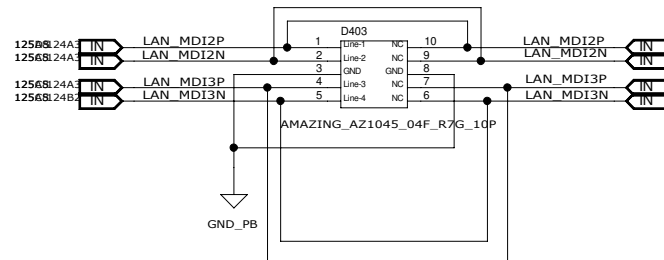
INVENTEC

TITLE
MODEL PROJECT FUNCTION
USB/DP DE-MUX

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB PIN 60xxxxxxx PCB VER XXX

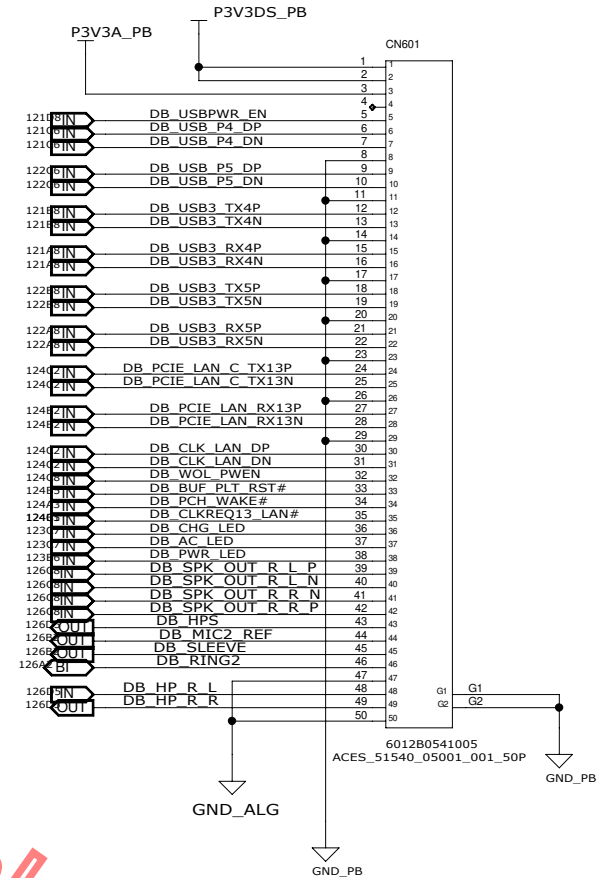
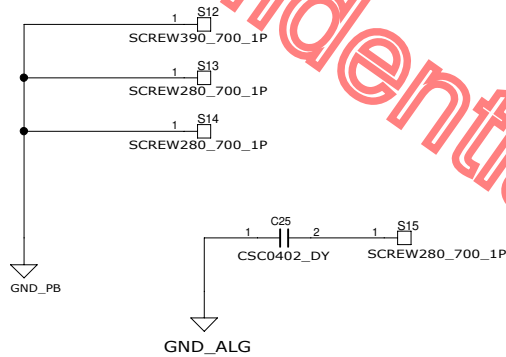
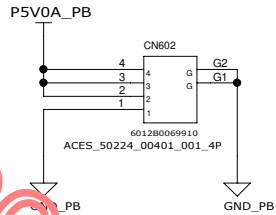
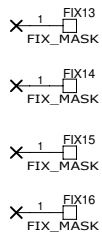
SHEET 124 of 139



A3	CS	1510XXXXXX 0 0	7
SHEET		125 of 139	

	1
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INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 127 of 139

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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FOR 17 SMALL BOARD

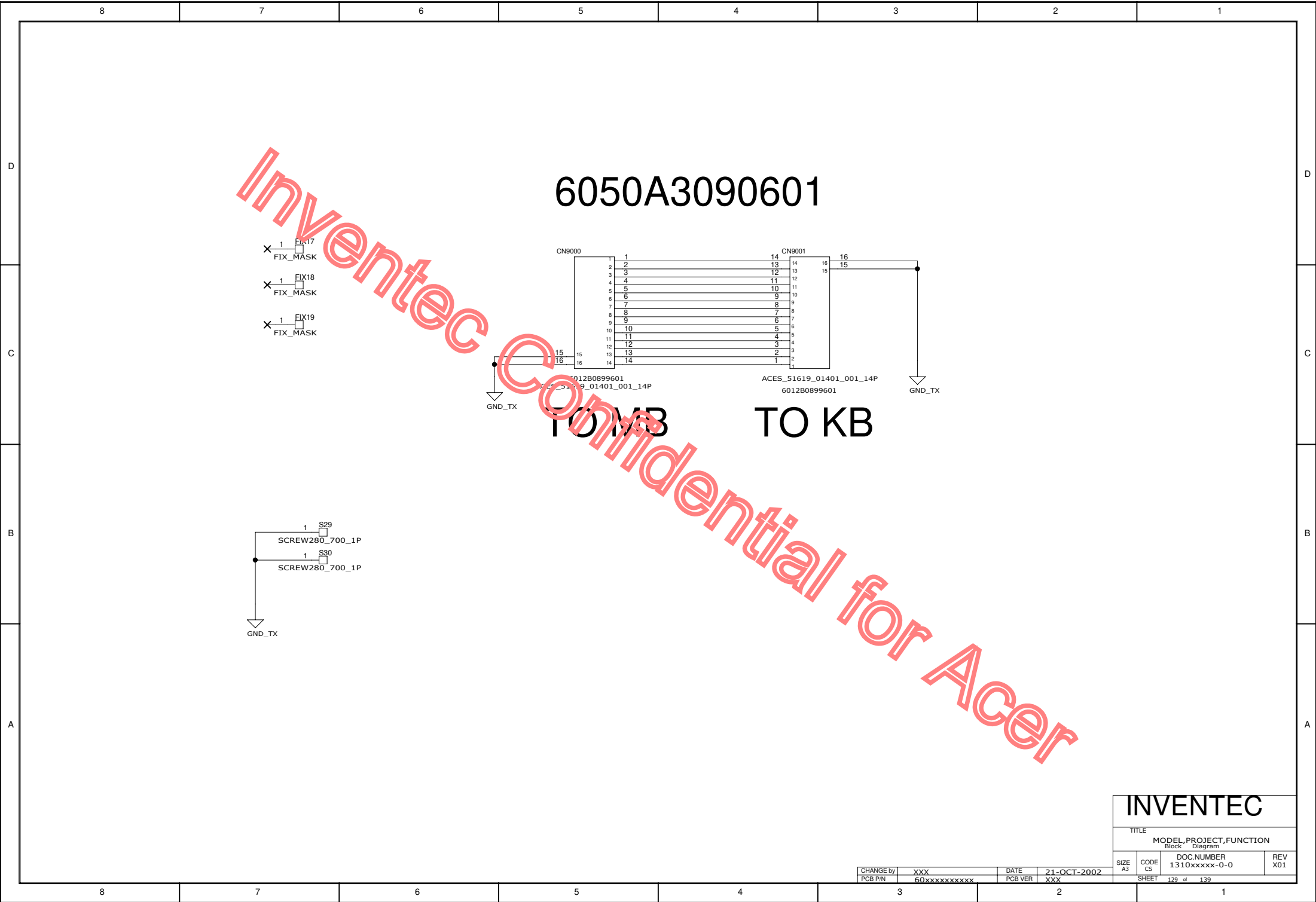
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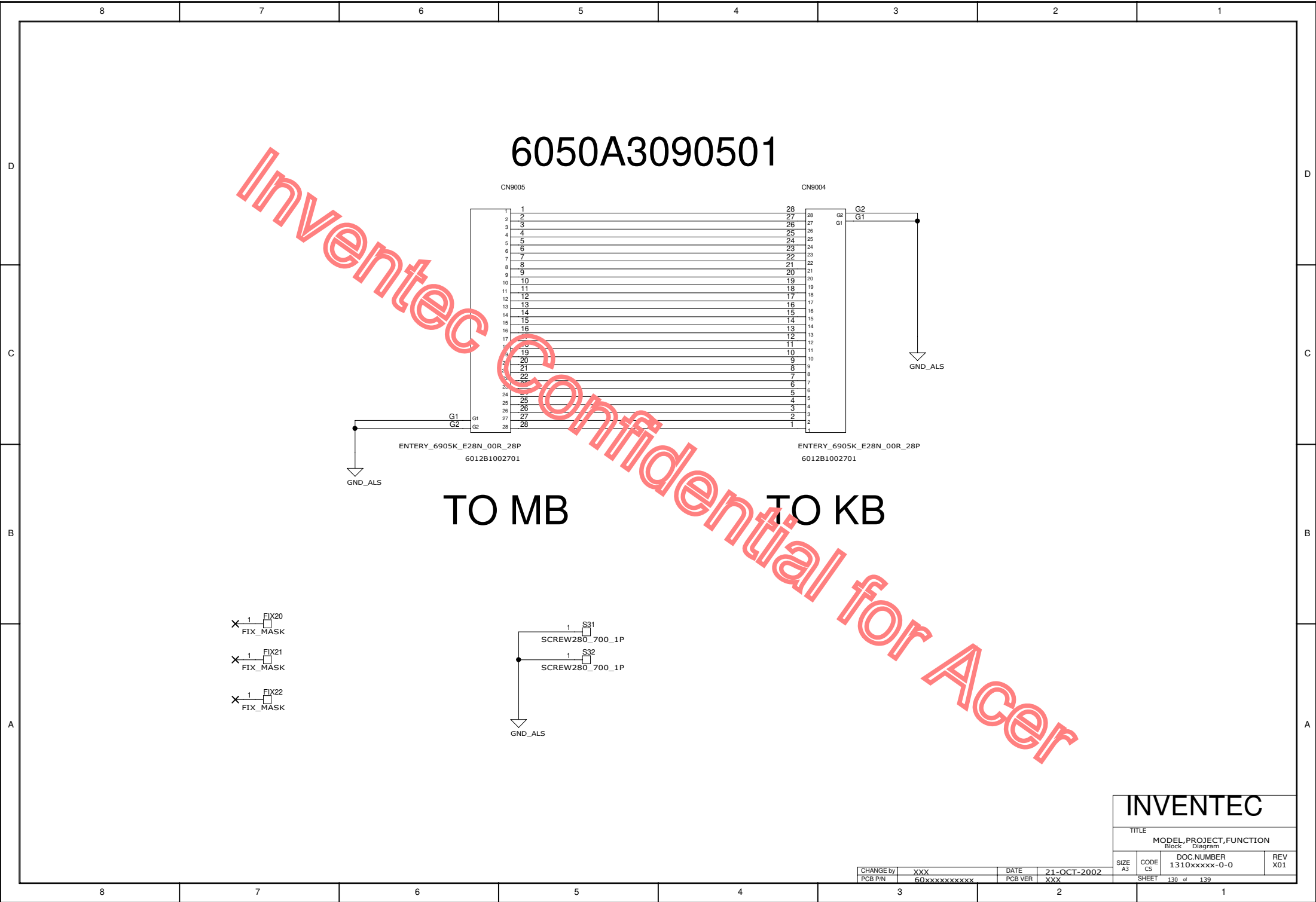
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 128 of 139





TO MB

TO KB

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 130 of 139

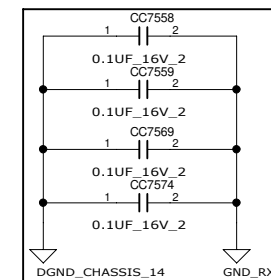
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D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

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FOR '15 AUDIO BOARD

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET

XXX	21-OCT-2002
60xxxxxxxxxx	XXX

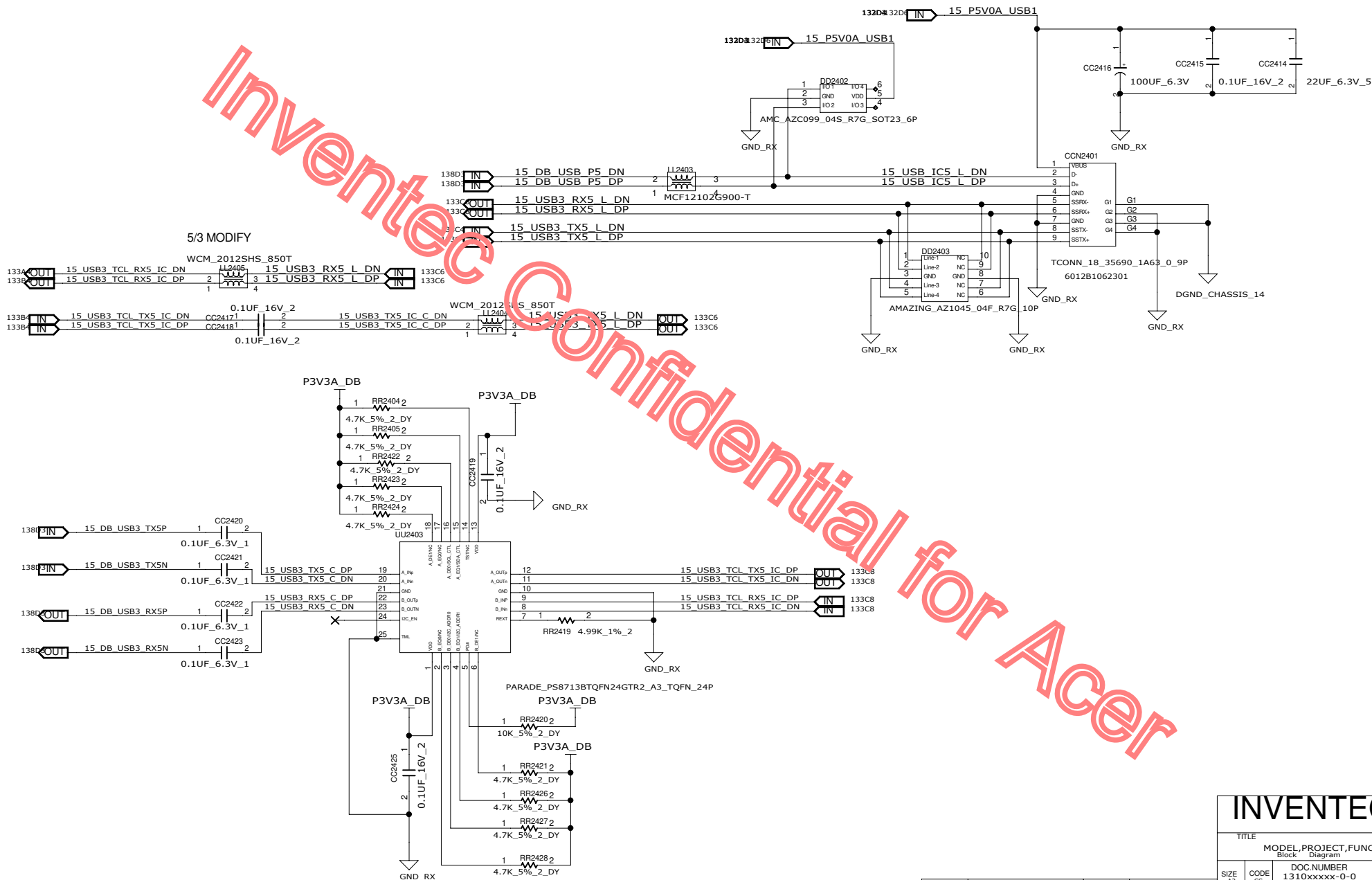


GND_RX  1 SST1900
STANDOFF_3.2_6.0
3.33MM
6052B0407801

INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0		REV X01
SHEET 132 of 130				

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



INVENTEC

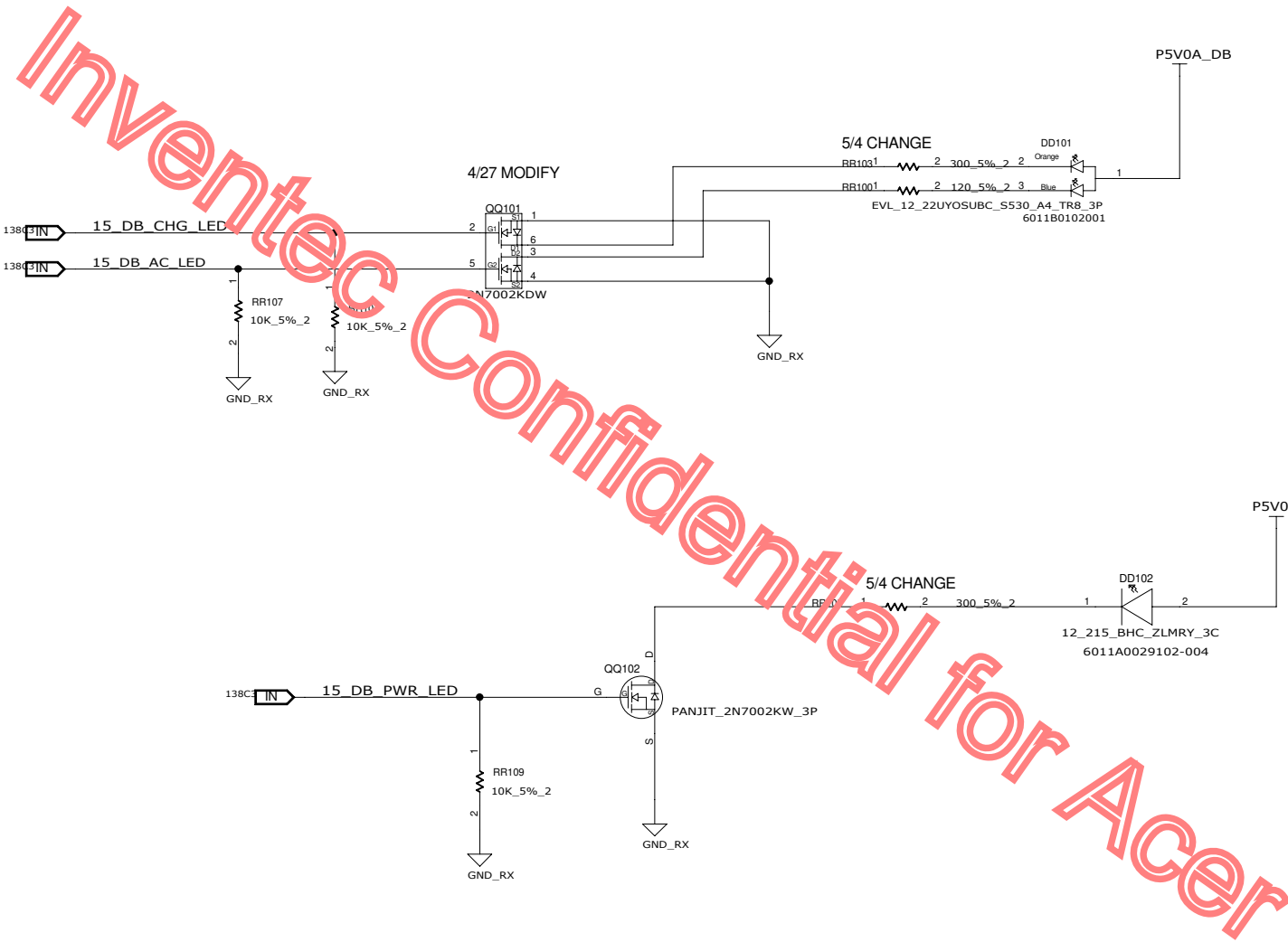
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS 1310xxxxx-0-0 REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

SHEET 133 of 139



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SHEET 134 of 139

The schematic diagram illustrates the electrical connections for a LAN module. Key components and their connections include:

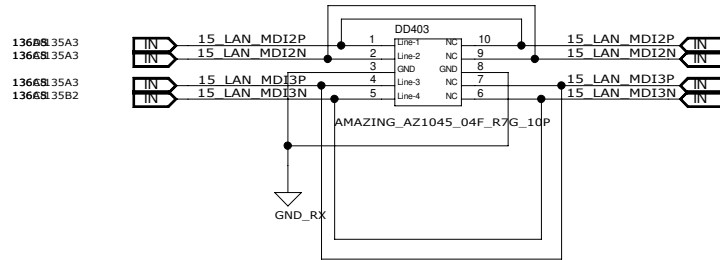
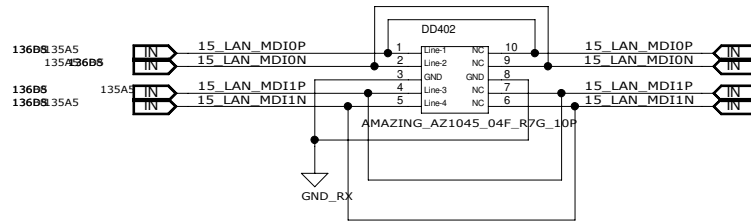
- Power and Grounding:**
 - P3V3A_LAN2:** A 3.3V power supply pin connected to various capacitors (e.g., CC408, CC409, CC410, CC411, CC412, CC424, CC425, CC426, CC427, CC428, CC436, CC437, CC438, CC439, CC440, CC441, CC442, CC443, CC444, CC445, CC446, CC447, CC448, CC449, CC450, CC451, CC452, CC453, CC454, CC455, CC456, CC457, CC458, CC459, CC460, CC461, CC462, CC463, CC464, CC465, CC466, CC467, CC468, CC469, CC470, CC471, CC472, CC473, CC474, CC475, CC476, CC477, CC478, CC479, CC480, CC481, CC482, CC483, CC484, CC485, CC486, CC487, CC488, CC489, CC490, CC491, CC492, CC493, CC494, CC495, CC496, CC497, CC498, CC499, CC500, CC501, CC502, CC503, CC504, CC505, CC506, CC507, CC508, CC509, CC510, CC511, CC512, CC513, CC514, CC515, CC516, CC517, CC518, CC519, CC520, CC521, CC522, CC523, CC524, CC525, CC526, CC527, CC528, CC529, CC530, CC531, CC532, CC533, CC534, CC535, CC536, CC537, CC538, CC539, CC540, CC541, CC542, CC543, CC544, CC545, CC546, CC547, CC548, CC549, CC550, CC551, CC552, CC553, CC554, CC555, CC556, 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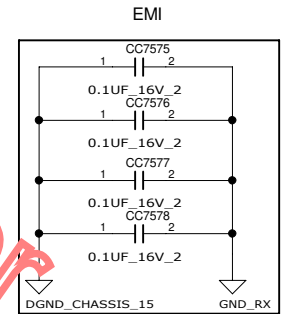
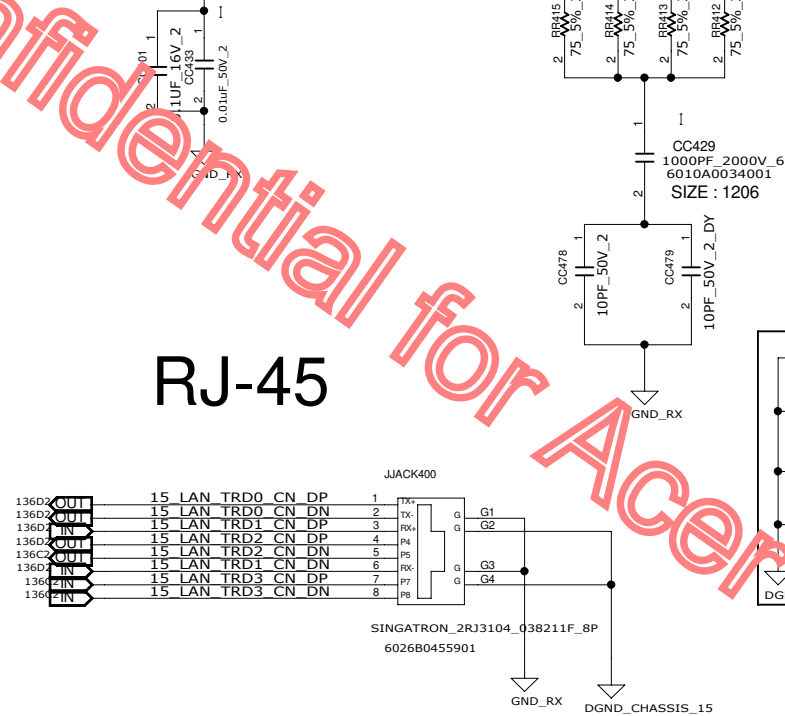
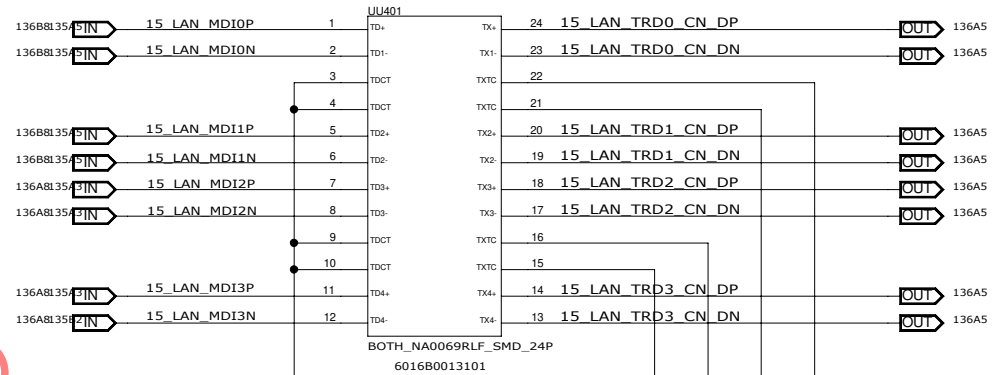
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TRANSFORMER

ESD



RJ-45



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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

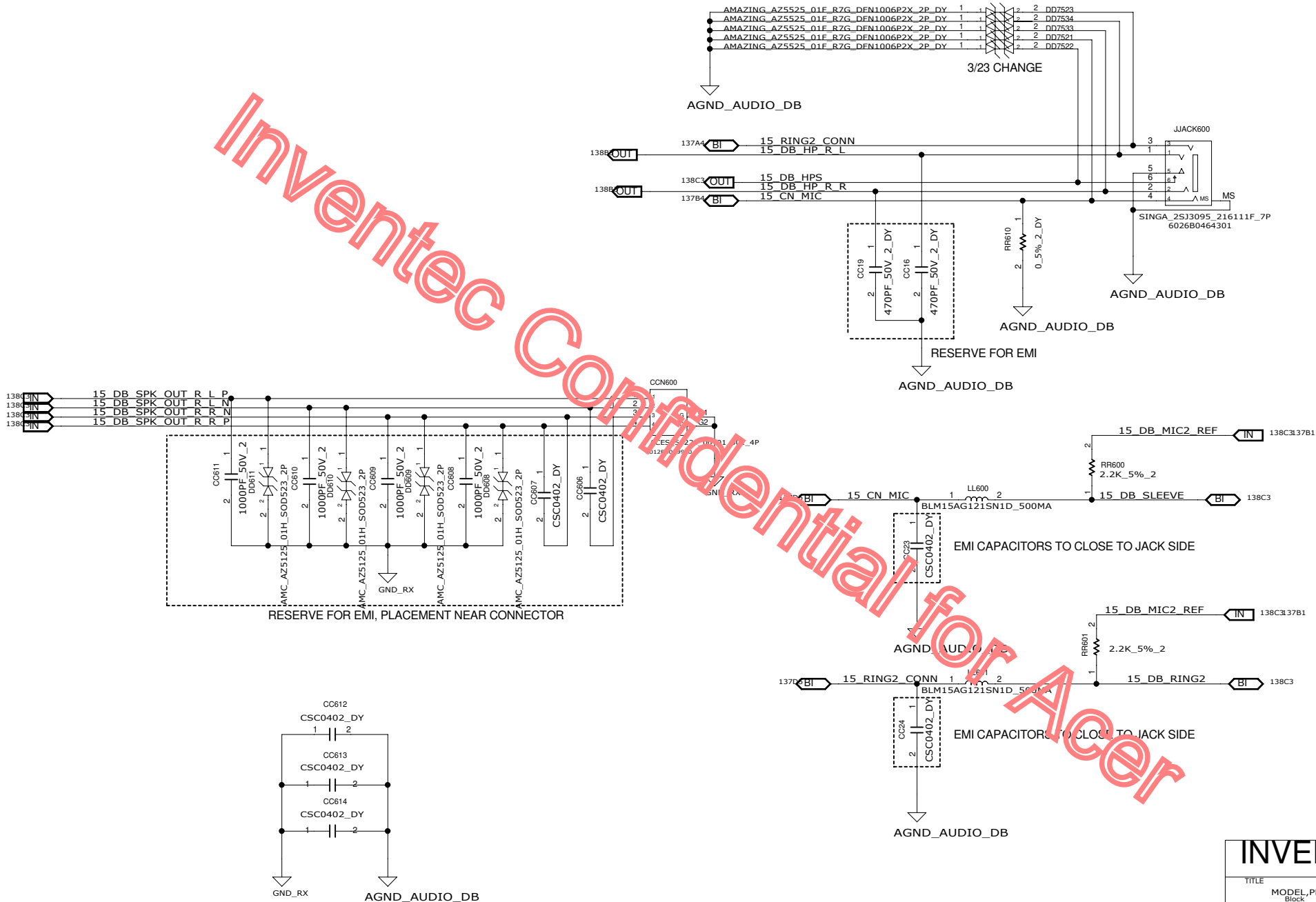
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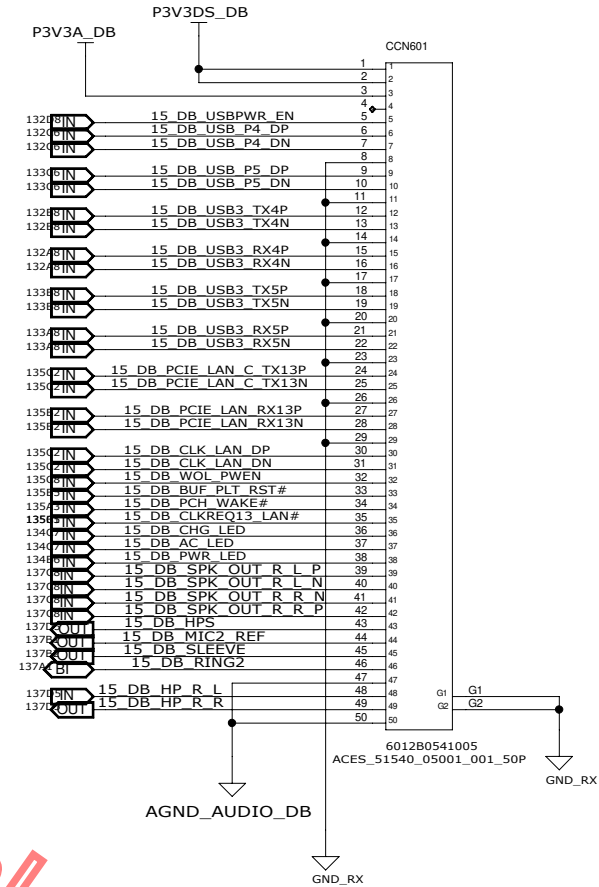
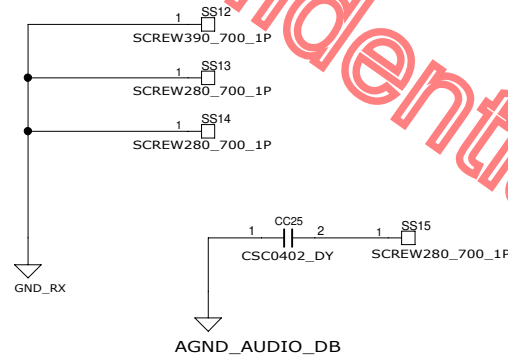
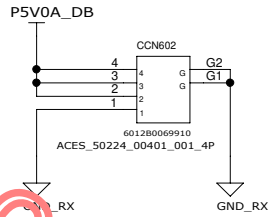
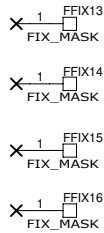
SHEET 136 of 139

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Inventec Confidential for Acer



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INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 138 of 139

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C							
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A							
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INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET

XXX	21-OCT-2002
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