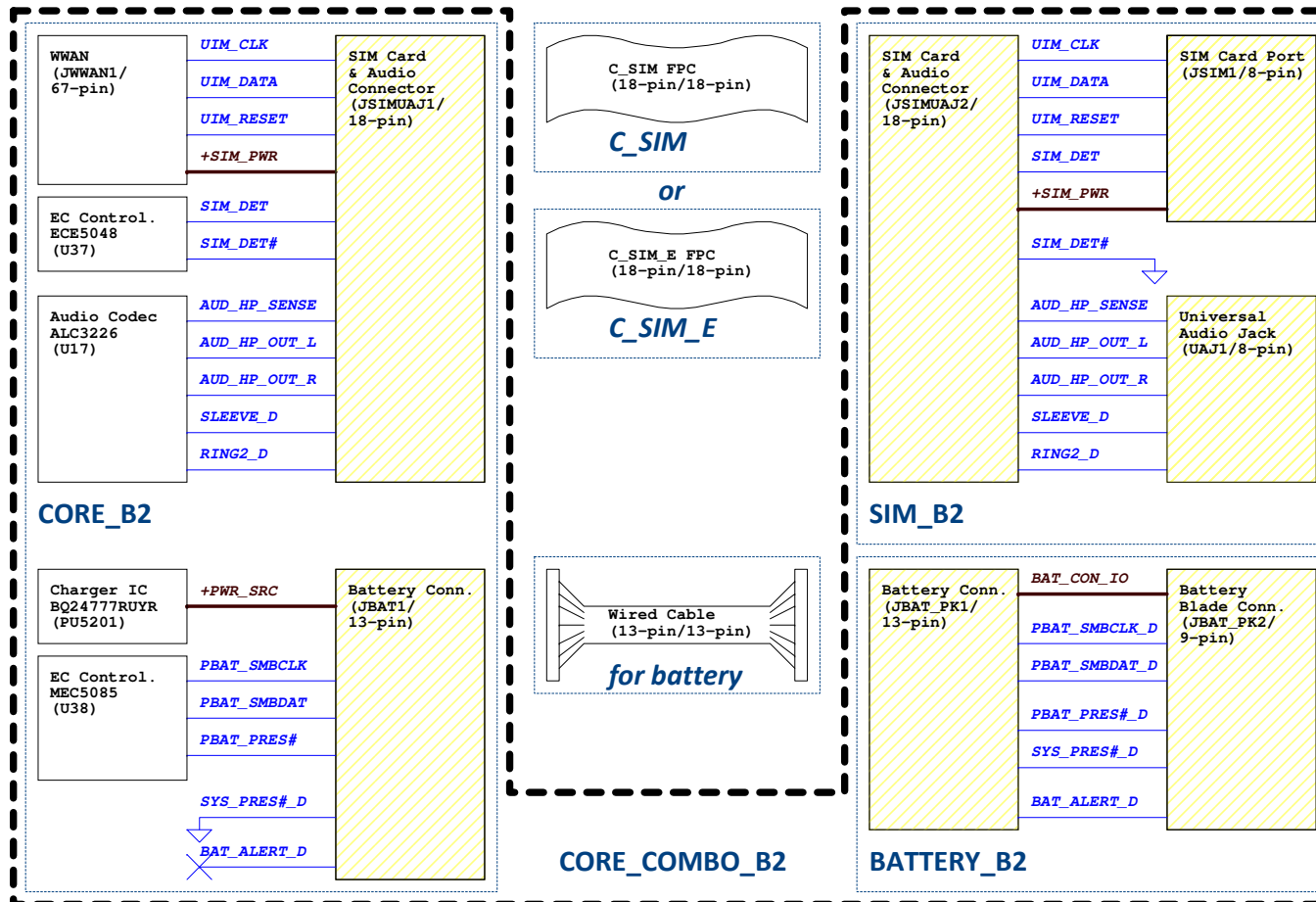


MCE2 A00 Reference Schematic

CORE_COMBO_B2 for Magellan / Columbus / Eriksson Gen2



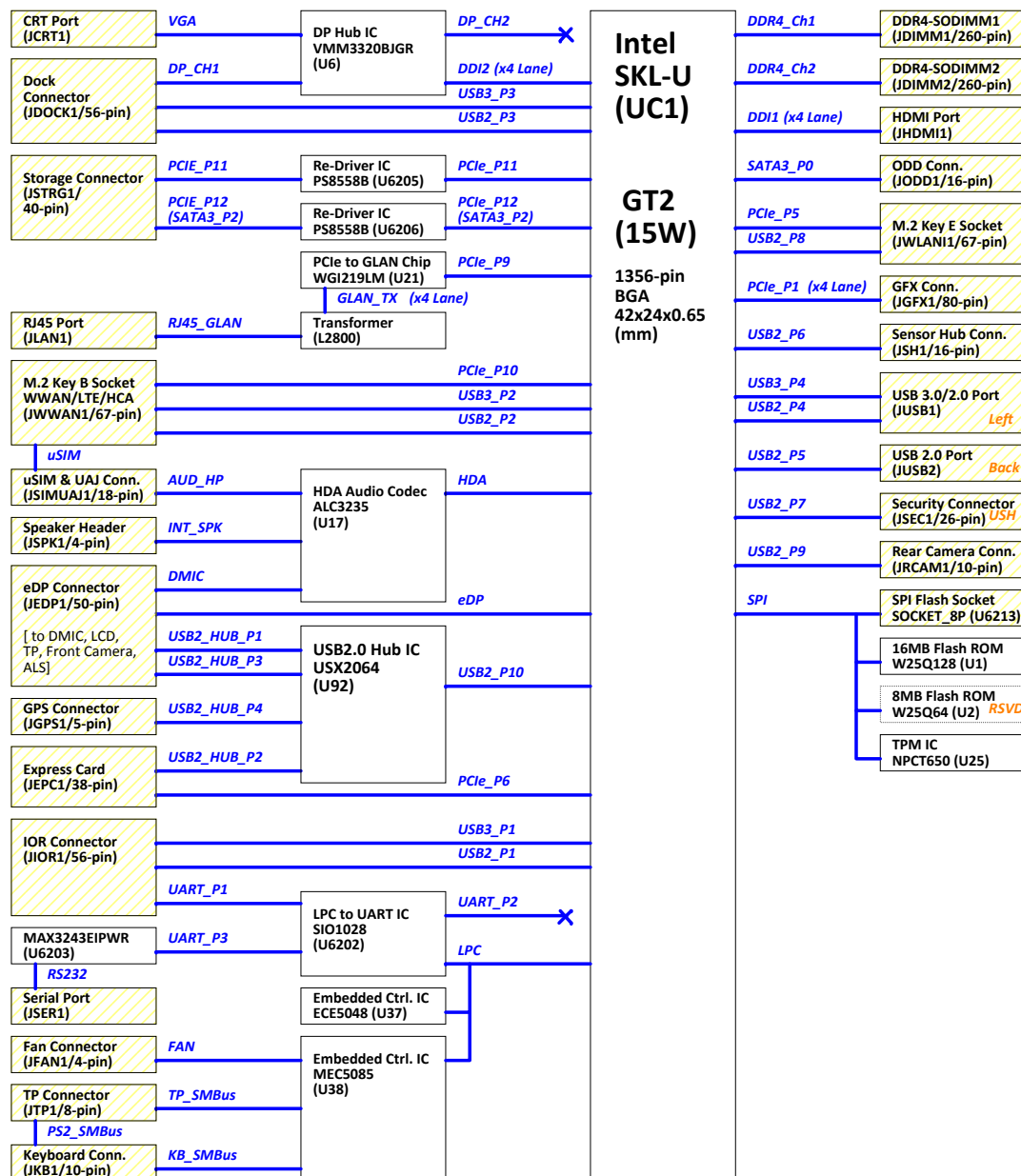
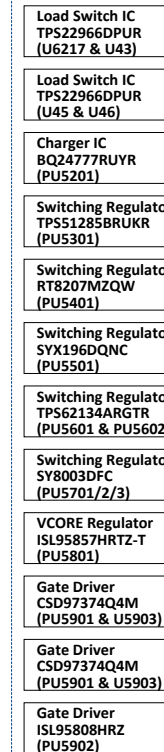
Note: Net names here may not be consistent with real net names in the schematic.

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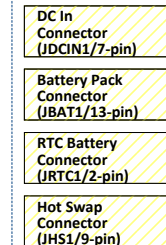
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DWG NO.	CORE_COMBO_B2	REV.	2.0
DATE	Friday, March 18, 2016	SHEET	1 of 81



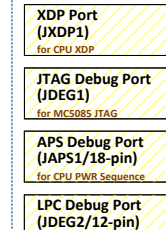
CORE_B2 System Block Diagram (A00)

**Power IC**

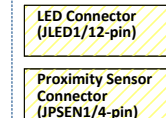
PWR Conn.



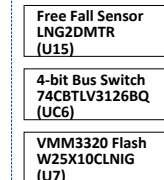
Debug Port



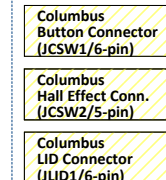
Misc. Conn.



Misc. IC



Col. Conn.



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TITLE		System Block Diagram	
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Note: Net names here may not be consistent with real net names in the schematic.

CORE_B2 Index and Configuraton (A00)

USB2.0 Port Map Configuration

SKL ULT	USB2.0	SCH Conf.	Destination	
	1	USB2_P1	IOR	(JIOR1)
	2	USB2_P2	WWAN	(JWWAN1)
	3	USB2_P3	DOCK	(JDOCK1)
	4	USB2_P4	USB3.0 Port	(JUSB1)
	5	USB2_P5	USB2.0 Port	(JUSB2)
	6	USB2_P6	Sensor Hub	(JSH1)
	7	USB2_P7	USH	(JSEC1)
	8	USB2_P8	Bluetooth	(JWLAN1)
	9	USB2_P9	Rear Cam	(JRCAM1)
10	USB2_P10	USB Hub	(TS, FCam, EC/PC, GPS)	

USH Configuration

USH	0	BIO
	1	NA

POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALW PLANE	M PLANE	SUS PLANE	RUN PLANE	CLK
S0 (Full ON) with M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) with M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) with M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) with M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) with M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) with M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) with M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIe/USB3.0/SATA Port Map Configuration

USB3.0	SSIC	PCIE	SATA	SCH Conf.	Destination	
USB3.0 1				USB3_P1	IOR	(JIOR1)
USB3.0 2	SSIC 1			USB3_P2	WWAN	(JWWAN1)
USB3.0 3	SSIC 2			USB3_P3	DOCK	(JDOCK1)
USB3.0 4				USB3_P4	USB3.0 Port	(JUSB1)
USB3.0 5		PCIE 1		PCle_P1	GFX	(JGFX1)
USB3.0 6		PCIE 2				
		PCIE 3				
		PCIE 4				
		PCIE 5		PCle_P5	WLAN	(JWLAN1)
		PCIE 6		PCle_P6	Express/PC Card	(JEPC1)
		PCIE 7	SATA 0	SATA3_P0	ODD	(JODD1)
		PCIE 8	SATA 1	PCle_P8	N/A	(N/A)
		PCIE 9		PCle_P9	LOM	(U21)
		PCIE 10		PCle_P10	WWAN	(JWWAN1)
		PCIE 11	SATA 1*	PCle_P11&P12	SATA Express HDD	(JSTRG1)
		PCIE 12	SATA 2	SATA_P2		

PM TABLE

power plane \ State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.0V_PRIM_CORE +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +VCC_CORE +VCC_GT	+3.3V_M	(M-OFF) +3.3V_M
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/No AC	OFF	OFF	OFF	OFF	OFF

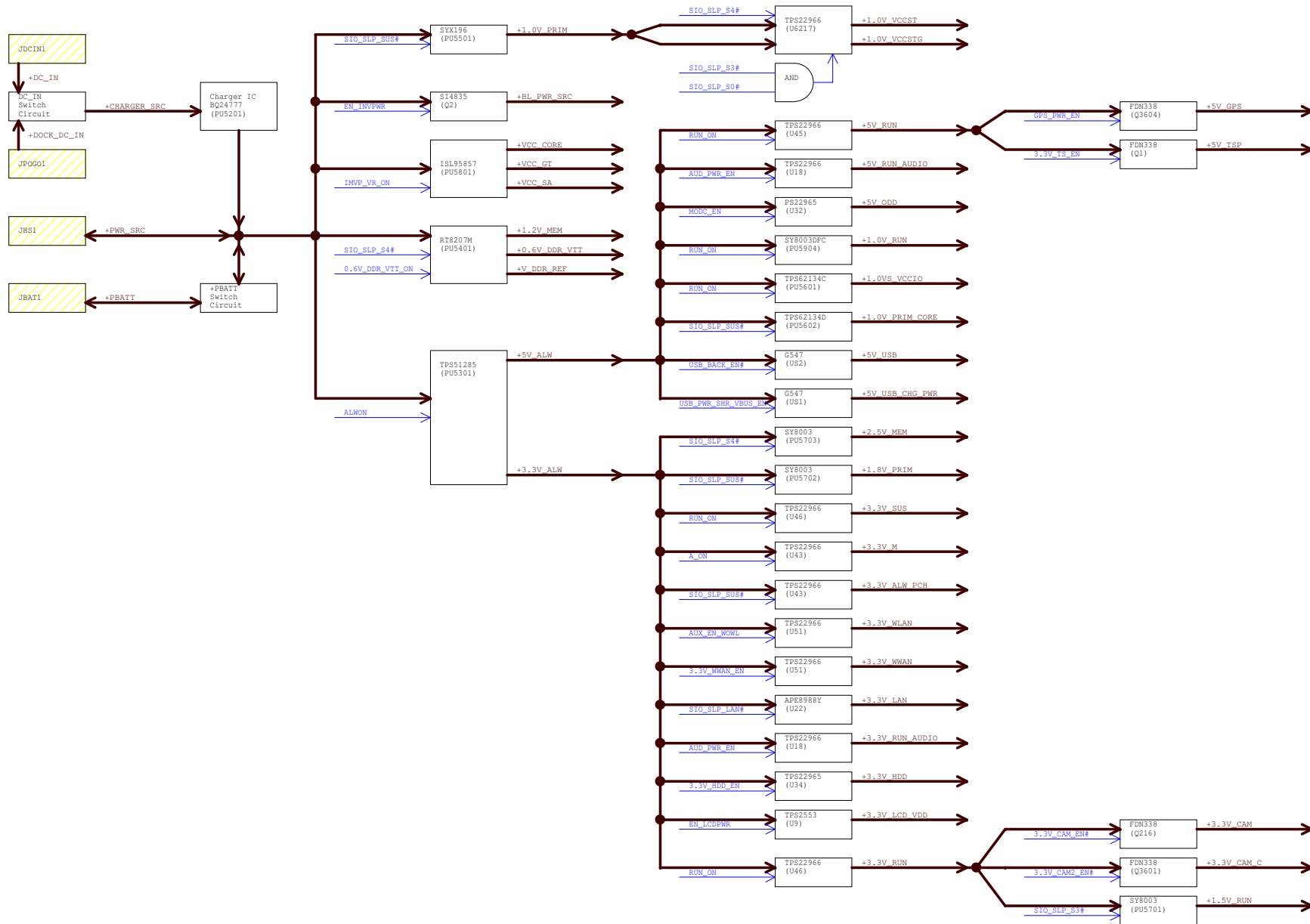
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TITLE Port Map	
DWG NO. CORE_B2	REV. 2.0
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CORE_B2 Power Rail (A00)



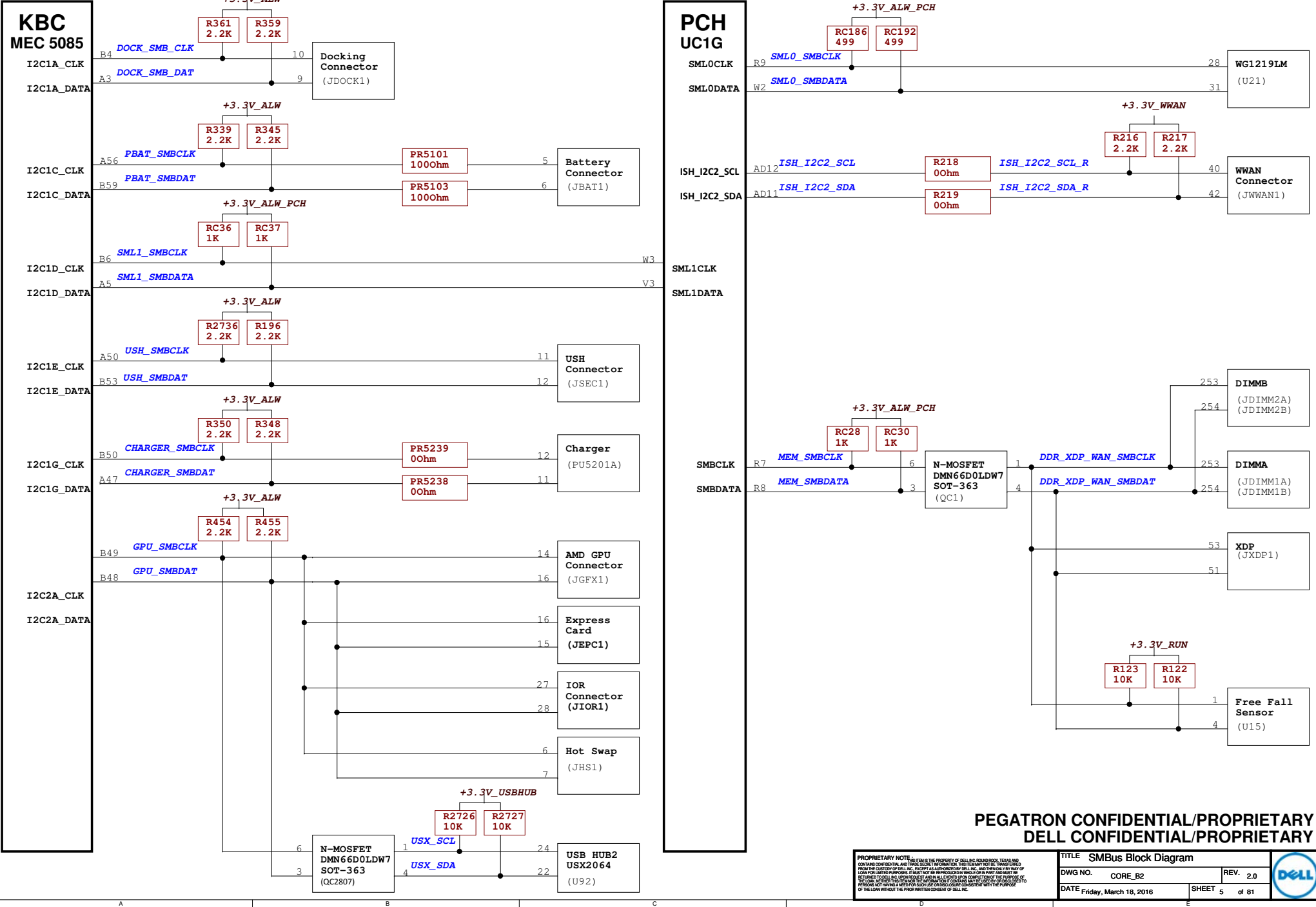
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TITLE		Power Rail	
DWG NO.		CORE_B2	REV. 2.0
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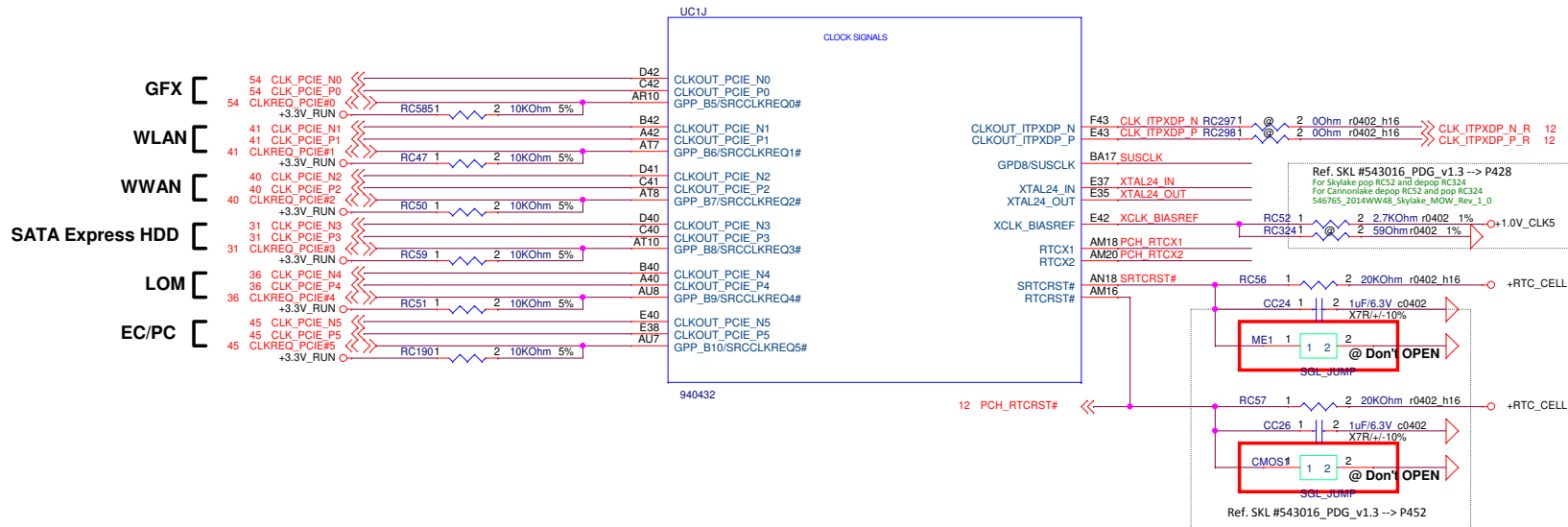
CORE_B2 SMBus Block Diagram (A00)



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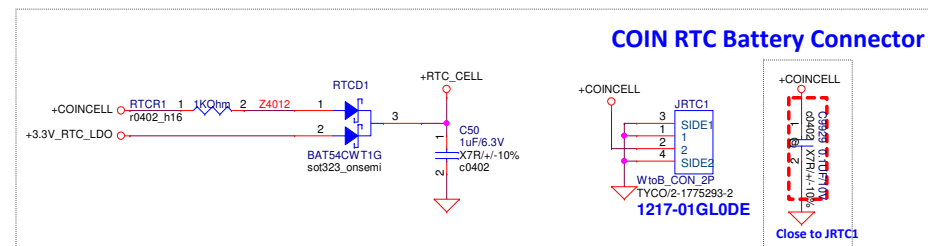
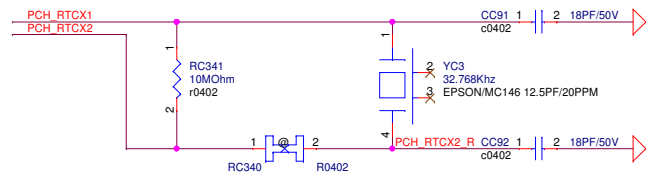
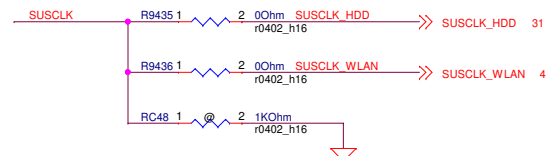
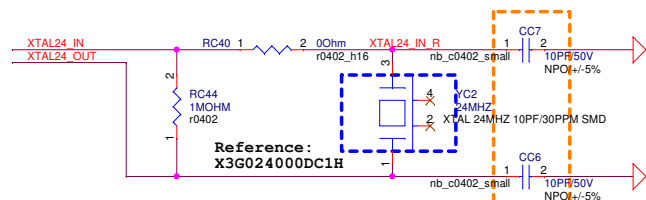
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DWG NO.	CORE_B2	REV.	2.0
DATE	Friday, March 18, 2016	SHEET	5 of 81





ME1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



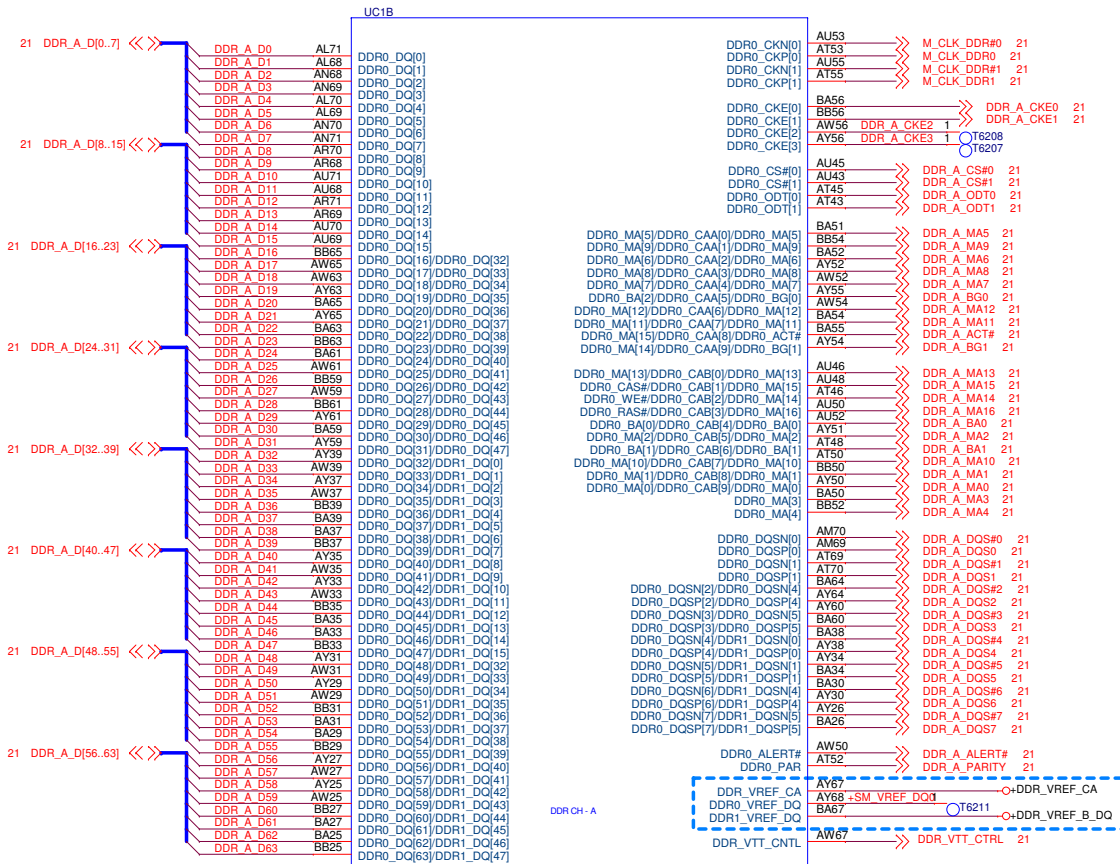
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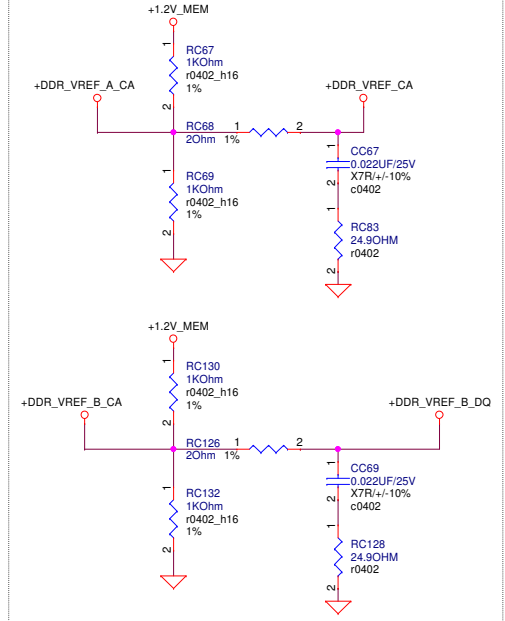
TITLE	CPU_03 CLK/XTAL/JRTC1
DWG NO.	CORE_B2
REV.	2.0
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DDR Interleave routing



Place near to SO-DIMM connector.



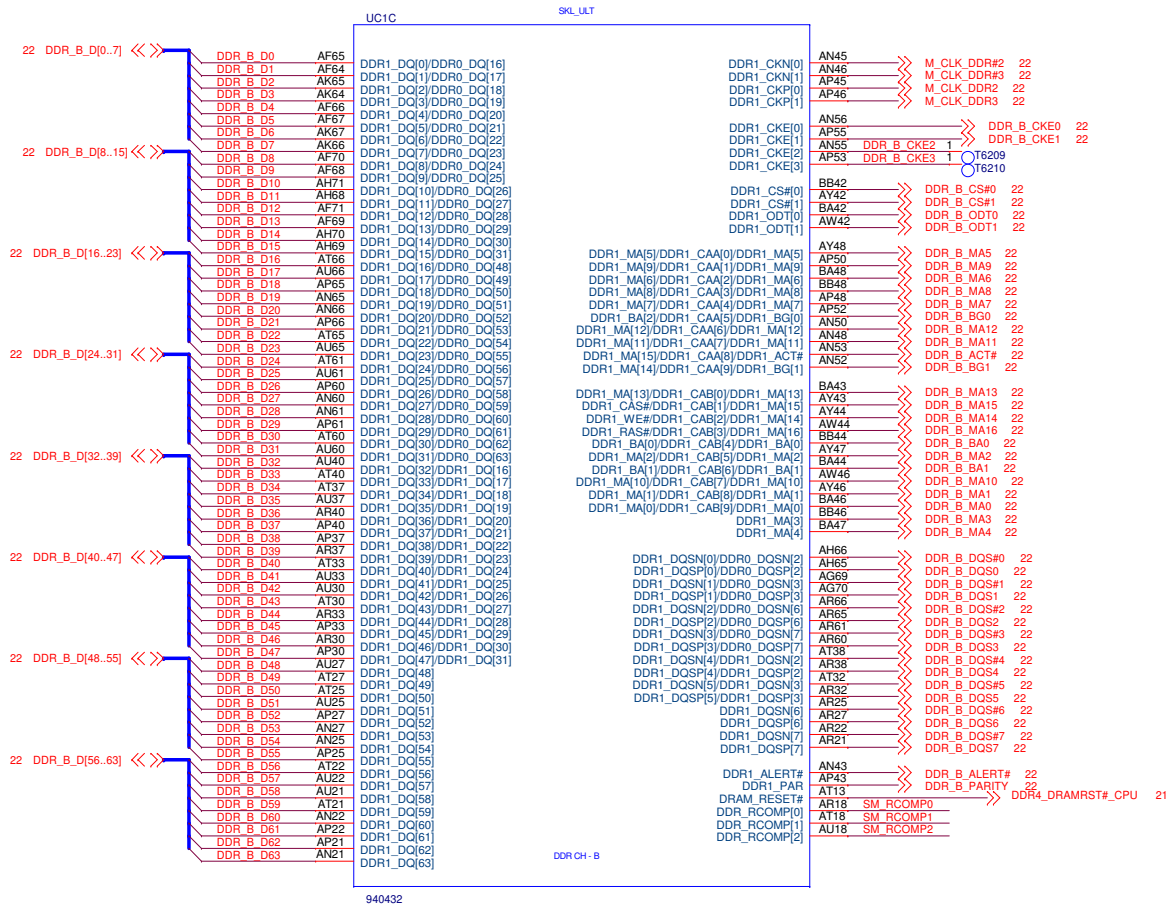
Ref. SKL #543016_PDG1.3--> P179

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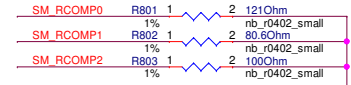
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DWG NO. CORE_B2		REV. 2.0	
DATE Friday, March 18, 2016		SHEET 9 of 81	



DDR interleave routing



DDR4 COMPENSATION SIGNALS



Layout Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Ref. SKL #543016_PDG1.3--> P151

Interleaved Memory

Ref. SKL #544924_EDS_v0.95--> P32

IL		IL	
Channel	Byte	Channel	Byte
DDR0	Byte0	DDR1	Byte0
DDR0	Byte1	DDR1	Byte1
DDR0	Byte2	DDR1	Byte2
DDR0	Byte3	DDR1	Byte3
DDR0	Byte4	DDR1	Byte4
DDR0	Byte5	DDR1	Byte5
DDR0	Byte6	DDR1	Byte6
DDR0	Byte7	DDR1	Byte7

NIL		NIL	
Channel	Byte	Channel	Byte
DDR0	Byte0	DDR0	Byte2
DDR0	Byte1	DDR0	Byte3
DDR0	Byte4	DDR0	Byte6
DDR0	Byte5	DDR0	Byte7
DDR1	Byte0	DDR1	Byte2
DDR1	Byte1	DDR1	Byte3
DDR1	Byte4	DDR1	Byte6
DDR1	Byte5	DDR1	Byte7

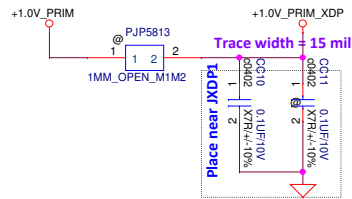
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TITLE CPU_05 DDR4 Channel 1		
DWG NO. CORE_B2	REV. 2.0	
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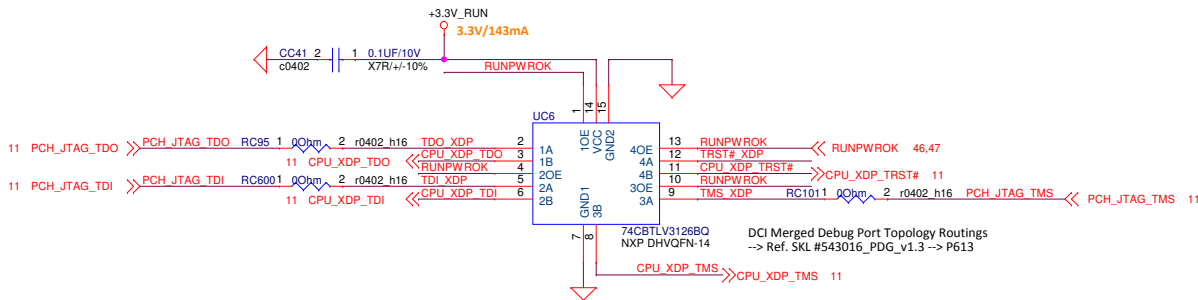
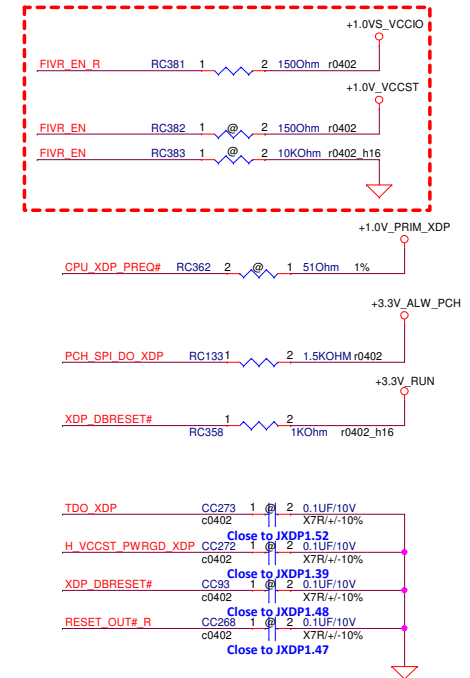
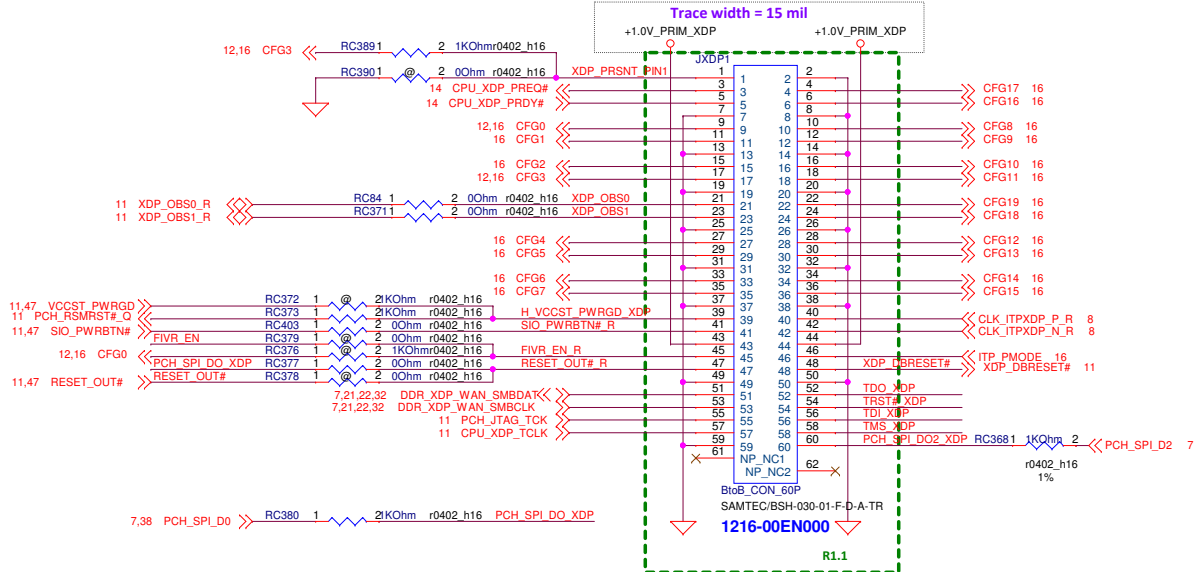


CPU XDP Power

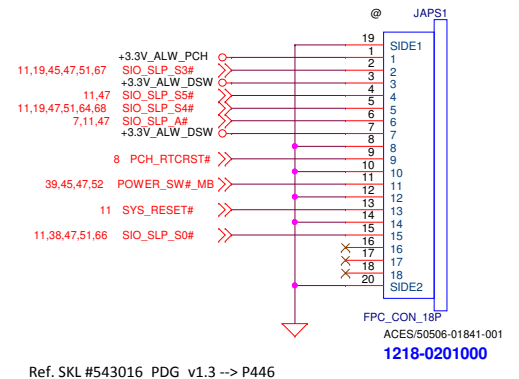


CPU XDP Connector

Ref. SKL #543016_PDG_v1.3 --> P627



CPU APS Connector

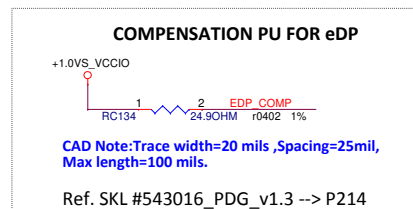
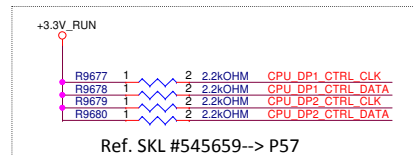
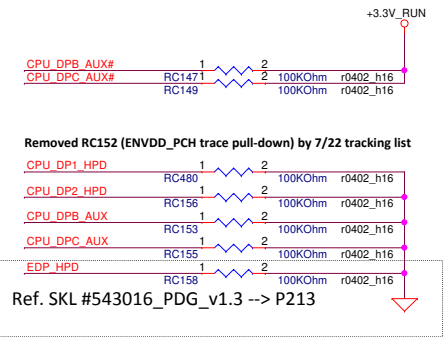
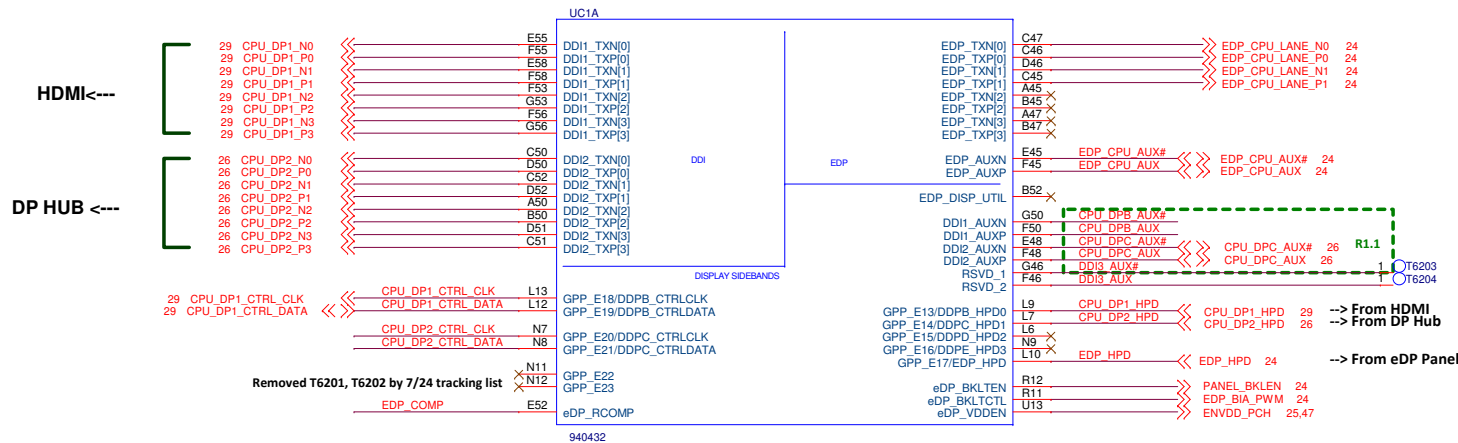


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TITLE	CPU_07 JAPS1/JXDP1	
DWG NO.	CORE_B2	REV. 2.0
DATE	Friday, March 18, 2016	SHEET 12 of 81

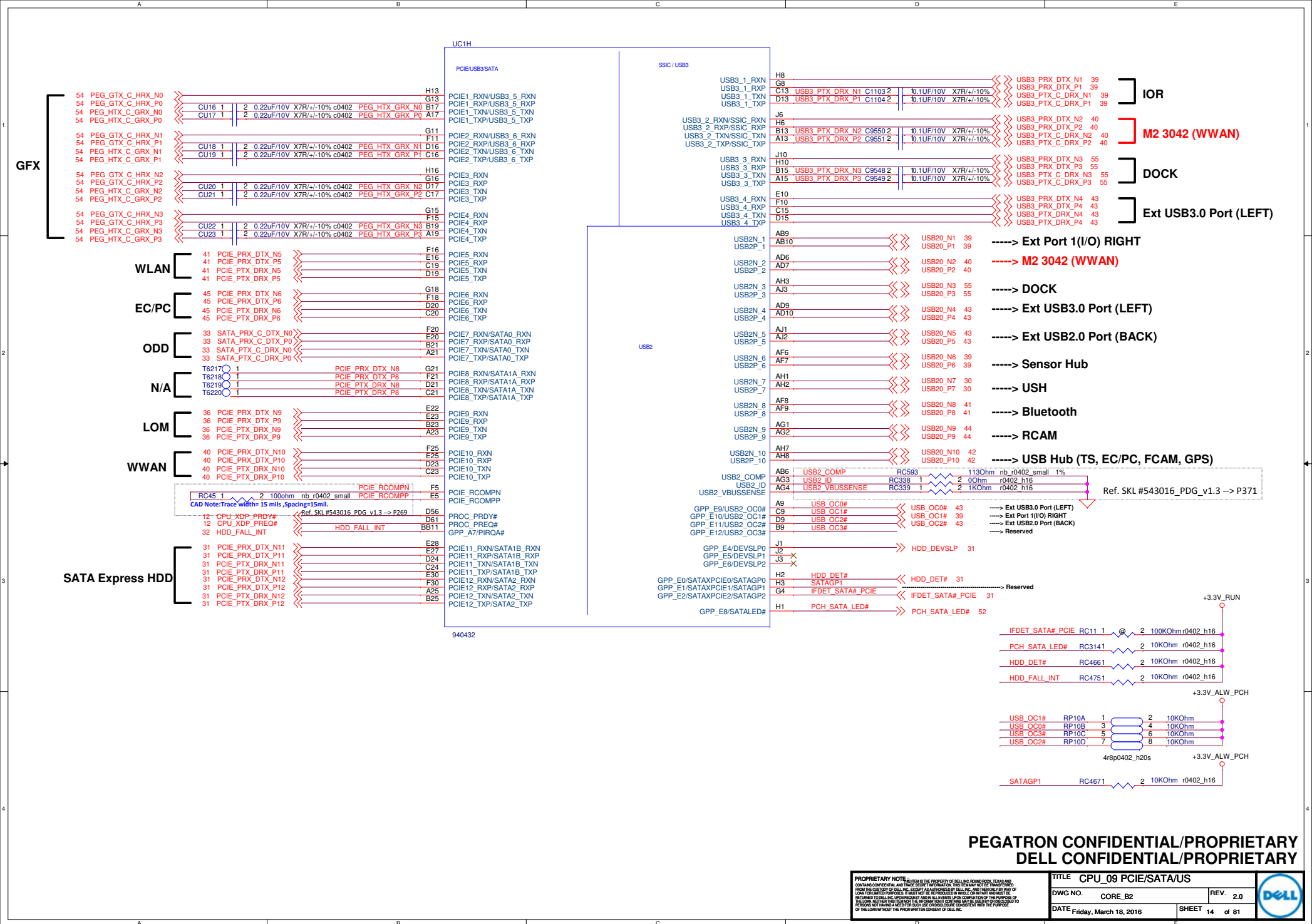


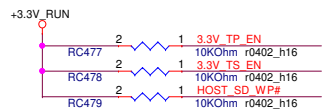
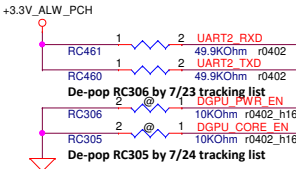
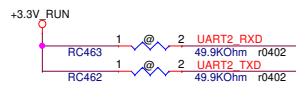


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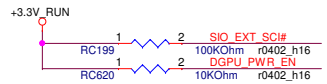
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TITLE		CPU_08 DD/EDP	
DWG NO.	CORE_B2	REV.	2.0
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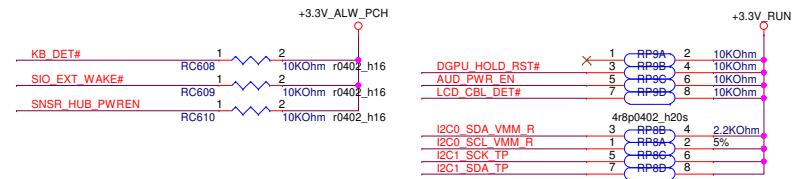
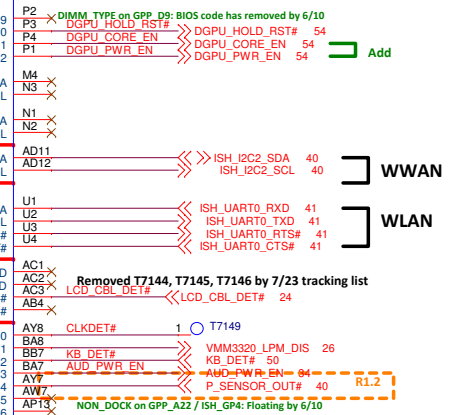
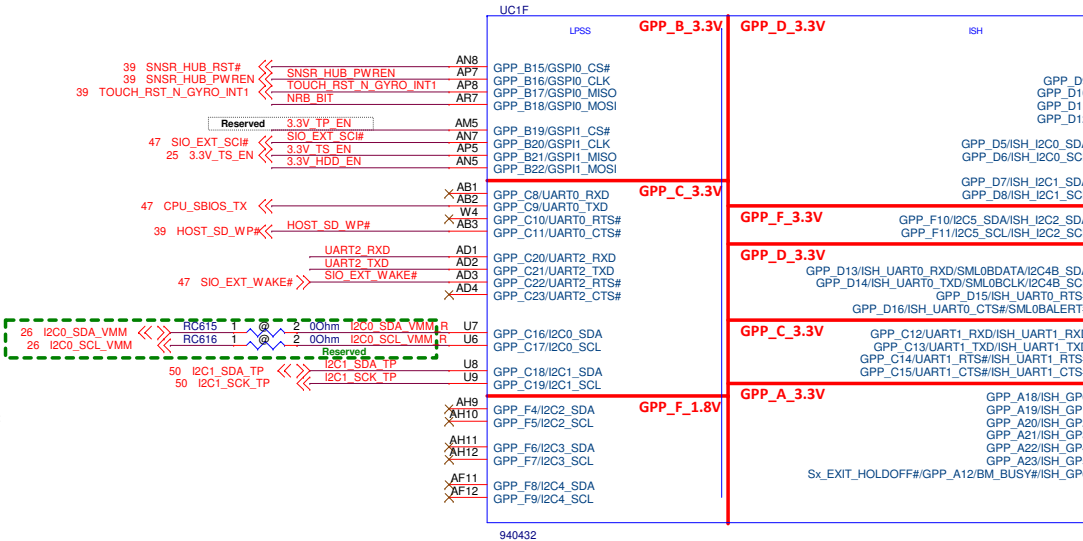
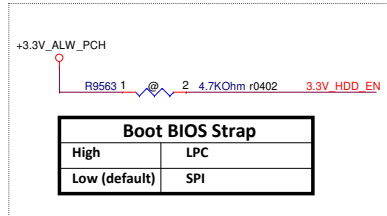
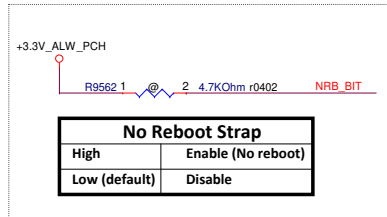


Removed RC482 ~ RC485 by 7/27 tracking list



Added RC620 by 7/23 tracking list

RC620 change to 10kohm from 100kohm by 7/24 tracking list



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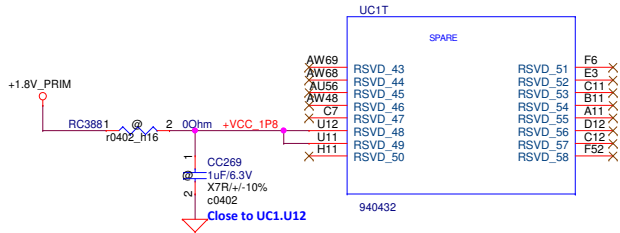
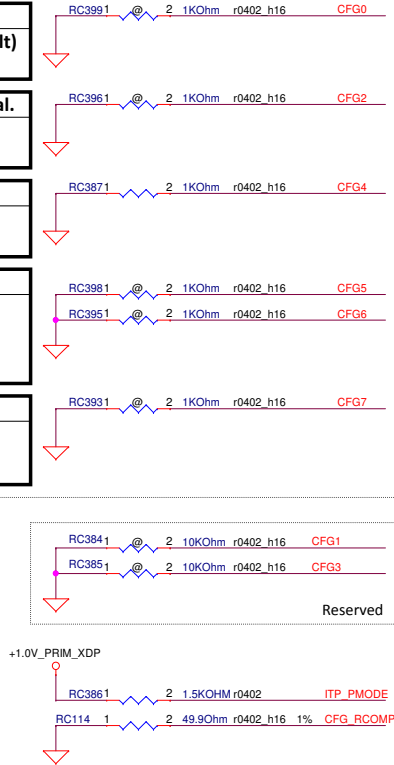
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TITLE	CPU_10 GPIO/I2C/ISH	
DWG NO.	CORE_B2	REV. 2.0
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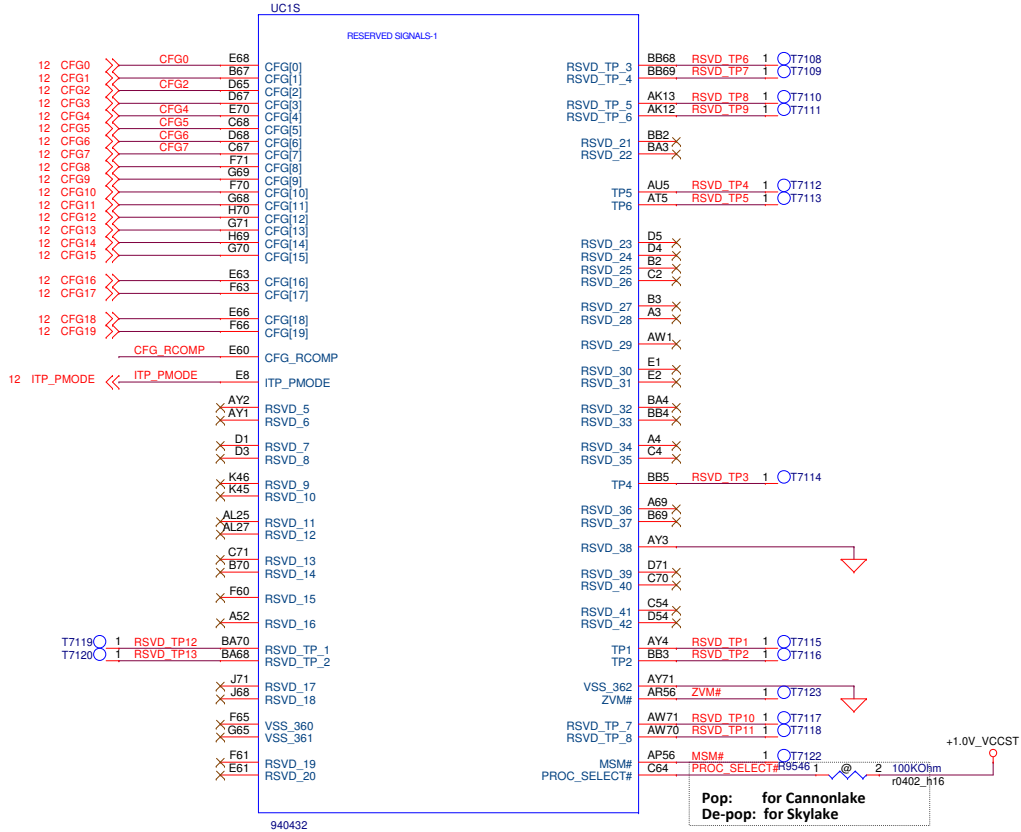


Configuration Signals: (Ref. SKL #544924_EDS_v0.94--> P170)

Stall reset sequence after PCU PLL lock	
CFG0	1 : No stall, Normal Operation (default) 0 : Stall.
PCI Express* Static x16 Lane Numbering Reversal.	
CFG2	1 : Normal operation. (default) 0 : Lane numbers reversed.
Display Port Presence Strap	
CFG4	1 : Disabled 0 : Enabled (default)
PCI Express* Bifurcation.	
CFG5 CFG6	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express* (default)
PEG Training	
CFG7	1 : PEG train immediately following RESET# de assertion. (default) 0 : PEG wait BIOS for training.



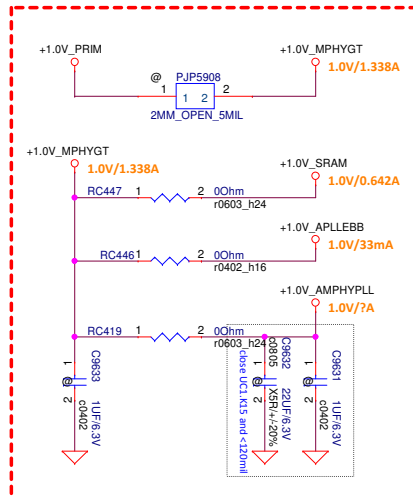
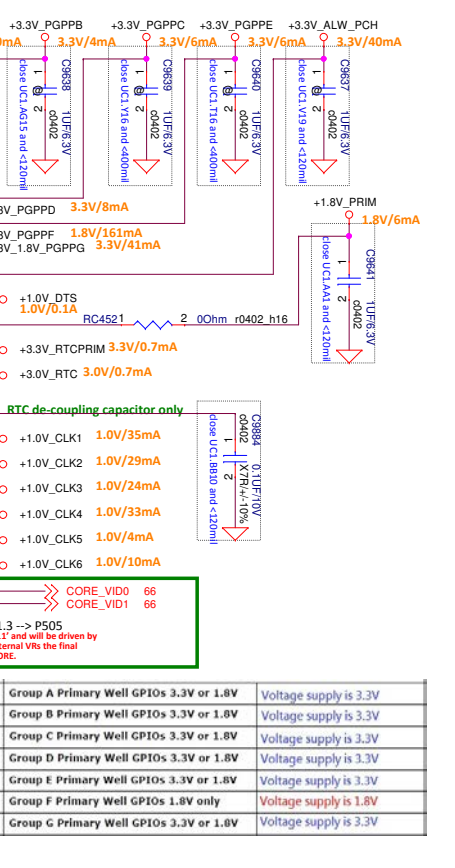
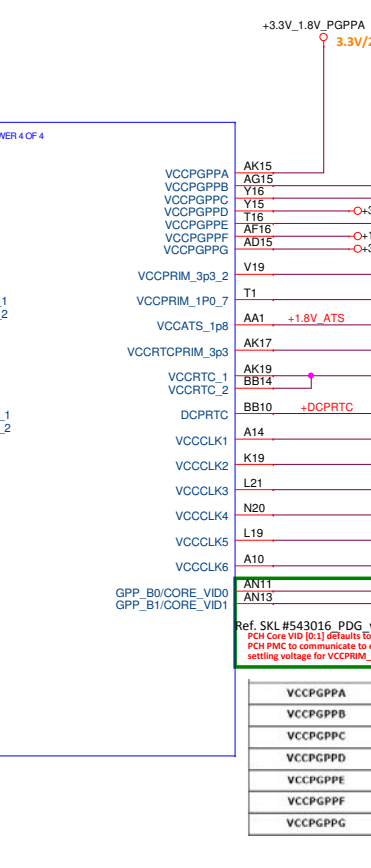
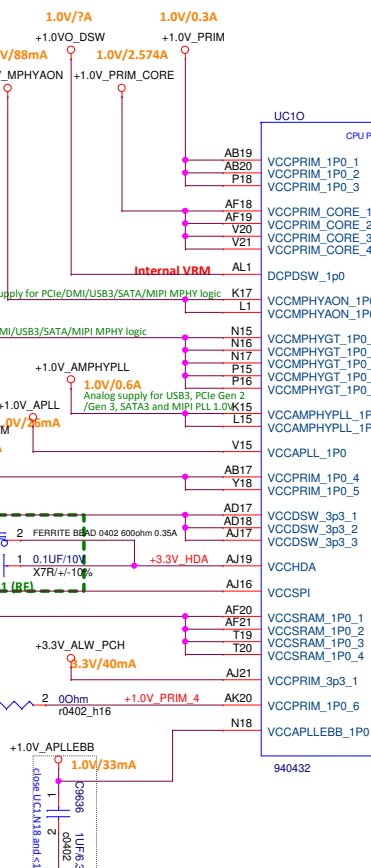
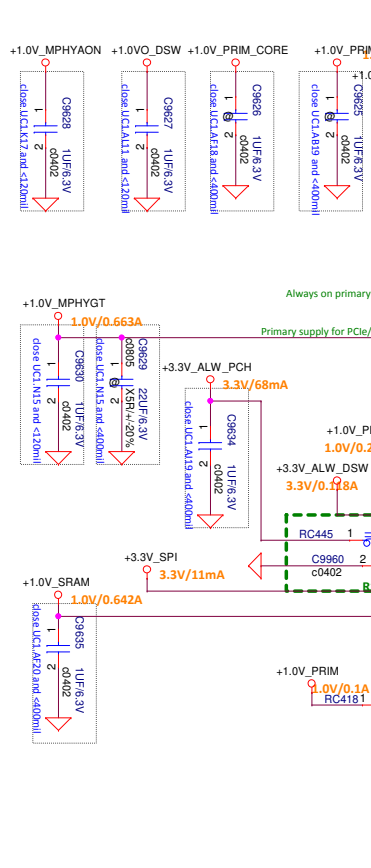
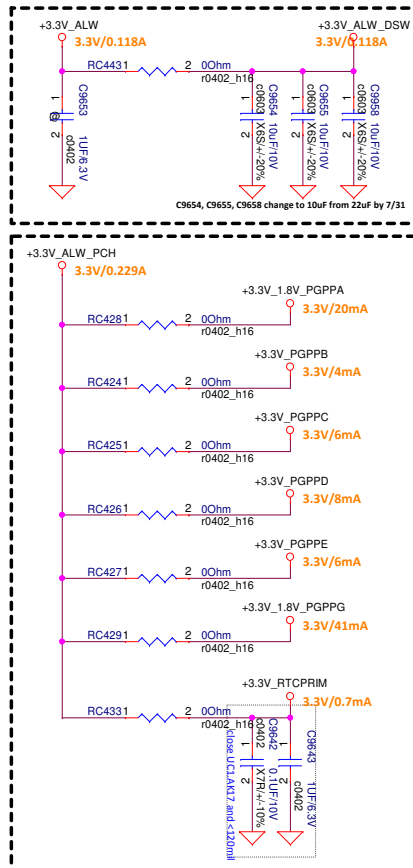
CFG STRAPS for CPU



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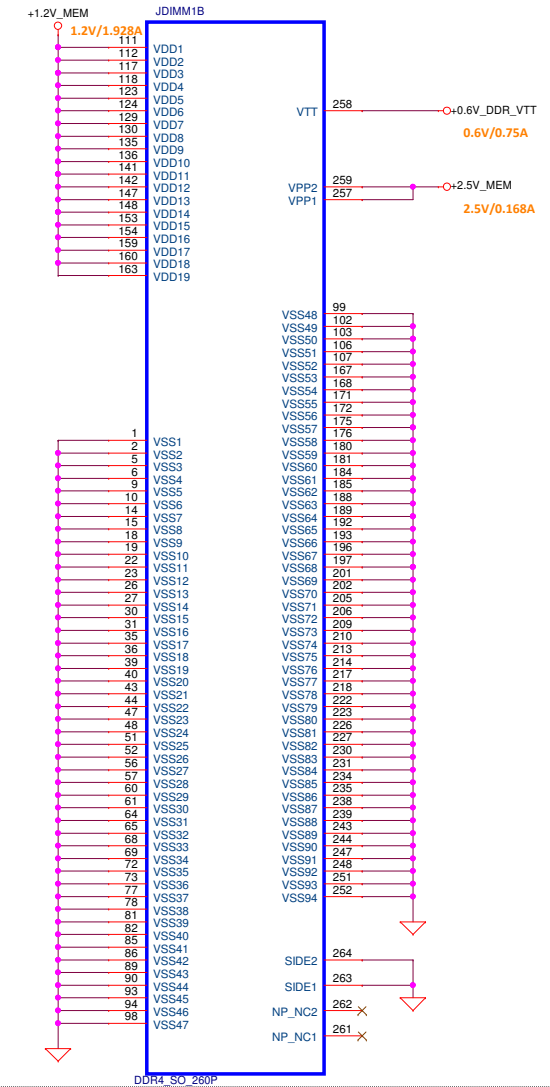
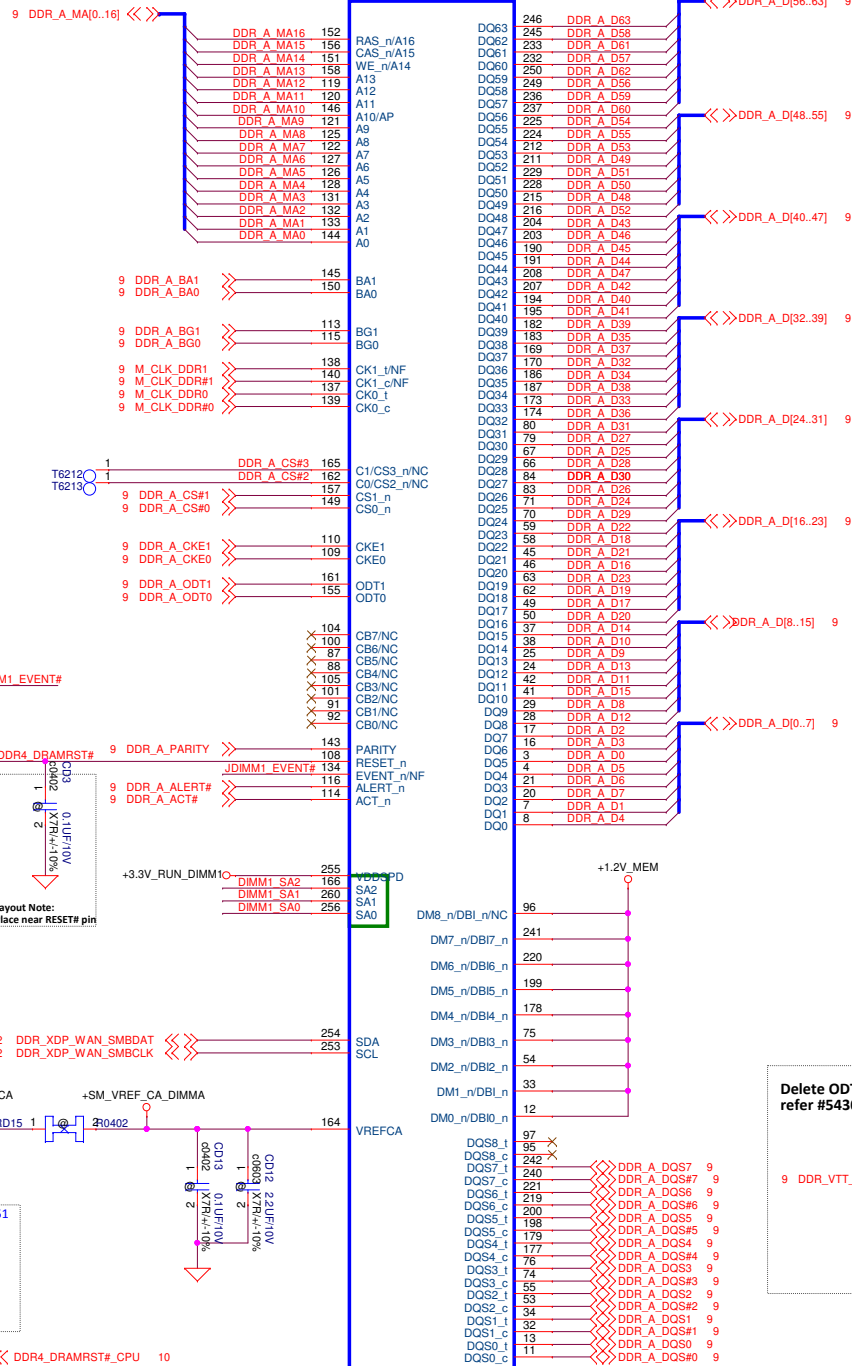
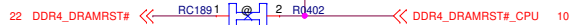
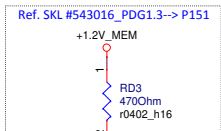
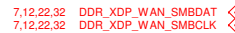
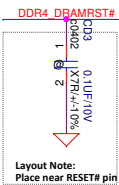
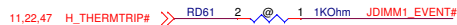
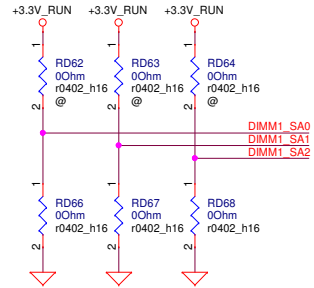
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DWG NO.	CORE_B2	REV.	2.0
DATE	Friday, March 18, 2016	SHEET	16 of 81



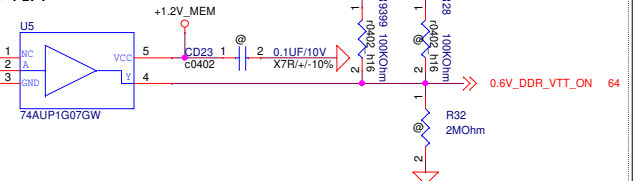


(I2C slave address select for SPD)

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



9 DDR_VTT_CTRL



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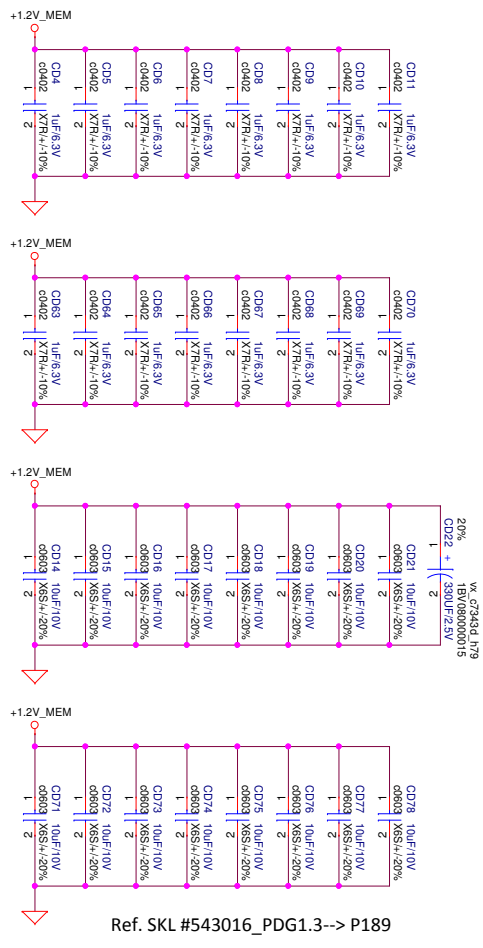
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TITLE		DDR4 JDIMM1		
DWG NO.		CORE_B2	REV. 2.0	
DATE		Friday, March 18, 2016	SHEET 21 of 81	

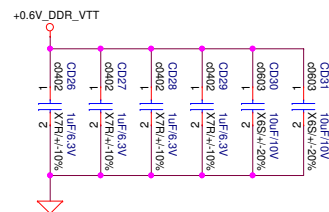


DDR4 DIMM1

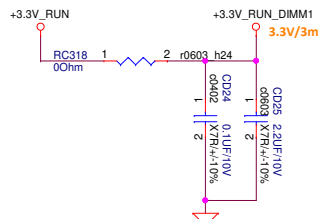
Layout Note:
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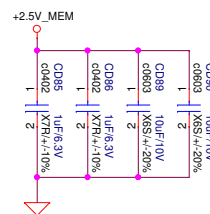
Layout Note:
Place near JDIMM1.258



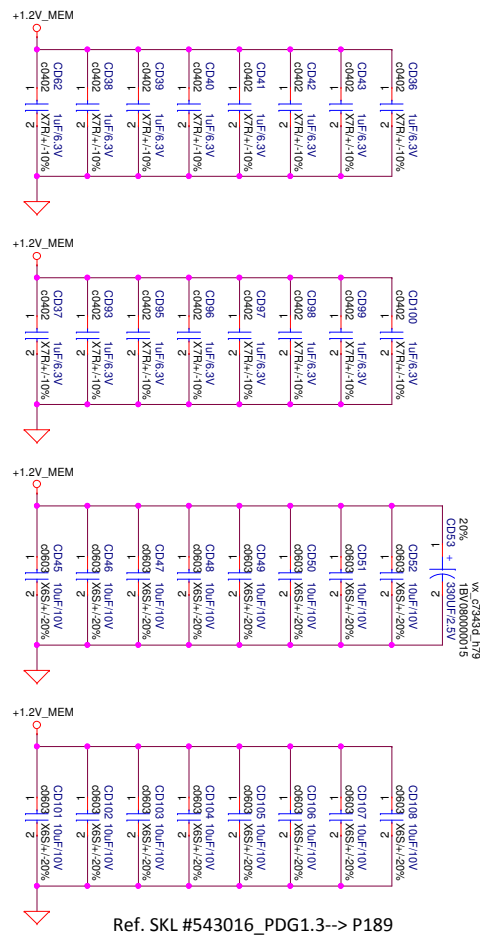
Layout Note:
Place near JDIMM1.255



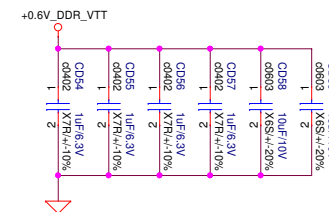
Layout Note:
Place near JDIMM1.257,259



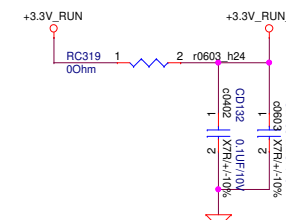
Layout Note:
Place near JDIMM2



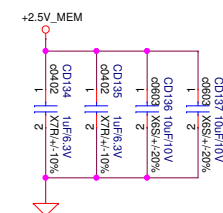
Layout Note:
Place near JDIMM2.258



Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMM2.257,259



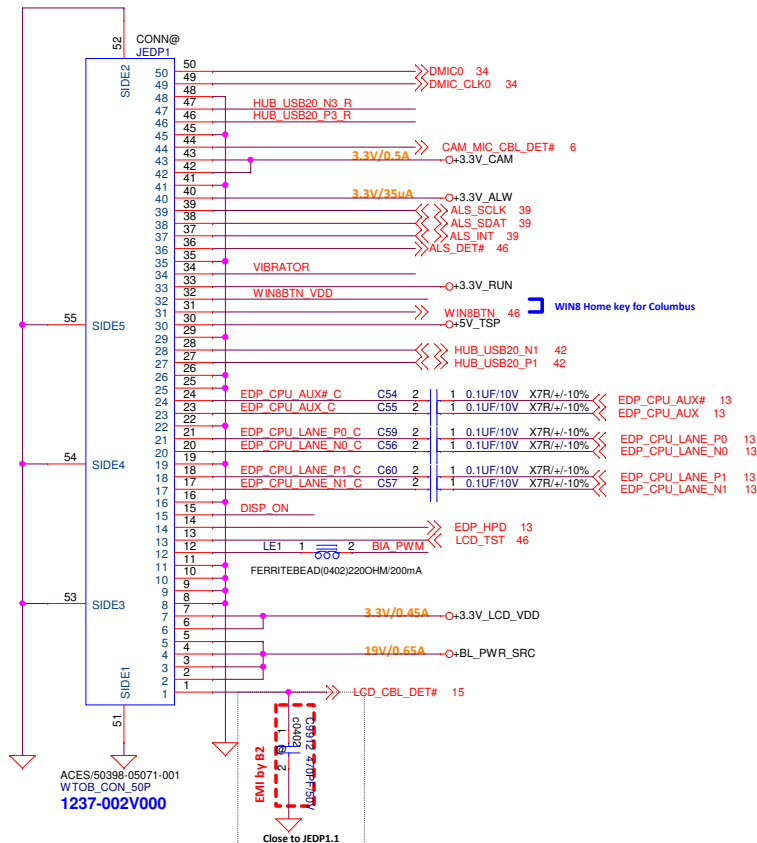
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TITLE		DDR4 JDIMM Decoupling		
DWG NO.		CORE_B2	REV. 2.0	
DATE		Friday, March 18, 2016	SHEET 23 of 81	



eDP Connector



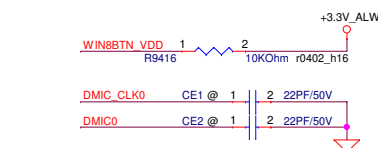
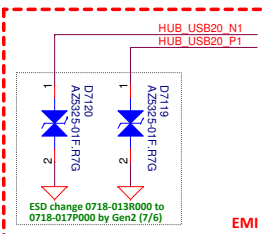
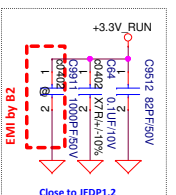
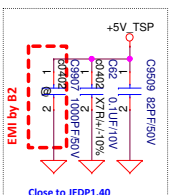
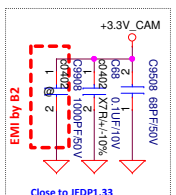
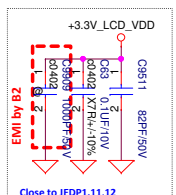
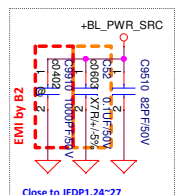
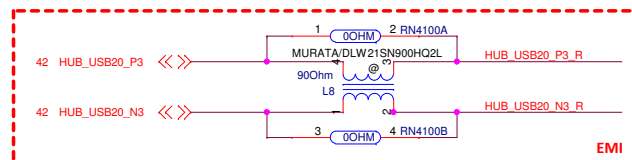
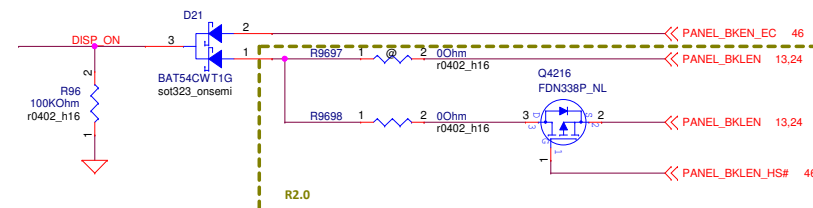
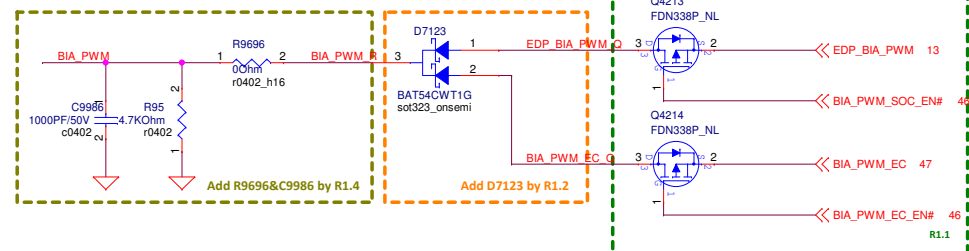
--> CAM+DMIC

--> ALS

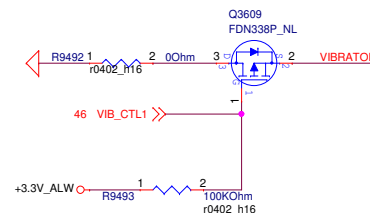
--> Vibrator

--> Touch Screen

--> eDP Panel



Vibrator Control



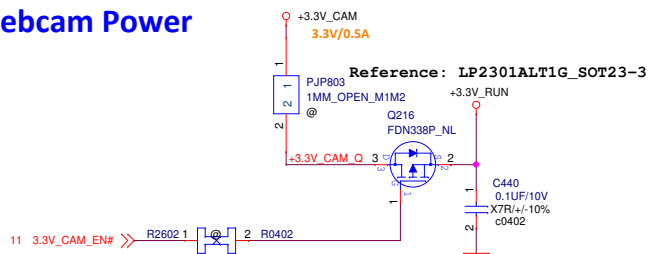
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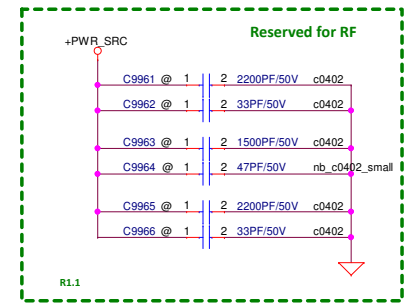
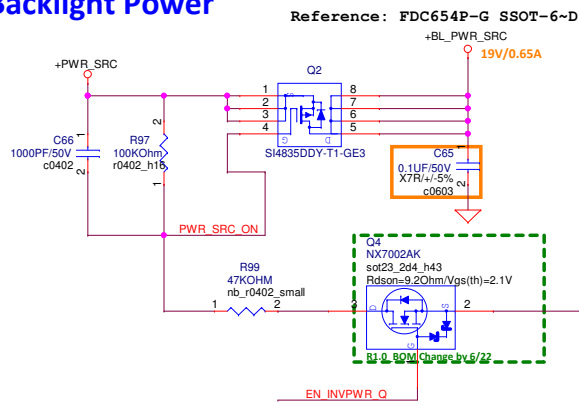
TITLE JEDP1	
DWG NO. CORE_B2	REV. 2.0
DATE Friday, March 18, 2016	SHEET 24 of 81



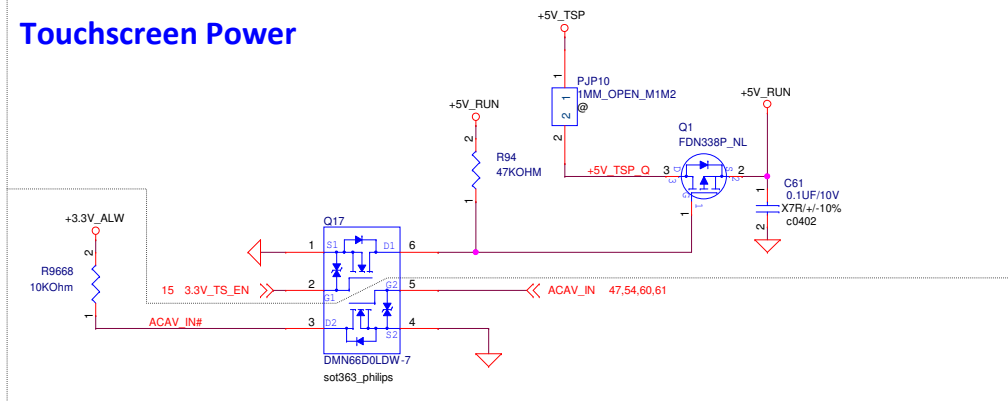
Webcam Power



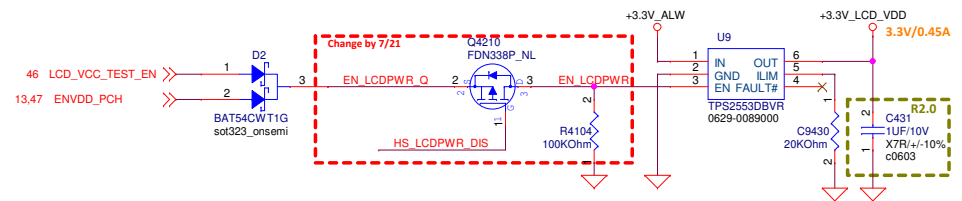
Backlight Power



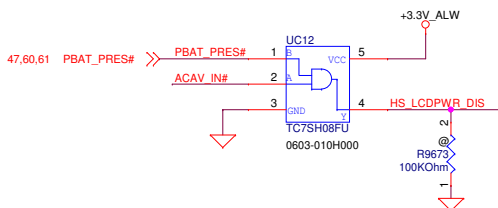
Touchscreen Power



LCDVDD Power

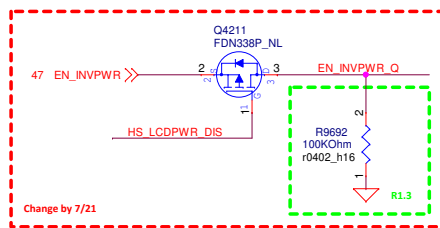


LCD Turn Off for Hotswap

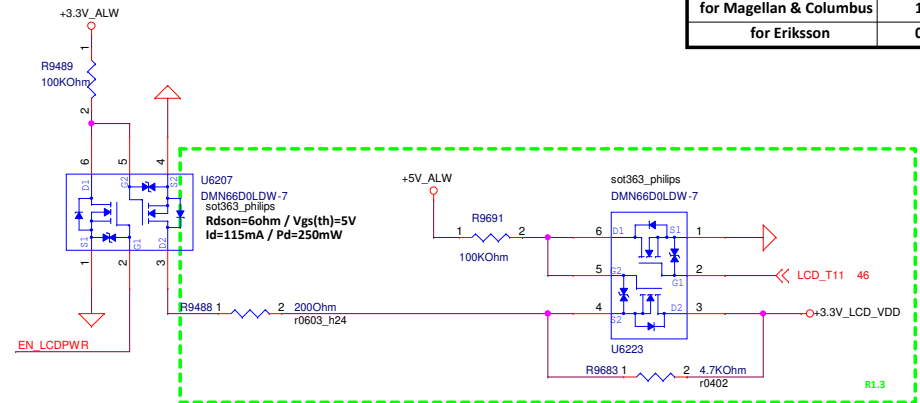


Battery (PBAT_PRES#)	AC IN (ACAV_IN#)	AND logic HS_LCDPWR_DIS	Panel Power
L	L	L	ON
L	H	L	ON
H	L	L	ON
H	H	H	OFF

Note: Battery(PBAT_PRES#),ACIN(ACAV_IN#)
H= un-plug, L= plug



LCDVDD Discharge



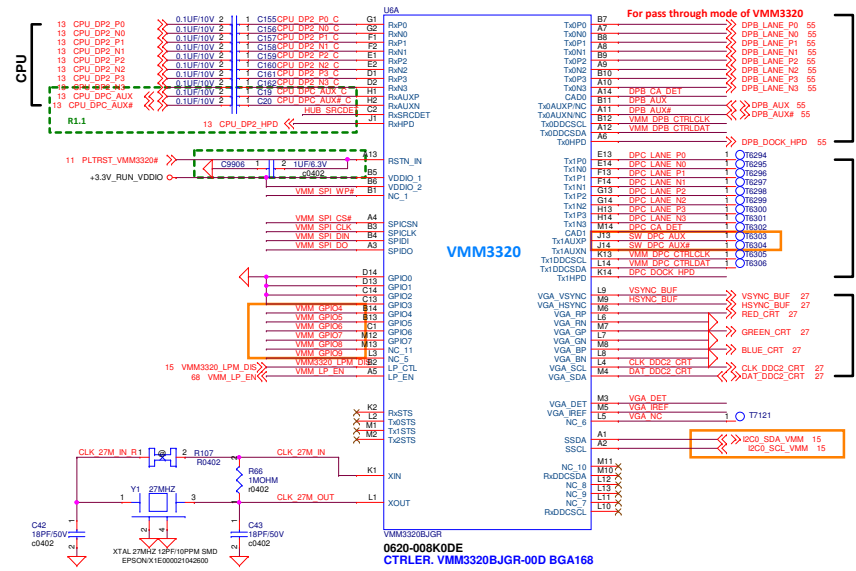
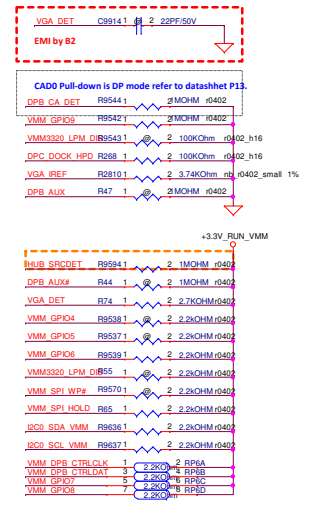
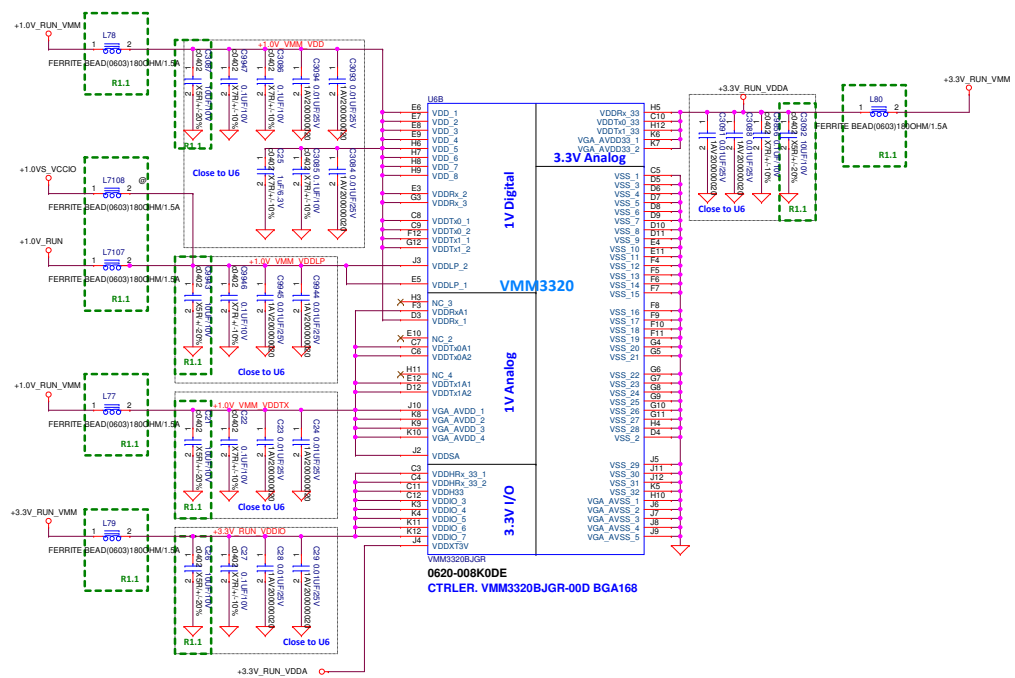
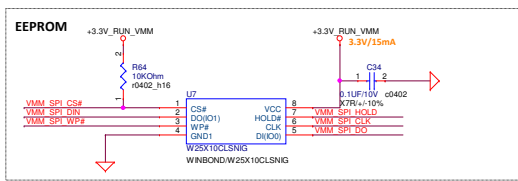
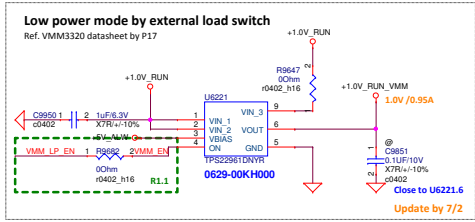
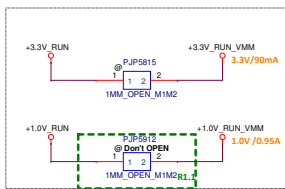
eDP power down timing at T11	
Function	LCD_T11
for Magellan & Columbus	1
for Eriksson	0

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TITLE JEDP1 Power	
DWG NO. CORE_B2	REV. 2.0
DATE Friday, March 18, 2016	SHEET 25 of 81



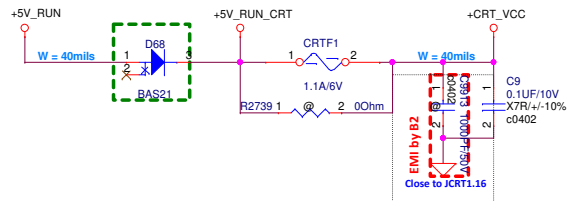


DOCK

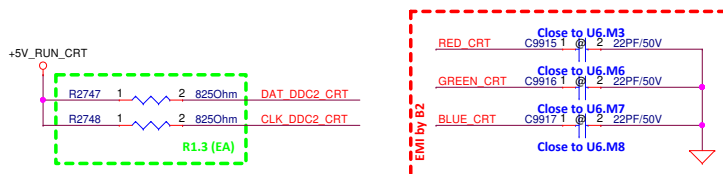
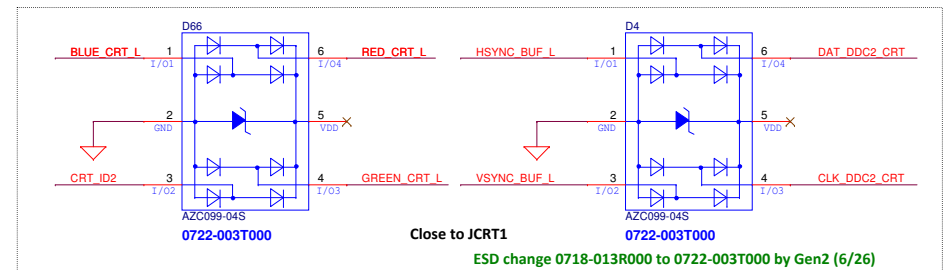
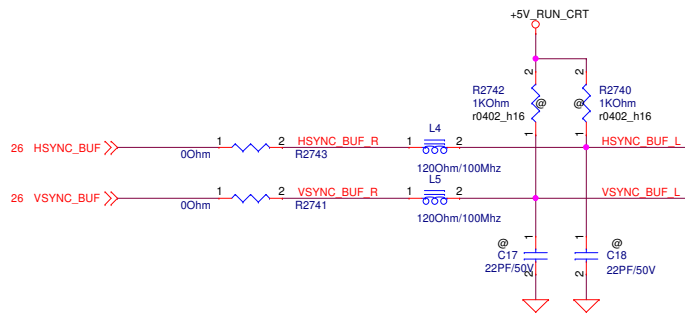
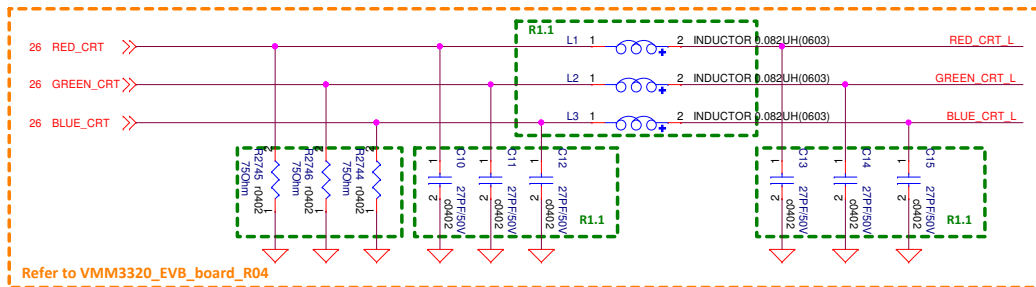
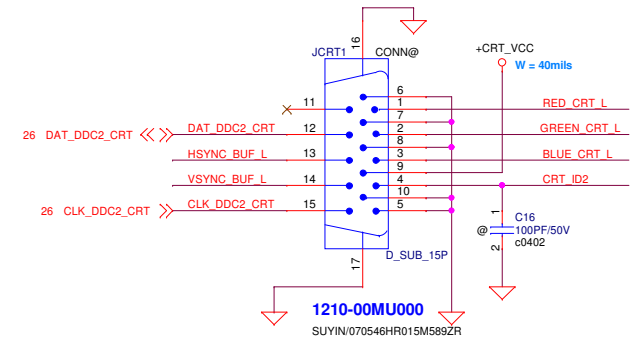
Reserved

VGA

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VGA Connector

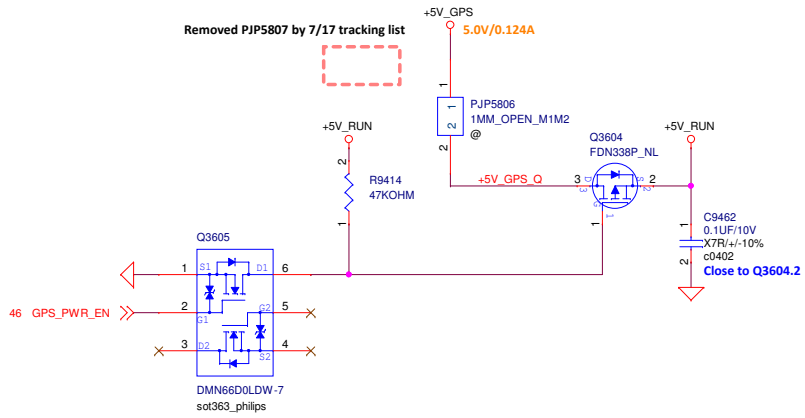


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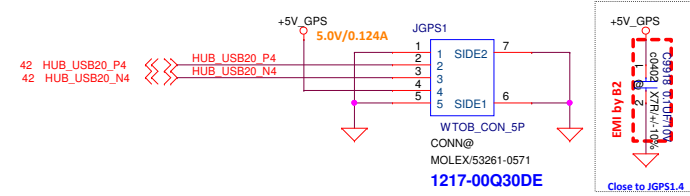
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TITLE JCRT1		
DWG NO. CORE_B2	REV. 2.0	
DATE Friday, March 18, 2016	SHEET 27 of 81	

GPS Power



GPS Connector



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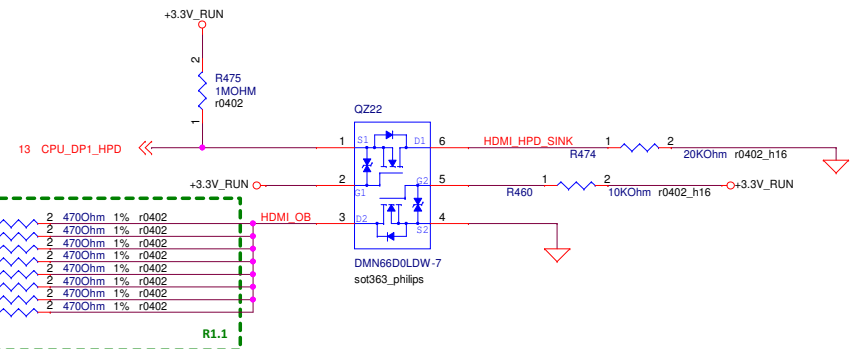
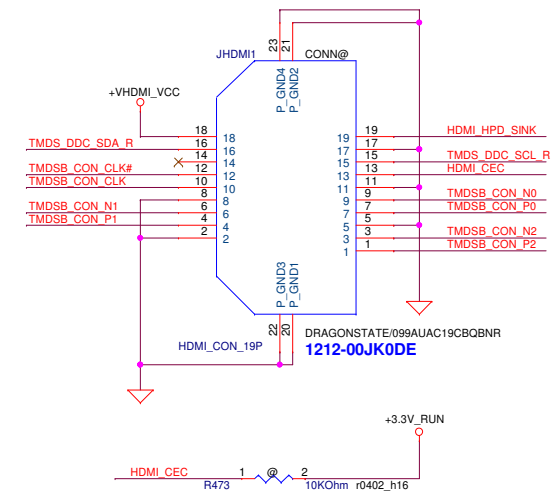
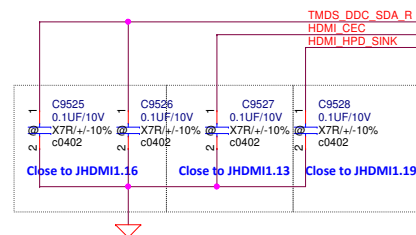
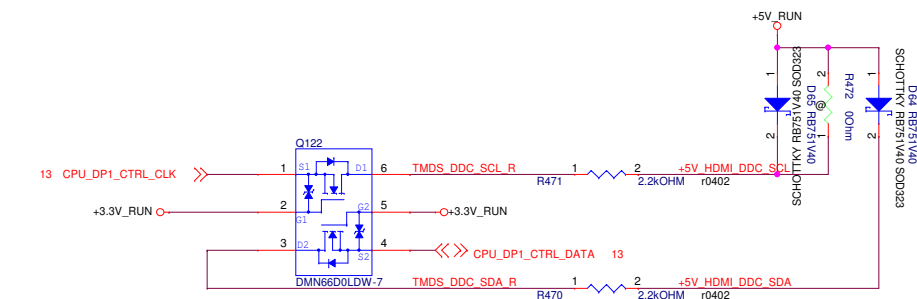
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TITLE	JGPS1
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DWG NO. CORE B2

REV. 2.0



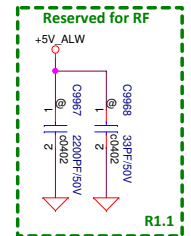
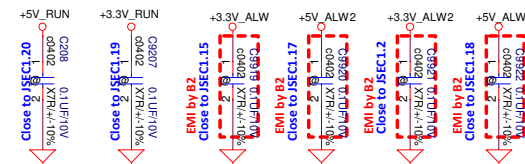
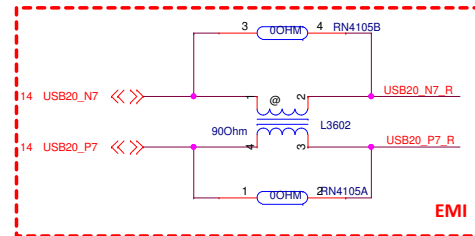
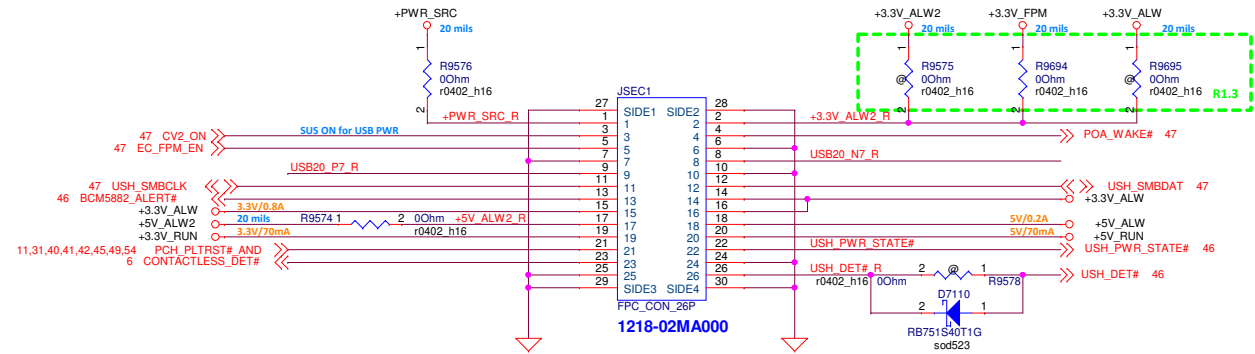
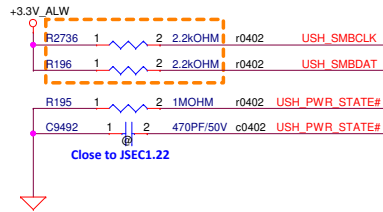


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TITLE JHDMI1	
DWG NO. CORE_B2	REV. 2.0
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Security Connector



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TITLE		JSEC1	
DWG NO.	CORE_B2	REV.	2.0
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SATA Express Re-Driver

PS8558B Note:

Equalizer control and program for channel A
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K
[A_EQ0,A_EQ1,A_EQ2] ==

L/L/L : for channel loss up to 17.3dB (default)
L/H/L : for channel loss up to 14.1dB
H/L/L : for channel loss up to 18.7dB
H/H/L : for channel loss up to 20.5dB
L/L/H : for channel loss up to 18dB
L/H/H : for channel loss up to 10dB
H/L/H : for channel loss up to 15.9dB
H/H/H : for channel loss up to 19.6dB

Equalizer control and program for channel B
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K
[B_EQ0,B_EQ1,B_EQ2] ==

L/L/L : for channel loss up to 17.3dB (default)
L/H/L : for channel loss up to 14.1dB
H/L/L : for channel loss up to 18.7dB
H/H/L : for channel loss up to 20.5dB
L/L/H : for channel loss up to 18dB
L/H/H : for channel loss up to 10dB
H/L/H : for channel loss up to 15.9dB
H/H/H : for channel loss up to 19.6dB

Programmable output de-emphasis level setting for channel A.
A_DE0: internally pulled up at ~150K
A_DE1 internally pulled down at ~150K
[A_DE1,A_DE0] ==

L/L -2 dB
H/L -7.5dB
L/H -3.5dB (default)
H/H -6 dB

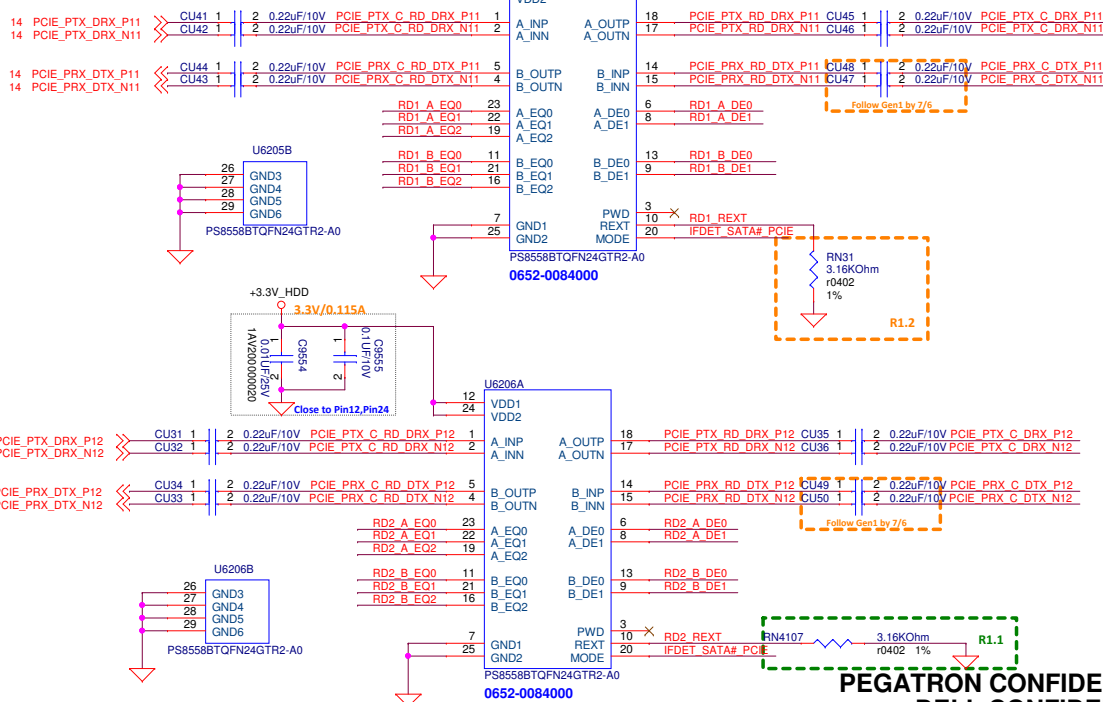
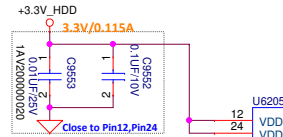
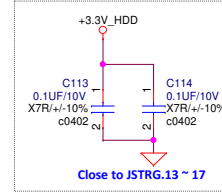
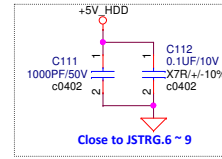
Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K
B_DE1 internally pulled down at ~150K
[B_DE1,B_DE0] ==

L/L -2 dB
H/L -7.5dB
L/H -3.5dB (default)
H/H -6 dB

IFDET_SATA#_PCIE	Device Interface
0 (default)	SATA
1	PCIE

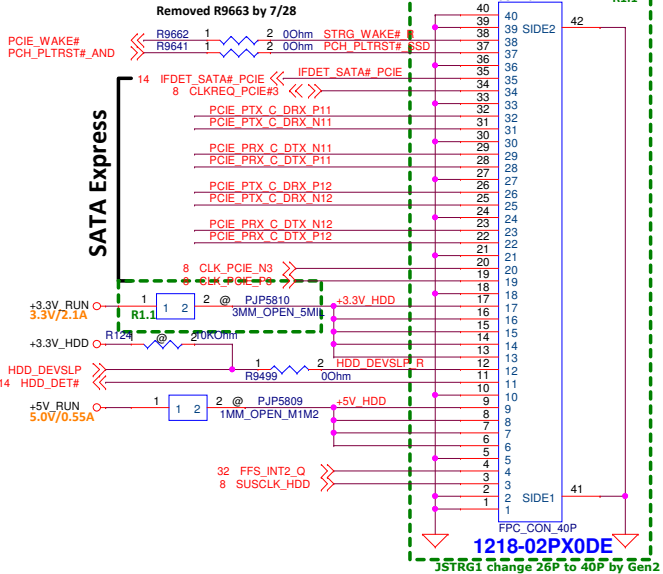


Removed U34, R9565, R9566, C462, C9951, C3078
on +3.3V_HDD power control by 7/24 tracking list



CU31~CU36, CU49, CU50 change to 0.01uF from 0.22uF for SATA device by 7/31
CU31~CU36, CU49, CU50 change to 0.22uF from 0.01uF for SATA device by 8/7

Storage Connector



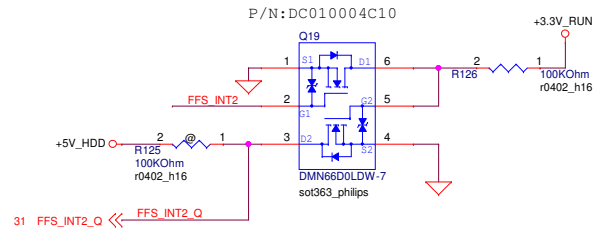
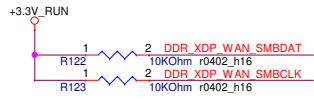
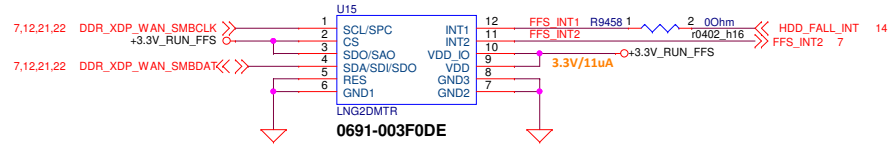
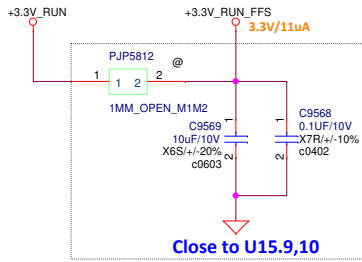
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TITLE	JSTRG1/PCIE_SATA Re-Driver
DWG NO.	CORE_B2
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Free Fall Sensor



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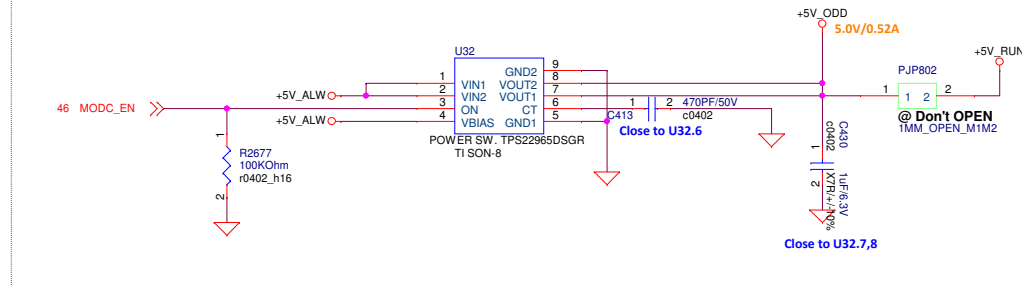
TITLE	Free Fall Sensor (LNG2DMTR)
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DWG NO.	CORE_B2	REV.	2.0
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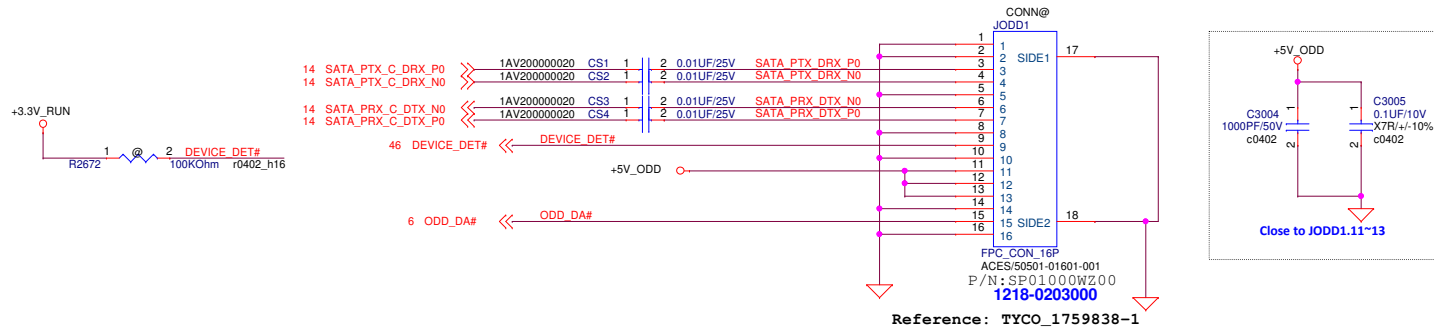
DATE	Friday, March 18, 2016	SHEET	32	of 81
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ODD power



ODD Connector



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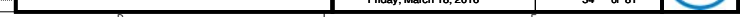
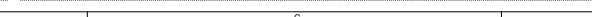
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TITLE	JODD1
DWG NO.	CORE_B2
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DATE	Friday, March 18, 2016
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LRCK: Audio serial data bus word clock input/output

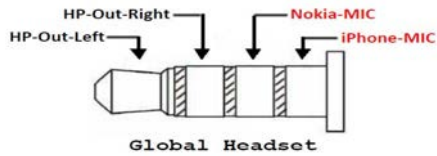


F F TO	TITLE Audio Codec (ALC3235-CG)		
	DWG NO. CORE_B2	REV. 2.0	
	DATE Friday, March 18, 2016	SHEET 24 of 81	

TITLE A. I. C. I. (ALC9995 00)	
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Friday, March 16, 2018	34	61	
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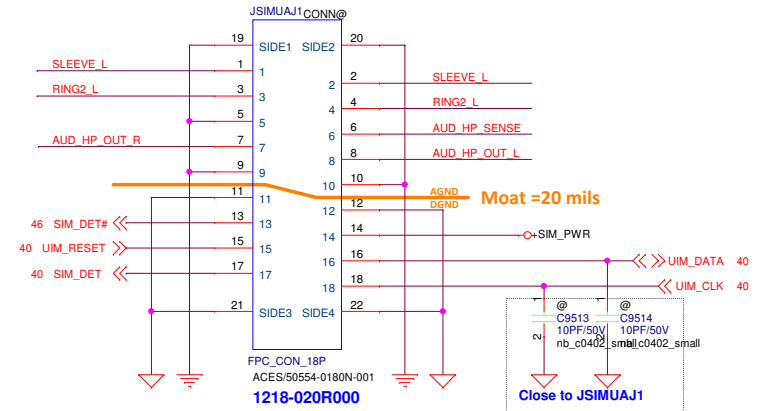
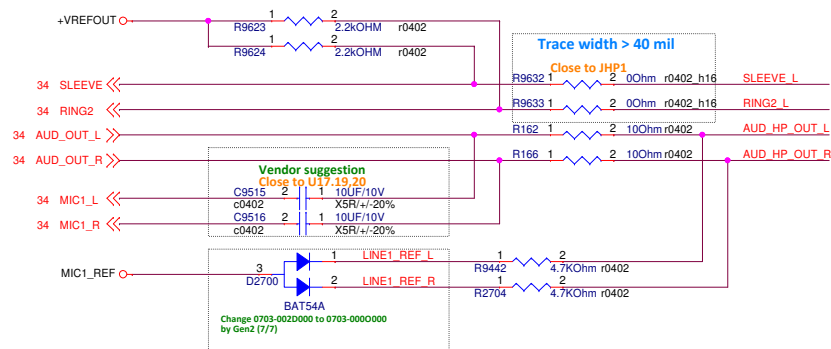
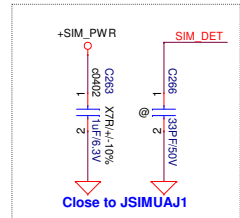




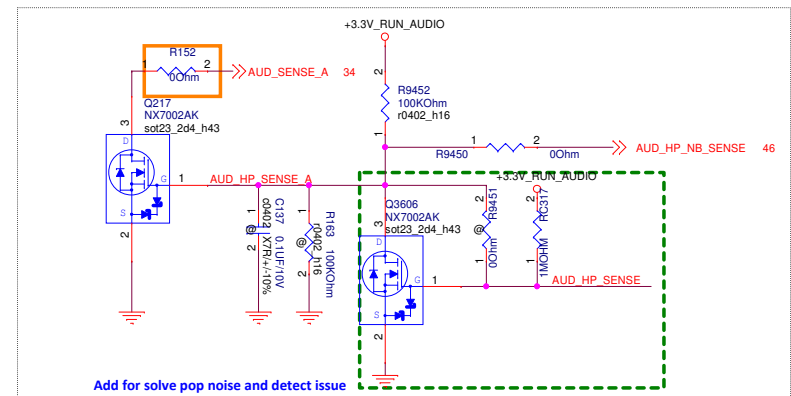
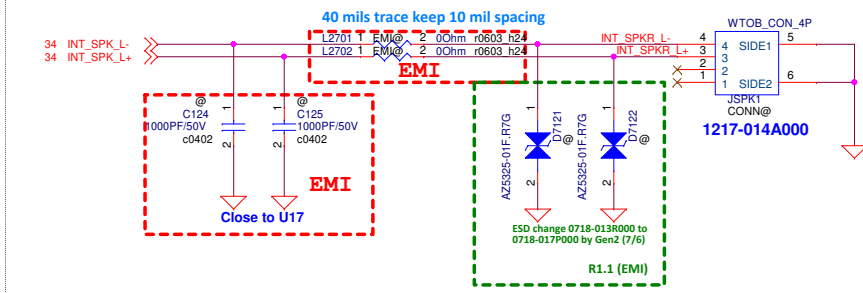
Dior Jack Requirements (Gen2):

1. Universal Audio jack (HP & mono mic).
2. Supports auto detect of both OMTP and CTIA headsets.
3. 3.5 mm jack with detect pin on tip.
4. Re-taskable to standard Microphone or Stereo Line Input.
5. Inline control support = Yes.
6. HP Amp power > 20 mW into 32ohm 1% THD+N.

uSIM + UAJ Connector



Internal Speaker Header (Mono)

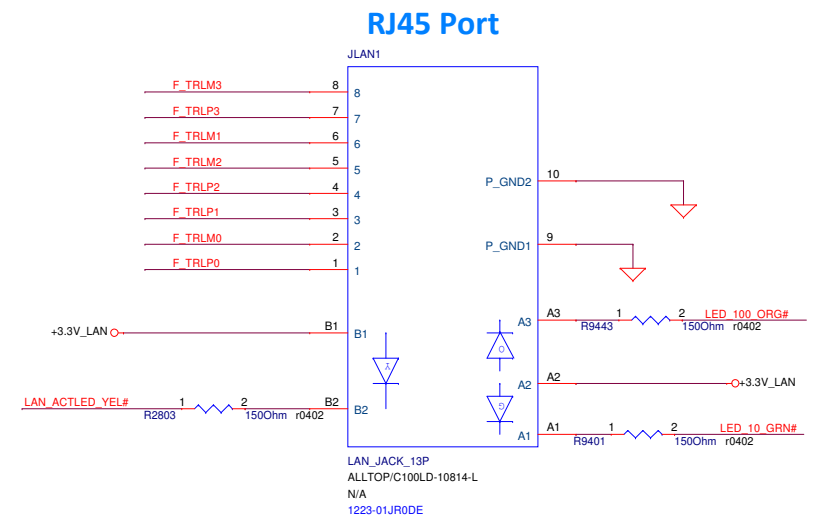
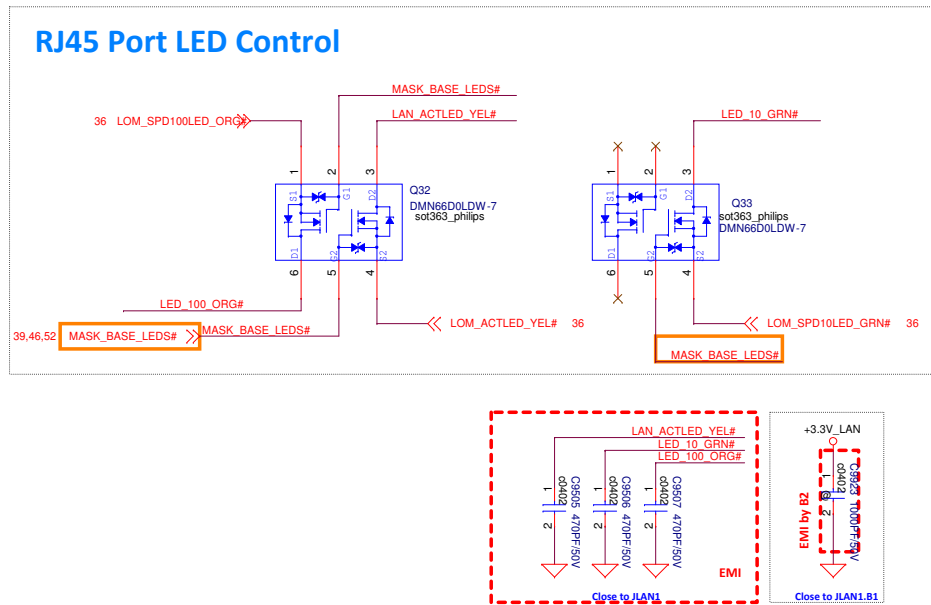
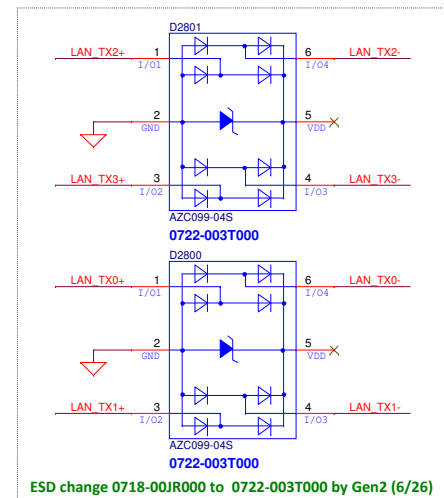
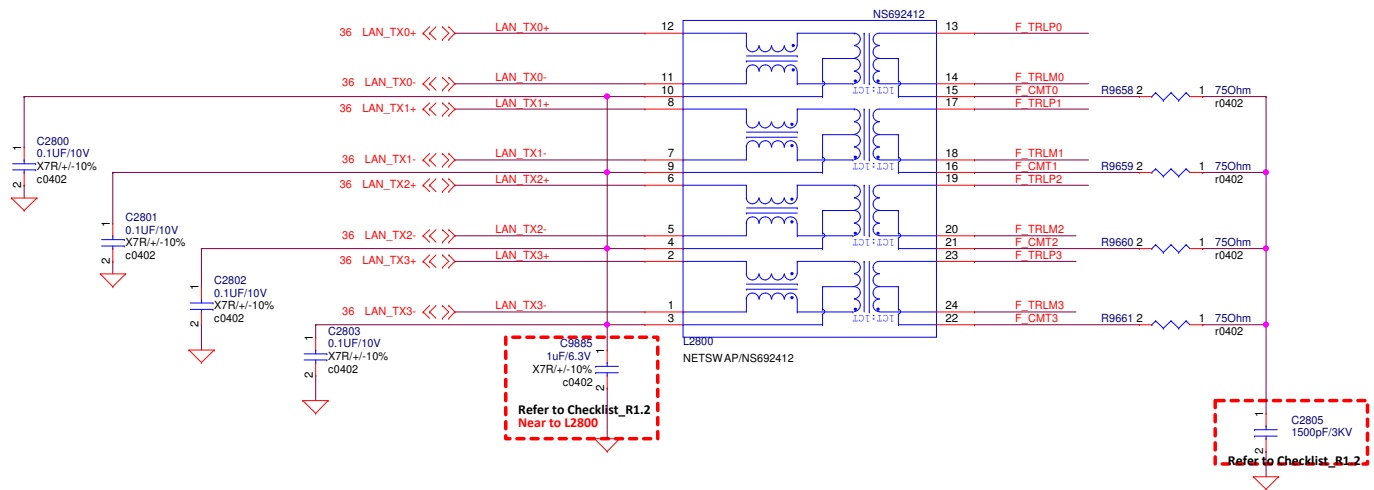


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DWG NO.	CORE_B2
REV.	2.0
DATE	Friday, March 18, 2016
SHEET	35 of 81

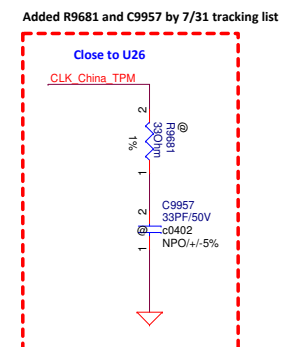
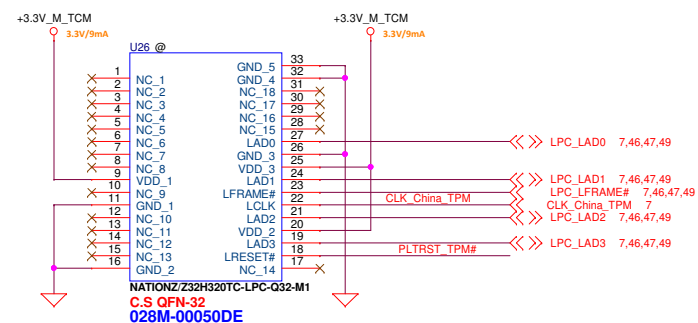
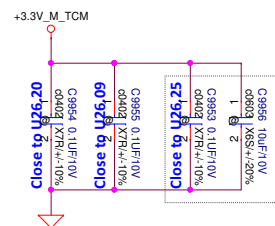
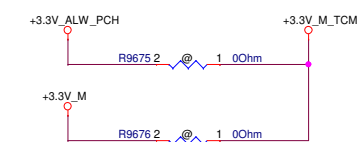
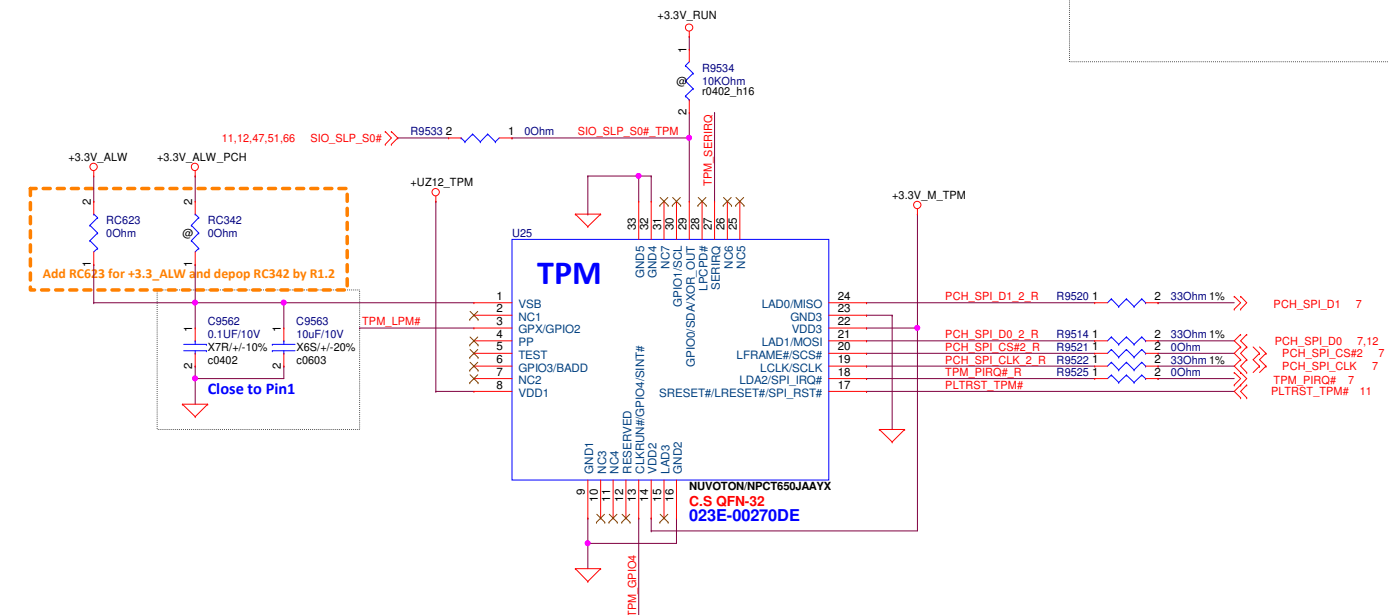
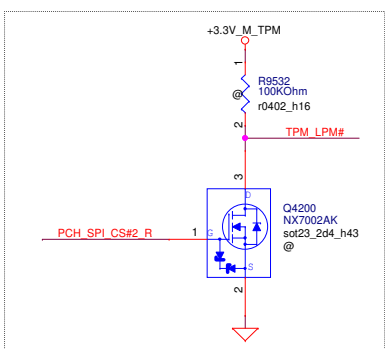
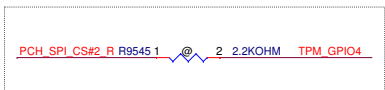
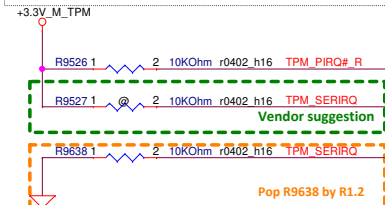
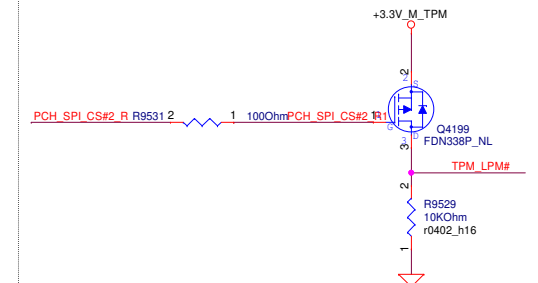
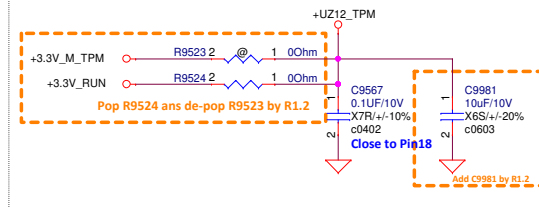
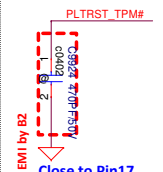
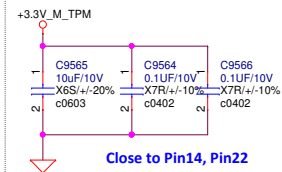
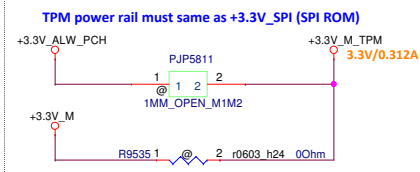




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China TPM

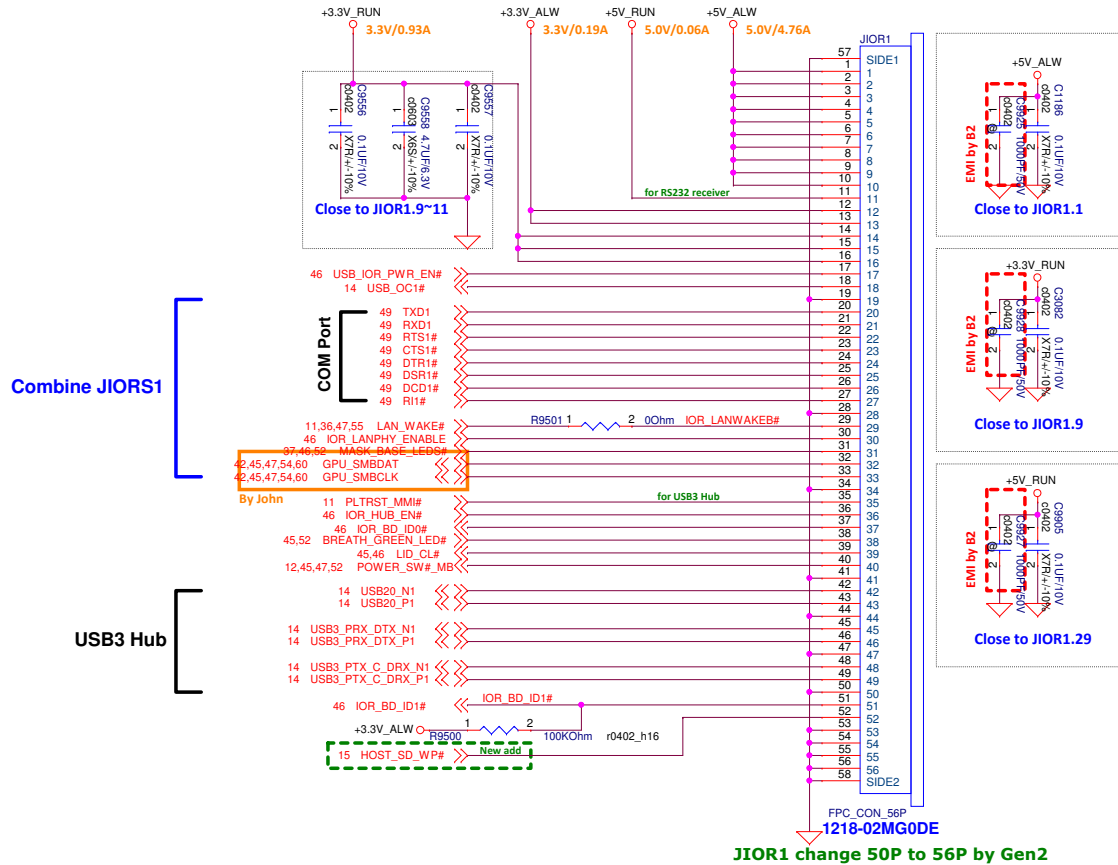
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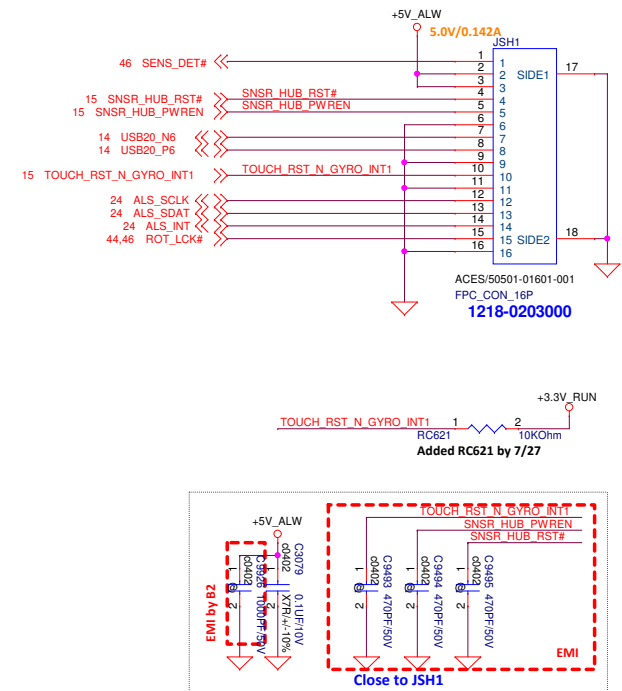
TITLE		TPM IC (NPCT650JAAYX)		
DWG NO.		CORE_B2	REV. 2.0	
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IOR Connector



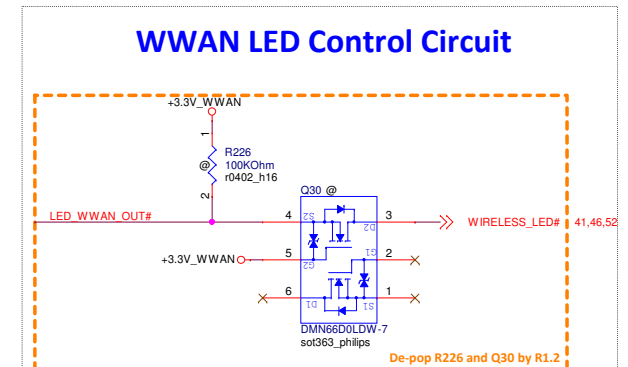
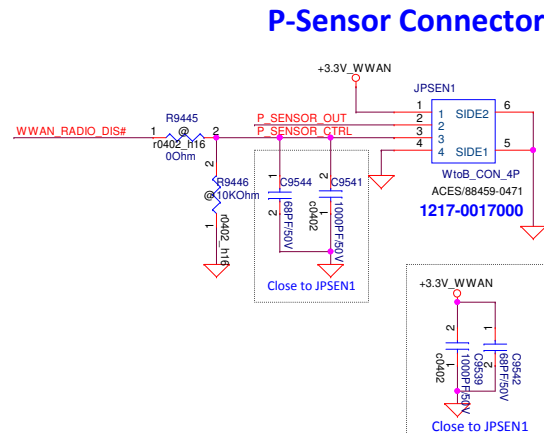
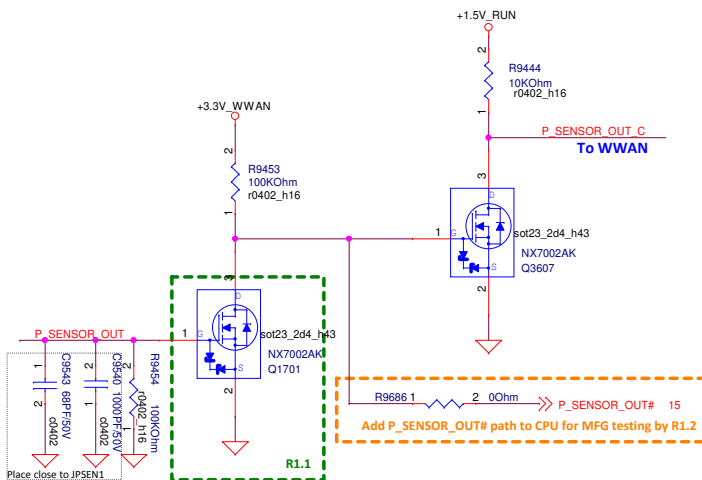
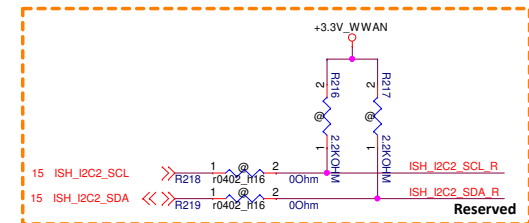
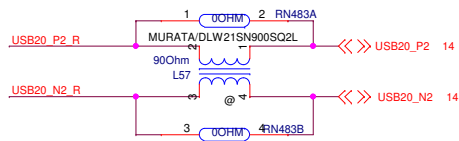
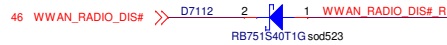
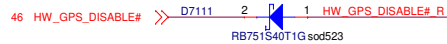
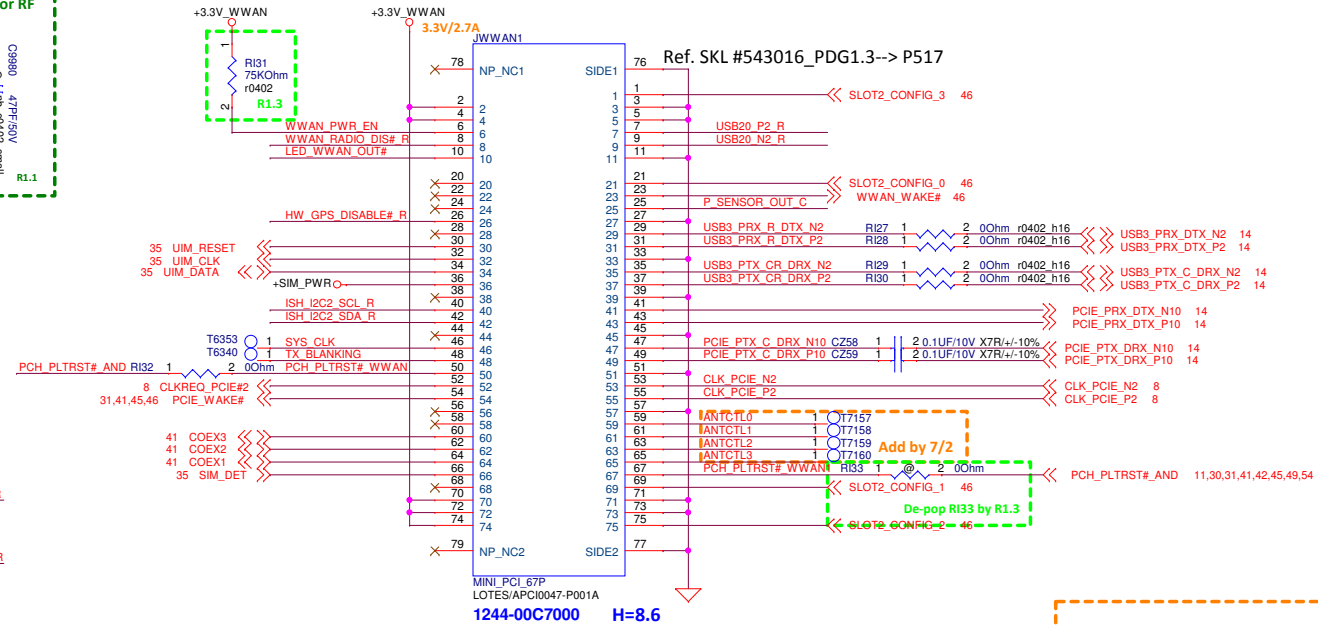
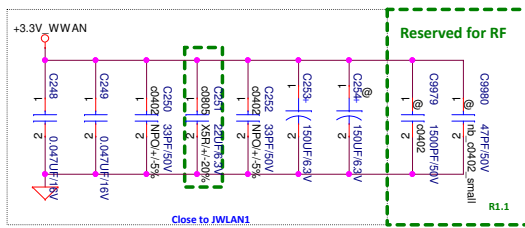
Sensor Hub Connector



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DWG NO. CORE_B2		REV. 2.0	
DATE Friday, March 18, 2016		SHEET 39 of 81	
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NGFF KEY-B WWAN/LTE Connector



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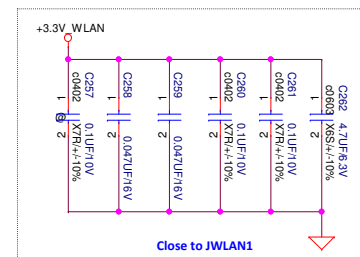
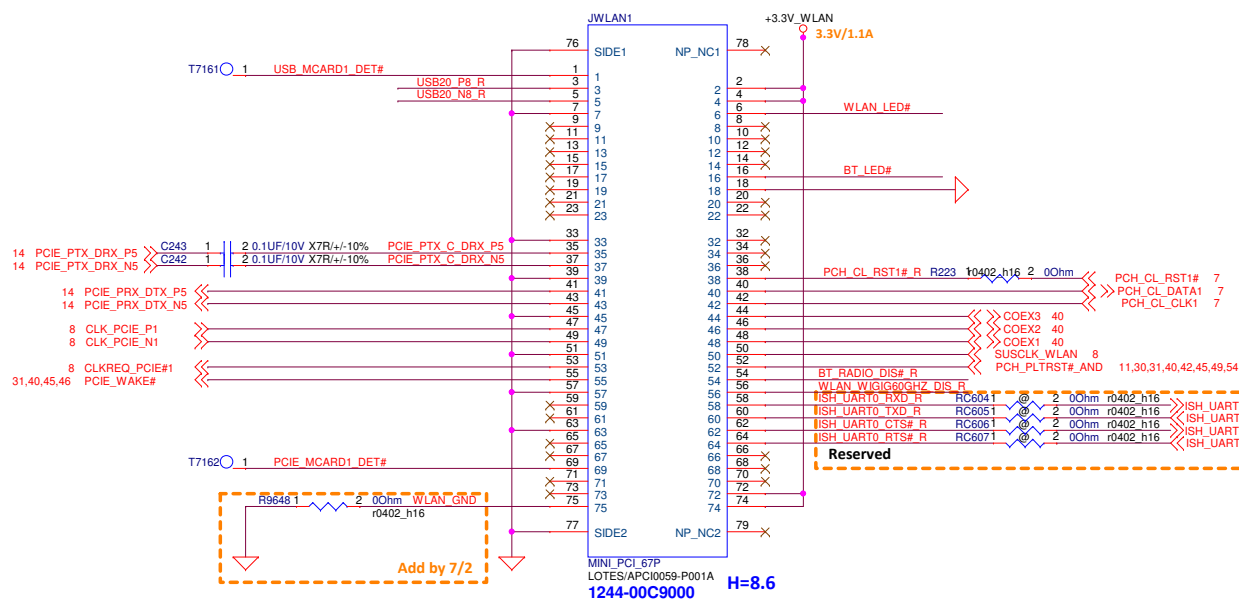
TITLE	JWWAN1/JPSEN1
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DWG NO.	CORE B2
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REV.	2.0
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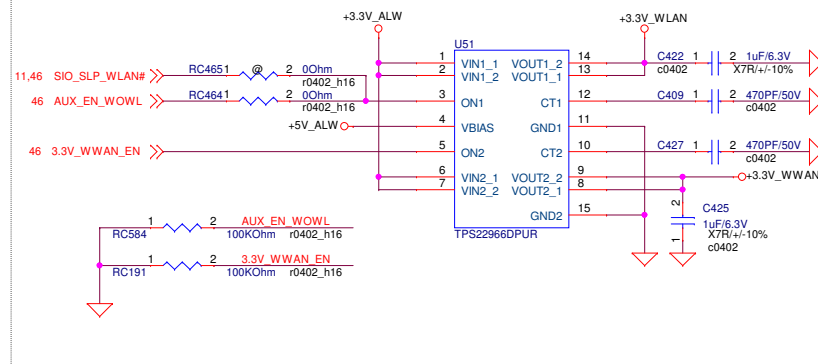


NGFF KEY-E WLAN/BT Connector

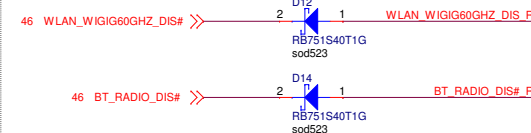
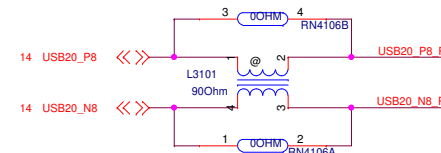
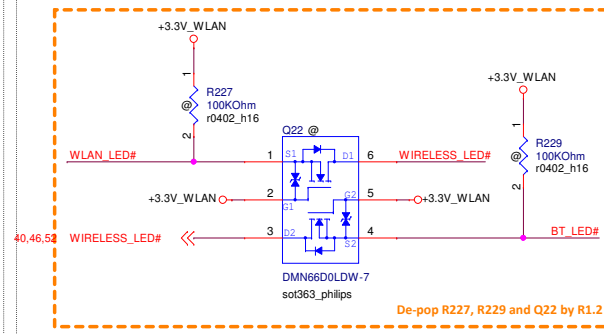


Reference: ACES 51700-0520W-001

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+−9%	1000	750	
+3.3Vaux	+−9%	330	250	250 (Wake enable) 5 (Not wake enable)



WLAN LED Control Circuit

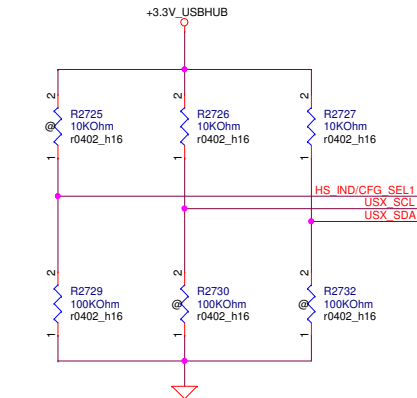
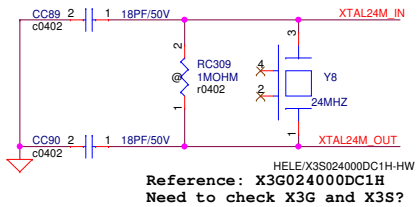
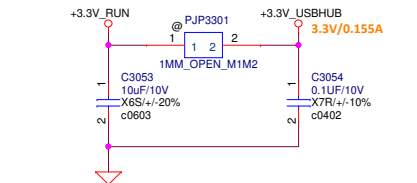


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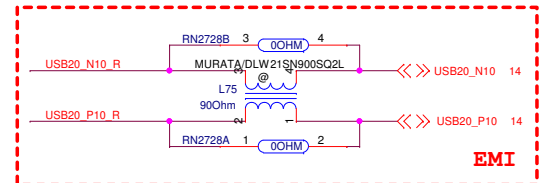
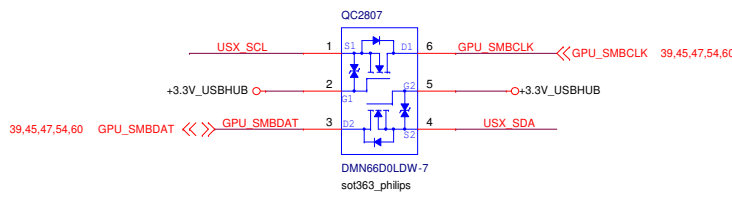
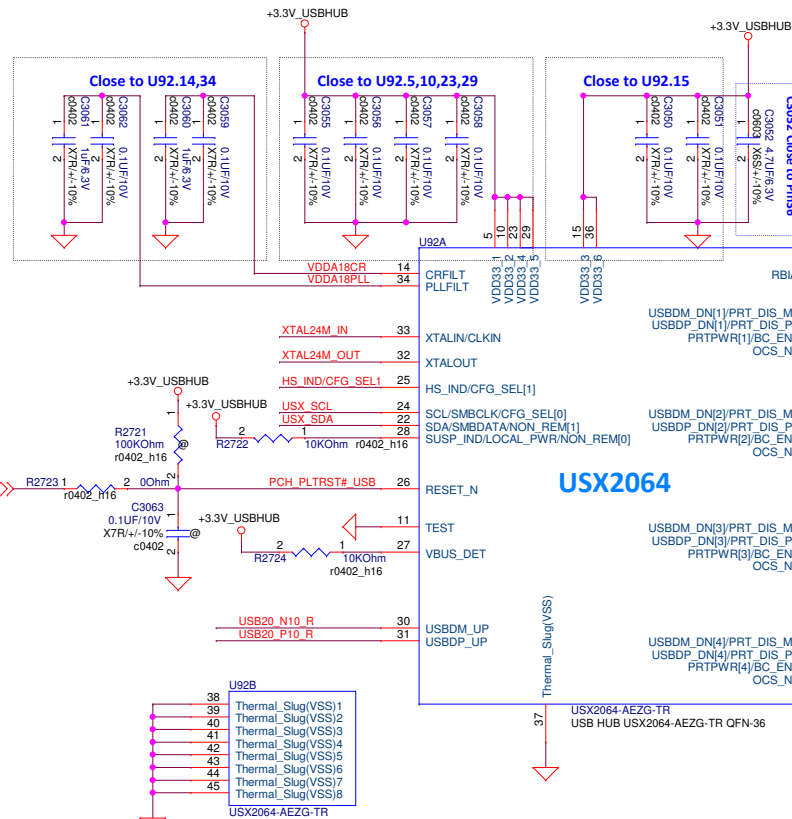
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TITLE JWLAN1		
DWG NO. CORE_B2	REV. 2.0	
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USX2064 CFG Selection Table		
CFG_SEL[0] \ CFG_SEL[1]	0	1
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM



1. Place R2720 close to Pin35 and trace width
USX2064_RBIAS is 20 mils
2. Kindly have R2720 a single via to GND plane.
Don't share the GND via with caps

Touch Screen

EC/PC

FCam

GPS

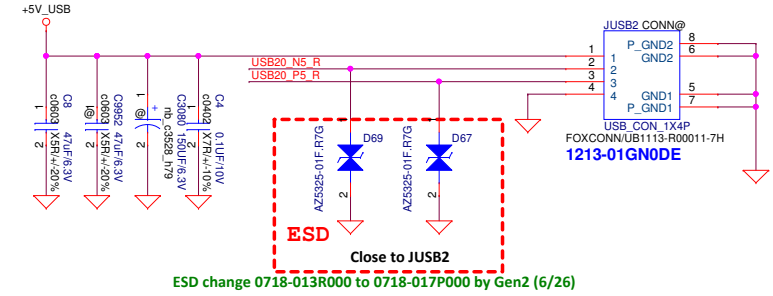
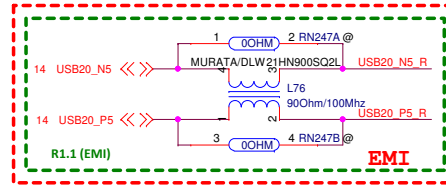
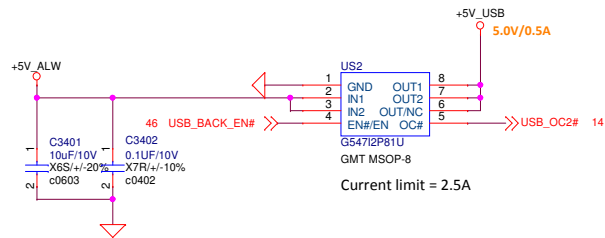
SMSC recommend:
Add 10K pull-up (to +3.3V_USB_HUB) at the un-used port to disable downstream port if internal default is used. These 2 10K reserved resistors should be de-pop by default, since they select to use "Configured via SMBUS" by default.

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TITLE USB2.0 Hub (USX2064)		
DWG NO.	CORE_B2	REV. 2.0
DATE	Friday, March 18, 2016	SHEET 42 of 81

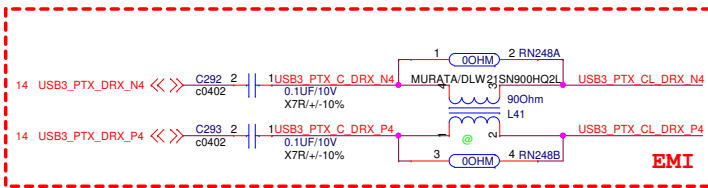
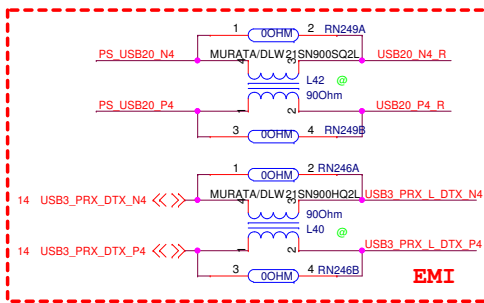
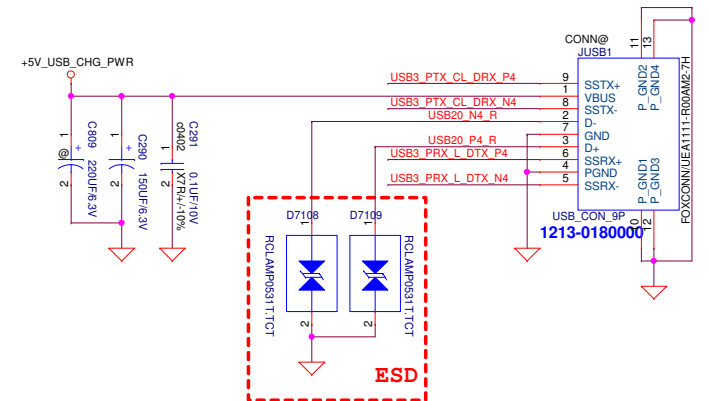
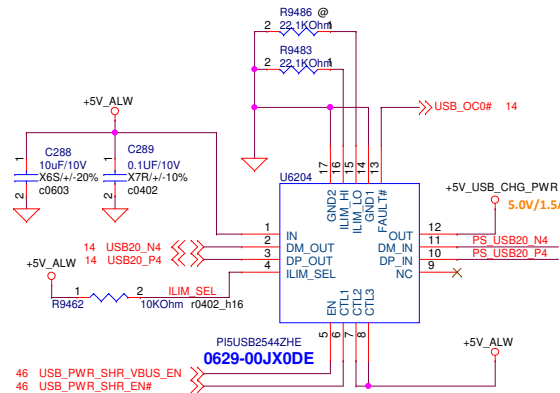
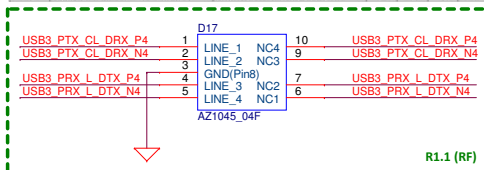




USB Charger

Ext USB Port (LEFT)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
ILIM_SEL Current Limit						
I_{OL}	OUT Current-Limit ^a	$V_{BUS_US} = 0V, R_{DS(on)} = 210k\Omega$	205	240	275	mA
		$V_{BUS_US} = 0V, R_{DS(on)} = 99.4k\Omega$	275	325	380	mA
		$V_{BUS_US} = 0V, R_{DS(on)} = 21.4k\Omega$	3150	3750	4400	mA
t_{res}	Response time to OUT short circuit ^b	$V_{BUS_US} = V_{IN}, R_{DS(on)} = 210k\Omega$	2340	2510	2685	ms
		$V_{BUS_US} = V_{IN}, R_{DS(on)} = 99.4k\Omega$	2770	2970	3170	ms
		$V_{BUS} = 5.0V, R = 0.1\Omega, \text{lead length} = 2"$	-	1.5	-	ms

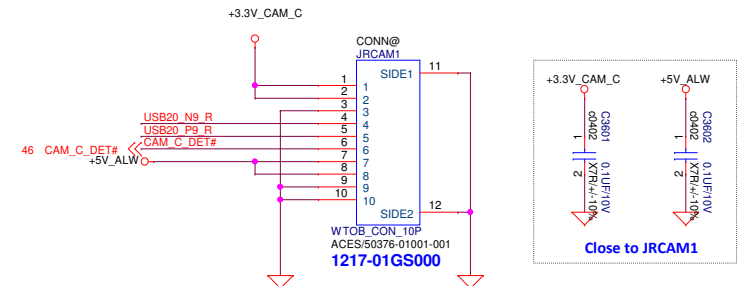


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DWG NO. CORE_B2				REV. 2.0		
DATE Friday, March 18, 2016				SHEET 43 of 81		

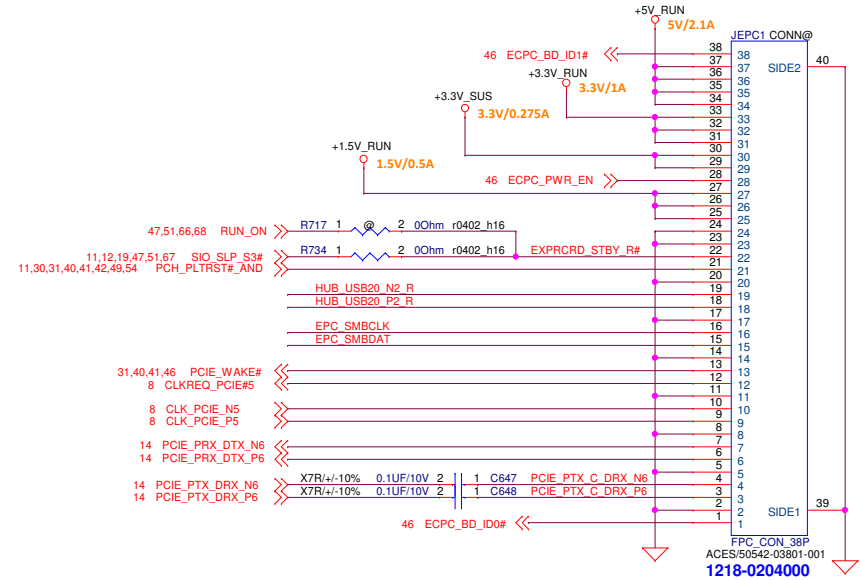
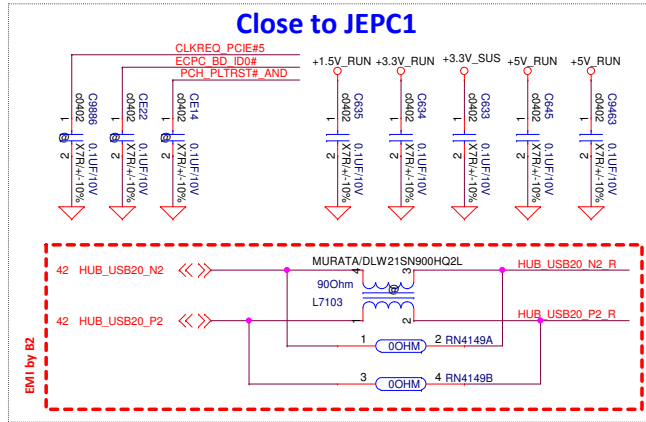
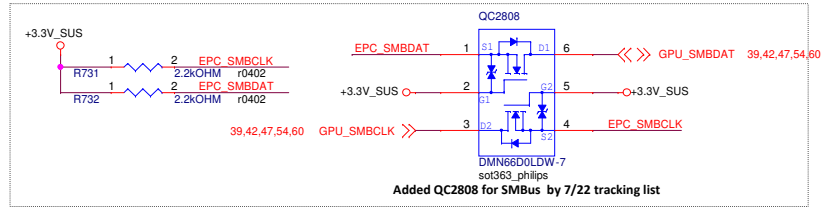
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1218-01YR000
Connect to C_Button_C FPC
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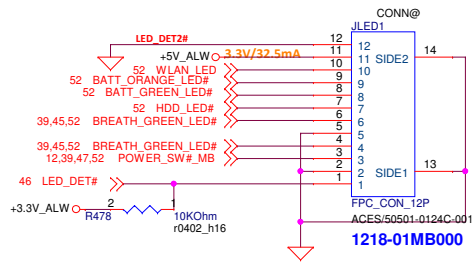


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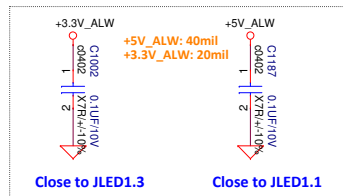
Express Card/PCMCIA Connector



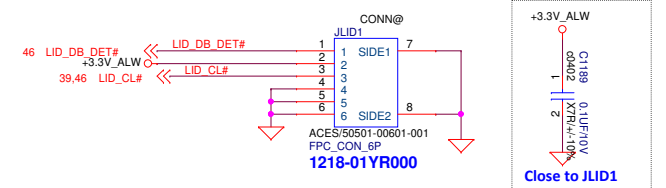
LED Connector



Connect to C_LED FPC



LID Connector

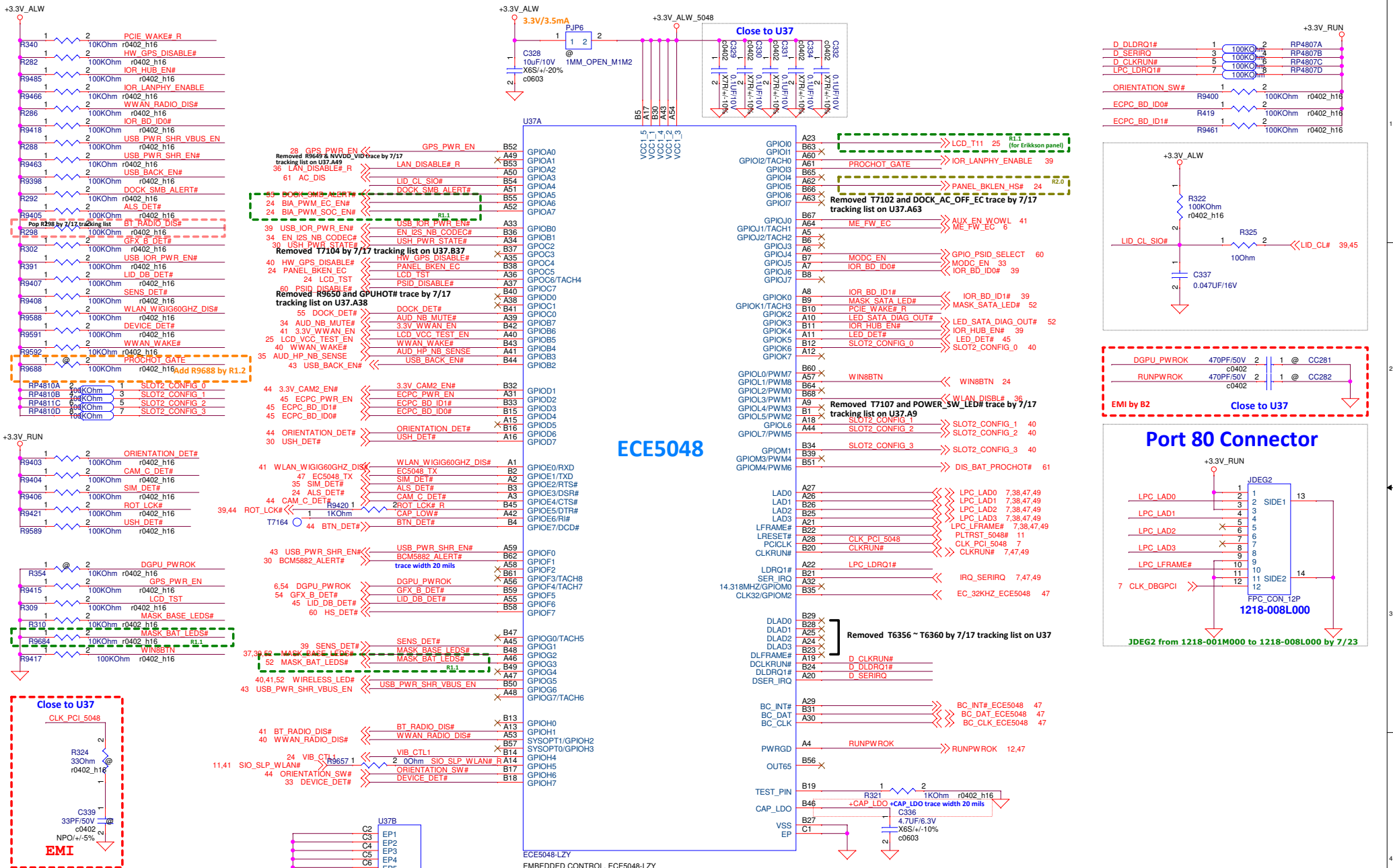


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TITLE	JEPC1/JLED1/JLID1	
DWG NO.	CORE_B2	REV. 2.0
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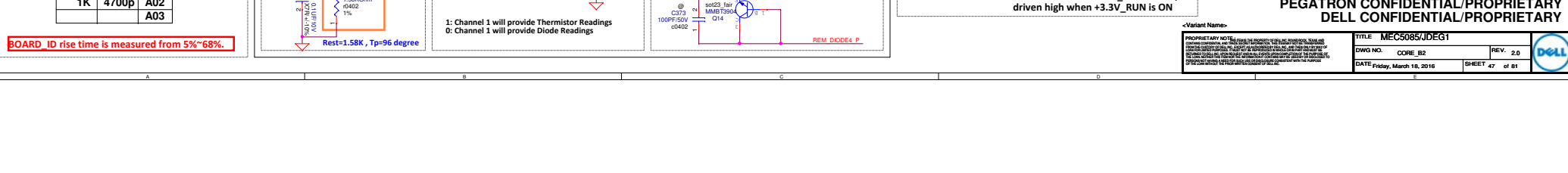
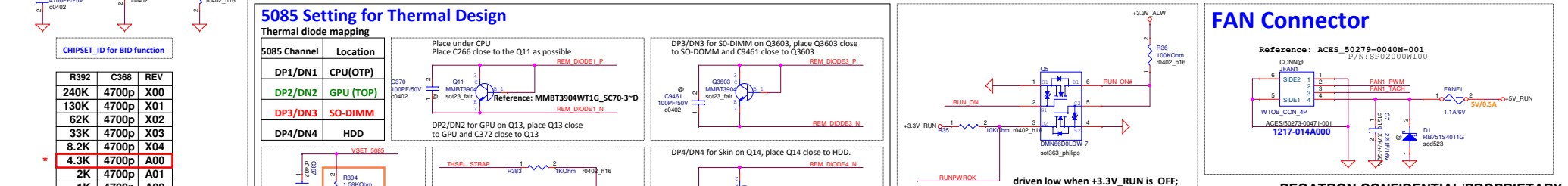
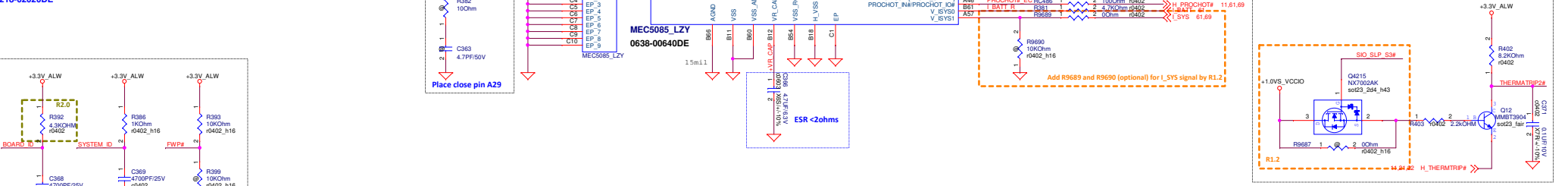
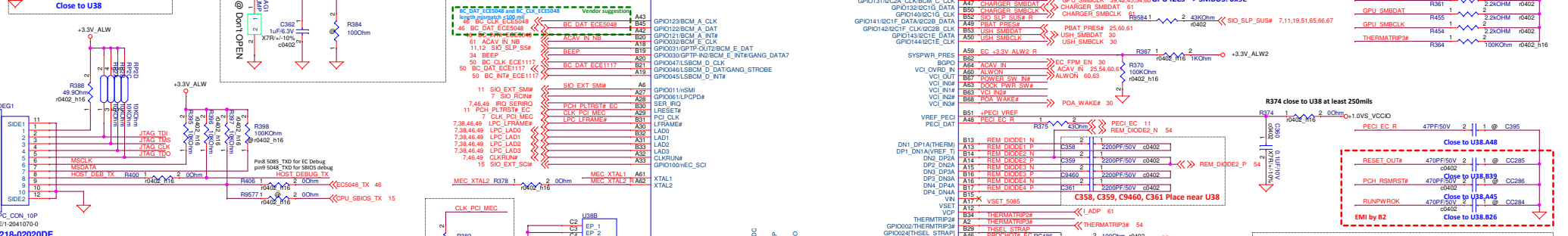
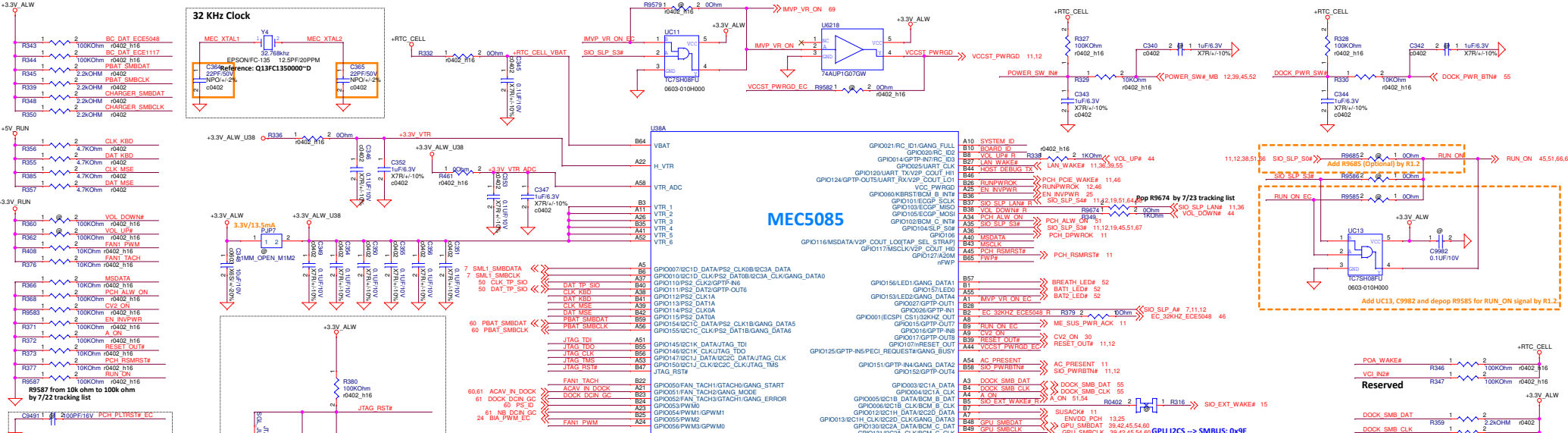
IOR_BD_ID#	IOR_BD_ID0#	Function
0	0	Magellan
0	1	Eriksson
1	0	Columbus
1	1	Board Missing (PAID failure)

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TITLE	ECE5048/JDEG2
DWG NO.	CORE_B2
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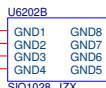
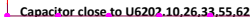


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DATE Friday, March 18, 2016		SHEET 48 of 81	





<0506: Vendor suggestion>If UART2 set as input, need to mount external PH/PL (can't be floating). If set as output, de-pop.

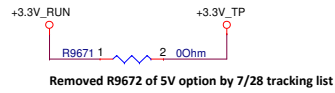
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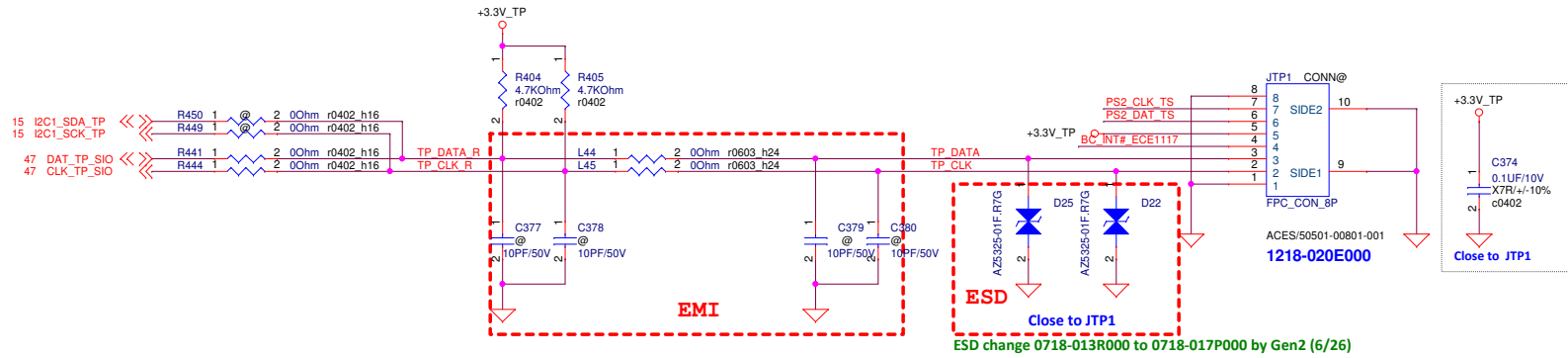
TITLE		LPC2UART IC (SIO1028)/JSER1	
DWG NO.		CORE_B2	REV.
DATE		SHEET	
Friday, March 18, 2016		49	of 50



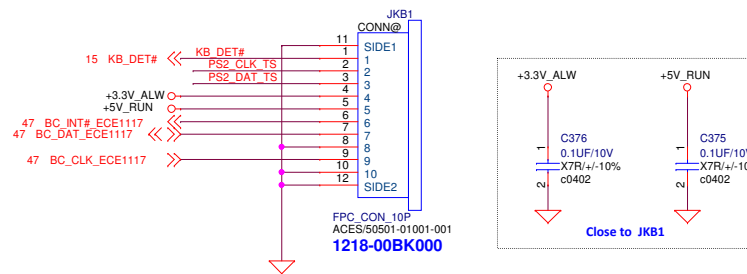
Touch Pad Power



Touch Pad Connector



KB Module Connector



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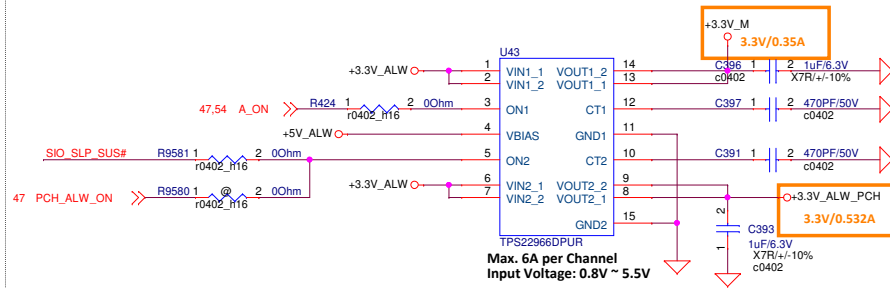
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TITLE JTP1/JKB1	
DWG NO. CORE_B2	REV. 2.0
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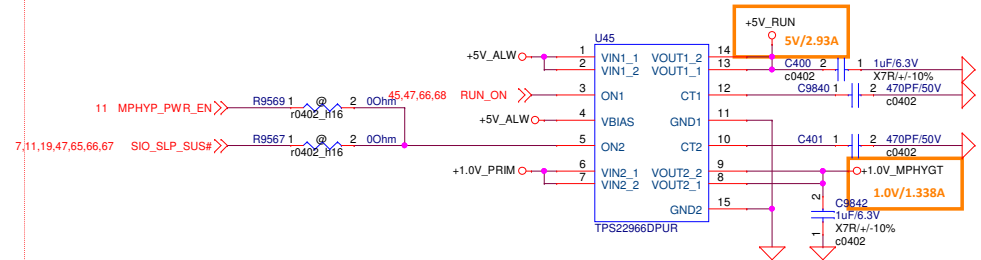


DC/DC Interface

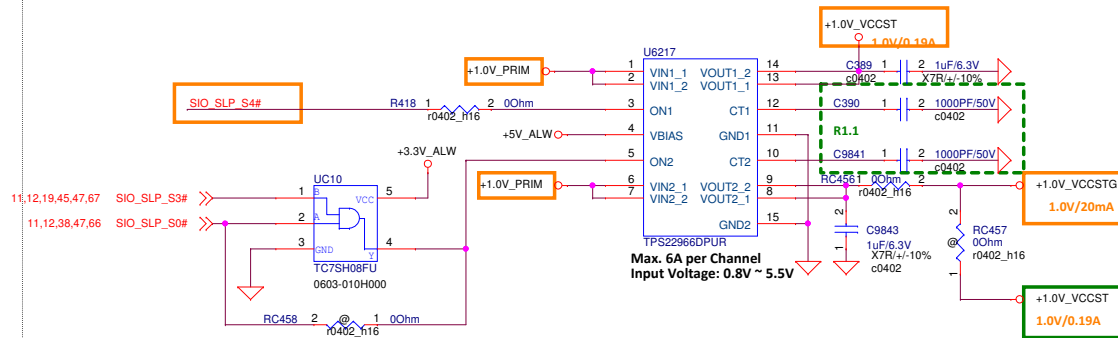
+3.3V_M / +3.3V_ALW_PCH Source



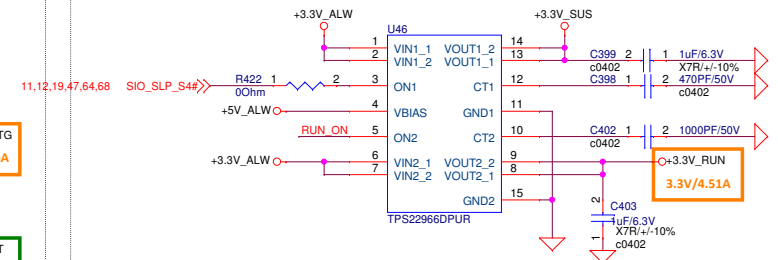
+5V_RUN / +1.0V_MPHYGT Source



+1.0V_VCCST / +1.0V_VCCSTG Source



+3.3V_RUN/+3.3V_SUS Source



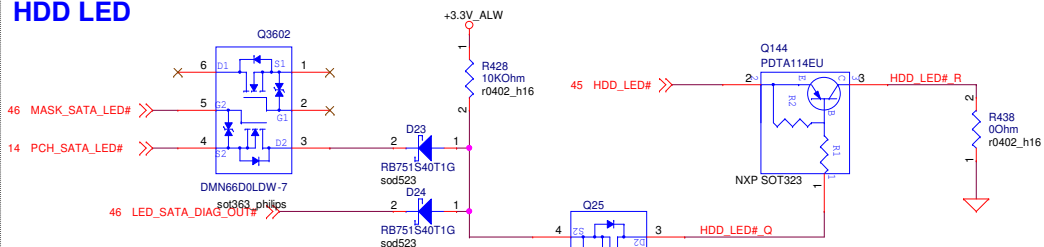
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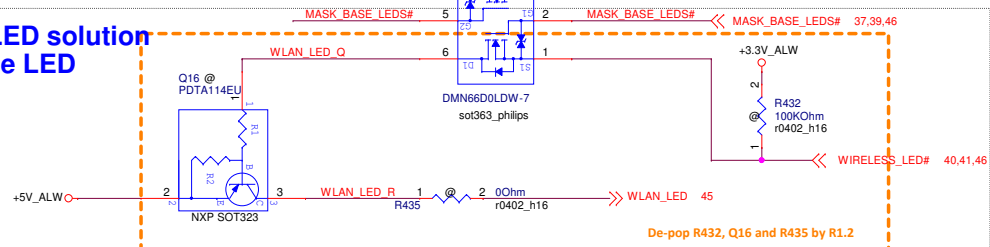
TITLE		Load Switch		
DWG NO.		CORE_B2	REV. 2.0	
DATE		Friday, March 18, 2016	SHEET 51 of 81	



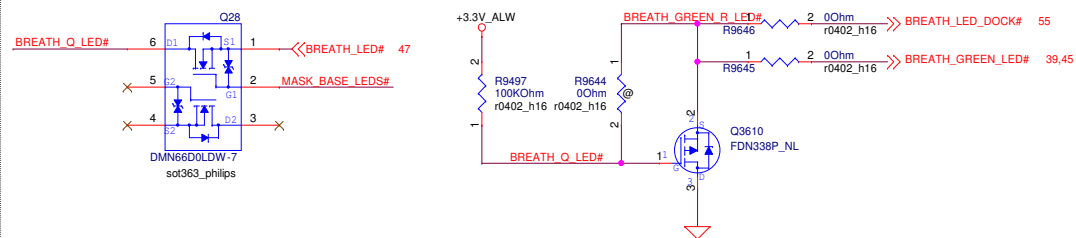
HDD LED



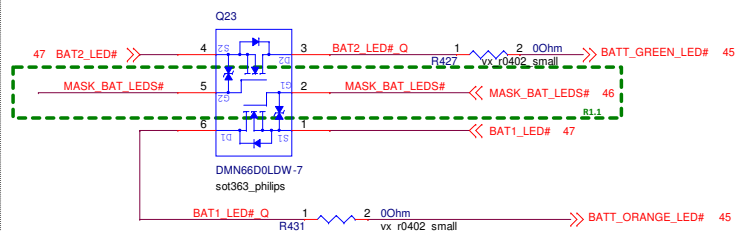
WLAN LED solution for White LED



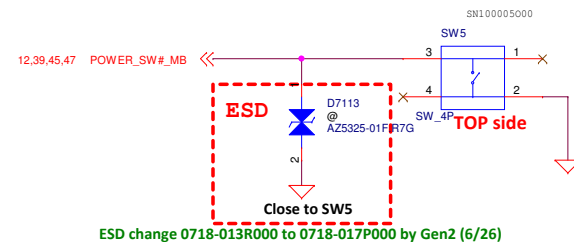
Breath LED



Battery LED



POWER SWITCH



ESD change 0718-013R000 to 0718-017P000 by Gen2 (6/26)

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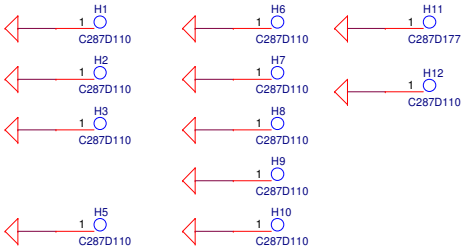
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TITLE LED Control Circuit		
DWG NO.	CORE_B2	REV. 2.0
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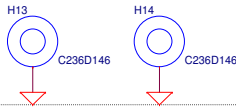
Screw Hole

Screw Hole Φ 2.8mm X7.3

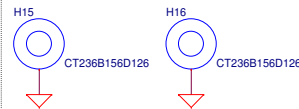


STANDOFF

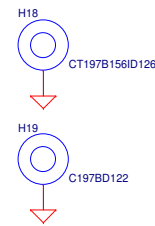
WWAN/WLAN STANDOFF



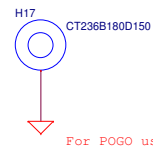
EDP STANDOFF



GPU STANDOFF



PEM STANDOFF

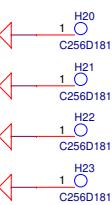


Tooling Hole

Tooling Hole



Tooling Hole



NPTH hole



NPTH hole



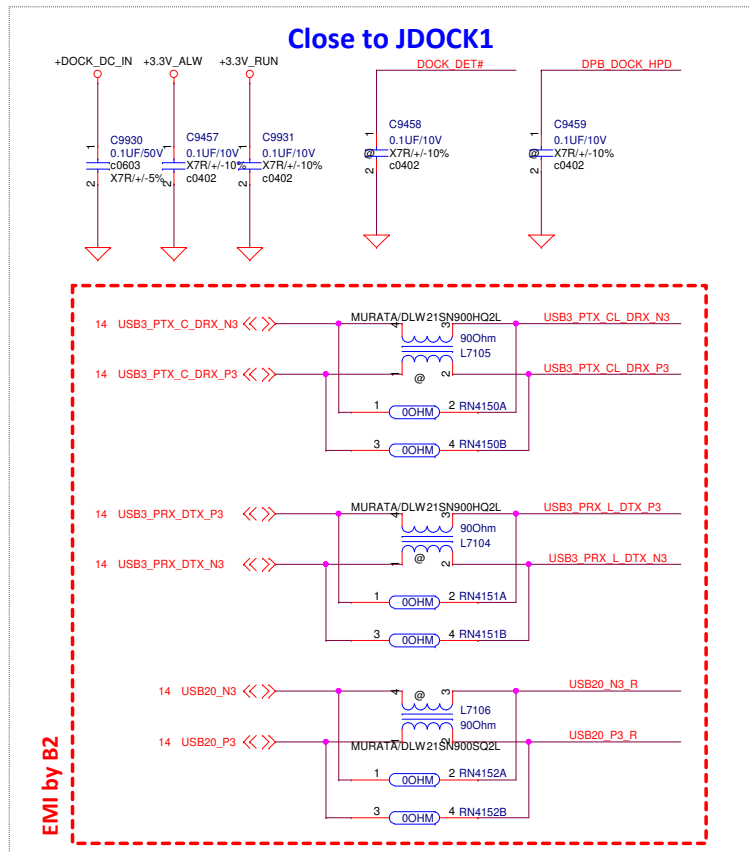
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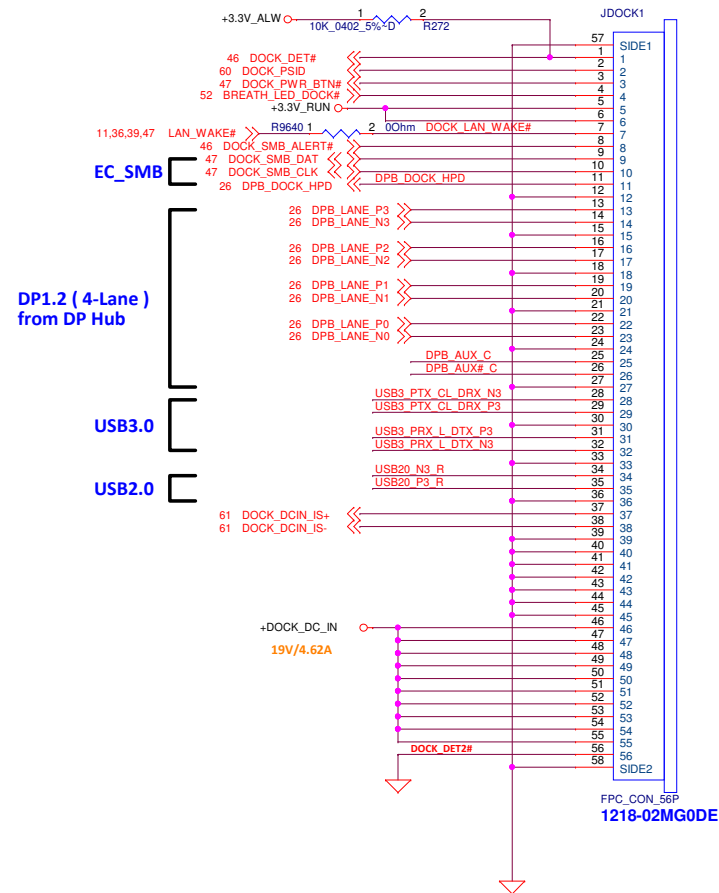
TITLE Mechanical Hole/Standoff
DWG NO. CORE_B2 REV. 2.0
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Docking Connector



26 DPB_AUX# X7R/+/-10% 0.1UF/10V 2 1 C9948 DPB_AUX# C
26 DPB_AUX# X7R/+/-10% 0.1UF/10V 2 1 C9949 DPB_AUX# C



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DWG NO. CORE_B2		REV. 2.0			
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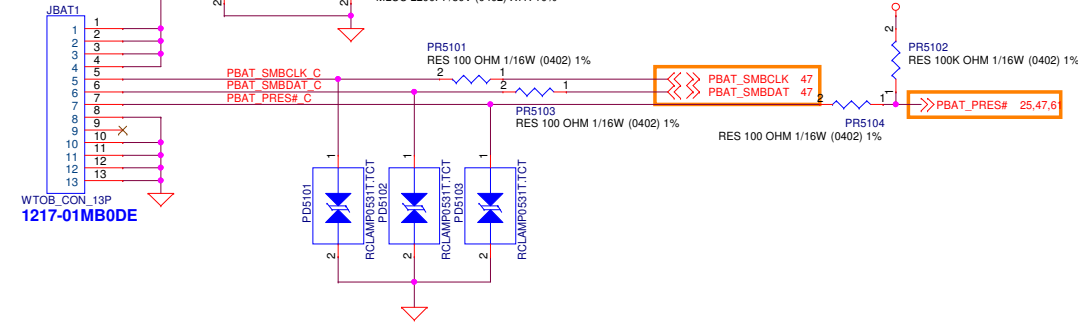
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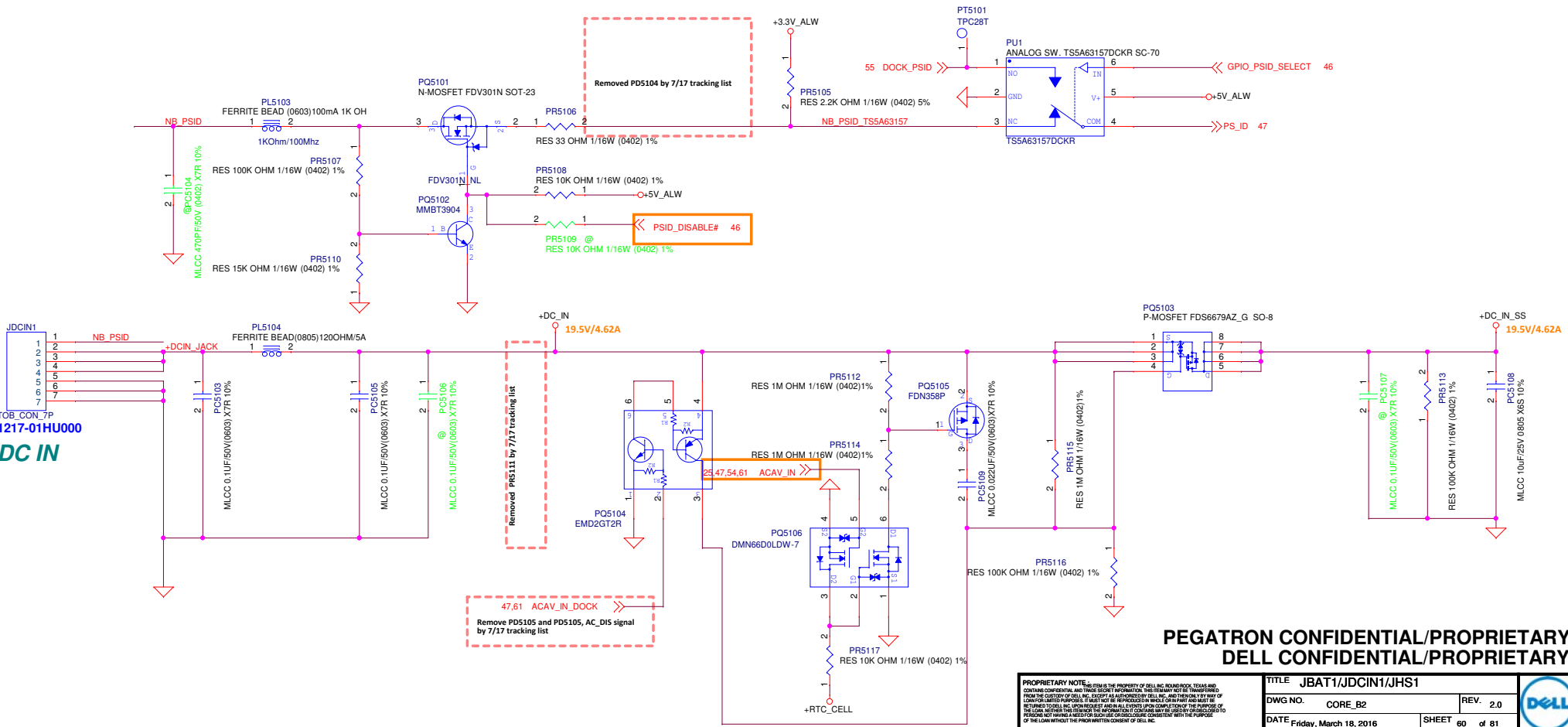
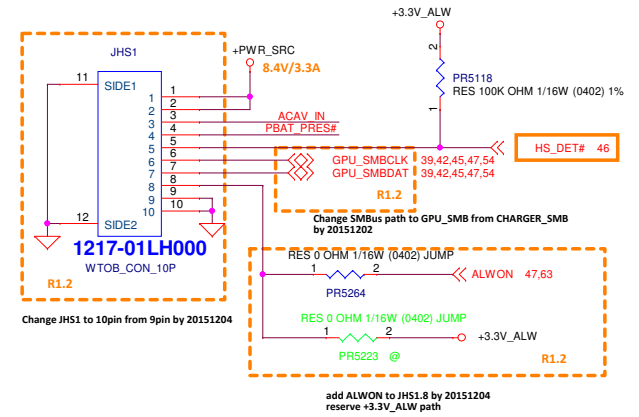
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Batt CON



Hot Swap Conn.



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TITLE JBAT1/JDCIN1/JHS1		
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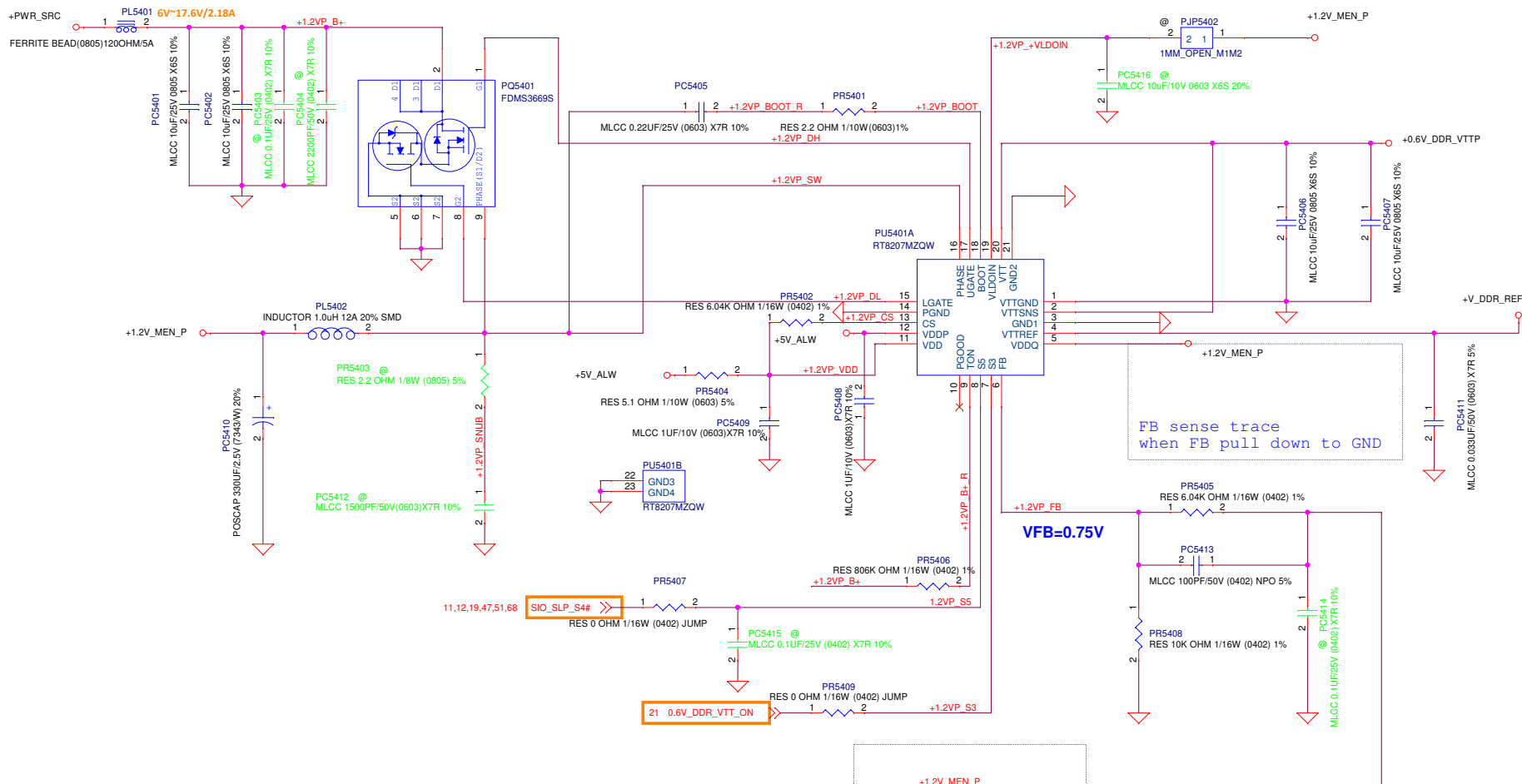
TITLE		Charger IC (BQ24777RUYR)		
DWG NO.		CORE_B2	REV. 2.0	
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+0.6V_DDR_VTT	
TDC -->	1.05A
Peak -->	1.5A

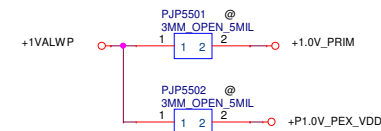
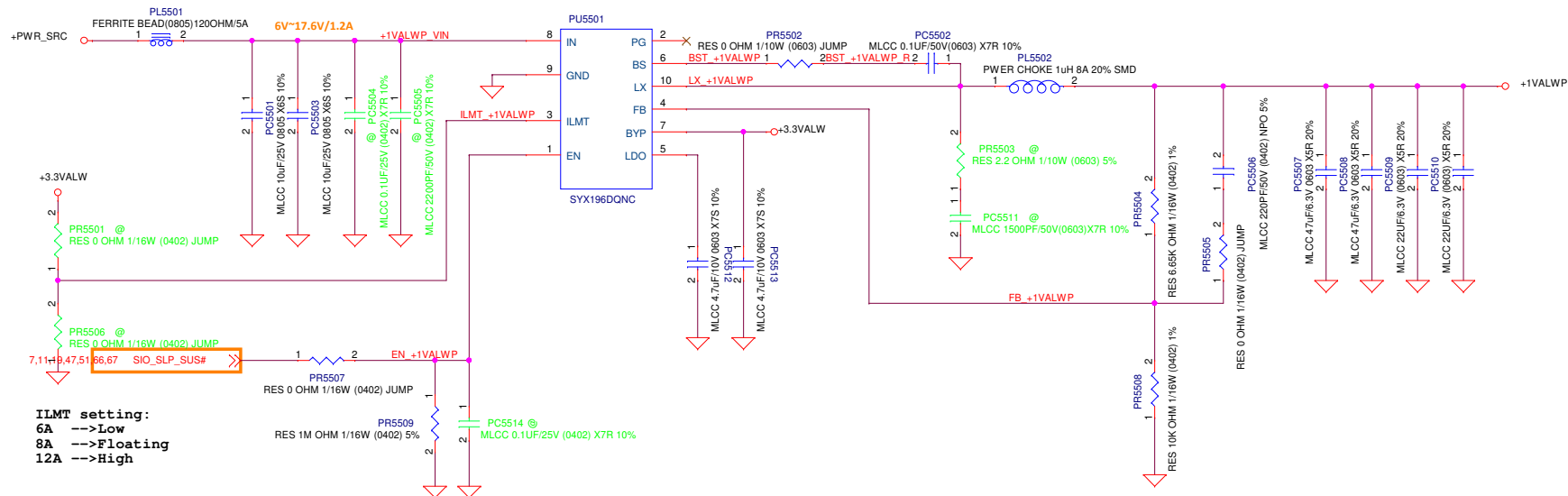
+1.2V_MEM	
TDC -->	8.75A
Peak -->	12.25A
OCP -->	14A
Fsw=300 kHz	

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TITLE +0.6V_DDR_VTT/+1.2V_MEM		
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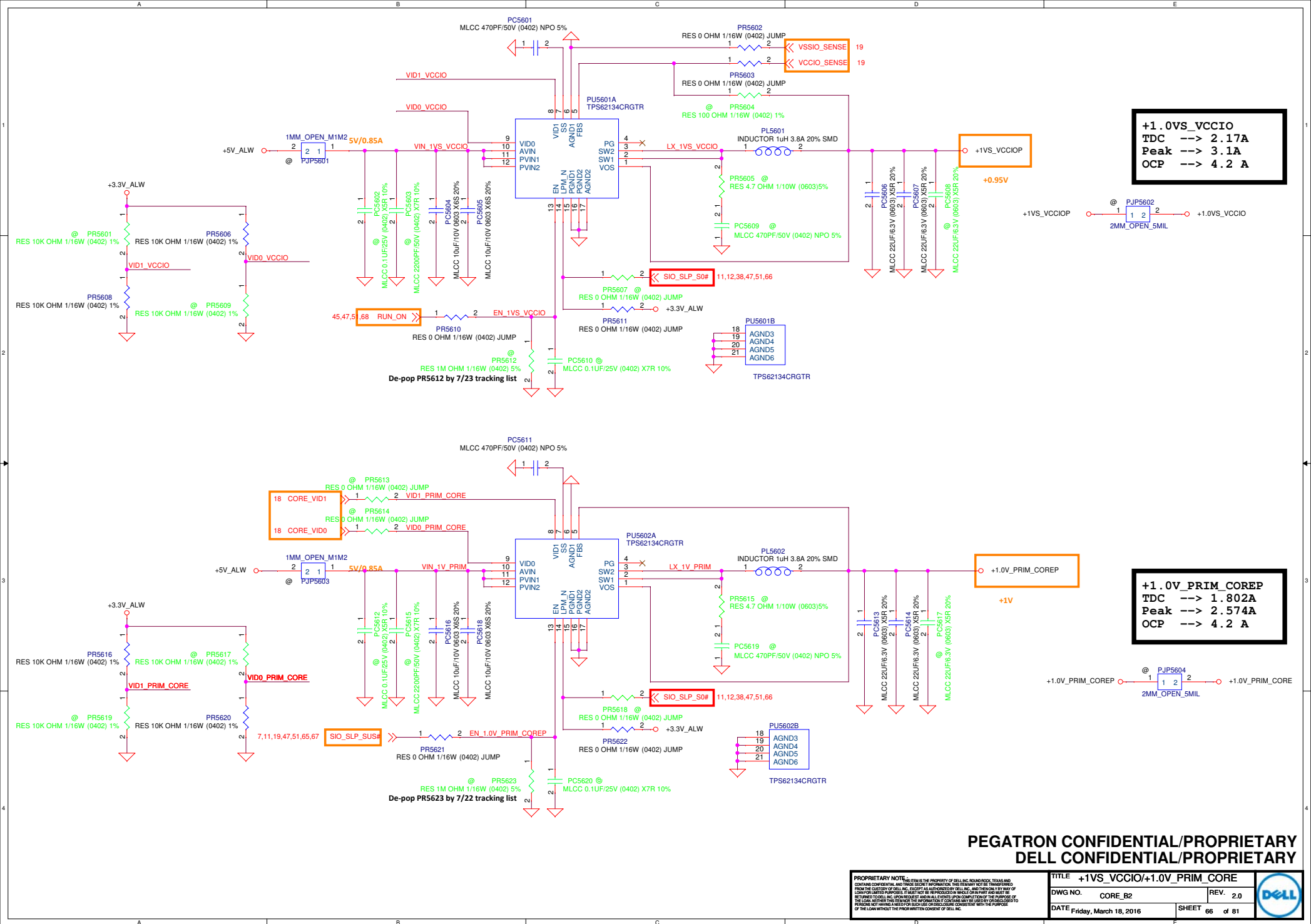


+1VALWP	
TDC -->	5.12A
Peak -->	7.212 A
OCF -->	8 A

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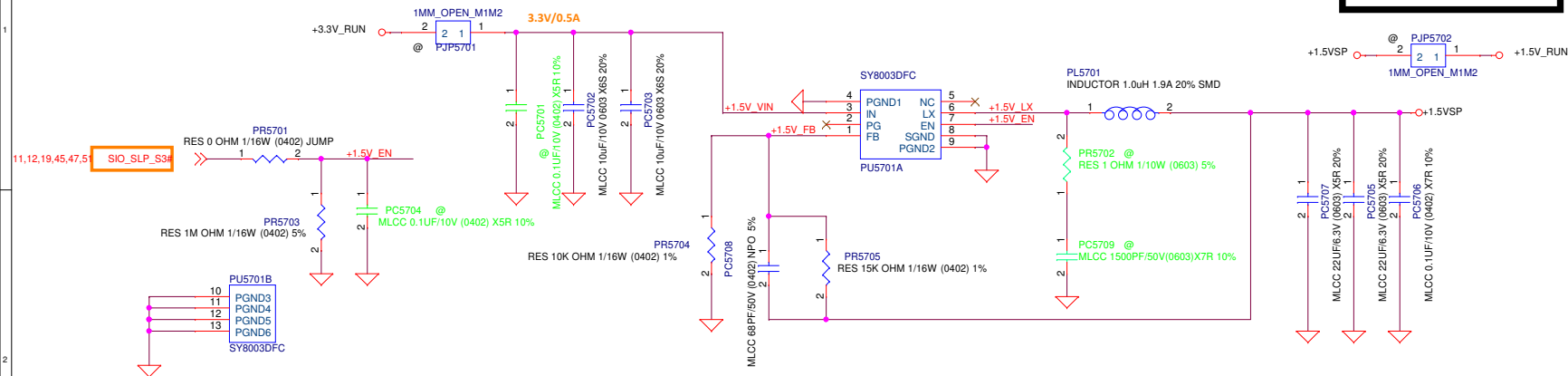
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TITLE +1VS_VCCIO/+1.0V_PRIM_CORE	
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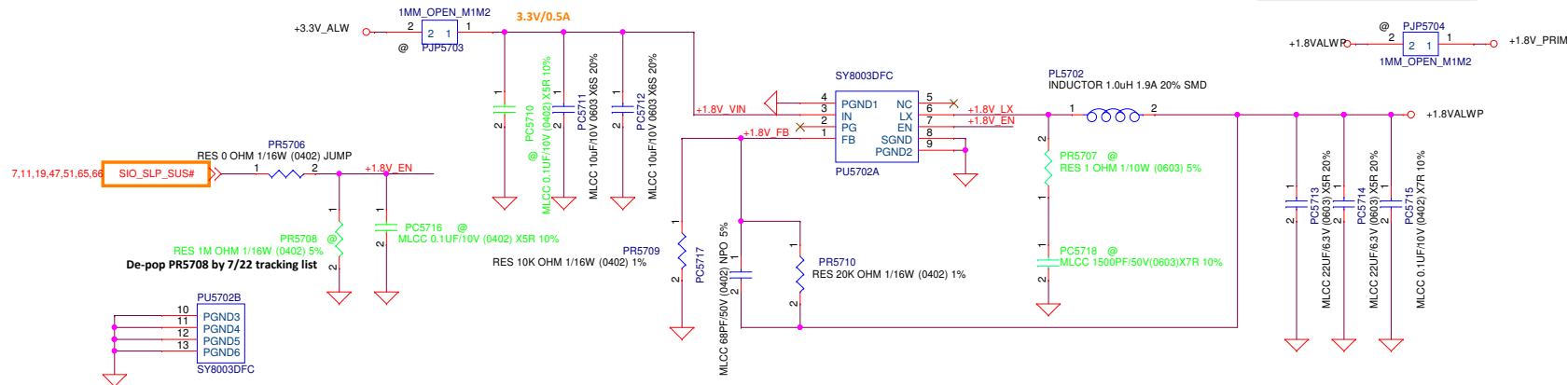
1.5V_RUN

+1.5V_RUN
TDC --> 0.47A
Peak --> 0.671A



+1.8V_PRIM

+1.8V_PRIM
TDC --> 0.292A
Peak --> 0.417A



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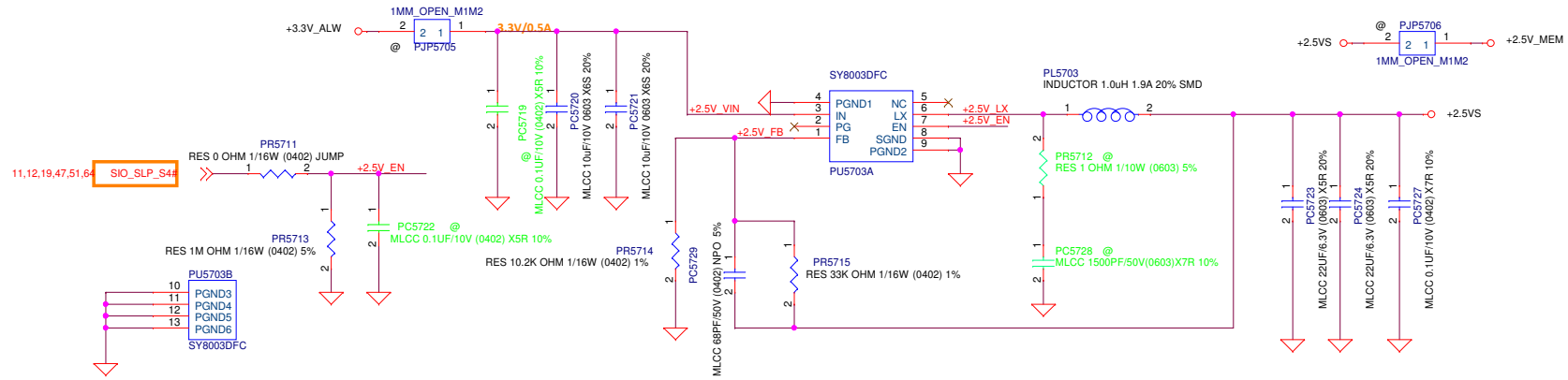
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TITLE +1.5V_RUN/+1.8V_PRIM		
DWG NO.	CORE_B2	REV. 2.0
DATE	Friday, March 18, 2016	SHEET 67 of 81



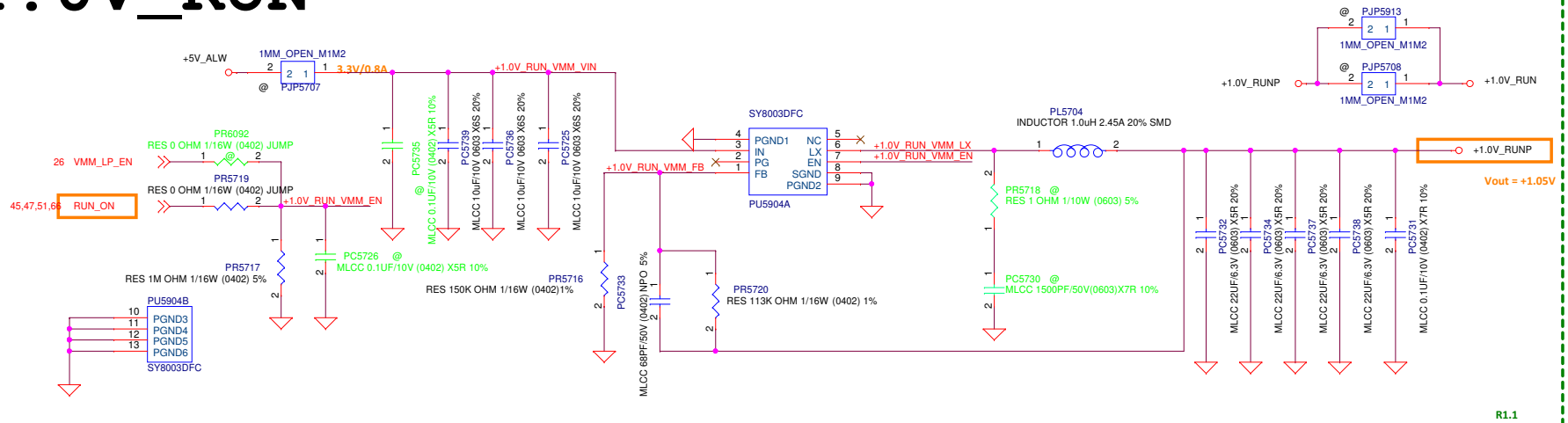
+2.5V_MEM

+2.5V_MEM
TDC --> 0.45A
Peak --> 0.6A



+1.0V_RUN

+1.0V_RUN_VMM
TDC --> 1A
Peak --> 2.1A



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TITLE: +2.5V_MEM/+1.0V_RUN_VMM		
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Place PH5801 Near PU5903

Place PH5805 Near PL5906

Place PH5804 Near PU5901

Place PH5602 Near PL5901

Place PH5802 Near PL5905

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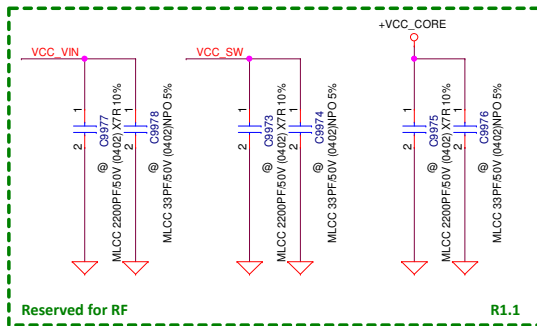
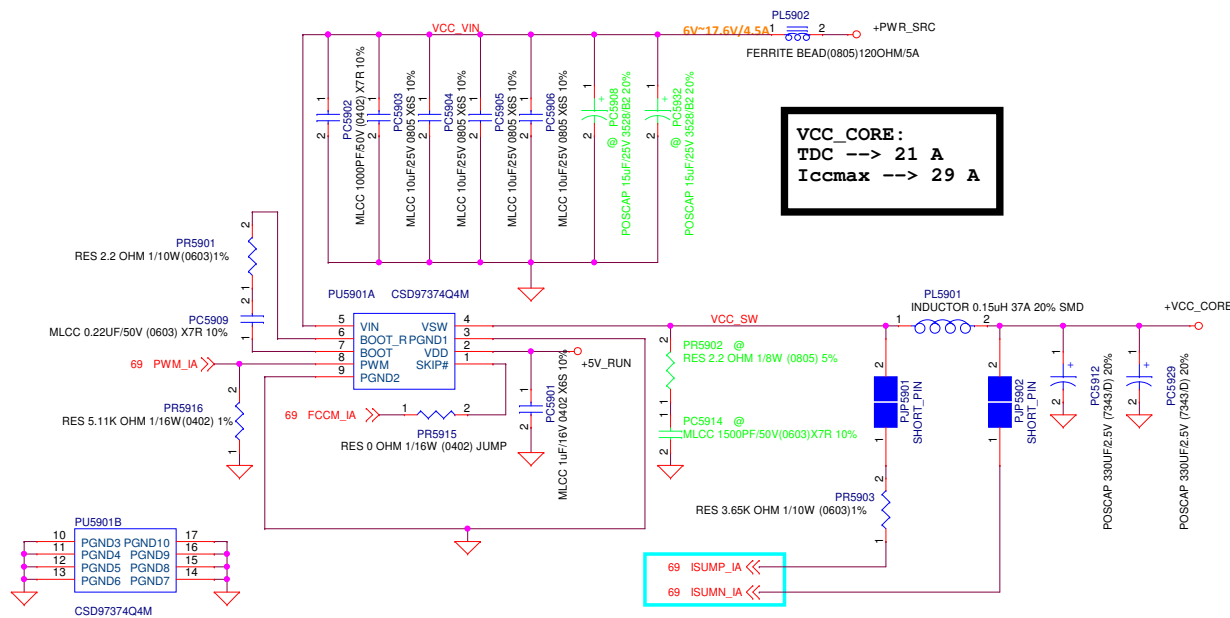
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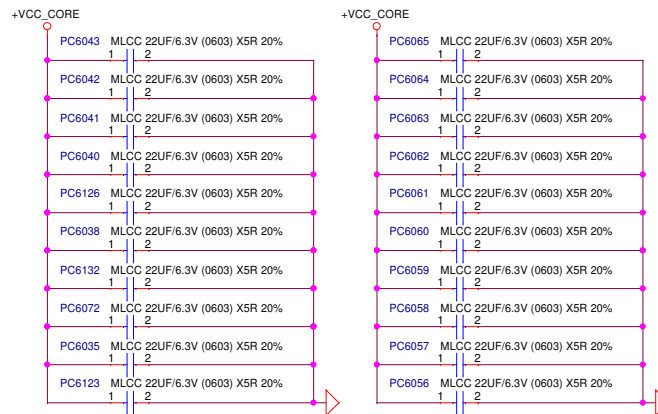
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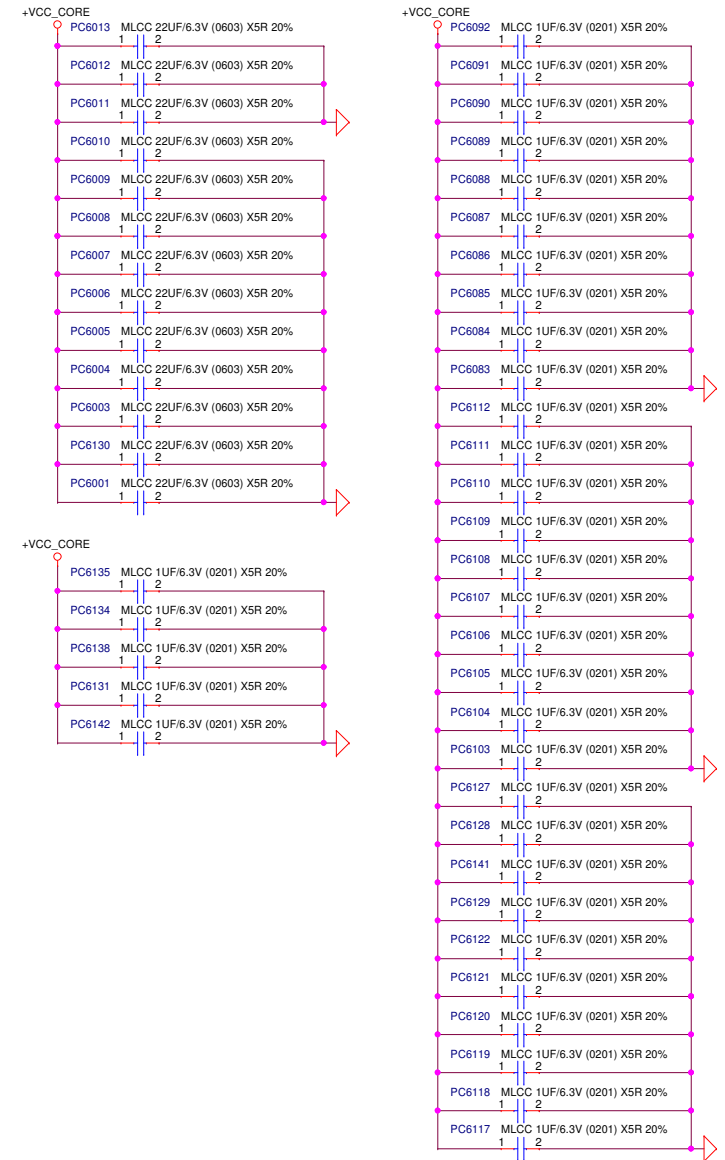
+VCC_CORE Gate Driver



Place 22uF_0603 x20 on CPU Top Side



Place 22uF_0603 x13 and 1uF_0201 x35 on CPU Back Side



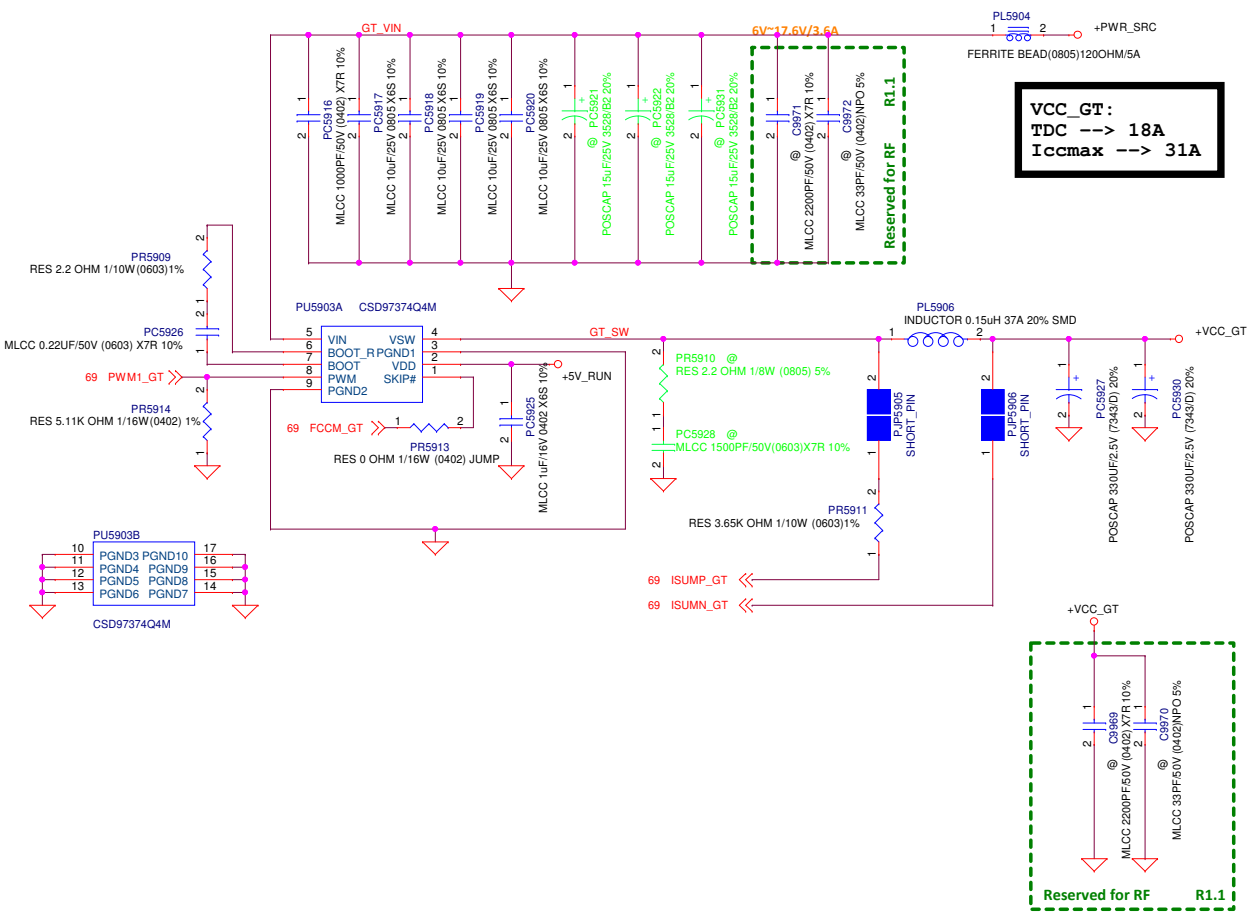
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TITLE +VCC_CORE Gate Driver		
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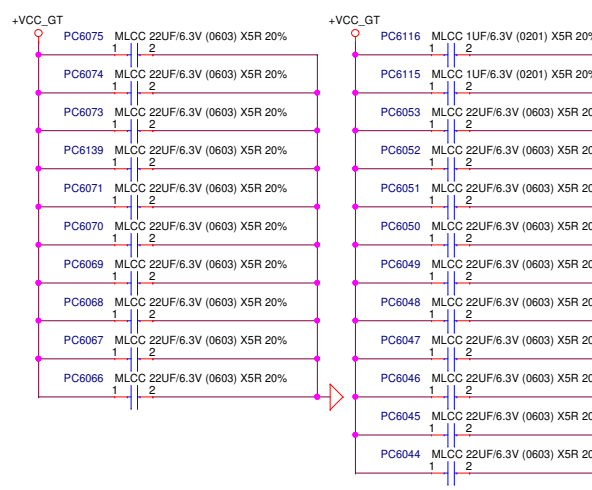
+VCC_GT Gate Driver



Place 22uF_0603 x13 and 1uF_0201 x12 on CPU Back Side



Place 22uF_0603 x20 and 1uF_0201 x2 on CPU Top Side

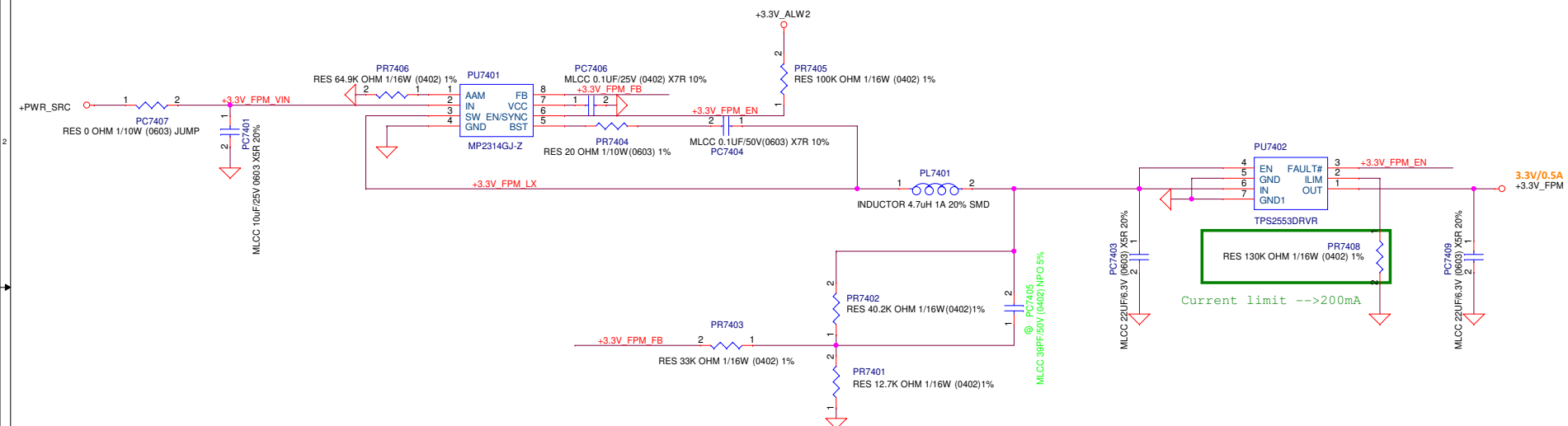


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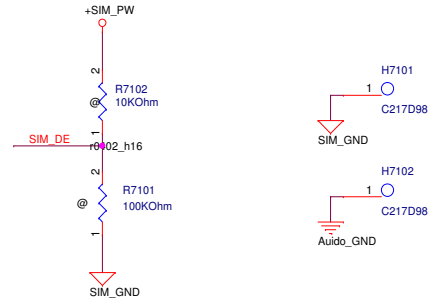
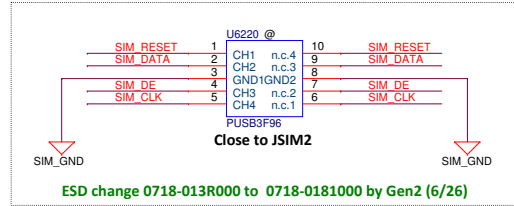
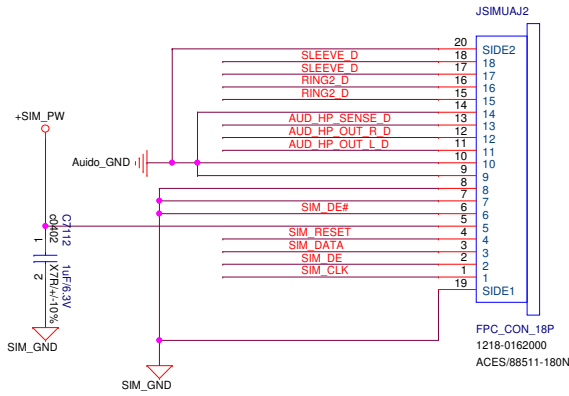
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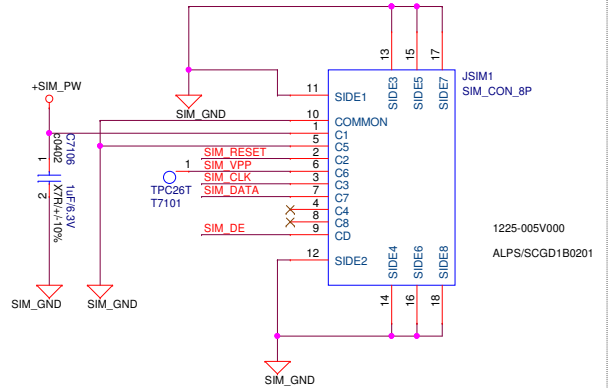
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ZIF Connector to MLB

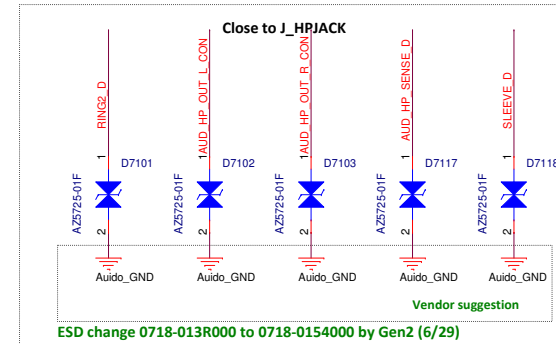
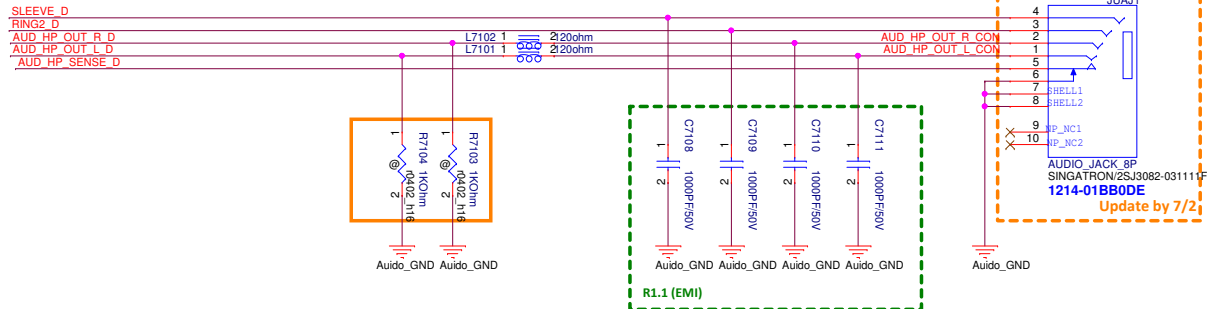


uSIM Card Push-Push



Audio Jack Connector

AUDIO COMBO PHONE JACK
auto sense OMTP and CTIA headset / support MIC-IN / HP & mono mic
SLEEVE_D & RING2_D LAYOUT TRACE WIDTH 80 mils

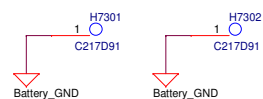
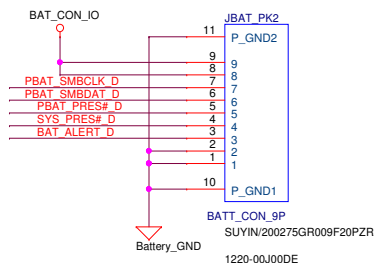


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TITLE	JSIMUAJ2/JSIM1/JUAJ1
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TITLE		JBAT_PK1/JBAT_PK2	
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