

Model : Carrizo-L AIO eMMC
PCB Ver : 1
PCB Number:15019
PCB P/N :
SCH Ver : 1
ECO# number :

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[illegible]

```
BOM Configuration
(R_):Unmount
(C_):Carrizo
(L_):Carrizo-L
(G_):GPU
(H_):UMA
(T_):TOUCH
(D_):Debug used
(B_):Battery Charger
(P_):for non-pAIO and
      w/O Battery Charger
(E_):eMMC
```

PCB BOARD SIZE

6 Layers

185mm X 230mm

-1 BUILD

AMD Carrioz/-L Platform

LAN : Gb LAN RTL811H

AUDIO: ALC3661

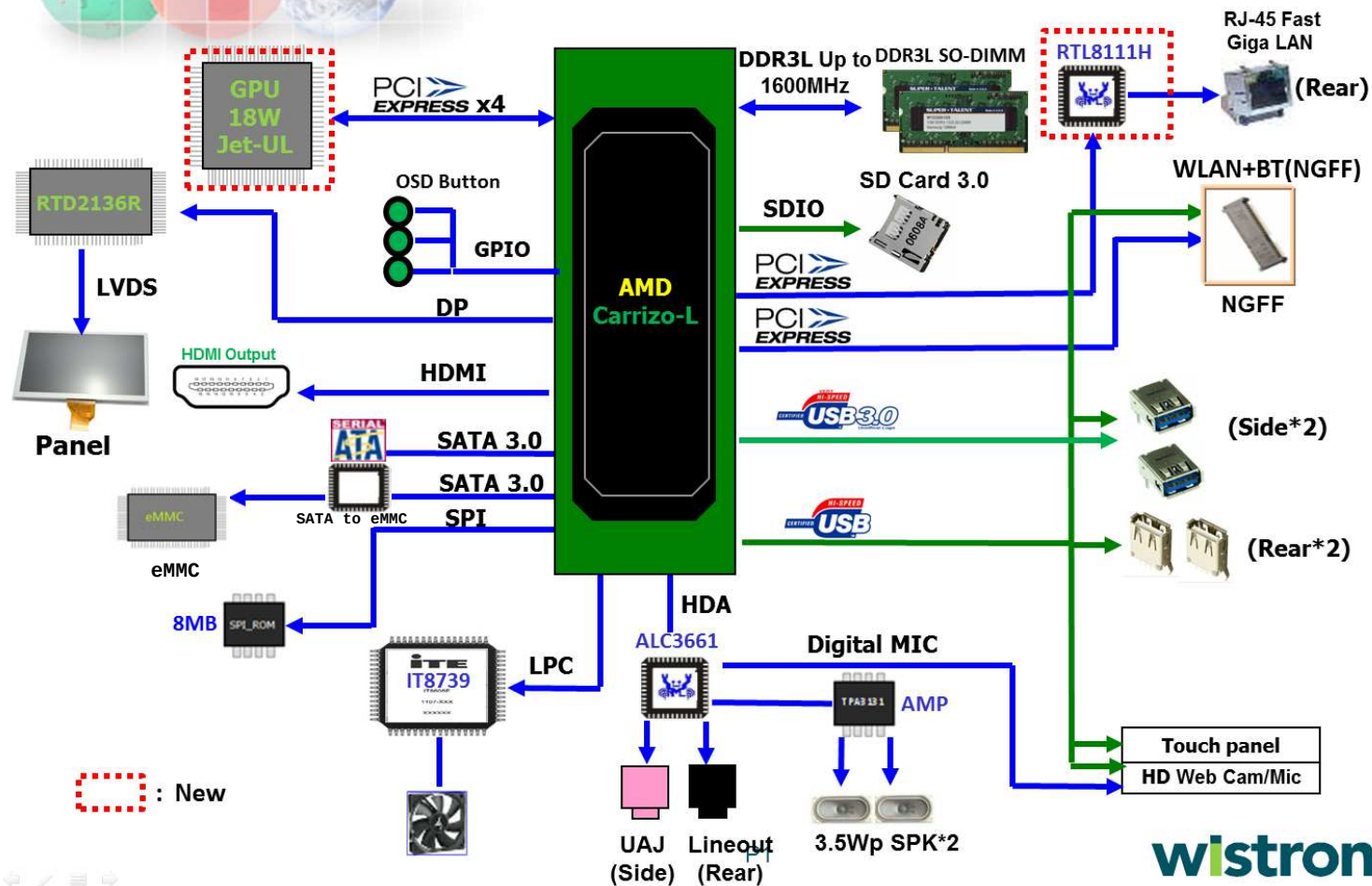
SIO_EC:ITE8739

Project Name: Orchid/Ontario Carrizo AIO
 Project Code: 3PD02001000
 PCB Version: SA
 PCB Number :15019

PCB BOARD SIZE
 185mm X 230mm
 6 Layer

Internal Slot/Header
 Front/Rear IO
 Chipset

Block Diagram for AMD Carrizo-L



wistron

Blanking

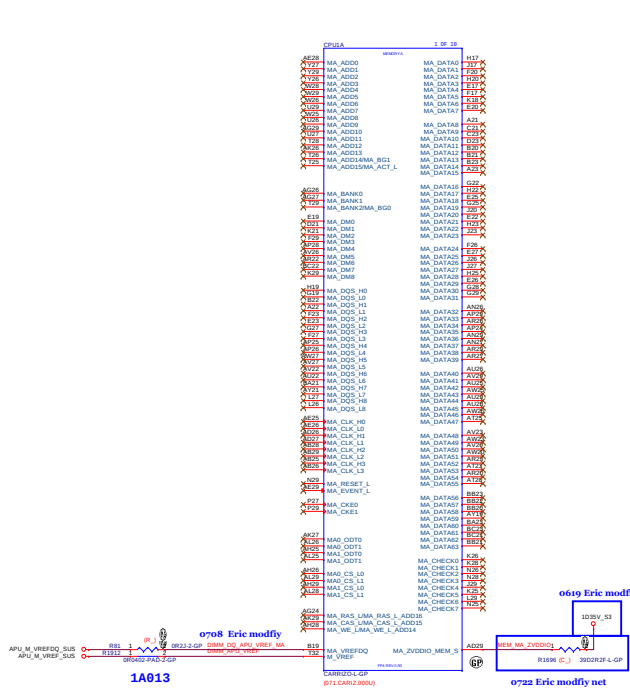
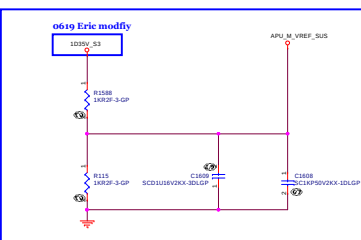
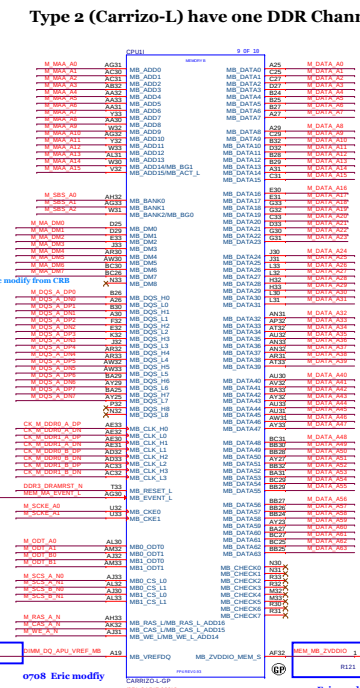
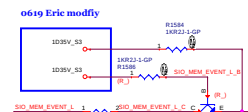
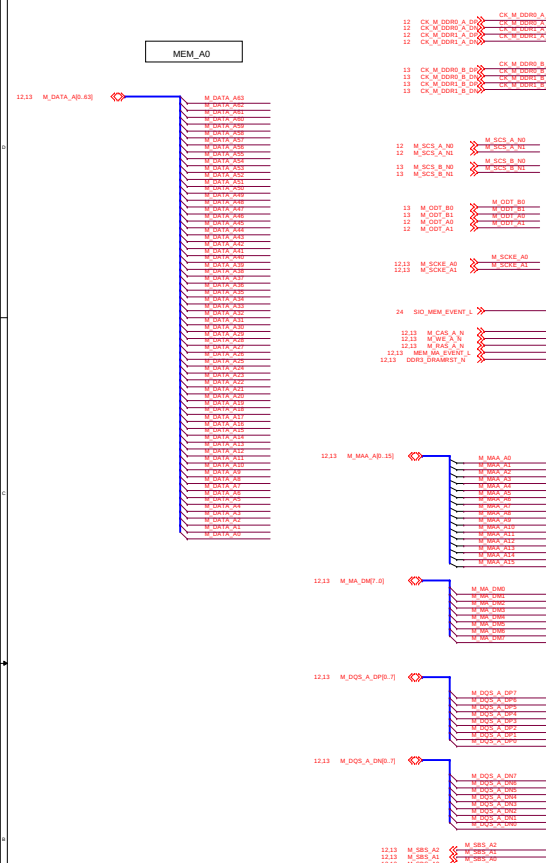
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Size A	Document Number Rosa_Carrizo AIO		Rev -1
Date:	Wednesday, July 01, 2015	Sheet	3 of 105

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0625 Eric modify for 2 DIMMs

Type 2 (Carrizo-L) have one DDR Channel,Labeled B



Group	Signal Name	Pin Type ¹	Connection	Termination ²	Level Shift ³	Termination Voltage	FP4 Processor Types									
							1	2	1	2	1	2	1	2	1	2
	MA_ZVIDEO_MEM_5	A	Pull-up resistor	—	39.2k (1.1V)	—	—	—	—	VIDEO_MEM_5_3	—	—	—	—	—	
	MB_ZVIDEO_MEM_5	A	Pull-up resistor	—	39.2k (2.1V)	—	—	—	—	VIDEO_MEM_5_3	—	—	—	—	—	

Table 3. Valid Socketed-Memory Configurations

Memory Type	Bus Layers	Number of DIMM Banks	Number of DIMMs Populated	DIMM 0	DIMM 1
UDIMM	4 or 6	1	1	500 DIM	
		2	1		500 DIM
			2	500 DIM	500 DIM
SO-DIMM	6	1	1	500 DIM	
			1		500 DIM
		2	2	500 DIM	500 DIM

Table 13. Memory Feature Compatibility

Memory Feature	FPGA Package	
	Type 1	Type 2
Memory Controller(s)	DDR3 Dual Channel	DDR3 Single Channel

5.1 Memory Interface

There are four signal groups for the memory bus interface—a Data group, a Control group, an Address/Command group, and a Clock group. The two types of FP4 processors support different memory configurations. See Table 1 for a list of FP4 processor type feature sets.

- Type 1 processors have two DDR3 channels, labeled A and B.
- Type 2 processors have one DDR3 channel, labeled B.

See the sections that follow for memory package-specific and implementation-specific information and design considerations.



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Title

Size
A

Document Number

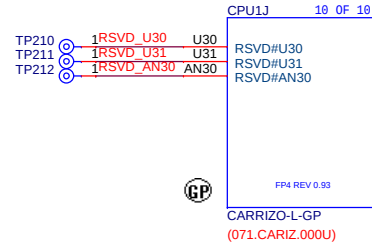
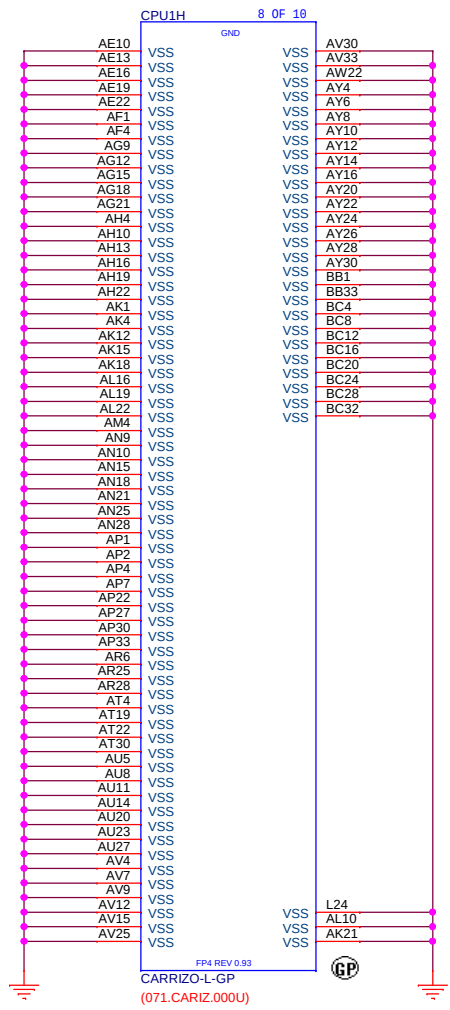
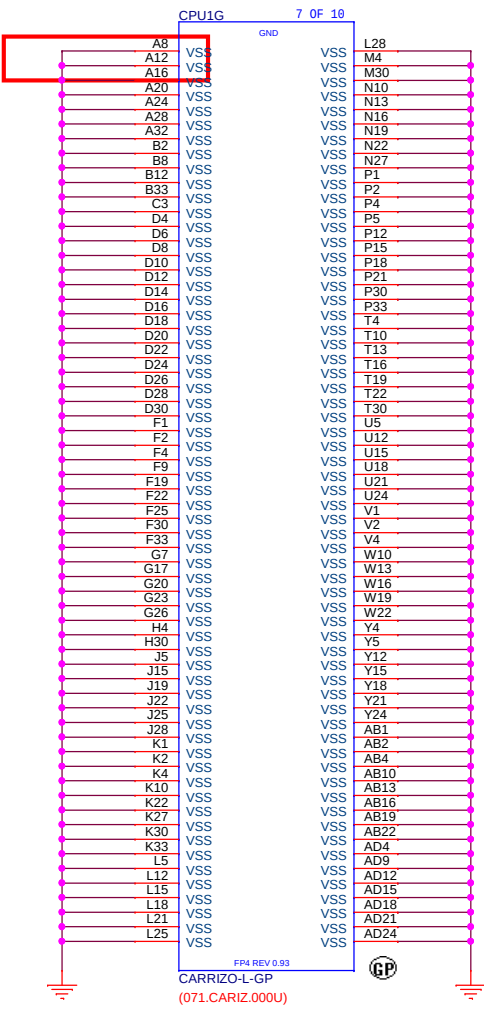
Rosa_Carrizo AIO

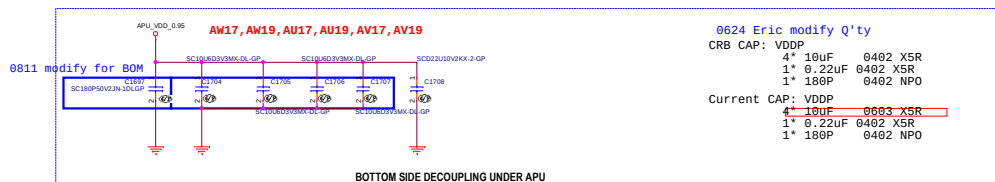
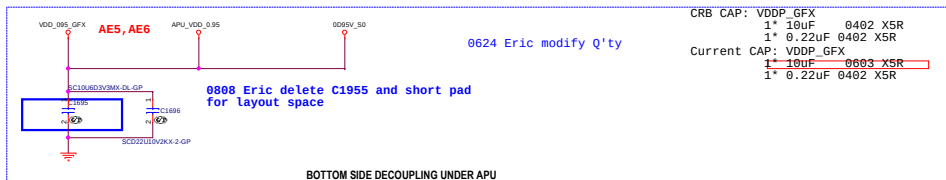
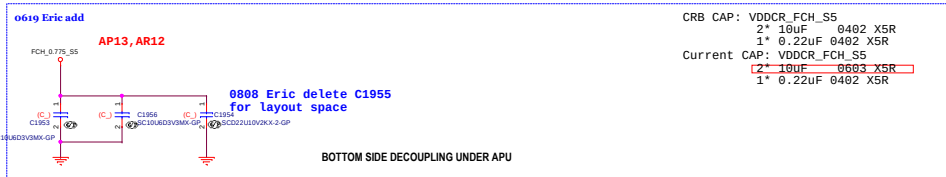
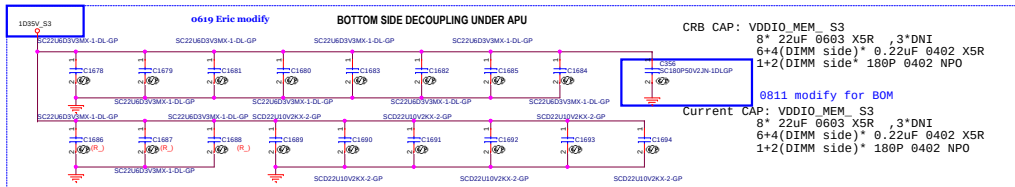
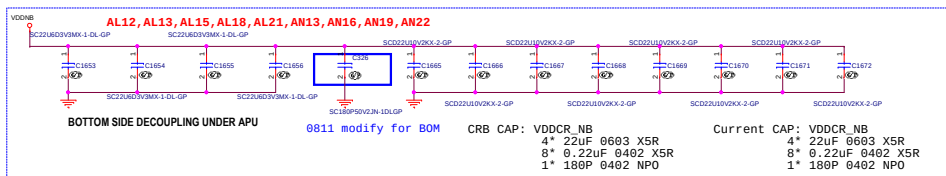
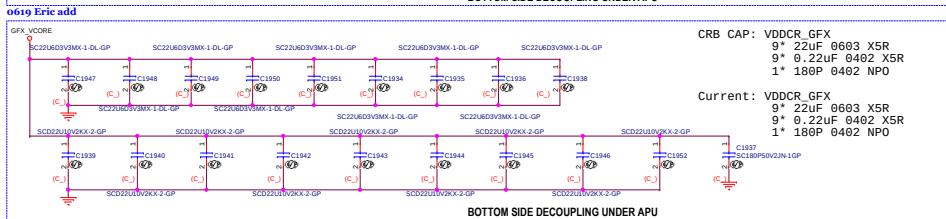
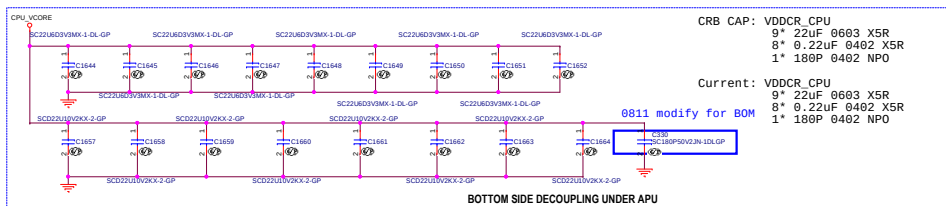
Rev
-1

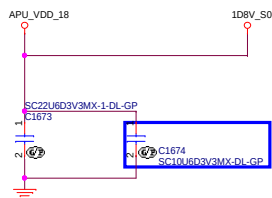
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AMD CRB for socket



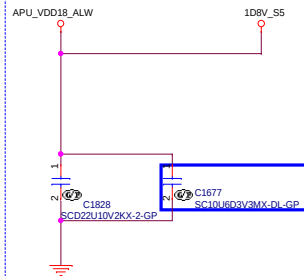




AP16, AP18

CRB CAP: VDDP_18
1* 10uF 0402 X5R
1* 22uF 0603 X5R

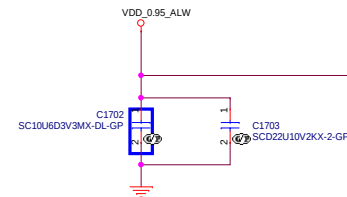
```
Current CAP: VDDP_18
1* 10uF 0603 X5R
1* 22uF 0603 X5R
```



AP10, AR9

CRB CAP: VDDP_18_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R

Current CAP: VDDP_18_S5
~~1* 10uF 0603 X5R~~
 1* 0.22uF 0402 X5R

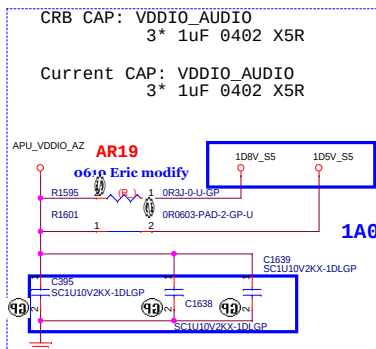


AN12, AP12

```
CRB CAP: VDDP_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R
```

```
Current CAP: VDDP_S5
1* 10uF 0603 X5R
1* 0.22uF 0402 X5R
```

delete for 0.95V_DUAL power rail, no use 0.95V_DUAL from CRB



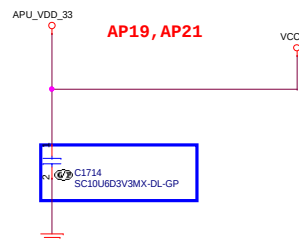
```
CRB CAP: VDDIO_AUDIO
          3* 1uF 0402 X5R

Current CAP: VDDIO_AUDIO
              3* 1uF 0402 X5R
```

AR19

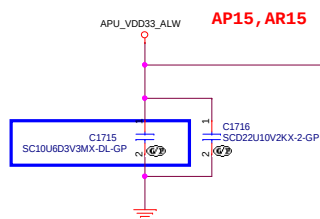
0610 Eric modify

1A015



AP19, AP21

```
CRB CAP: VDD_33
1* 10uF 0402 X5R
Current CAP: VDD_33
1* 10uF 0603 X5R
```



AP15, AR15

```
CRB CAP: VDD_33_S5
1* 10uF 0402 X5R
1* 0.22uF 0402 X5R
Current CAP: VDD_33_S5
1* 10uF 0603 X5R
1* 0.22uF 0402 X5R
```

```
Current CAP: VDD_33_S5
1* 10uF 0603 X5R
1* 0.22uF 0402 X5R
```

0624 Eric delete

0624 Eric delete

```

5.13 M_DATA_A[0..63] << >>
5.13 M_DQS_A_DP[0..7] << >>
5.13 M_DQS_A_DN[0..7] << >>
5.13 M_MA_DM[7..0] << >>

```

```

5,13 M_MAA_A[0..15]
5,13 M_WE_A_N
5,13 M_CAS_A_N
5,13 M_RAS_A_N
5,13 M_SBS_A0
5,13 M_SBS_A1
5,13 M_SBS_A2

```

5	M_SCS_A_N0	
5	M_SCS_A_N1	
5,13	M_SCKE_A0	
5,13	M_SCKE_A1	
5	M_ODT_A0	
5	M_ODT_A1	

```

5 CK_M_DDR0_A_DP
5 CK_M_DDR0_A_DN
5 CK_M_DDR1_A_DP
5 CK_M_DDR1_A_DN

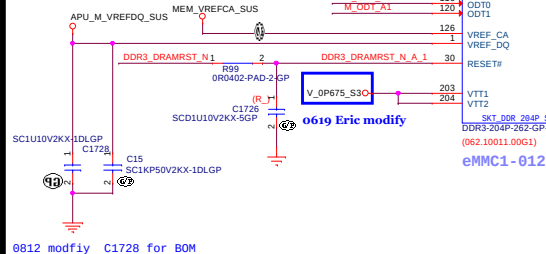
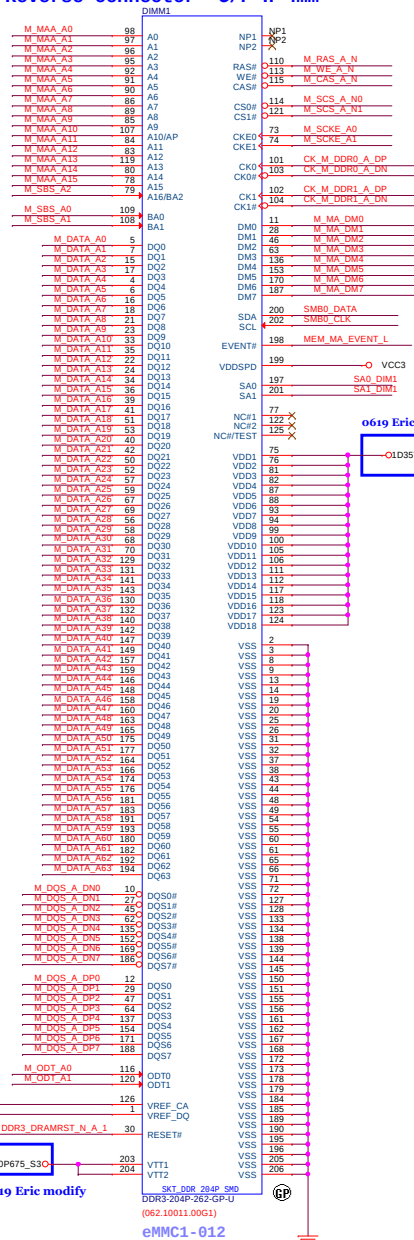
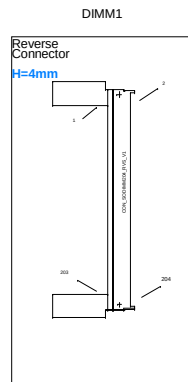
```

5.13 DDR3_DRAMRST_N <<—

13,18,55,67 SMB0_CLK <<<—

13,18,55,67 SMB0_DATA <<<—

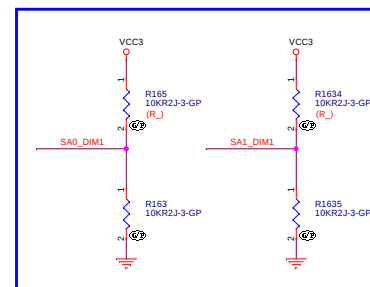
5.13 MEM MA EVENT L <<—



0812 modfiy C1728 for BOM

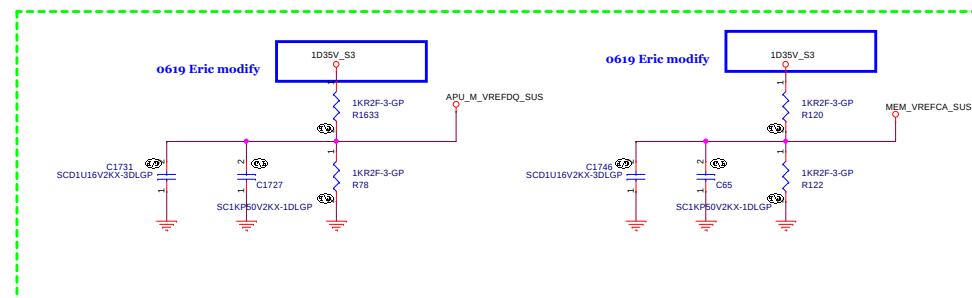
The image displays three circuit diagrams, each representing a different power plane: 0610, 0810, and 0811.

- 0610 eric modify for DIMM Slot Decoupling:** This diagram shows a power plane with a 1D35V_S3 input. It features several decoupling capacitors (C353, C337, C1723, C60, C392, C46) connected to a common rail. The rail is connected to a 1D35V_S3 input and a 0811 eric modify for BOM output. The capacitors are labeled with their values and the rail they connect to (e.g., SCD1U16V2KX-3DLGP).
- 0810 eric modify for BOM:** This diagram shows a power plane with a 1D35V_S3 input. It features a decoupling capacitor (C353) connected to a common rail. The rail is connected to a 1D35V_S3 input and a 0811 eric modify for BOM output. The capacitor is labeled with its value and the rail it connects to (e.g., SCD1U16V2KX-3DLGP).
- 0811 eric modify for BOM:** This diagram shows a power plane with a 1D35V_S3 input. It features a decoupling capacitor (C353) connected to a common rail. The rail is connected to a 1D35V_S3 input and a 0811 eric modify for BOM output. The capacitor is labeled with its value and the rail it connects to (e.g., SCD1U16V2KX-3DLGP).



```
CRB CAP: VDDIO_MEM_S3
        6* 0.1uF 0402 X5R , 6*DNI
        2*100u
        4(DIMM side)* 0.22uF 0402 X5R
        2(DIMM side)* 180P 0402 NPO
```

```
Current CAP: VDDIO_MEM_S3
6* 0.1uF 0402 X5R
4(DIMM side)* 0.22uF 0402 X5R
2(DIMM side)* 180P 0402 NPO
```



DDR DATA

5.12 M_DATA_A0[63]
5.12 M_DQS_A_D0[0:7]
5.12 M_DQS_A_D0[0:7]
5.12 M_MA_DM[7:0]

DDR CMD/ADD

5.12 M_MAA_A0[15]
5.12 M_WE_A_N
5.12 M_CAS_A_N
5.12 M_RAS_A_N

DDR CTRL

5 M_SCS_B_N0
5 M_SCS_B_N1
5.12 M_SCKE_A0
5.12 M_SCKE_A1
5 M_ODT_B0
5 M_ODT_B1

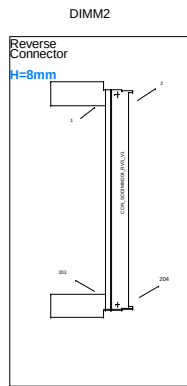
DDR CLOCK

5 CK_M_DDR0_B_DP
5 CK_M_DDR0_B_DN
5 CK_M_DDR1_B_DP
5 CK_M_DDR1_B_DN

DDR OTHERS

5.12 DDR3_DRAMRST_N
12.18.55.67 SMB0_CLK
12.18.55.67 SMB0_DATA
5.12 MEM_MA_EVENT_L

0724 Eric change Symbol to Reverse connector G/F/H=8mm 0724 add F7 for 10u" part



M_MAA_A0	98	A0	NP1	NP2
M_MAA_A1	97	A1	NP1	NP2
M_MAA_A2	96	A2	NP1	NP2
M_MAA_A3	95	A3	NP1	NP2
M_MAA_A4	94	A4	NP1	NP2
M_MAA_A5	93	A5	NP1	NP2
M_MAA_A6	92	A6	NP1	NP2
M_MAA_A7	91	A7	NP1	NP2
M_MAA_A8	90	A8	NP1	NP2
M_MAA_A9	89	A9	NP1	NP2
M_MAA_A10	88	A10	NP1	NP2
M_MAA_A11	87	A11	NP1	NP2
M_MAA_A12	86	A12	NP1	NP2
M_MAA_A13	85	A13	NP1	NP2
M_MAA_A14	84	A14	NP1	NP2
M_MAA_A15	83	A15	NP1	NP2
M_SBS_A0	109	BA0	NP1	NP2
M_SBS_A1	108	BA1	NP1	NP2
M_DATA_A0	5	DQ0	NP1	NP2
M_DATA_A1	6	DQ1	NP1	NP2
M_DATA_A2	7	DQ2	NP1	NP2
M_DATA_A3	8	DQ3	NP1	NP2
M_DATA_A4	9	DQ4	NP1	NP2
M_DATA_A5	10	DQ5	NP1	NP2
M_DATA_A6	11	DQ6	NP1	NP2
M_DATA_A7	12	DQ7	NP1	NP2
M_DATA_A8	13	DQ8	NP1	NP2
M_DATA_A9	14	DQ9	NP1	NP2
M_DATA_A10	15	DQ10	NP1	NP2
M_DATA_A11	16	DQ11	NP1	NP2
M_DATA_A12	17	DQ12	NP1	NP2
M_DATA_A13	18	DQ13	NP1	NP2
M_DATA_A14	19	DQ14	NP1	NP2
M_DATA_A15	20	DQ15	NP1	NP2
M_DATA_A16	21	DQ16	NP1	NP2
M_DATA_A17	22	DQ17	NP1	NP2
M_DATA_A18	23	DQ18	NP1	NP2
M_DATA_A19	24	DQ19	NP1	NP2
M_DATA_A20	25	DQ20	NP1	NP2
M_DATA_A21	26	DQ21	NP1	NP2
M_DATA_A22	27	DQ22	NP1	NP2
M_DATA_A23	28	DQ23	NP1	NP2
M_DATA_A24	29	DQ24	NP1	NP2
M_DATA_A25	30	DQ25	NP1	NP2
M_DATA_A26	31	DQ26	NP1	NP2
M_DATA_A27	32	DQ27	NP1	NP2
M_DATA_A28	33	DQ28	NP1	NP2
M_DATA_A29	34	DQ29	NP1	NP2
M_DATA_A30	35	DQ30	NP1	NP2
M_DATA_A31	36	DQ31	NP1	NP2
M_DATA_A32	37	DQ32	NP1	NP2
M_DATA_A33	38	DQ33	NP1	NP2
M_DATA_A34	39	DQ34	NP1	NP2
M_DATA_A35	40	DQ35	NP1	NP2
M_DATA_A36	41	DQ36	NP1	NP2
M_DATA_A37	42	DQ37	NP1	NP2
M_DATA_A38	43	DQ38	NP1	NP2
M_DATA_A39	44	DQ39	NP1	NP2
M_DATA_A40	45	DQ40	NP1	NP2
M_DATA_A41	46	DQ41	NP1	NP2
M_DATA_A42	47	DQ42	NP1	NP2
M_DATA_A43	48	DQ43	NP1	NP2
M_DATA_A44	49	DQ44	NP1	NP2
M_DATA_A45	50	DQ45	NP1	NP2
M_DATA_A46	51	DQ46	NP1	NP2
M_DATA_A47	52	DQ47	NP1	NP2
M_DATA_A48	53	DQ48	NP1	NP2
M_DATA_A49	54	DQ49	NP1	NP2
M_DATA_A50	55	DQ50	NP1	NP2
M_DATA_A51	56	DQ51	NP1	NP2
M_DATA_A52	57	DQ52	NP1	NP2
M_DATA_A53	58	DQ53	NP1	NP2
M_DATA_A54	59	DQ54	NP1	NP2
M_DATA_A55	60	DQ55	NP1	NP2
M_DATA_A56	61	DQ56	NP1	NP2
M_DATA_A57	62	DQ57	NP1	NP2
M_DATA_A58	63	DQ58	NP1	NP2
M_DATA_A59	64	DQ59	NP1	NP2
M_DATA_A60	65	DQ60	NP1	NP2
M_DATA_A61	66	DQ61	NP1	NP2
M_DATA_A62	67	DQ62	NP1	NP2
M_DATA_A63	68	DQ63	NP1	NP2
M_DQS_A_D0	10	DQS0	NP1	NP2
M_DQS_A_D1	11	DQS1	NP1	NP2
M_DQS_A_D2	12	DQS2	NP1	NP2
M_DQS_A_D3	13	DQS3	NP1	NP2
M_DQS_A_D4	14	DQS4	NP1	NP2
M_DQS_A_D5	15	DQS5	NP1	NP2
M_DQS_A_D6	16	DQS6	NP1	NP2
M_DQS_A_D7	17	DQS7	NP1	NP2
M_ODT_B0	116	ODT0	NP1	NP2
M_ODT_B1	117	ODT1	NP1	NP2
M_ODT_B2	118	ODT2	NP1	NP2
M_ODT_B3	119	ODT3	NP1	NP2
M_ODT_B4	120	ODT4	NP1	NP2
M_ODT_B5	121	ODT5	NP1	NP2
M_ODT_B6	122	ODT6	NP1	NP2
M_ODT_B7	123	ODT7	NP1	NP2
M_ODT_B8	124	ODT8	NP1	NP2
M_ODT_B9	125	ODT9	NP1	NP2
M_ODT_B10	126	ODT10	NP1	NP2
M_ODT_B11	127	ODT11	NP1	NP2
M_ODT_B12	128	ODT12	NP1	NP2
M_ODT_B13	129	ODT13	NP1	NP2
M_ODT_B14	130	ODT14	NP1	NP2
M_ODT_B15	131	ODT15	NP1	NP2
M_ODT_B16	132	ODT16	NP1	NP2
M_ODT_B17	133	ODT17	NP1	NP2
M_ODT_B18	134	ODT18	NP1	NP2
M_ODT_B19	135	ODT19	NP1	NP2
M_ODT_B20	136	ODT20	NP1	NP2
M_ODT_B21	137	ODT21	NP1	NP2
M_ODT_B22	138	ODT22	NP1	NP2
M_ODT_B23	139	ODT23	NP1	NP2
M_ODT_B24	140	ODT24	NP1	NP2
M_ODT_B25	141	ODT25	NP1	NP2
M_ODT_B26	142	ODT26	NP1	NP2
M_ODT_B27	143	ODT27	NP1	NP2
M_ODT_B28	144	ODT28	NP1	NP2
M_ODT_B29	145	ODT29	NP1	NP2
M_ODT_B30	146	ODT30	NP1	NP2
M_ODT_B31	147	ODT31	NP1	NP2
M_ODT_B32	148	ODT32	NP1	NP2
M_ODT_B33	149	ODT33	NP1	NP2
M_ODT_B34	150	ODT34	NP1	NP2
M_ODT_B35	151	ODT35	NP1	NP2
M_ODT_B36	152	ODT36	NP1	NP2
M_ODT_B37	153	ODT37	NP1	NP2
M_ODT_B38	154	ODT38	NP1	NP2
M_ODT_B39	155	ODT39	NP1	NP2
M_ODT_B40	156	ODT40	NP1	NP2
M_ODT_B41	157	ODT41	NP1	NP2
M_ODT_B42	158	ODT42	NP1	NP2
M_ODT_B43	159	ODT43	NP1	NP2
M_ODT_B44	160	ODT44	NP1	NP2
M_ODT_B45	161	ODT45	NP1	NP2
M_ODT_B46	162	ODT46	NP1	NP2
M_ODT_B47	163	ODT47	NP1	NP2
M_ODT_B48	164	ODT48	NP1	NP2
M_ODT_B49	165	ODT49	NP1	NP2
M_ODT_B50	166	ODT50	NP1	NP2
M_ODT_B51	167	ODT51	NP1	NP2
M_ODT_B52	168	ODT52	NP1	NP2
M_ODT_B53	169	ODT53	NP1	NP2
M_ODT_B54	170	ODT54	NP1	NP2
M_ODT_B55	171	ODT55	NP1	NP2
M_ODT_B56	172	ODT56	NP1	NP2
M_ODT_B57	173	ODT57	NP1	NP2
M_ODT_B58	174	ODT58	NP1	NP2
M_ODT_B59	175	ODT59	NP1	NP2
M_ODT_B60	176	ODT60	NP1	NP2
M_ODT_B61	177	ODT61	NP1	NP2
M_ODT_B62	178	ODT62	NP1	NP2
M_ODT_B63	179	ODT63	NP1	NP2
M_ODT_B64	180	ODT64	NP1	NP2
M_ODT_B65	181	ODT65	NP1	NP2
M_ODT_B66	182	ODT66	NP1	NP2
M_ODT_B67	183	ODT67	NP1	NP2
M_ODT_B68	184	ODT68	NP1	NP2
M_ODT_B69	185	ODT69	NP1	NP2
M_ODT_B70	186	ODT70	NP1	NP2
M_ODT_B71	187	ODT71	NP1	NP2
M_ODT_B72	188	ODT72	NP1	NP2
M_ODT_B73	189	ODT73	NP1	NP2
M_ODT_B74	190	ODT74	NP1	NP2
M_ODT_B75	191	ODT75	NP1	NP2
M_ODT_B76	192	ODT76	NP1	NP2
M_ODT_B77	193	ODT77	NP1	NP2
M_ODT_B78	194	ODT78	NP1	NP2
M_ODT_B79	195	ODT79	NP1	NP2
M_ODT_B80	196	ODT80	NP1	NP2
M_ODT_B81	197	ODT81	NP1	NP2
M_ODT_B82	198	ODT82	NP1	NP2
M_ODT_B83	199	ODT83	NP1	NP2
M_ODT_B84	200	ODT84	NP1	NP2
M_ODT_B85	201	ODT85	NP1	NP2
M_ODT_B86	202	ODT86	NP1	NP2
M_ODT_B87	203	ODT87	NP1	NP2
M_ODT_B88	204	ODT88	NP1	NP2
M_ODT_B89	205	ODT89	NP1	NP2
M_ODT_B90	206	ODT90	NP1	NP2
M_ODT_B91	207	ODT91	NP1	NP2
M_ODT_B92	208	ODT92	NP1	NP2
M_ODT_B93	209	ODT93	NP1	NP2
M_ODT_B94	210	ODT94	NP1	NP2
M_ODT_B95	211	ODT95	NP1	NP2
M_ODT_B96	212	ODT96	NP1	NP2
M_ODT_B97	213	ODT97	NP1	NP2
M_ODT_B98	214	ODT98	NP1	NP2
M_ODT_B99	215	ODT99	NP1	NP2
M_ODT_B100	216	ODT100	NP1	NP2
M_ODT_B101	217	ODT101	NP1	NP2
M_ODT_B102	218	ODT102	NP1	NP2
M_ODT_B103	219	ODT103	NP1	NP2
M_ODT_B104	220	ODT104	NP1	NP2
M_ODT_B105	221	ODT105	NP1	NP2
M_ODT_B106	222	ODT106	NP1	NP2
M_ODT_B107	223	ODT107	NP1	NP2
M_ODT_B108	224	ODT108	NP1	NP2
M_ODT_B109	225	ODT109	NP1	NP2
M_ODT_B110	226	ODT110	NP1	NP2
M_ODT_B111	227	ODT111	NP1	NP2
M_ODT_B112	228	ODT112	NP1	NP2
M_ODT_B113	229	ODT113	NP1	NP2
M_ODT_B114	230	ODT114	NP1	NP2
M_ODT_B115	231	ODT115	NP1	NP2
M_ODT_B116	232	ODT116	NP1	NP2
M_ODT_B117	233	ODT117	NP1	NP2
M_ODT_B118	234	ODT118	NP1	NP2
M_ODT_B119	235	ODT119	NP1	NP2
M_ODT_B120	236	ODT120	NP1	NP2
M_ODT_B121	237	ODT121	NP1	NP2
M_ODT_B122	238	ODT122	NP1	NP2
M_ODT_B123	239	ODT123	NP1	NP2
M_ODT_B124	240	ODT124	NP1	NP2
M_ODT_B125	241	ODT125	NP1	NP2
M_ODT_B126	242	ODT126	NP1	NP2
M_ODT_B127	243	ODT127	NP1	NP2
M_ODT_B128	244	ODT128	NP1	NP2
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M_ODT_B130	246	ODT130	NP1	NP2
M_ODT_B131	247	ODT131	NP1	NP2
M_ODT_B132	248	ODT132	NP1	NP2
M_ODT_B133	249	ODT133	NP1	NP2
M_ODT_B134	250	ODT134	NP1	NP2
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M_ODT_B136	252	ODT136	NP1	NP2
M_ODT_B137	253	ODT137	NP1	NP2
M_ODT_B138	254	ODT138	NP1	NP2
M_ODT_B139	255	ODT139	NP1	NP2
M_ODT_B140	256	ODT140	NP1	NP2
M_ODT_B141	257	ODT141	NP1	NP2
M_ODT_B142	258	ODT142	NP1	NP2
M_ODT_B143	259	ODT143	NP1	NP2
M_ODT_B144	260	ODT144	NP1	NP2
M_ODT_B145	261	ODT145	NP1	NP2
M_ODT_B146	262	ODT146	NP1	NP2
M_ODT_B147	263	ODT147	NP1	NP2
M_ODT_B148	264	ODT148	NP1	NP2
M_ODT_B149	265	ODT149	NP1	NP2
M_ODT_B150	266	ODT150	NP1	NP2
M_ODT_B151	267	ODT151	NP1	NP2
M_ODT_B152	268	ODT152	NP1	NP2
M_ODT_B153	269	ODT153	NP1	NP2
M_ODT_B154	270	ODT154	NP1	NP2
M_ODT_B155	271	ODT155	NP1	NP2
M_ODT_B156	272	ODT156	NP1	NP2
M_ODT_B157	273	ODT157	NP1	NP2
M_ODT_B158	274	ODT158	NP1	NP2
M_ODT_B159	275	ODT159	NP1	NP2
M_ODT_B160	276	ODT160	NP1	NP2
M_ODT_B161	277	ODT161	NP1	NP2
M_ODT_B162	278	ODT162	NP1	NP2
M_ODT_B163	279	ODT163	NP1	NP2
M_ODT_B164	280	ODT164	NP1	NP2
M_ODT_B165	281	ODT165	NP1	NP2
M_ODT_B166	282	ODT166	NP1	NP2
M_ODT_B167	283	ODT167	NP1	NP2
M_ODT_B168	284	ODT168	NP1	NP2
M_ODT_B169	285	ODT169	NP1	NP2
M_ODT_B170	286	ODT170	NP1	NP2
M_ODT_B171	287	ODT171	NP1	NP2
M_ODT_B172	288	ODT172	NP1	NP2
M_ODT_B173	289	ODT173	NP1	NP2
M_ODT_B174	290	ODT174	NP1	NP2
M_ODT_B175	291	ODT175	NP1	NP2
M_ODT_B176	292	ODT176	NP1	NP2
M_ODT_B177	293	ODT177	NP1	NP2
M_ODT_B178	294	ODT178	NP1	NP2
M_ODT_B179	295	ODT179	NP1	NP2
M_ODT_B180	296	ODT180	NP1	NP2
M_ODT_B181	297	ODT181	NP1	NP2
M_ODT_B182	298	ODT182	NP1	NP2
M_ODT_B183	299	ODT183	NP1	NP2
M_ODT_B184	300	ODT184	NP1	NP2
M_ODT_B185	301	ODT185	NP1	NP2
M_ODT_B186	302	ODT186	NP1	NP2
M_ODT_B187	303	ODT187	NP1	NP2
M_ODT_B188	304	ODT188		

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Strap Pin

Description	LPC_CLK0	LPC_CLK1	LFRAME_L
GPIO	CK_P_33M_SIO	LPC_CLK1	LFRAMEJ_FW4
Schematic			
	15,24,36 CK_P_33M_SIO	15,68 LPC_CLK1	15,24,36,68 LFRAMEJ_FW4
	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	
PULL HIGH	BOOT FAIL TIMER ENABLED		SPI ROM (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)		LPC ROM

Strap Pin

SB012 Eric modfiy BOM

Description	RTC_CLK Int pull-up	SYS_RST_L	AGPIO3	BLINK
GPIO	SUSCLK_32_APU_C	FP_RST_N	AGPIO3	AGPIO11
Schematic				
	18,61 SUSCLK_32_APU_C	18 FP_RST_N	18 AGPIO3	18 AGPIO11
			SB039	
PULL HIGH	RTC coin Battery is not implemented (DEFAULT)	normal reset mode (DEFAULT)	Enhanced Reset logic (Default) for faster resume from S5	LDT_RST#/LDT_PWRGD output to APU (DEFAULT)
PULL LOW	RTC coin Battery is implemented	short reset mode	Traditional Reset logic (DEFAULT)	LDT_RST#/LDT_PWRGD output to Pads

Table 90. Strapping Options

SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LFRAME_L	ROMTYPE	II	1	0	LPC ROM
				1	SPI ROM (Default)
LPCCLK1	CLKGEN	II	1	0	Reserved
				1	Configured for internal clock-generator (Default)
LPCCLK0	BOOTFAILTIMER	II	0	0	Boot Fail Timer Disabled (Default)

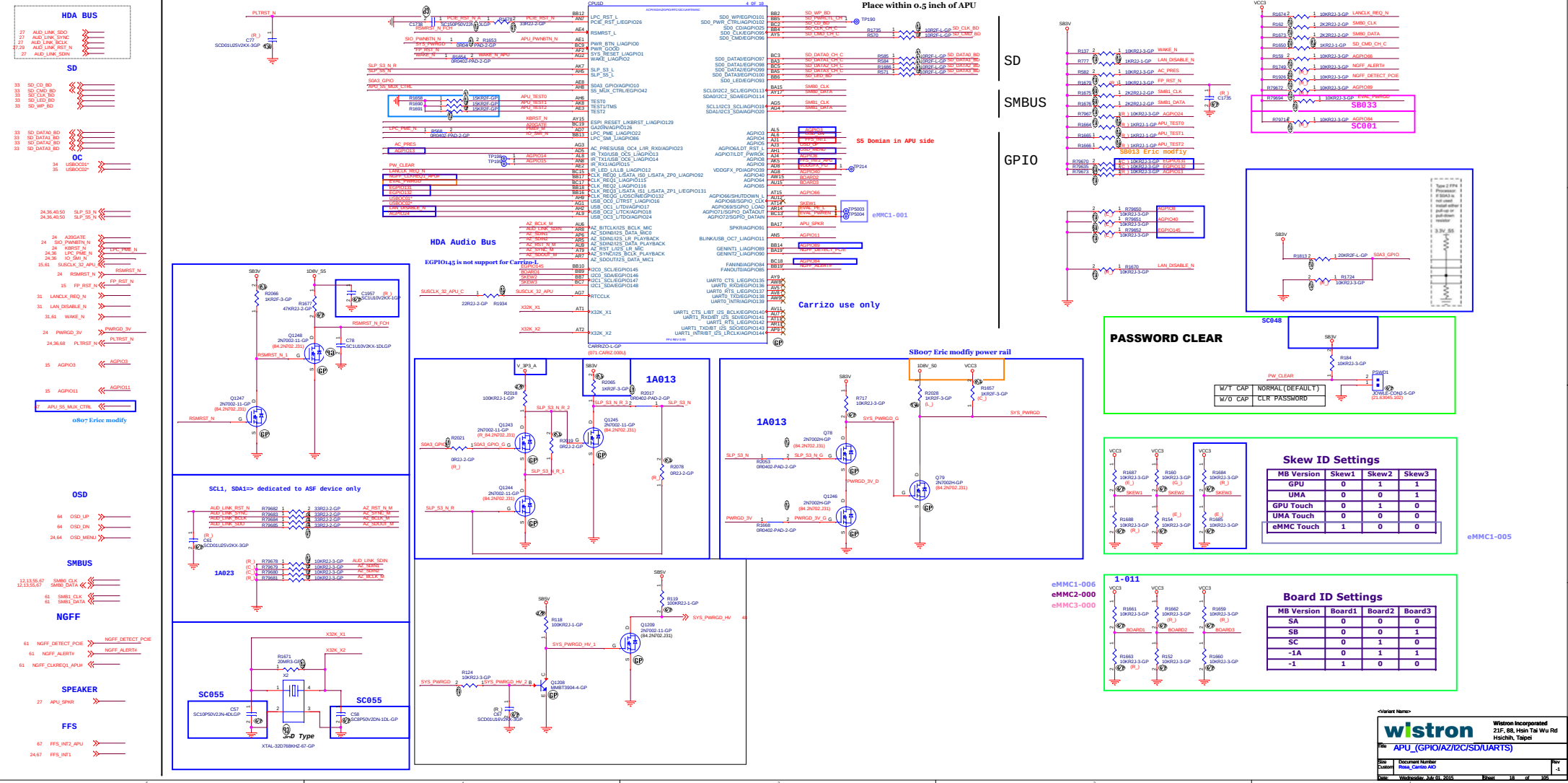
Table 90. Strapping Options (continued)

SIGNAL Name	Strap Name	Type	Default Value	Bit Value	Description
LPCCLK0	BOOTFAILTIMER	II	0	1	Boot Fail Timer Enabled
RTCCCLK	RTC Coin Battery	I	1	0	RTC Coin Battery is not implemented
				1	RTC Coin Battery is implemented (Default)
SYS_RESET_L	ShortReset	I	1	0	Reserved
				1	Normal powerup/reset timing (Default)
AGPIO3	Alternate Reset	I	1	0	Traditional Reset logic (Type 1 FP4 Processor Only) 2 kΩ (± 5%) pull-down resistor to VSS
				1	Enhanced Reset logic (Default) for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5
					Note: - Platforms that are designed for AOAC complaint are recommended to use Alternate Reset - To ensure the strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config value until 20 ms after RsmRstB has risen to at least 3.0 v.

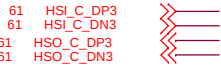
Title	APU_FP4(SATA/USB/LPC/SPI)		
Size	Document Number		Rev
C	Rosa_Carrizo AIO		-
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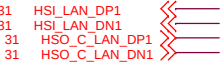
		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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Wireless

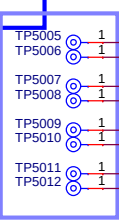


Giga LAN

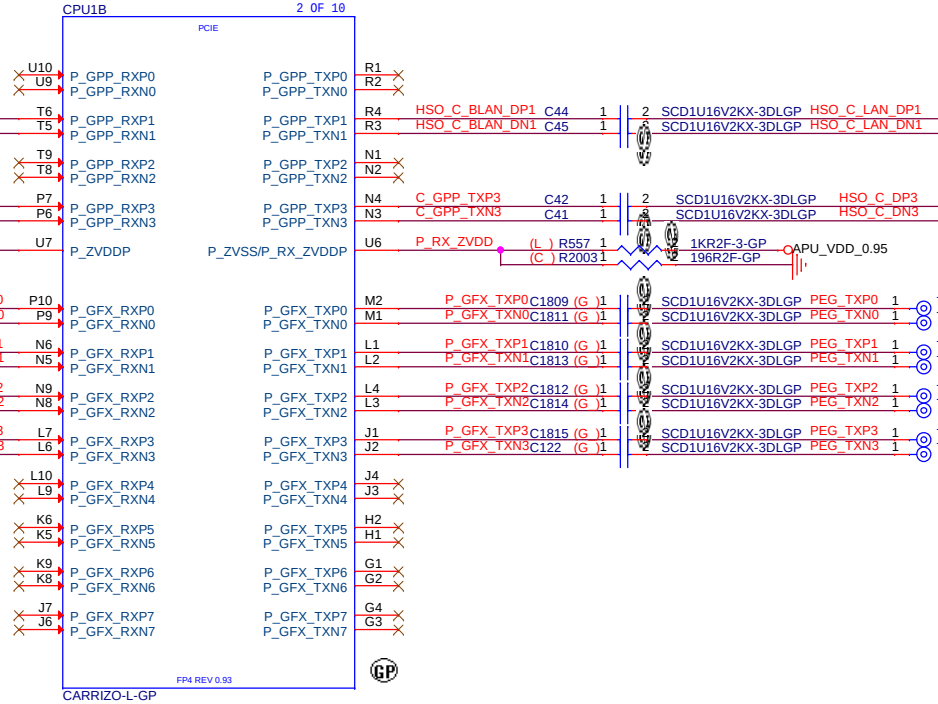


0625 Eric modify

APU_VDD_0.95 1K69R2F-2-GP (C_64.19605.6DL.L)
Type1 Carrizo use 196 ohms
Type2 Carrizo-L use 1.69k ohms



eMMC1-001



Type1 Type2 Type1 Type2

P_ZVDDP	A	Pull-up resistor		196Ω (± 1%)	1.69 kΩ (± 1%)	—	VDDP	
P_ZVSS/ P_RX_ZVDD P	A	Pull-down resistor	Pull-up resistor	196Ω (± 1%)	1 kΩ (± 1%)	—	VSS	VDDP

<Variant Name>



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Hsichih, Taipei

Title 019_APU_FP4(PCIE I/F)

Size B Document Number Rosa_Carrizo AIO Rev -1

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SPI ROM

SPI . ROM

SPI ROM

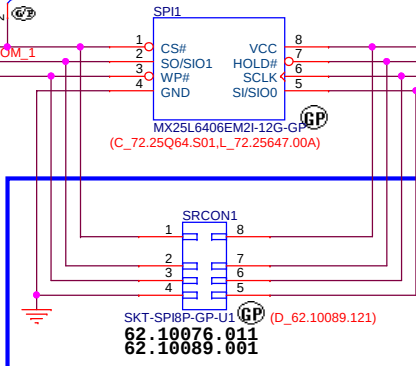
16 SPI_CLK >>>
16 SPI_CS_N >>>
16 SPI_DATAOUT >>>
16 SPI_DATAIN >>>
16 SPI_WP# >>>
16 SST_HOLDJ_1 >>>

SPI_CS_N
SPI_DATAIN R17401 2
SPI_WP# 0R0402-PAD-2-GP

0626 Eric modify 33ohms Res to 0 ohm

WP# function is not supported when
SPI ROM is used on descriptor mode.

SOP8 for 8Mb



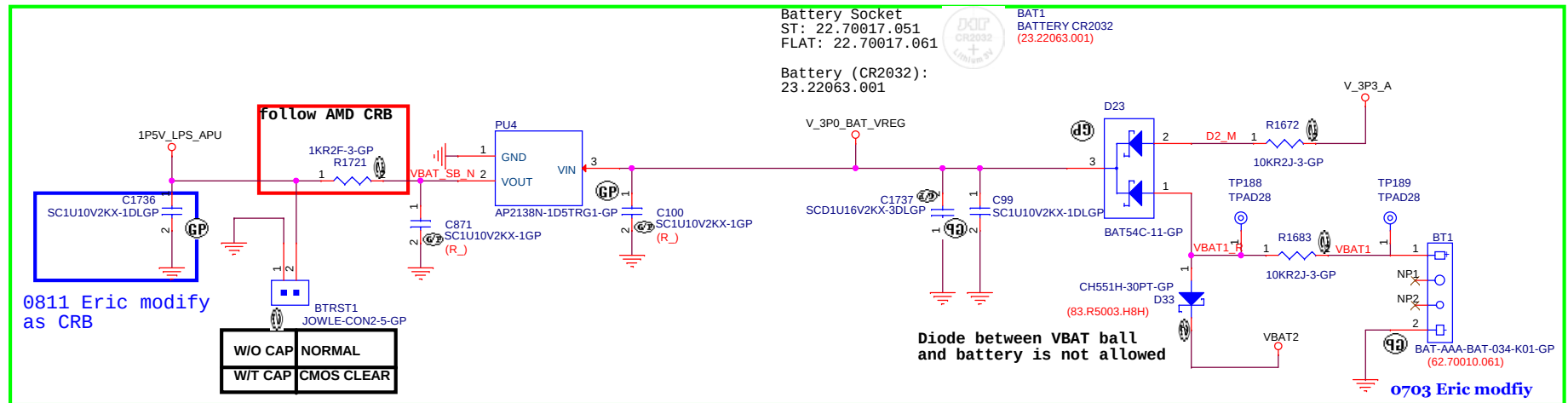
SPI socket mount in SA stage

1A009

SB015 0929 Eric modify
BIOS P/N and socket

SB036 0929 Eric modify socket P/N

RTC



0811 Eric modify
as CRB

W/O CAP	NORMAL
W/T CAP	CMOS CLEAR

Diode between VBAT ball
and battery is not allowed

0703 Eric modify

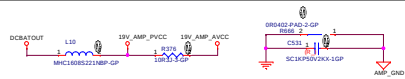
<Variant Name>

wistron
Title 025_Flash ROM/RTC

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Internal Speaker x 2

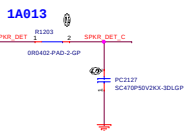
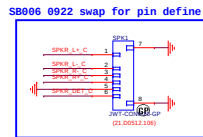
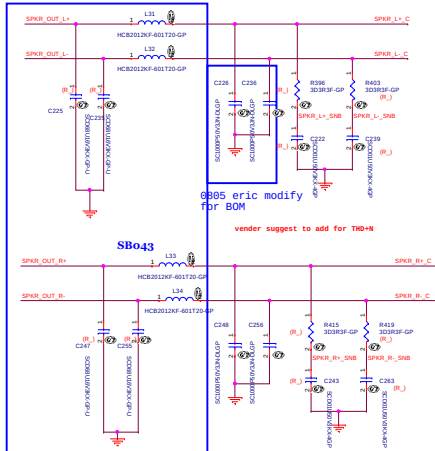


Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 μF	1.8 Hz
26 dB	30 kΩ	3.3 μF	1.8 Hz
32 dB	15 kΩ	5.6 μF	2.3 Hz
36 dB	9 kΩ	10 μF	1.8 Hz

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND) ⁽¹⁾	R2 (to GND) ⁽¹⁾	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

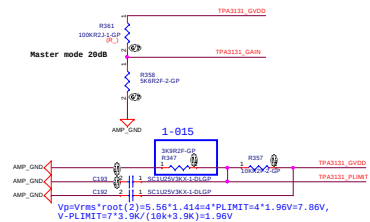
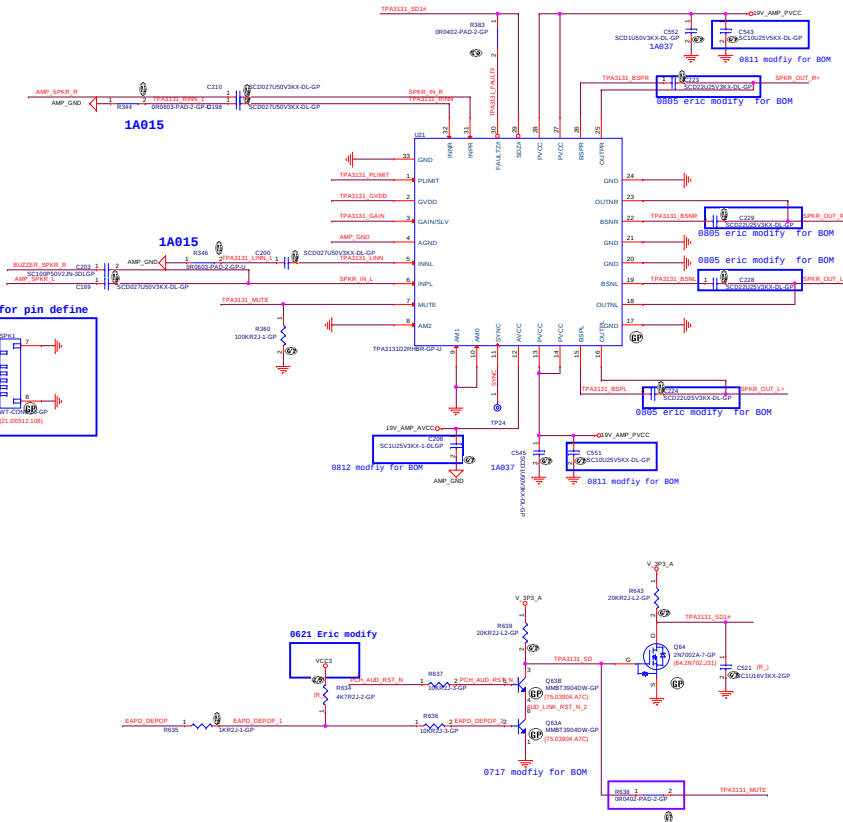
$$P_{OUT} = \left(\frac{R_L}{R_L + 2 \times R_{OUT}} \right)^2 \times V_p^2$$

Where:
 R_L is the total series resistance including R_{OUT} , and output filter resistance.
 R_L is the load resistance.
 V_p is the peak amplitude.
 $V_p = 4 \times PLIMIT$ voltage if $PLIMIT < 4 \times V_p$
 $P_{OUT} (10\%THD) = 1.25 \times P_{OUT} (undistorted)$

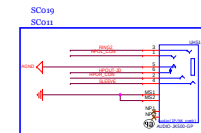
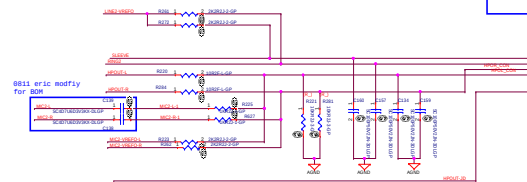
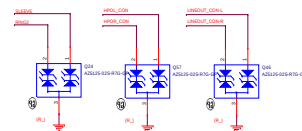
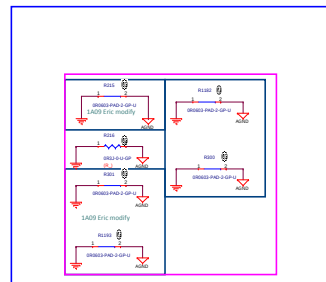
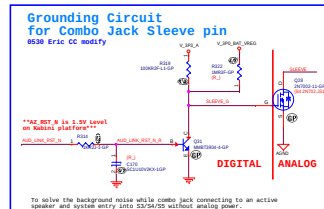
Table 3. POWER LIMIT Example

PLIMIT (V)	PLIMIT VOLTAGE (V ²)	R to GND	R to GND	OUTPUT VOLTAGE (V _{OUT})
24 V	576	50kΩ	50kΩ	17.80
24 V	576	45 kΩ	51 kΩ	12.87
24 V	576	2.2kΩ	24 kΩ	8.90
12 V	144	50kΩ	50kΩ	10.33
12 V	144	2.2kΩ	24 kΩ	9.00
12 V	144	1.5kΩ	18 kΩ	8.30

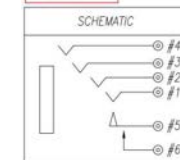
(1) PLIMIT measurements taken with 0VdB gain set to 20dB and input voltage set to 1V_{rms}



0731 Eric modfiy location for layout



```
Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND
```



4-pin 3.5mm Headset Connector Pinout



Nokia, Lenovo mobile		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Microphone
4	Sleeve	Ground / Common

iPhone, Samsung, Blackberry, HTC		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Ground / Common
4	Sleeve	Microphone

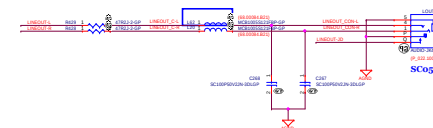
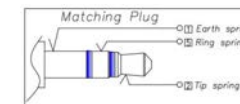


TABLE A: Circuit



	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

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16 CK_GLAN_DP >>>
   CK_GLAN_DN >>>

19 HSI_LAN_DP1 >>>
   HSI_LAN_DN1 >>>
19 HSD_C_LAN_DP1 >>>
   HSD_C_LAN_DN1 >>>

24 PLTRST_LAN_N >>>
   18.61 WAKE_N >>>

18 LAN_DISABLE_N >>>
   18 LANCJK_REQ_N >>>

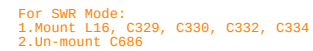
24 EC_LAN_DISABLE_N >>>


32 LAN_MDIO_DP >>>
   LAN_MDQ_DP >>>
   LAN_MDIQ_DP >>>

32 LAN_MDQ_DP >>>
   LAN_MDQ_DP >>>
   LAN_MDQ_DP >>>
   LAN_MDQ_DP >>>
   LAN_MDQ_DP >>>

32 LINK_ACTIVITY_N >>>
   SPEED_100_N >>>
   SPEED_1000_N >>>

```



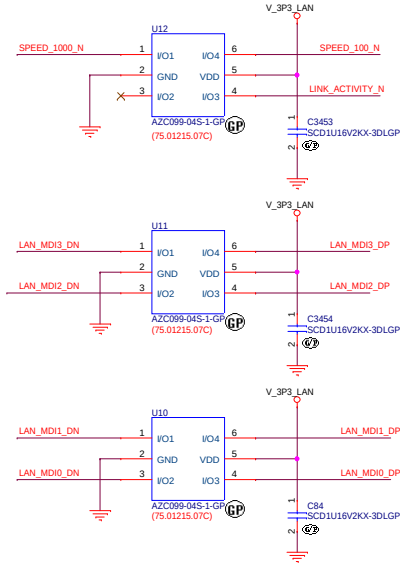
For LDO Mode:

1. Reserve C351 0.1u cap on LAN_1P05_OUT
2. Use 0 ohm resistor to connect LAN_1P05_OUT and V_1P05_LAN
3. Un-mount C686



31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LINK_ACTIVITY_N
31 SPEED_100_N
31 SPEED_1000_N

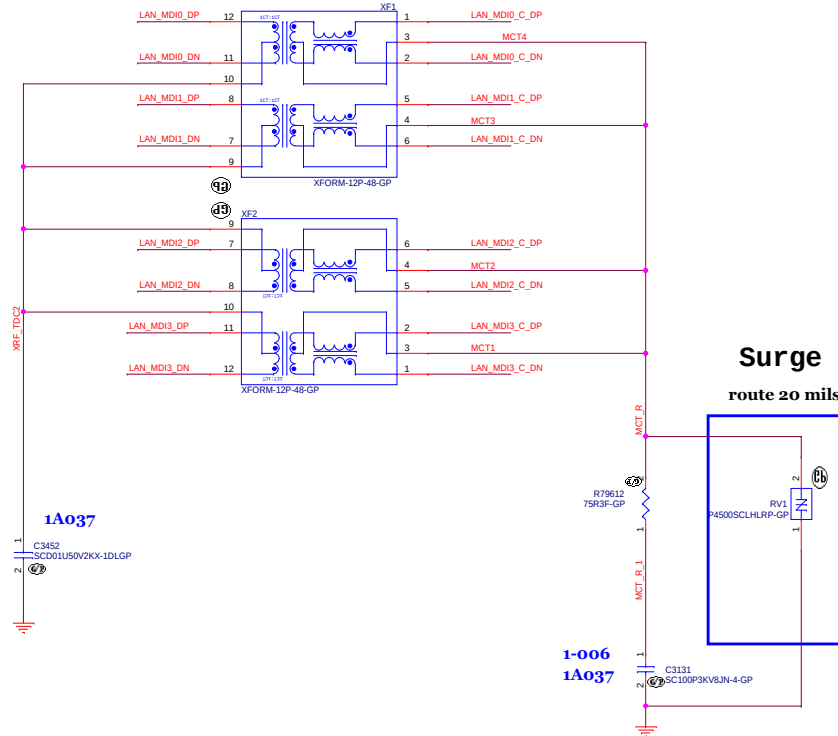
ESD



For LAN differential signal :



Transformer

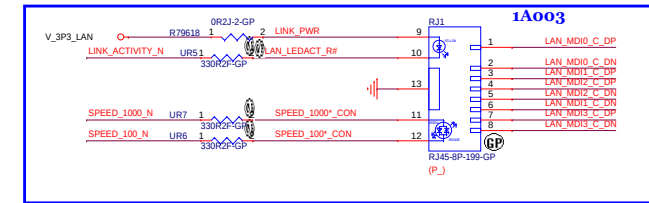


Surge
route 20 mils

SC053
SC018

	Giga	100	10
Link	Orange	Green	Green
Act	Yellow	Yellow	Yellow
	Blink	Blink	Blink

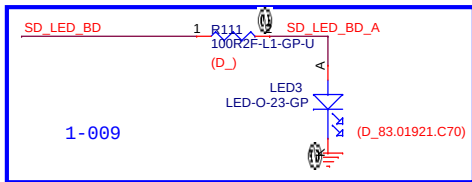
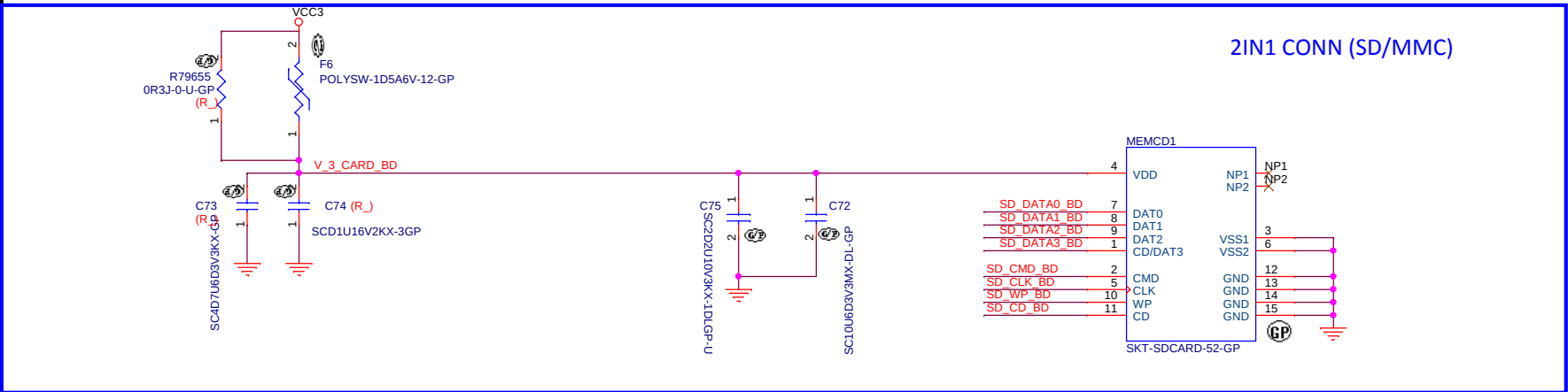
RJ45



6 LED LAYOUT	7 LED LAYOUT														
<table border="1"> <tr> <th>NODE</th><th>COLOR</th></tr> <tr> <td>9(+)</td><td>10(-)</td></tr> <tr> <td>10(+)</td><td>YELLOW</td></tr> </table>	NODE	COLOR	9(+)	10(-)	10(+)	YELLOW	<table border="1"> <tr> <th>NODE</th><th>COLOR</th></tr> <tr> <td>11(+)</td><td>12(-)</td></tr> <tr> <td>11(-)</td><td>12(+)</td></tr> <tr> <td>12(+)</td><td>ORANGE</td></tr> </table>	NODE	COLOR	11(+)	12(-)	11(-)	12(+)	12(+)	ORANGE
NODE	COLOR														
9(+)	10(-)														
10(+)	YELLOW														
NODE	COLOR														
11(+)	12(-)														
11(-)	12(+)														
12(+)	ORANGE														

CAER READER

18 SD_DATA0_BD
18 SD_DATA1_BD
18 SD_DATA2_BD
18 SD_DATA3_BD
18 SD_CD_BD
18 SD_CMD_BD
18 SD_CLK_BD
18 SD_LED_BD
18 SD_WP_BD



<Variant Name>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title 033_CardReader Conn

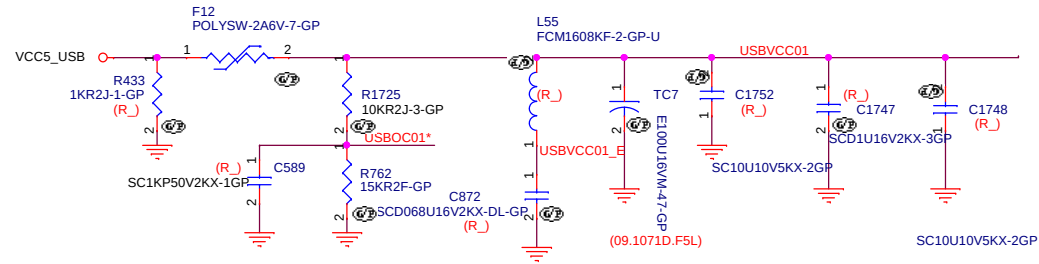
Size	Document Number	Rev
B	Rosa_Carizo AIO	-1

Date: Wednesday, July 01, 2015 Sheet 33 of 105

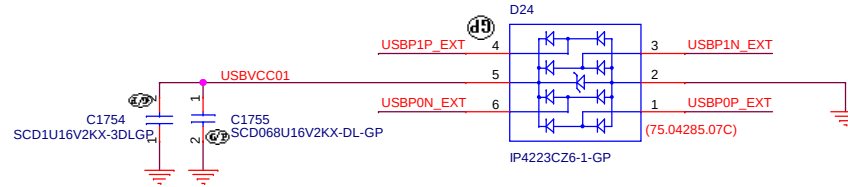
USB



USB_Power . . .Rear

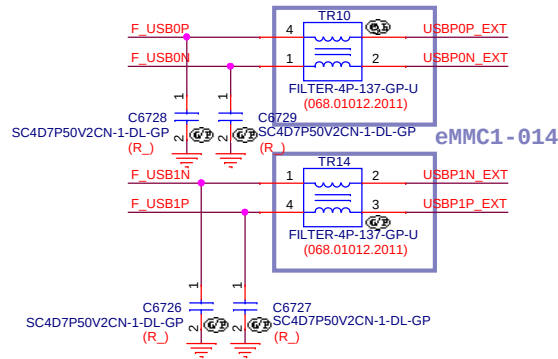


ESD

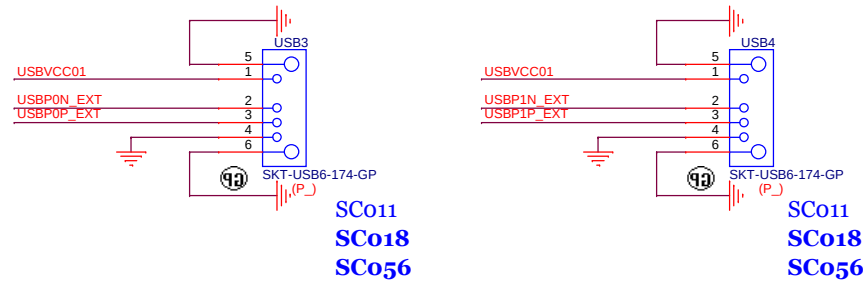


EMI

1-017



Rear USB1



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

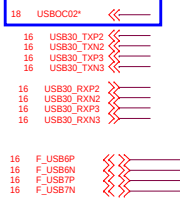
Title **034_USB2.0 CONN**

Size B Document Number
Rosa_Carizo AIO

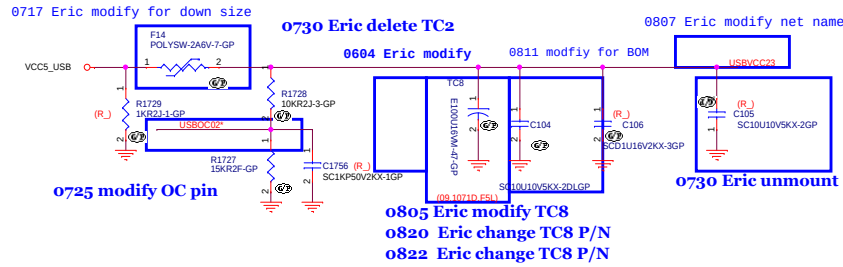
Rev
-1

Date: Wednesday, July 01, 2015 Sheet 34 of 105

USB 3.0

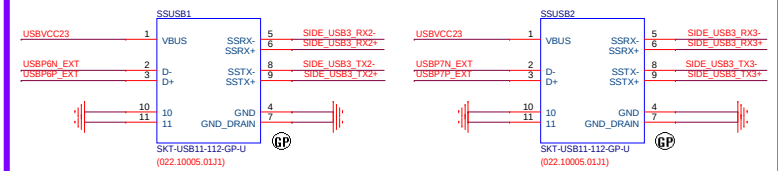


USB_Power...Side1

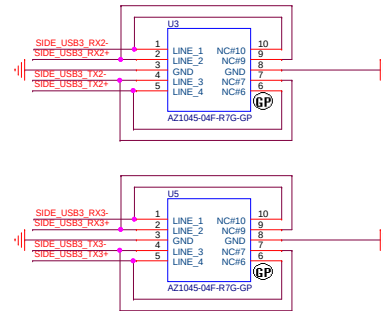
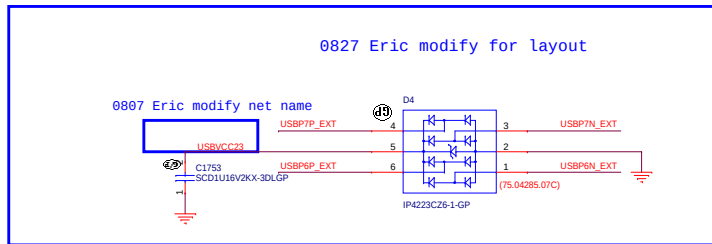


SC058

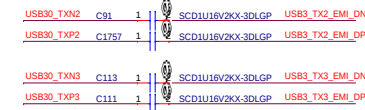
Side USB 3.0



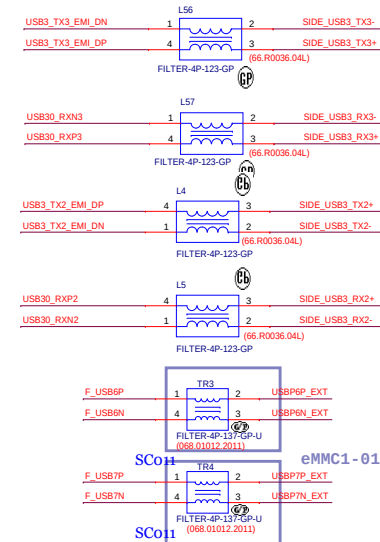
ESD

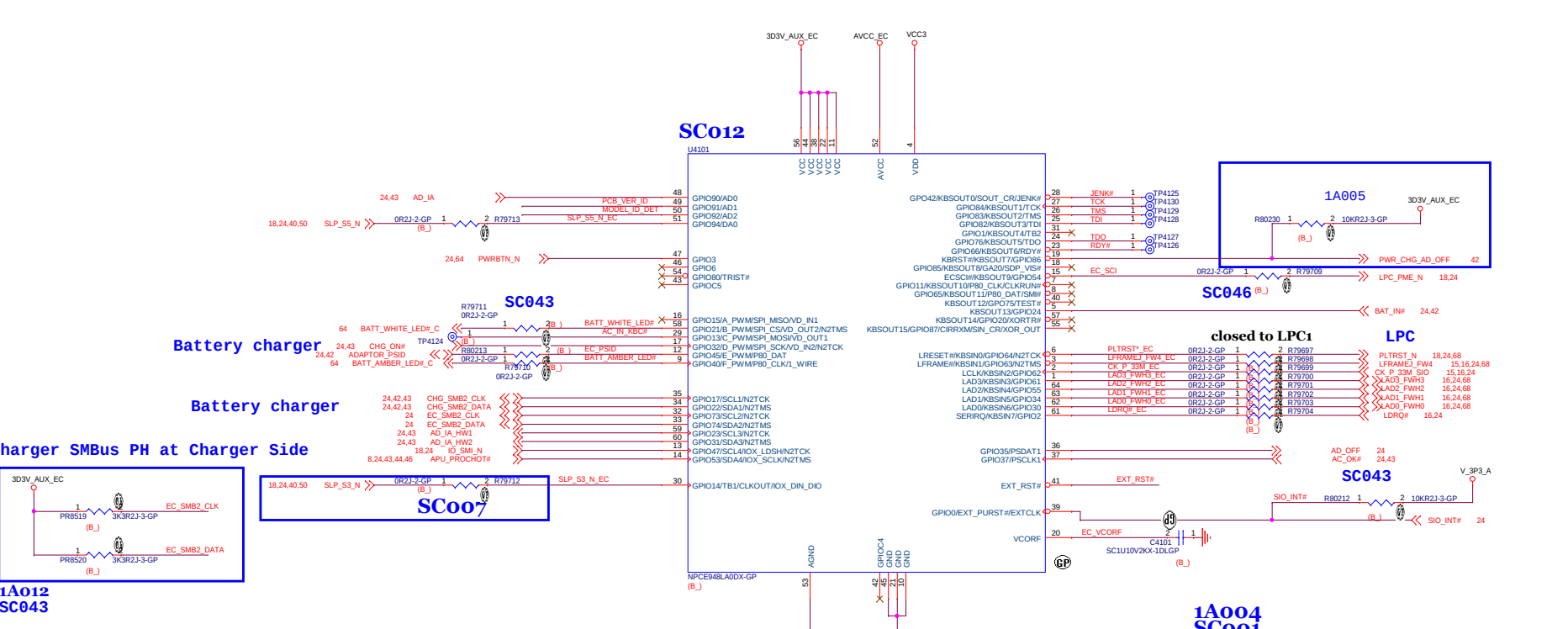


EMI

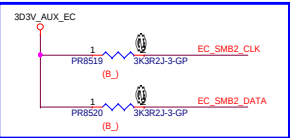


EMI



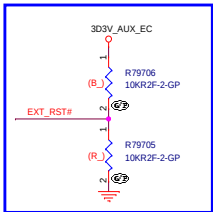
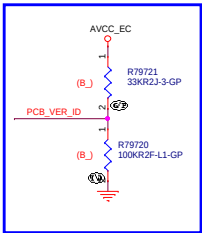
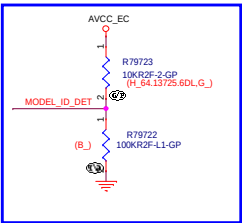


Charger SMBus PH at Charger Side



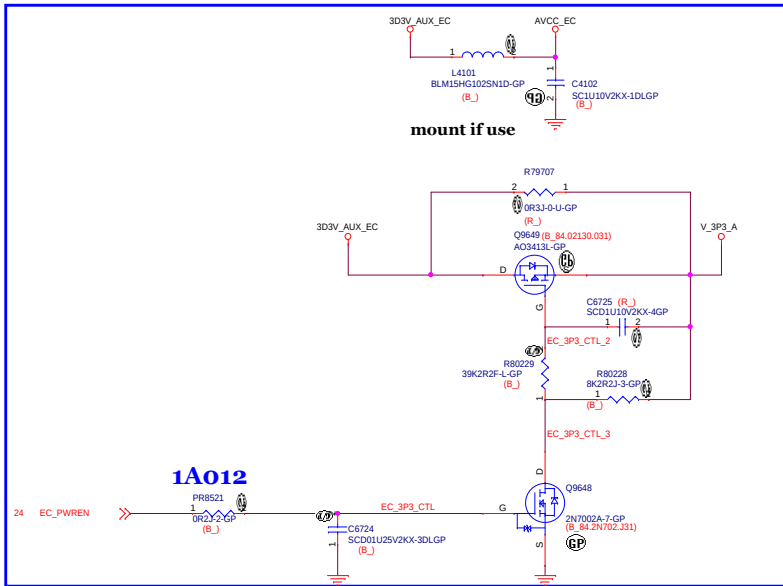
1A012
SC043

SC003
SC008



PCB_VER_AU	Pull-Low Register	Pull-High Register	Typical Voltage
SA	100.0 K	10.0 K	3.000 V
SB	100.0 K	20.0 K	2.750 V
SC	100.0 K	33.0 K	2.481 V
-1	100.0 K	47.0 K	2.245 V

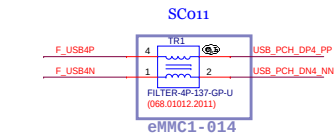
MODEL_ID_DET	Pull-Low Register	Pull-High Register	Typical Voltage
Carrizo GPU	100.0 K	10.0 K	3.000 V
Carrizo UMA	100.0 K	13.7 K	2.902 V
Braswell GPU	100.0 K	57.6 K	2.094 V
Braswell UMA	100.0 K	64.9 K	2.001 V
SKL-U GPU	100.0 K	154.0 K	1.299 V
SKL-U UMA	100.0 K	200.0 K	1.100 V



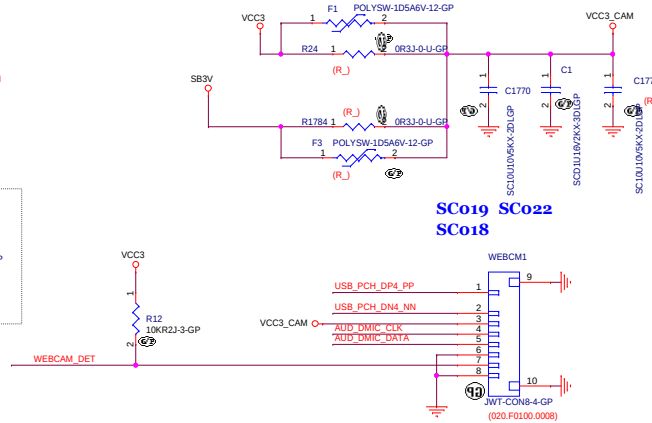
WEBCAM



WEBCAM



FOR EMI



<Variant Name>

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File: **038_WEBCAM**

Size	Document Number	Rev
C	Rosa_Carizo AIO	-1

Date: Wednesday, July 01, 2015 Sheet 38 of 106

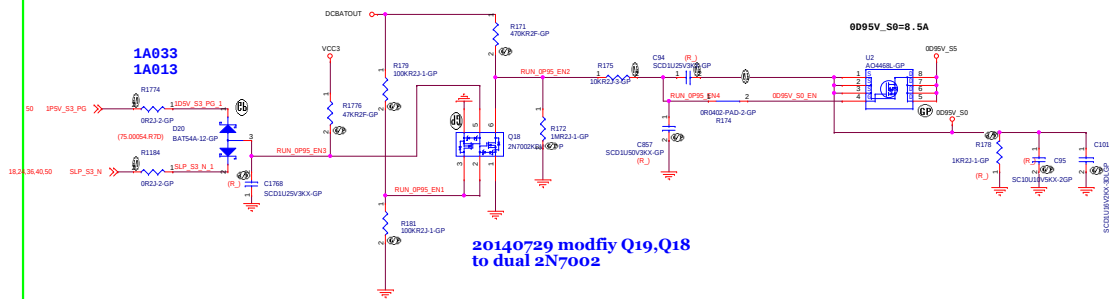
	5	4	3	2	1
D					D
C					C
B					B
A				<Variant Name> wistron Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei Title Card Reader Size A Document Number Rosa_Carrizo AIO Rev -1 Date: Wednesday, July 01, 2015 Sheet 39 of 105	A
	5	4	3	2	1

Run Power(0.95_S5->0.95_S0)

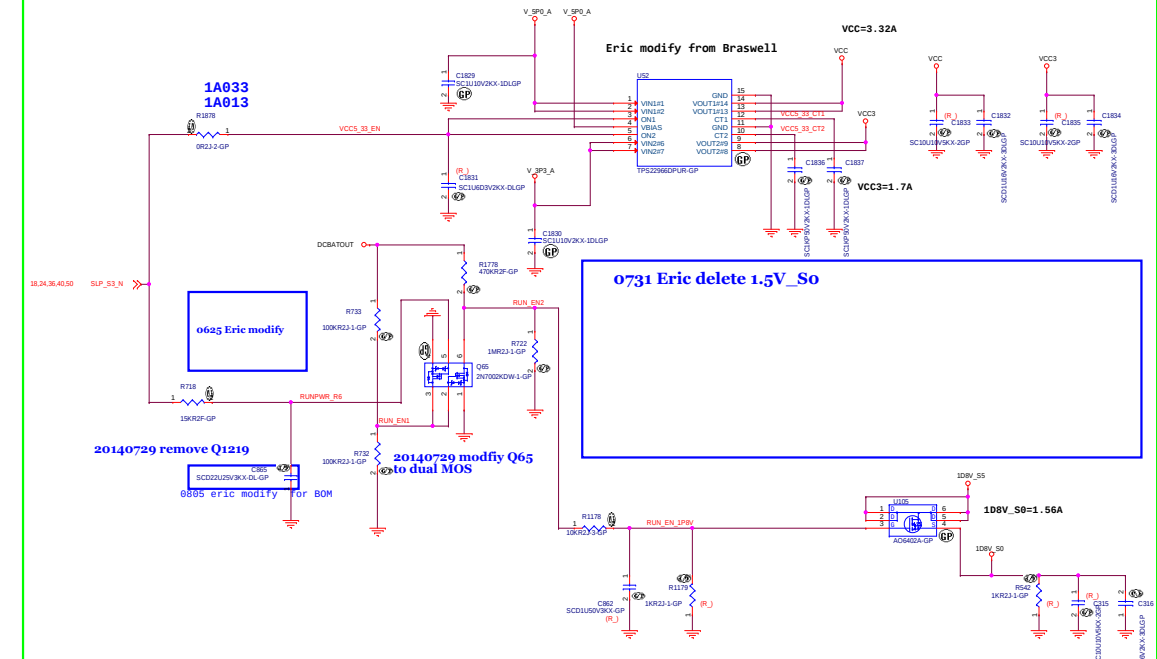
**1A033
1A013**

0.05V_S8=8.5A

20140729 modify Q19,Q18 to dual 2N7002



20140729 modify Q19,Q18
to dual 2N7002

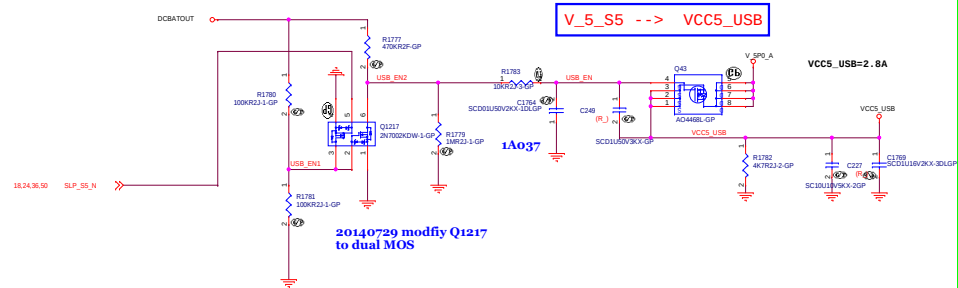
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Run Power(5V_S5->VCC USB)

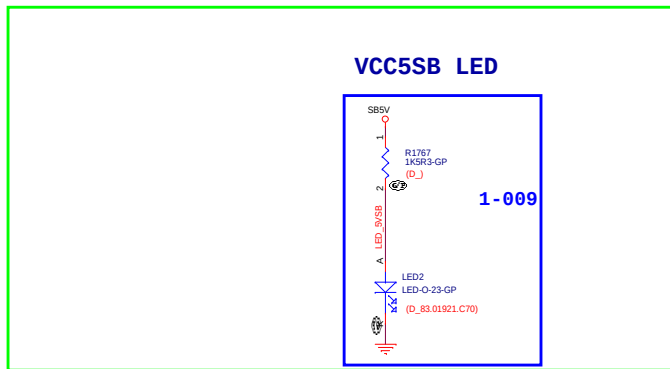
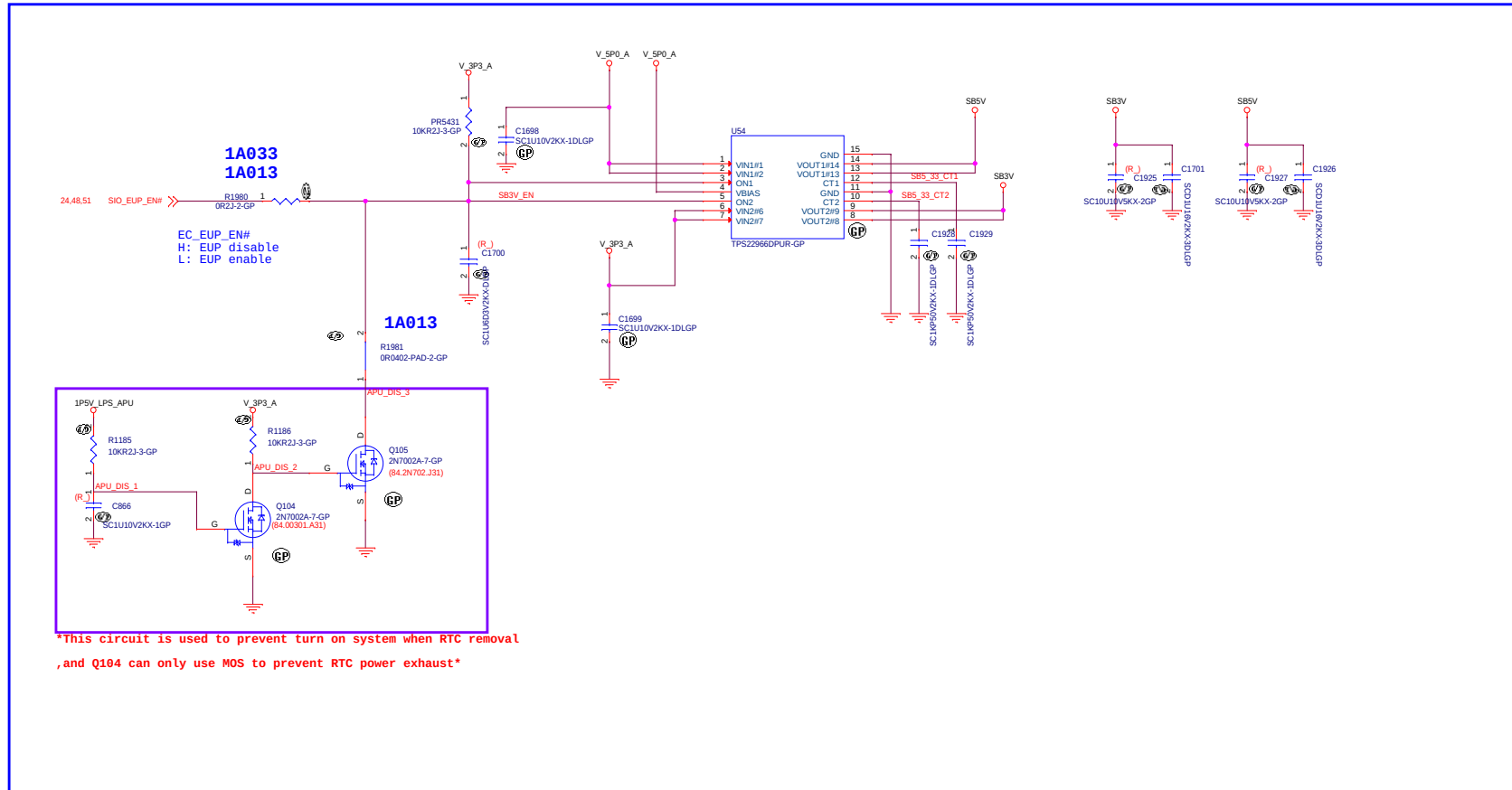
1A037

20140729 modify Q1217 to dual MOS

VCC5_USB=2.8A



0618 Eric modfiy from Braswell EUP Power



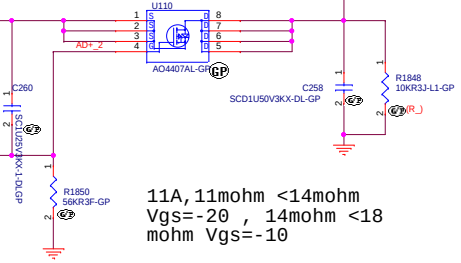
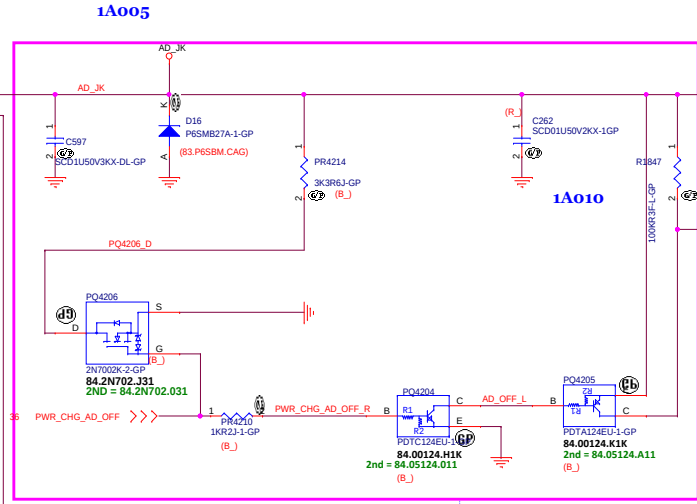
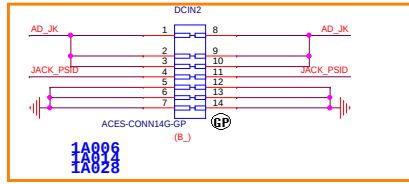
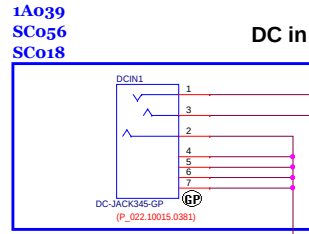
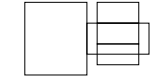
DCIN

Adaptor in to generate DCBATOUT

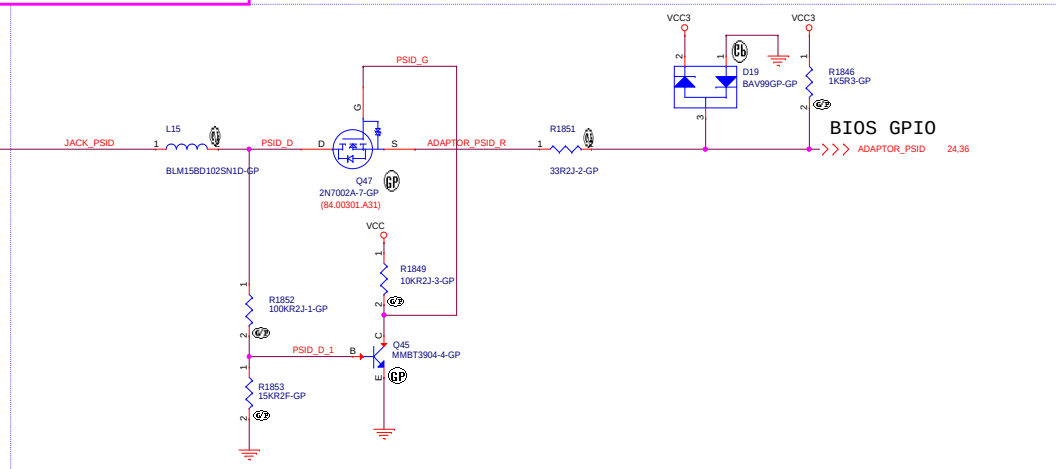
For layout top and bottom the same
U33

R981 R982 R983

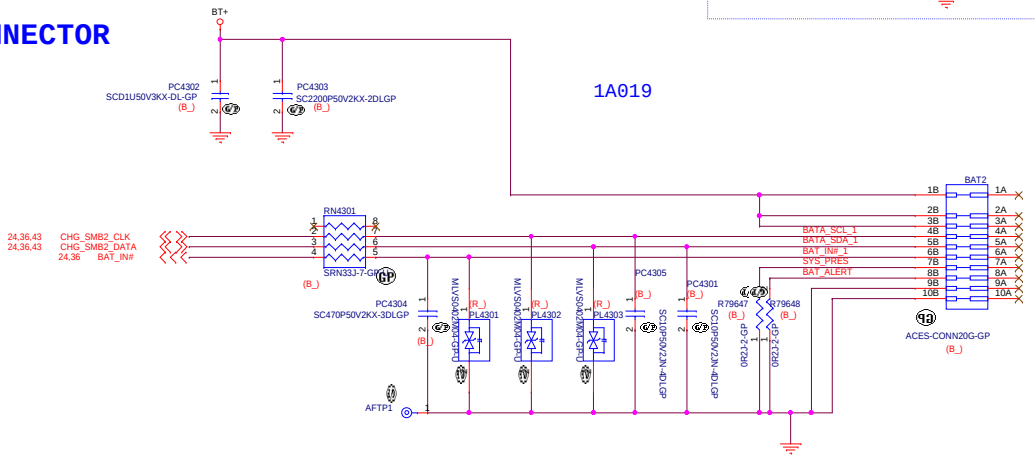
R1718



11A, 11mohm < 14mohm
Vgs = -20, 14mohm < 18
mohm Vgs = -10



BATTERY CONNECTOR



1A019

SB021 Eric delete 2 short pads

SB032 20141001

SB053

Note: PC4421 place closed PU4401 pin4.

Using 0603 0 OHM for PRE_SDV.

Charger Current=1.4~3.6A

PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

wistron

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Hsinchu, Taipei

Title 043_CHARGER

Size Document Number
Customer Rosa_Canizo AIO

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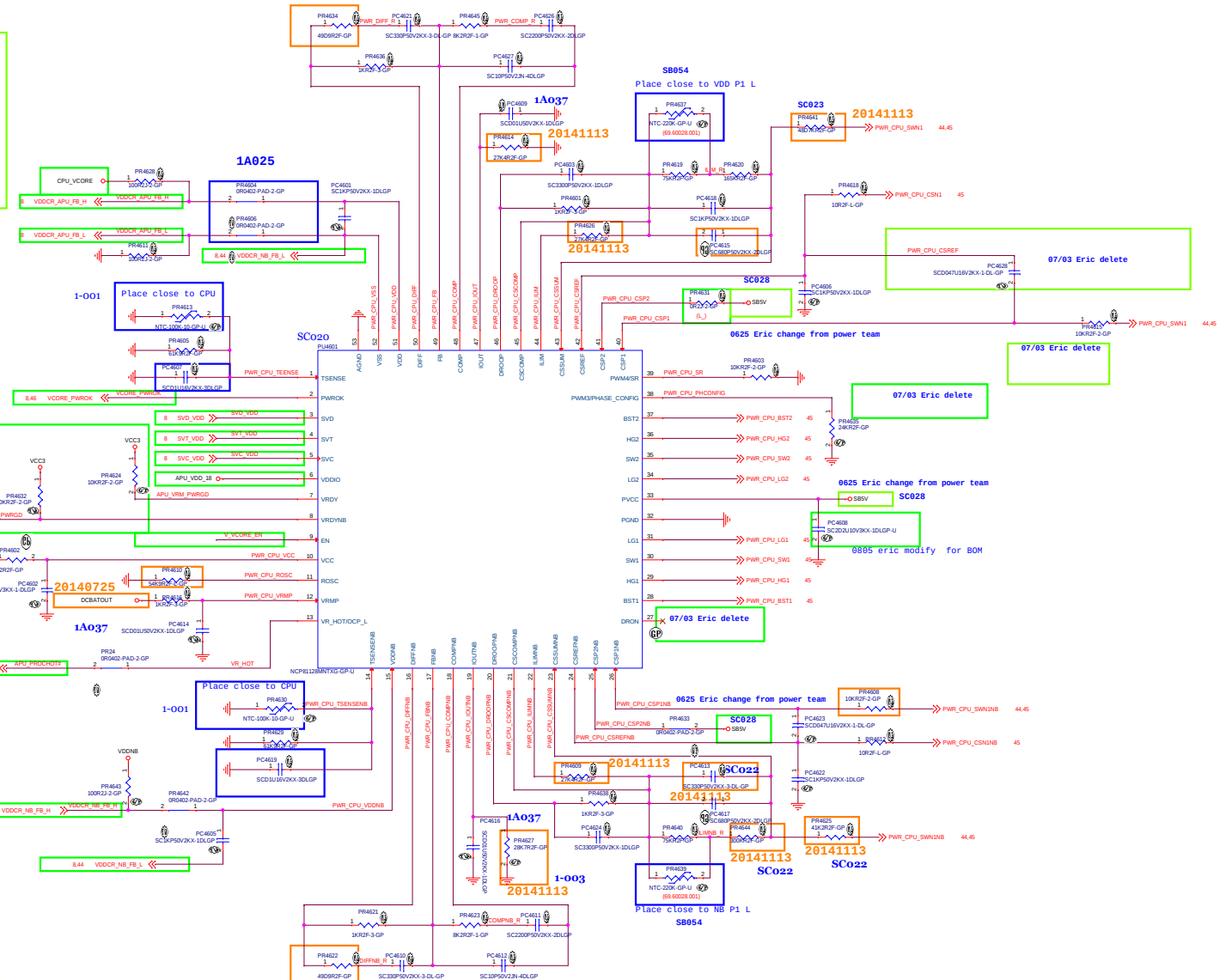
Rev
-1

power team
EE

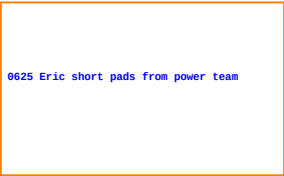
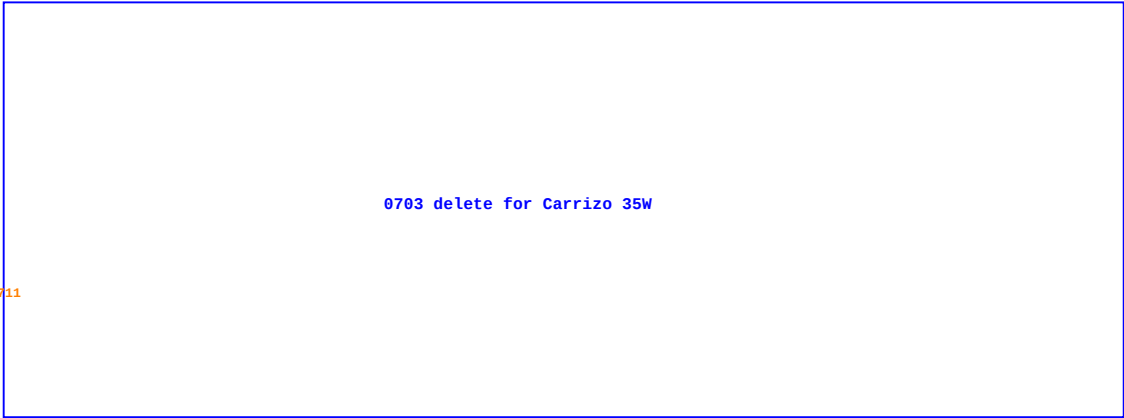
DCBATOUT--> CPU_VCORE

SVC	SVD	BOOT VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

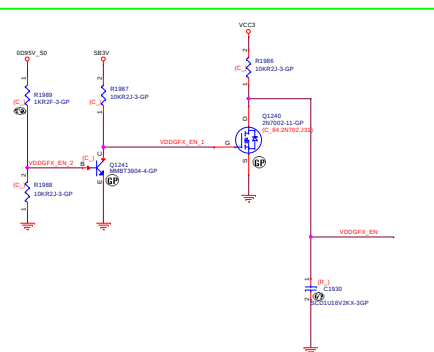
Config	Resistor value	Main Rail		North Bridge Rail	
		Phase 1	Phase 2	Phase 1	Phase 2
1	220k-eyes	SW1.H01.B0T.L01	SW2.H02.B0T.L02	PWM0	PWM4
2	100k	PWM0	SW1.H01.B0T.L01	PWM4	SW2.H02.B0T.L02
3	75k	PWM0	PWM4	SW1.H01.B0T.L01	SW2.H02.B0T.L02
4	24k	SW1.H01.B0T.L01	PWM0	SW2.H02.B0T.L02	PWM4



 power team
 EE

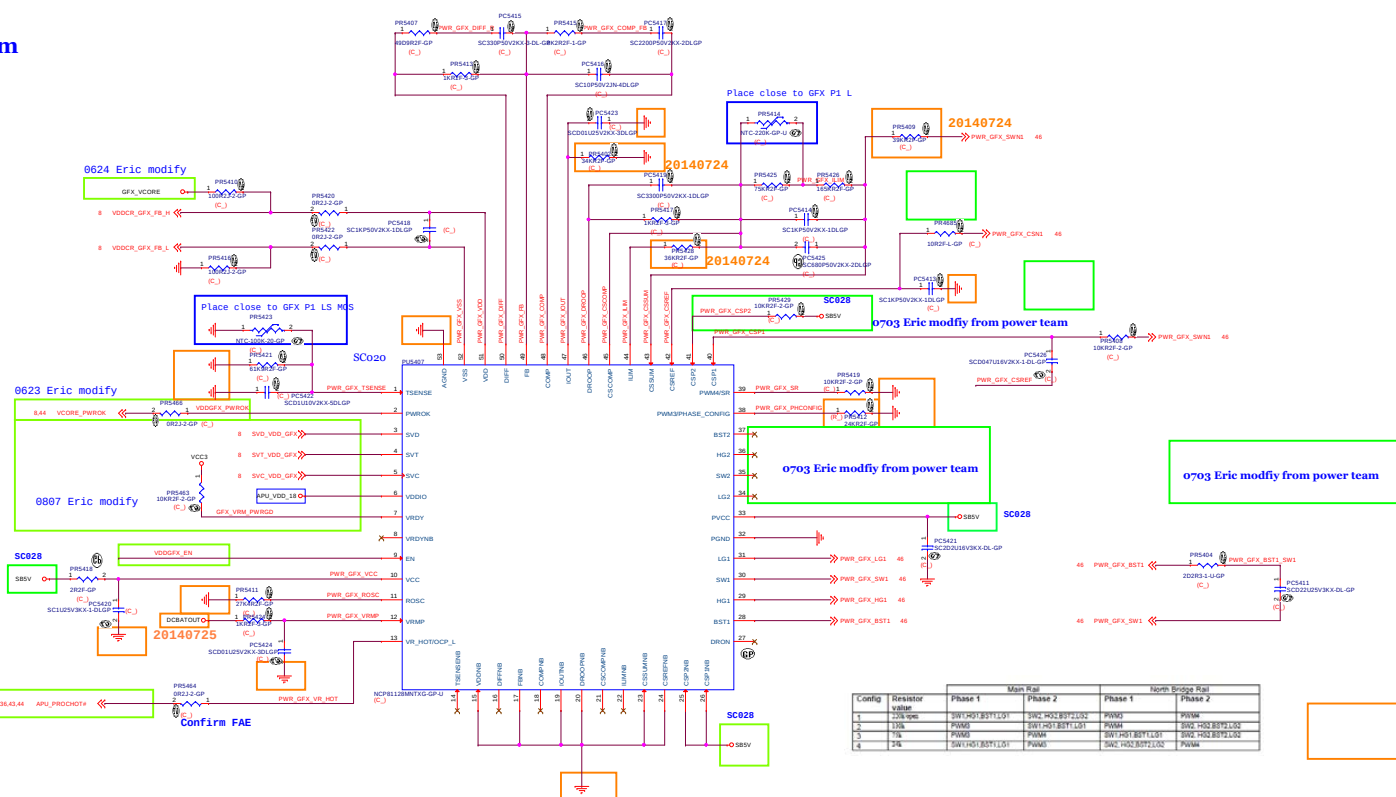


- power team
- EE



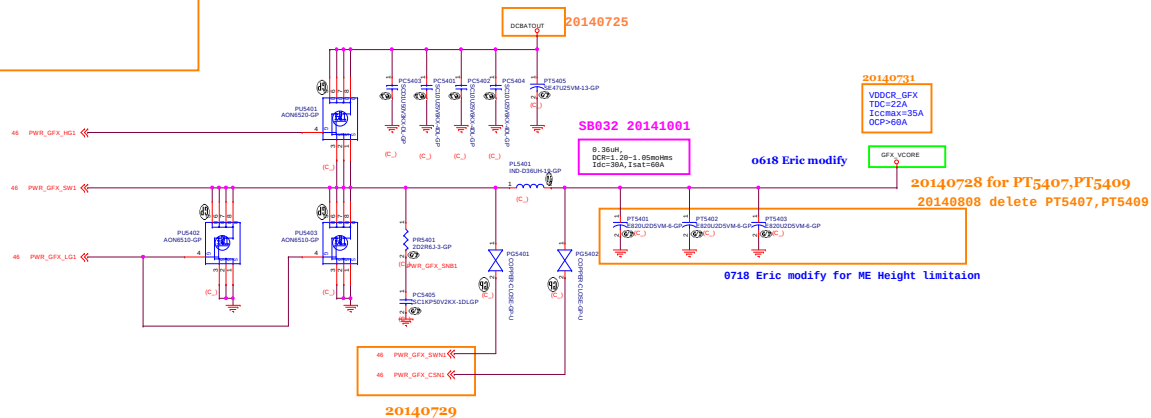
0618 Eric modify

20140725



Config	Resistor value	Main Rail		North Bridge Rail	
		Phase 1	Phase 2	Phase 1	Phase 2
1	2.0k open	SW1.H01.B0Y1.L01	SW2.H02.B0Y2.L02	PWM0	PWM
2	10k	PWM0	SW1.H01.B0Y1.L01	PWM0	SW2.H02.B0Y2.L02
3	1k	PWM0	PWM0	SW1.H01.B0Y1.L01	SW2.H02.B0Y2.L02
		SW1.H01.B0Y1.L01	PWM0	SW1.H01.B0Y1.L01	PWM0

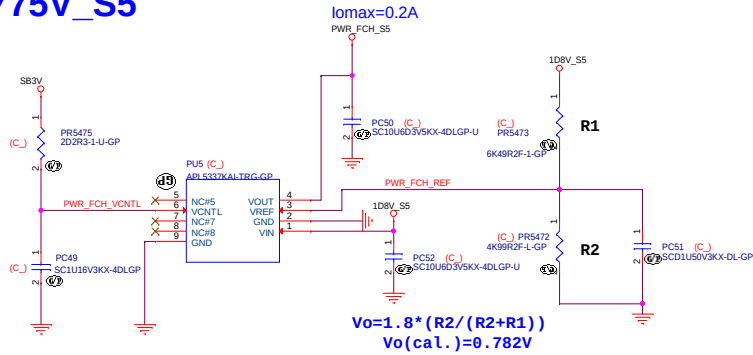
0625 Eric delete short pads



V_1P8_S5 --> V_0P775_S5

o807 Eric modify

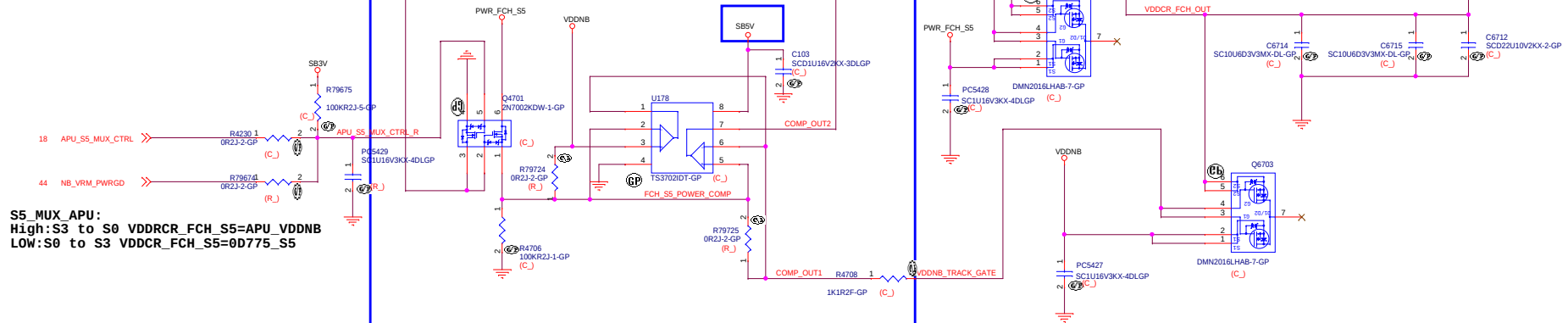
0.775V_S5



VDDCR_FCH_ALW

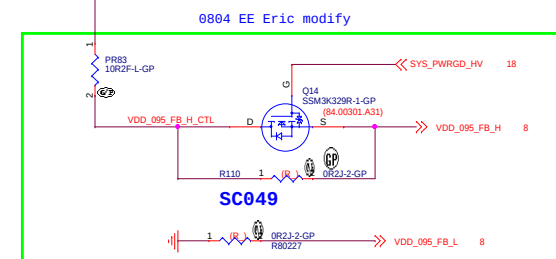
SC005

SC029



power team
EE

$$\begin{aligned} V_{out} &= 0.704 * (1 + R_1/R_2) \\ &= 0.704 * (1 + 11.8/33) \\ &= 0.9557V \end{aligned}$$

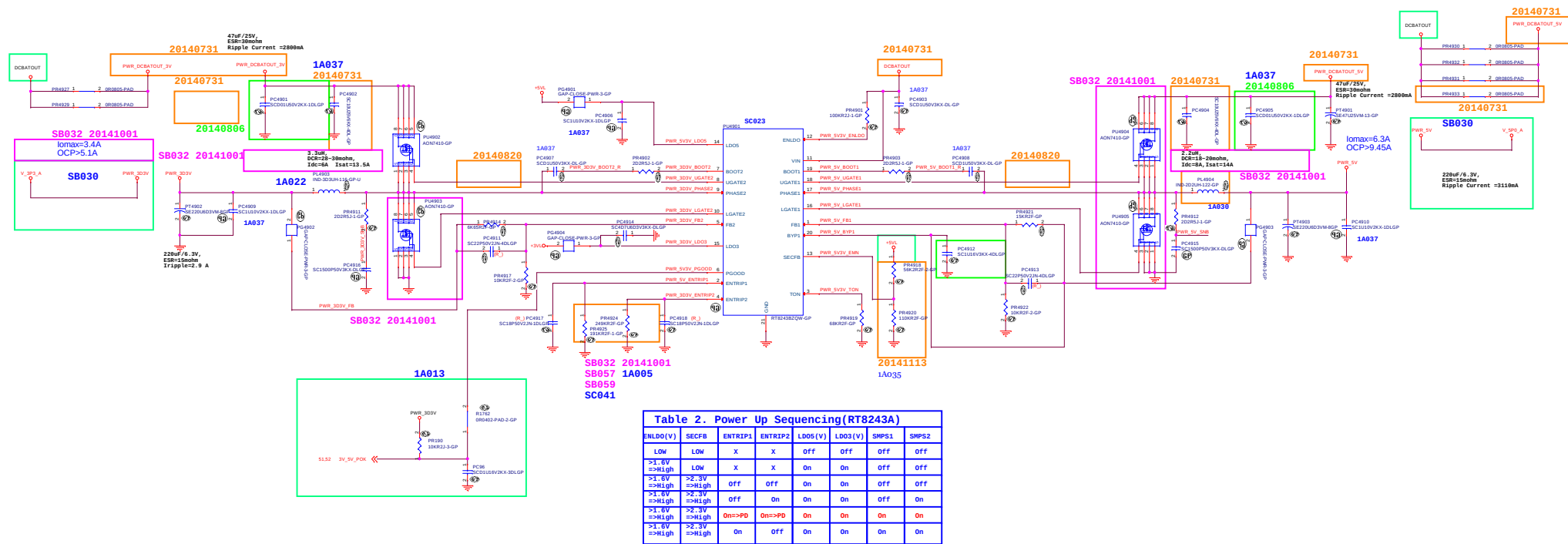


05/26 Eric modify from power team

- power team
- EE

DCBATOUT--> V_3P3_A

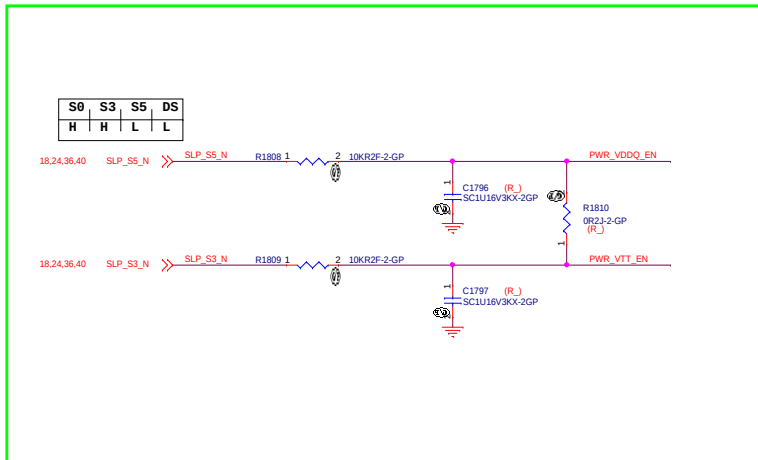
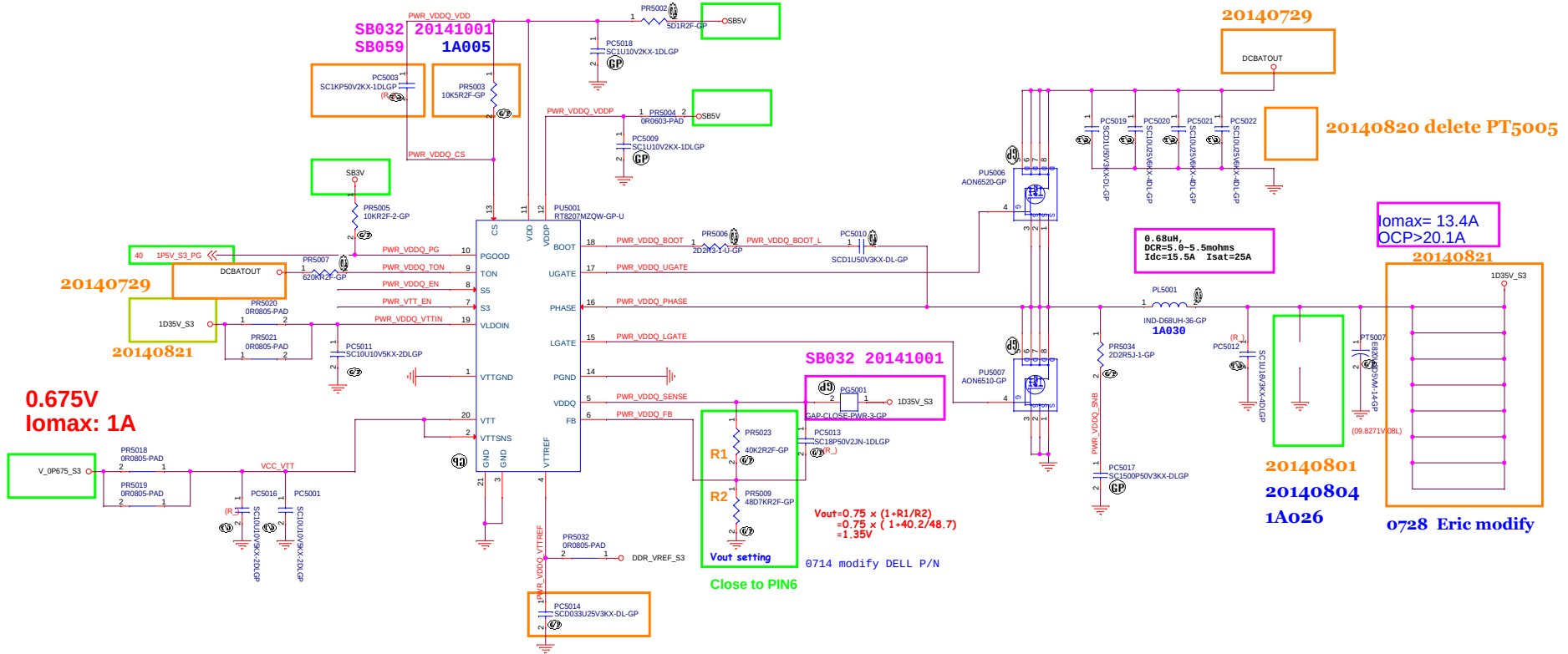
DCBATOUT--> V_5P0_A



05/26 Eric modify from power team

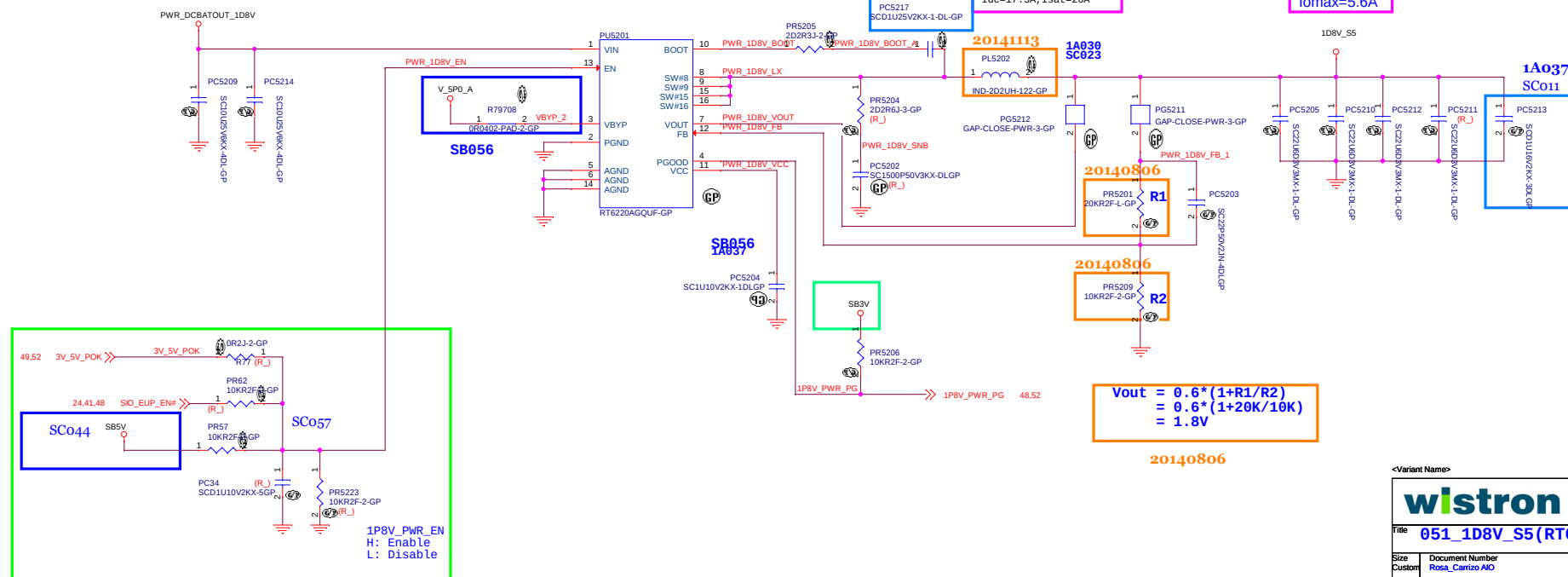
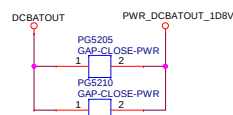
DCBATOUT--> V_1P35_S3

power team
EE

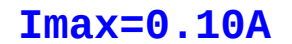


power team
EE

1D8V



Iomax=0.1A



<Variant Name>



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Hsichih, Taipei

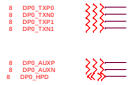
Title	TBD
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Size C	Document Number Rosa_Carrizo AIO
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Rev	
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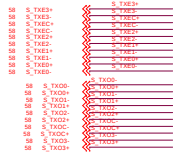
APU DP to RTD2136S



SMBus



TO LVDS CN



From SIO



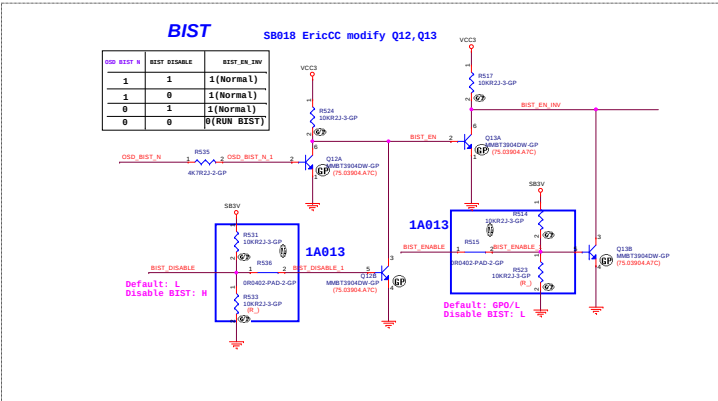
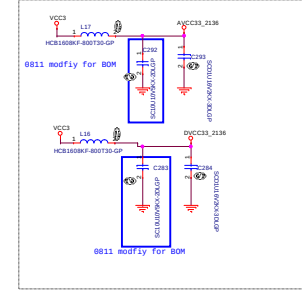
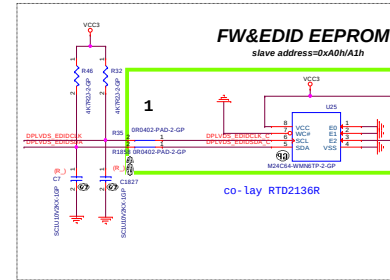
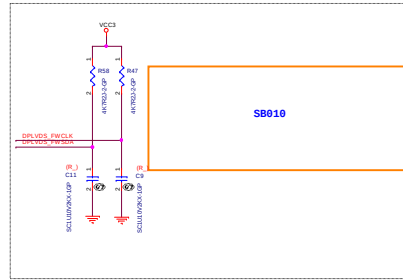
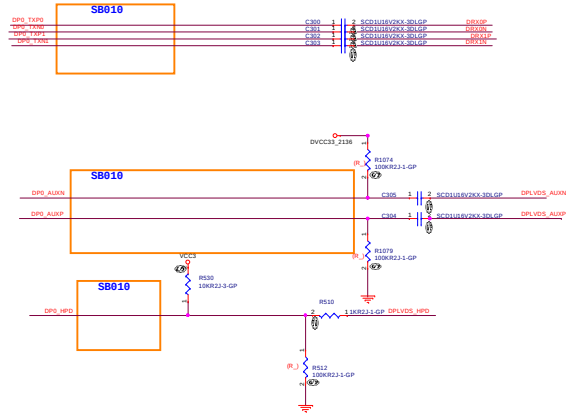
From OSD BTN



From APU



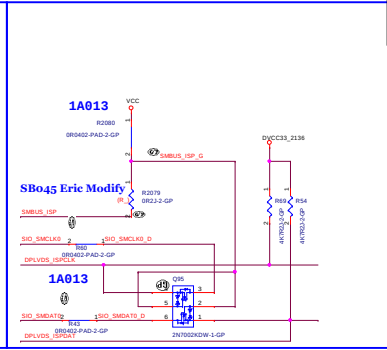
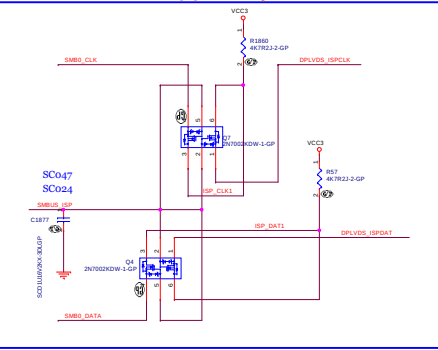
To SIO



SMBUS_ISP H : Simultaneous Mode
SMBUS_ISP L : Isolate Mode
Firmware update by SMBUS

ISP Programming

slave address=0x94h/95h



co-lay RTD2136R notice
1. unmount: R591, R598, U23
mount: R667, R668, U41
2. change to 2.2uH(68.2R21F.10E)
3. change to 10uF(78.10623.51L)

Dual Mode Regulator Configuration

2.2-uH(L47)	0 ohm(L47)
SWR	Connect
LDO	NC
	Connect

Mode Configure Table(Power On Latch)

From RTD2136S to LVDS

55	S_TXE3+	S_TXE3+
55	S_TXE3-	S_TXE3-
55	S_TXE2+	S_TXE2+
55	S_TXE2-	S_TXE2-
55	S_TXE1+	S_TXE1+
55	S_TXE1-	S_TXE1-
55	S_TXE0+	S_TXE0+
55	S_TXE0-	S_TXE0-
55	S_TXD3+	S_TXD3+
55	S_TXD3-	S_TXD3-
55	S_TXD2+	S_TXD2+
55	S_TXD2-	S_TXD2-
55	S_TXD1+	S_TXD1+
55	S_TXD1-	S_TXD1-
55	S_TXD0+	S_TXD0+
55	S_TXD0-	S_TXD0-

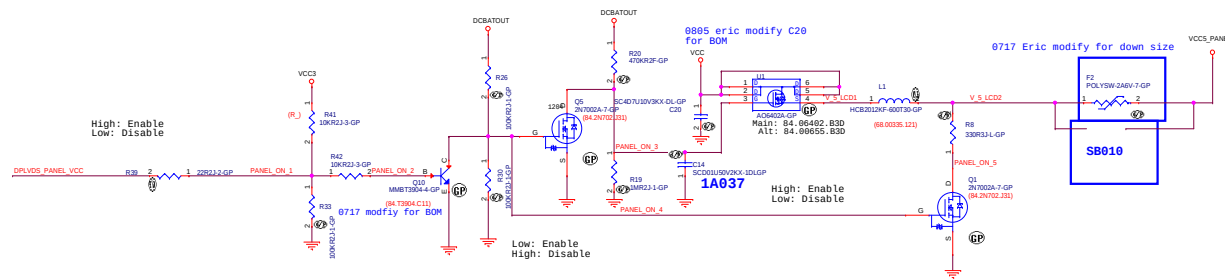
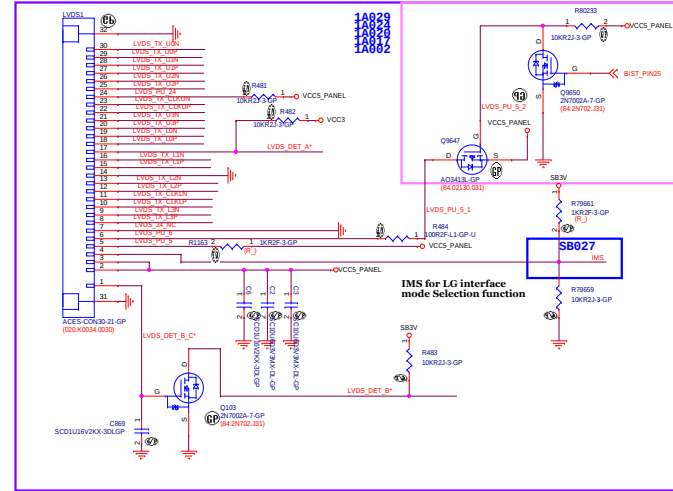
GPIO

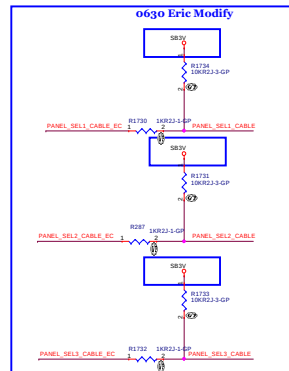
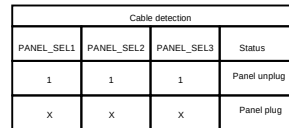
24	LVDS_DET_A*	
24	LVDS_DET_B*	
15	DPLVDS_PANEL_VCC	DPLVDS_PANEL_VCC
24	IMS	IMS

From RTD2136R 0716 Eric modify

S_TXD0+	LVDS_TX_USP
S_TXD0-	LVDS_TX_USM
S_TXD1+	LVDS_TX_USP
S_TXD1-	LVDS_TX_USM
S_TXD2+	LVDS_TX_USP
S_TXD2-	LVDS_TX_USM
S_TXD3+	LVDS_TX_USP
S_TXD3-	LVDS_TX_USM
S_TXD0+	LVDS_TX_USP
S_TXD0-	LVDS_TX_USM
S_TXE1+	LVDS_TX_LSP
S_TXE1-	LVDS_TX_LSM
S_TXE2+	LVDS_TX_LSP
S_TXE2-	LVDS_TX_LSM
S_TXE3+	LVDS_TX_LSP
S_TXE3-	LVDS_TX_LSM
S_TXE0+	LVDS_TX_USP
S_TXE0-	LVDS_TX_USM

SB001 0916 swap for pin define
SB009 0925 change LVDS connector
SB022 0930 change LVDS connector

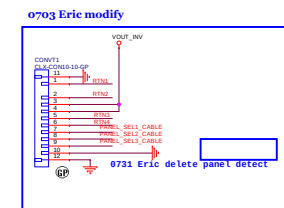
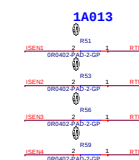
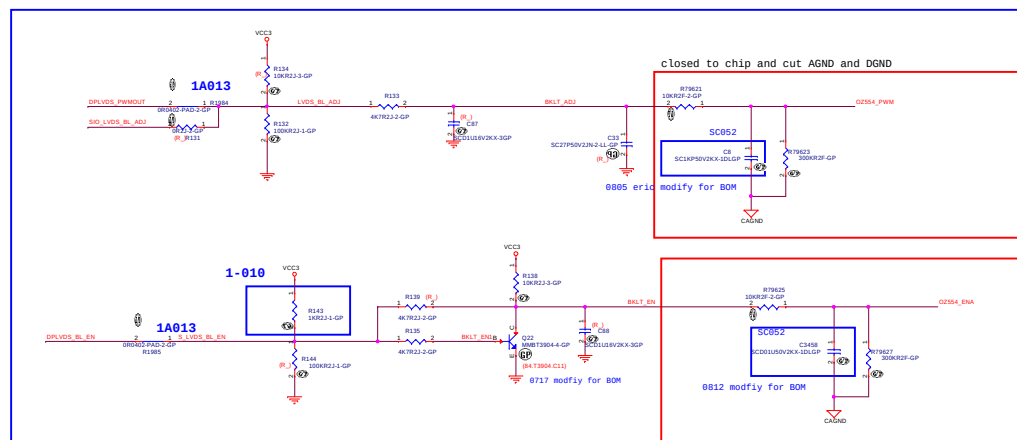
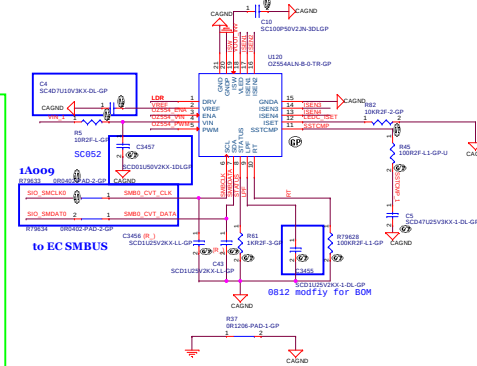




SCoo4

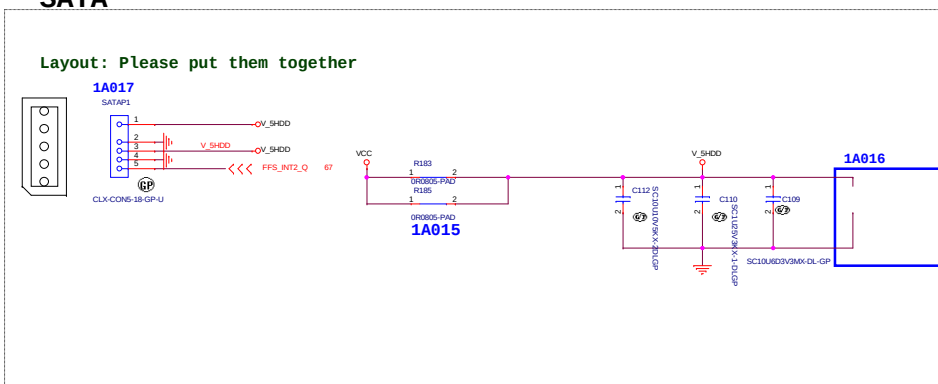
		Cable Spec			
23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout	
LG	1	0	0	3.4 Vout 1,2,3 RTN	
BOE	1	1	0	3.4 Vout 1,2,3 RTN	
AUO	1	0	1	3.4 Vout 1,2,3,4 RTN	

19.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
AUO	0	1	0	3.4 Vout 1,2,3,4 RTN
LG	0	0	1	3.4 Vout 1,2 RTN

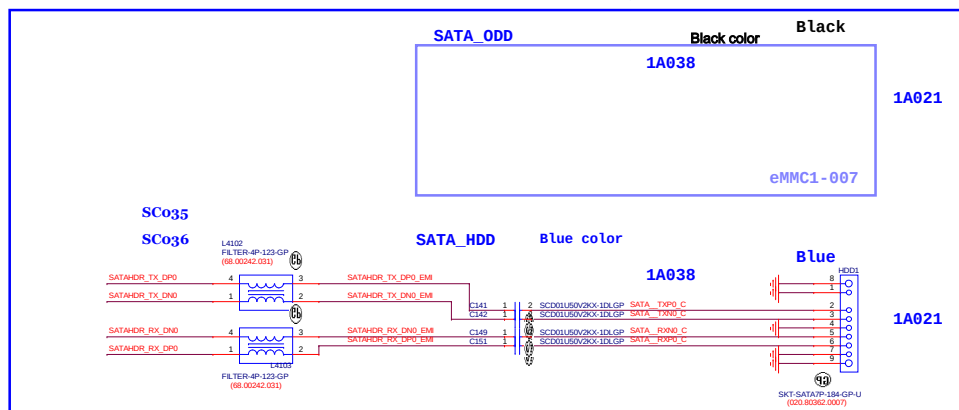


SATA

16	SATAHDR_RX_DP0	
16	SATAHDR_RX_DN0	
16	SATAHDR_TX_DN0	
16	SATAHDR_TX_DP0	

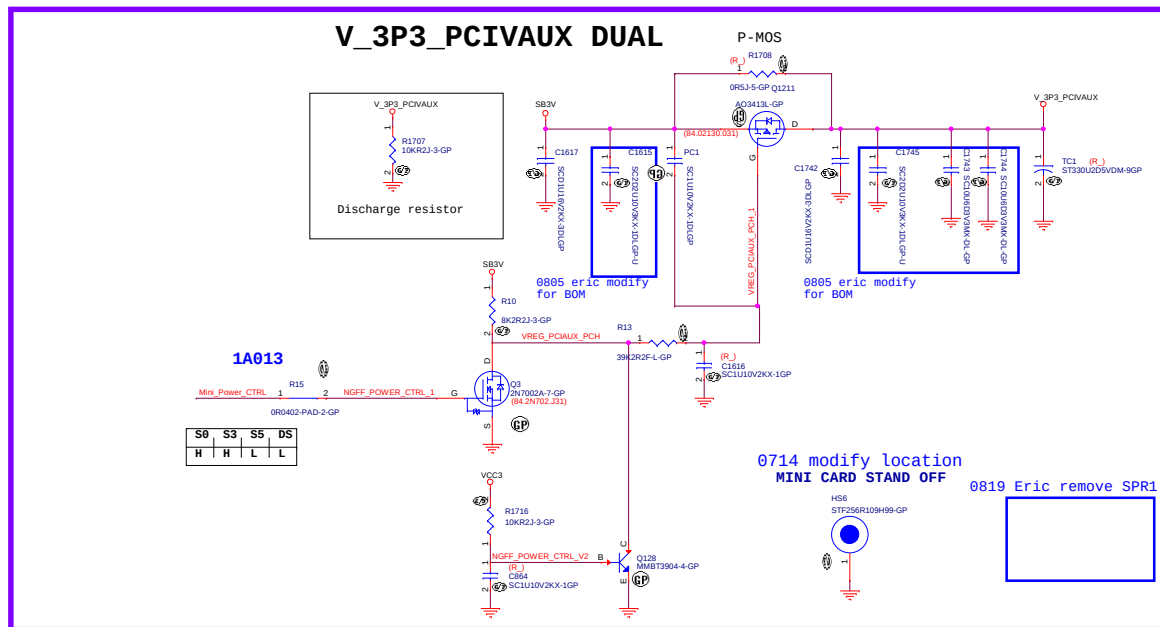
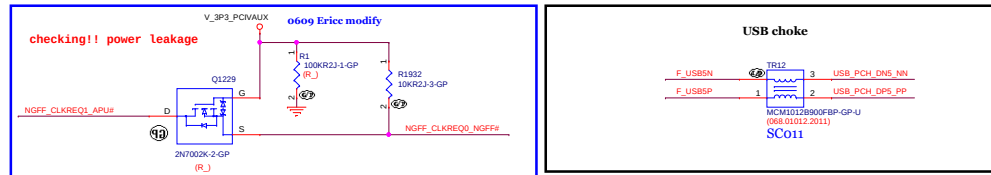
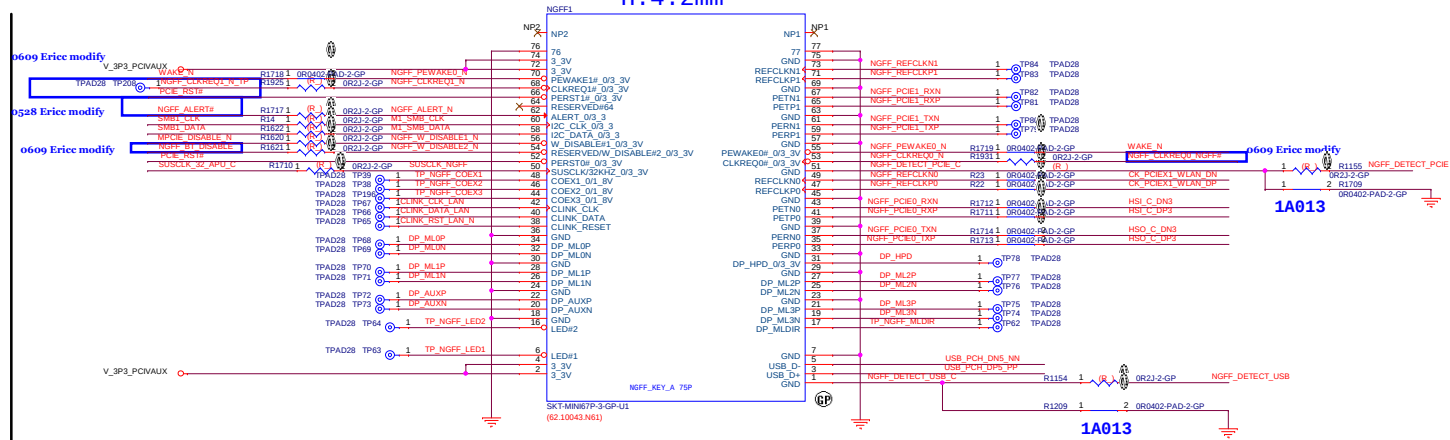


0811 Eric modify SATA connector
0725 Eric modify SATA connector



NGFF(A Key)

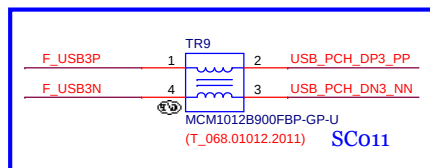
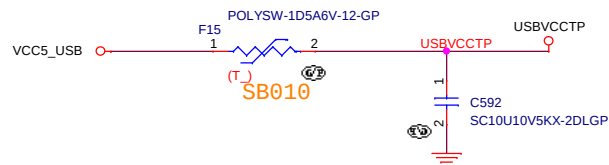
H: 4.2mm



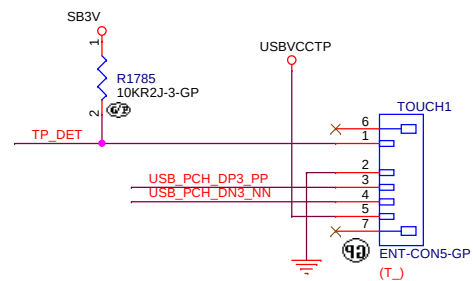
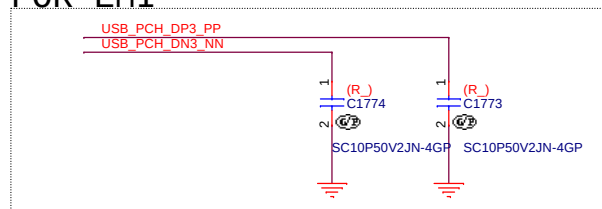
USB TOUCH PANEL

16 F_USB3P
16 F_USB3N
24 TP_DET

TOUCH PANEL



FOR EMI



<Variant Name>

wistron

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Title **062_TOUCH**

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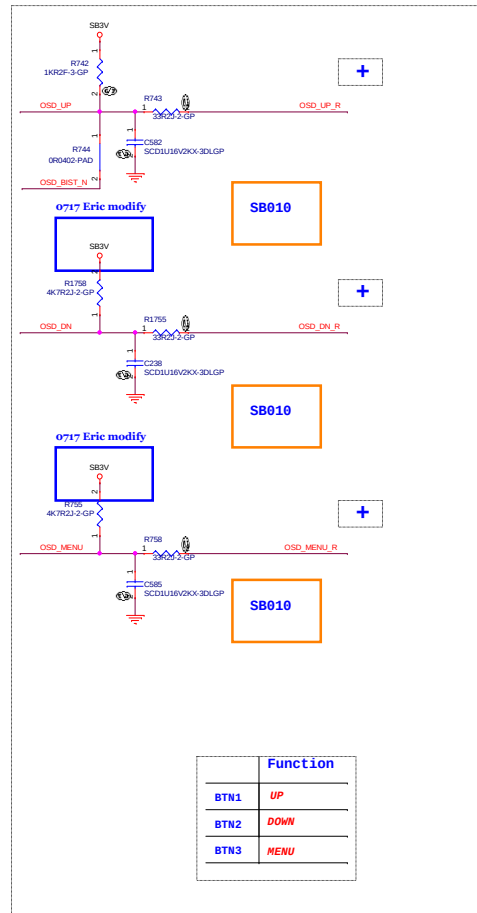


24,36 PWRBTN_N << PWRBTN_N

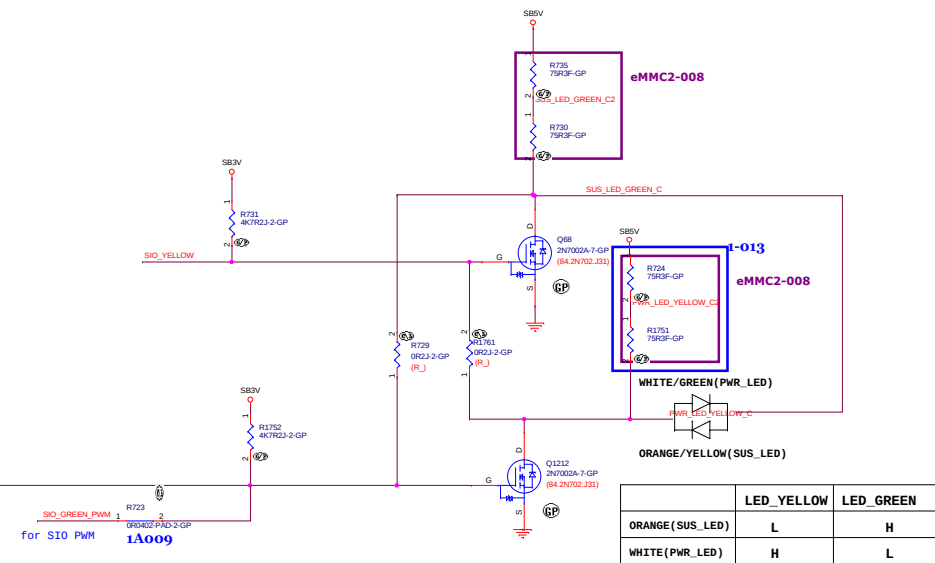
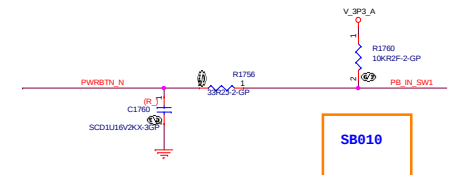
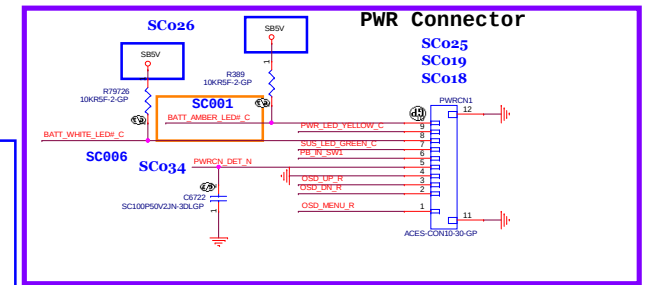
HD_LED

16	APU_SATA_LED_N	»
24	SIO_HDD_LED	»
24	SIO_YELLOW	»
24	SIO_GREEN	»
24	SIO_GREEN_PWM	«

18,24	OSD_MENU	OSD_MENU
18	OSD_UP	OSD_UP
18	OSD_DN	OSD_DN
55	OSD_BIST_N	OSD_BIST_N
24	PWRCN_DET_N	PWRCN_DET_N



The diagram illustrates the SATA LED control circuit. It features two LEDs: **APU SATA LED N** and **SATA_LED_N_C 1**. The **APU SATA LED N** is connected to **SB3V** and **SID_GREEN** through a resistor **R82002 (4K7C23-2-GP)**. The **SATA_LED_N_C 1** is connected to **SB3V** and **SID_GREEN** through a resistor **R82001 (4K7C23-2-GP)**. A 74VHC125 (Q9646) is used as a buffer, with its input connected to the **APU SATA LED N** and its output connected to the **SATA_LED_N_C 1**.

[illegible]

	LED_YELLOW	LED_GREEN
ORANGE(SUS_LED)	L	H
WHITE(PWR_LED)	H	L

<Variant Name>



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

Size
A4

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Title

Size
A3

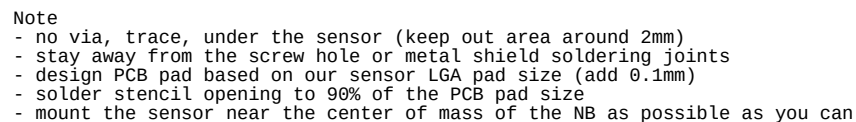
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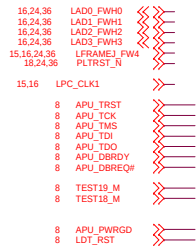
0716 modfiy from PLANO



Note

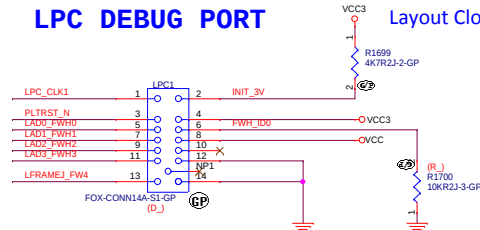
- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

LPC DEBUG PORT



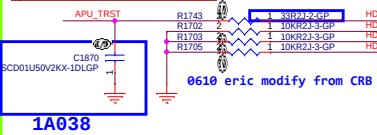
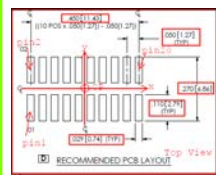
LPC DEBUG PORT

Layout Close SIO



Pin height 2.3mm

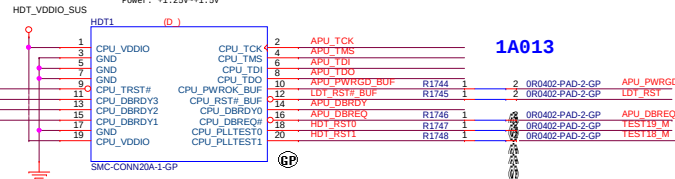
Follow Eagle



1A038

Debug Header

Power: +1.25V~+1.5V



70 EMMC_DATA_0
70 EMMC_DATA_1
70 EMMC_DATA_2
70 EMMC_DATA_3
70 EMMC_DATA_4
70 EMMC_DATA_5
70 EMMC_DATA_6
70 EMMC_DATA_7
70 EMMC_CLK
70 EMMC_CMD

18,24,36,68 PLTRST_N >>>

24 EMMC_RESET_SIO>>>

The schematic diagram illustrates the connection of two eMMC components, eMMC1-011 and eMMC1-010, to a microcontroller (U903A). The power supply network is shown with DVCC3 and DVCC1D8V rails. The eMMC1-011 is connected to the U903A via the data bus (A3-A7, B3-B7, C4-C7, H10, J5, K8, N2, P4, P6). The eMMC1-010 is connected to the U903A via the data bus (A3-A7, B3-B7, C4-C7, H10, J5, K8, N2, P4, P6). The U903A is a KLMBG4GEND-B031-GP microcontroller.

[illegible]

EMMC_RCLK_M

R90012
10KR2J-3-GP
(R_)

Signal	Pin	Connector	Pin	Signal
EMMC_CMD	R90013 1	(R.)	1	TP5014
EMMC_DATA_0	R90014 1	(R.)	1	TP5015
EMMC_DATA_1	R90015 1	(R.)	1	TP5016
EMMC_DATA_2	R90016 1	(R.)	1	TP5017
EMMC_DATA_3	R90017 1	(R.)	1	
EMMC_DATA_4	R90018 1	(R.)	1	
EMMC_DATA_5	R90019 1	(R.)	1	
EMMC_DATA_6	R90020 1	(R.)	1	
EMMC_DATA_7	R90021 1	(R.)	1	
EMMC_E9		(R.)	1	
EMMC_E10			1	
EMMC_F10			1	
EMMC_K10			1	

U903B		2 OF 2	
A1	NC#A1	NC#J3	J3
A2	NC#A2	NC#J12	J12
A8	NC#A8	NC#J13	J13
A9	NC#A9	NC#J14	J14
A10	NC#A10	NC#K1	K1
A11	NC#A11	NC#K2	K2
A12	NC#A12	NC#K3	K3
A13	NC#A13	NC#K12	K12
A14	NC#A13	NC#K12	K13
B1	NC#A14	NC#K13	K14
B7	NC#B1	NC#K14	L1
B8	NC#B7	NC#L1	L2
B9	NC#B8	NC#L2	L3
B10	NC#B9	NC#L3	L12
B11	NC#B10	NC#L12	L13
B12	NC#B11	NC#L13	L14
B13	NC#B12	NC#L14	M1
B14	NC#B13	NC#M1	M2
C1	NC#B14	NC#M2	M3
C3	NC#C1	NC#M3	M7
C5	NC#C3	NC#M7	M8
C7	NC#C5	NC#M8	M9
C8	NC#C7	NC#M9	M10
C9	NC#C8	NC#M10	M11
C10	NC#C9	NC#M11	M12
C11	NC#C10	NC#M12	M13
C12	NC#C11	NC#M13	M14
C13	NC#C12	NC#M14	N1
C14	NC#C13	NC#N1	N3
D1	NC#C14	NC#N3	N6
D2	NC#D1	NC#N6	N7
D3	NC#D2	NC#N7	N8
D4	NC#D3	NC#N8	N9
D12	NC#D4	NC#N9	N10
D13	NC#D12	NC#N10	N11
D14	NC#D13	NC#N11	N12
E1	NC#D14	NC#N12	N13
E2	NC#E1	NC#N13	N14
E3	NC#E2	NC#N14	P1
E12	NC#E3	NC#P1	P2
E13	NC#E12	NC#P2	P8
E14	NC#E13	NC#P8	P9
F1	NC#E14	NC#P9	P11
F2	NC#F1	NC#P11	P12
F3	NC#F2	NC#P12	P13
F12	NC#F3	NC#P13	P14
F13	NC#F12	NC#P14	
F14	NC#F13		
G1	NC#F14		A7
G2	NC#G1	RFU#A7	E5
G12	NC#G2	RFU#E5	E8
G13	NC#G12	RFU#E8	
G14	NC#G13	RFU#E9	EMMC_E9
H1	NC#G14	RFU#E10	EMMC_E10
H2	NC#H1	RFU#F10	F10
H3	NC#H2	RFU#G3	EMMC_F10
H12	NC#H3	RFU#G10	G10
H13	NC#H12	RFU#K6	K6
H14	NC#H13	RFU#K7	K7
J1	NC#H14	RFU#K10	
J2	NC#J1	RFU#P7	EMMC_K10
	NC#J2	RFU#P10	P7



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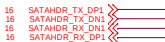
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eMMC1-004

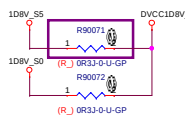
eMMC DATA



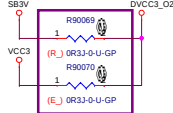
SATA 3.0



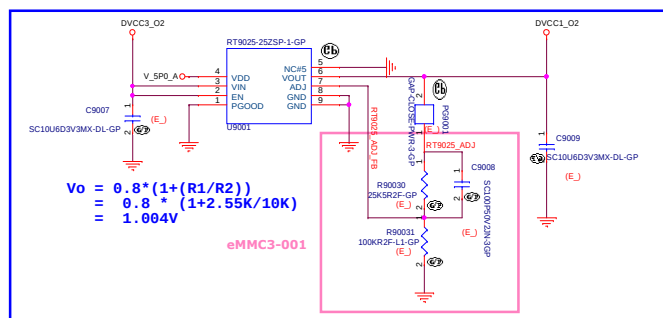
eMMC2-002



eMMC2-006



20150505 eMMC2-001

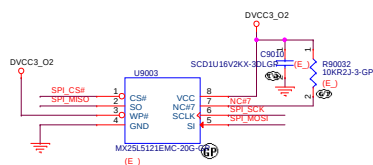


$$V_o = 0.8 * (1 + (R1/R2))$$

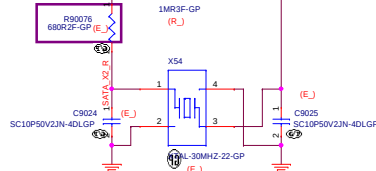
$$= 0.8 * (1 + 2.55K/10K)$$

$$= 1.004V$$

eMMC3-001



eMMC2-004

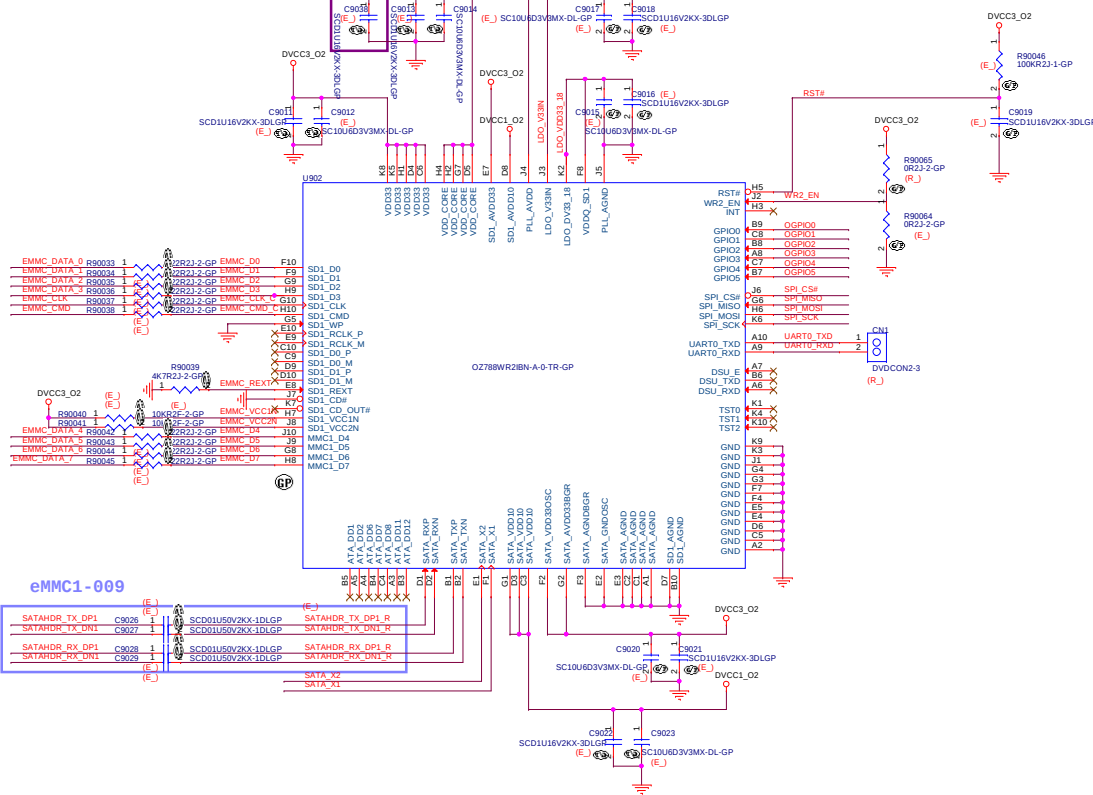


P1V active total current is about 120mA;
P3V3 active total current is about 20mA.
(Not include eMMC chip current)

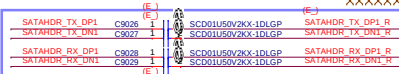
eMMC2-003



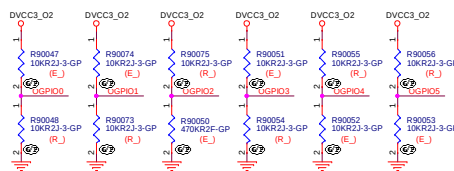
eMMC2-003



eMMC1-009



eMMC GPIO



GPIO0 can be used as GPIO. And default is input mode, please clamp this pin to GND or P3V3 to avoid input floating condition if customer doesn't use this pin.

GPIO1 is LED control signal output as default. If LED is not used, please leave this pin open.

GPIO : 2013.08.19
0 : Lo (for input mode)
1 : Lo (for input mode)
2 : Hi = FW skip 10s time out
3 : Hi = 50MHz CPU clock
4 : Hi = 50MHz CPU clock
5 : Lo = 24bit (Which Flash?)

	Pull-down	Pull-up
GPIO3	FW will wait init done bit set or 10s time out	FW skip 10s time out
GPIO4	100MHz CPU clock frequency	50MHz CPU clock frequency
GPIO5	SPI 24bit Mode	SPI 16bit Mode

<Variant Name>

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File	070_eMMC_OZ788	Rev
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Title

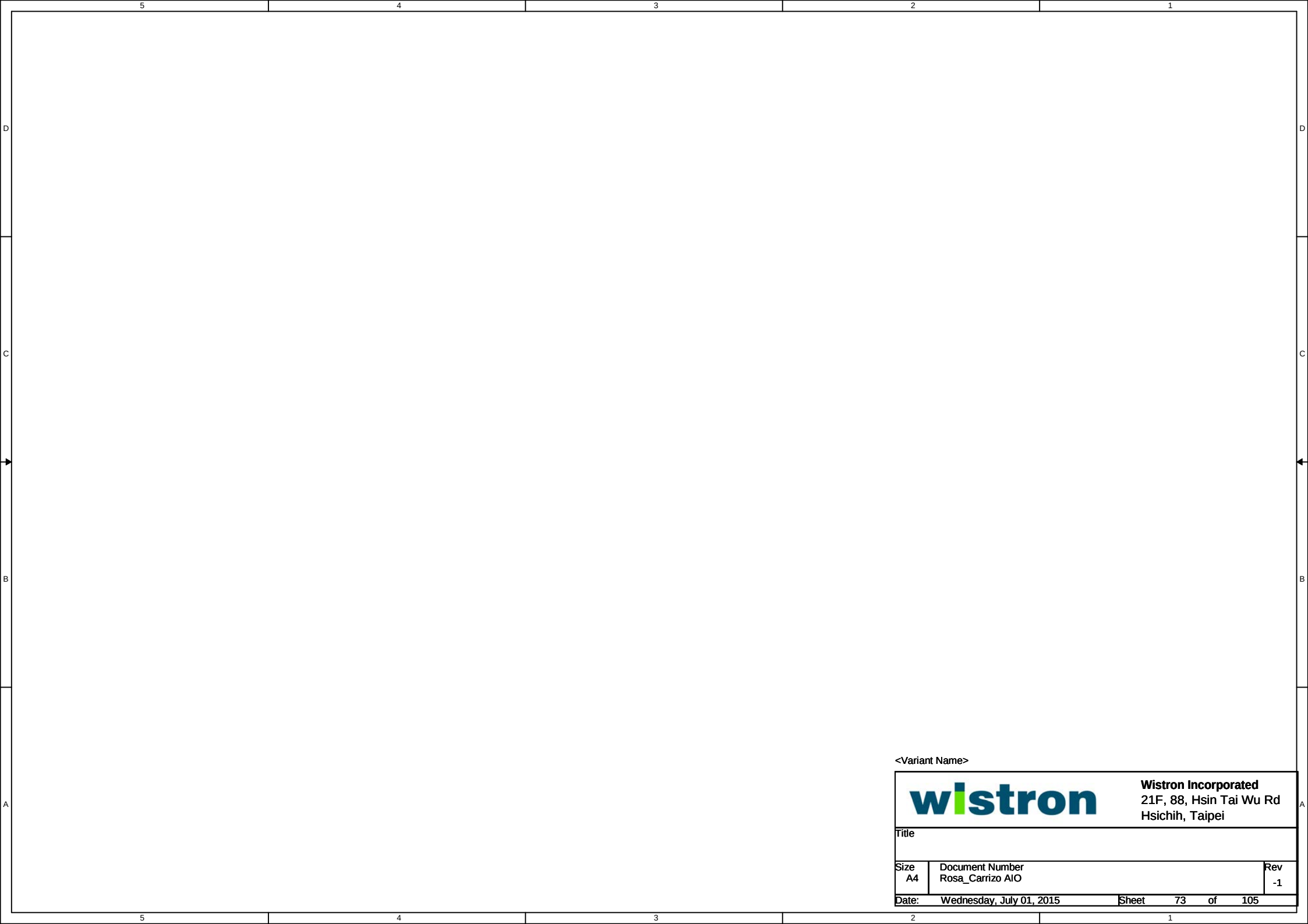
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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eMMC1-000

eMMC1-000

eMMC1-000

emmc1-000



5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>



0617 Eric delete TPM

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Title TPM		
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A																								

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<Variant Name>

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Title TBD			
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	123-129
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	78-84
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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A4

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C																								
B																								
A																								

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6-1.2-7c(2.40) stack up and impedance

產品編號		6-1.2-7c	注意事項	1. Impedance Control tolerance +/- 10% 2. Coupon 製作參考 Impedance report 請依照 Wistron 規格製作					
波中距 (mm)		1.2 ± 0.12							
Stack up			Impedance Request List						
			Thickness (mil)	Layer	L1 (Ref. Plane) ^①	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)	
				Spec	Single Ended Type (Trace width : mil)				
L1	TOP								

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wistron

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101_Stackup

Size B

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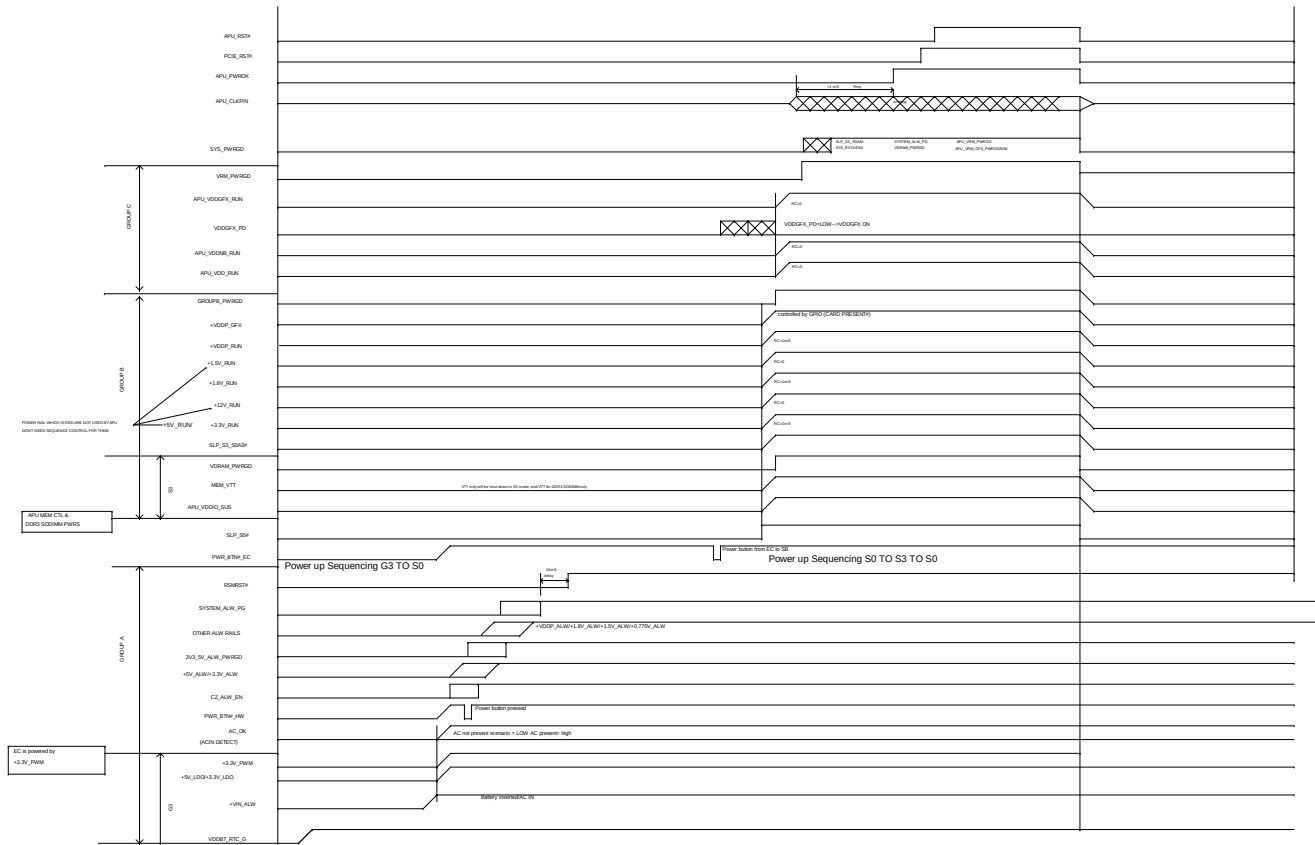
Date

Wednesday, July 01, 2015

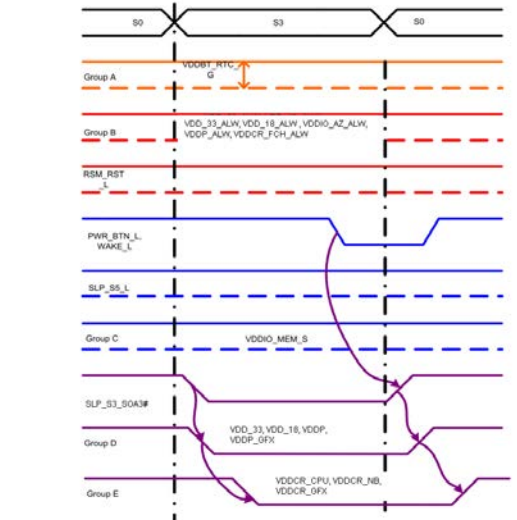
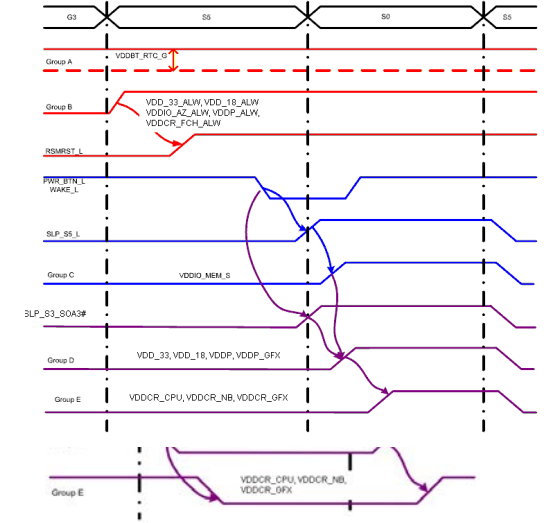
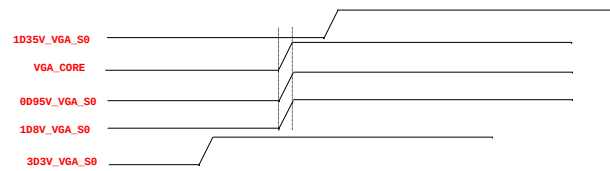
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FROM AMD CRB BOARD

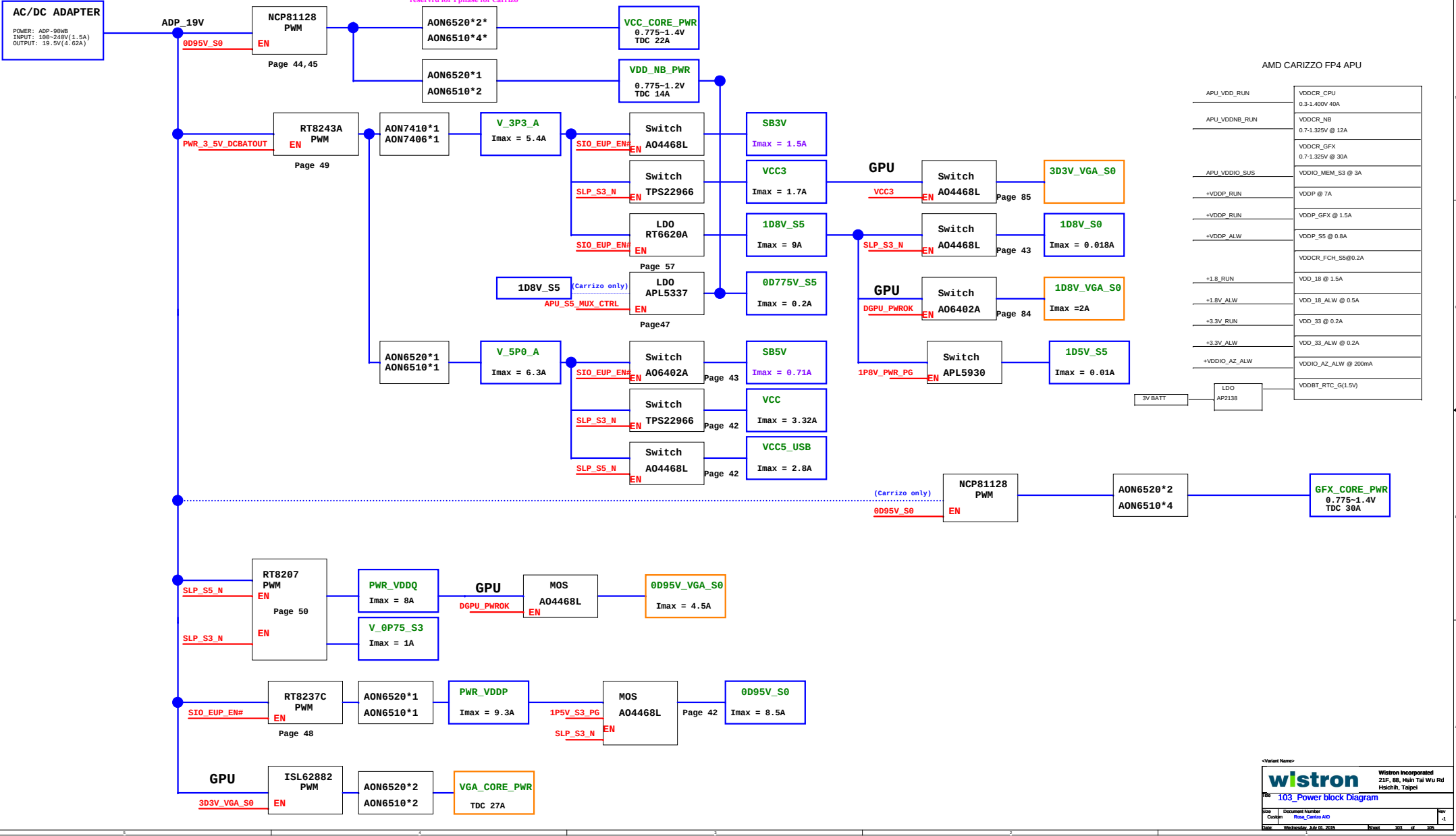


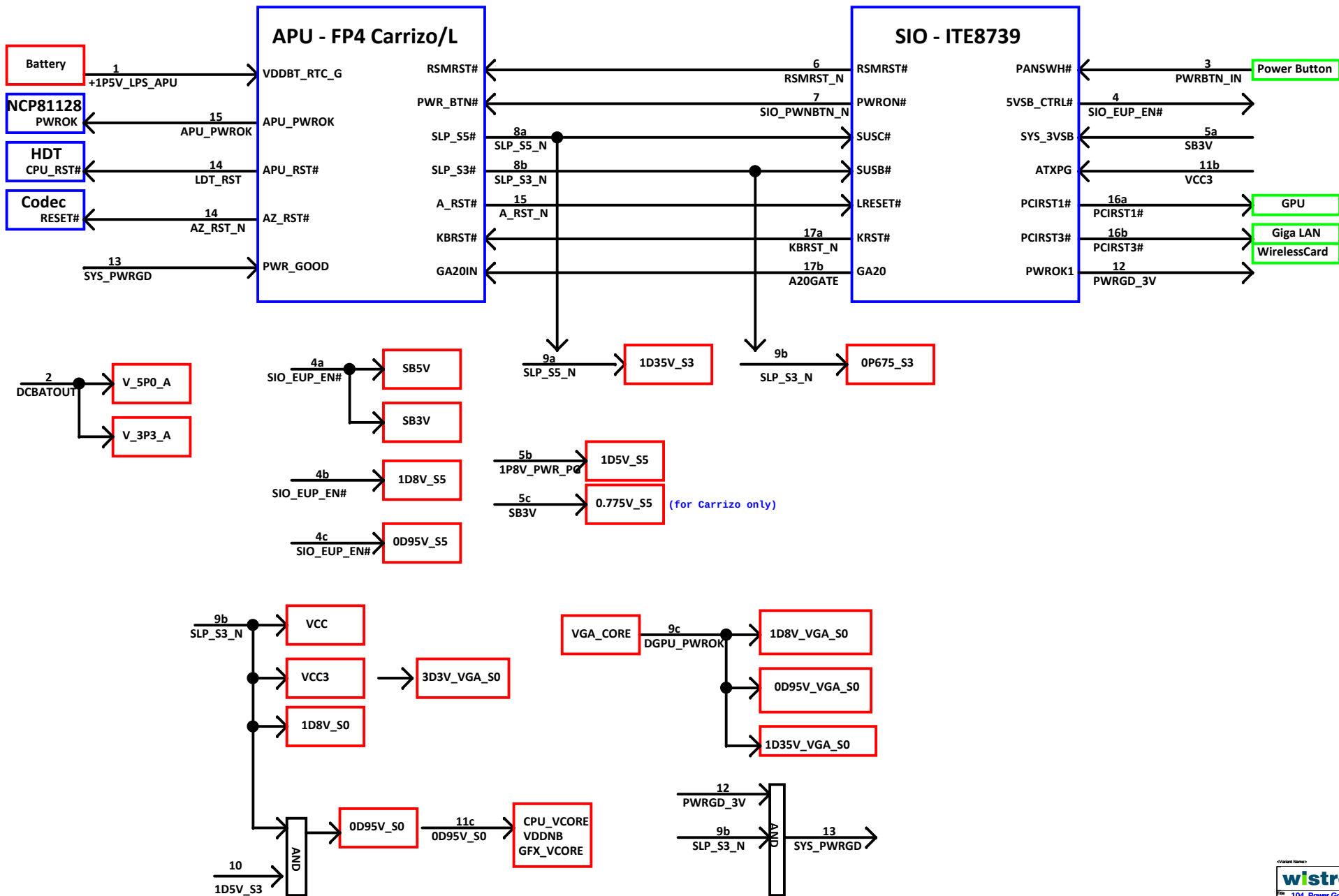
AMD GPU sequence

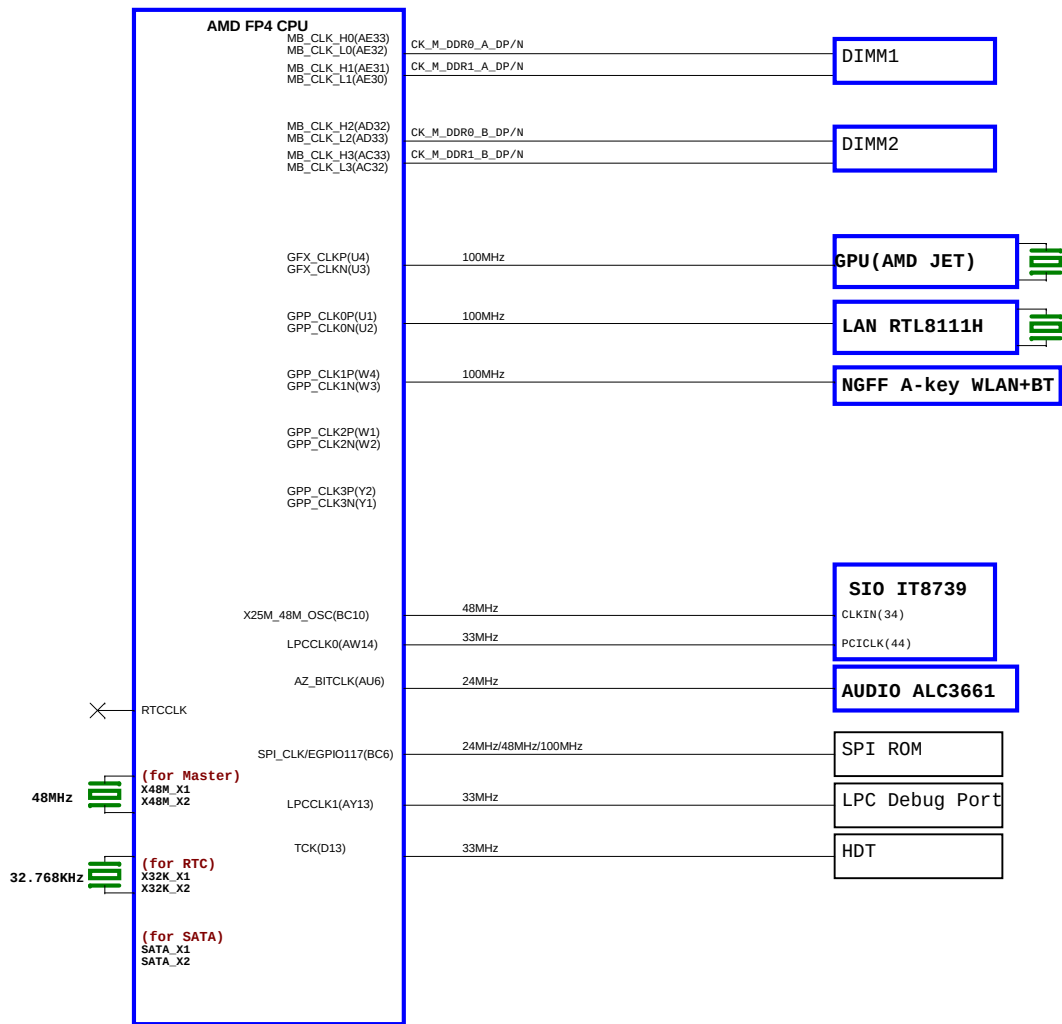


Power on Sequence required:

- There is no sequencing requirement between power supplies within the individual power groups.
- All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 12% of its specified minimum operating voltage.
- All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 12% of its specified minimum operating voltage.
- All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 12% of its specified minimum operating voltage.







SMBus Block Diagram

ALL SLAVE ADDRESS IS 8-BIT INCLUDING W/R BIT
SLAVE ADDRESS FOR SLOT/HEADER PLEASE REFER TO MODULE SPEC

