

COMPAL CONFIDENTIAL

MODEL NAME :
FDI40 N3-14", FDI4A V3-14", FDI43 N5-14",
FDI50 N3-15", FDI5A V3-15", FDI53 N5-15",
FDI70 N3-17"

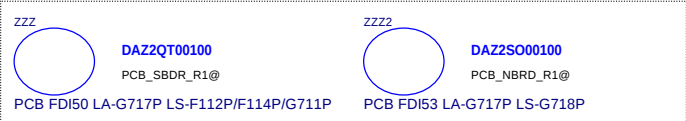
PCB NO : DA60027S000 (SBDR)
DA60027S100 (NBDR)

BOM P/N :

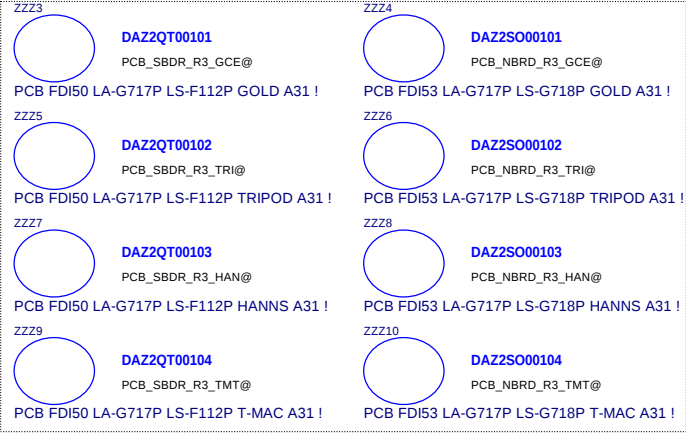
SBDR-UMA	NBDR-UMA	X4E
431AJ331L51 431AJ331L54	431AJ331L01	X4E AJ331L51(N3)
431AJ331L52 431AJ331L55	431AJ331L02	X4E AJ331L52(V3)
431AJ331L53 431AJ331L56	431AJ331L03	X4E AJ331L01(N5)

CML-U+MEC1418
2019-06-19
REV : 1.0 (A00)

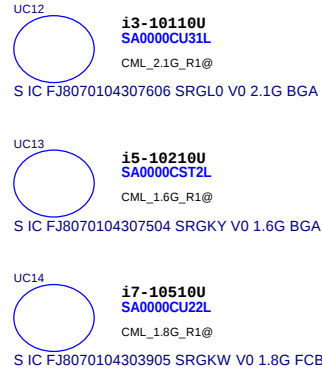
PCB R1



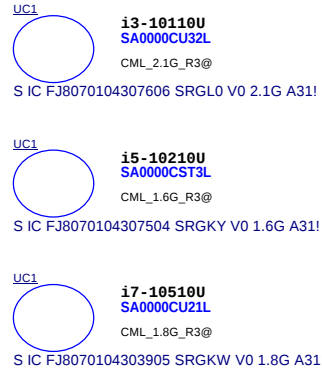
PCB R3



CPU R1



CPU R3



@ : Un-pop Component
DIS@ : GPU Support
N3@/V3@ : Inspiron/Vostro
CML@/CNL@ : CML/CNL
BASE@/PREM@ : (Pentium)(Celeron)i3 i5 i7

EC@ : EC Support
JP@/PJP@ : JUMP
100@/1000@: Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
750_CTPM@:750 and china TPM
ST_CTPM@:ST and china TPM
CTPM@:China TPM
FFS@ : Free Fall Sensor
TYPEC@ : TypeC
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component

PCB@/PCB_R1@/PCB_R3_G@/PCB_R3_T@/PCB_R3_H@/PCB_R3_TM@: PCB MB

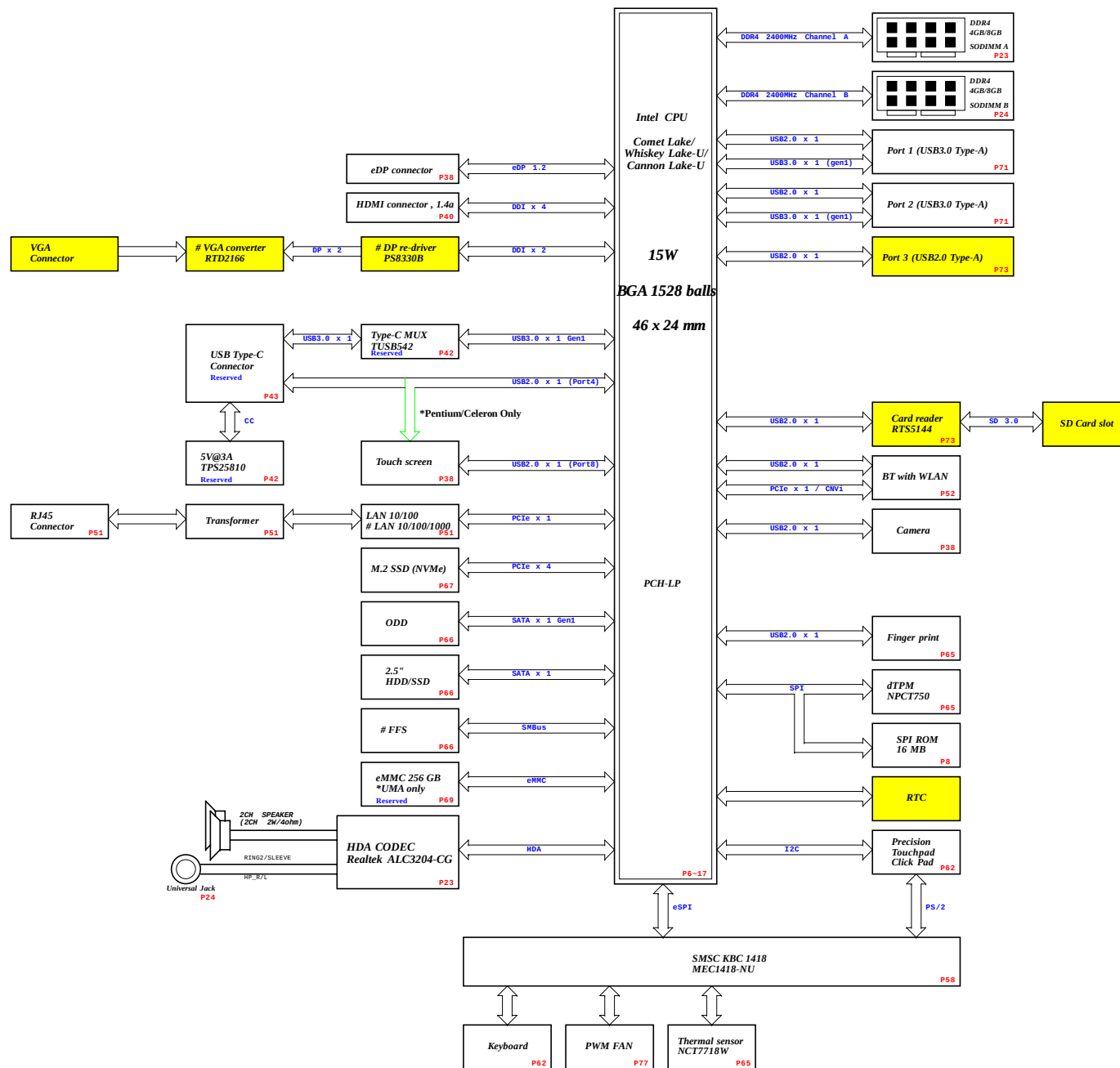
PCB_NBRD_R1@: PCB MB for NBDR
TS_NON@/TS_USB@/TS_I2C@: Touch Screen Interface Select
SBDR@/NBDR@: SBDR/ NBDR Select

Layout Dell logo

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REV: X00
PWB: 9HTP8

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Size		Document Number		Rev	
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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 Port, IO/B
4*	Touch screen
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Reserved
9	NA
10	BT

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 port1
USB3.0-2	PCIE-2		NA
USB3.0-3	PCIE-3		USB3.0 port2
USB3.0-4	PCIE-4		TypeC
USB3.0-5	PCIE-5		
USB3.0-6	PCIE-6		
	PCIE-7		
	PCIE-8		
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA ODD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

Board ID & Model ID Table

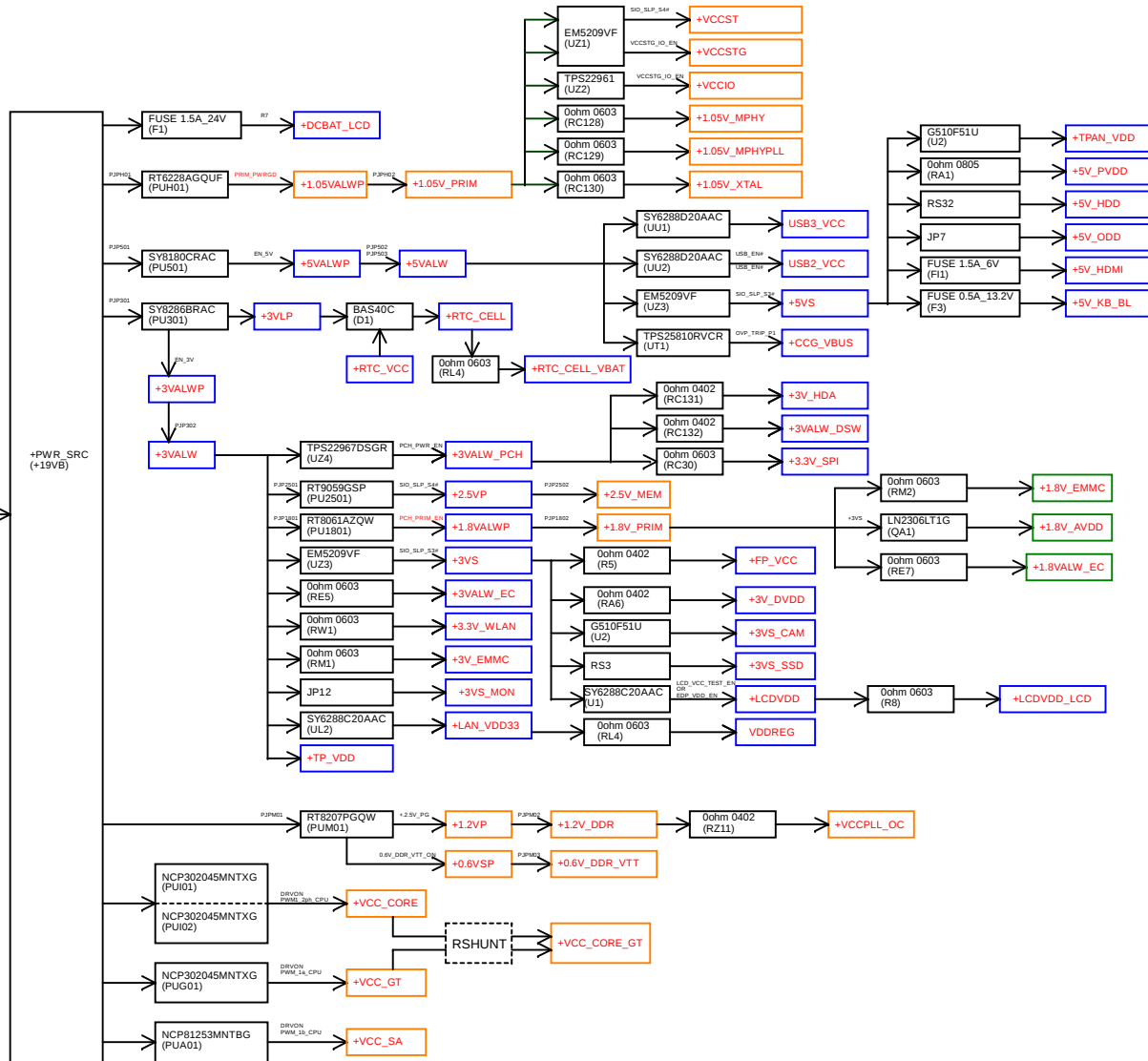
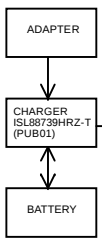
#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100	10.0	3.000	EVT	SBDR-UMA
2	100	17.8	2.801	DVT1	
3	100	27.0	2.598		NBDR-UMA
4	100	37.4	2.402	DVT2	
5	100	49.9	2.201		SBDR-DSC
6	100	64.9	2.001	Pilot	
7	100	82.5	1.808		NBDR-DSC
8	100	107.0	1.594		
9	100	154.0	1.299		
10	100	200.0	1.100		

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

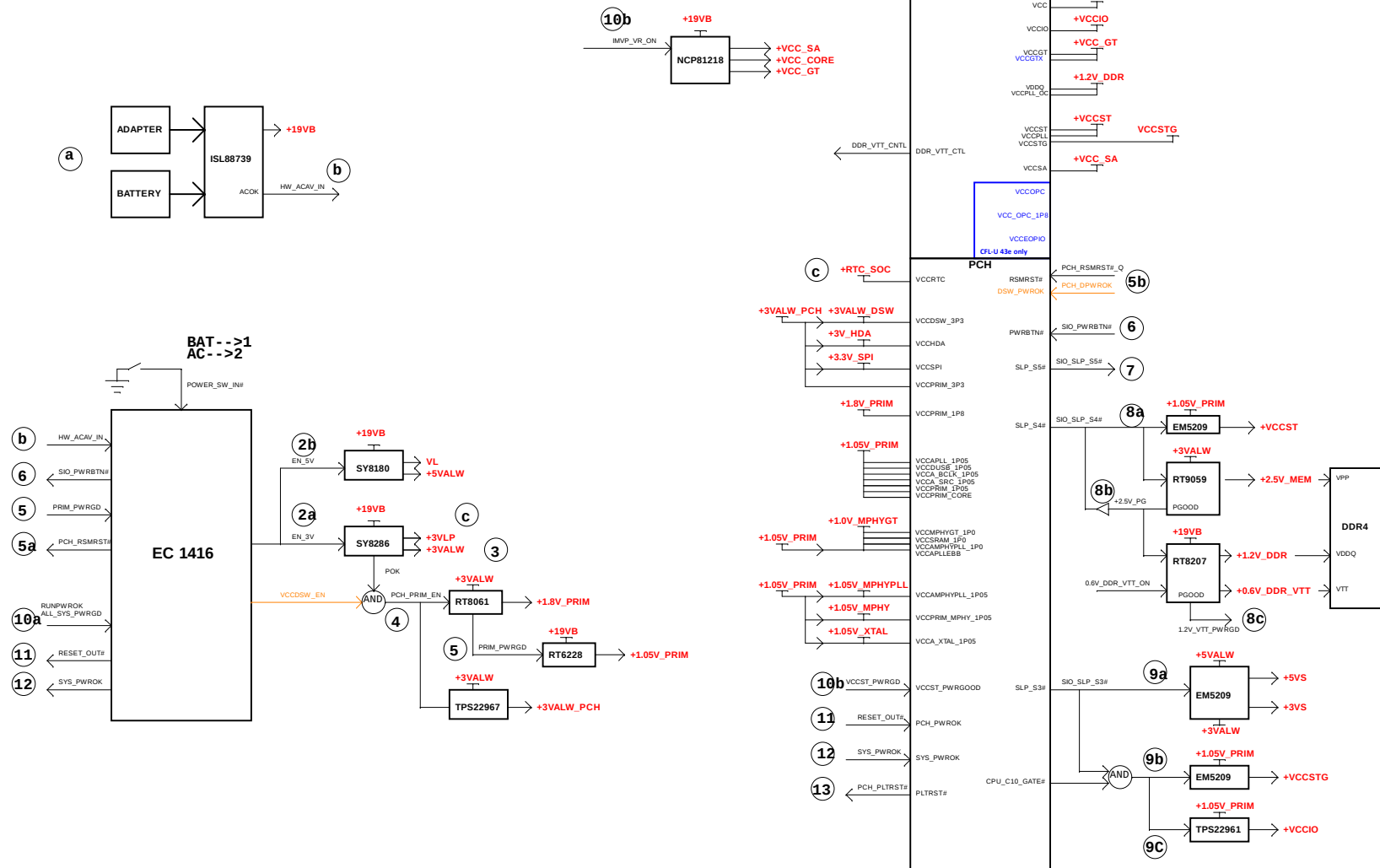
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

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CPU PWR
GPU PWR
Peripheral Device PWR

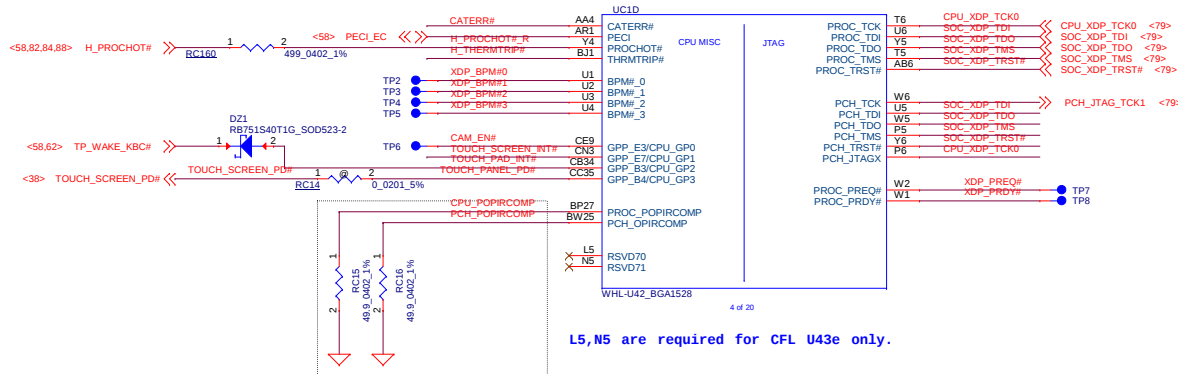
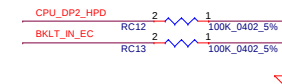
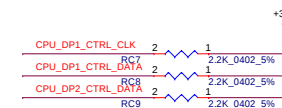
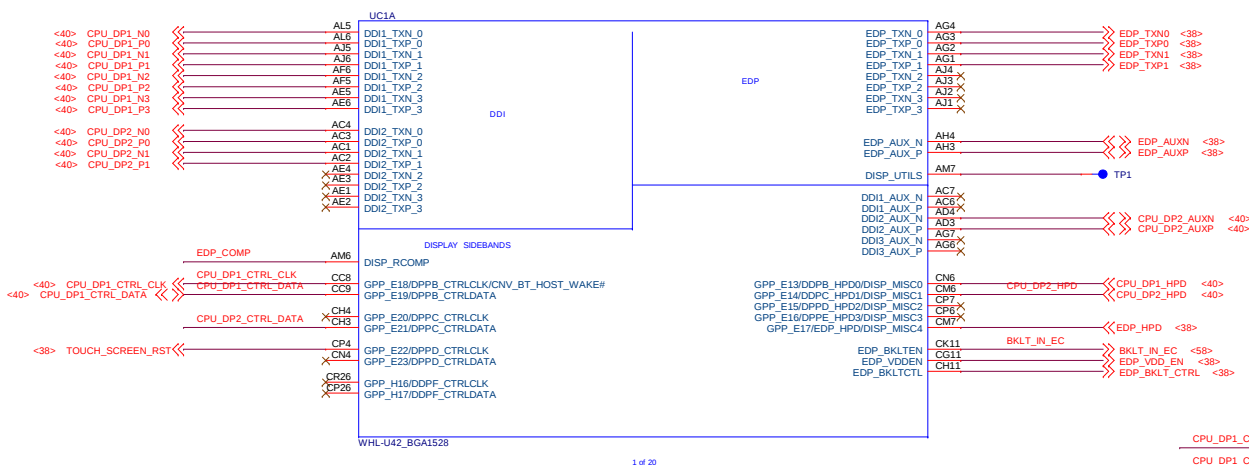
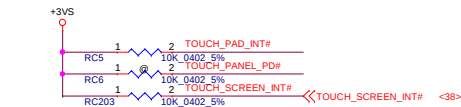
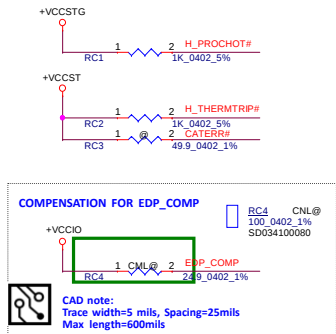


Timing Diagram for S5 to S0 mode



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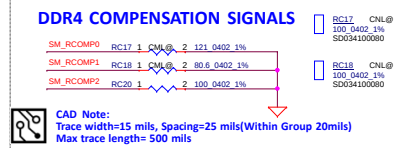
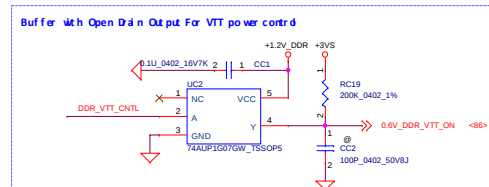
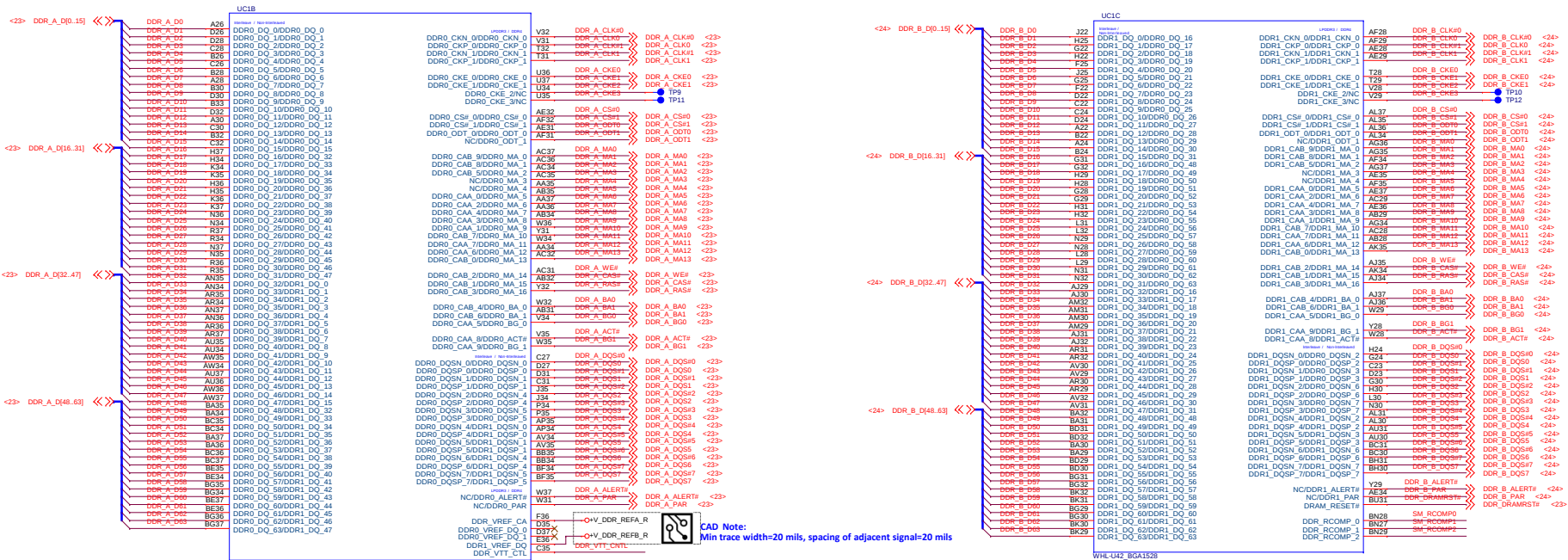
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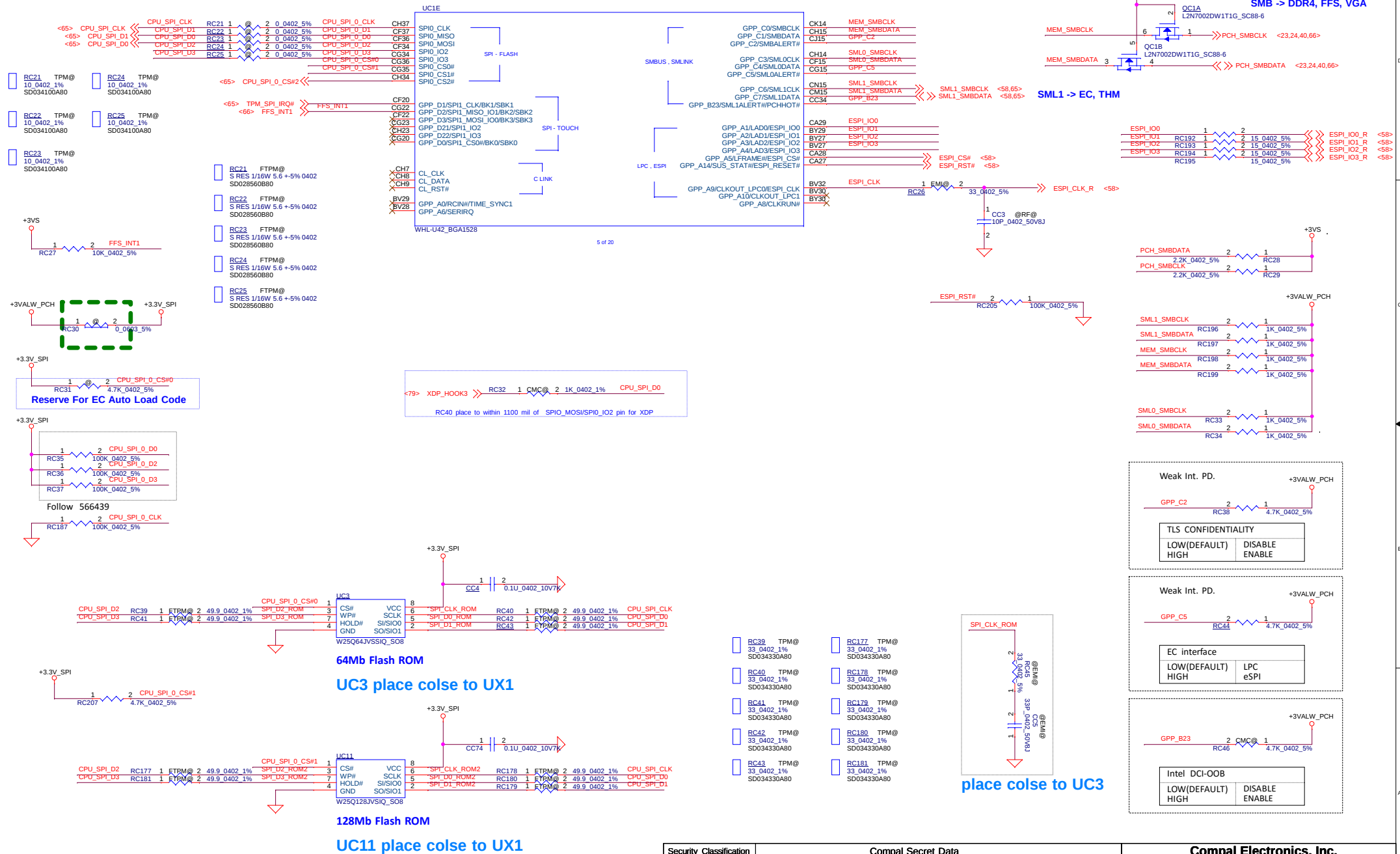
COMPENSATION FOR OPORCOMP
CAD Note:
Min trace width=10 mils, Max trace length=500 mils

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DDR4 Interleaved Memory

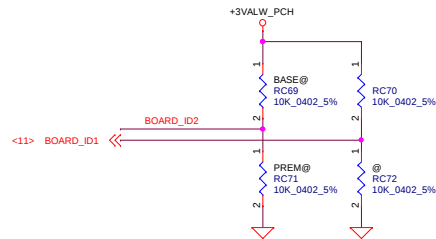
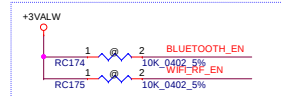
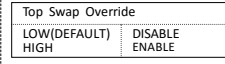


RC21~RC25 place colse to Device

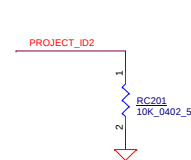
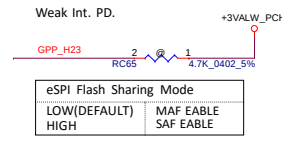
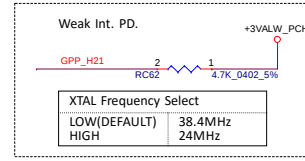
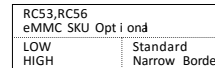
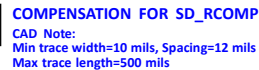
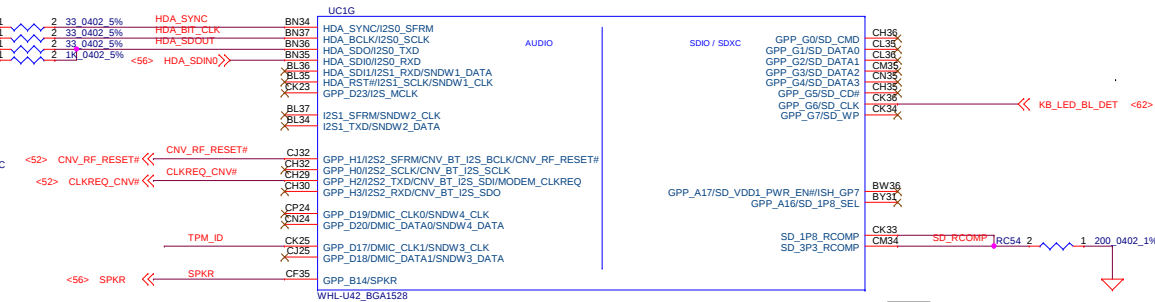


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LOW = ENABLE -->ME lock, can't update ME
HIGH = DISABLE -->ME un-lock, can update ME



CPU ID	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
CML-U	---	RC70
WHL-U(Reserved)	---	RC72
Pentium/Celeron	RC69	---
i3/i5/i7	RC71	---



PROJECT_ID2	
LOW(DEFAULT)	UMA
HIGH	DIS

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RCU7, RCU8, RCU9, RCU10 close to Device

UC1J

CLOCK SIGNALS

CLKOUT_ITPXD_P_N
CLKOUT_ITPXD_P_P
CLKOUT_PCIE_N_1
CLKOUT_PCIE_P_1
CLKOUT_PCIE_N_2
CLKOUT_PCIE_P_2
CLKOUT_PCIE_N_3
CLKOUT_PCIE_P_3
CLKOUT_PCIE_N_4
CLKOUT_PCIE_P_4
CLKOUT_PCIE_N_5
CLKOUT_PCIE_P_5

GPP_B8/SRCLKREQ#0
GPP_B9/SRCLKREQ#1
GPP_B7/SRCLKREQ#3
GPP_B9/SRCLKREQ#4
GPP_B10/SRCLKREQ#5

GPDB/SUSCLK#
XTAL_IN
XTAL_OUT
XCLK_BIASREF
CLKIN_XTAL
RTCK1
RTCK2
SRTCST#
RTCKST#

WLAN--> [<S2> CLK_PCIE_N1
<S2> CLK_PCIE_P1
<S2> CLKREQ_PCIE#1]

LAN--> [<S1> CLK_PCIE_N2
<S1> CLK_PCIE_P2
<S1> CLKREQ_PCIE#2]

SSD--> [<67> CLK_PCIE_N4
<67> CLK_PCIE_P4
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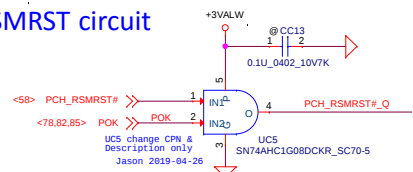
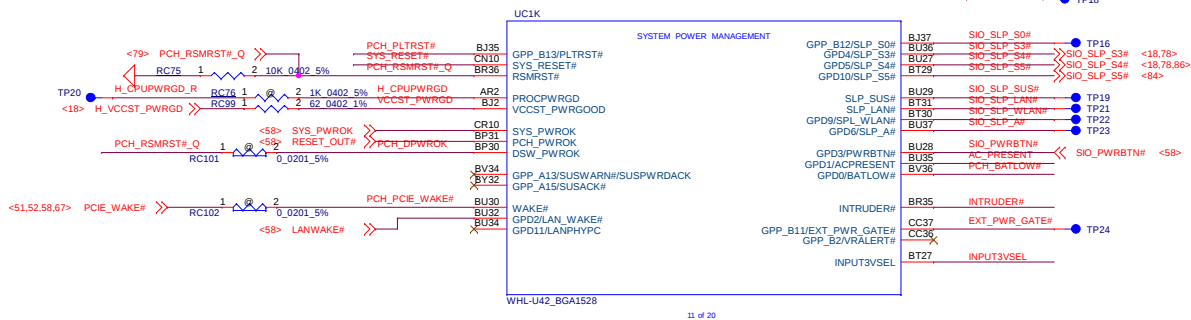
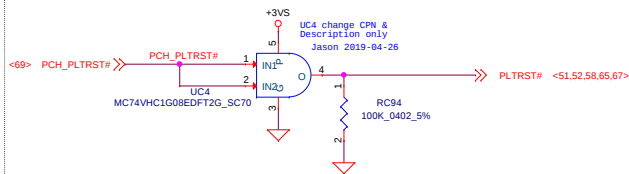
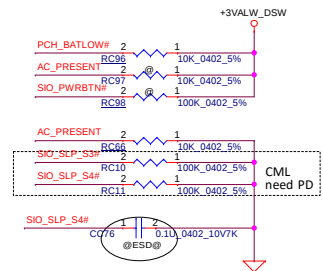
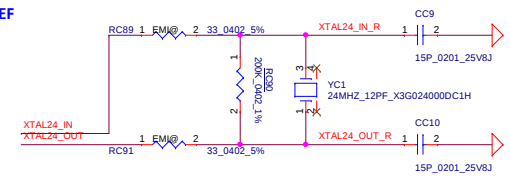
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RCB5 1 2 10K 0402 5%
RCB8 1 2 10K 0402 5%

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AY3
CF32
BC1
BC2
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BH4
XE31
BA1
BA2
CE30
BE1
BE2
CF31

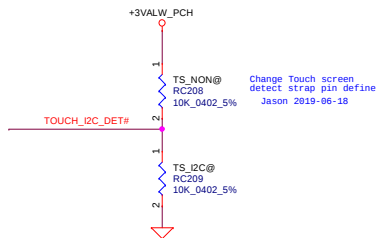
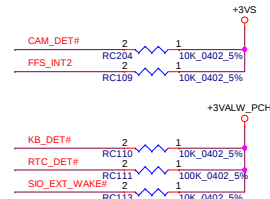
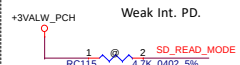
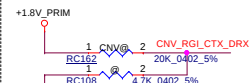
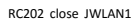
WHL-U42_BGA1528

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COMPENSATION FOR XCLK_BIASREF
CAD Note:
Min trace width=10 mils, Spacing=15 mils
Max trace length=1000 mils



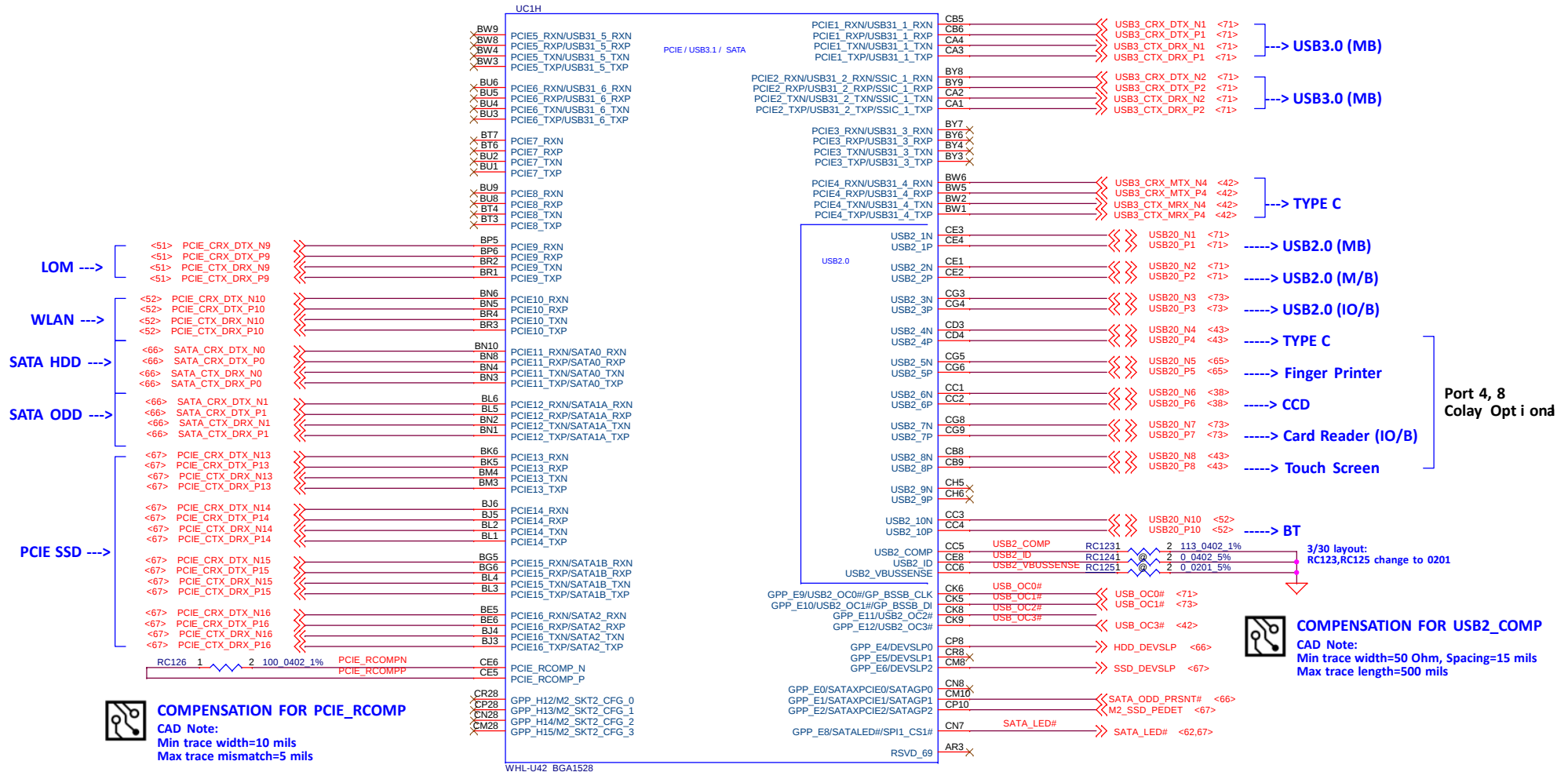
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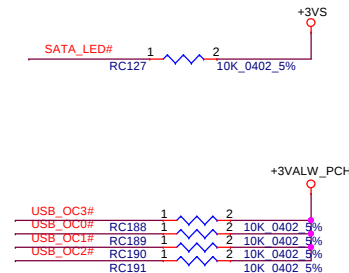
RC208,RC209 Touch panel interface	
LOW	I2C
HIGH	USB

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

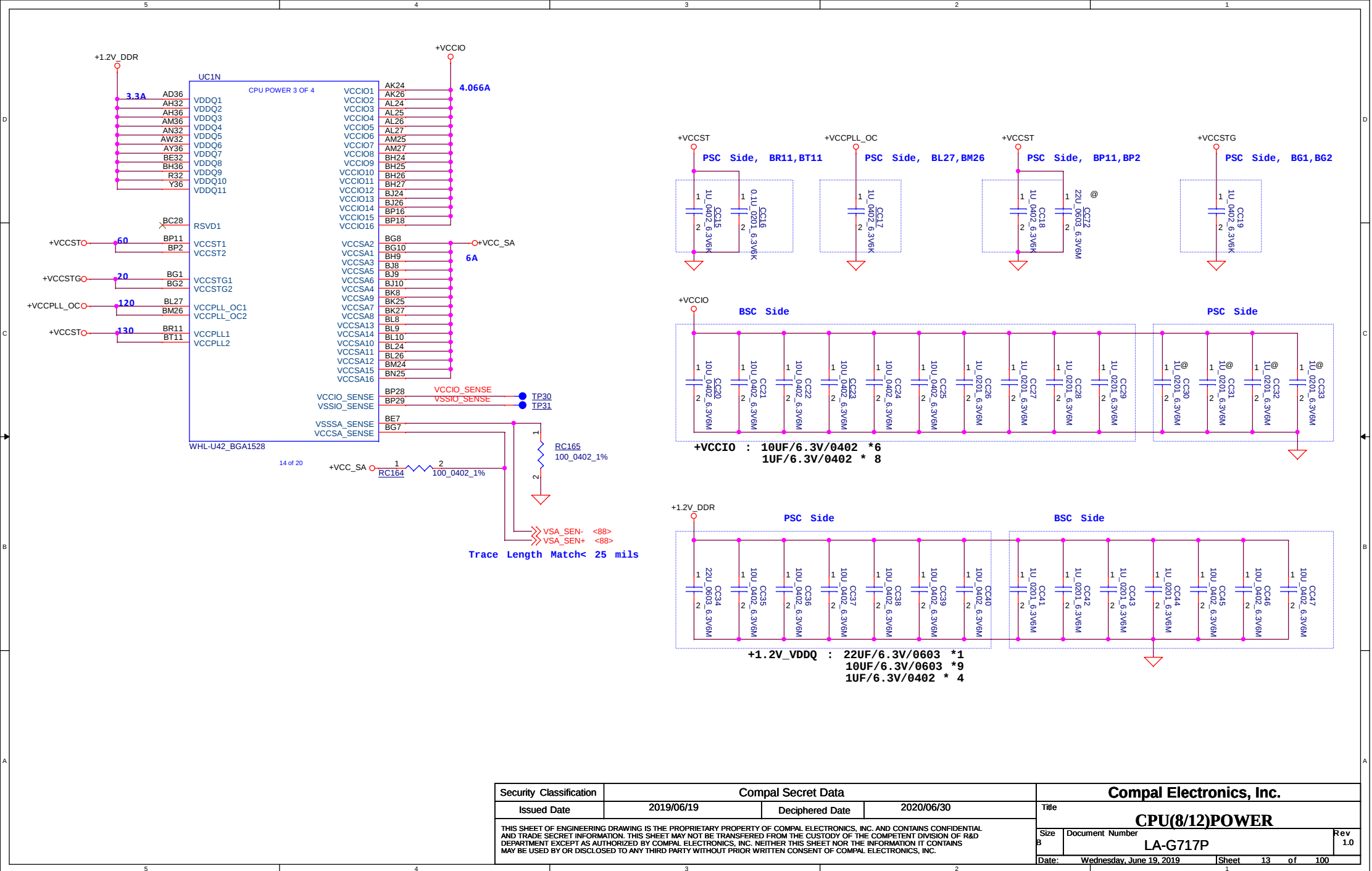
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Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	CPU(612)GPIO	
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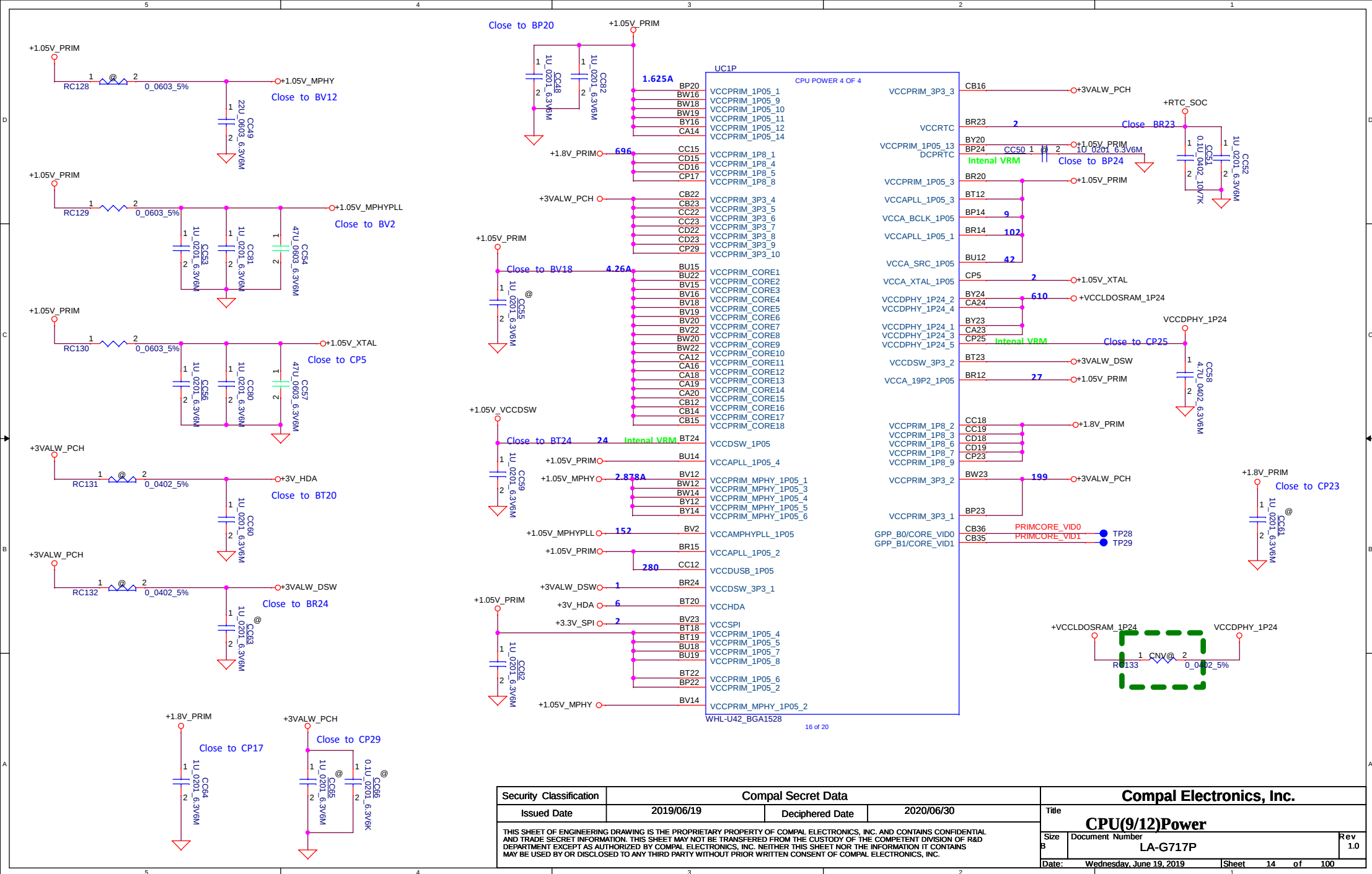
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USB_OC1#	USB Port (DB)
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USB_OC3#	USB Port (Type-C)
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD

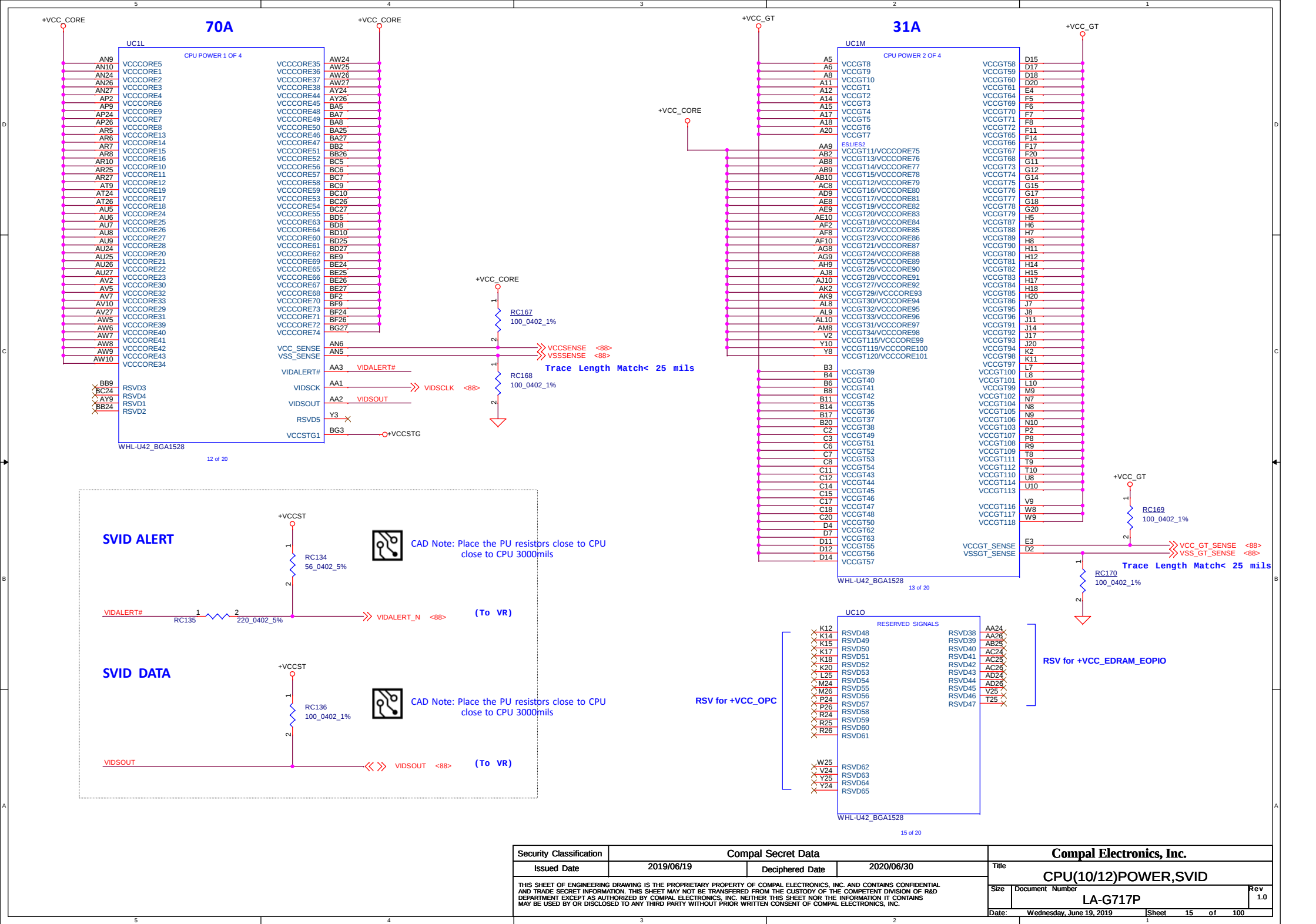


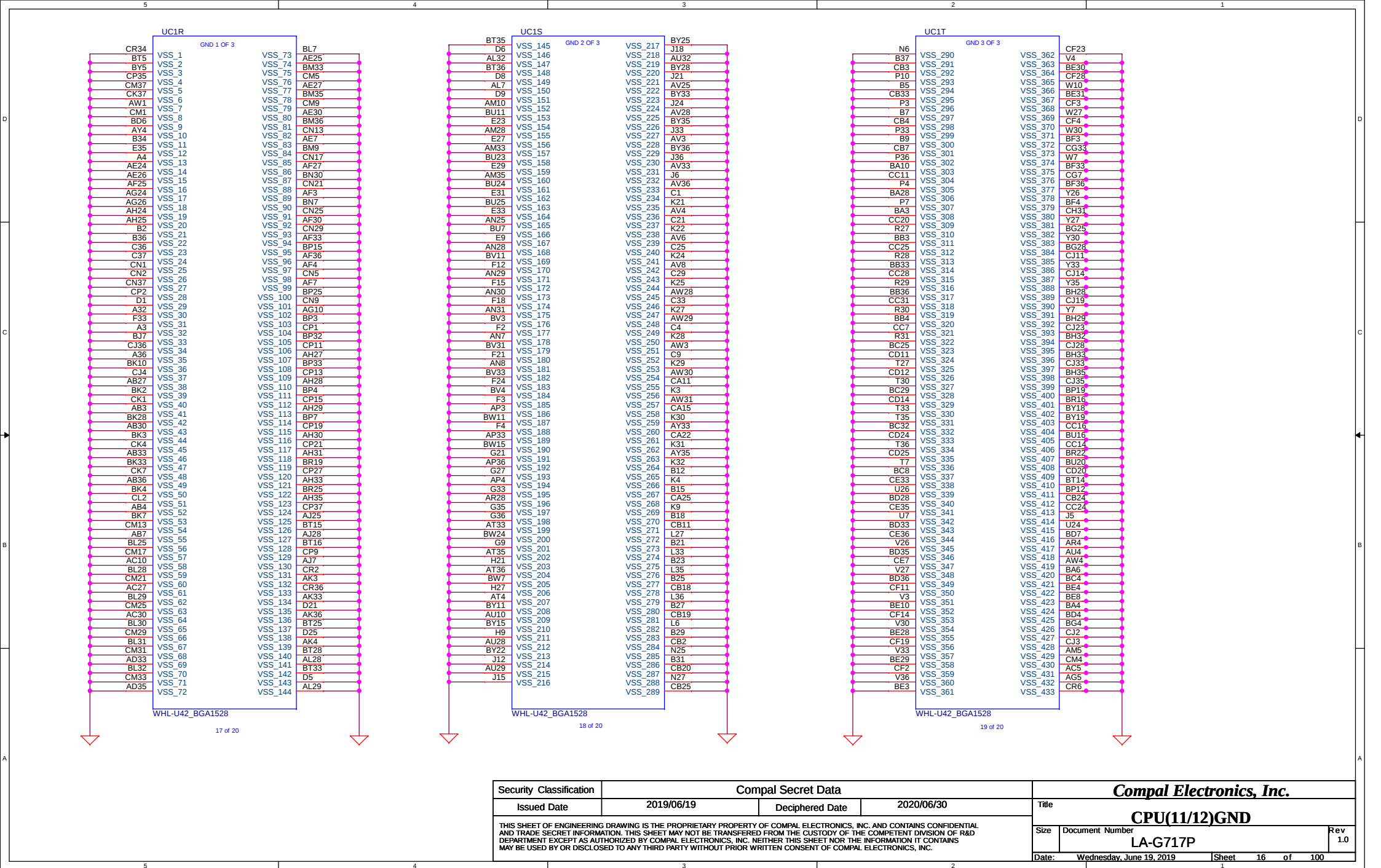
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								Size Custom	Document Number			LA-G717P			Rev 1.0
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								Size	Document Number		Rev	
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								Date: Wednesday, June 19, 2019		Sheet 13 of 100		



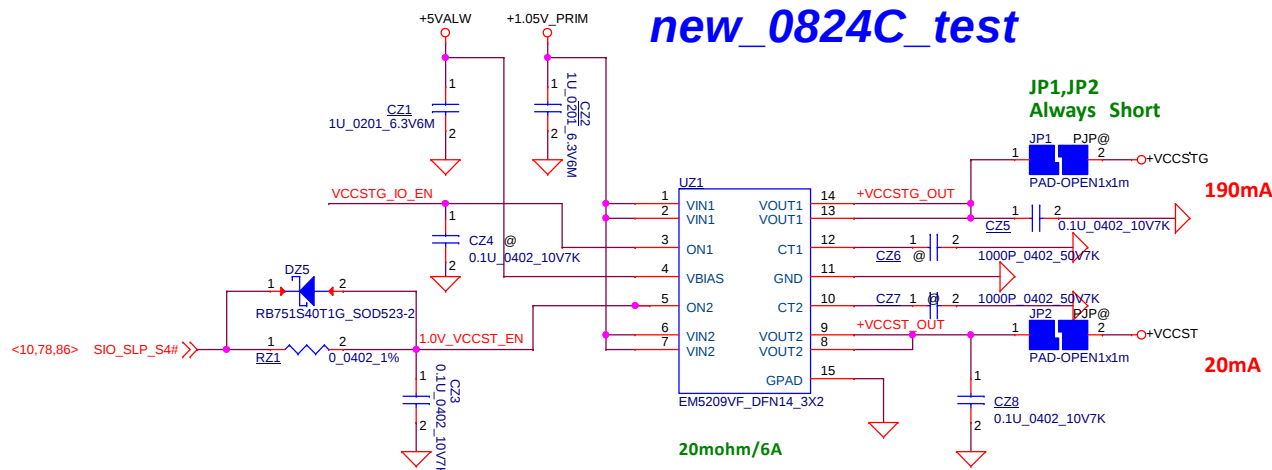




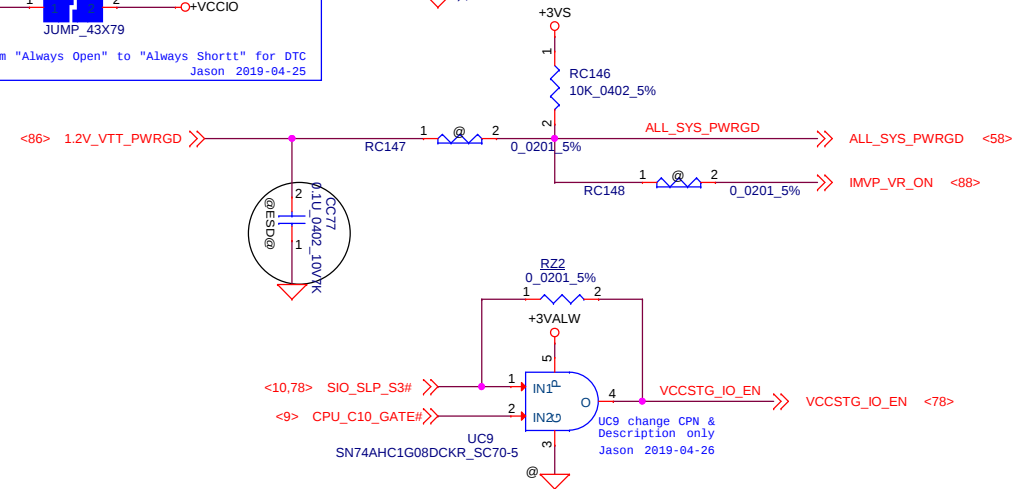
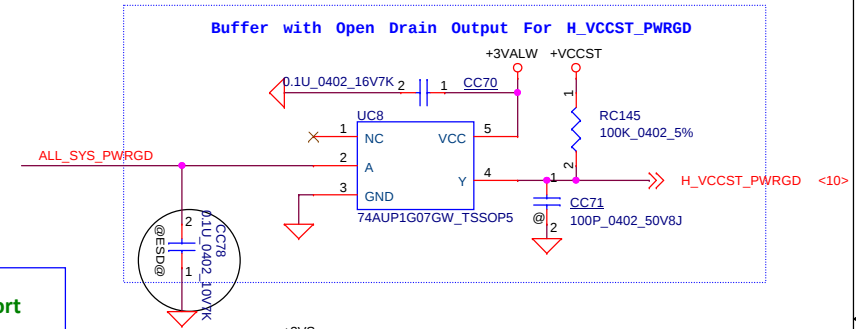
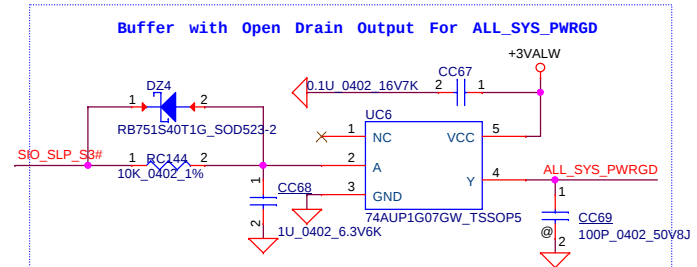
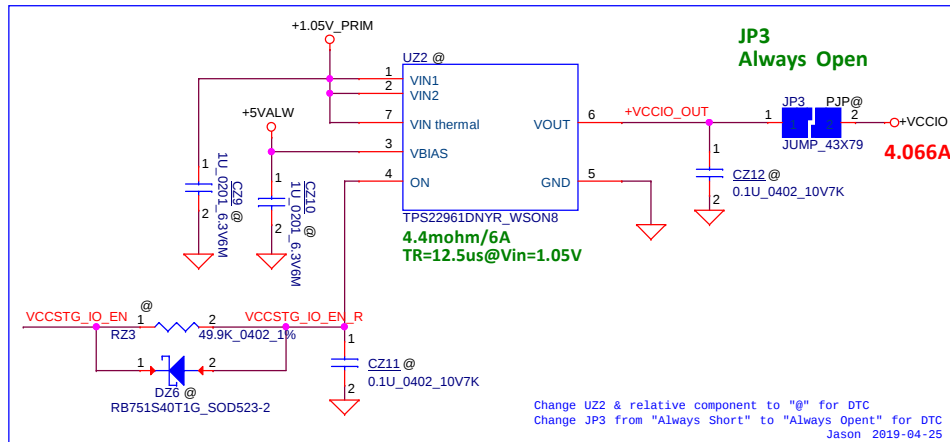
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		Size		Document Number		Rev			
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+1.05V_PRIM TO +VCCST /+VCCSTG

new_0824C_test



+1.05V_PRIM TO +VCCIO



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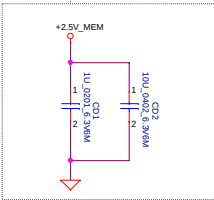
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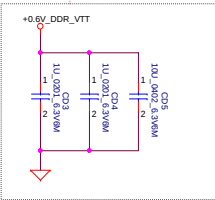
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Main Func = DDR

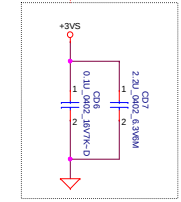
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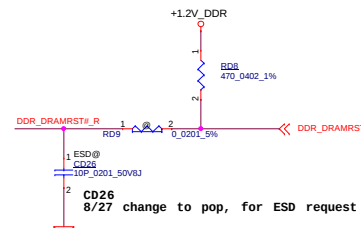
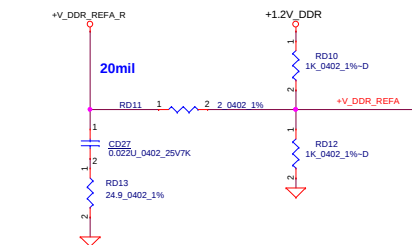
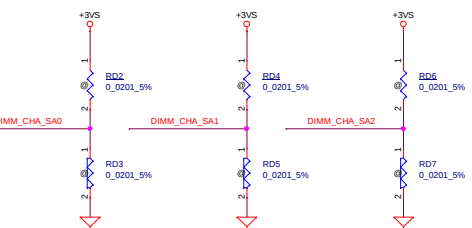
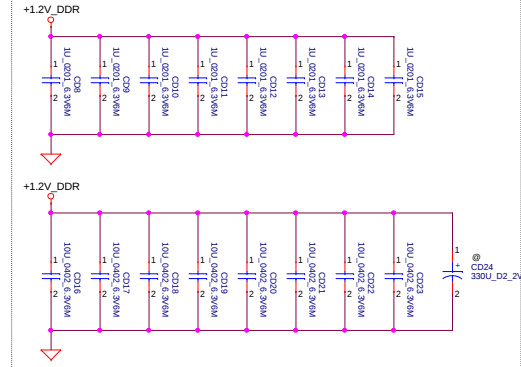
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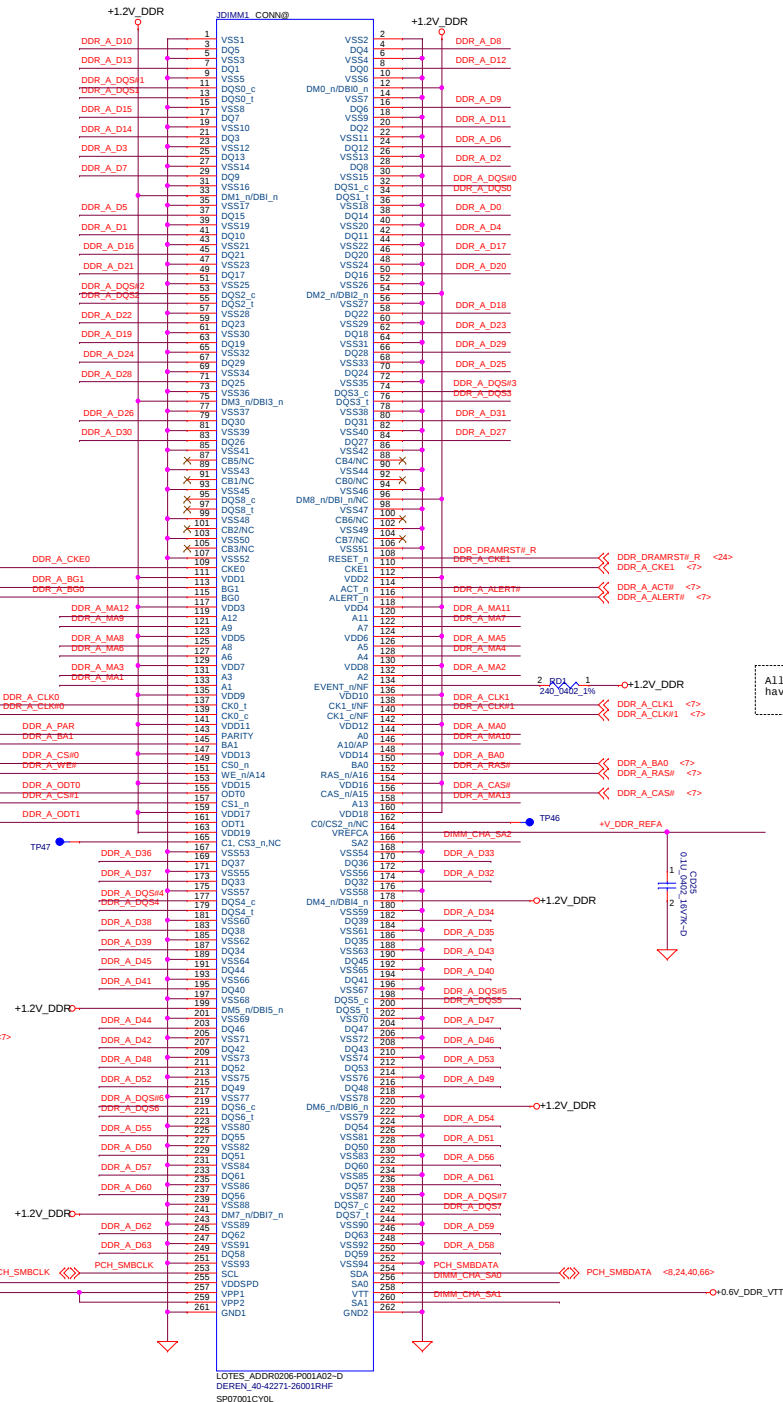
Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1



<7> DDR_A_D0..63
<7> DDR_A_MA0..13
<7> DDR_A_DQ50[0..7]
<7> DDR_A_DQ50[8..7]



All VREF traces should
have 10 mil trace width

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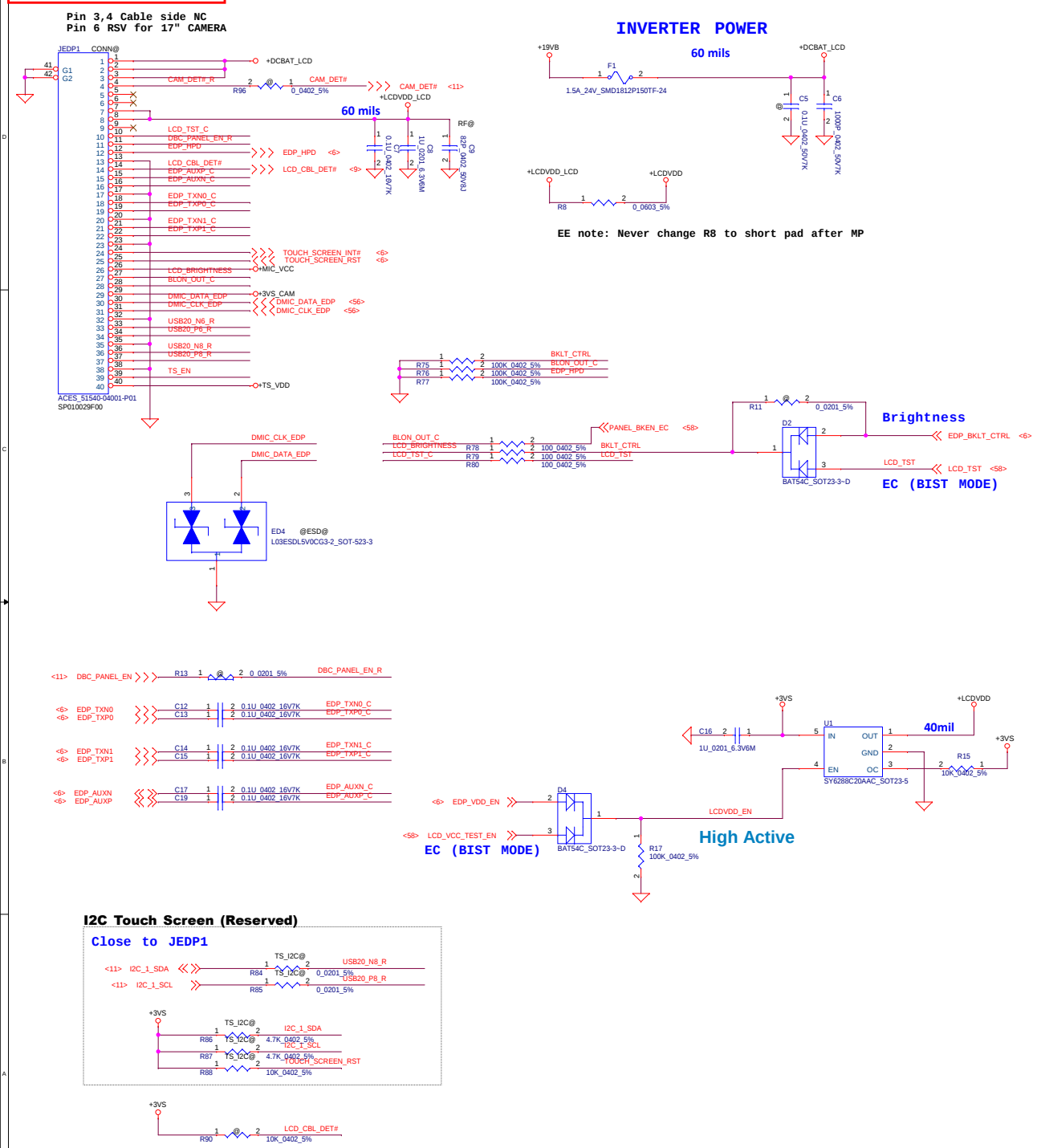
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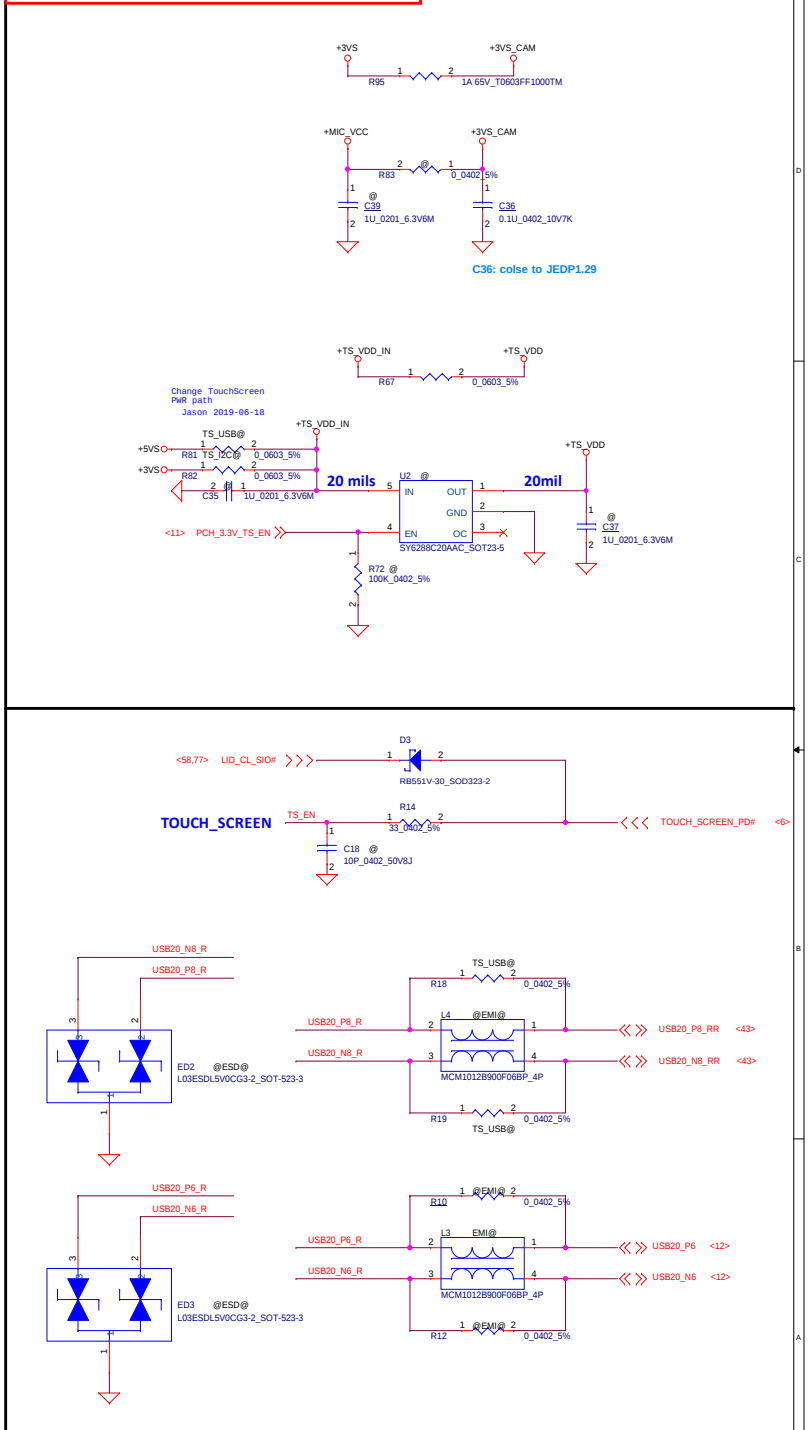
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Main Func = LCD



Main Func = CAM&MIC, TS



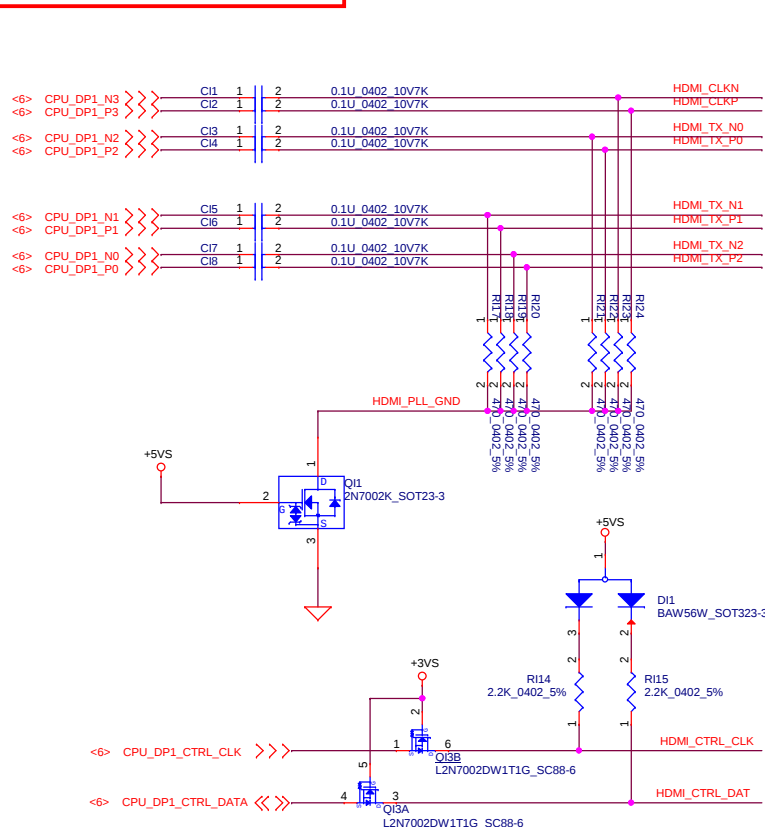
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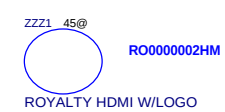
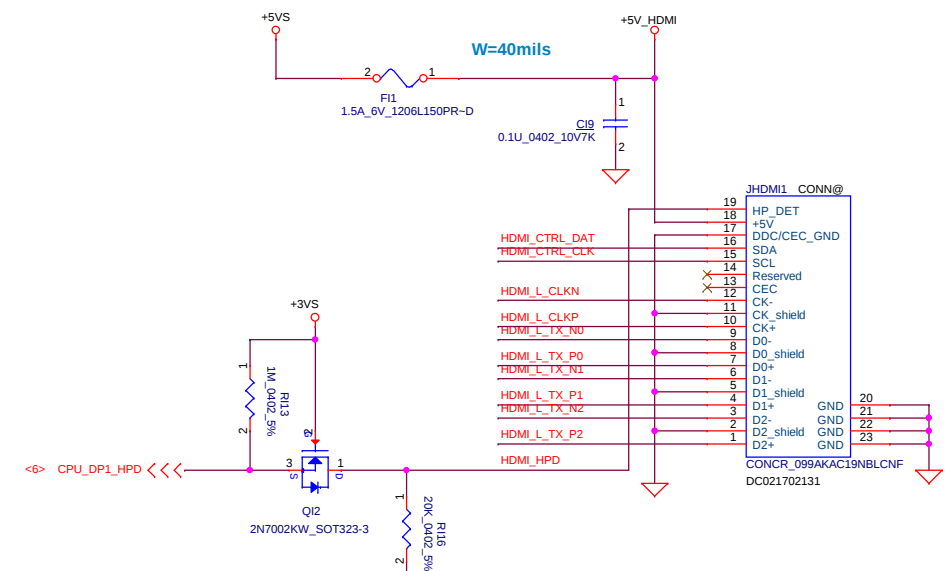
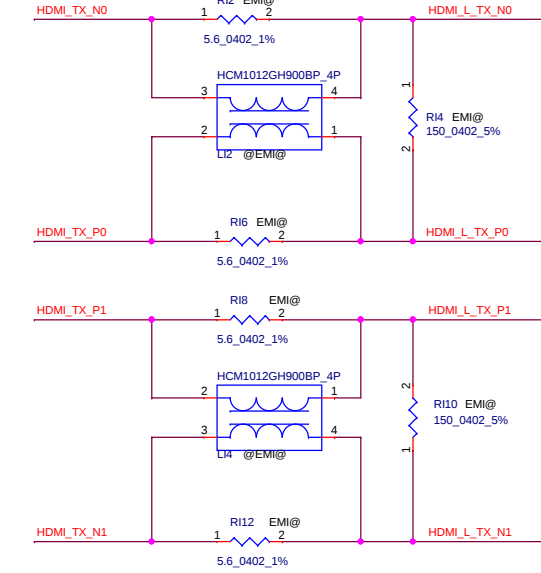
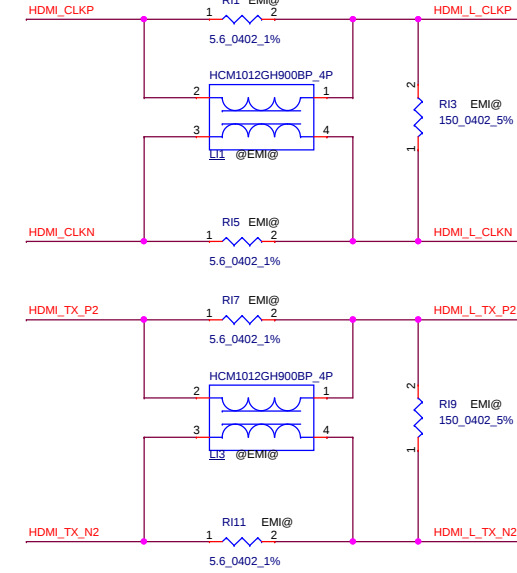
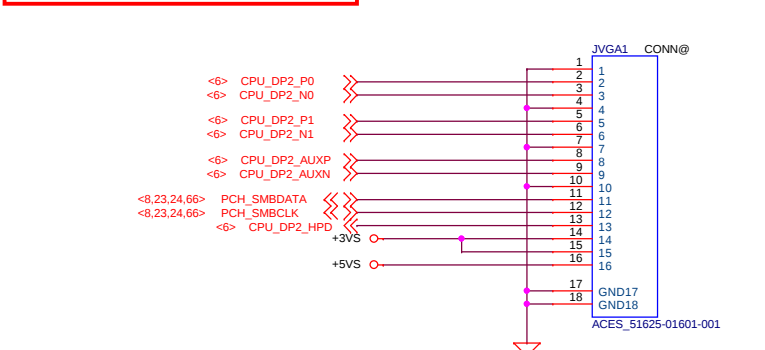
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				Date:	Wednesday, June 19, 2019	Sheet 39 of 100
				LA-G717P		1.0

Main Func = HDMI



Main Func = VGA



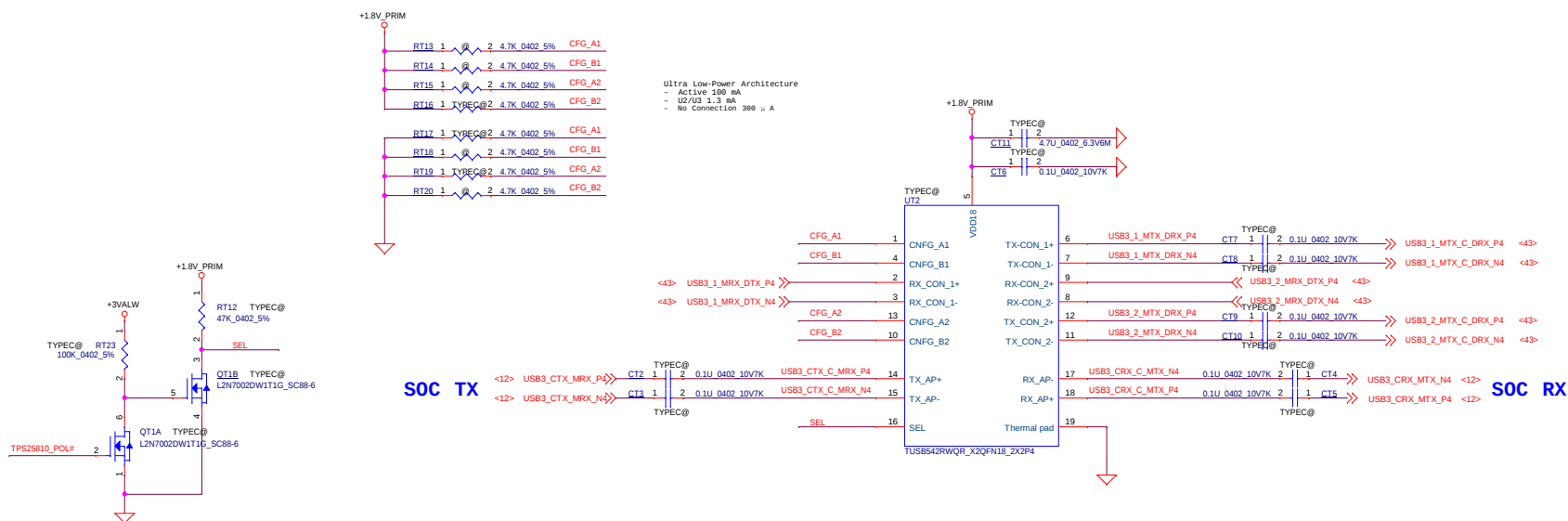
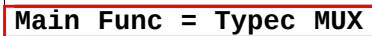
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						Size	Document Number		Rev	
							LA-G717P		1.0	
						Date:	Wednesday, June 19, 2019		Sheet	40 of 100

Main Function:

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5V@3A



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					LA-G717P	1.0
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					LA-G717P	1.0
Date:	Wednesday, June 19, 2019		Sheet	48	of	100

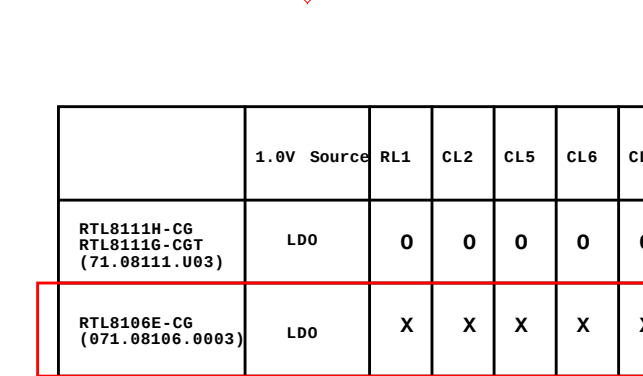
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					LA-G717P	1.0
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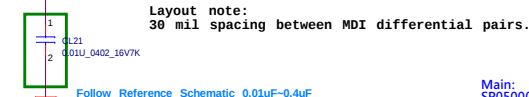
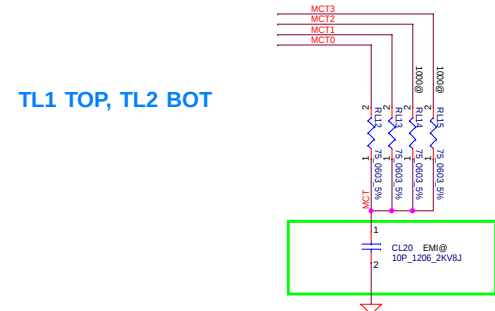
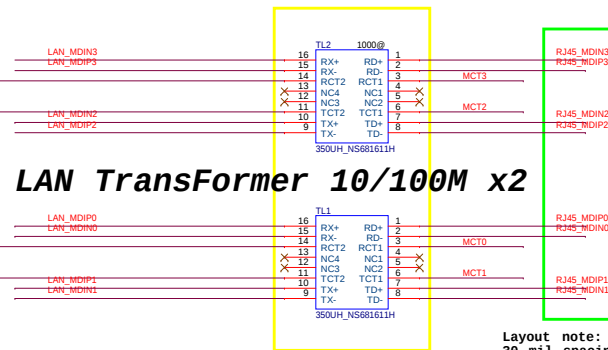
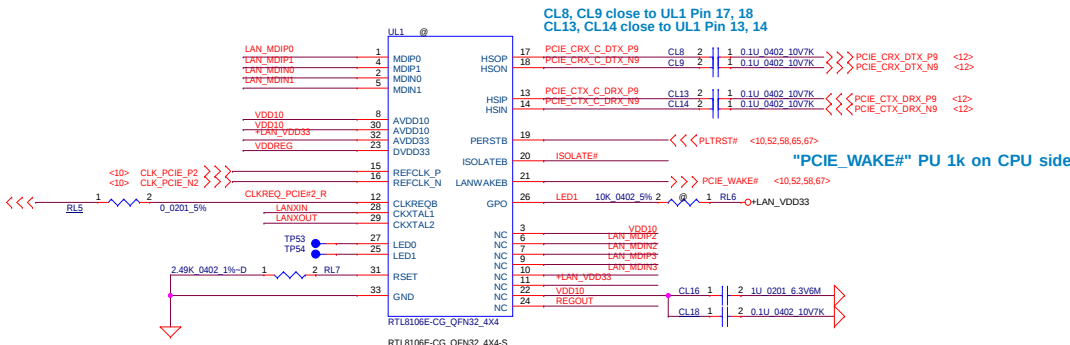
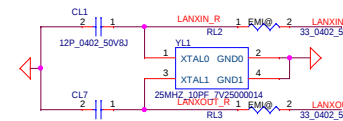
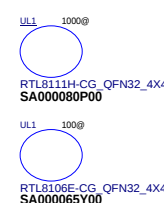
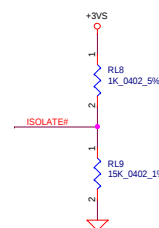
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					LA-G717P	1.0
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Main Func = LAN

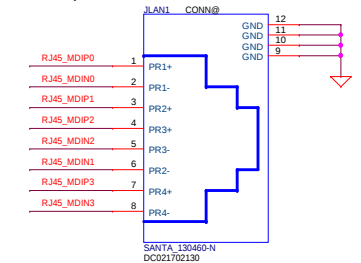
**LAN CHIP 10/100/1000**

RTL8111H-CG	RTL8106E-CG
SA000000P00	SA000005Y00
LDO mode	LDO mode
10/100/1000M	10/100M



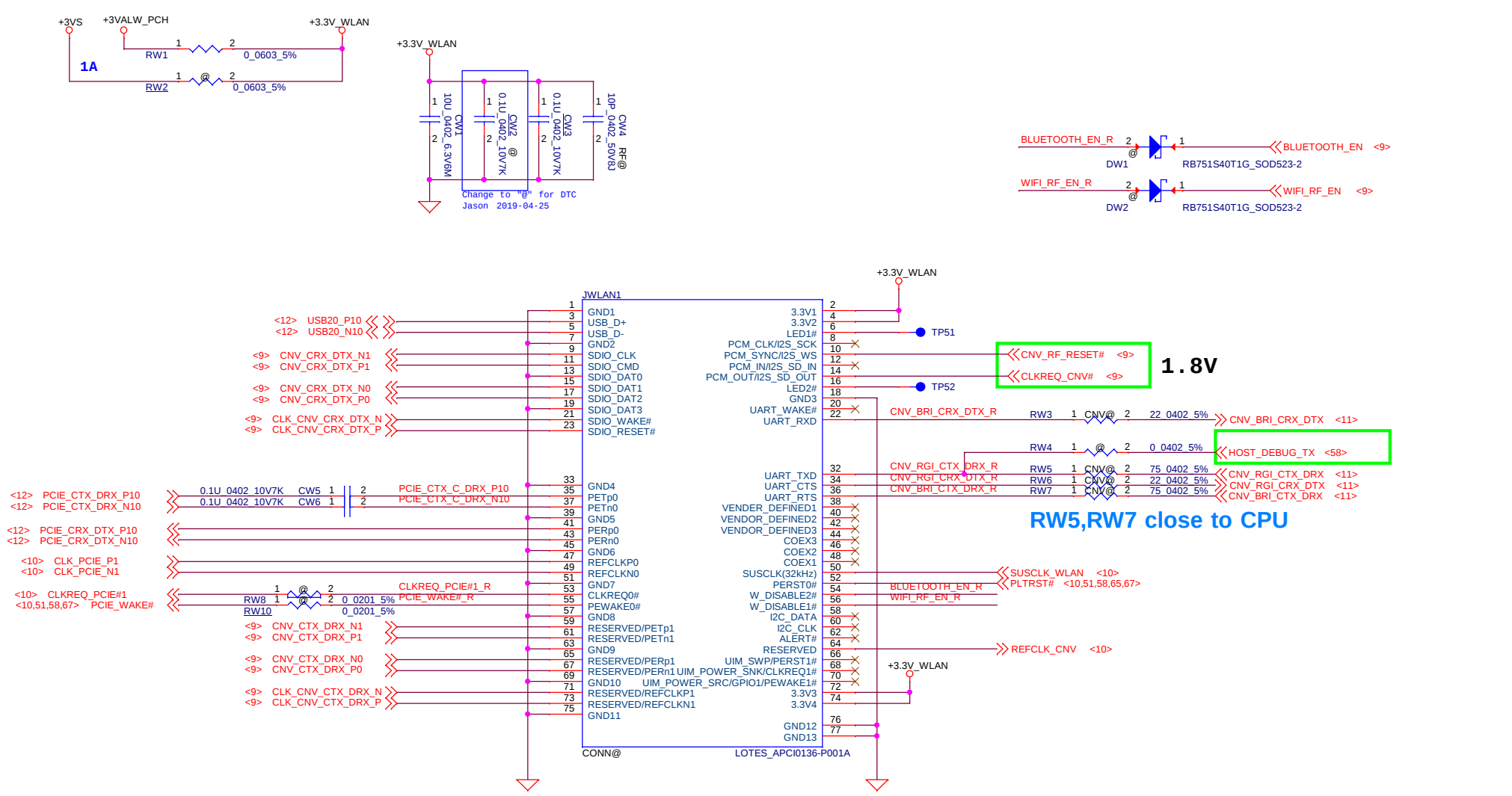
Main:
SP050006H00, S X'FORM_ NS0014 LF LAN
2nd:
SP050006W00, S X'FORM_ HD-245 10/100 PC CARD LAN

	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	0	0	0	0	0	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	0



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Main Func = WLAN E Key CONN



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Size		Document Number		Rev	
		LA-G717P		1.0	
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Main Function: WIGIG / WIDI

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					LA-G717P	1.0
Date:				Wednesday, June 19, 2019		
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Main Function:

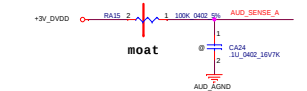
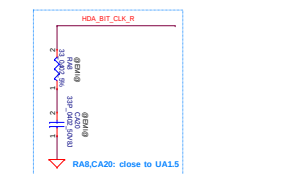
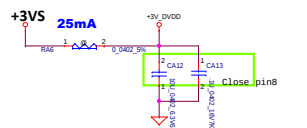
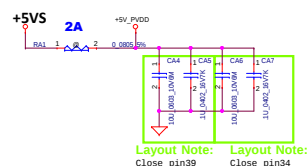
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					LA-G717P	1.0
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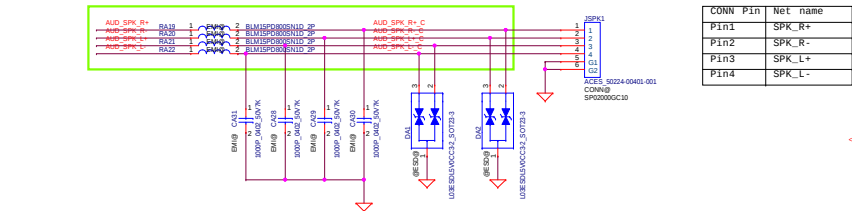
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					LA-G717P	1.0
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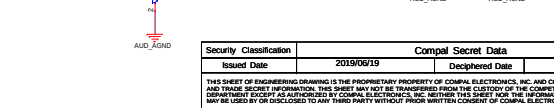
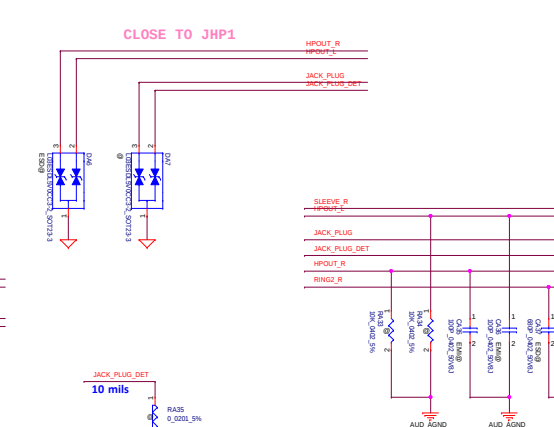
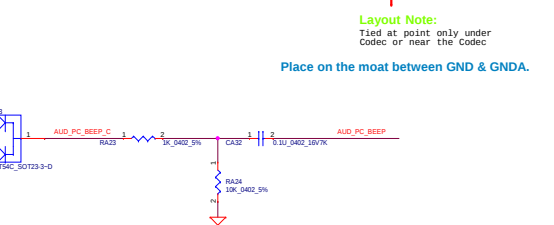
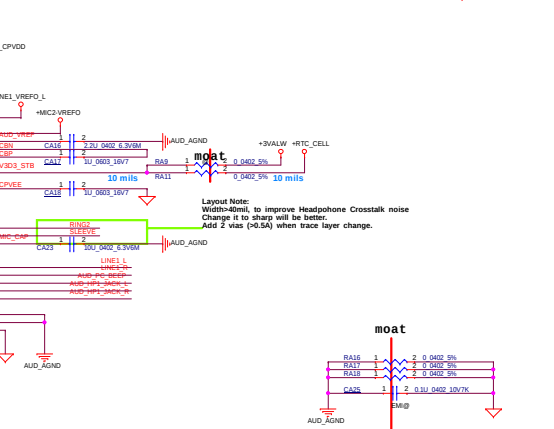
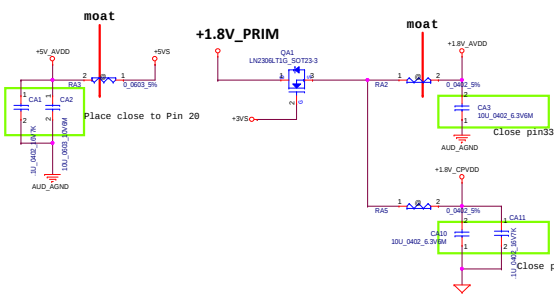
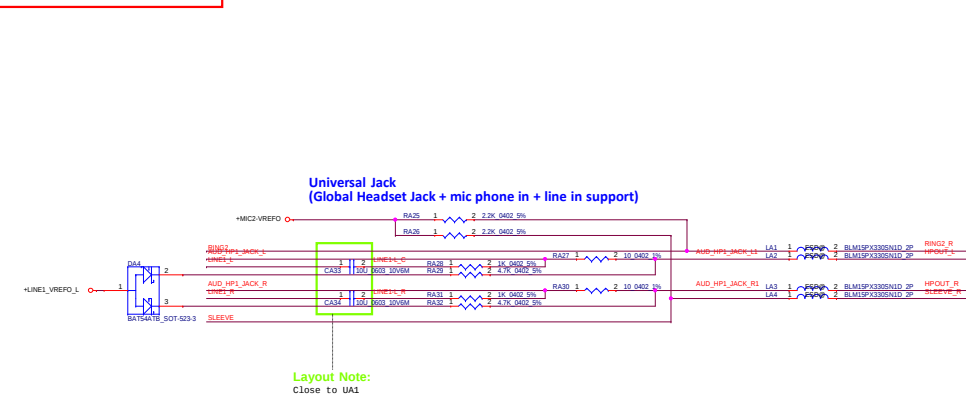


Layout Note: Speaker trace width >40mil @ 2W40hm speaker power



CONN Pin	Net name
Pin1	SPK_+
Pin2	SPK_+
Pin3	SPK_+
Pin4	SPK_+

Main Func = Audio Jack

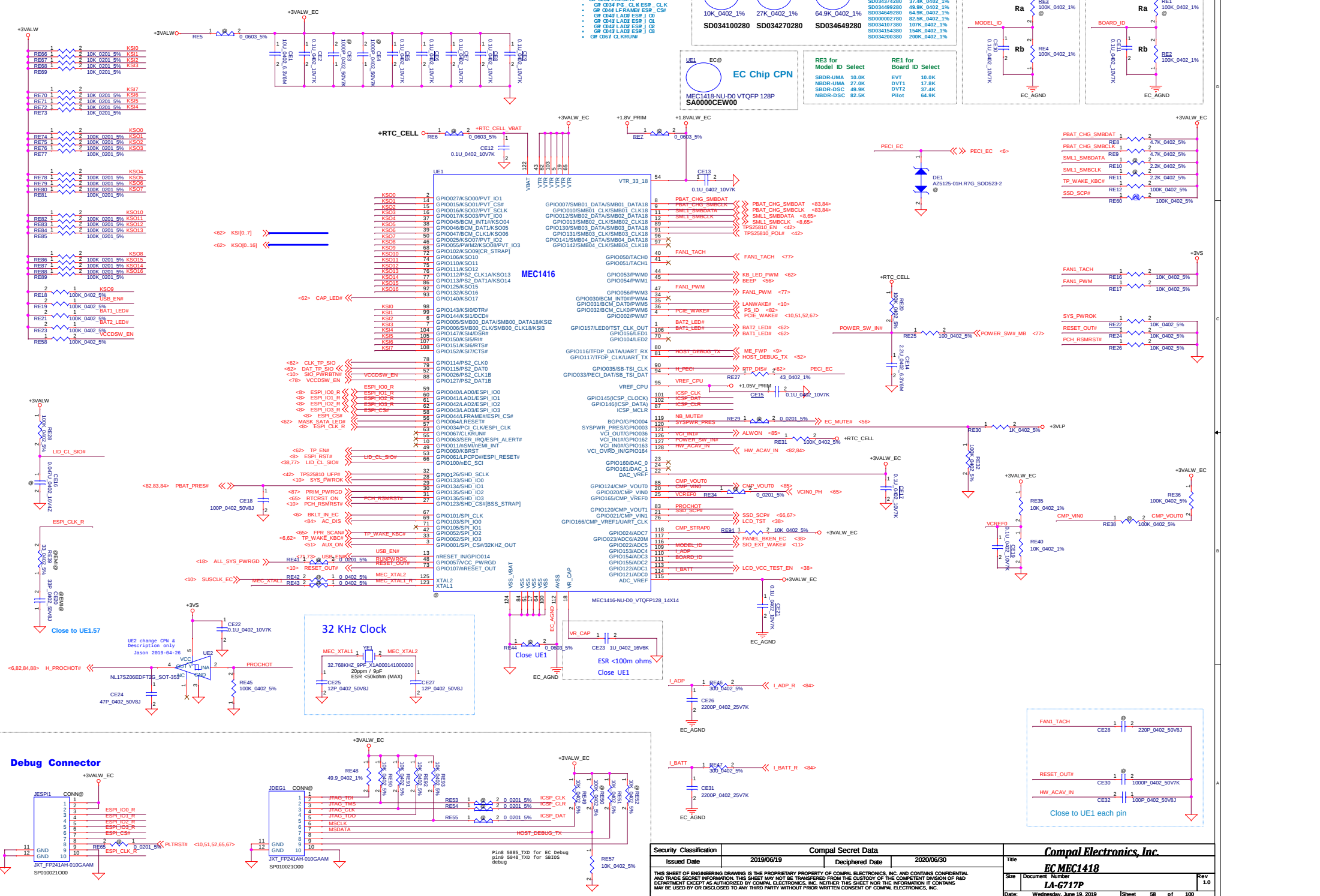


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Main Func = EC



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Title		Compal Electronics, Inc.	
EC MEC1418		Rev 1.0	
Size	Document Number	LA-671P	
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					LA-G717P	1.0
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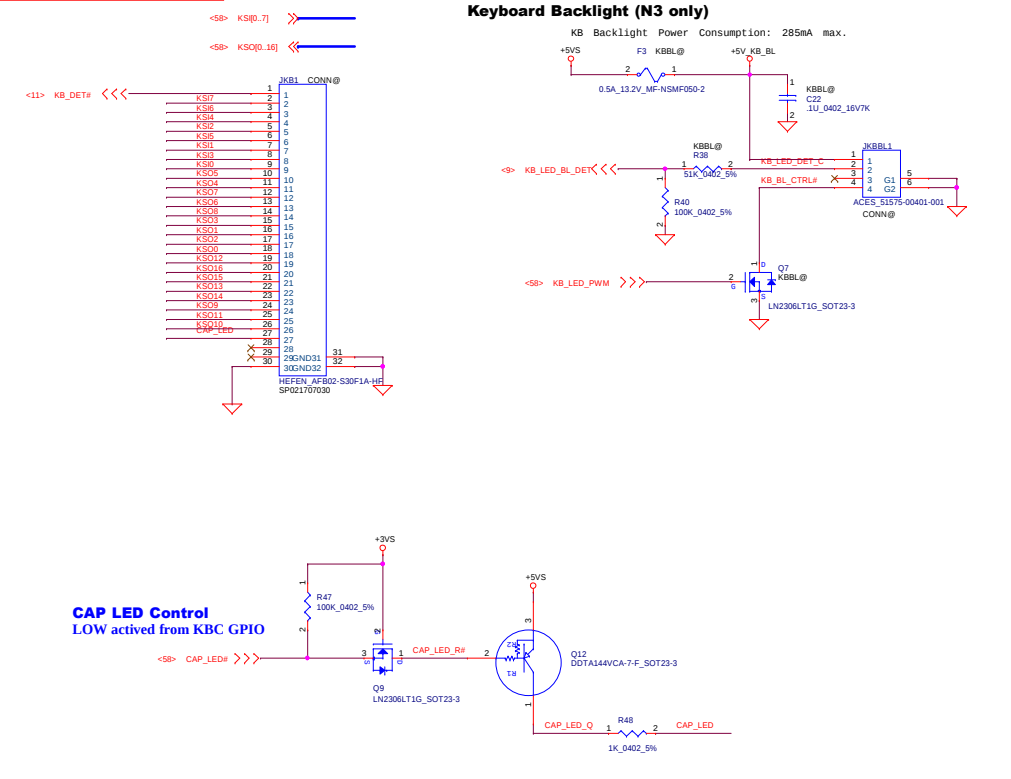
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					LA-G717P	1.0
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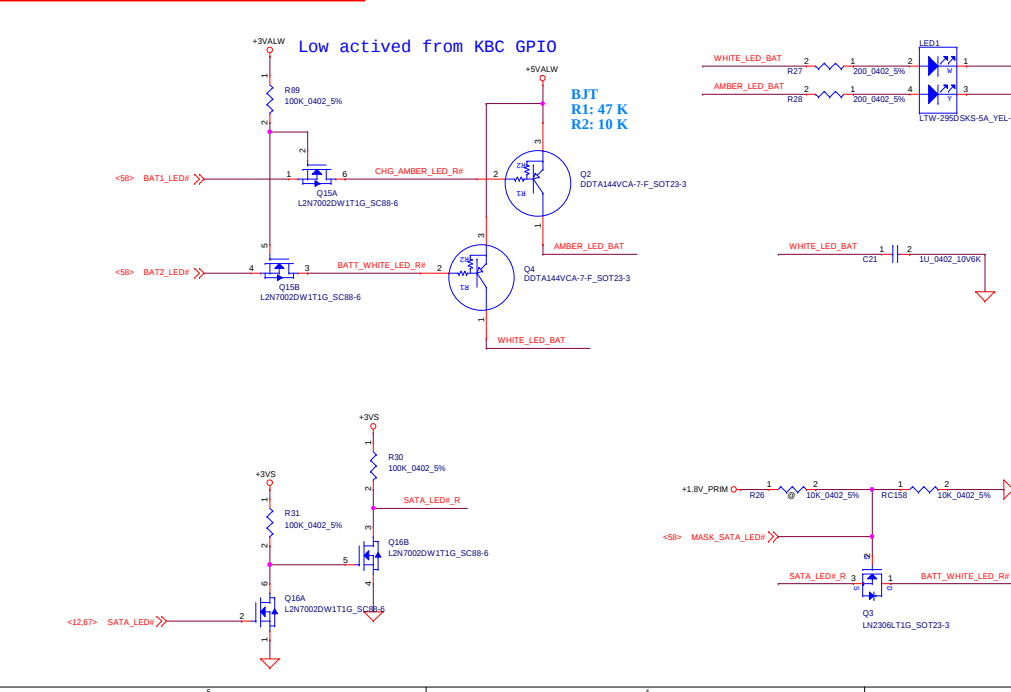
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				Date:	Wednesday, June 19, 2019	Sheet 61 of 100
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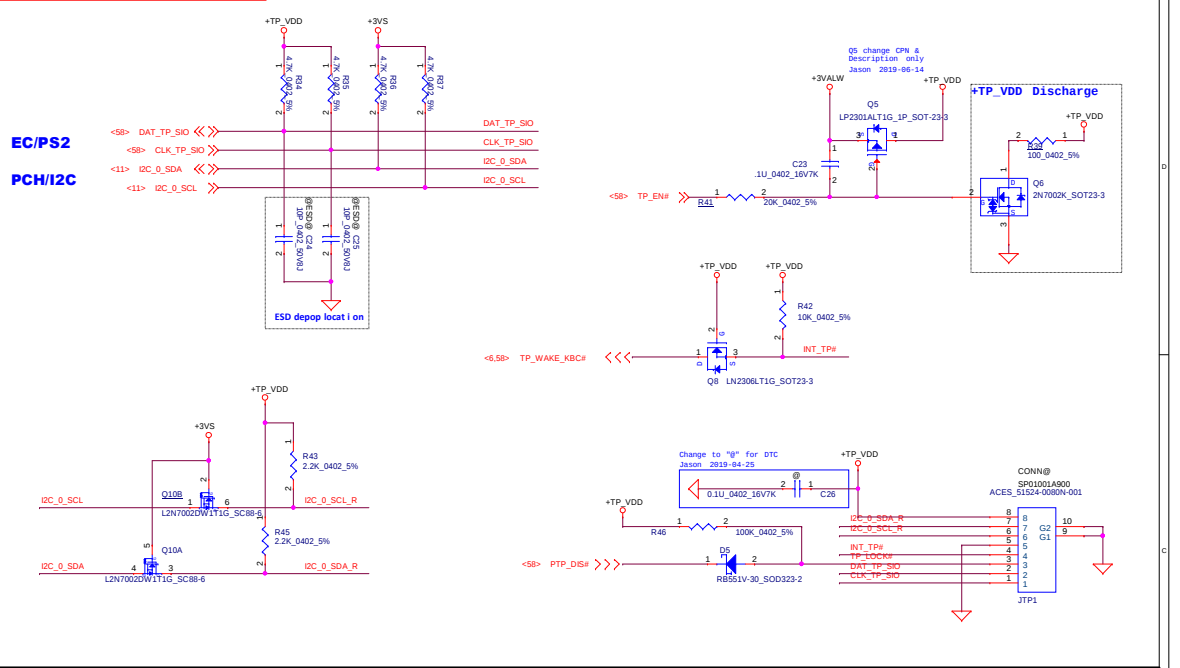
Main Func = KB



Main Func = Battery LED



Main Func = TPAD



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Main Function:

Reserved

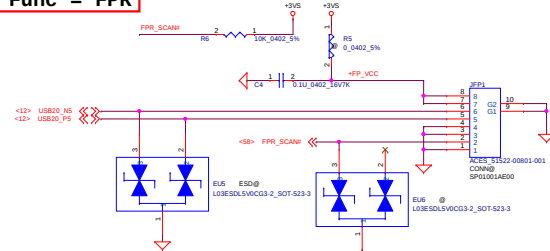
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	Reserved	
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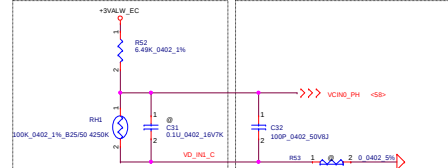
Main Func = FPF



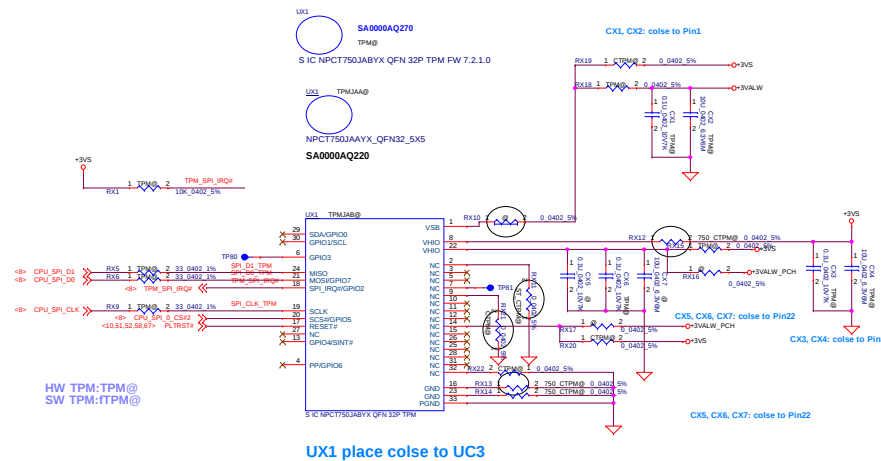
Main Func = OTP

Put below CPU

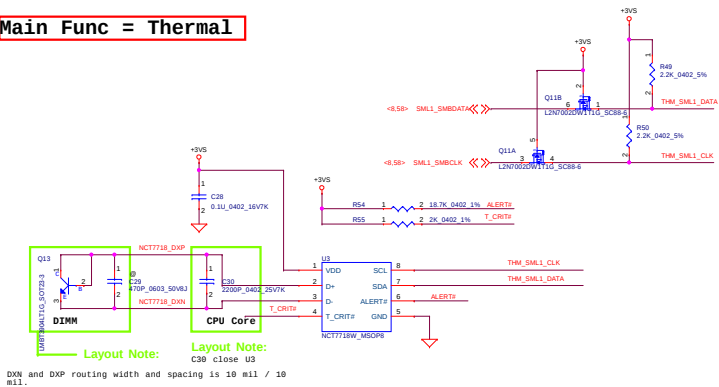
Close to KBC
CMP_VIN0 for system thermal sensor



Main Func = TPM

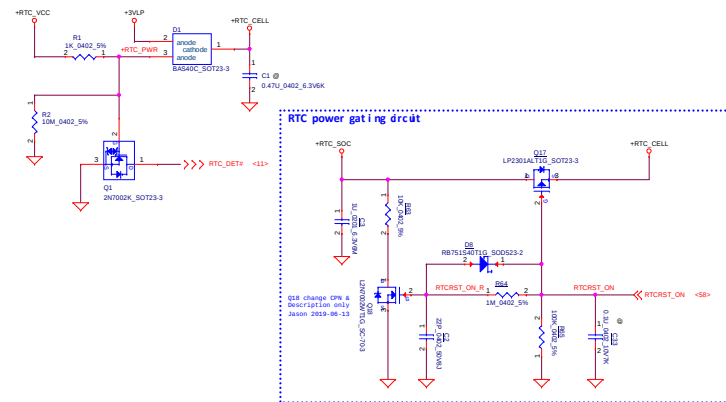


Main Func = Thermal

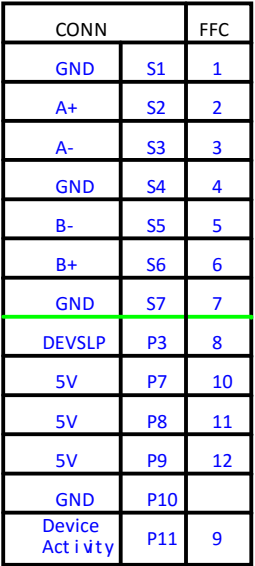


TEMPERATURE [°C]		T_CRST#				
		2KG	7.5KG	10.5KG	14KG	18.7KG
ALERT#	2KG	77	87	97	107	117
	7.5KG	79	89	99	109	119
	10.5KG	81	91	101	111	121
	14KG	83	93	103	113	123
	18.7KG	85	95	105	115	125

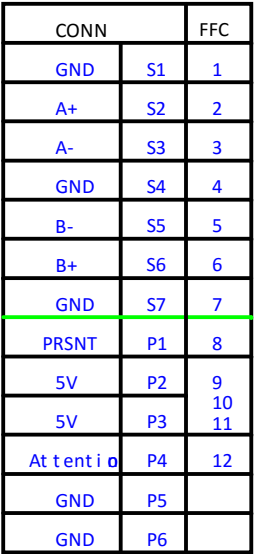
Main Func = RTC

[illegible]

Main Func = HDD&FFS



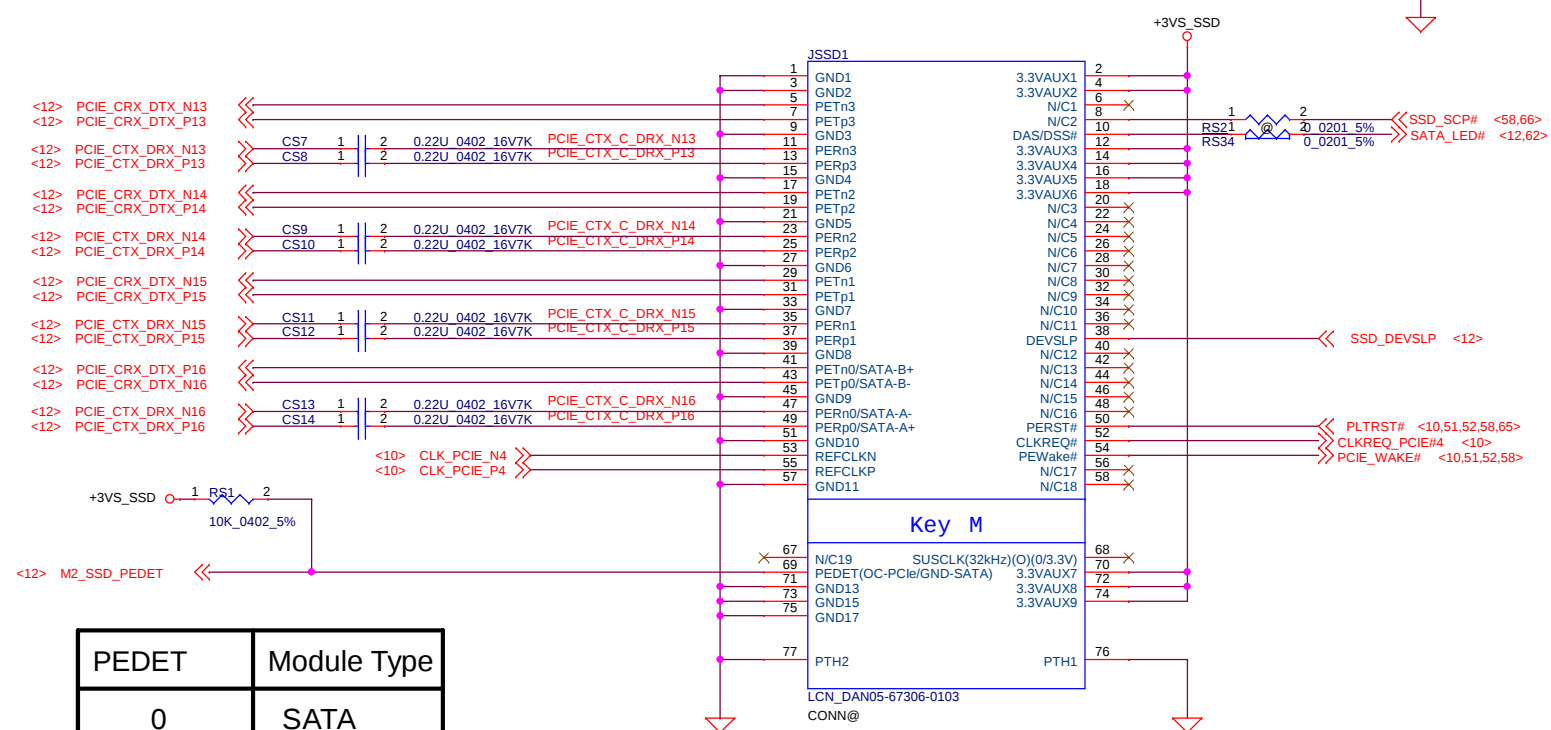
Main Func = ODD



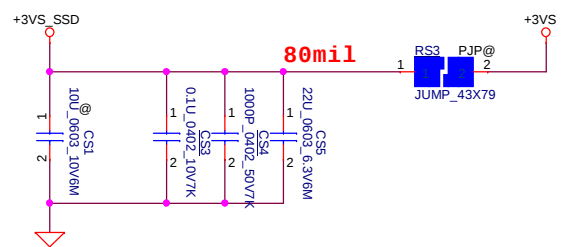
Security Classification	Compal Secret Data			Compal Electronics, Inc. HDD/FFS/ODD	
Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	
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Main Func = SSD M Key CONN

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIe

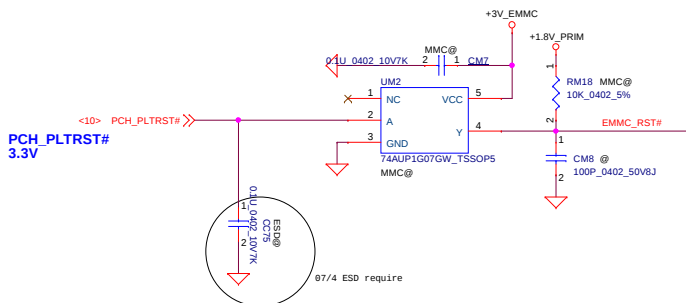
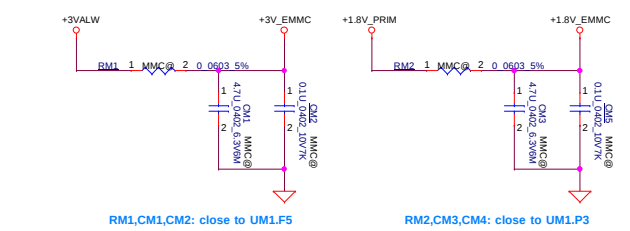
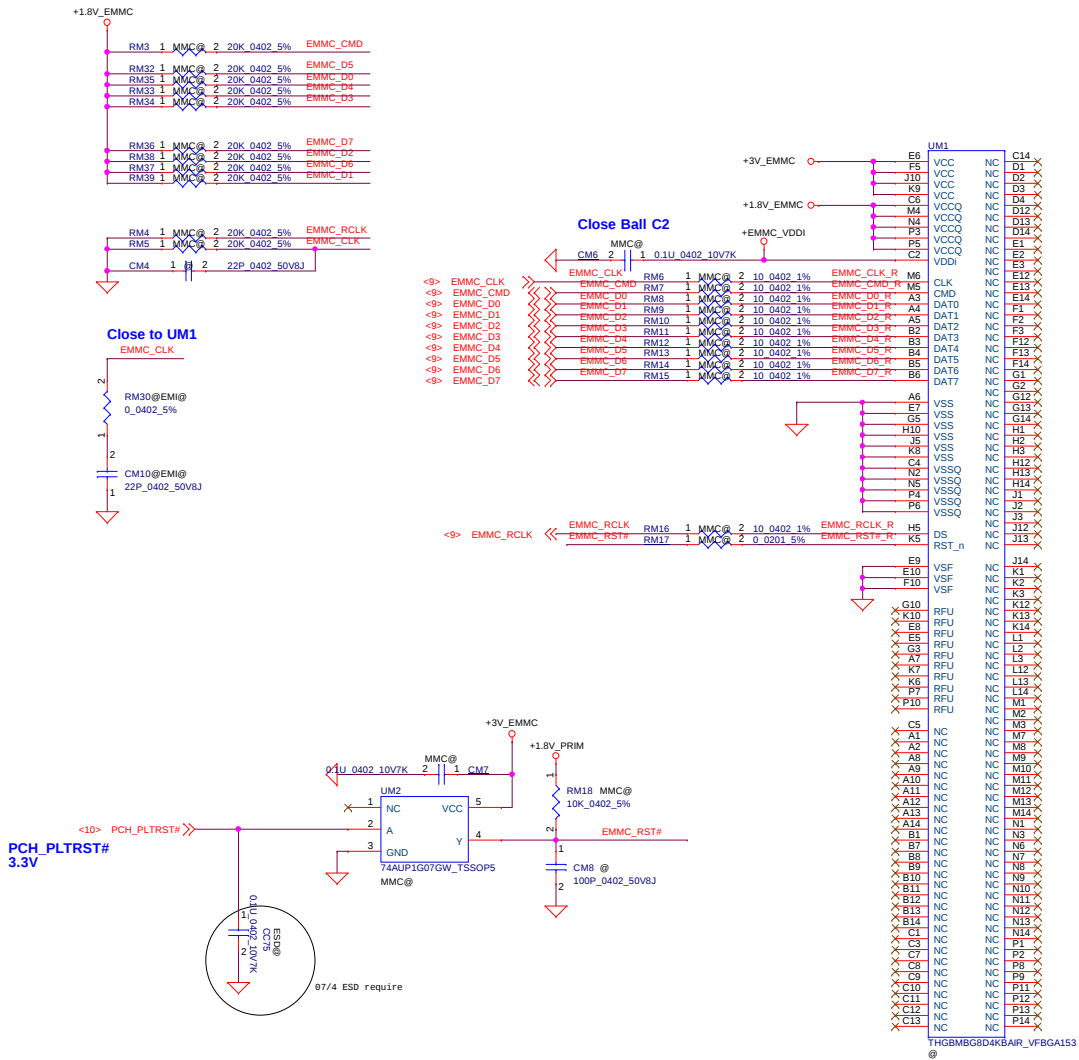


Main Function:

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Main Func = eMMC



UM1
HYNIX
SA00009N50L
HYNIX_128G@
S IC FL 128G H26M88002AMR FBGA 153P
SA00009N50L, S IC FL 256G H28S90302BMR FBGA 153P, A.2 (Design)

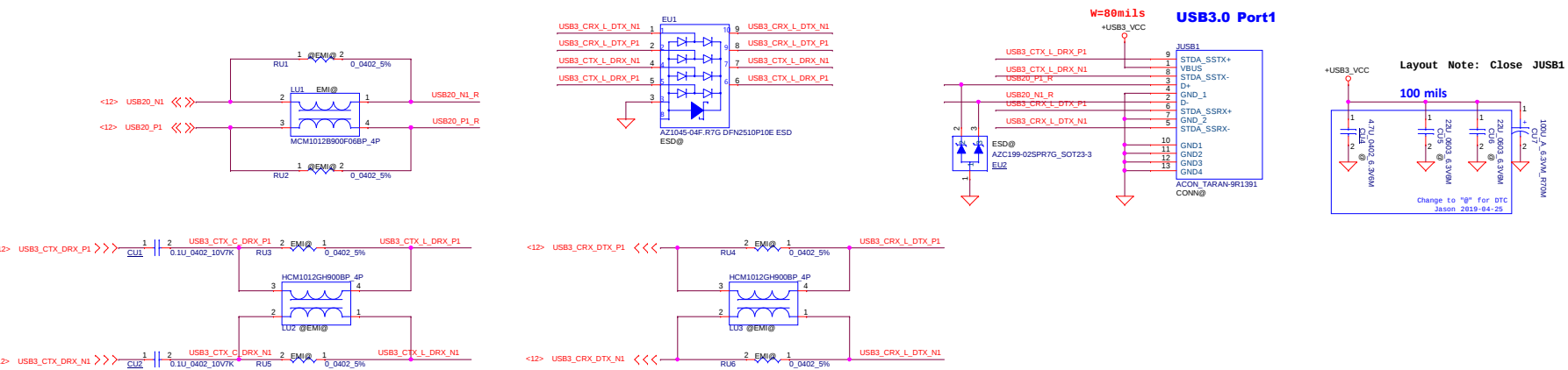
Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2019/06/19	Deciphered Date	2020/06/30	eMMC		Rev
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				Date:	Wednesday, June 19, 2019	Sheet 69 of 100

Main Function:

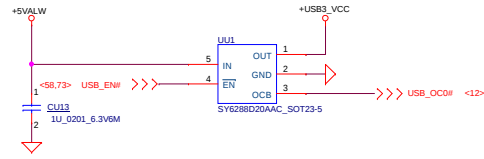
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					LA-G717P	1.0
Date: Wednesday, June 19, 2019				Sheet	70 of 100	

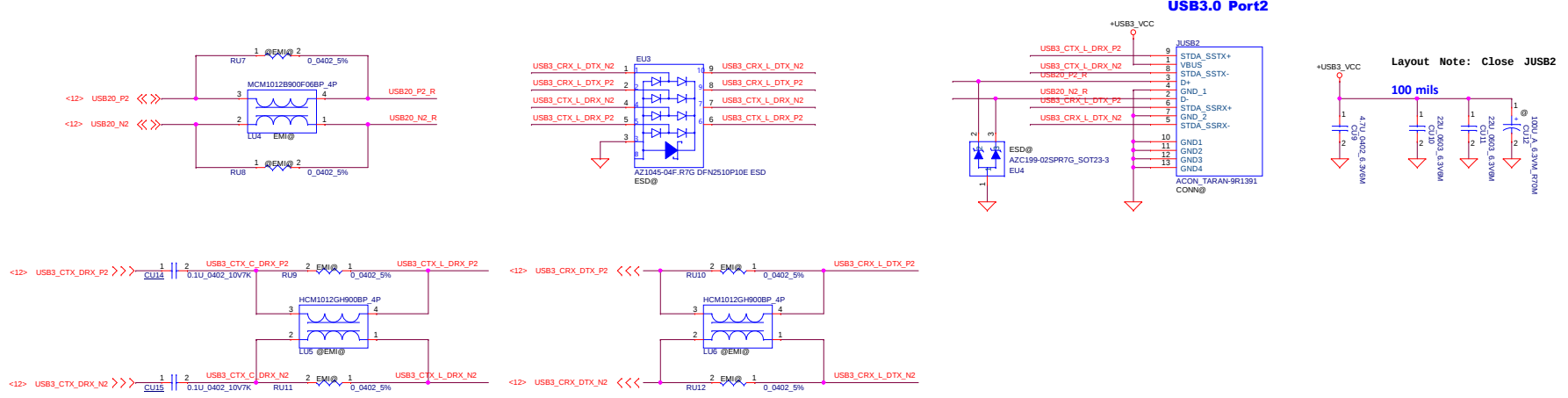
Main Func = USB3.0 Port1



Maximum Output Current 2A



Main Func = USB3.0 Port2



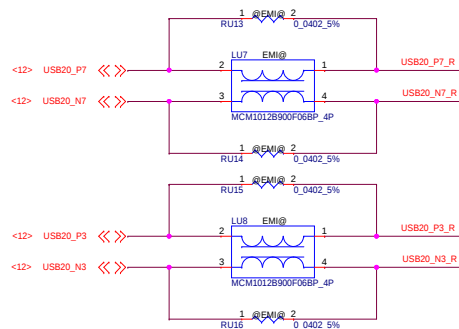
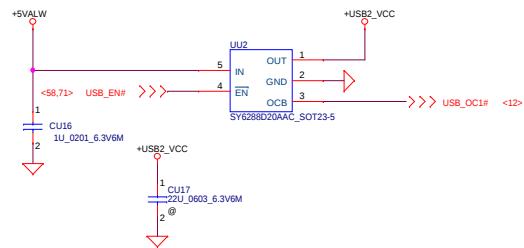
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Size	Document	Number	Rev	LA-G717P	
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Main Function:

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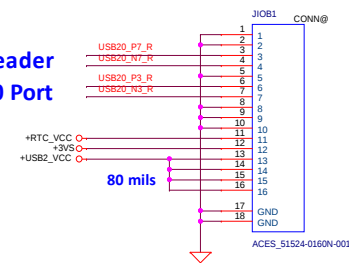
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Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	Reserved	
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Main Func = USB2.0 Port3 + Card Reader on I/O/B



USB2.0/Card Reader connector

CardReader
USB2.0 Port



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					LA-C717P	1.0
				Date:	Wednesday, June 18, 2019	Sheet 73 of 100

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					LA-G717P	1.0
Date: Wednesday, June 19, 2019				Sheet	74 of 100	

Main Function:

Reserved

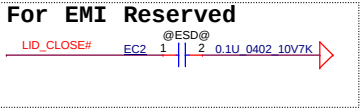
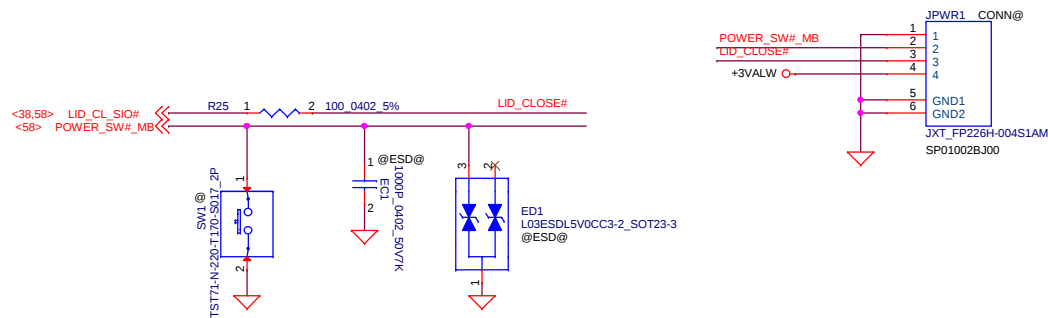
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title	Reserved	
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					LA-G717P	1.0
Date:	Wednesday, June 19, 2019			Sheet	75	of 100

Main Function:

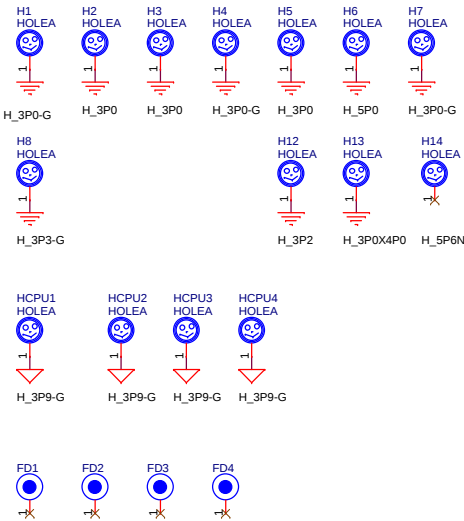
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					LA-G717P	1.0
				Date:	Wednesday, June 19, 2019	Sheet 76 of 100

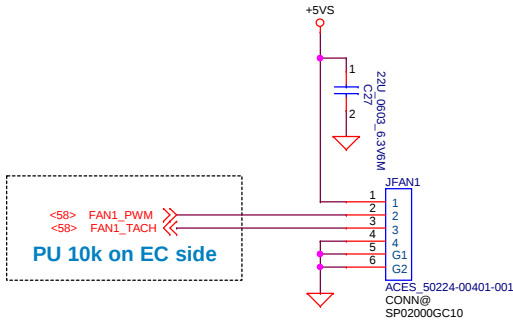
Main Func = Power BTN Low activated from KBC GPIO



Screw hole/FD

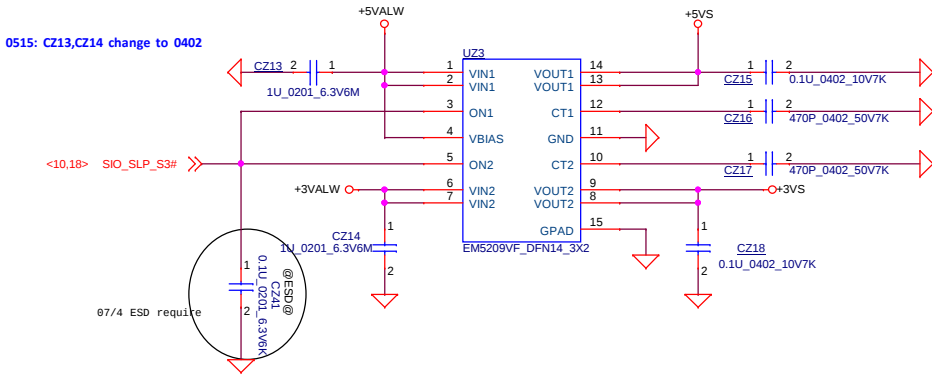


FAN

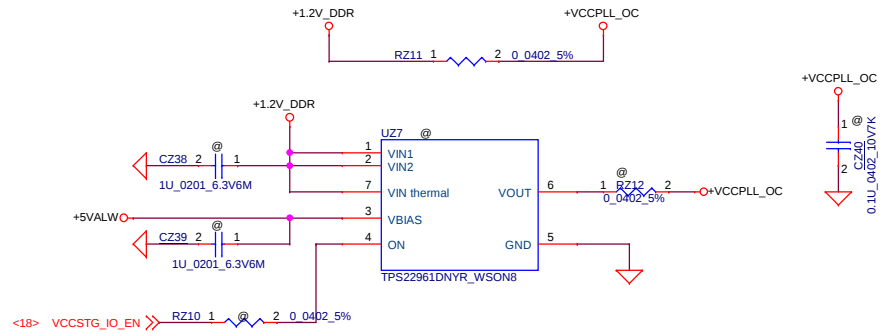


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				Size	Document Number	Rev
					LA-G717P	1.0
Date: Wednesday, June 19, 2019				Sheet	77	of 100

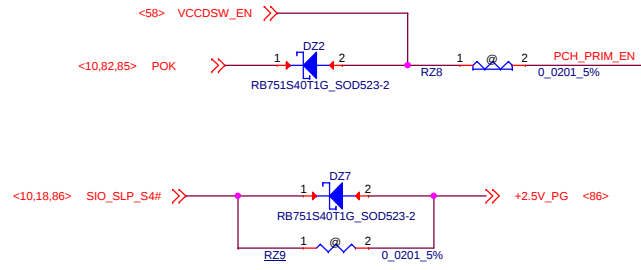
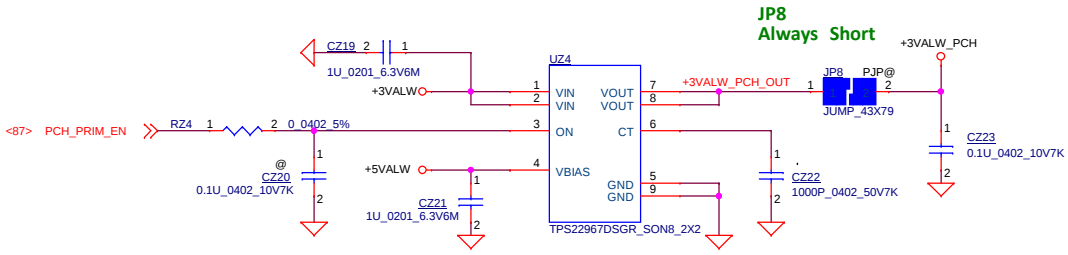
+5VS/+3VS for System



+VCCPLL_OC source



+3VALW_PCH for System



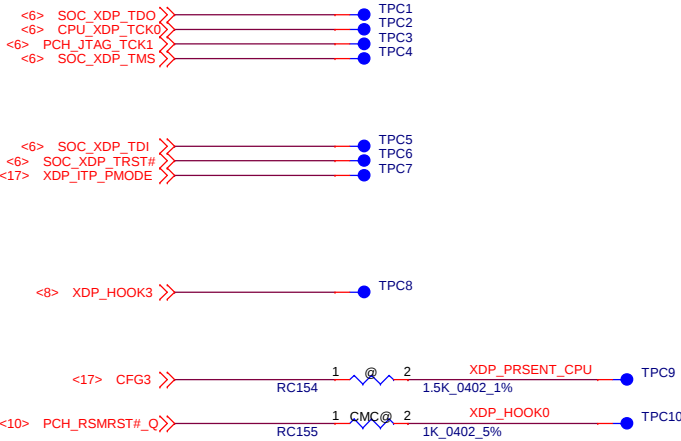
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2019/06/19	Deciphered Date	2020/06/30	Title		
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PortConnector Less Routing Topology

Follow KBL DCI Link
RC152 need POP
RC156 need POP

Place to CPU side

Place to CPU side



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				Size	Document Number	Rev
				B	LA-G717P	1.0
				Date:	Wednesday, June 19, 2019	Sheet 79 of 100

Main Func = Power Monitor

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								Size	Document Number		Rev	
								LA-G717P		1.0		
								Date:		Wednesday, June 19, 2019		Sheet

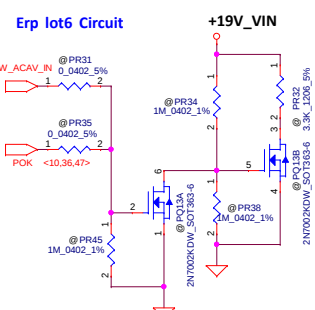
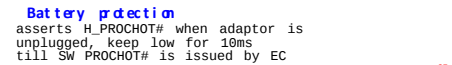
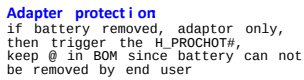
Reserve

DELL CONFIDENTIAL/PROPRIETARY

		Compal Electronics, Inc.	
Title		Reserve for PWR	
Size	Document Number		Rev 1.0
Date: Wednesday, June 19, 2019		Sheet 81 of	100

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A	B	C	D
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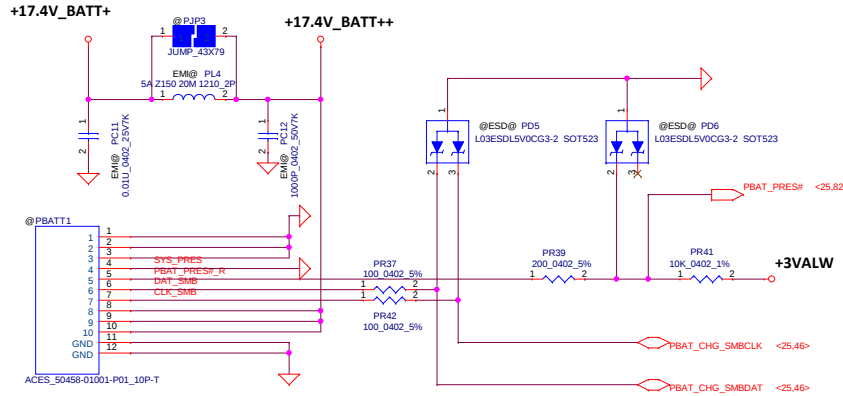
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Main Func = BATT CONN

Bat tery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

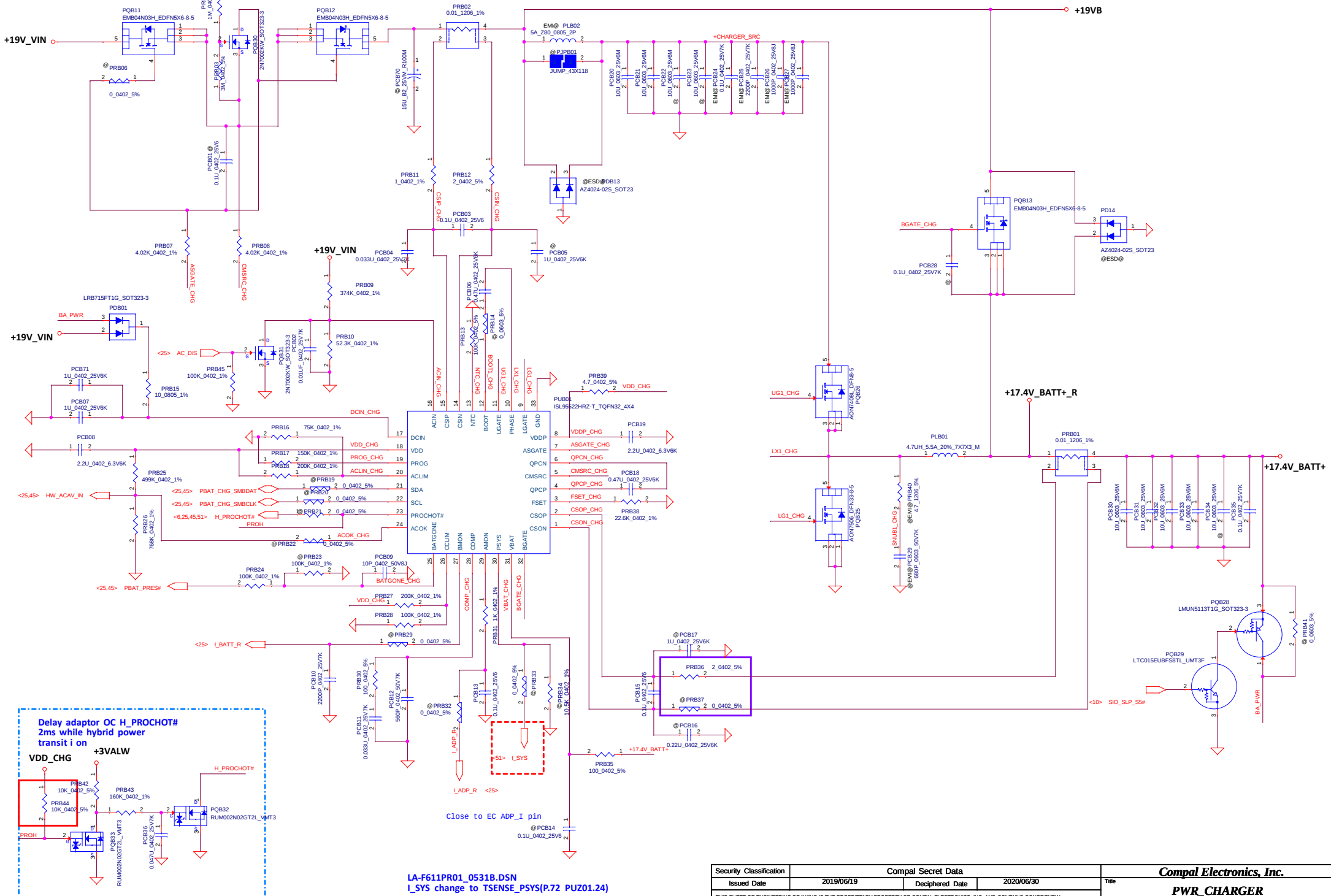
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DELL CONFIDENTIAL/PROPRIETARY

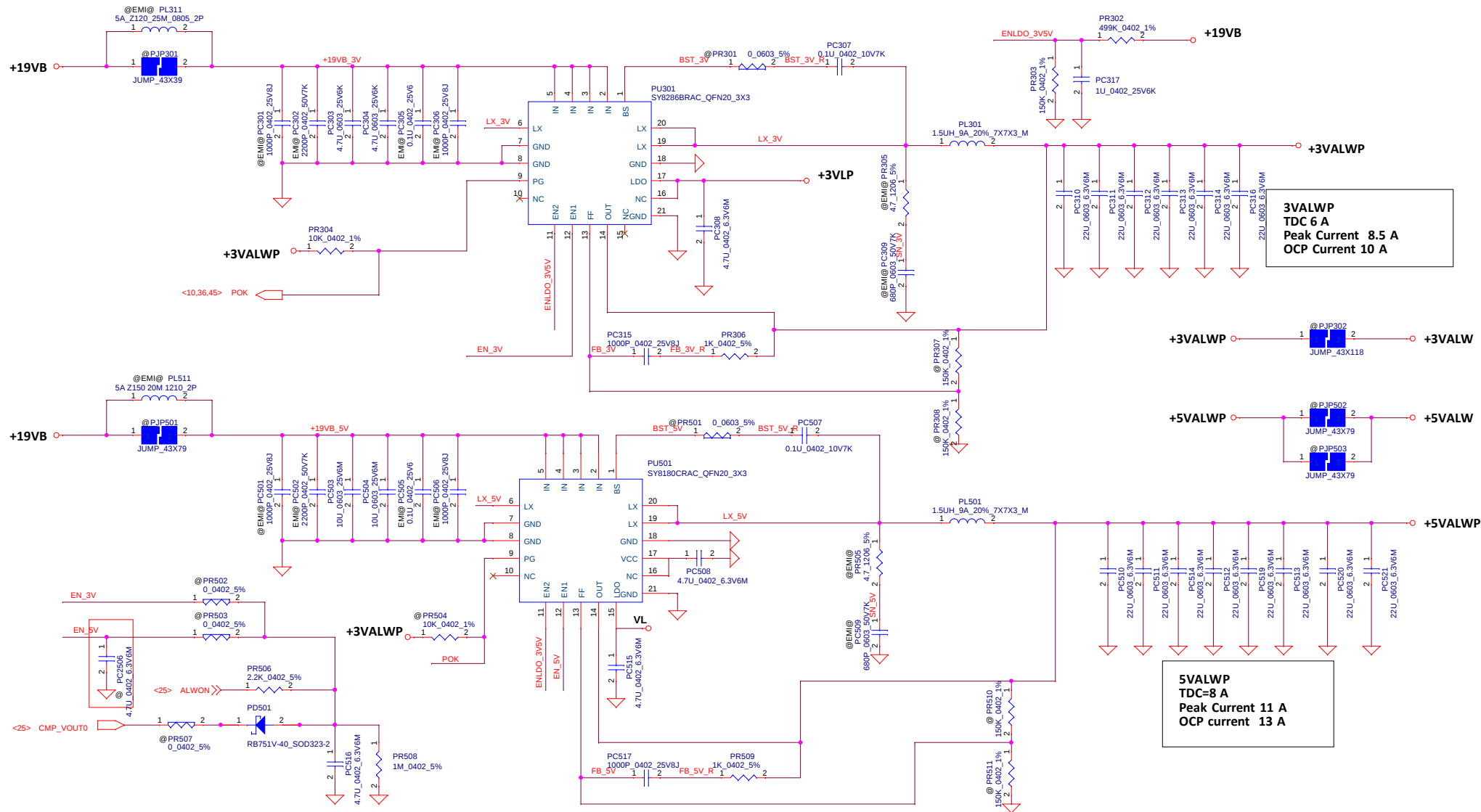
Security Classification		Compal Secret Data		Title	
Issued Date	2019/06/19	Deciphered Date	2020/06/30	PWR_BATT CONN	
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Main Func = CHARGER



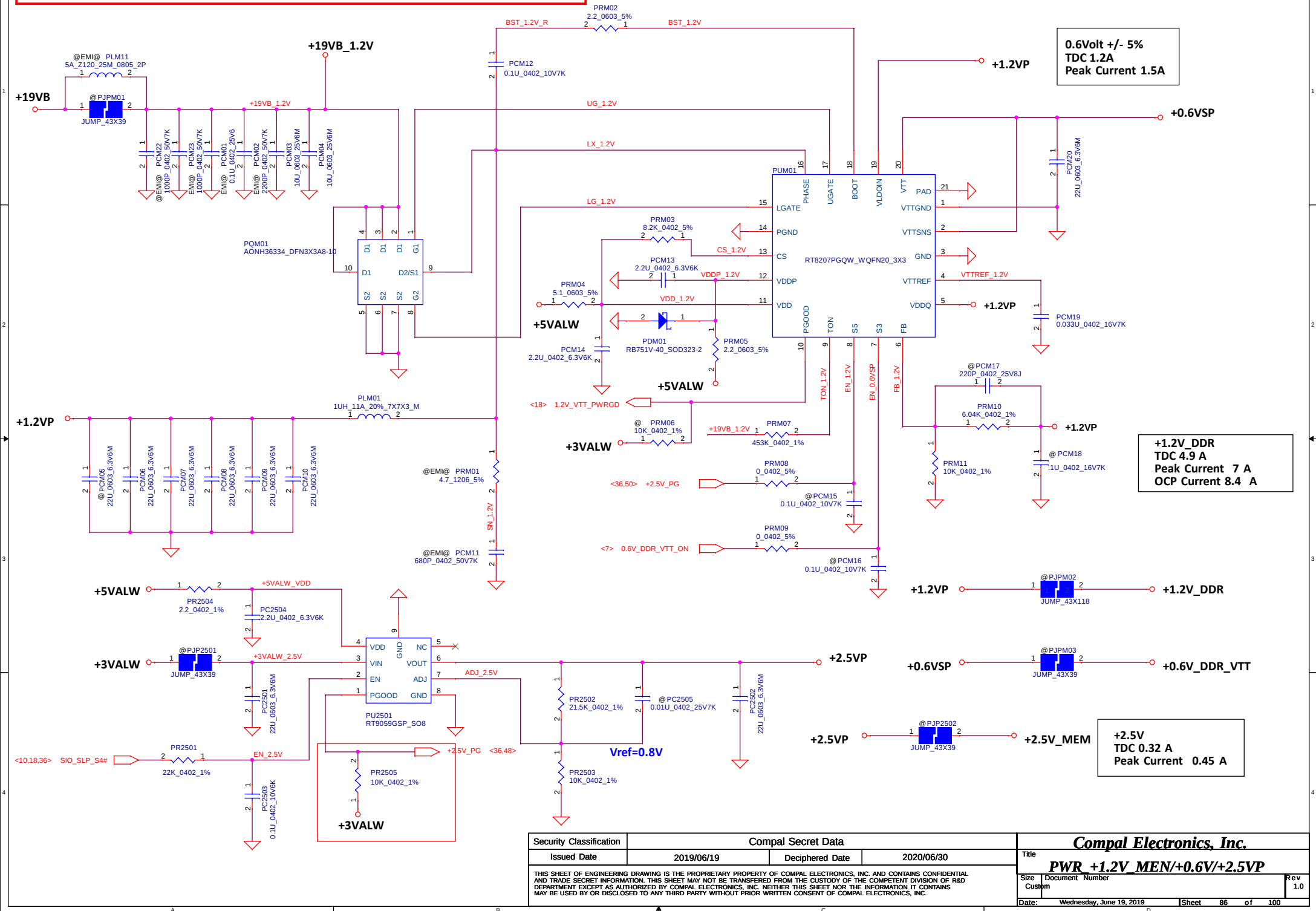
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Issued Date		2019/06/19	Deciphered Date		2020/06/30
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				PWR CHARGER	
				Size	Document Number
				LA-G717P	Rev 1.0
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Main Func = 3.3VALWP/5VALWP

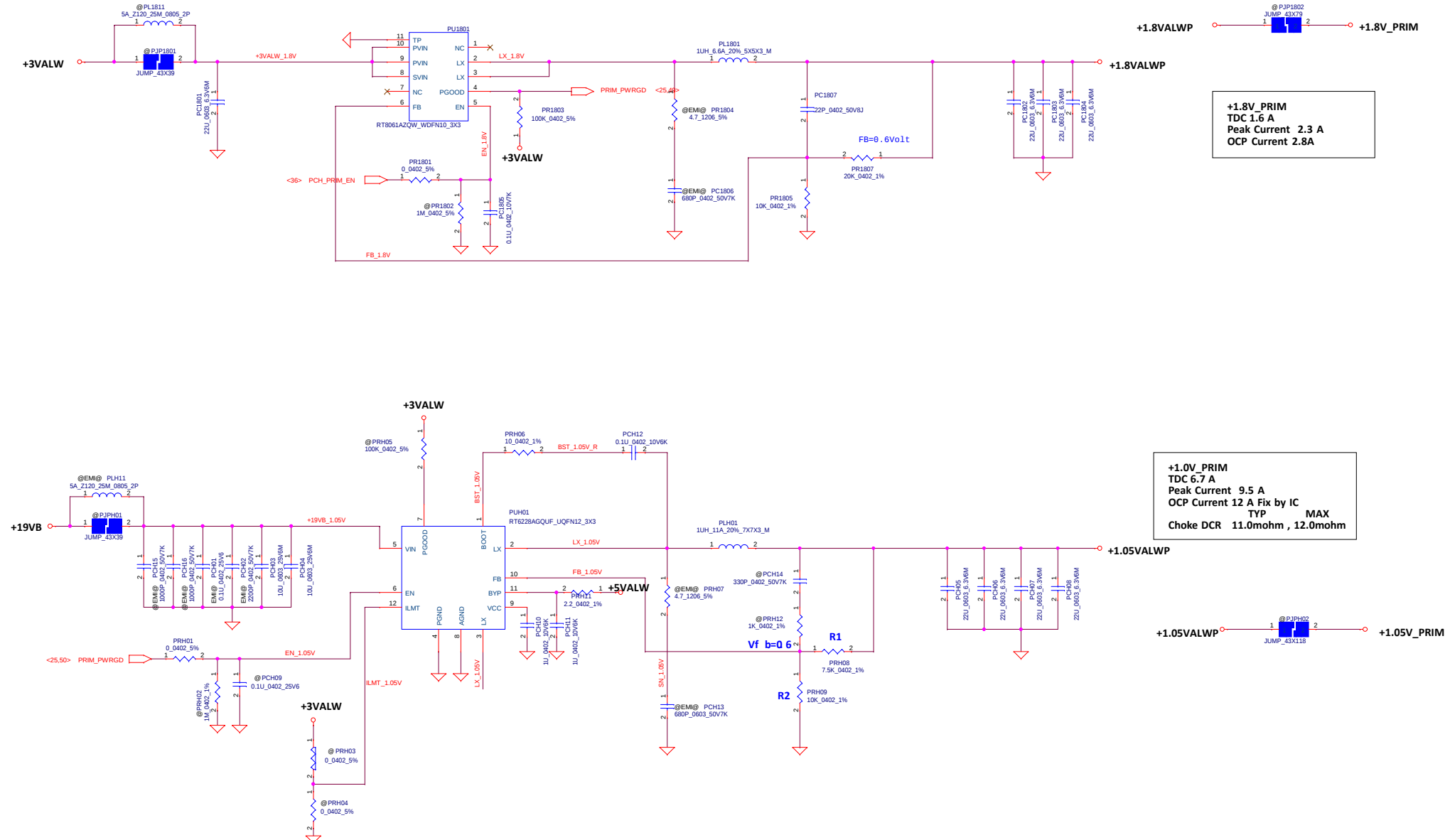


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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/ +2.5VP

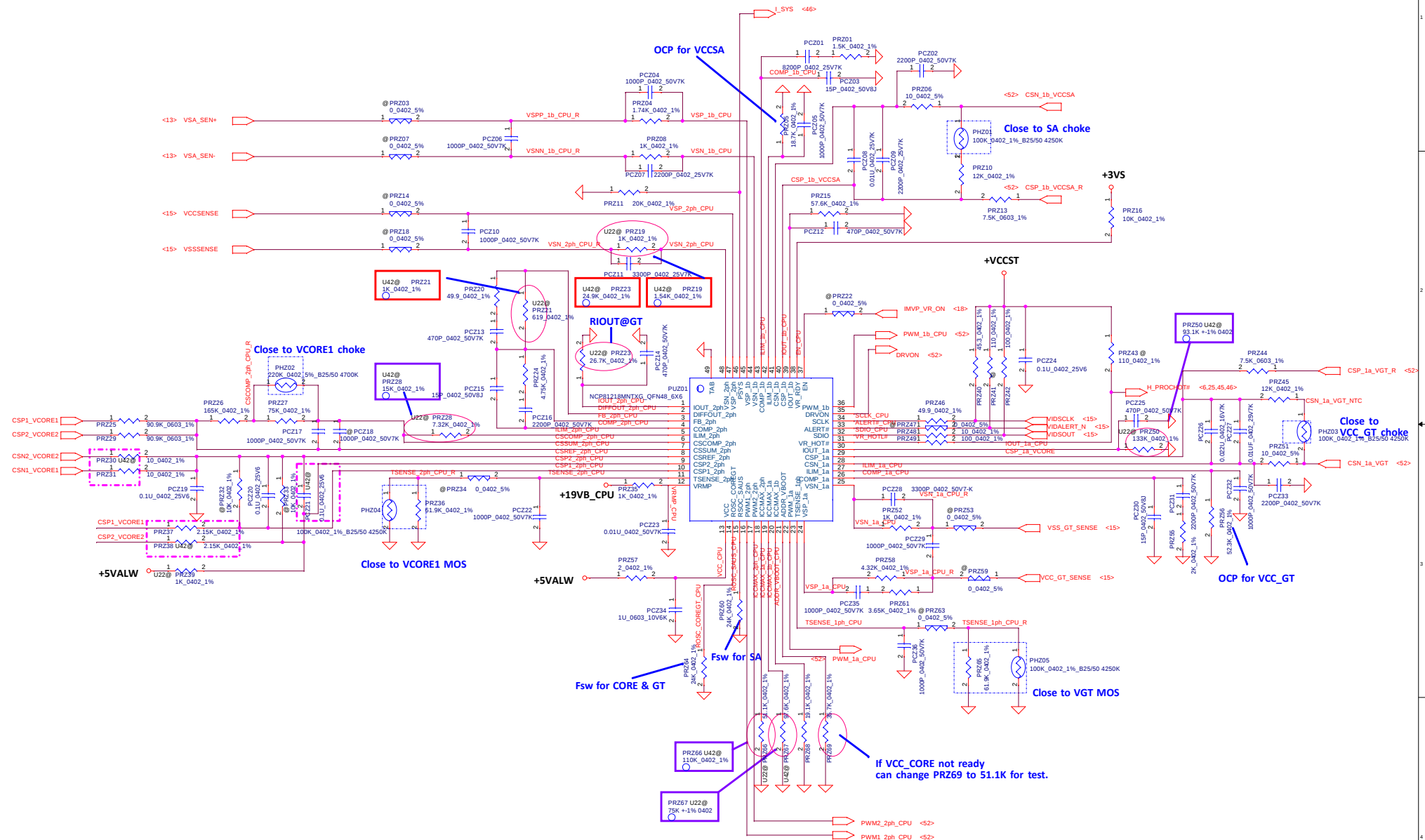


Main Func = +1.8VALWP / +1.05VALWP



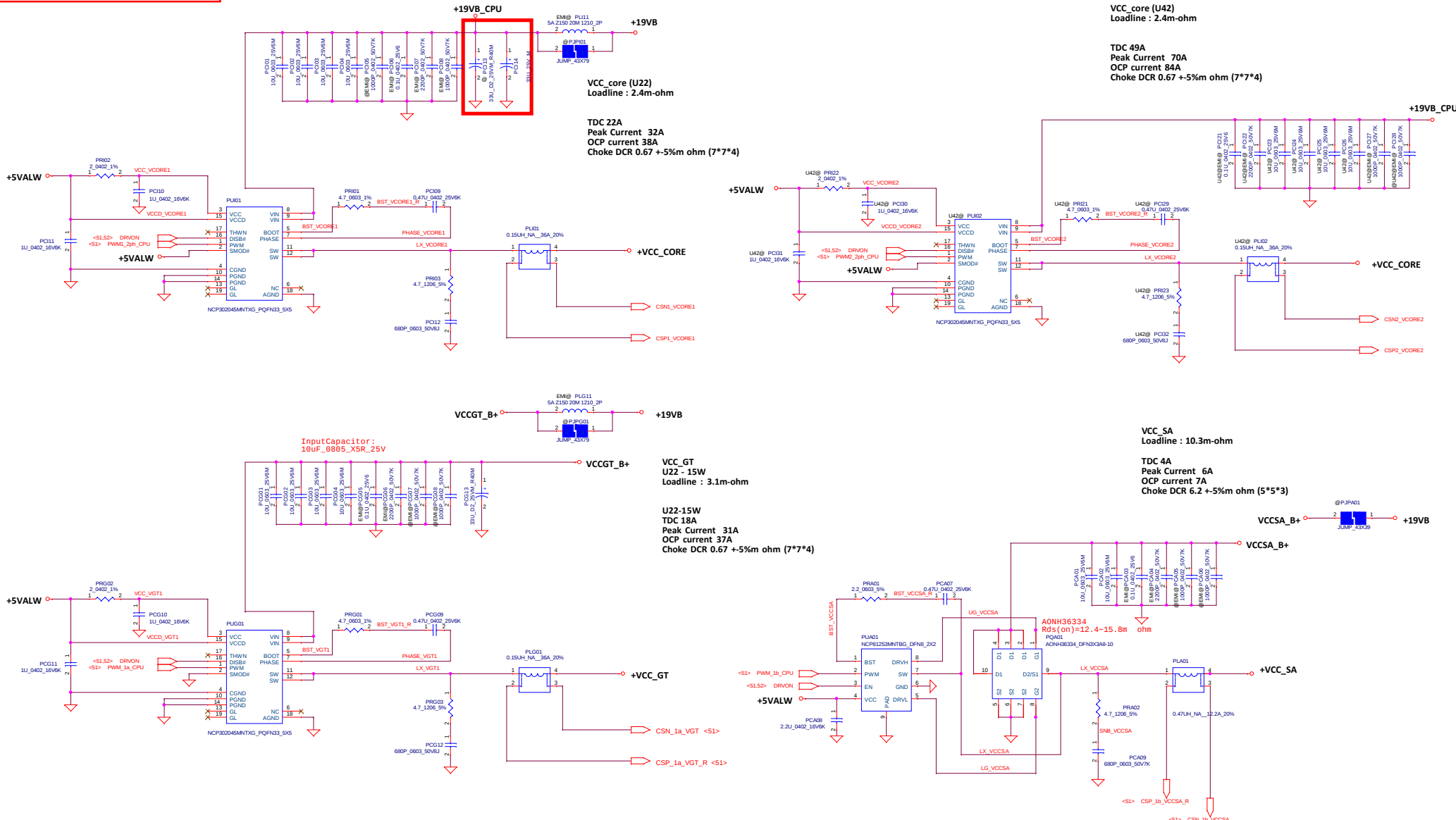
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Main Func = CPU



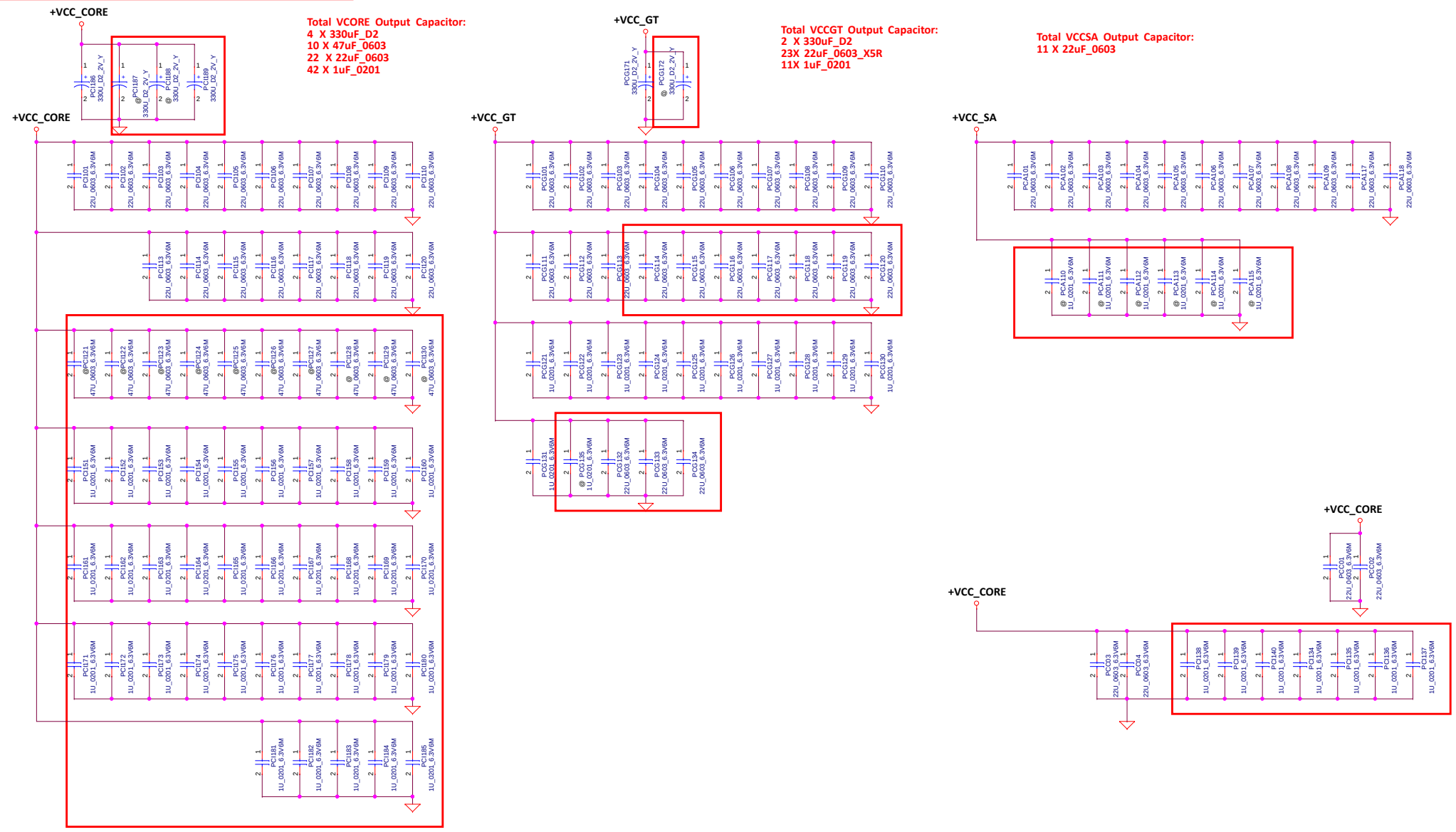
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Main Func = CPUcore IA/GT/SA



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Main Func = CPU/ VGA / SA MLCC



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DVT1 EE change list

Design Change					
Item	Date	Page	Part reference	Change description	Reason
Based on 05/15					
1	2018/5/17	8		Add RC207, CPU_SPI_0_CS#1	For 2nd ROM
2	2018/5/17	14		CC52,CC48,CC51,C5 change to 0402	meet purchase requirement
3	2018/5/17	29		CV73*CV78, CV100*CV109 change to 0402	meet purchase requirement
4	2018/5/20			Del C56,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize
5	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch
6	2018/6/4	38		Connect UC1,CC30 to R72, Add RC208,RC209	For 17" Touch
7	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize
8	2018/6/4	16		CL16 change to 0201	MLCC downsize
9	2018/6/13	58		CA16 change to 0402	MLCC downsize
10	2018/6/19	71		Swap D+/D- on JUSB1 Conn	For BITS377044
11	2018/6/19	38		Add LCD_CBI_DET# on Jedp pin14 and Connect to GPP_C10	For BITS378028
12	2018/7/4	65		add Rx10*14	co-lay ST TPM
13	2018/7/4			add CC75,C241,CC76,CC77,CC78,CC79	For ESD requirement
14	2018/7/6	65		add Rx15*RX19	co-lay China TPM

Version Change List (P. I. R. List)

Item Page# Title Date Request Owner Issue Description Solution Description Rev.

1	P51	PWR	20160321	COMPAL			0.1(X00)
2	P56	PWR	20160321	COMPAL			0.1(X00)
3							
4							
5							
6							
7							
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