WASP 13 CS
Whiskey Lake-U

2019-01
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DIS only installed

<Core Design>

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Title: Cover Page		
Size: A 4	Document Number: WASP 13" WHL-U	Rev: A00
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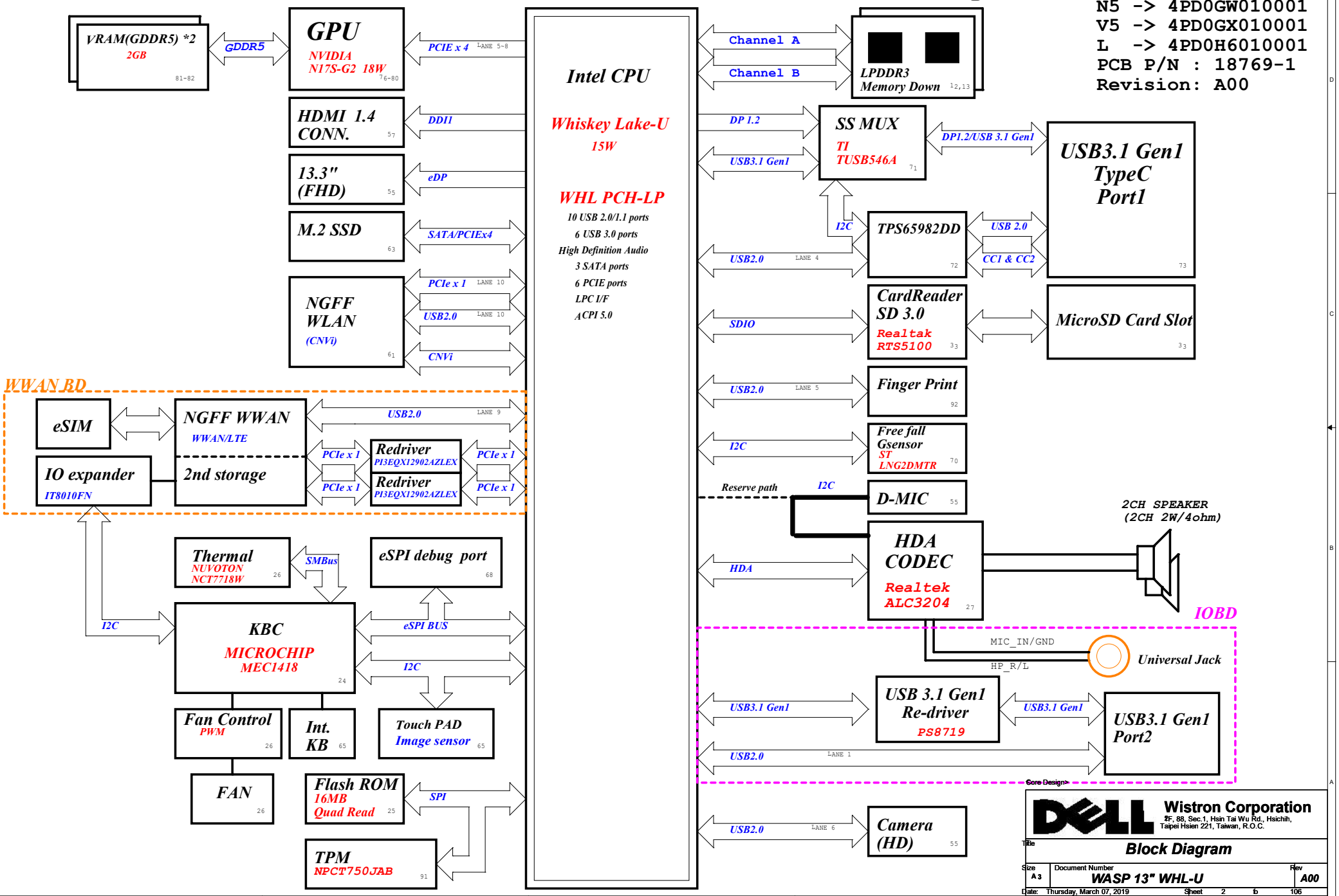
WASP 13" CPU 15W + GPU 18W Block Diagram

Project code :
N5 -> 4PD0GW010001
V5 -> 4PD0GX010001
L -> 4PD0H6010001
PCB P/N : 18769-1
Revision: A00



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Title: Block Diagram

Size	Document Number	Rev
A3	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 2 of 106

Main Func = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TP_WAKE_KBC#
55 TOUCH_PANEL_PD#
17 H_CPUPWRGD

1V_VCCSTG = 1.05V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

R301 Rb 1KR2J-1-GP
R302 Ra 499R2F-2-GP
PROCHOT#_CPU

CPU1D 4 OF 20
WHISKEY-LAKE-GP
ZZ.00CPU.271

PECI_CPU AA4
PROCHOT#_CPU_R AR1
THERMTRIP#_CPU Y4
BJ1

CATERR#
PECI
PROCHOT#
THRMTRIP#

TP307 BPM_N0 U1
TP308 BPM_N1 U2
TP302 BPM_CPU_N2 U3
TP303 BPM_CPU_N3 U4

BPM#0
BPM#1
BPM#2
BPM#3

PROC_TCK T6
PROC_TDI U6
PROC_TDO Y5
PROC_TMS T5
PROC_TRST# AB6

XDP_TCLK 1 TP309
XDP_TDI 1 TP310
XDP_TDO_CPU
XDP_TMS
XDP_TRST# 1 TP313

PCH_TCK W6
PCH_TDI U5
PCH_TDO W5
PCH_TMS P5
PCH_TRST# Y6
PCH_JTAGX P6

PCH_TCK 1 TP314
1 TP316
1 TP317

TP304 GPP_E3/CPU_GP0 CE9
TOUCH_PANEL_INTR# CN3
TP_WAKE_KBC# CB34
TOUCH_PANEL_PD# CC35

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

PROC_PREQ# W2
PROC_PRDY# W1

XDP_PREQ# 1 TP305
XDP_PRDY# 1 TP306

R304 49D9R2F-GP CPU_POPIRCOMP BP27
R305 49D9R2F-GP PCH_POPIRCOMP BW25

PROC_POPIRCOMP
PCH_OPIRCOMP

3D3V_S5_PCH
R303 DY 100KR2J-1-GP TP_WAKE_KBC#

1V_VCCST_CPU
R308 1KR2J-1-GP THERMTRIP#_CPU

1V_VCCSTG
1V_VCCSTG = 1.05V
R310 51R2J-2-GP XDP_TDO_CPU
R317 51R2J-2-GP XDP_TCLK

THERMTRIP#_CPU
H_CPUPWRGD

D301 DY AZ5125-02S-R7G-GP
75.05125.07D

<Core Design>

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Title: CPU (THML/JTAG)

Size	Document Number	Rev
A4	WASP 13" WHL-U	A 00

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Main Func = CPU

DP to HDMI1.4

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 HDMI_HPD_CPU

57 CPU_DP1_CTRL_CLK
57 CPU_DP1_CTRL_DATA

DP for Type-C Mux

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
71,72 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL

55 EDP_VDD_EN

15 GPP_H17_STRAP

24 GC6_THM_DIS#

3D3V_S0

20180904 Stuff
R402 1 2 10KR2J-L-GP
SIO_EXT_SMI#

RN401
1 4 CPU_DP1_CTRL_DATA
2 3 CPU_DP1_CTRL_CLK
SRN2K2J-1-GP

RN403
1 4 CPU_DP2_CTRL_DATA
2 3 CPU_DP2_CTRL_CLK
SRN2K2J-1-GP

R403 1 2 100KR2J-1-GP
DP1_HPD_CPU_R

3D3V_S5_PCH

RN405 SA 0816
1 4
2 3
SRN10KJ-5-GP

CPU_DP_HPD_P

Q401
1 6 DP1_HPD_CPU_R
2 5 DP1_HPD_CPU
3 4
2N7002KDW-1-GP

75.27002.F7C

DP to HDMI

DP for Type-C Mux

1V_VCCIO

R401 1 2 24D9R2F-L-GP

CPU1A 1 OF 20

HDMI_DDI_TX_N0	AL5	DDI1_TXN0	EDP_TXN0	AG4	eDP_TX_CPU_N0
HDMI_DDI_TX_P0	AL6	DDI1_TXP0	EDP_TXP0	AG3	eDP_TX_CPU_P0
HDMI_DDI_TX_N1	AJ5	DDI1_TXN1	EDP_TXN1	AG2	eDP_TX_CPU_N1
HDMI_DDI_TX_P1	AJ6	DDI1_TXP1	EDP_TXP1	AG1	eDP_TX_CPU_P1
HDMI_DDI_TX_N2	AF6	DDI1_TXN2	EDP_TXN2	AJ4	
HDMI_DDI_TX_P2	AF5	DDI1_TXP2	EDP_TXP2	AJ3	
HDMI_DDI_TX_N3	AE5	DDI1_TXN3	EDP_TXN3	AJ2	
HDMI_DDI_TX_P3	AE6	DDI1_TXP3	EDP_TXP3	AJ1	
DP2_DDI_TX_N0	AC4	DDI2_TXN0			
DP2_DDI_TX_P0	AC3	DDI2_TXP0	EDP_AUX_N	AH4	eDP_AUX_CPU_N
DP2_DDI_TX_N1	AC1	DDI2_TXN1	EDP_AUX_P	AH3	eDP_AUX_CPU_P
DP2_DDI_TX_P1	AC2	DDI2_TXP1			
DP2_DDI_TX_N2	AE4	DDI2_TXN2	DISP_UTILS	AM7	
DP2_DDI_TX_P2	AE3	DDI2_TXP2			
DP2_DDI_TX_N3	AE1	DDI2_TXN3	DDI1_AUX_N	AC7	
DP2_DDI_TX_P3	AE2	DDI2_TXP3	DDI1_AUX_P	AC6	
			DDI2_AUX_N	AD4	DP2_AUX_CPU_N
			DDI2_AUX_P	AD3	DP2_AUX_CPU_P
			DDI3_AUX_N	AG7	
			DDI3_AUX_P	AG6	

GPP_E13/DDPB_HPD0/DISP_MISC0	CN6	HDMI_HPD_CPU	
GPP_E14/DDPC_HPD1/DISP_MISC1	CM6	DP1_HPD_CPU_R	
GPP_E15/DPPD_HPD2/DISP_MISC2	CP7	SIO_EXT_SMI#	
GPP_E16/DPPE_HPD3/DISP_MISC3	CP6		
GPP_E17/EDP_HPD/DISP_MISC4	CM7	eDP_HPD_CPU	
EDP_BKLTEN	CK11	L_BKLT_EN	
EDP_VDDEN	CG11	EDP_VDD_EN	
EDP_BKLTCTL	CH11	L_BKLT_CTRL	

eDP_RCOMP_CPU	AM6	DISP_RCOMP	
CPU_DP1_CTRL_CLK	CC8	GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#	
CPU_DP1_CTRL_DATA	CC9	GPP_E19/DPPB_CTRLDATA	
CPU_DP2_CTRL_CLK	CH4	GPP_E20/DPPC_CTRLCLK	
CPU_DP2_CTRL_DATA	CH3	GPP_E21/DPPC_CTRLDATA	
	CP4	GPP_E22/DPPD_CTRLCLK	
	CN4	GPP_E23/DPPD_CTRLDATA	
GC6_THM_DIS#	CR26	GPP_H16/DDPF_CTRLCLK	
GPP_H17_STRAP	CP26	GPP_H17/DDPF_CTRLDATA	

WHISKEY-LAKE-GP

ZZ.00CPU.271

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 □[□□1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k □□5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k □□5% resistor	NC

<Core Design>

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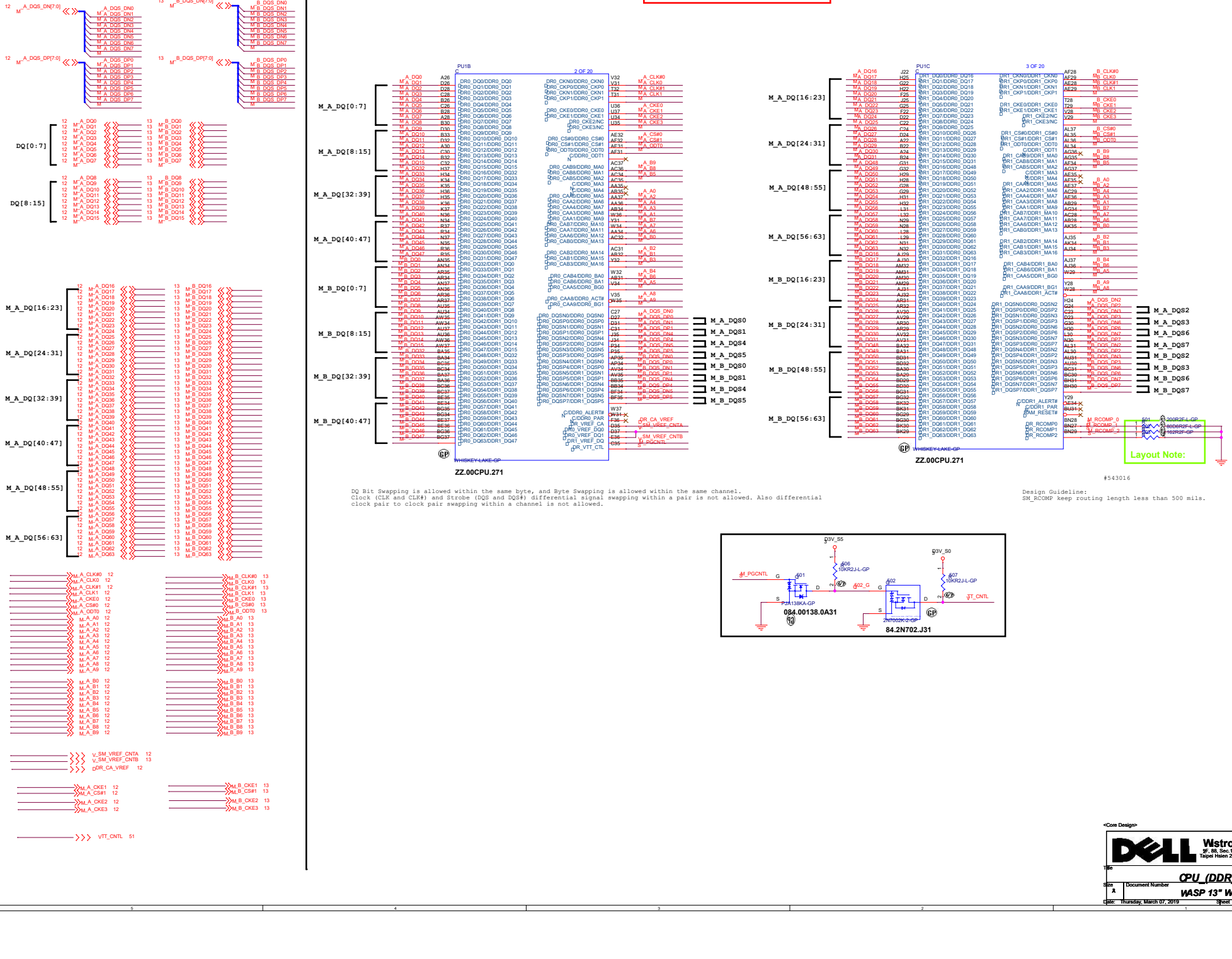
Title: CPU (DDI/EDP)

Size: A4 | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type: Non-Interleaved Type



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

#543016

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Title: CPU_(DDR)

Size	Document Number	Rev
A	WASP 13" WHL-U	A0

Date: Thursday, March 07, 2019 Sheet 5 of 108

Main Func = CPU

15 CFG3
15 CFG4

CPU1Q — 17 OF 20
WHL QS/CFL/WHL_ES1_CNL U

CFG3
CFG4

T4 CFG0
R4 CFG1
T3 CFG2
R3 CFG3
J4 CFG4
M4 CFG5
J3 CFG6
M3 CFG7
R2 CFG8
N2 CFG9
R1 CFG10
N1 CFG11
J2 CFG12
L2 CFG13
J1 CFG14
L1 CFG15
L3 CFG16
N3 CFG18
L4 CFG17
N4 CFG19

R601 1 — 2 49D9R2F-GP — CFG_RCOMP — AB5 CFG_RCOMP

TP618 — 1 ITP_PMODE — W4 ITP_PMODE

CG2 RSVD#CG2
CG1 RSVD#CG1

H4 RSVD#H4
H3 RSVD#H3

BV24 RSVD#BV24
BV25 RSVD#BV25

BK36 RSVD#BK36
BK35 RSVD#BK35

W3 RSVD#W3
AM4 RSVD#AM4

AM3 RSVD_TP#AM3

F37 RSVD_TP#F37
F34 RSVD_TP#F34
CP36 IST_TRIG
CN36 RSVD_TP#CN36

IST_TRIG — 1 — TP620 — TPAD14-OP-GP

BJ36 RSVD_TP#BJ36
BJ34 RSVD_TP#BJ34

BK34 TP#BK34
BR18 TP#BR18

BT9 RSVD_TP#BT9
BT8 RSVD_TP#BT8

BP8 RSVD_TP#BP8
BP9 RSVD_TP#BP9

CR4 RSVD#CR4

CP3 RSVD#CP3
CR3 RSVD#CR3

AT3 RSVD_TP#AT3
AU3 RSVD_TP#AU3

AN1 RSVD#AN1
AN2 RSVD#AN2

AN4 RSVD#AN4
AN3 RSVD#AN3

AL2 IST_TP0
AL1 IST_TP1

AL4 IST_TRIG0
AL3 IST_TRIG1

BP34 TP#BP34
BP36 VSS
BP35 TP#BP35

CR35 RSVD_TP#CR35

E1 SKTOCC# — SKTOCC# 1 — TP619

GP

WHISKEY-LAKE-GP

ZZ.00CPU.271

<Core Design>

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Title: **CPU (CFG/IST)**

Size	Document Number	Rev
A4	WASP 13" WHL-U	A00

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Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

SVID DATA

1V_VCCST_CPU
#544669
CLOSE TO CPU
R726
100R2F-L1-GP-U
SVID_DATA_CPU_R R709 1 2 0R0402-PAD SVID_DATA_CPU

SVID CLOCK

1V_VCCST_CPU
#544669
CLOSE TO VR
R723
DY 54D9R2F-L1-GP
SVID_CLK_CPU_R R732 1 2 0R0402-PAD SVID_CLK_CPU

SVID ALERT

1V_VCCST_CPU
#544669
CLOSE TO CPU
R727
56R2J-4-GP
SVID_ALERT#_CPU_R R728 1 2 220R2J-L2-GP SVID_ALERT#_CPU

SVID_543016:

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (□□0.1 inch).
Route the Alert signal between the Clock and the Data signals.

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu1} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

1V_CPU_CORE
CPU1L
1 2 OF 20
1V_CPU_CORE

AN9	VCCCORE	VCCCORE	AW24
AN10	VCCCORE	VCCCORE	AW25
AN24	VCCCORE	VCCCORE	AW26
AN26	VCCCORE	VCCCORE	AW27
AN27	VCCCORE	VCCCORE	AY24
AP2	VCCCORE	VCCCORE	AY26
AP9	VCCCORE	VCCCORE	BA5
AP24	VCCCORE	VCCCORE	BA7
AP26	VCCCORE	VCCCORE	BA8
AR5	VCCCORE	VCCCORE	BA25
AR6	VCCCORE	VCCCORE	BA27
AR7	VCCCORE	VCCCORE	BB2
AR8	VCCCORE	VCCCORE	BB26
AR10	VCCCORE	VCCCORE	BC5
AR25	VCCCORE	VCCCORE	BC6
AR27	VCCCORE	VCCCORE	BC7
AT9	VCCCORE	VCCCORE	BC9
AT24	VCCCORE	VCCCORE	BC10
AT26	VCCCORE	VCCCORE	BC26
AU5	VCCCORE	VCCCORE	BC27
AU6	VCCCORE	VCCCORE	BD5
AU7	VCCCORE	VCCCORE	BD8
AU8	VCCCORE	VCCCORE	BD10
AU9	VCCCORE	VCCCORE	BD25
AU24	VCCCORE	VCCCORE	BD27
AU25	VCCCORE	VCCCORE	BE9
AU26	VCCCORE	VCCCORE	BE24
AU27	VCCCORE	VCCCORE	BE25
AV2	VCCCORE	VCCCORE	BE26
AV5	VCCCORE	VCCCORE	BE27
AV7	VCCCORE	VCCCORE	BF2
AV10	VCCCORE	VCCCORE	BF9
AV27	VCCCORE	VCCCORE	BF24
AW5	VCCCORE	VCCCORE	BF26
AW6	VCCCORE	VCCCORE	BG27
AW7	VCCCORE	VCCCORE	
AW8	VCCCORE	VCC_SENSE	AN6 V CCCORE_SENSE
AW9	VCCCORE	VSS_SENSE	AN5 V SSCORE_SENSE
AW10	VCCCORE	VIDALERT#	AA3 S VID_ALERT#_CPU_R
BB9	RSVD#BB9	VIDSCK	AA1 S VID_CLK_CPU_R
BC24	RSVD#BC24	VIDSOUT	AA2 S VID_DATA_CPU_R
AY9	RSVD#AY9	RSVD#Y3	Y3
BB24	RSVD#BB24	VCCSTG	BG3

1 V_VCCSTG

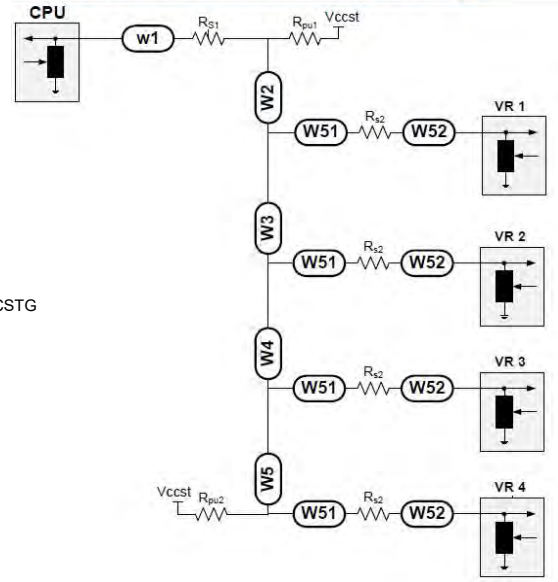
WHISKEY-LAKE-GP
ZZ.00CPU.271

1 V_CPU_CORE
R 719
100R2F-L1-GP-U
V CCCORE_SENSE
V SSCORE_SENSE
R 720
100R2F-L1-GP-U

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology



<Core Design>

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Title: CPU (VCORE/VID)

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 Sheet 7 of 106

Main Func = CPU

46 VSSGT_SENSE
46 VCCGT_SENSE
46 VSSSA_SENSE
46 VCCSA_SENSE

1V_VCCGT
R807 100R2F-L1-GP-U
VCCGT_SENSE
VSSGT_SENSE
R808 100R2F-L1-GP-U

1V_VCCSA
R810 100R2F-L1-GP-U
VCCSA_SENSE
VSSSA_SENSE
R809 100R2F-L1-GP-U

CPU1M 13 OF 20
WHL QS/CFL/WHL_ES1_CNL U

A5	VCCGT	VCCGT	H12
A6	VCCGT	VCCGT	H14
A8	VCCGT	VCCGT	H15
A11	VCCGT	VCCGT	H17
A12	VCCGT	VCCGT	H18
A14	VCCGT	VCCGT	H20
A15	VCCGT	VCCGT	J7
A17	VCCGT	VCCGT	J8
A18	VCCGT	VCCGT	J11
A20	VCCGT	VCCGT	J14
B3	VCCGT	VCCGT	J17
B4	VCCGT	VCCGT	J20
B6	VCCGT	VCCGT	K2
B8	VCCGT	VCCGT	K11
B11	VCCGT	VCCGT	L7
B14	VCCGT	VCCGT	L8
B17	VCCGT	VCCGT	L10
B20	VCCGT	VCCGT	M9
C2	VCCGT	VCCGT	N7
C3	VCCGT	VCCGT	N8
C6	VCCGT	VCCGT	N9
C7	VCCGT	VCCGT	N10
C8	VCCGT	VCCGT	P2
C11	VCCGT	VCCGT	P8
C12	VCCGT	VCCGT	R9
C14	VCCGT	VCCGT	T8
C15	VCCGT	VCCGT	T9
C17	VCCGT	VCCGT	T10
C18	VCCGT	VCCGT	U8
C20	VCCGT	VCCGT	U10
D4	VCCGT	VCCGT	V9
D7	VCCGT	VCCGT	W8
D11	VCCGT	VCCGT	W9
D12	VCCGT	VCCGT	AA9
D14	VCCGT	VCCCORE	AB2
D15	VCCGT	VCCCORE	AB8
D17	VCCGT	VCCCORE	AB9
D18	VCCGT	VCCCORE	AB10
D20	VCCGT	VCCCORE	AC8
E4	VCCGT	VCCCORE	AD9
F5	VCCGT	VCCCORE	AE8
F6	VCCGT	VCCCORE	AE9
F7	VCCGT	VCCCORE	AE10
F8	VCCGT	VCCCORE	AF2
F11	VCCGT	VCCCORE	AF8
F14	VCCGT	VCCCORE	AF10
F17	VCCGT	VCCCORE	AG8
F20	VCCGT	VCCCORE	AG9
G11	VCCGT	VCCCORE	AH9
G12	VCCGT	VCCCORE	AJ8
G14	VCCGT	VCCCORE	AJ10
G15	VCCGT	VCCCORE	AK2
G17	VCCGT	VCCCORE	AK9
G18	VCCGT	VCCCORE	AL8
G20	VCCGT	VCCCORE	AL9
H5	VCCGT	VCCCORE	AL10
H6	VCCGT	VCCCORE	AM8
H7	VCCGT	VCCCORE	V2
H8	VCCGT	VCCCORE	Y8
H11	VCCGT	VCCCORE	Y10
		VCCGT_SENSE	E3
		VSSGT_SENSE	D2

1V_VCCGT
1V_VCCGT
1V_CPU_CORE
VCCGT_SENSE
VSSGT_SENSE
WHISKEY-LAKE-GP
ZZ.00CPU.271

1 D2V_S3
DY C 804 SC1U10V2KX-1DLGP

C PU1N 1 4 OF 20

AD36	VDDQ	VCCIO_OUT	AK24
AH32	VDDQ	VCCIO_OUT	AK26
AH36	VDDQ	VCCIO_OUT	AL24
AM36	VDDQ	VCCIO_OUT	AL25
AN32	VDDQ	VCCIO_OUT	AL26
AW32	VDDQ	VCCIO_OUT	AL27
AY36	VDDQ	VCCIO_OUT	AM25
BE32	VDDQ	VCCIO_OUT	AM27
BH36	VDDQ	VCCIO_OUT	BH24
R32	VDDQ	VCCIO_OUT	BH25
Y36	VDDQ	VCCIO_OUT	BH26
		VCCIO_OUT	BH27
		VCCIO_OUT	BJ24
		VCCIO_OUT	BJ26
		VCCIO_OUT	BP16
		VCCIO_OUT	BP18
BC28	RSVD#BC28		
BP11	VCCST	VCCSA	BG8
BP2	VCCST	VCCSA	BG10
		VCCSA	BH9
		VCCSA	BJ8
		VCCSA	BJ9
BG1	VCCSTG	VCCSA	BJ10
BG2	VCCSTG	VCCSA	BK8
BL27		VCCSA	BK25
BM26	VCCPLL_OC	VCCSA	BK27
	VCCPLL_OC	VCCSA	BL8
BR11		VCCSA	BL9
BT11	VCCPLL	VCCSA	BL10
	VCCPLL	VCCSA	BL24
		VCCSA	BL26
		VCCSA	BM24
		VCCSA	BN25
BP28	VCCIO_SENSE		
BP29	VSSIO_SENSE		
BE7	VSSSA_SENSE	V SSSA_SENSE	
BG7	VCCSA_SENSE	V CCSA_SENSE	

1 V_VCCIO
+VCCIO(ICCMAX.=2.73A
1 V_VCCSA
1 V_VCCST_CPU
C 801 1 2 SC1U10V2KX-1DLGP 0.04 A
1 V_VCCSTG
C 802 1 2 SC1U10V2KX-1DLGP
1 D2V_VCCSFR_OC
C 803 1 2 SC1U10V2KX-1DLGP
1 V_VCCST_CPU 0.12 A
C807 SC22U6D3V3MX-1-DL-GP
C806 SC1U10V2KX-1DLGP
C805 SCD1U16V2KX-3DLGP
WHISKEY-LAKE-GP
ZZ.00CPU.271

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VCCGT/VCCIO/VDDQ/VCCSA)

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 Sheet 8 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*WASP 13" WHL-U*	*A00*

Date: Thursday, March 07, 2019 | Sheet 9 of 106

Main Func = CPU

1V_CPU_CORE

1V_CPU_CORE

22U 0603 x 39 (7DY)

PC1002 PC1003 PC1004 PC1005 PC1006 PC1007 PC1008 PC1009 PC1010 PC1011 PC1012 PC1013 PC1014 PC1015 PC1016 PC1017 PC1018 PC1019 PC1020 PC1021
U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42

SC22U6D3V3MX-1-DL-GP ×20

PC1022 PC1023 PC1024 PC1025 PC1026 PC1027 PC1028 PC1029 PC1030 PC1031 PC1032 PC1034 PC1036 PC1079 PC1080 PC1081 PC1082 PC1083 PC1084
DY DY DY U42 DY U42 DY DY DY DY DY DY U42

SC22U6D3V3MX-1-DL-GP ×20

VCCGT

1V_VCCGT

22U 0603 x 35 (9 DY)

PC1037 PC1038 PC1039 PC1040 PC1041 PC1042 PC1043 PC1044 PC1045 PC1046 PC1047 PC1048 PC1049 PC1050 PC1051 PC1052 PC1053 PC1054 PC1055 PC1056
DY

SC22U6D3V3MX-1-DL-GP ×20

PC1057 PC1058 PC1059 PC1060 PC1061 PC1062 PC1063 PC1064
DY DY DY

SC22U6D3V3MX-1-DL-GP ×8

PC1065 PC1066 PC1067 PC1068 PC1069 PC1070 PC1001
DY DY DY DY DY

SC22U6D3V3MX-1-DL-GP ×8

VCCSA

1V_VCCSA

22U 0603 x 8 (3DY)

PC1071 PC1072 PC1073 PC1074 PC1075 PC1076 PC1077 PC1078
DY DY DY

SC22U6D3V3MX-1-DL-GP ×8

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP1)		
Size: A4	Document Number: WASP 13" WHL-U	Rev: A 00
Date: Thursday, March 07, 2019	Sheet 10 of 106	

Main Func = CPU

PCH DERIVED RAILS

1D0V_S5

C1112 C1128 C1129

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

3D3V_S5_PCH — R1103 — 3D3V_VCCPRIM

0R0603-PAD

DY C1113 SC22U6D3V3MX-1-DL-GP

1D8V_S5 — R1104 — 1D8V_VCCPRIM

0R0603-PAD

DY C1122 SC22U6D3V3MX-1-DL-GP

3D3V_VCCPRIM

DY C1123 SC10U6D3V3MX-DL-GP

UNSLICED GT

1V_VCCGT

1U 0402 x 6

C1102 C1103 C1104 C1105 C1106 C1107

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

VCCIO

1V_VCCIO

+VCCIO(ICCMAX.=2.73A)

C1133 C1134 C1135

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

C1108 C1109 C1110 C1111

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

1D0V_S5

DY C1115 SC22U6D3V3MX-1-DL-GP
C1114 SC1U10V2KX-1DLGP

1D0V_S5

C1116 C1117

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

1D0V_S5

DY C1118 SC22U6D3V3MX-1-DL-GP
C1119 SC1U10V2KX-1DLGP

1D0V_S5

DY C1120 SC10U6D3V3MX-DL-GP
C1121 SC1U10V2KX-1DLGP

1D2V_S3

DY C1132 DY C1131 C1130

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

C1136 C1137 C1138

SC10U6D3V3MX-DL-GP
SC10U6D3V3MX-DL-GP
SC10U6D3V3MX-DL-GP

C1139 C1140 C1141 C1142

SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP

<Core Design>

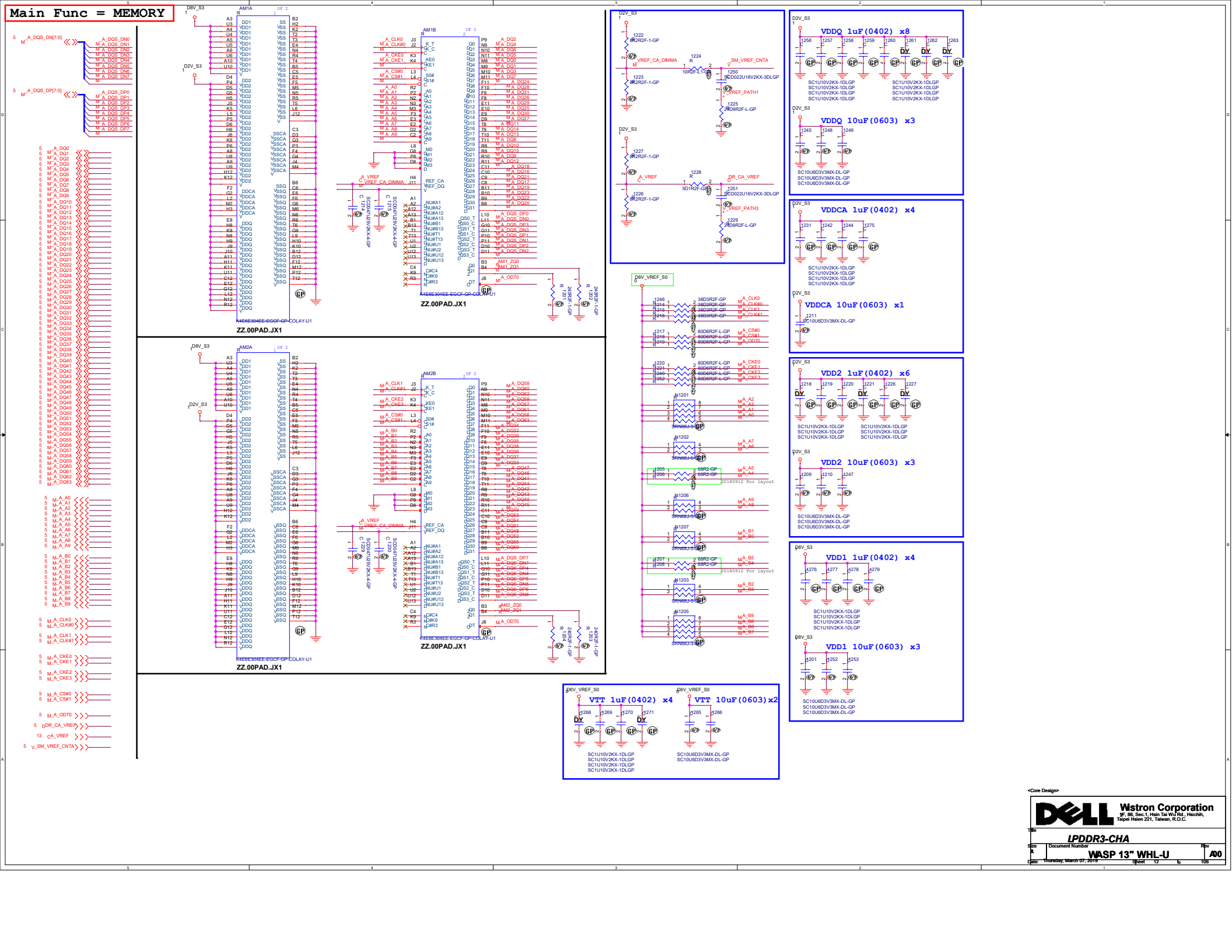
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

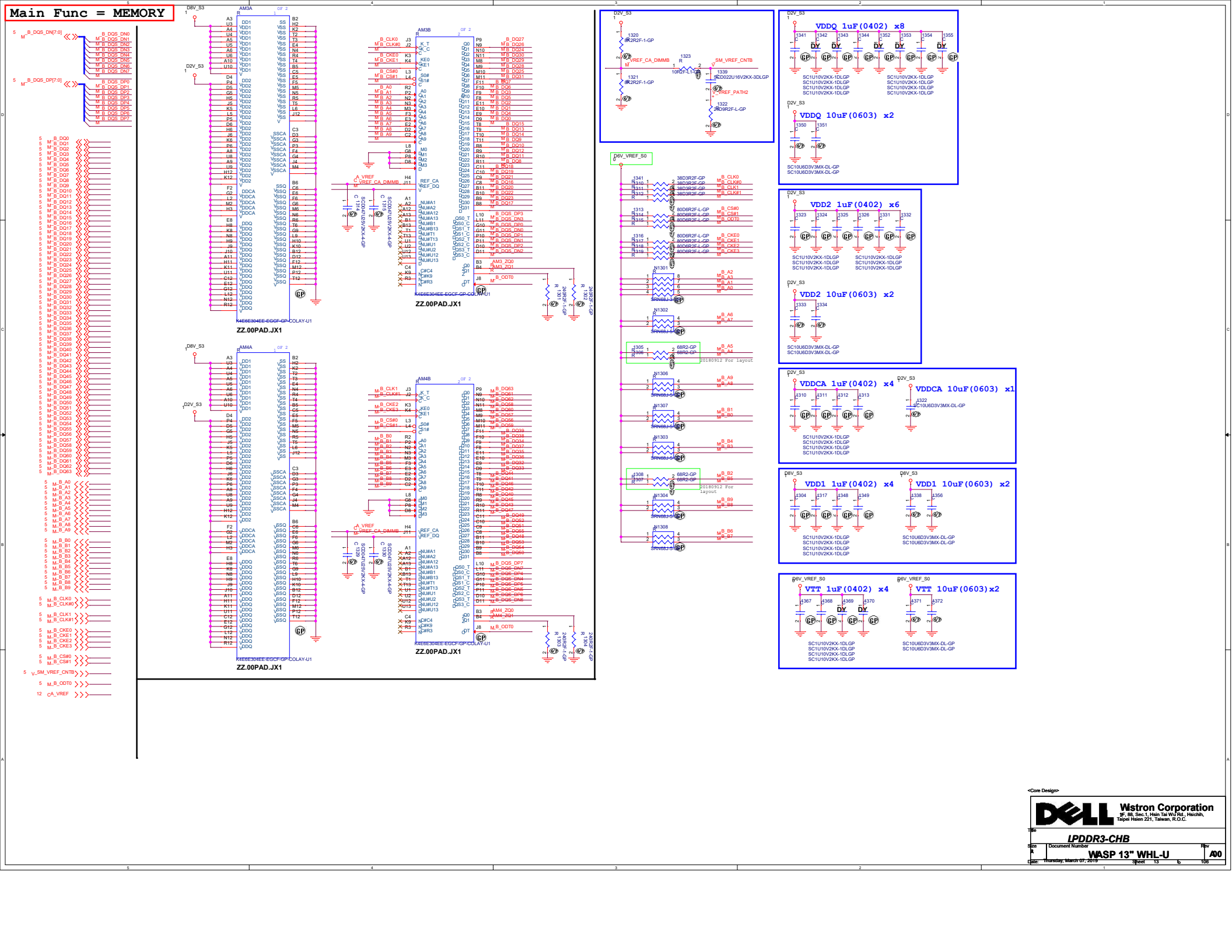
Size	Document Number	Rev
A4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 Sheet 11 of 106

Main Func = MEMORY



Main Func = MEMORY



(Blanking)

<Core Design>

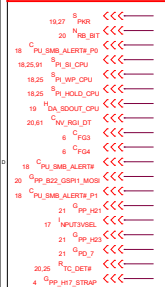
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*WASP 13" WHL-U*	*A00*

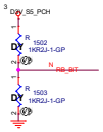
Date: Thursday, March 07, 2019 | Sheet 14 of 106

Main Func = PCH

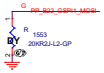


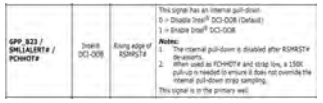
GPP_B14

GPP_B18

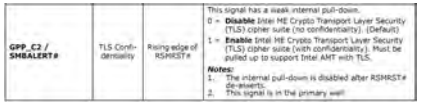


GPP_B22



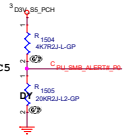


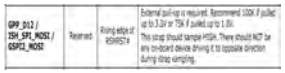
GPP_B23



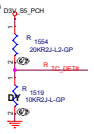
GPP_C2

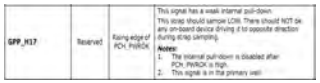
GPP_C5



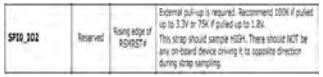


GPP_D12

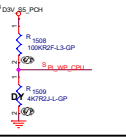


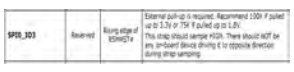


GPP_H21

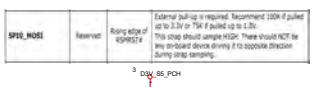


SPI0_IO2

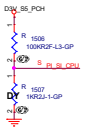


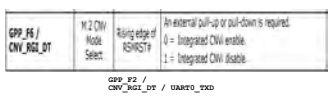


SPI0_IO3

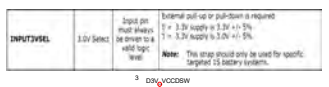


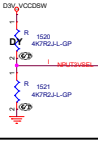
SPI0_MOSI



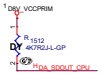


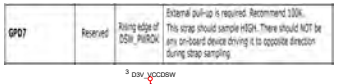
GPP_E2 / CNV_RGI_DT / UART0_TXD



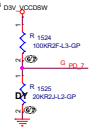


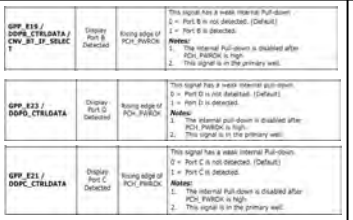
GPP_B2 / HDA_SDO / I2S0_TXD / HDACPU_SDO





GPD7





(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

[BDW Only]PHYSICAL DEBUG ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Strap pins)

Size	Document Number	Rev
C	W ASP 13" WHL-U	0B

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Main Func = PCH

PCIE

61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P

66 WWAN_PCIE_RX_N11
66 WWAN_PCIE_RX_P11
66 WWAN_PCIE_TX_N11
66 WWAN_PCIE_TX_P11

66 WWAN_PCIE_RX_N12
66 WWAN_PCIE_RX_P12
66 WWAN_PCIE_TX_N12
66 WWAN_PCIE_TX_P12

63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P

63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1

63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2

63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3

76 GFX_PCIE_RX_N0
76 GFX_PCIE_RX_P0
76 GFX_PCIE_TX_N0
76 GFX_PCIE_TX_P0

76 GFX_PCIE_RX_N1
76 GFX_PCIE_RX_P1
76 GFX_PCIE_TX_N1
76 GFX_PCIE_TX_P1

76 GFX_PCIE_RX_N2
76 GFX_PCIE_RX_P2
76 GFX_PCIE_TX_N2
76 GFX_PCIE_TX_P2

76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3
76 GFX_PCIE_TX_N3
76 GFX_PCIE_TX_P3

USB3.0

66 USB1_USB30_RX_N
66 USB1_USB30_RX_P

66 USB1_USB30_TX_N
66 USB1_USB30_TX_P

71 USB4_USB30_RX_N
71 USB4_USB30_RX_P

71 USB4_USB30_TX_N
71 USB4_USB30_TX_P

USB2.0

72 USB4_USB20_N
72 USB4_USB20_P

66 USB1_USB20_N
66 USB1_USB20_P

55 CCD_USB20_N
55 CCD_USB20_P

61 BT_USB20_N
61 BT_USB20_P

92 FP1_USB20_N
92 FP1_USB20_P

66 WWAN_USB20_N
66 WWAN_USB20_P

66 USB_OC0#
72 USB_OC3#

24 mCARD_PCIE#_SATA

63 SSD_DEVSLP
63 M2_SSD_PEDET

64 PCH_SATA_LED#

66 WSSD_DEVSLP

GPU

GFX_PCIE_TX_N0 C1606 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_N0
GFX_PCIE_TX_P0 C1605 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_P0
GFX_PCIE_TX_N1 C1608 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_N1
GFX_PCIE_TX_P1 C1607 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_P1
GFX_PCIE_TX_N2 C1610 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_N2
GFX_PCIE_TX_P2 C1609 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_P2
GFX_PCIE_TX_N3 C1612 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_N3
GFX_PCIE_TX_P3 C1611 1 — 2 SCD22U16V2KX-DL-GP GFX_PCIE_TX_C_P3

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

WLAN

2ND M.2

SSD

R1604 1 — 2 100R2F-L1-GP-U

CPU1H

8 OF 20

GFX_PCIE_RX_N0 BW9 — PCIE5_RXN/USB31_5_RXN
GFX_PCIE_RX_P0 BW8 — PCIE5_RXP/USB31_5_RXP
GFX_PCIE_TX_C_N0 BW4 — PCIE5_TXN/USB31_5_TXN
GFX_PCIE_TX_C_P0 BW3 — PCIE5_TXP/USB31_5_TXP
GFX_PCIE_RX_N1 BU6 — PCIE6_RXN/USB31_6_RXN
GFX_PCIE_RX_P1 BU5 — PCIE6_RXP/USB31_6_RXP
GFX_PCIE_TX_C_N1 BU4 — PCIE6_TXN/USB31_6_TXN
GFX_PCIE_TX_C_P1 BU3 — PCIE6_TXP/USB31_6_TXP
GFX_PCIE_RX_N2 BT7 — PCIE7_RXN
GFX_PCIE_RX_P2 BT6 — PCIE7_RXP
GFX_PCIE_TX_C_N2 BU2 — PCIE7_TXN
GFX_PCIE_TX_C_P2 BU1 — PCIE7_TXP
GFX_PCIE_RX_N3 BU9 — PCIE8_RXN
GFX_PCIE_RX_P3 BU8 — PCIE8_RXP
GFX_PCIE_TX_C_N3 BT4 — PCIE8_TXN
GFX_PCIE_TX_C_P3 BT3 — PCIE8_TXP
BP5 — PCIE9_RXN
BP6 — PCIE9_RXP
BR2 — PCIE9_TXN
BR1 — PCIE9_TXP
WLAN_PCIE_RX_N BN6 — PCIE10_RXN
WLAN_PCIE_RX_P BN5 — PCIE10_RXP
WLAN_PCIE_TX_N BR4 — PCIE10_TXN
WLAN_PCIE_TX_P BR3 — PCIE10_TXP
WWAN_PCIE_RX_N11 BN10 — PCIE11_RXN/SATA0_RXN
WWAN_PCIE_RX_P11 BN8 — PCIE11_RXP/SATA0_RXP
WWAN_PCIE_TX_N11 BN4 — PCIE11_TXN/SATA0_TXN
WWAN_PCIE_TX_P11 BN3 — PCIE11_TXP/SATA0_TXP
WWAN_PCIE_RX_N12 BL6 — PCIE12_RXN/SATA1A_RXN
WWAN_PCIE_RX_P12 BL5 — PCIE12_RXP/SATA1A_RXP
WWAN_PCIE_TX_N12 BN2 — PCIE12_TXN/SATA1A_TXN
WWAN_PCIE_TX_P12 BN1 — PCIE12_TXP/SATA1A_TXP
SSD_PCIE_RX_N3 BK6 — PCIE13_RXN
SSD_PCIE_RX_P3 BK5 — PCIE13_RXP
SSD_PCIE_TX_N3 BM4 — PCIE13_TXN
SSD_PCIE_TX_P3 BM3 — PCIE13_TXP
SSD_PCIE_RX_N2 BJ6 — PCIE14_RXN
SSD_PCIE_RX_P2 BJ5 — PCIE14_RXP
SSD_PCIE_TX_N2 BL2 — PCIE14_TXN
SSD_PCIE_TX_P2 BL1 — PCIE14_TXP
SSD_PCIE_RX_N1 BG5 — PCIE15_RXN/SATA1B_RXN
SSD_PCIE_RX_P1 BG6 — PCIE15_RXP/SATA1B_RXP
SSD_PCIE_TX_N1 BL4 — PCIE15_TXN/SATA1B_TXN
SSD_PCIE_TX_P1 BL3 — PCIE15_TXP/SATA1B_TXP
SSD_SATA_RX_N BE5 — PCIE16_RXN/SATA2_RXN
SSD_SATA_RX_P BE6 — PCIE16_RXP/SATA2_RXP
SSD_SATA_TX_N BJ4 — PCIE16_TXN/SATA2_TXN
SSD_SATA_TX_P BJ3 — PCIE16_TXP/SATA2_TXP
PCIE_RCOMPN CE6 — PCIE_RCOMP_N
PCIE_RCOMPP CE5 — PCIE_RCOMP_P
CP28 — PP_H12/M2_SKT2_CFG0
CP28 — PP_H13/M2_SKT2_CFG1
CN28 — PP_H14/M2_SKT2_CFG2
CM28 — PP_H15/M2_SKT2_CFG3

WHISKEY-LAKE-GP
ZZ.00CPU.271

PCIE1_RXN/USB31_1_RXN CB5 — USB1_USB30_RX_N
PCIE1_RXP/USB31_1_RXP CB6 — USB1_USB30_RX_P
PCIE1_TXN/USB31_1_TXN CA4 — USB1_USB30_TX_N
PCIE1_TXP/USB31_1_TXP CA3 — USB1_USB30_TX_P

IO board USB3.1

PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN BY8
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP BY9
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN CA2
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP CA1

(#545659)
The xHCI controller supports USB Debug port on all USB3.0 capable ports.

PCIE3_RXN/USB31_3_RXN BY7
PCIE3_RXP/USB31_3_RXP BY6
PCIE3_TXN/USB31_3_TXN BY4
PCIE3_TXP/USB31_3_TXP BY3

PCIE4_RXN/USB31_4_RXN BW6 — USB4_USB30_RX_N
PCIE4_RXP/USB31_4_RXP BW5 — USB4_USB30_RX_P
PCIE4_TXN/USB31_4_TXN BW2 — USB4_USB30_TX_N
PCIE4_TXP/USB31_4_TXP BW1 — USB4_USB30_TX_P

USB3.1 Type C

USB2N_1 CE3 — USB1_USB20_N
USB2P_1 CE4 — USB1_USB20_P
USB2N_2 CE1
USB2P_2 CE2
USB2N_3 CG3
USB2P_3 CG4
USB2N_4 CD3 — USB4_USB20_N
USB2P_4 CD4 — USB4_USB20_P

USB3.1 Type C

USB2N_5 CG5 — FP1_USB20_N
USB2P_5 CG6 — FP1_USB20_P

Fingerprint Reader

USB2N_6 CC1 — CCD_USB20_N
USB2P_6 CC2 — CCD_USB20_P

CAMERA

USB2N_7 CG8
USB2P_7 CG9
USB2N_8 CB8
USB2P_8 CB9
USB2N_9 CH5 — WWAN_USB20_N
USB2P_9 CH6 — WWAN_USB20_P
USB2N_10 CC3 — BT_USB20_N
USB2P_10 CC4 — BT_USB20_P
USB2_COMP CC5 — USBCOMP
USB_ID CE8 — USB2_ID
USB_VBUSSENSE CC6 — USB2_VBUSSENSE
PP_E9/USB2_OC0#/GP_BSSB_CLK CK6 — USB_OC0#
PP_E10/USB2_OC1#/GP_BSSB_DI CK5 — USB_OC1#
PP_E11/USB2_OC2# CK8 — USB_OC2#
PP_E12/USB2_OC3# CK9 — USB_OC3#
PP_E4/DEVSLP0 CP8 — SIO_EXT_SCI#
PP_E5/DEVSLP1 CR8 — SSD_DEVSLP
PP_E6/DEVSLP2 CM8 — SSD_DEVSLP
PP_E0/SATAXPCIE0/SATAGP0 CM10 — M2_SSD_PEDET#
PP_E1/SATAXPCIE1/SATAGP1 CP10 — M2_SSD_PEDET
PP_E2/SATAXPCIE2/SATAGP2 CN8
PP_E8/SATALED#/SPI1_CS1# CN7 — PCH_SATA_LED#
SVD# AR3

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

3D3V_S0
R1606 1 — 2 10KR2J-L-GP PCH_SATA_LED#
R1608 1 — 2 10KR2J-L-GP SIO_EXT_SCI#
3D3V_S5_PCH
RN1601 SRN10KJ-8-GP
1 8 USB_OC3#
2 7 USB_OC2#
3 6 USB_OC1#
4 5 USB_OC0#
R1601 1 — 2 0R2J-L-GP USB2_ID
R1602 1 — 2 0R2J-L-GP USB2_VBUSSENSE
R1603 1 — 2 113R2F-GP USBCOMP

2ND_M2_SSD_PEDET# — R1605 1 — 2 — mCARD_PCIE#_SATA
From EC
0R0402-PAD

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes 1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s) x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

(#543016)
Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 kΩ to 10 kΩ on the motherboard.
Do not use both pull-up and pull-down.
Either pull-up or pull-down is acceptable.

(#571021_CFLU) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)
Size: B | Document Number: WASP 13" WHL-U | Rev: A00
Date: Thursday, March 07, 2019 | Sheet 16 of 106

Main Func = PCH

24 SYS_PWROK
24,26 RESET_OUT#
24,40,46 VCCST_PWRGD
24,64 PCH_RSMRST#
25,45 3V_5V_PWRGD
40,91 PM_SLP_S0#
40 PM_SLP_S3#
40,51,92 PM_SLP_S4#
24 SIO_PWRBTN#
44 AC_IN#
15 INPUT3VSEL
61,63,66,76,91 PLTRST#_CPU
3 H_CPUPWRGD

20180905
EMC add

SYS_PWROK — AZ5725-01FDR7G-GP ED1701
PLTRST#_CPU — AZ5725-01FDR7G-GP ED1702
RESET_OUT# — TVL5VB1-DFN1006-2L-GP ED1703
3V_5V_PWRGD — TVL5VB1-DFN1006-2L-GP ED1704

PM_RSMRST# — AZ5725-01FDR7G-GP ED1706
VCCST_PWRGD_R — AZ5725-01FDR7G-GP ED1707

20180918
EMC Modify

1D8V_VCCPRIM
R1738 1 DY 2 10KR2J-L-GP ME_SUS_PWR_ACK_R

3D3V_VCCDSW
RN1704 1 4 AC_PRESENT
2 3 PCIE_WAKE#_CPU
SRN10KJ-GP
R1707 1 2 10KR2J-L-GP LAN_WAKE#

RTC_AUX_S5
#544669 (CRB): 330k.
R1730 1 2 330KR2J-L1-GP SM_INTRUDER#

3D3V_VCCPRIM
R1731 1 2 100KR2F-L3-GP EXT_PWR_GATE#
R1701 1 2 10KR2J-L-GP XDP_DBRESET#

3D3V_S5
R1721 1 2 10KR2J-L-GP GPD11/LANPHYPC
R1717 1 2 10KR2J-L-GP SYS_PWROK
RN1703 1 4 PM_RSMRST#
2 3 PM_PCH_PWROK
SRN100KJ-GP

SUSACK#_R R1708 1 DY 2 ME_SUS_PWR_ACK_R
0R2J-2-GP
RESET_OUT# 1 R1706 2 0R0402-PAD PM_PCH_PWROK
PM_RSMRST# 1 R1704 2 0R0402-PAD PCH_DPWROK

3D3V_S0
R1718 1 DY 2 100KR2F-L3-GP
R1716 100KR2F-L3-GP
VCCST_PWRGD 1 2 VCCST_PWRGD_R
R1719 47KR2F-GP
DY C1711 SCD1U16V2KX-3DLGP

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

CPU1K 11 OF 20

PCH_PLTRST# BJ35 — GPP_B13/PLTRST#
XDP_DBRESET# CN10 — SYS_RESET#
PM_RSMRST# BR36 — RSMRST#
H_CPUPWRGD AR2 — PROCPWRGD
VCCST_PWRGD_R BJ2 — VCCST_PWRGOOD
SYS_PWROK CR10 — SYS_PWROK
PM_PCH_PWROK BP31 — PCH_PWROK
PCH_DPWROK BP30 — DSW_PWROK
ME_SUS_PWR_ACK_R BV34 — GPP_A13/SUSWARN#/SUSPWRDACK
SUSACK#_R BY32 — GPP_A15/SUSACK#
PCIE_WAKE#_CPU BU30 — WAKE#
LAN_WAKE# BU32 — GPD2/LAN_WAKE#
GPD11/LANPHYPC BU34 — GPD11/LANPHYPC

GPP_B12/SLP_S0# BJ37 PM_SLP_S0#
GPD4/SLP_S3# BU36 PM_SLP_S3#
GPD5/SLP_S4# BU27 PM_SLP_S4#
GPD10/SLP_S5# BT29 PM_SLP_S5# 1 TP1710
SLP_SUS# BU29
SLP_LAN# BT31
GPD9/SPL_WLAN# BT30 AUX_EN_WOWL 1 TP1715
GPD6/SLP_A# BU37 PM_SLP_A# 1 TP1706
GPD3/PWRBTN# BU28 SIO_PWRBTN# 1 TP1714
GPD1/ACPRESENT BU35 AC_PRESENT
GPD0/BATLOW# BV36 PCH_BATLOW#
INTRUDER# BR35 SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# CC37 EXT_PWR_GATE#
GPP_B2/VRALERT# CC36 VRALERT# 1 TP1708
INPUT3VSEL BT27 INPUT3VSEL

WHISKEY-LAKE-GP
ZZ.00CPU.271

B ATLOW#:
Pull-up required even if not implemented.

3D3V_AUX_S5
R1727 1 2 100KR2J-1-GP
R1726 10KR2J-L-GP
Q1701
3V_5V_POK# 3
PM_RSMRST# R1702 1 2 PCH_RSMRST#
1KR2J-1-GP 3V_5V_PWRGD
PJT138KA-GP
075.00138.0A7C

3D3V_VCCDSW
R1722 10KR2J-L-GP
PCH_BATLOW#
R1723 DY 10KR2J-L-GP

Reserve by NON DS3 function 20150413

D1701 RB520S30-GP
A K AC_IN#
83.R2003.A8M
Q1702
3D3V_AUX_S5
R1737 1 2 PM_RSMRST#_M
100KR2J-1-GP
AC_PRESENT
PM_RSMRST#
2N7002KDW-1-GP
75.27002.F7C

PLTRST#_CPU
R1713 1 2 PCH_PLTRST#
0R0402-PAD
R1715 100KR2J-1-GP
DY C1701 SC220P50V2KX-3DLGP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: Custom
Document Number: WASP 13" WHL-U
Rev: A 00
Date: Thursday, March 07, 2019
Sheet 17 of 106

Main Func = PCH

For eSPI

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device3), Function0, offset DCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC. Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

GPU
WLAN
2nd SSD
SSD

Don't Change R1839,R1840 To Short Pad For RF Immunity Requirement.

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(SPI/ESPI/SMBS/XTAL/CLK)

Size	Document Number	Rev
Custom	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 | Sheet 18 of 106

Main Func = PCH

27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC

55 DMIC_SCL_CPU
55 DMIC_SDA_CPU

61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
65 KB_LED_BL_DET
24,85 DGPU_PWROK
15,27 SPKR
98 ME_FWP_SW
15 HDA_SDOUT_CPU

33 SD_PWR_EN#

33 SD_SDATA0
33 SD_SDATA1
33 SD_SDATA2
33 SD_SDATA3

33 SD_CLK
33 SD_CMD

33 SD_CD_N
33 SD_WP

CPU1G 7 OF 20

HDA_SYNC_CPU BN34 — HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 — HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 — HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 — HDA_SDI0/I2S0_RXD
TP1903 TPAD14-OP-GP
HDA_RST_N_CPU BL36 — HDA_SDI1/I2S1_RXD/SNDW1_DATA
KB_LED_BL_DET BL35 — HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 — GPP_D23/I2S_MCLK
BL37 — I2S1_SFRM/SNDW2_CLK
BL34 — I2S1_TXD/SNDW2_DATA

GPP_H1_SFRM CJ32 — GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 — GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
GPP_H2_CLKREQ0 CH29 — GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 — GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DMIC_SCL_CPU CP24 — GPP_D19/DMIC_CLK0/SNDW4_CLK
DMIC_SDA_CPU CN24 — GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_A16/SD_1P8_SEL
TPM_ID CK25 — GPP_D17/DMIC_CLK1/SNDW3_CLK
DGPU_PWROK CJ25 — GPP_D18/DMIC_DATA1/SNDW3_DATA
SD_1P8_RCOMP
SD_3P3_RCOMP
SPKR CF35 — GPP_B14/SPKR

GPP_G0/SD_CMD CH36 SD_CMD
GPP_G1/SD_DATA0 CL35 SD_SDATA0
GPP_G2/SD_DATA1 CL36 SD_SDATA1
GPP_G3/SD_DATA2 CM35 SD_SDATA2
GPP_G4/SD_DATA3 CN35 SD_SDATA3
GPP_G5/SD_CD# CH35 SD_CD_N
GPP_G6/SD_CLK CK36 SD_CLK
GPP_G7/SD_WP CK34 SD_WP

BW36 SD_PWR_EN#
BY31
CK33 SD_RCOMP — R 19011 200R2F-L-GP — 2
CM34

GP

WHISKEY-LAKE-GP
ZZ.00CPU.271

3D3V_S5
R1910 10KR2J-L-GP
fTPM
TPM_ID
R1911 10KR2J-L-GP
TPM

HDA_SYNC_CODEC — R 19081 — 2 — 0R2J-L-GP — HDA_SYNC_CPU

Layout Note: R1920 & R1921 need to close for merge prepare

HDA_BITCLK_CODEC — R 19201 — 2 — 0R2J-L-GP — HDA_BITCLK_CPU
HDA_SDOUT_CODEC — R 19211 — 2 — 33R2F-3-GP — HDA_SDOUT_CPU

ME_FWP_SW — R 19091 — 2 — 1KR2J-1-GP

BT_PCMFRM_RSTN — R 19131 — 2 — 33R2F-3-GP — GPP_H1_SFRM
BT_PCMOUT_CLKREQ0 — R 19121 — 33R2F-3-GP — GPP_H2_CLKREQ0

HDA_BITCLK_CODEC
DY E C1901 SC10P50V2JN-4DLGP
20180904 EMC add

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

<Core Design>

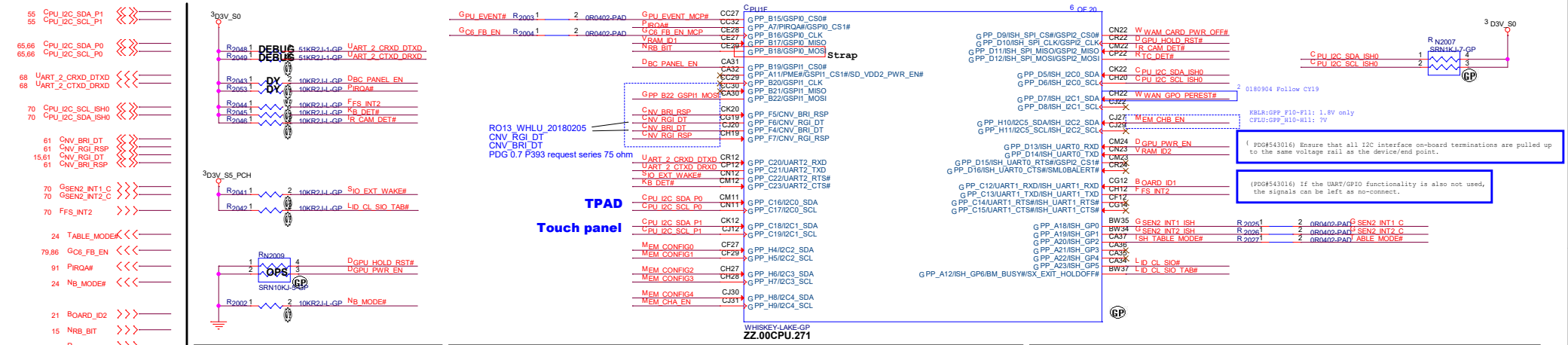
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

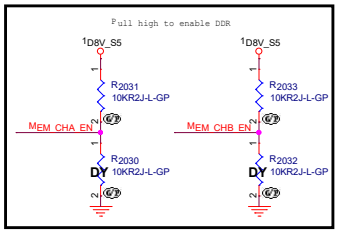
Title: **CPU (HDA/I2S/SD/DMIC)**

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 Sheet 19 of 106

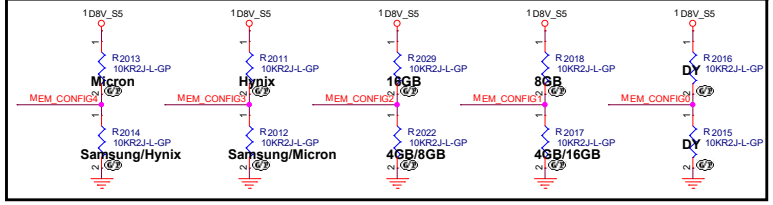
Main Func = PCH





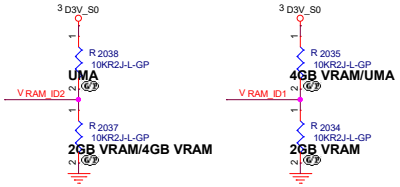
CY19 MEM_CONFIG Mapping table

ID	Description	Setting	Mapping
MEM_CONFIG[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	SDP/DDP Configuration	1	SDP
		0	DDP



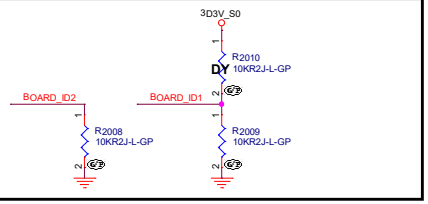
CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



CY19 Board ID Mapping table

ID	Description	Setting	Mapping
Board ID[2:1]	Board SKU ID	11	KBL-U
		10	KBL-R
		01	N/A
		00	SKL-U



<Core Design>
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)

Size: C custom | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 20 of 106

Main Func = PCH

15 GPD_7
15 GPP_H21
15 GPP_H23
18 PROJECT_ID0
20 BOARD_ID2
40 GPPC_H18_VCCIO_LPM
55 TOUCH_DETECT
21,61 CNV_WR_CLK_DP
21,61 CNV_WR_CLK_DN
21,61 CNV_WR_CLK_DP
21,61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1
61 WIFI_RF_EN
61 BLUETOOTH_EN
61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
66 WWAN_BB_RST#

3D3V_S0

R2110 1 DY 2 10KR2J-L-GP SPK_ID
R2101 1 2 150R2F-1-GP CNV_WT_RCOMP
R2108 1 2 200R2F-L-GP EMMC_RCOMP

TOUCH_DETECT 1 R2102 2 TOUCH_DETECT_R
0R0402-PAD

GPPC_H18_BOOTMPC 1 R2119 2 GPPC_H18_VCCIO_LPM
0R0402-PAD

R2120 1 DY 2 75KR2J-GP WWAN_BB_RST#

CPU1I 9 OF 20

CNV_WR_DN0 CR30
CNV_WR_DP0 CP30
CNV_WR_DN1 CM30
CNV_WR_DP1 CN30
CNV_WT_DN0 CN32
CNV_WT_DP0 CM32
CNV_WT_DN1 CP33
CNV_WT_DP1 CN33
CNV_WR_CLK_DN CN31
CNV_WR_CLK_DP CP31
CNV_WT_CLK_DN CP34
CNV_WT_CLK_DP CN34
CNV_WT_RCOMP CP32
CR32
CP20
PROJECT_ID1 CK19
PROJECT_ID2 CG17
SPK_ID CR14
BLUETOOTH_EN CP14
TOUCH_DETECT_R CN14
BOARD_ID2 CM14
CJ17
CH17
WWAN_BB_RST# CF17

CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_RCOMP#CP32
CNV_WT_RCOMP#CR32
GPP_F0/CNV_PA_BLANKING
GPP_F1
GPP_F2
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_F8/CNV_MFUART2_RXD
GPP_F9/CNV_MFUART2_TXD
GPP_F23/A4WP_PRESENT

GPP_H18/CPU_C10_GATE# CN27 G PPC_H18_BOOTMPC
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 G PP_H21
GPP_H22 CN26
GPP_H23 CM26 G PP_H23
GPP_F10 CK17
GPD7 BV35 G PD_7
GPP_F3 CN20 P ROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 W IFI_RF_EN
GPP_H20/IMGCLKOUT1 CH25
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16
EMMC_RCOMP CK15 E MMC_RCOMP

GPP_F:
VCCPGPPF = 1.8V Only

WHISKEY-LAKE-GP
ZZ.00CPU.271

PROJECT_ID[1:0]

1D8V_VCCPRIM
R2111 10KR2J-L-GP PROJECT_ID1
R2112 DY 10KR2J-L-GP
1D8V_VCCPRIM
R2113 DY 10KR2J-L-GP PROJECT_ID0
R2114 10KR2J-L-GP

PROJECT_ID[3:2]

1D8V_VCCPRIM
R2117 10KR2J-L-GP
Inspiron/Vostro
PROJECT_ID3
R2118 10KR2J-L-GP
Latitude
1D8V_VCCPRIM
R2115 10KR2J-L-GP
Inspiron/Latitude
PROJECT_ID2
R2116 10KR2J-L-GP
Vostro

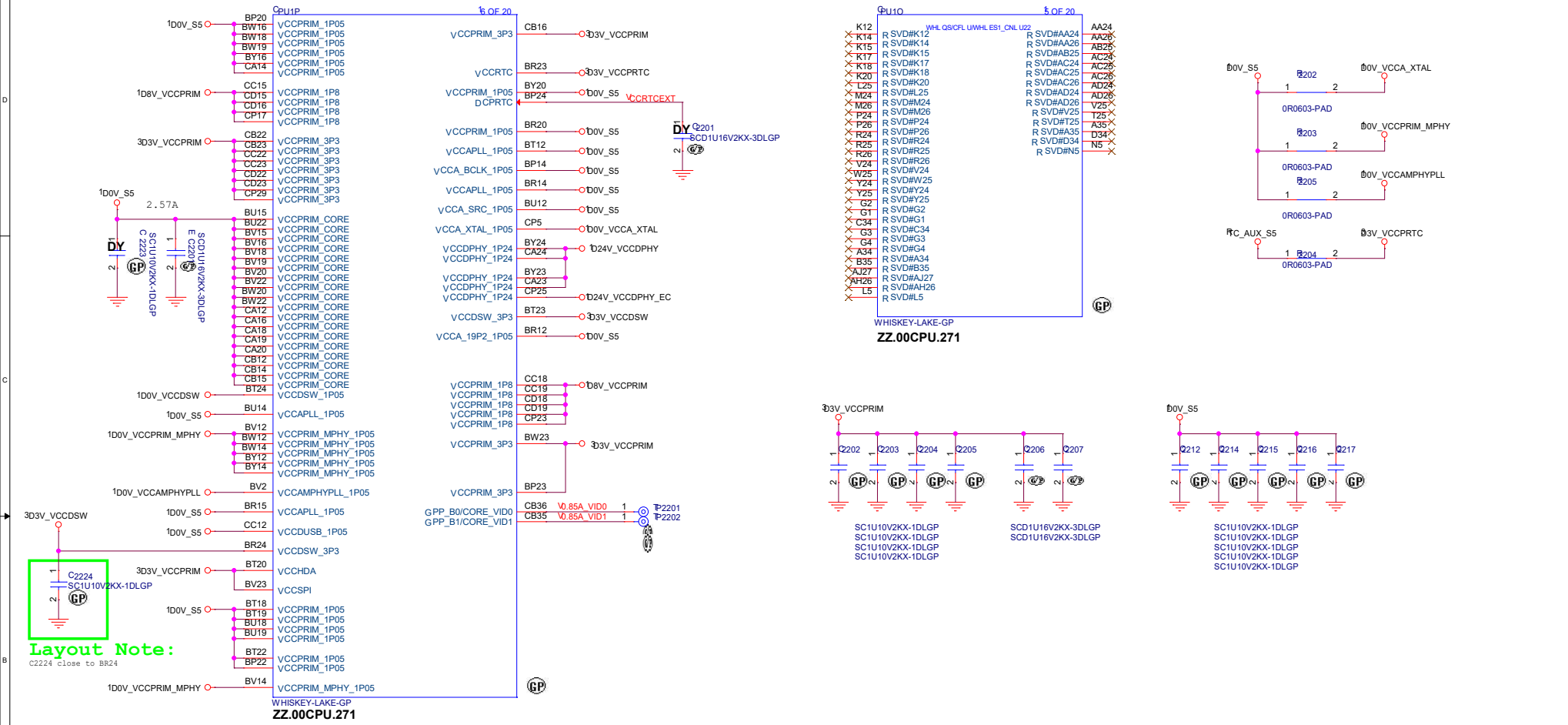
ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Sereis
		01	7000 Sereis
		00	N/A

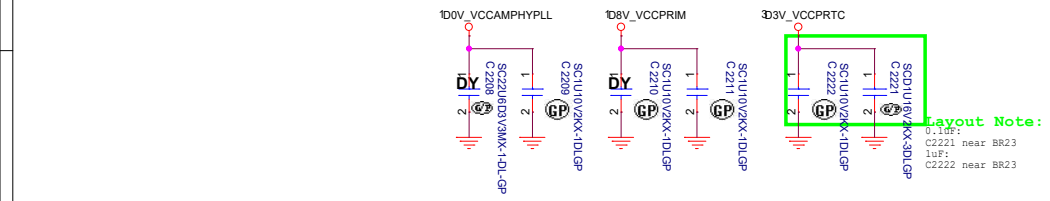
<Core Design>

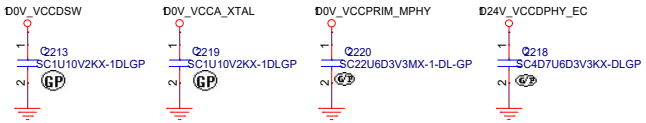
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER1)
Size: A4
Document Number: WASP 13" WHL-U
Rev: A00
Date: Thursday, March 07, 2019
Sheet 21 of 106

Main Func = PCH







<Core Design>

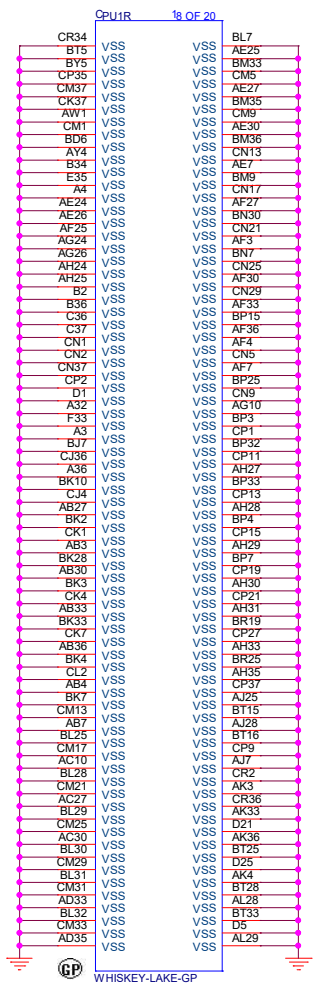
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(RSVD)

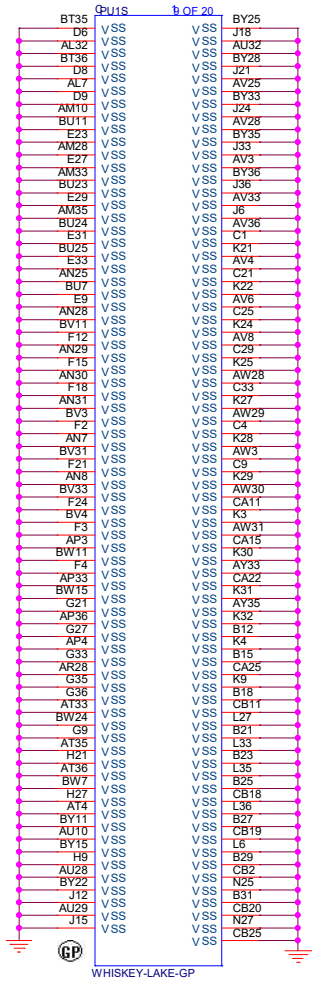
Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 22 of 106

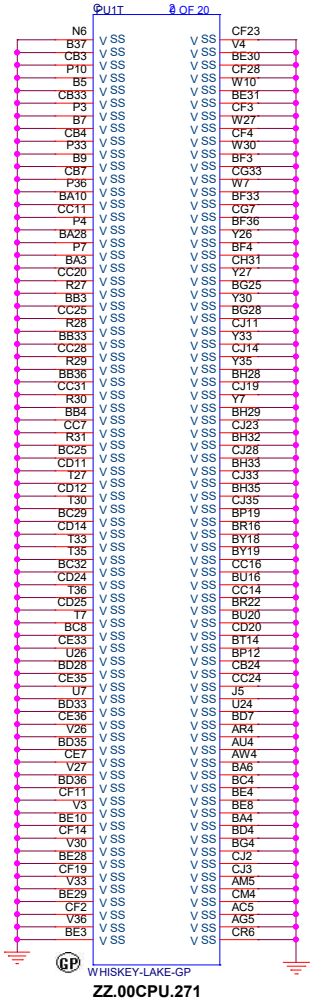
Main Func = PCH



ZZ.00CPU.271



ZZ.00CPU.271



ZZ.00CPU.271

<Core Design>

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2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 23 of 106

Main Func = KBC

RTC GEN 9 reset circuit

Layout Note:
Need very close to EC

BATTER /CHARGER
CPU/ Thermal/TYPEC

For eSPI

Power Switch Logic(PSL)

BOARD_ID VERSION_A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Waps_X00	100.0K	10.0K	3.0V
Waps_X01	100.0K	17.8K	2.801V
Waps_X02	100.0K	27.0K	2.598V
Waps_A00	100.0K	37.4K	2.402V
Waps_X03	100.0K	49.9K	2.201V
Waps_X04	100.0K	64.9K	2.001V
Waps_X05	100.0K	82.5K	1.808V
Waps_A01	100.0K	107K	1.594V
Waps_A02	100.0K	154K	1.299V
Waps_A03	100.0K	200K	1.100V

MODEL_ID_DET (GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K	3.0V
TBD	100.0K	17.8K	2.801V
Waps 13" UMA	100.0K	27.0K	2.598V
TBD	100.0K	37.4K	2.402V
TBD	100.0K	49.9K	2.201V
Waps 13" DIS	100.0K	64.9K	2.001V
TBD	100.0K	82.5K	1.808V
TBD	100.0K	107K	1.594V
TBD	100.0K	154K	1.299V
TBD	100.0K	200K	1.100V

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

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Taipei Hsien 221, Taiwan, R.O.C.

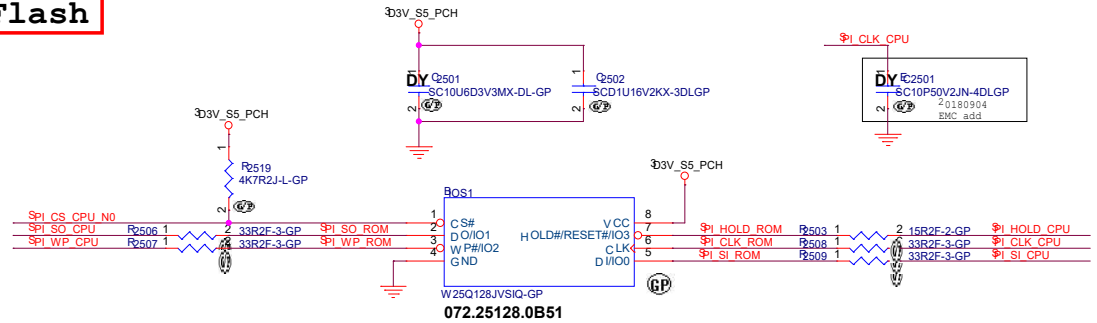
Title: KBC Nuvoton MEC1416

Size: C | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 24 of 106

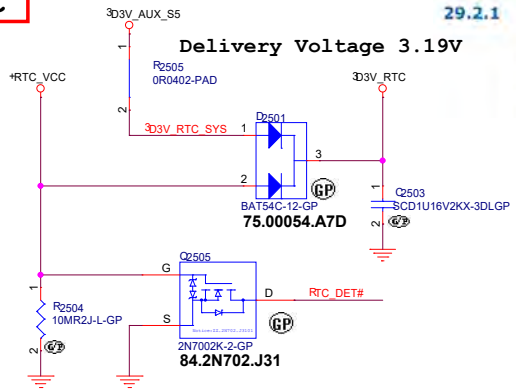
Main Func = SPI Flash

15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU
18 SPI_CS_CPU_N0
18,91 SPI_CLK_CPU
15,18,91 SPI_SI_CPU
18,91 SPI_SO_CPU



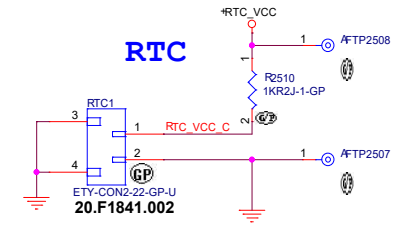
Main Func = RTC

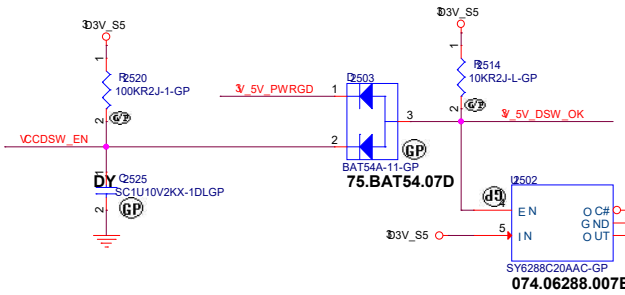
24 RTCRST_ON
24 VCCDSW_EN
17,45 3V_5V_PWRGD
52,53 3V_5V_DSW_OK
15,20 RTC_DET#

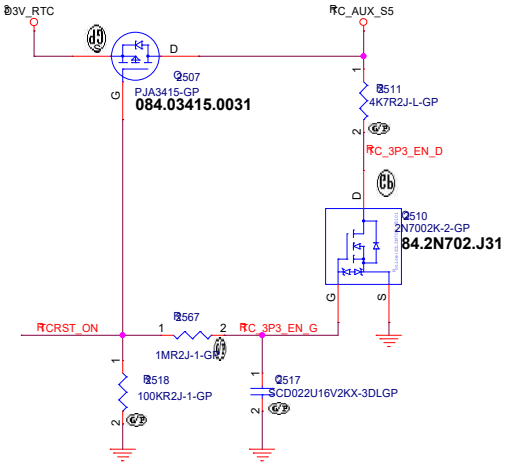


29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.







<Core Design>

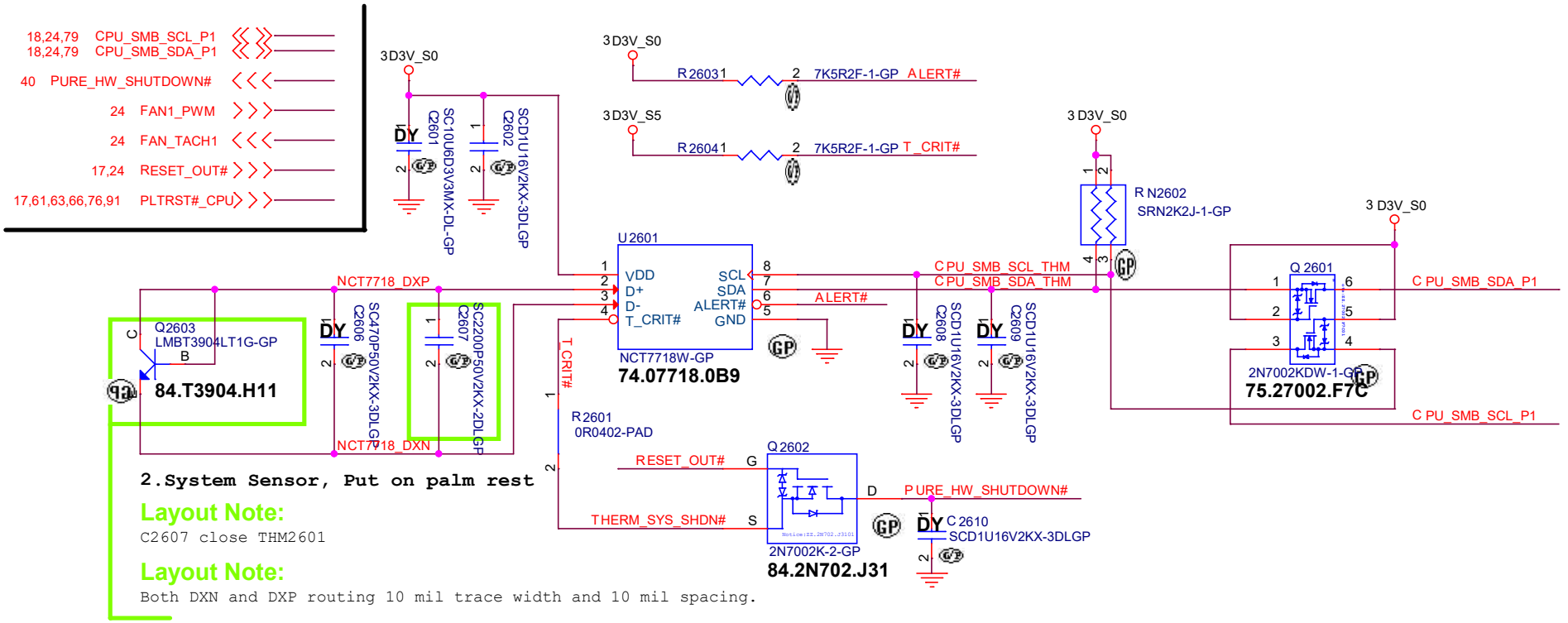
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 25 of 106

Main Func = Thermal Sensor



2.System Sensor, Put on palm rest

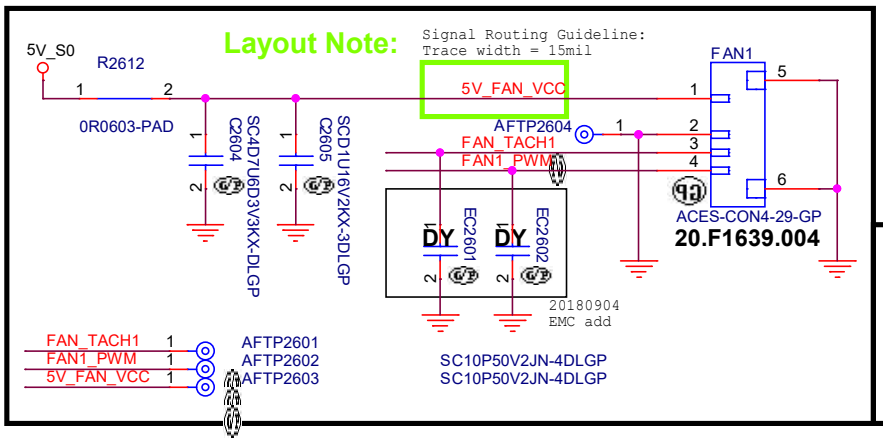
Layout Note:

C2607 close THM2601

Layout Note:

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 26 of 106

Audio Codec Chip ALC3204

Main Func = Audio

19 HDA_SDIN0_CPU
19 HDA_SDOUT_CODEC
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC

29 AUD_SPK_R+
29 AUD_SPK_R-
29 AUD_SPK_L+
29 AUD_SPK_L-

55 DMIC_SCL_CODEC
55 DMIC_SDA_CODEC

17,40 PM_SLP_S3#
29,66 AUD_SENSE
24 NB_MUTE#
15,19 SPKR
24 BEEP
29,66 AUD_RING
29,66 AUD_SLEEVE

29 LINE1_L
29 LINE1_R

29 LINE1_VREFO
29 MIC2_VREFO_R

29,66 AUD_HP1_JACK_L
29,66 AUD_HP1_JACK_R

DVDD must >= DVDD_IO

3D3V_S0 — R2715 0R0603-PAD — +3V_1D8V_DVDD
C2740 SC2D2U10V3KX-1DLGP-U
C2741 SCD1U16V2KX-3DLGP

5V_S0 — R2701 0R0805-PAD — +5V_PVDD
R2707 0R0805-PAD

1D8V_S0 — R2709 0R0402-PAD — 1D8V_CPVDD

moat
Analog
Digital

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is unavailable, please make sure that switch frequency operates at out-band(over 20KHz)

1D8V_S0 — R2719 0R0402-PAD — C2710 SC10U6D3V3MX-DL-GP — AUD_AGND

+5V_PVDD >2A
C2713 SC10U6D3V3MX-DL-GP
C2714 SCD1U16V2KX-3DLGP
C2717 SC10U6D3V3MX-DL-GP
C2718 SCD1U16V2KX-3DLGP

C2711 SC10U6D3V3MX-DL-GP — LDO2_CAP — +3V_1D8V_AVDD

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_R-
AUD_SPK_R+

PDB_R

ALC3204
QFN40 (5X5)
071.03204.0003
ALC3204-CG-GR-U

AUD_HP1_JACK_L
AUD_HP1_JACK_R

1D8V_CPVDD — C2705 SC2D2U10V3KX-1DLGP-U; C2704 SCD1U16V2KX-3DLGP; C2708 SC2D2U10V3KX-1DLGP-U; C2709 SCD1U16V2KX-3DLGP

Q2702 SC2D2U10V3KX-1DLGP-U
R2702 100KR2J-1-GP
C2703 SC2D2U10V3KX-1DLGP-U

U2701 pins: CBP, CPVDD, CBN, CPVEE, HP-OUT-R, HP-OUT-L, LINE1-VREFO-L, MIC2-VREFO, VREF, LDO1-CAP, AVDD1, AVSS1, LINE1-L, LINE1-R, D33STB, MIC2-CAP, LEEV/MIC2-R, RING2/MIC2-L, HP/LINE1-JD_JD1, CBEEP, AVSS2, LDO2-CAP, AVDD2, PVDD1, SPK-L+, SPK-L-, SPK-R-, SPK-R+, PVDD2, PDB, GND, DVDD, GPIO0/DMIC-DATA12, GPIO1/DMIC-CLK, SDATA-OUT, BIT-CLK, LDO3-CAP, SDATA-IN, DVDD-IO, SYNC, DC_DET

LINE1_L
LINE1_R
D33_STB
MIC_CAP — C2715 SC10U6D3V3MX-DL-GP
AUD_SLEEVE
AUD_RING
AUD_HPJD_N
AUD_PC_BEEP

+5V_AVDD — moat — +5V_S0
R2703 0R0603-PAD
C2707 SC10U6D3V3MX-DL-GP
C2709 SCD1U16V2KX-3DLGP
AUD_AGND

Layout Note:
Place close to Pin 20

+3V_1D8V_DVDD
C2720 SC10U6D3V3MX-DL-GP
C2721 SCD1U16V2KX-3DLGP
place close to pin1

C2722 SC4D7U6D3V3KX-DLGP
place close to pin8

Q2722 SC10U6D3V3MX-DL-GP

Analog
Digital
moat

DMIC_SDA_CODEC
DMIC_SCL_CODEC
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC_R
LDO3_CAP
HDA_CODEC_SDIN0
HDA_SYNC_CODEC
DVSS

Azalia I/F EMI
HDA_SDOUT_CODEC — EC2707 SC22P50V2JN-8-GP
HDA_BITCLK_CODEC — EC2711 SC22P50V2JN-8-GP
DMIC_SDA_CODEC — EC2710 SC22P50V2JN-8-GP
DMIC_SCL_CODEC — EC2706 SC33P50V2JN-3DLGP
20180911 Vendor add

SPKR — R2741 0R0402-PAD — HDA_SPKR_R — D2703 BAT54C-12-GP — AUD_PC_BEEP_C — C2735 SCD1U16V2KX-3DLGP — AUD_PC_BEEP
BEEP — R2734 0R0402-PAD — KBC_BEEP_R
R2735 1KR2J-1-GP
DY C2739 SC100P50V2JN-3DLGP
75.00054.A7D

+3V_1D8V_DVDD — R2717 100KR2J-1-GP — R2712 0R0402-PAD — NB_MUTE#
20180911 Vendor stuff

+3V_1D8V_DVDD — R2710 100KR2J-1-GP — R2711 200KR2F-L-GP — AUD_SENSE — AUD_HPJD_N

moat
20180904 EMC modify
EC2701 EC2702 EC2703 EC2704 EC2705 SC1KP50V2KX-1DLGP
AUD_AGND

R2704 R2705 R2706 0R0603-PAD
AUD_AGND

Layout Note:
Tied at point only under Codec or near the Codec

Open drain output. pull up to DVDD or max. 5V
For RTC Gen9 reset circuit change power rail. 20170921

3D3V_RTC — R2708 0R0402-PAD — VSD3_STB
3D3V_S0 — R2716 DY 100KR2J-1-GP — DVSS

HDA_SDIN0_CPU — R2724 22R2J-L1-GP — HDA_CODEC_SDIN0
HDA_BITCLK_CODEC — R2723 22R2J-L1-GP — HDA_BITCLK_CODEC_R

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204
Size: B
Document Number: WASP 13" WHL-U
Rev: A00
Date: Thursday, March 07, 2019
Sheet 27 of 106

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 Sheet 28 o f 106

Main Func = Audio

Speaker

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L-
27 AUD_SPK_L+

AUD_SPK_R+ ER2901 1 2 0R3J-0-U-GP AUD_SPK_R+_C
AUD_SPK_R- ER2902 1 2 0R3J-0-U-GP AUD_SPK_R-_C
AUD_SPK_L+ ER2903 1 2 0R3J-0-U-GP AUD_SPK_L+_C
AUD_SPK_L- ER2904 1 2 0R3J-0-U-GP AUD_SPK_L-_C

SPK1
ACES-CON4-29-GP
20.F1639.004

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

C2902 C2901 C2903 C2904
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP

AUD_SPK_L-_C AUD_SPK_L+_C AUD_SPK_R-_C AUD_SPK_R+_C
AFTP2901
AFTP2902
AFTP2903
AFTP2904

20180911
Vendor modify

27 LINE1_VREFO
27 MIC2_VREFO_R
27,66 AUD_HP1_JACK_L
27,66 AUD_HP1_JACK_R
27 LINE1_L
27 LINE1_R
27,66 AUD_SLEEVE
27,66 AUD_RING
27,66 AUD_SENSE

LINE1_VREFO
D2901
BAW56-9-GP-U
75.00056.07D
LINE1_VREFO_L
LINE1_VREFO_R
RN2902
SRN4K7J-8-GP
RN2901
SRN2K2J-1-GP
MIC2_VREFO_R
AUD_RING
AUD_HP1_JACK_L
LINE1_L C29071 2 SC10U6D3V3MX-DL-GP
AUD_HP1_JACK_R
LINE1_R C29081 2 SC10U6D3V3MX-DL-GP
AUD_SLEEVE

20180911
Vendor modify

AUD_SENSE 10 mils
DY C2909
SC10U6D3V3MX-DL-GP
AUD_AGND

<Core Design>

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Title: Audio IO

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 29 of 106

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 30 o f 106

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN RTL8106

Size	Document Number	Rev
A 4	***WASP 13" WHL-U***	***A 00***

Date: Thursday, March 07, 2019	Sheet 31 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 | Sheet 32 of 106

Main Func = Card Reader

19 SD_SDATA0
19 SD_SDATA1
19 SD_SDATA2
19 SD_SDATA3
19 SD_CD_N
19 SD_CLK
19 SD_CMD
19 SD_PWR_EN#
19 SD_WP

NO.	PIN #	FUNCTION
1	#9	DAT2
2	#1	CD/DAT3
3	#2	CMD
4	#3-1	VSS
5	#3-2	VSS
6	#4	VDD
7	#5	CLD
8	CD	CARD DETECT
9	#6	VSS
10	#7	DATO
11	#8	DATI
12	WP1	WRITE PROTECT(VSS)
13	WP2	WRITE PROTECT(VDD)
14	FRAME	GND
15	FRAME	GND
16	FRAME	GND
17	FRAME	GND

	WRITE PROTECT SWITCH		CARD DETECT SWITCH
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UN INSERTION	OPEN		OPEN
CARD HALF INSERTION	CLOSE		OPEN
CARD INSERTION	OPEN	CLOSE	CLOSE

N/O — OPEN — CLOSE

3D3V_S5 — R3301 0R0603-PAD — 3D3V_CARD_S5
SCD1U16V2KX-3DLGP C3309
SC4D7U6D3V3KX-DLGP C3302

U3301 RTS5100-GR-GP
071.05100.0003

DV3318_S_PAD 5
DV3318_ANA_CORE 9
3D3V_CARD 10
3D3V_CARD_S5 11, 26
DV3318_HOST 13
VIO_18 14
DV12S 20

C_SD_D0 18
C_SD_D1 17
C_SD_D2 23
C_SD_D3 22
C_SD_CMD 21
C_SD_CLK 19
C_SD_CD# 24
C_SD_WP 25

GPIO0 31
GPIO1 30
FWP/GPIO2 29
GPIO3 28
GPIO4 27

SD_1P8_SEL 1
CD_WP_REV# 12
SD_PWR_EN# 32

GND 33

SD_SDATA0 R33171 0R2J-L-GP → SD_SDATA0_R 7
SD_SDATA1 R33181 0R2J-L-GP → SD_SDATA1_R 8
SD_SDATA2 R33191 0R2J-L-GP → SD_SDATA2_R 2
SD_SDATA3 R33201 0R2J-L-GP → SD_SDATA3_R 3
SD_CMD R33151 0R2J-L-GP → SD_CMD_R 4
SD_CLK R33161 0R2J-L-GP → SD_CLK_R 6
SD_CD_N → 15
SD_WP → 16

H_SD_D0 H_SD_D1 H_SD_D2 H_SD_D3 H_SD_CMD H_SD_CLK H_SD_CD# H_SD_WP

C_SD_D0 R33101 0R2J-L-GP C ARD_SDATA0
C_SD_D1 R33111 0R2J-L-GP C ARD_SDATA1
C_SD_D2 R33061 0R2J-L-GP C ARD_SDATA2
C_SD_D3 R33071 0R2J-L-GP C ARD_SDATA3
C_SD_CMD R33081 0R2J-L-GP C ARD_CMD
C_SD_CLK R33091 0R2J-L-GP C ARD_CLK
C ARD_CD_N
C_SD_WP
C 3301 SC6P50V2CN-1-NL-GP

U 3301_GPIO0 R 33141 DY 0R2J-L-GP
F WP/GPIO2 R 33221 DY 0R2J-L-GP
G PIO3 R 33231 DY 0R2J-L-GP
G PIO4

S D_1P8_SEL R 33261 DY 0R2J-L-GP
C D_WP_REV# R 33241 DY 0R2J-L-GP
S D_PWR_EN# R

U 3301_GPIO0 1 — A FTP3301
U 3301_GPIO1 1 — A FTP3302

DV3318_S_PAD
SCD1U16V2KX-3DLGP C3305
SC2D2U10V3KX-1DLGP-U C3304

DY C3313 SC6P50V2CN-1-NL-GP

DV3318_ANA_CORE
SCD1U16V2KX-3DLGP C3308
SC2D2U10V3KX-1DLGP-U C3307

DV3318_HOST
DV12S
C3310 C3311
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

3D3V_S5
R3331 1KR2F-3-GP
DY
SD_WP
R3332 1KR2F-3-GP

3 D3V_CARD
SC4D7U6D3V3KX-DLGP C3312
SCD1U16V2KX-3DLGP C3303

C ARD1
VDD 4
DAT0 7
DAT1 8
DAT2 1
CD/DAT3 2
CLK 5
CMD 3
VSS 9 10
VSS 6 11
12 13 14
C ARD_CD_N
C ARD_SDATA0
C ARD_SDATA1
C ARD_SDATA2
C ARD_SDATA3
C ARD_CLK
C ARD_CMD
SDCARD-8P-10-GP
62.10051.I71

C_SD_WP
R 3333 1KR2F-3-GP

3D3V_S5
R3325 10KR2J-L-GP
SD_PWR_EN# R33291 2 0R0402-PAD SD_PWR_EN#_R

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5100

Size	Document Number	Rev
A4	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 — Sheet 33 of 106

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 Sheet 34 o f 106

SSID = USB3.0

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB switch

Size	Document Number	Rev
	WASP 13" WHL-U	A 00

Date: Thursday, March 07, 2019 | Sheet 3 5 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
USB30

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

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(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 | Sheet 37 of 106

Main Func = USB3.0 Redriver

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

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(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

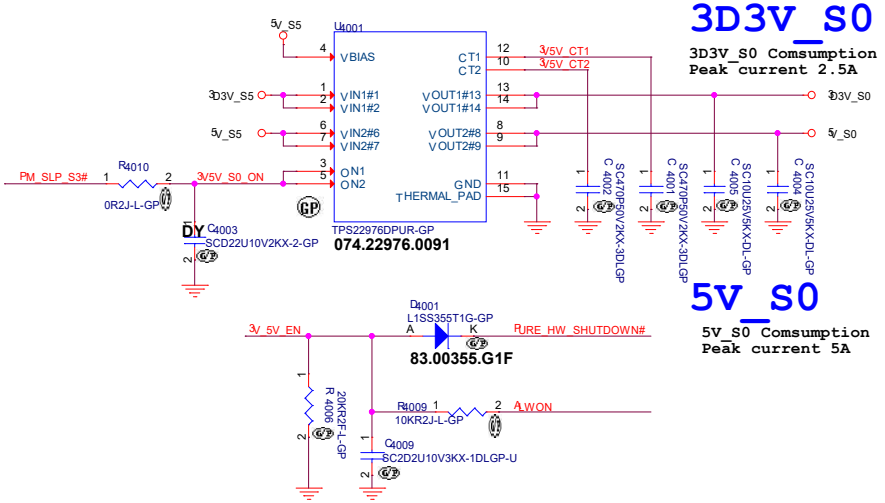
Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 Sheet 39 o f 106

Main Func = Power Plane & Sequence

17 PM_SLP_S3#
17,24,46 VCCST_PWRGD
17,51,92 PM_SLP_S4#
17,91 PM_SLP_S0#
21 GPPC_H18_VCCIO_LPM
24 ALWON
24,53 PRIM_PWRGD
26 PURE_HW_SHUTDOWN#
45 3V_5V_EN
51 PWR_VDDQ_PG

ROSA Run Power



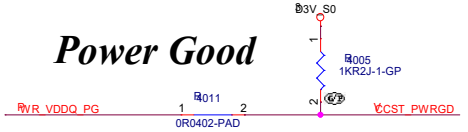
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

5V_S0

5V_S0 Comsumption
Peak current 5A

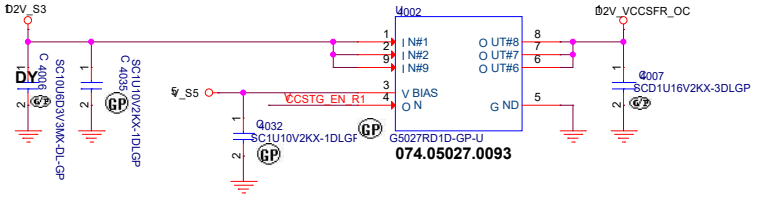
Power Good



[#543016] Optional, Added for addition system robustness

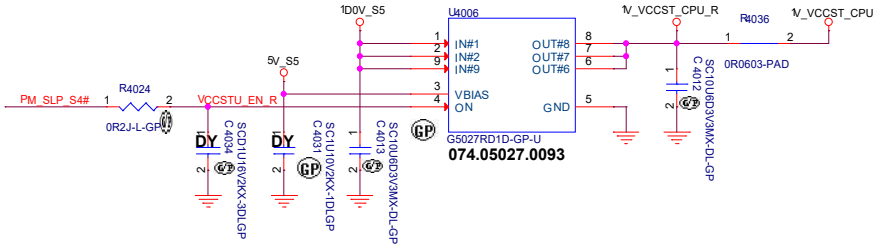
NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

VCCSFR_OC

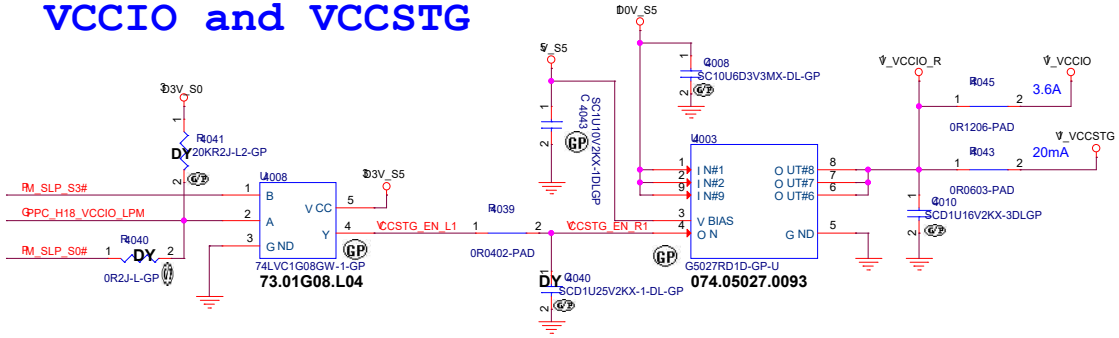


MANAGEMENT RAIL POWER GENERATION

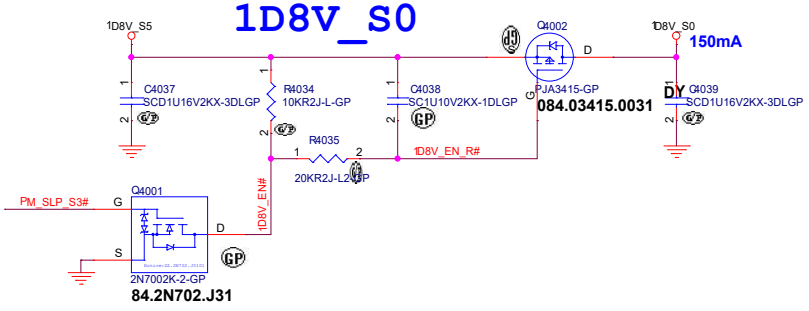
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.



VCCIO and VCCSTG



1D8V_S0



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
B	WASP 13" WHL-U	A00

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(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 Sheet 41 o f 106

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

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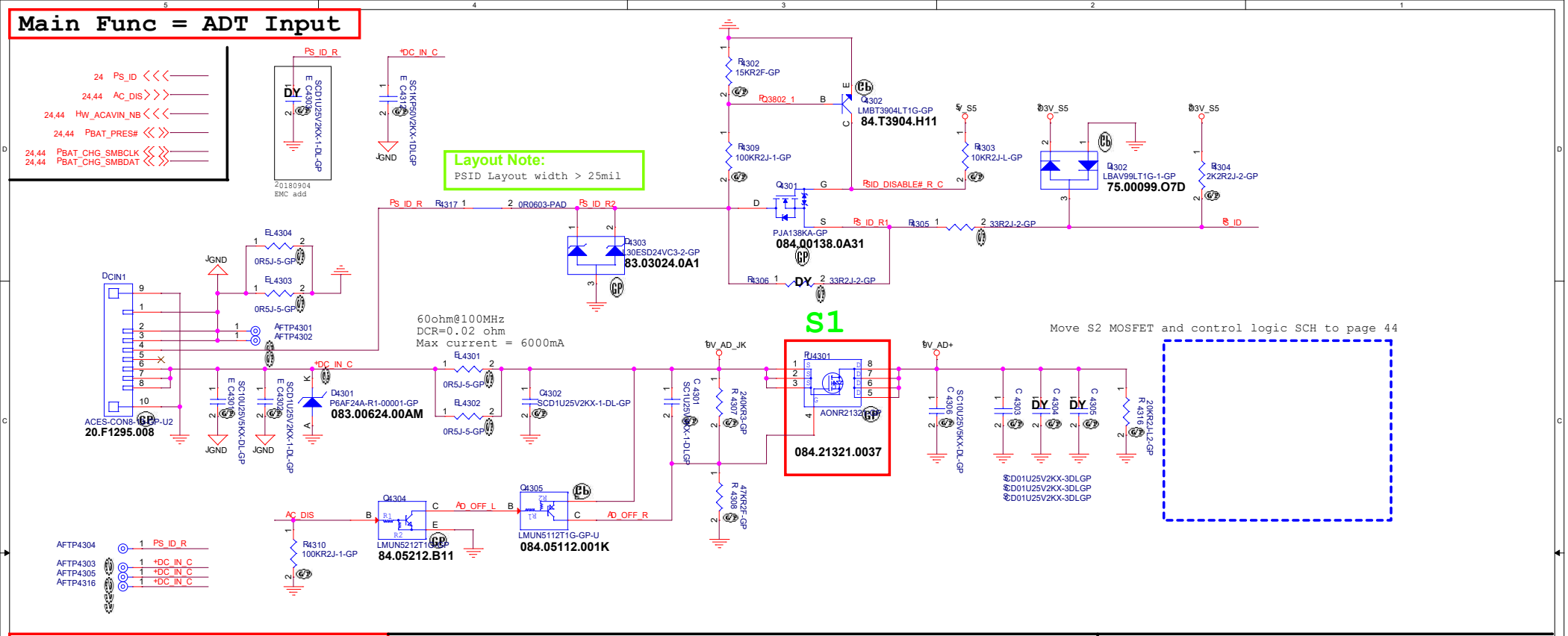
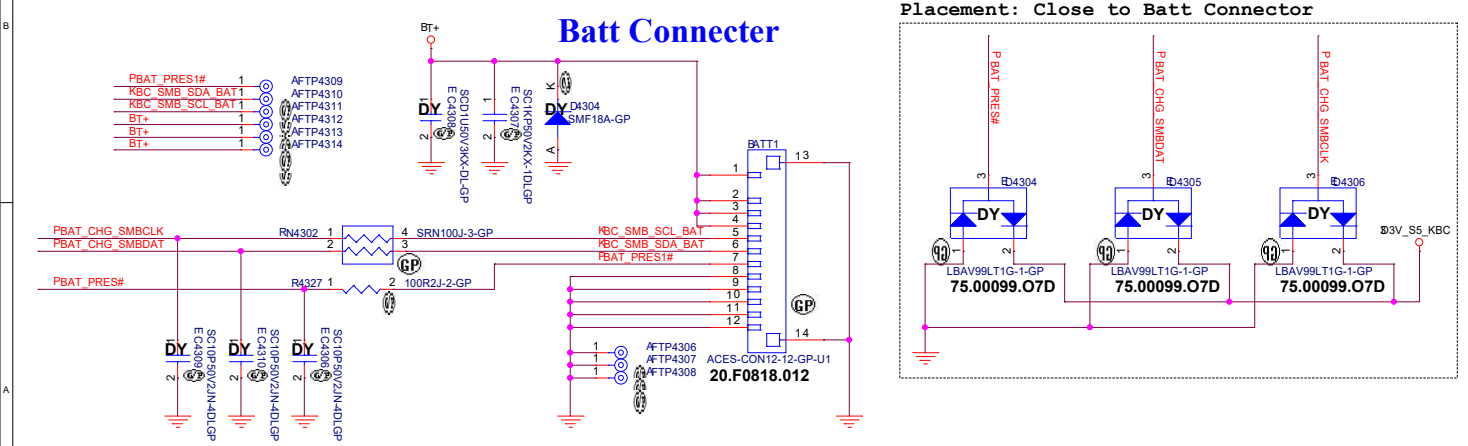
Main Func = ADT Input

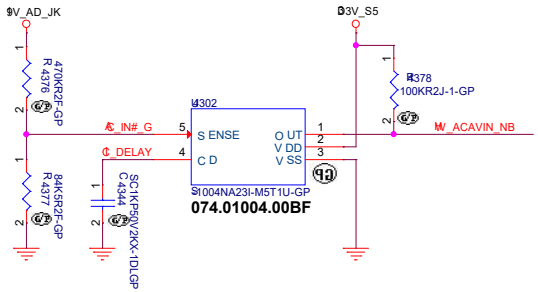


Main Func = M-BAT Input



Placement: Close to Batt Connector

Barrel Adapter Piug-in Detect



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 43 of 106

Main Func = Charger

ISL9538H For Charger

OFFPAGE

From MCP ACK

	ISL9538H	ISL95522
PR4468	100K(63.10434.10L)	100K(64.R0005.6DL)
PC4469	1500p(78.15224.2FLDL)	DY
PQ4451	084.02421.0031	DY
PR4469	DY	0R(64.R0005.6DL)
PR4441	DY	0R(64.R0005.6DL)
PR4440	0R(64.R0005.6DL)	DY
PR4471	0R(64.R0005.6DL)	DY
PR4470	DY	0R(64.R0005.6DL)

S2

084.21321.0037

75.27002.F7C

75.00054.A7D

83.R2003.A8M

068.2R210.2351
10mm x 11.2mm
x 2mm
DCR=8~9mohm
Idm=13A
Iset=10A

075.07321.0073

084.03305.0037

+3D3V_VDD_DCIN

20V>+DC_IN>4.7V

E-LDO

74.02204.03F

Vout=1.24*(1+(R1/R2))

Vcore_OVP

Trigger Voltage
VDD=4.5V, Vcore > 1.88V
VDD= 5V, Vcire > 2.084V
VDD=5.5V, Vcire > 2.3V

74.00331.H2F

83.00355.G1F

Vsys_UVP

Trigger Voltage
VDD=4.5V, DCBATOUT < 5.39V
VDD= 5V, DCBATOUT < 5.98V
VDD=5.5V, DCBATOUT < 6.58V

74.00331.H2F

83.00355.G1F

75.27002.F7C

PU +VCCSTG = 1.0 V on CPU side

84.2N702.J31

Barrel Prochot
Follow custormer circuits.

TypeC Prochot
Follow custormer circuits.

Wistron Corporation

Power (Charger_ISL9538)

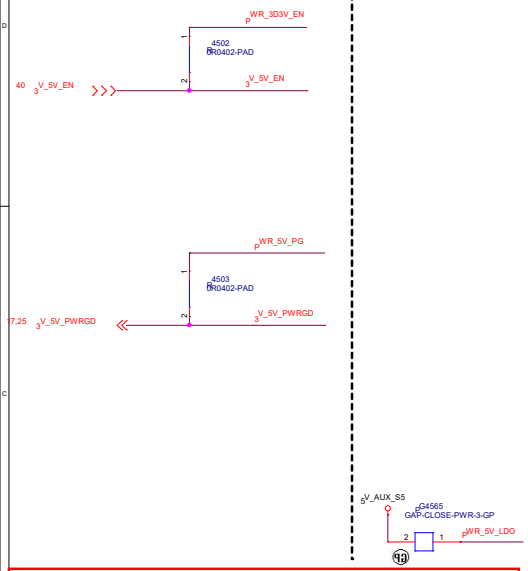
W ASP 13" WHL-U

Thursday, March 07, 2019

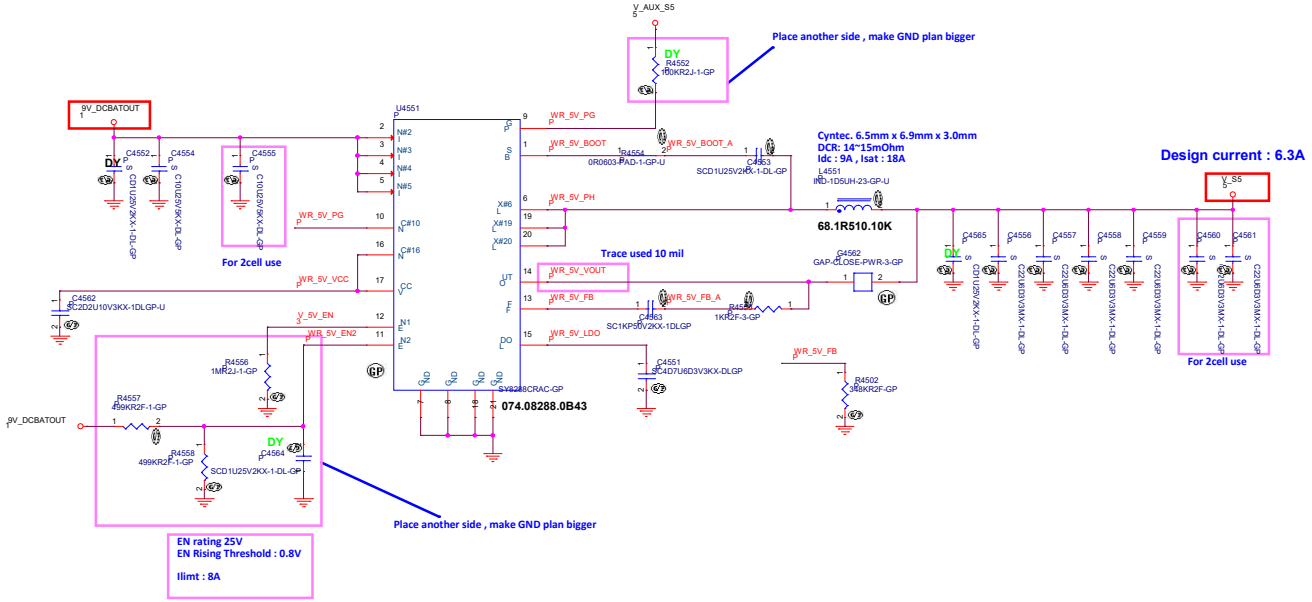
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP



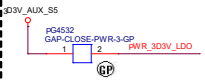
SY8288C For 5V



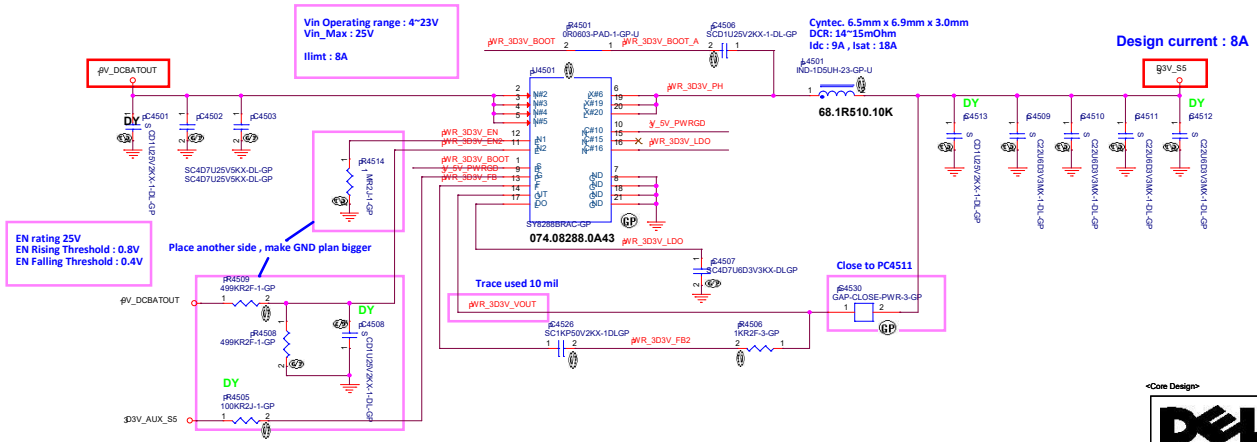
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



SY8288B For 3D3V



<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 45 of 108

Main Func = CPU_CORE

OFFPAGE

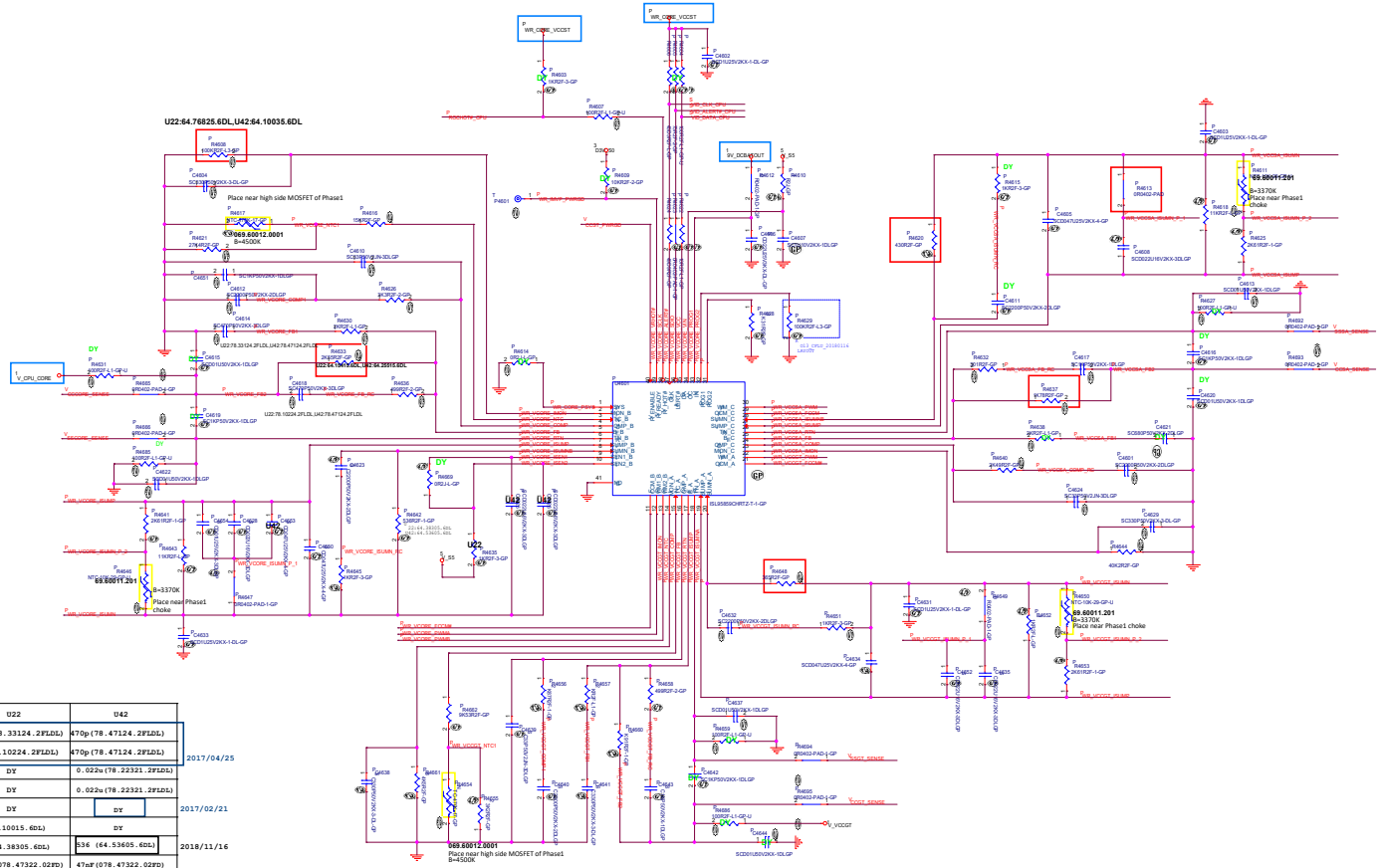
PH on CPU side

For VCCGT Sense

For Vcore Sense

EE side Link
SVID Pull High V

ISL95859C For CPUCORE



	U22	U42	
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)	
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)	2017/04/25
PC4625	DY	0.022u(78.22321.2FLDL)	
PC4626	DY	0.022u(78.22321.2FLDL)	
PR4669	DY	DY	2017/02/21
PR4635	1K(64.10015.6DL)	DY	
PR4642	383(64.38305.6DL)	536 (64.53605.6DL)	2018/11/16
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)	
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	
PC4654	10nF(78.10322.2FLDL)	10nF(78.10322.2FLDL)	
PC4653	DY	47nF(078.47322.02FD)	
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)	
PR4608	76.8K(64.76825.6DL)	100K (64.10035.6DL)	

Wistron Corporation
2F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95859_CPUCORE(1/3))

Size: A | Document Number: W ASP 13" WHL-U | Rev: A0

Date: Thursday, March 01, 2018 | Sheet 45 of 106

Main Func = CPU_CORE

AOZ5038Q For VCORE

OFFPAGE

9V_DCBATOUT

WR_DCBATOUT_VCOREA

L4703 HCB2012KF-600T50-GP-U

L4704 HCB2012KF-600T50-GP-U

46 WR_VCORE_PWMA
46 WR_VCORE_PWMB
46 WR_VCORE_FCCM#
46 WR_VCORE_ISEN1
46 WR_VCORE_ISEN2
46 WR_VCORE_ISUMP
46 WR_VCORE_ISUMN

For acoustic noise

WR_DCBATOUT_VCOREA

C4702 SE33U25VM-11-GP 79.33612.20L

5V_S5

C4777 SC2D2U6D3V2MX-DL-GP

R4703 2D2R2F-GP

WR_VCORE_VCCDA

C4709 SC2D2U6D3V2MX-DL-GP

U4701

C4702 C4703 C4704 C4705 DY

WR_VCORE_BOOTA_RC

SC10U25V3MX-5-GP x4

R4704 2D2R3F-L-GP

C4708 SCD22U25V3KX-DL-GP

WR_VCORE_BOOTA

WR_VCORE_BOOTRA

WR_VCORE_SWA

WHL_U42_15W
Icc(max)=70A
TDC=48A

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

L4701 IND-D15UH-33-GP 068.R1510.1171

V_CPU_CORE

WR_VCORE_PWMA
WR_VCORE_FCCM#

R4702 0R0402-PAD-1-GP
R4706 0R0402-PAD-1-GP

WR_VCORE_PWMA_RA
WR_VCORE_FCCM#_RA

R4717 5K11R2F-L1-GP DY

AOZ5038QI-05-GP
074.05038.0A73

R4705 2D2R6J-3-GP DY

WR_VCORE_SNB1

C4710 SC1KP50V2KX-1DLGP DY

C4708 GAP-CLOSE-PWR-3-GP

C4709 GAP-CLOSE-PWR-3-GP

L4703 SE330U2VDM-4-GP 79.33719.20C

WR_VCORE_ISUMP_GA

WR_VCORE_ISUMN_GA

WR_VCORE_ISEN1 R4721 100KR2F-L3-GP

WR_VCORE_ISUMP R4708 3K65R2F-1-GP

WR_VCORE_ISUMN R4709 10R2F-L1-GP

WR_VCORE_ISEN2 R4722 100KR2F-L3-GP DY

5V_S5

U42 C4766 SC2D2U6D3V2MX-DL-GP

R4713 2D2R2F-GP

WR_VCORE_VCCDB

C4712 SC2D2U6D3V2MX-DL-GP

U4702

C4716 C4717 C4714 C4715 DY

WR_VCORE_BOOTB_RC

SC10U25V3MX-5-GP x4

R4710 2D2R3F-L-GP

C4711 SCD22U25V3KX-DL-GP

WR_VCORE_BOOTB

WR_VCORE_BOOTRB

WR_VCORE_SWB

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

L4702 IND-D15UH-33-GP 068.R1510.1171

V_CPU_CORE

WR_VCORE_PWMB
WR_VCORE_FCCM#

R4711 0R0402-PAD-1-GP
R4712 0R0402-PAD-1-GP

WR_VCORE_PWMB_RA
WR_VCORE_FCCM#_RB

R4718 5K11R2F-L1-GP DY

U42
AOZ5038QI-05-GP
074.05038.0A73

R4714 2D2R6J-3-GP DY

WR_VCORE_SNB2

C4713 SC1KP50V2KX-1DLGP DY

C4713 GAP-CLOSE-PWR-3-GP

C4715 GAP-CLOSE-PWR-3-GP

L4701 SE330U2VDM-4-GP 79.33719.20C

WR_VCORE_ISUMP_GB

WR_VCORE_ISUMN_GB

WR_VCORE_ISEN2 R4723 100KR2F-L3-GP

WR_VCORE_ISUMP R4716 3K65R2F-1-GP

WR_VCORE_ISUMN R4715 10R2F-L1-GP

WR_VCORE_ISEN1 R4724 100KR2F-L3-GP DY

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (5038_CPU_VCORE(2/3))

Size: Custom | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 47 of 106

Main Func = CPU_CORE

AOZ5038Q For VCCGT

Offpage-Signal

19V_DCBATOUT

PWR_DCBATOUT_VCCGT

PL4802 HCB2012KF-800T50-GP-U

PL4803 HCB2012KF-800T50-GP-U

46 PWR_VCCGT_PWM
46 PWR_VCCGT_FCCM#
46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN

PWR_DCBATOUT_VCCGT

PC4801 C10U25V3MX-5-GP DY
PC4802 C10U25V3MX-5-GP
PC4803 C10U25V3MX-5-GP
PC4804 C10U25V3MX-5-GP

For acoustic noise

PWR_DCBATOUT_VCCGT

PC4805 SE33U25VM-11-GP
79.33612.20L

5V_S5

PC4866 SC2D2U6D3V2MX-DL-GP

PR4804 2D2R2F-GP

PWR_VCCGT_VCC_R

PC4808 SC2D2U6D3V2MX-DL-GP

PR4802 0R0402-PAD-1-GP

PWR_VCCGT_PWM

PR4812 5K11R2F-L1-GP DY

PR4806 0R0402-PAD-1-GP

PWR_VCCGT_FCCM#

PWR_VCCGT_PWM_R

PWR_VCCGT_FCCM#_R

PU4801

AOZ5038QI-05-GP
074.05038.0A73

VCC PVCC VIN VIN VIN VIN VIN

NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35

BOOT VSWH#7 VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26

NC#4 AGND PGND PGND PGND PGND PGND PGND

PWR_VCCGT_BOOT_RC

PR4805 2D2R3F-L-GP

PC4807 SCD22U25V3KX-DL-GP

PWR_VCCGT_BOOT

PWR_VCCGT_BOOTR

PWR_VCCGT_SW

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

WHL_U42_15W
Icc(max)=31A
TDC=18A

PL4801 IND-D15UH-33-GP

068.R1510.1171

V_VCCGT

PR4803 2D2R6J-3-GP DY

PWR_VCCGT_SNB

PC4806 SC1KP50V2KX-1DLGP DY

PR4808 3K65R2F-1-GP

PC4807 GAP-CLOSE-PWR-3-GP

PWR_VCCGT_ISUMP_G

PWR_VCCGT_ISUMP

PC4808 GAP-CLOSE-PWR-3-GP

PWR_VCCGT_ISUMN_G

PR4801 0R0402-PAD-1-GP

PWR_VCCGT_ISUMN

PC4801 SE330U2VDM-4-GP PANASONIC
ESR: 9 mohm

Wistron Corporation
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Title: POWER (5038_CPU_VCORE(3/3))

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

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RSVD

<Core Design>

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Title: POWER (CPU_VCCGTS_RSVD)

Size	Document Number	Rev
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Main Func = CPU_CORE

ISL95808 For VCCSA

OFFPAGE

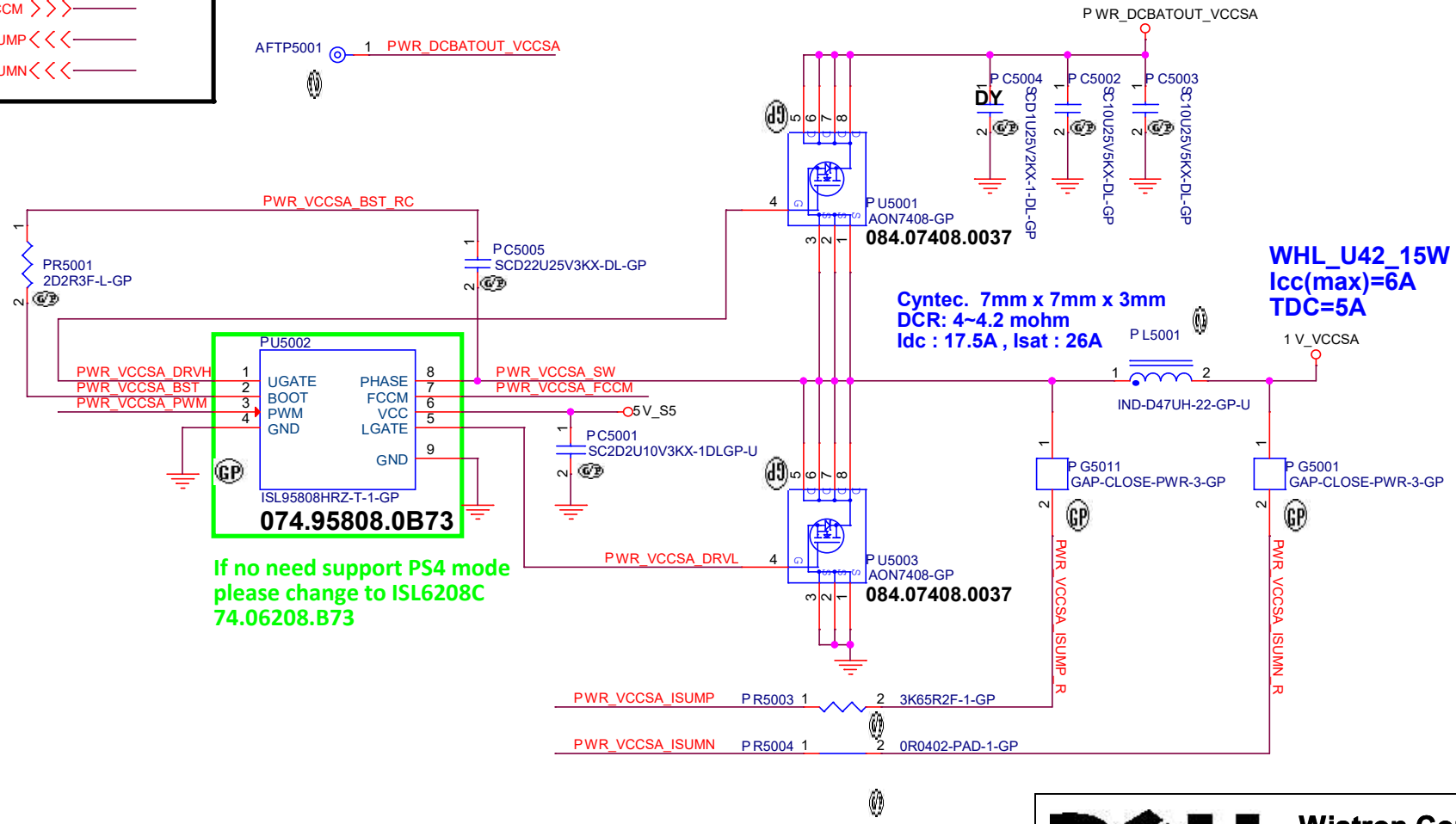
19V_DCBATOUT — R5001 (0R6J-L-GP) — PWR_DCBATOUT_VCCSA

46 PWR_VCCSA_PWM >>>

46 PWR_VCCSA_FCCM >>>

46 PWR_VCCSA_ISUMP <<<

46 PWR_VCCSA_ISUMN <<<



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Title: POWER (ISL95808_VCCSA)

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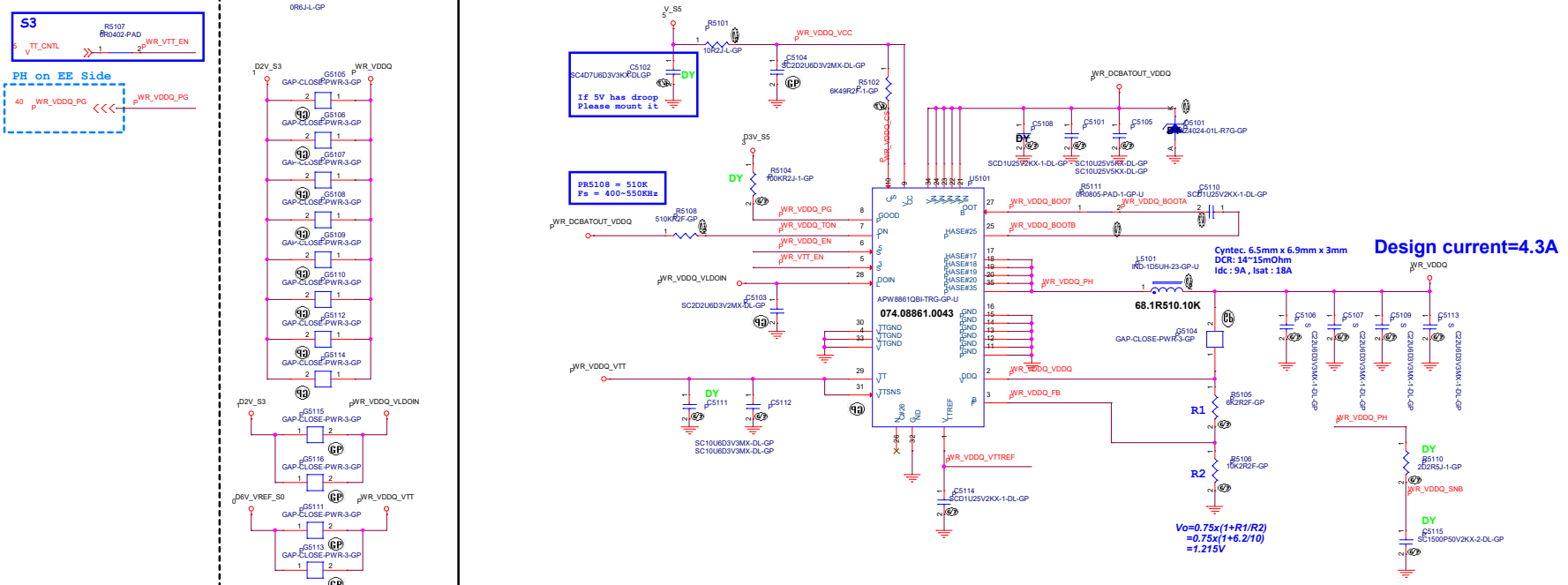
SSID = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

OFFPAGE-GAP

G5388 For VDDQ/VTT



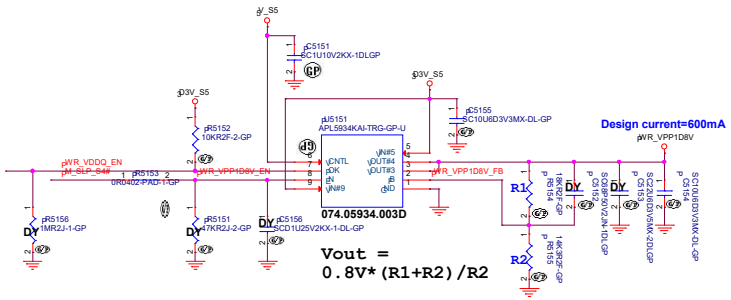
SSID = PWR.Plane.Regulator_1D8V

OFFPAGE-Signal

OFFPAGE-GAP

PH on EE Side

APL5934 For 1D8V



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (G5388_VDDQ_VTT_VPP)

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

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SSID = PWR.Plane.Regulator_1D0V

OFFPAGE-Signal

25,53 3V_5V_DSW_OK

AOZ2262 For 1D0V

OFFPAGE-GAP

19V_DCBATOUT

PWR_DCBATOUT_1D05V

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PG5203 GAP-CLOSE-PWR-3-GP

3D3V_S5

PR5208 100KR2J-1-GP

PWR_1D0V_PG

5V_S5

PC5202 SC4D7U25V5KX-DL-GP

PU5201

VCC

IN#7

IN#8

IN#9

TON

PGOOD

EN

PFM#

SS

LX#18

LX#17

LX#16

LX#11

LX#10

BST

FB

AGND

PGND

AOZ2262QI-10-2-GP

074.02262.M002

PWR_1D05V_PH

PWR_1D05V_BT

PWR_1D05V_VFB

PWR_1D05V_TON

PWR_1D0V_PG

PWR_1D05V_EN

PWR_1D05V_PFM

PWR_1D05V_SS

PR5201 95K3R2F-GP

PC5209

PC5210

SC10U25V5KX-DL-GP

SC10U25V5KX-DL-GP

SCD1U25V2KX-1-DL-GP

3V_5V_DSW_OK PR5210 47KR2F-GP

SCD1U16V2KX-3DLGP

PR5203 100KR2F-L-GP

SCD01U25V2KX-3DLGP

Cyntec. 6.5mm x 6.9mm x 3mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A

PL5201 COIL-1UH-34-GP-U1

68.1R01A.20B

PC5204 SCD1U25V2KX-1-DL-GP

PC5210 GAP-CLOSE-PWR-3-GP

Design current =9.3A

D0V_S5

PC5201 PC5203 PC5205 PC5207 PC5206

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

PWR_1D05V_VFB_A

PR5202 8K16R2F-GP

PC5212 SC220P50V2KX-3DLGP

PR5204 10KR2F-2-GP

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

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Title: POWER (AOZ2261Q_1D0V)

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

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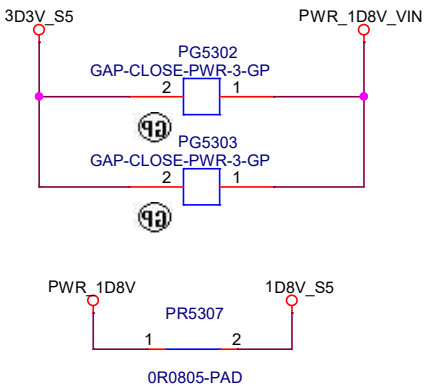
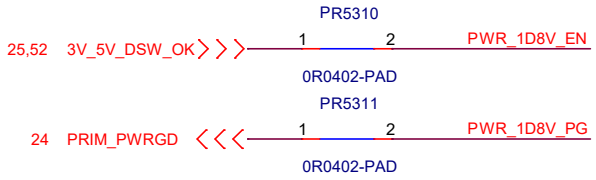
Main Func = 1D8V

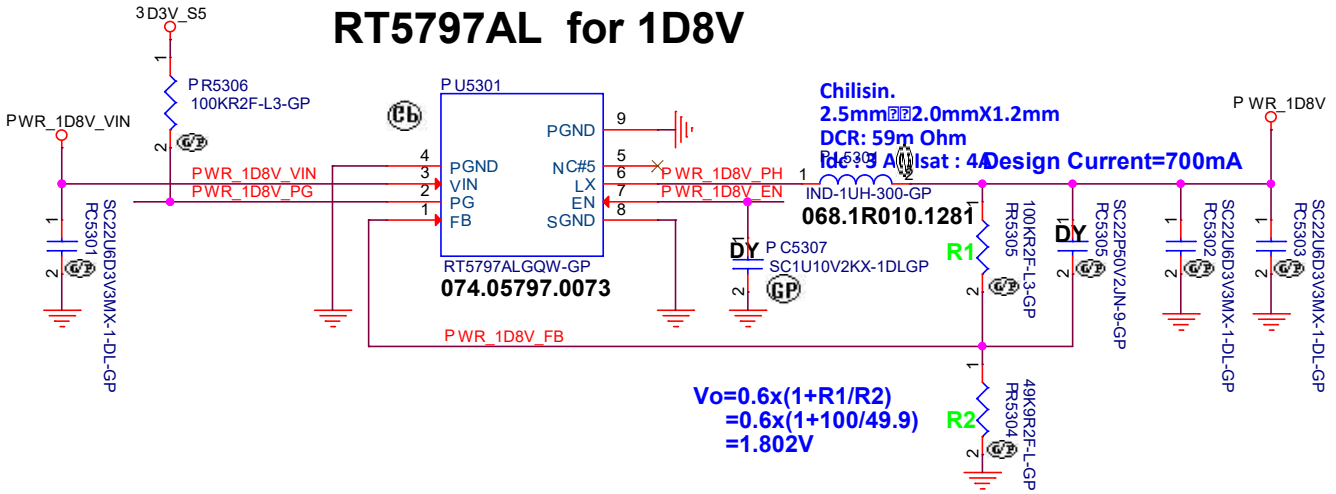
OFFPAGE_GAP



OFFPAGE



RT5797AL for 1D8V



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Title	POWER (APL5934_1D8V)	
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Title

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Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

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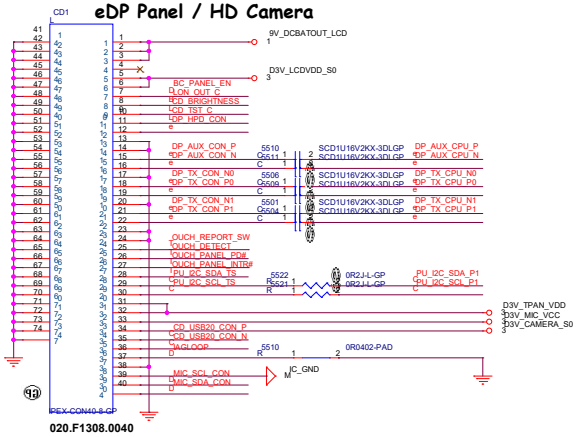
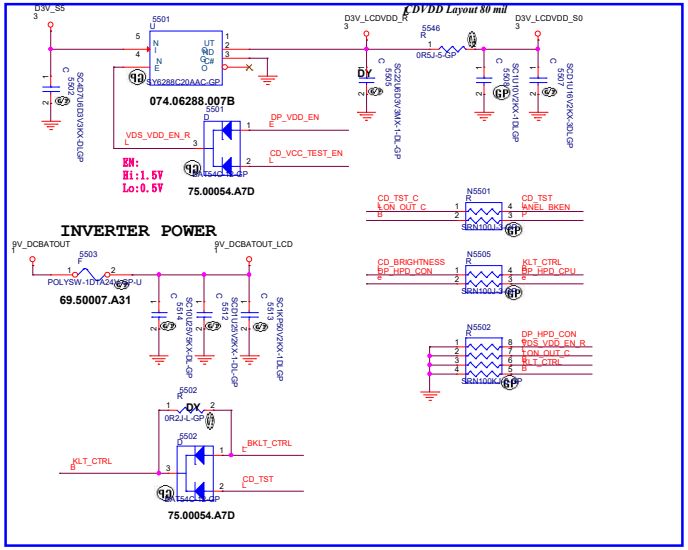
Main Func = LCD

eDP Panel / HD Camera



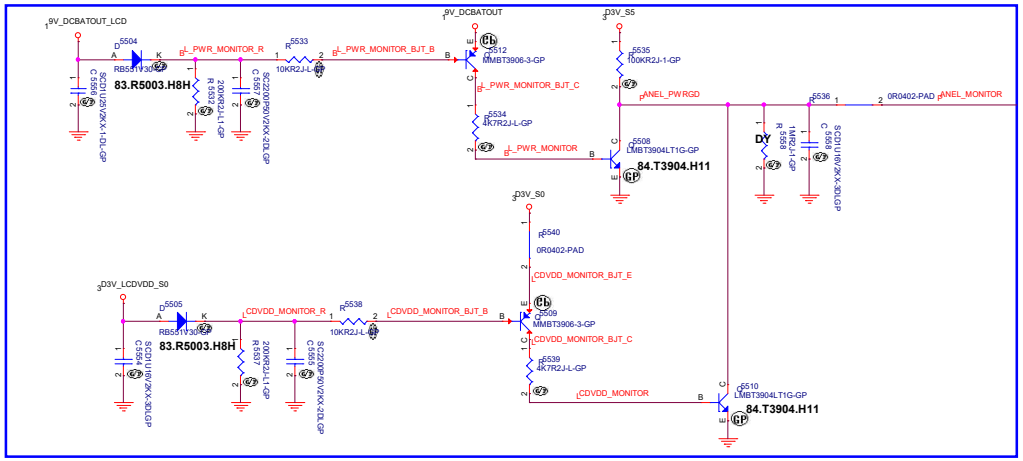
020.F1308.0040

CPU DD Layout 80 mil

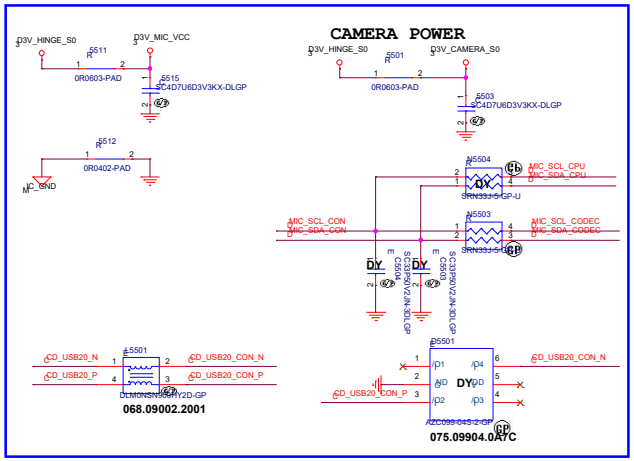


M-BIST/ LCD BIST -20180425

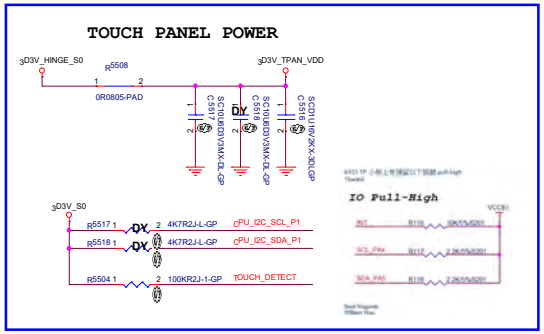
LCD BIST for G10 (Was test only for G9)

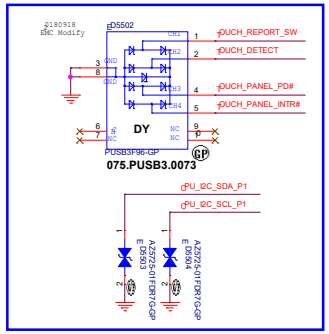


CAMERA POWER



TOUCH PANEL POWER





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Title: LCD&CAM&DMC&Touch

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

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A 4	WASP 13" WHL-U	A 00

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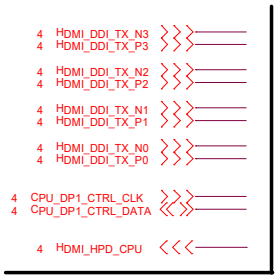
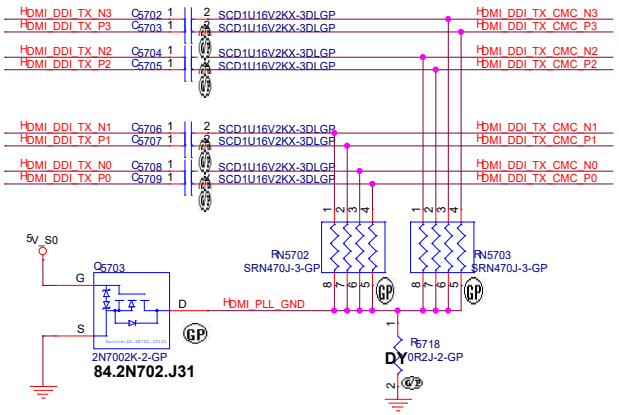
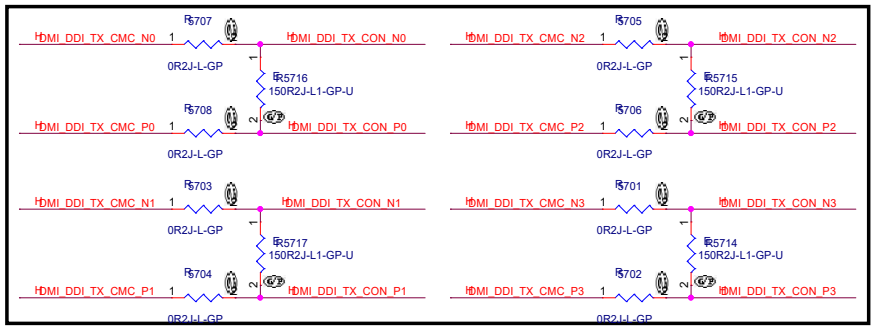
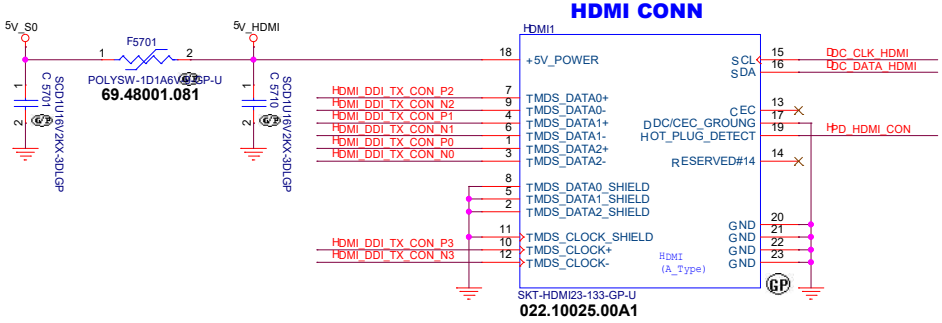
Main Func = HDMI

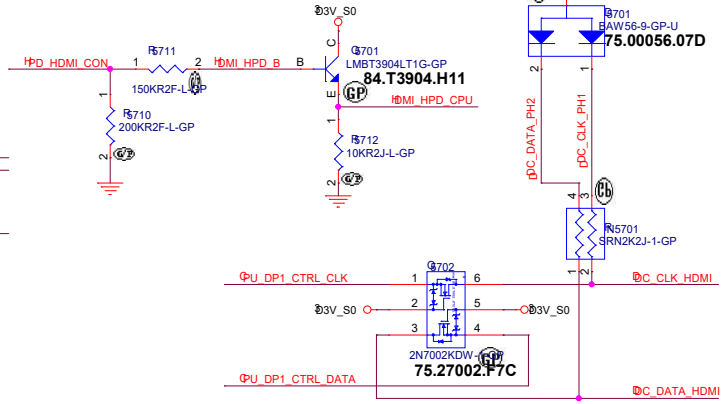




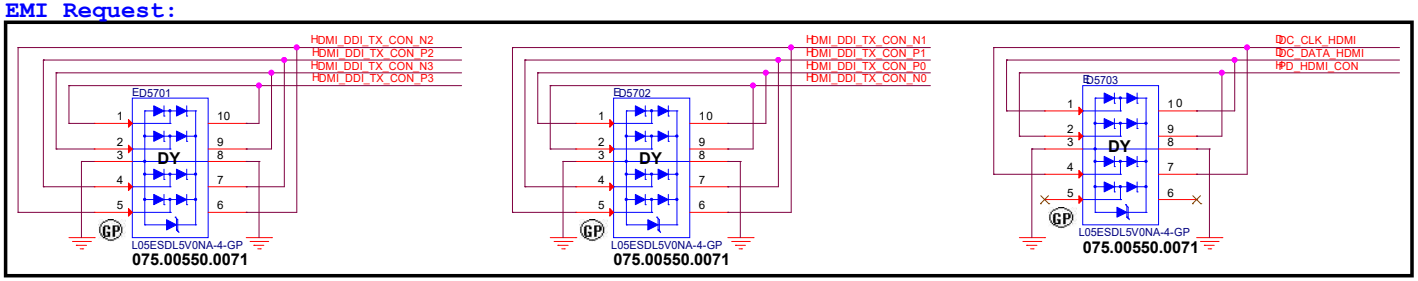


HDMI CONN





EMI Request:



<Core Design>

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Title: HDMI

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 57 of 106

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

Date: Thursday, March 07, 2019 Sheet 58 o f 106

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<Core Design>

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Title
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A4	*WASP 13" WHL-U*	

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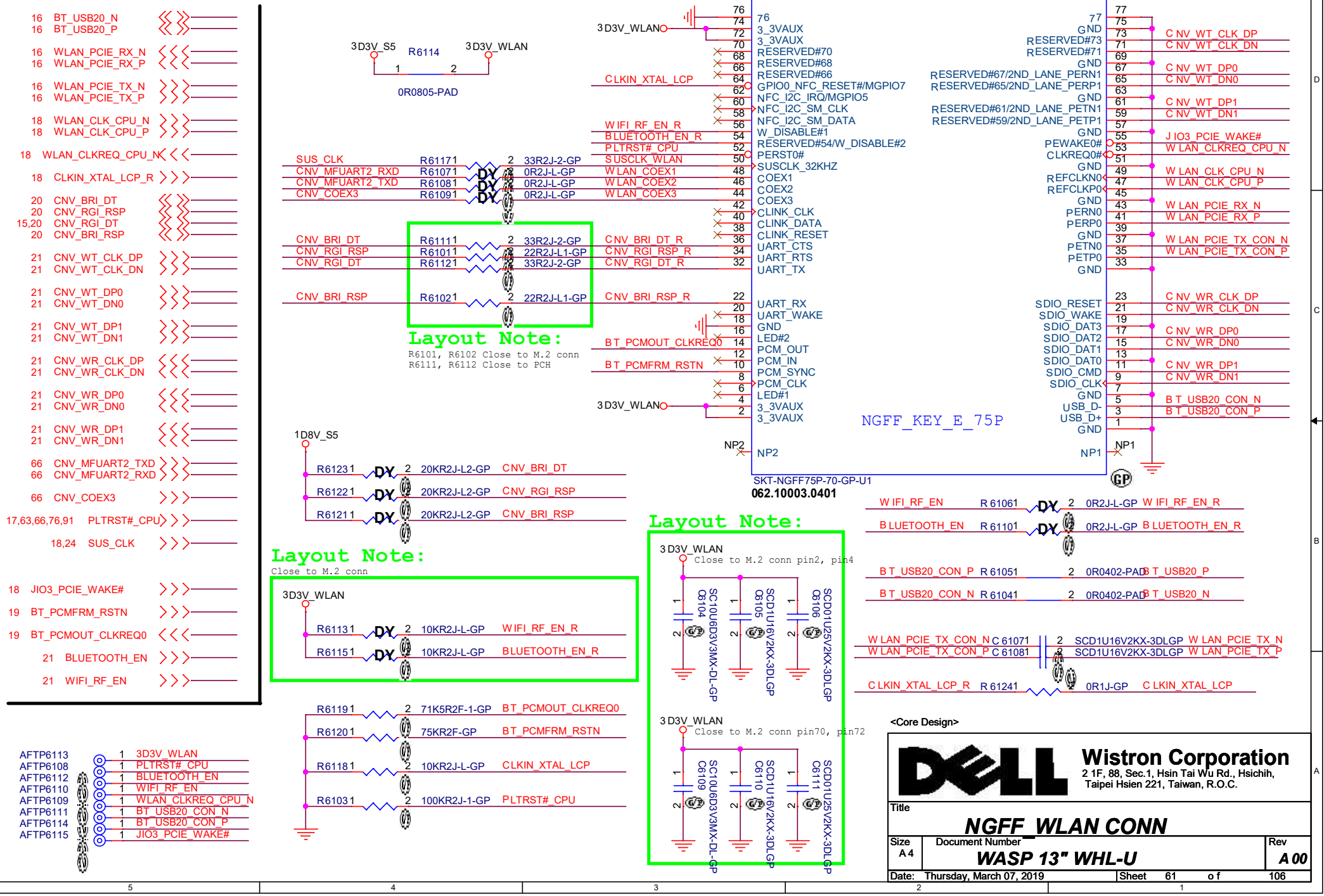
Title

SATA IF_HDD/ODD

Size	Document Number	Rev
A 4	**WASP 13" WHL-U**	**A00**

Date: Thursday, March 07, 2019 Sheet 60 o f 106

Main Func = WLAN



<Core Design>

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Title: NGFF_WLAN CONN

Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00

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<Core Design>

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Title: INT IO WWAN		
Size: A4	Document Number: WASP 13" WHL-U	Rev: A00
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Main Func = SSD M.2

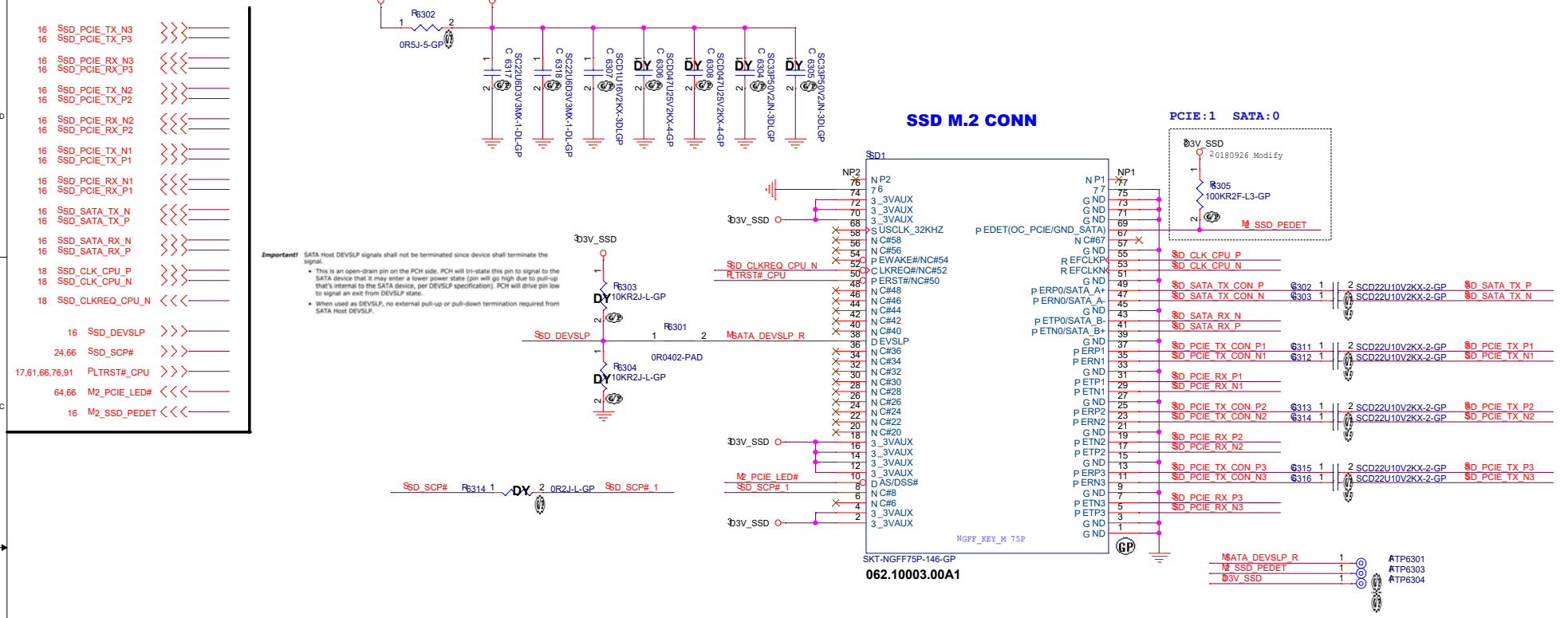

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title: SSD M.2/eMMC

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

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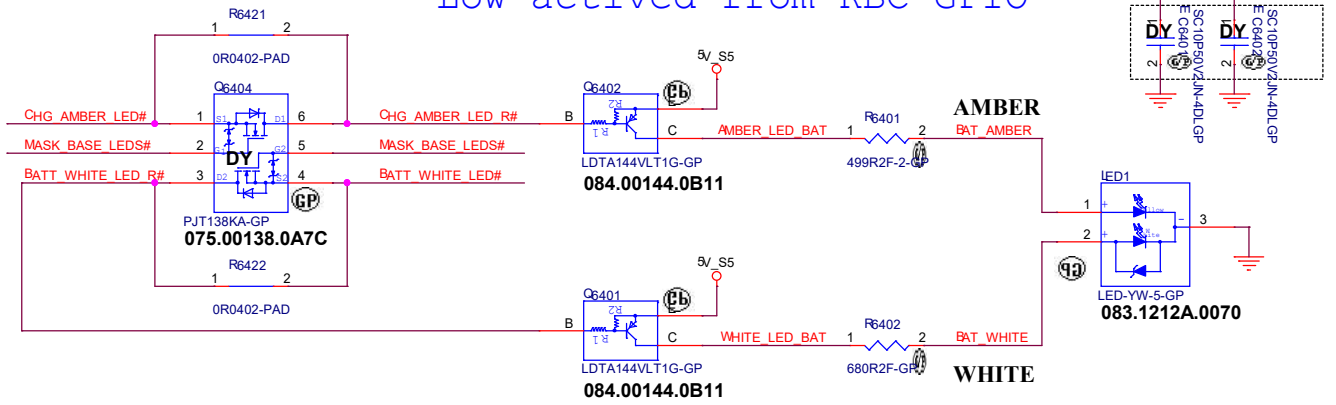
Main Func = Power BTN

24 CHG_AMBER_LED#
24 BATT_WHITE_LED#
24 SYS_LED_MASK#_R
16 PCH_SATA_LED#
63,66 M2_PCIE_LED#
20,24,67,92 LID_CL_SIO#
24 MASK_SATA_LED#
24,92 KBC_PWRBTN#
24,44 HW_ACAV_IN
17,24 PCH_RSMRST#
24 EC_D_INHIB

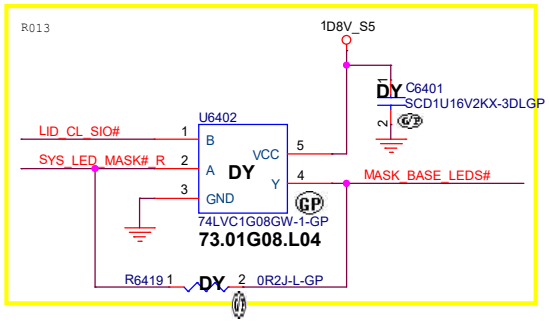
Battery LED1 (AMBER_LED)

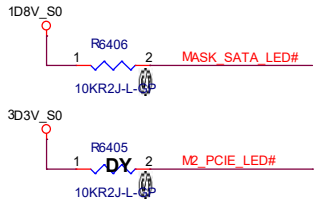
Low actived from KBC GPIO



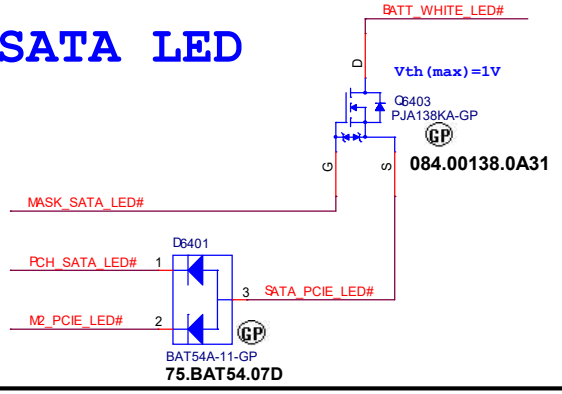
Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

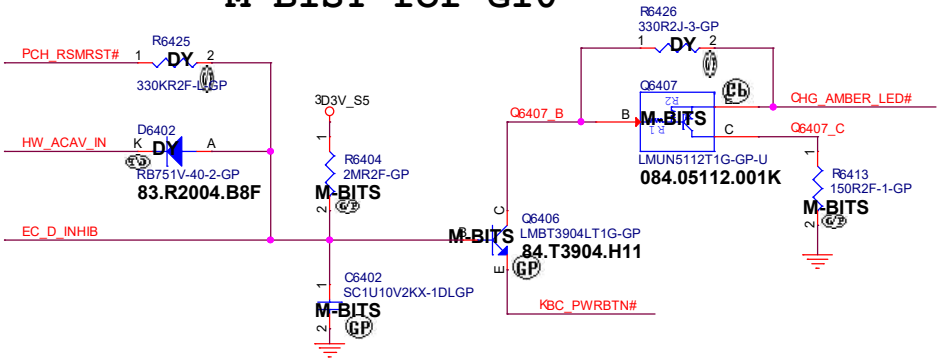




SATA LED



M-BIST for G10



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

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Title: LED Board&Power Button

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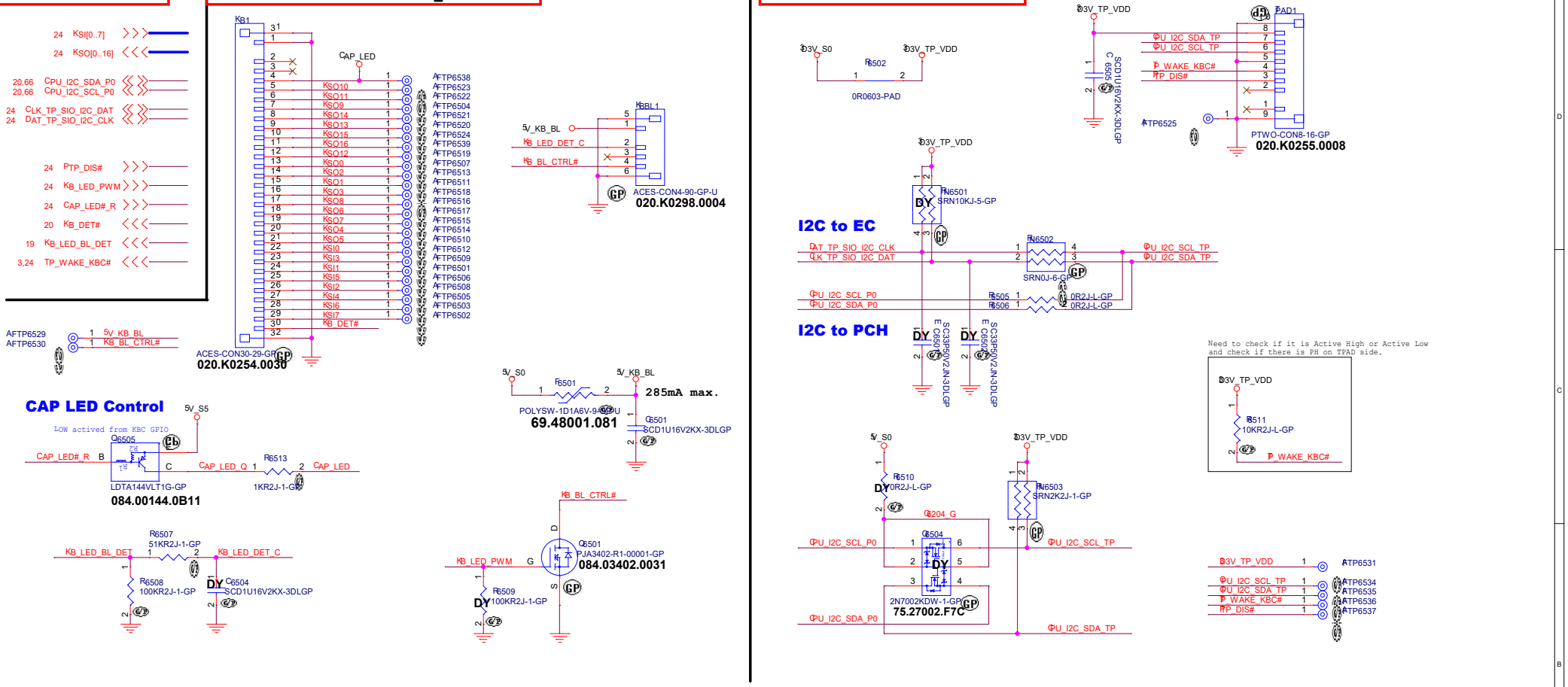
SSID = KB

Main Func = Keyboard

Main Func = TPAD



<Core Design>

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Title: Key Board&Touch Pad

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

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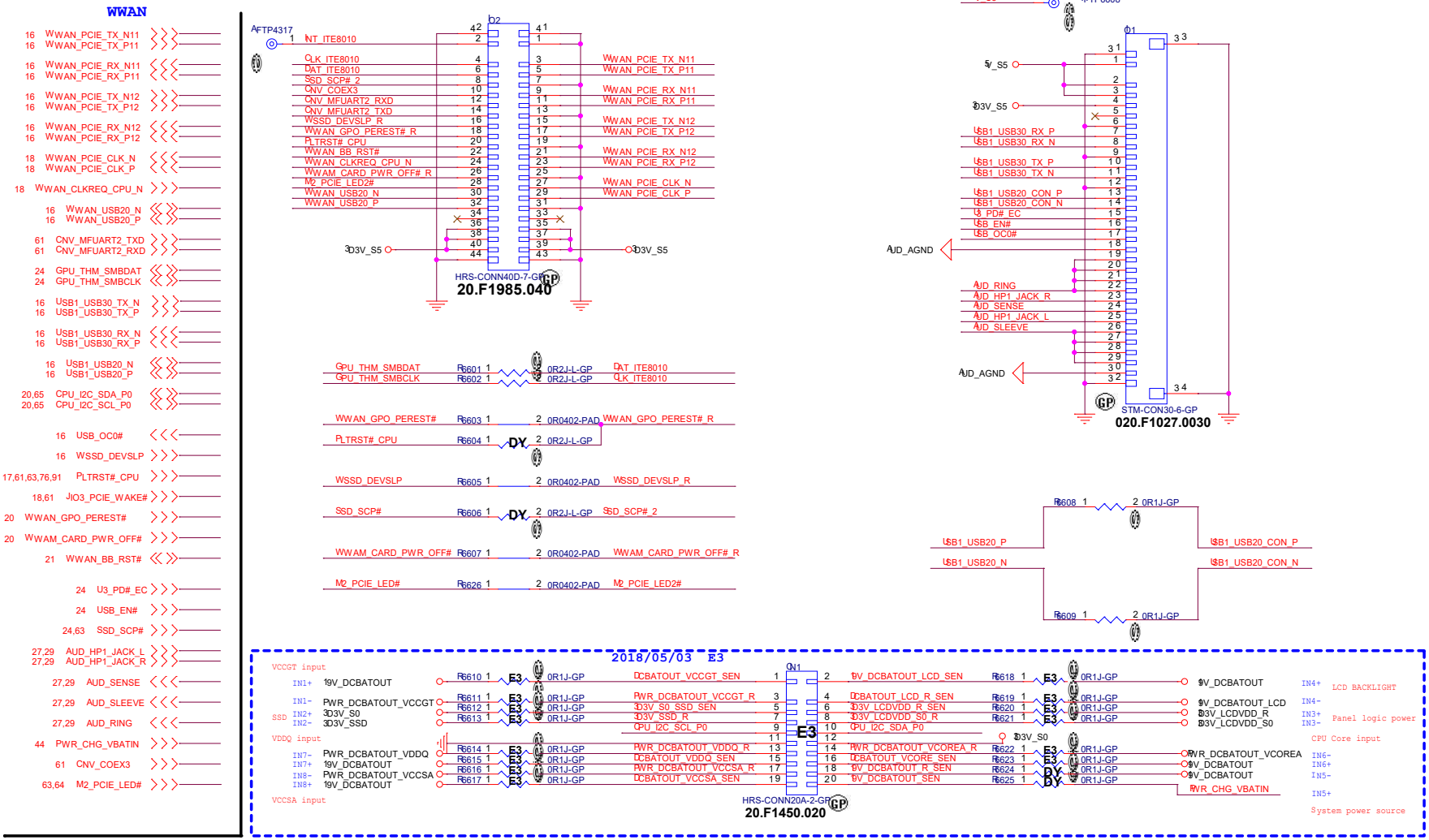
Main Func = IO Connector



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Title: IO Board Connector

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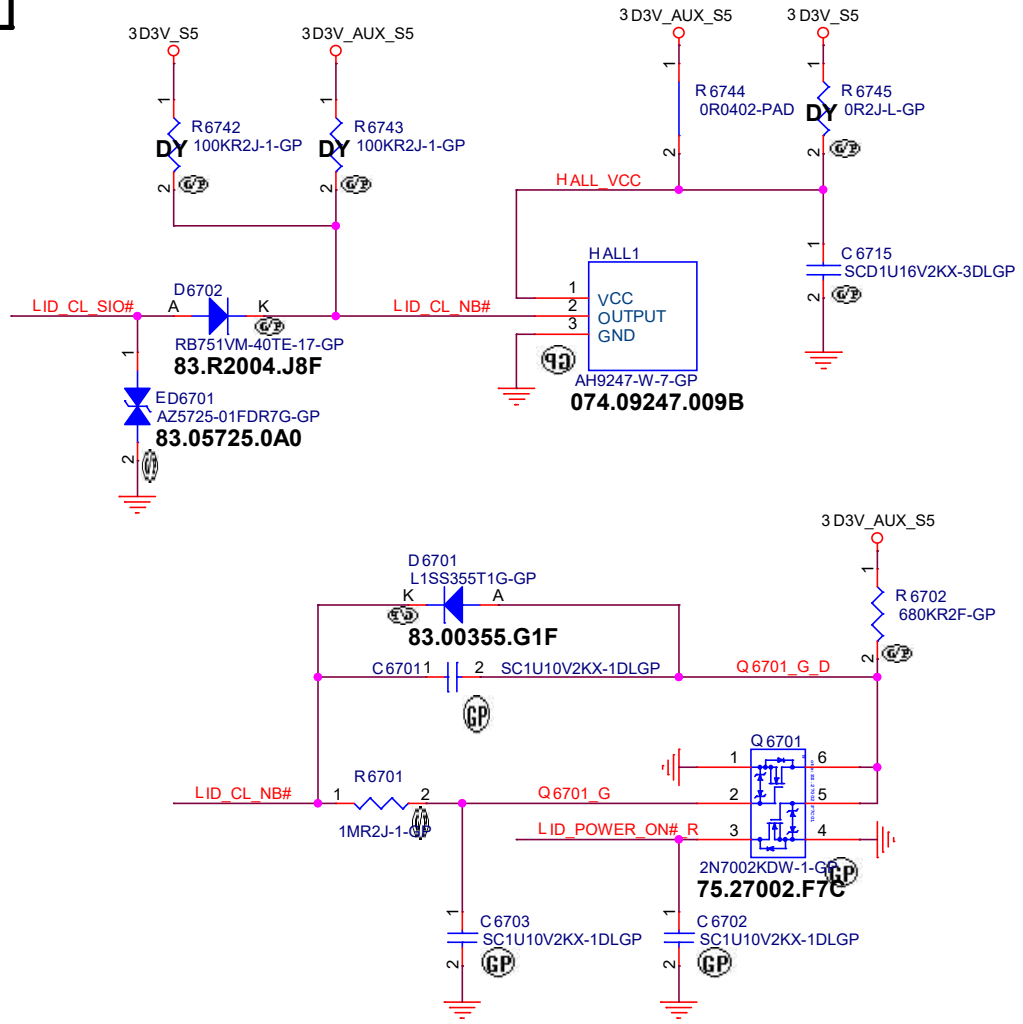
Main Func = HALL SENSOR

24 LID_POWER_ON#_R >>>
20,24,64,92 LID_CL_SIO# <<<

LID sensor



<Core Design>

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Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
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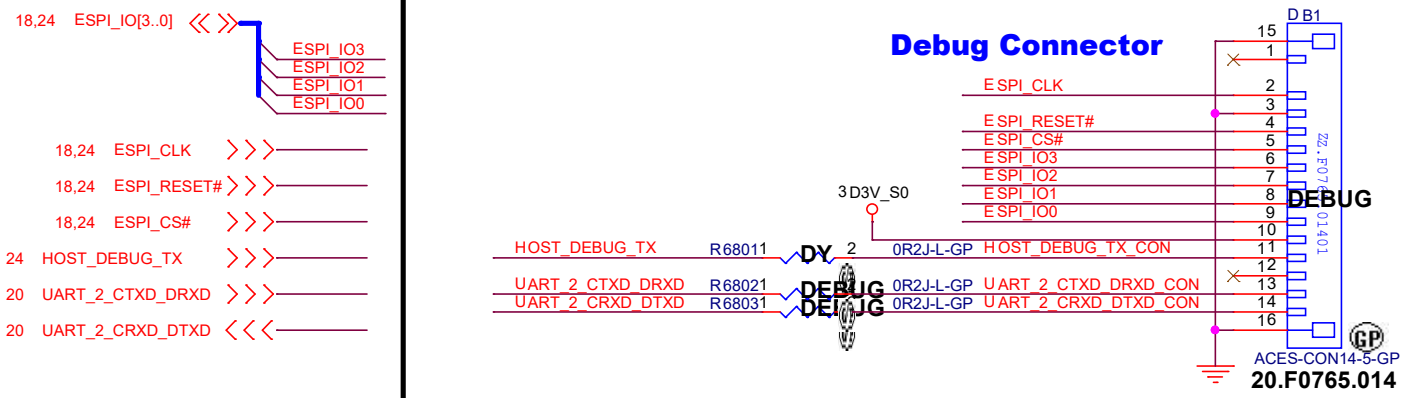
Main Func = Debug



<Core Design>

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Title: ***Dubug connector***

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A 4	***WASP 13" WHL-U***	***A 00***

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A 4	***WASP 13" WHL-U***	***A 00***

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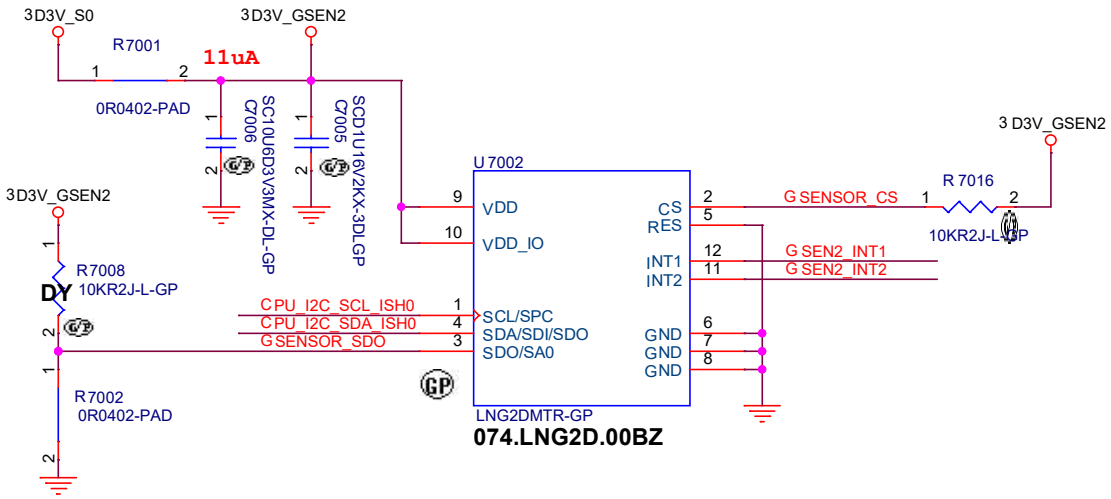
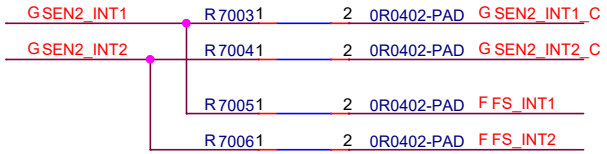
Main Func = G-sensor

20 GSEN2_INT1_C
20 GSEN2_INT2_C

18 FFS_INT1
20 FFS_INT2

20 CPU_I2C_SCL_ISH0
20 CPU_I2C_SDA_ISH0





<Core Design>

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Title: Sensor

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A 00

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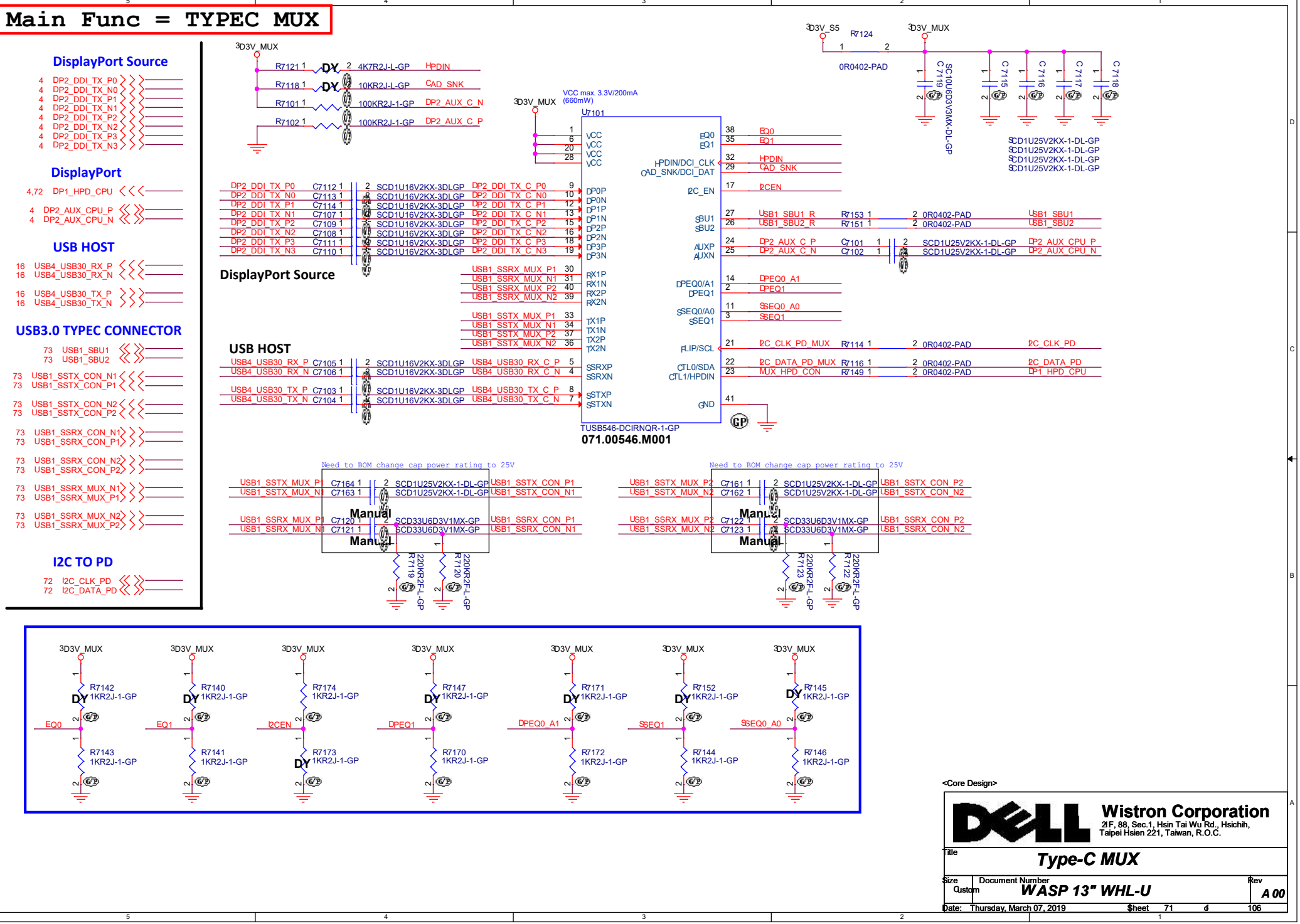
Main Func = TYPEC MUX



<Core Design>

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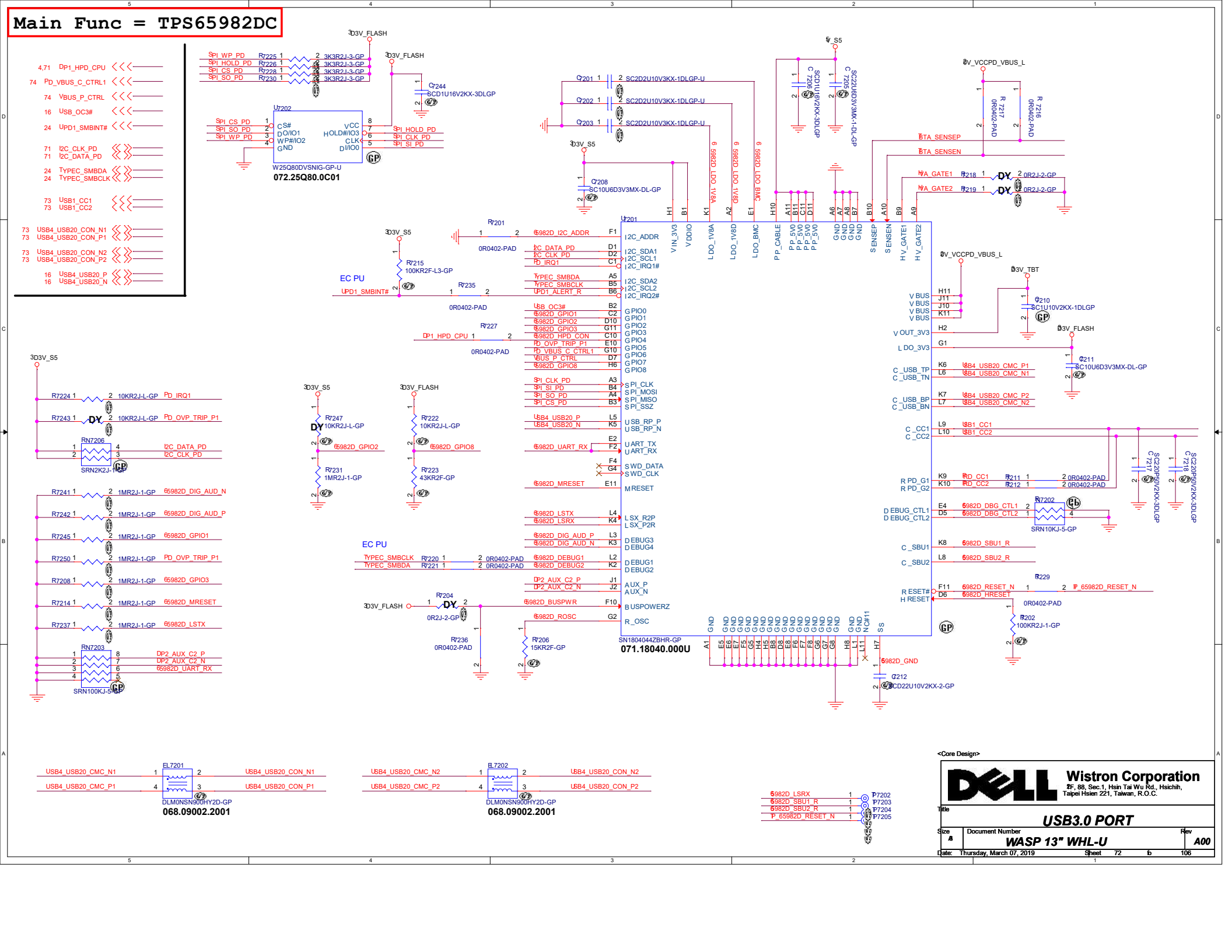
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Type-C MUX	
Size: Custom	Document Number: WASP 13" WHL-U	Rev: A 00
Date: Thursday, March 07, 2019	Sheet 71 of 106	

Main Func = TPS65982DC



Main Func = TYPEC CONNECTOR

71 USB1_SSRX_MUX_N1
71 USB1_SSRX_MUX_P1
71 USB1_SSRX_MUX_N2
71 USB1_SSRX_MUX_P2
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2
72 USB4_USB20_CON_N1
72 USB4_USB20_CON_P1
72 USB4_USB20_CON_N2
72 USB4_USB20_CON_P2
71 USB1_SBU1
71 USB1_SBU2
72 USB1_CC1
72 USB1_CC2

USB1_SBU1
USB1_SBU2
R7330 2MR2F-GP
R7331 2MR2F-GP

20V_VCCPD_VBUS_L
20V_VCCPD_VBUS
ER7301 0R5J-5-GP
ER7302 0R5J-5-GP
C7301 SC1U25V3KX-1-DLGP
D7301 BX310F-R1-00000-GP
83.3R010.C8M
DY
C7305 SC10U25V5KX-DL-GP
C7306 SC1U25V3KX-1-DLGP
C7302 SCD1U25V2KX-1-DL-GP
C7303 SCD1U25V2KX-1-DL-GP
C7304 SCD1U25V2KX-1-DL-GP
C7307 SCD1U25V2KX-1-DL-GP

ED7301
USB1_SSTX_CON_N1
USB1_SSTX_CON_P1
USB1_SSRX_MUX_N1
USB1_SSRX_MUX_P1
L05ESDL5V0NA-4-GP
075.00550.0071

ED7302
USB1_SSRX_MUX_P2
USB1_SSRX_MUX_N2
USB1_SSTX_CON_P2
USB1_SSTX_CON_N2
L05ESDL5V0NA-4-GP
075.00550.0071

ED7303
USB4_USB20_CON_N1
USB4_USB20_CON_P1
USB4_USB20_CON_N2
USB4_USB20_CON_P2
L05ESDL5V0NA-4-GP
075.00550.0071

ED7304
USB1_CC1
USB1_CC2
USB1_SBU1
USB1_SBU2
L05ESDL5V0NA-4-GP
075.00550.0071

20V_VCCPD_VBUS
USB1
GND SSTXP1 SSTXN1 VBUS#A4 CC1 DP1 DN1 RFU1 VBUS#A9 SSRXN2 SSRXP2 GND
GND SSTXP2 SSTXN2 VBUS#B4 CC2 DP2 DN2 RFU2 VBUS#B9 SSRXN1 SSRXP1 GND
NP1 NP2
GROUND CHASSIS#13 CHASSIS#14 CHASSIS#15 CHASSIS#20 CHASSIS#21 CHASSIS#22
USB1_SSTX_CON_P1
USB1_SSTX_CON_N1
USB1_CC1
USB4_USB20_CON_P1
USB4_USB20_CON_N1
USB1_SBU1
USB1_SSRX_CON_N2
USB1_SSRX_CON_P2
USB1_SSTX_CON_P2
USB1_SSTX_CON_N2
USB1_CC2
USB4_USB20_CON_P2
USB4_USB20_CON_N2
USB1_SBU2
USB1_SSRX_CON_N1
USB1_SSRX_CON_P1
SKT-USB34-21-GP-U1
022.10005.M021

<Core Design>

Wistron Corporation
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Title: GPU(1/5)PEG
Size: A 4
Document Number: WASP 13" WHL-U
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Date: Thursday, March 07, 2019
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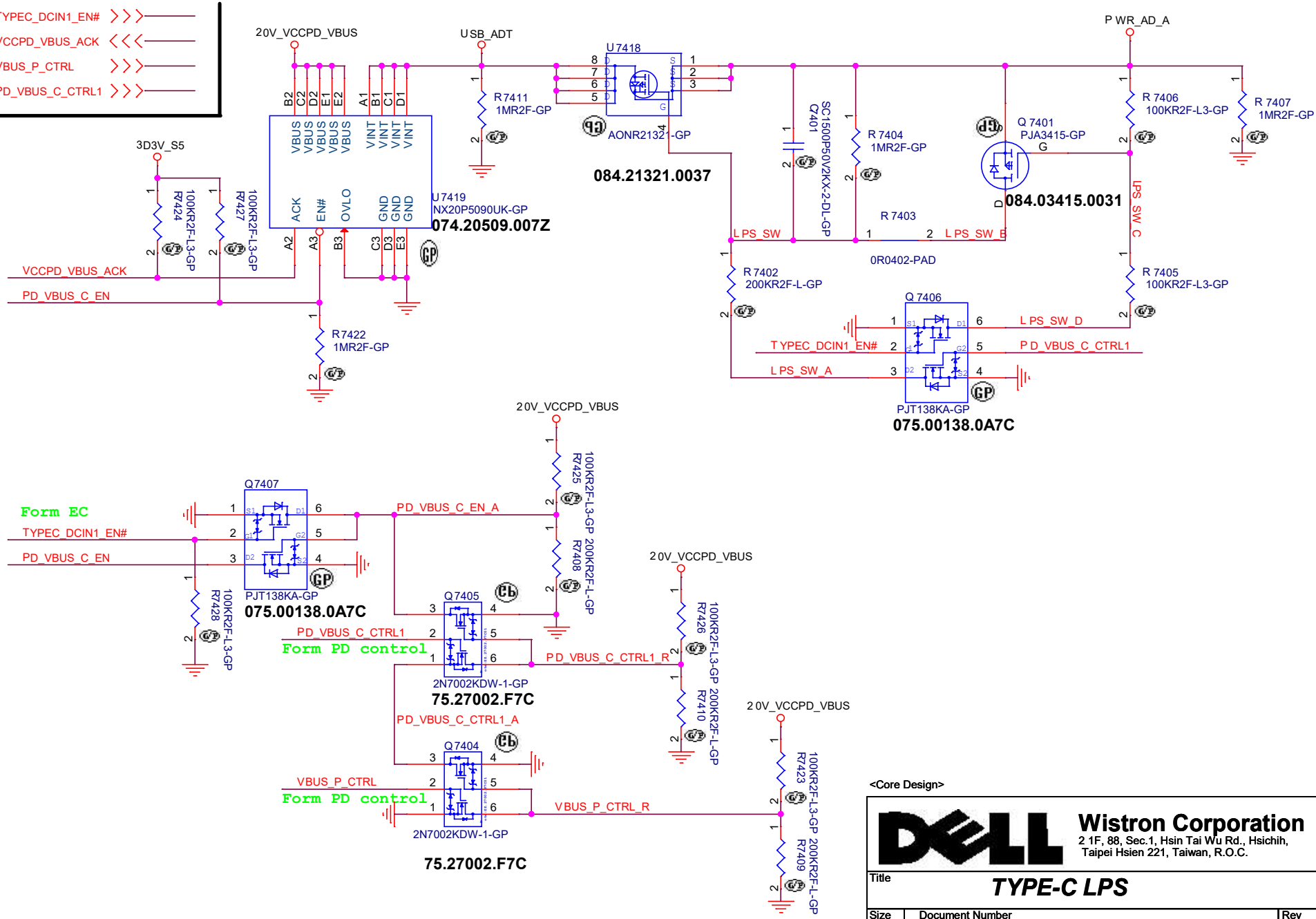
Main Func = TYPEC protect

24 TYPEC_DCIN1_EN#
44 VCCPD_VBUS_ACK
72 VBUS_P_CTRL
72 PD_VBUS_C_CTRL1



<Core Design>

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Title: **TYPE-C LPS**

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

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(Blanking)

<Core Design>

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Title
GPU(3/5)VRAMI/F

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 75 o f 106

Main Func = dGPU

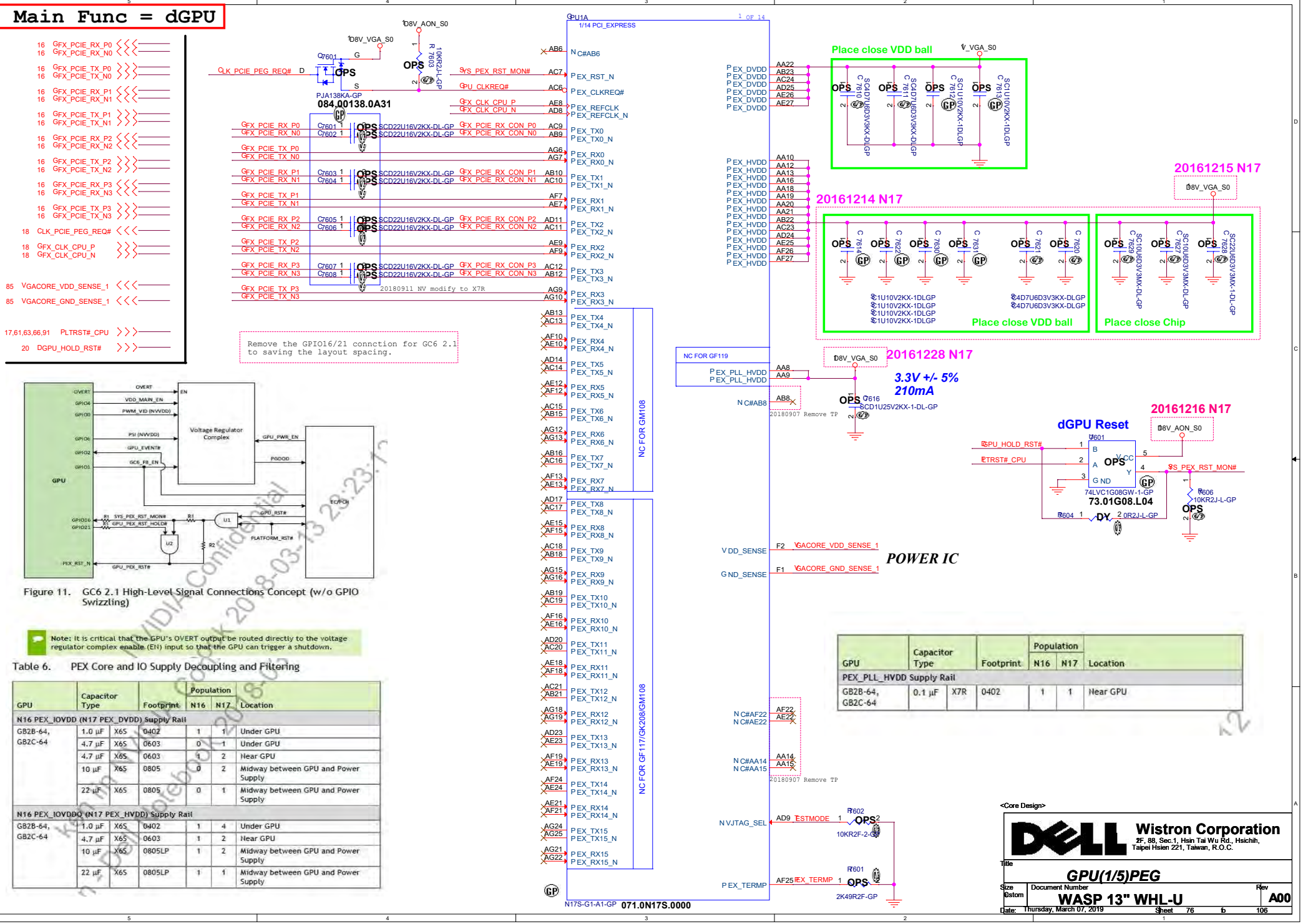

Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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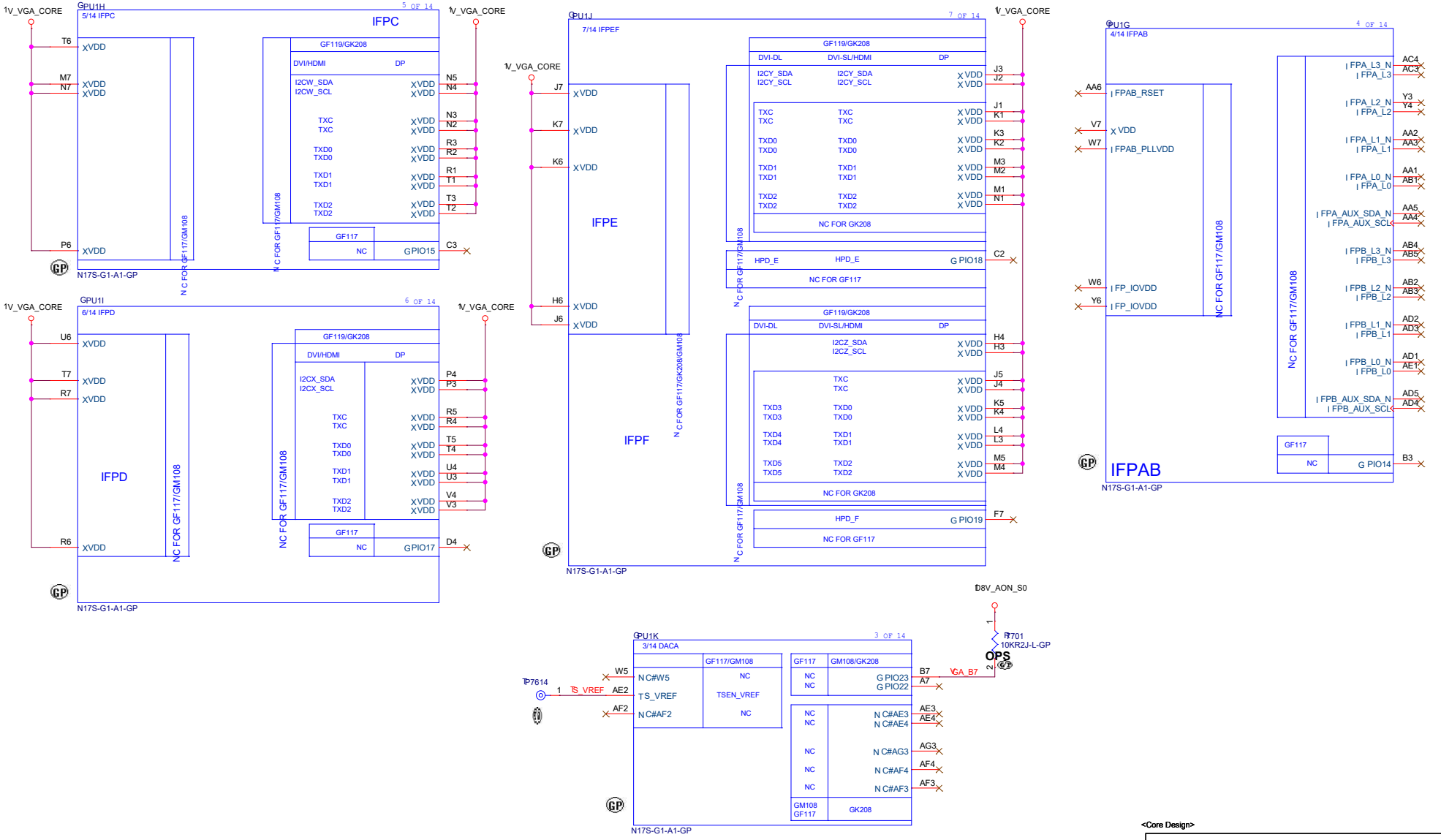
Title: GPU(1/5)PEG
Size: Custom
Document Number: WASP 13" WHL-U
Rev: A00
Date: Thursday, March 07, 2019
Sheet 76 of 106

Main Func = dGPU



<Core Design>

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Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A4	WASP 13" WHL-U	A00

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Main Func = dGPU

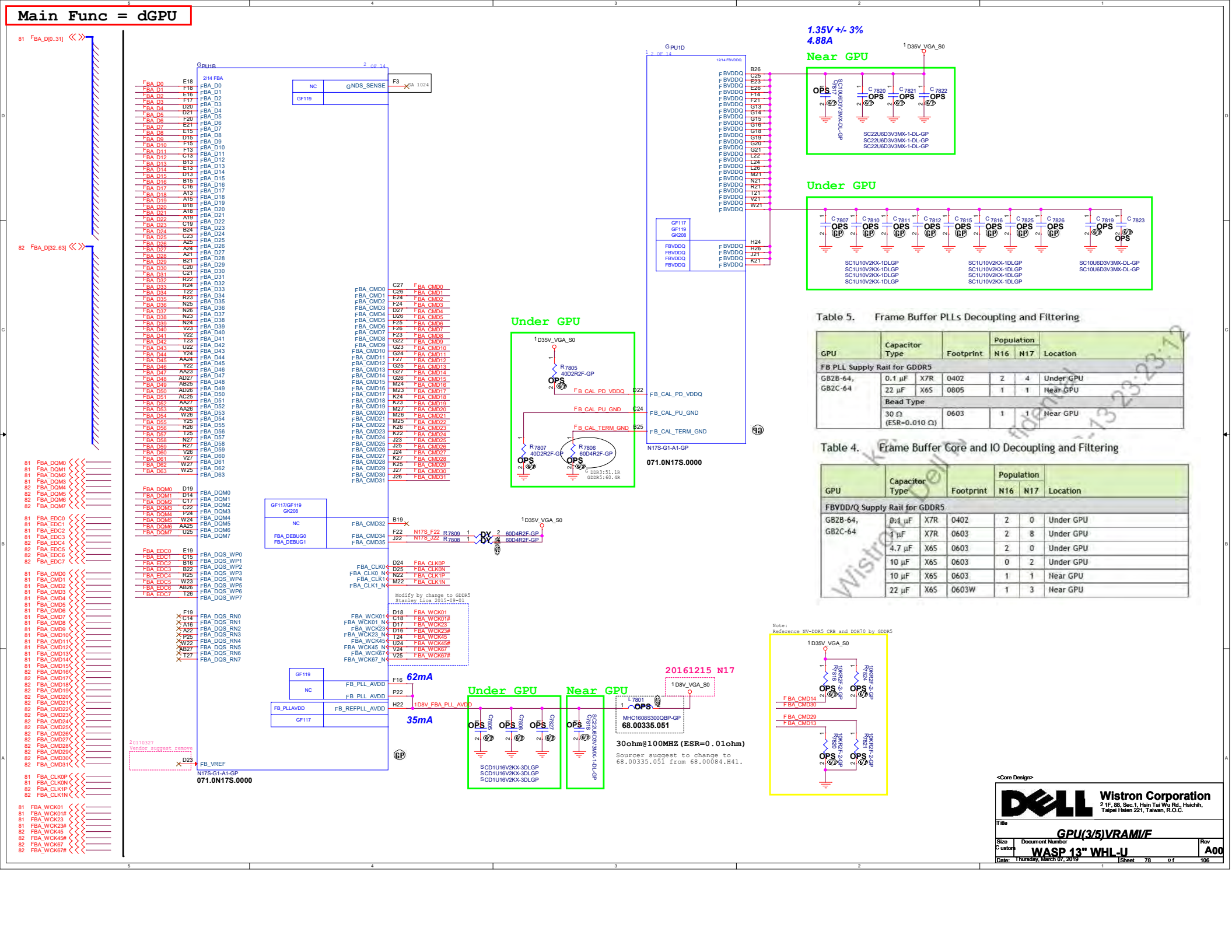

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

<Core Design>

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Title: GPU(3/5)VRAMI/F

Size: C | Document Number: WASP 13" WHL-U | Rev: A00

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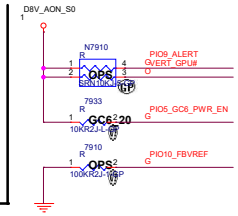
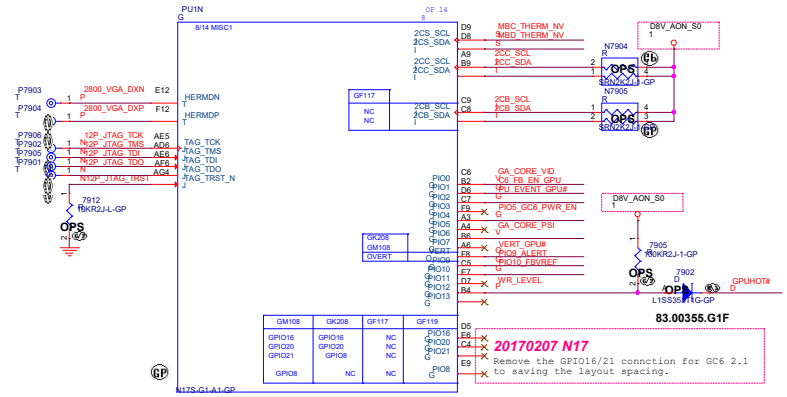
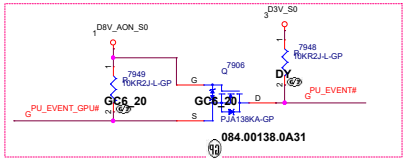
Main Func = dGPU

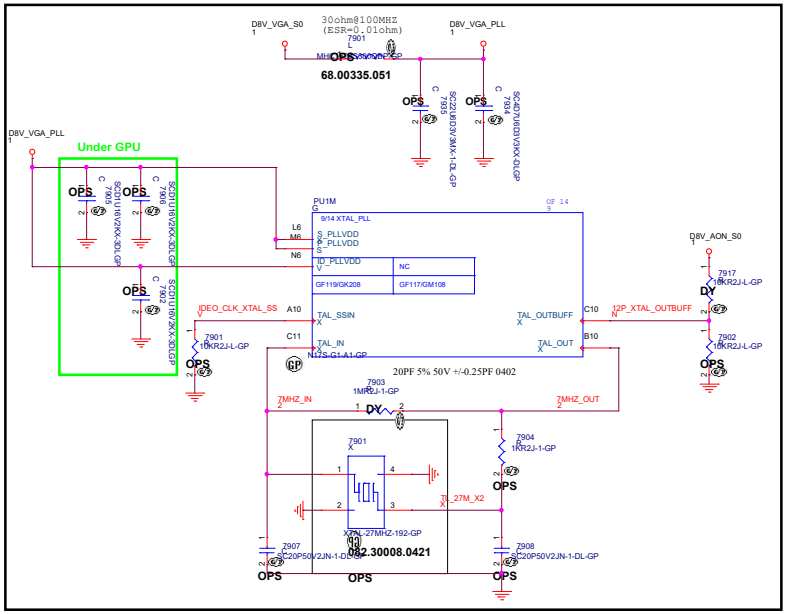




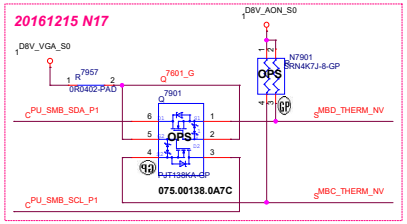


20170207 N17

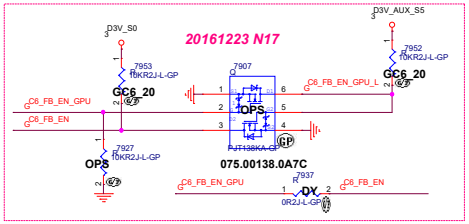
Remove the GPIO16/21 connction for GC6 2.1 to saving the layout spacing.



20161215 N17



20161223 N17



15V-GS supports Binary Mode.
15V-GM supports Multi-Level Strap.

Strap Pin [5:3]

Strap Pin [2:0]

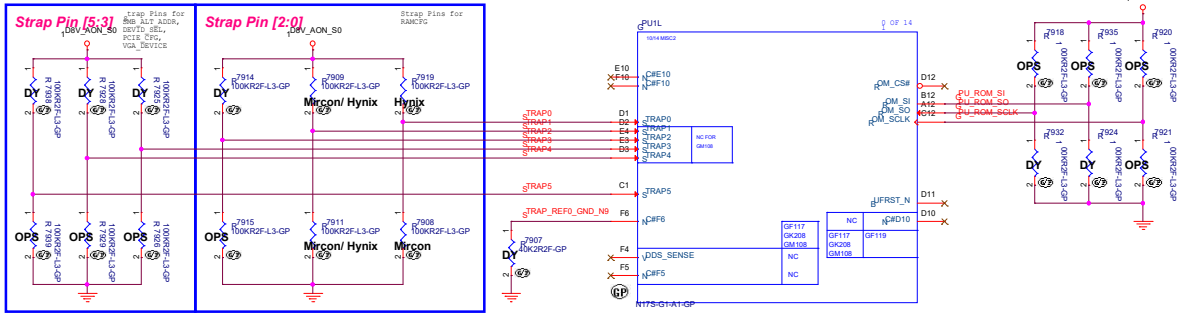


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins (see Note)			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
3	H	H	L	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVTD_SEL, PCIE_CFG, VGA_DEVICE

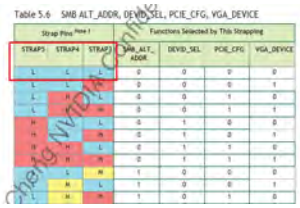


Table 5.3 RAMCFG

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:
1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

<Core Design>

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Title: GPU(4/5)GPIO/STRAP

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

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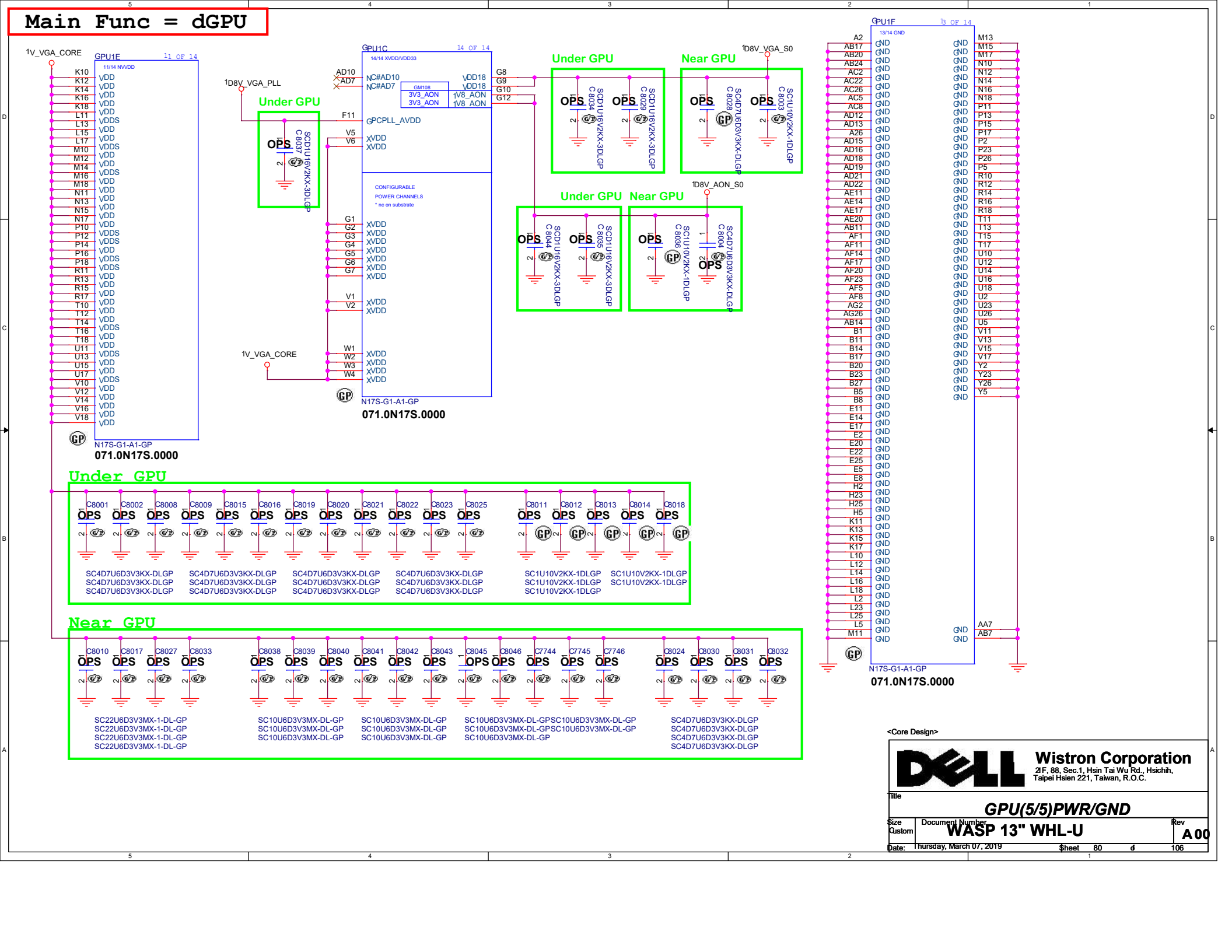
Main Func = dGPU



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU(5/5)PWR/GND**

Size	Document Number	Rev
Custom	WASP 13" WHL-U	A00

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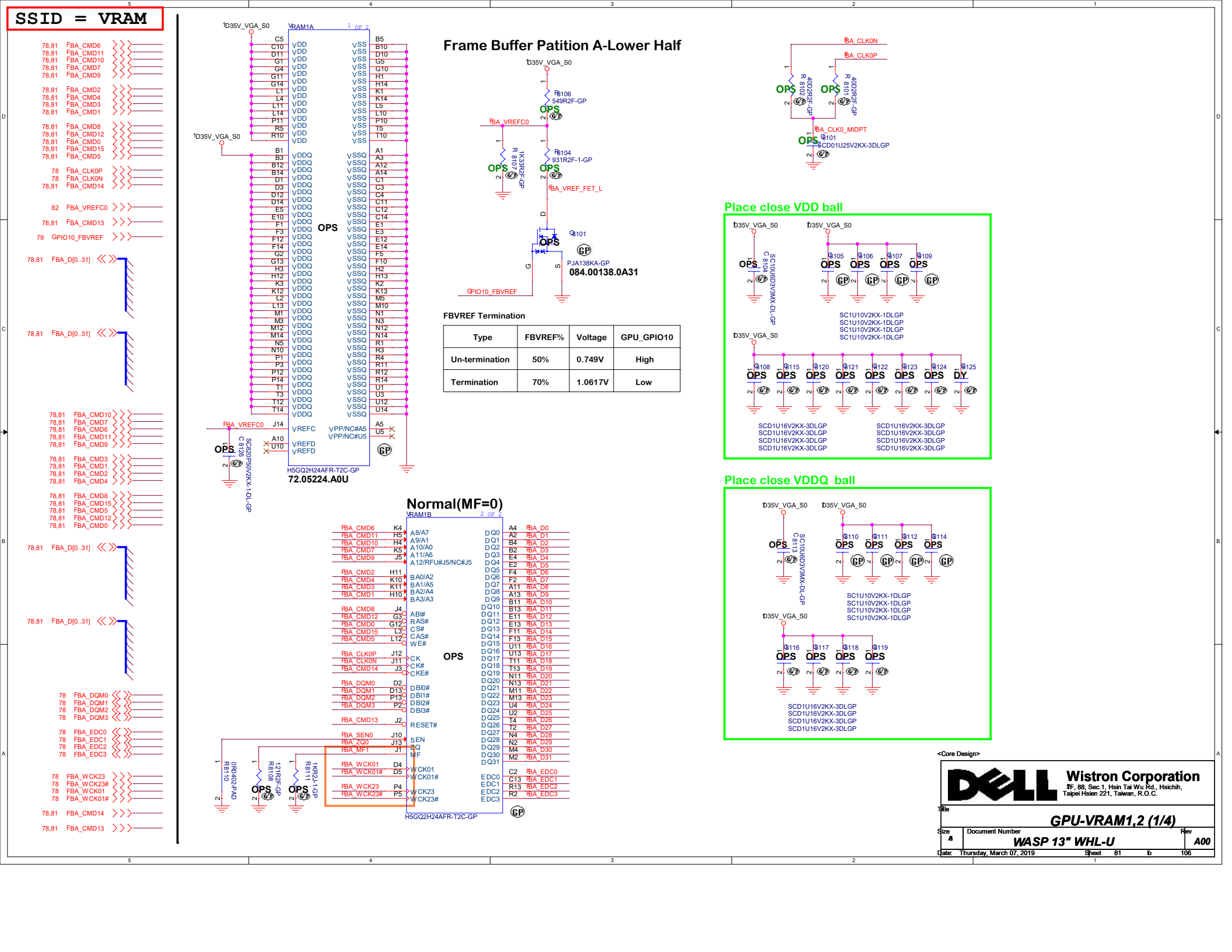
SSID = VRAM



Frame Buffer Patition A-Lower Half

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Place close VDD ball

Place close VDDQ ball

Normal(MF=0)

<Core Design>

Wistron Corporation
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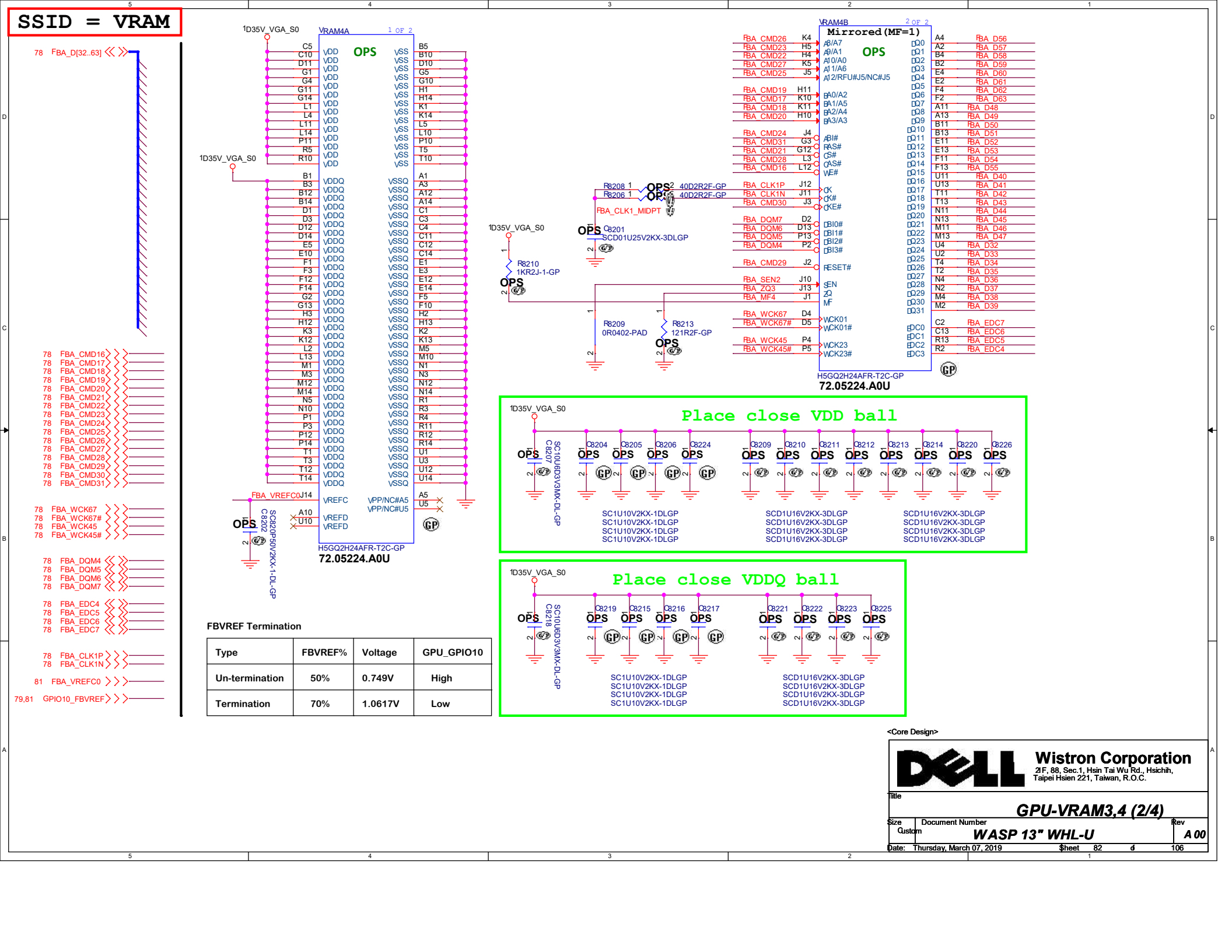
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 81 of 106

SSID = VRAM



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 82 of 106

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<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

Date: Thursday, March 07, 2019 Sheet 83 o f 106

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<Core Design>

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Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A 4	WASP 13" WHL-U	A00

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OFFPAGE-Signal

OFFPAGE-GAP

RT8816A For NVVDDS

VGA : N17S-G2 / NVVDD
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

need 1.8V

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

For VGA_CORE sequence
EE need check

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.84V
2Phase with DEM	1.08V to 1.32V
2phase with CCM	1.6V to 5.5V

ID:31/54A ,
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)

Cyntec 6.8mmx7.3mmx3mm
DCR: 1.9~2.3 mohm
Idc : 27A , Isat : 61A

VGA : N17S-G2 / NVVDD
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

OCP setting

SS setting

Place Near GPU (NVVDDS)
1X330uF (Poscap) - PTB511 (Page85)

Wistron Corporation

GPU (RT8816A_VGA)

W ASP 13" WHL-U

Main Func = dGPU

RT5797 for 1.8V_AON_S0

1D8V_AON_S0 to 1D8V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

1D35V_VGA_S0

VGA_CORE

1D8V_VGA_S0

1D8V_AON_S0

For tuning VGA_CORE sequence.

RT5797 for 1V_VGA_S0

1D35V_VGA_S0

SY8288RAC for 1D35V

OCP setting	
High	16A
Float	12A
Low	8A

[DG-07158-001 Rev03]

<Core Design>

緯創資通 Wistron Corporation

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Title: DISCRETE VGA POWER

Size: C | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 86 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*WASP 13" WHL-U*	

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(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A 4	*WASP 13" WHL-U*	*A 00*

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Main Func = UnusedParts

H51 STFT237B158R128H48-GP	H52 STFT237B158R128H48-GP	H5 HOLE233R142-GP-U1	H20 HOLE233R142-GP-U1
434.0FD01.0001	434.0FD01.0001	ZZ.00PAD.5S1	ZZ.00PAD.5S1
H9 HOLE233R142-GP-U1	H10 HOLE233R142-GP-U1	H11 HOLE233R142-GP-U1	H12 HOLE233R142-GP-U1
ZZ.00PAD.5S1	ZZ.00PAD.5S1	ZZ.00PAD.5S1	ZZ.00PAD.5S1
H13 HOLE276R150-GP	H14 HOLE276R150-GP	H15 HOLE276R150-GP	H22 HOLET237B213R142-GP
ZZ.00PAD.H91	ZZ.00PAD.H91	ZZ.00PAD.H91	ZZ.SCREW.0A1

1V_VCCGT

1V_CPU_CORE

1V_VCCSA

5V_S0

20180918 EMC Modify

19V_DCBATOUT

5V_S5

1D2V_S3

1D3V_S0

1V_VGA_CORE

19V_DCBATOUT

1D0V_S5

1D3V_S5

1V_VGA_CORE

19V_DCBATOUT

PWR_DCBATOUT_VCCSA

PWR_AD_B

1D35V_VGA_S0

1V_CPU_CORE

1V_VCCGT

3D3V_S5

5V_S5

1D2V_S3

PWR_AD_B

C8901 C8902 C8903

SC10U25V3MX-5-GP
SC10U25V3MX-5-GP
SC10U25V3MX-5-GP

1D35V_VGA_S0

1V_CPU_CORE

1V_VCCGT

3D3V_S5

3D3V_S0

1D2V_S3

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Title: UNUSED PARTS/EMI Capacitors

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Title

Reserved

Size	Document Number	Rev
A 4	***WASP 13" WHL-U***	***A 00***

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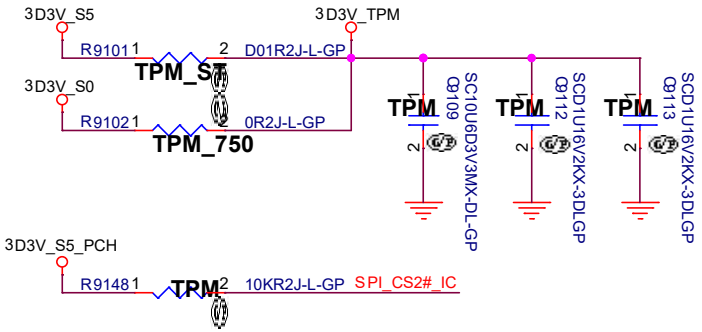
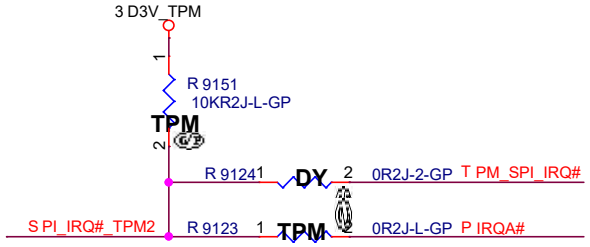
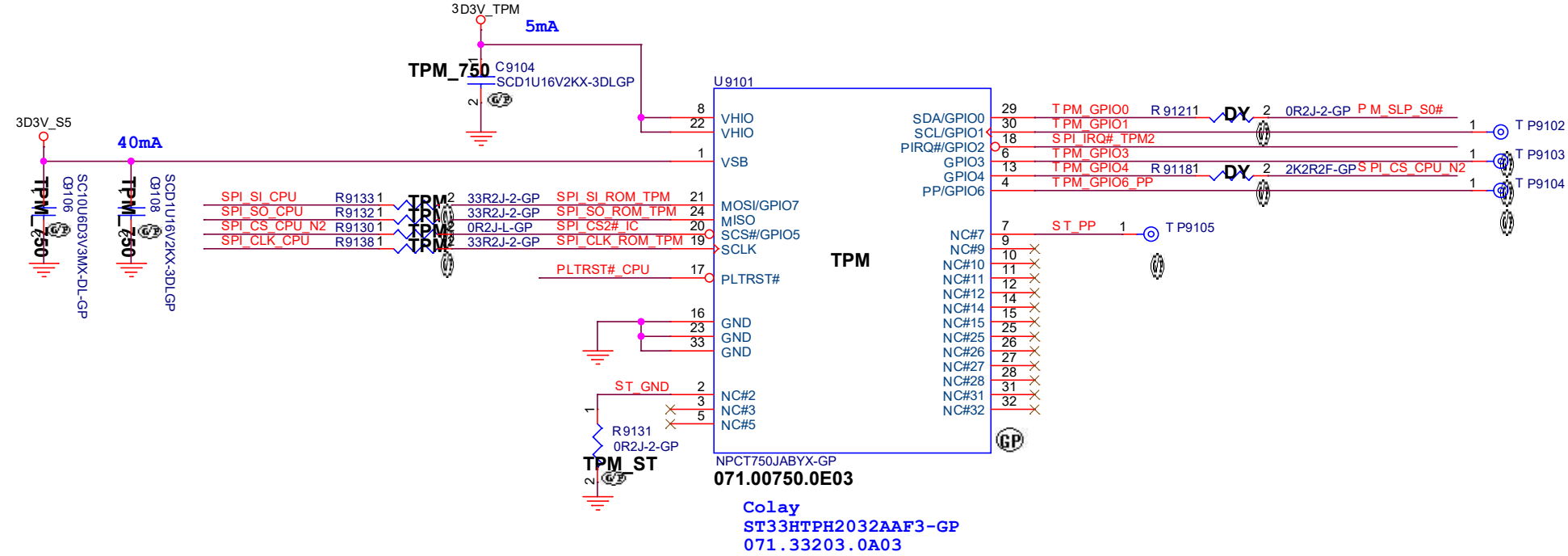
Main Func = TPM

15,18,25 SPI_SI_CPU
18 SPI_CS_CPU_N2
18,25 SPI_CLK_CPU
18,25 SPI_SO_CPU
17,40 PM_SLP_S0#
17,61,63,66,76 PLTRST#_CPU
18 TPM_SPI_IRQ#
20 PIRQA#







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ST33HTPH2032AAF3-GP
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Title: TPM2.0

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Main Func = FPR

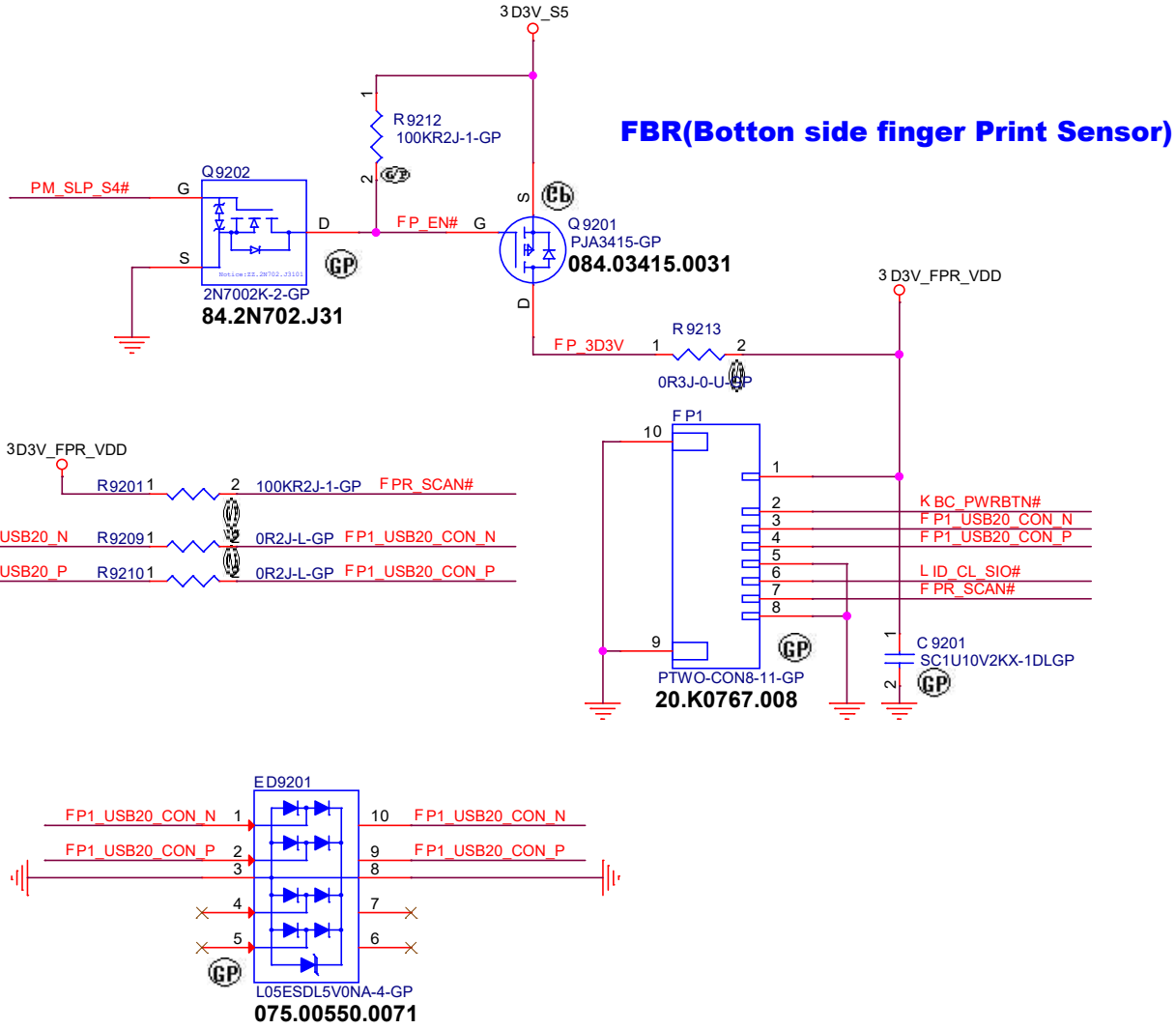
16 FP1_USB20_N
16 FP1_USB20_P
24 FPR_SCAN#
24,64 KBC_PWRBTN#
17,40,51 PM_SLP_S4#
20,24,64,67 LID_CL_SIO#

	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

GF5288WN1+GF128A+GM168 Module design

CN PIN Map

Pin NO.	INFO
1	VCC 3.3V
2	PWBTN
3	USB N
4	USB P
5	GND
6	LID closed
7	GPIO Key shielding
8	GND (ID pin)



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Title: ***(Reserved)Finger Print***

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Title: *LVDS_Switch*

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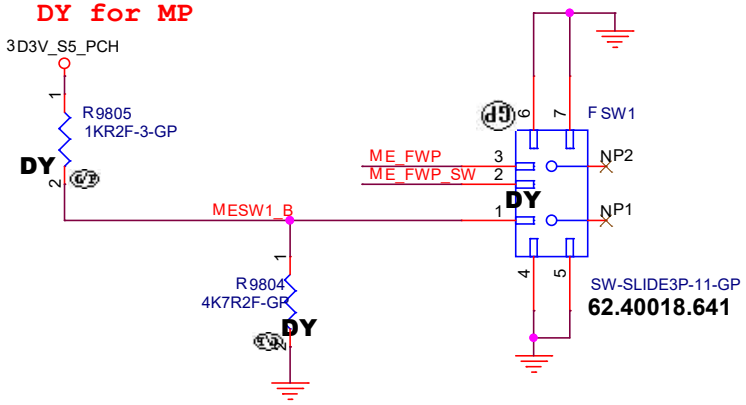
Main Func = SWITCH

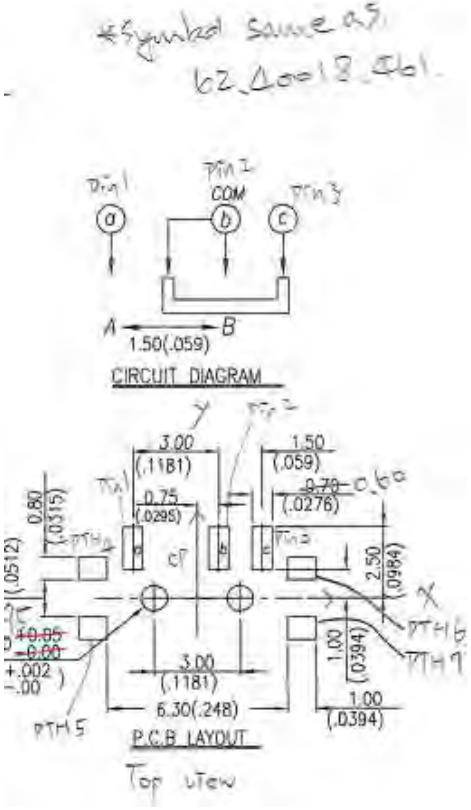
24 ME_FWP >>>——
19 ME_FWP_SW <<<——

Firmware SW

Default setting:pull LOW
DY for MP



	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override



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Title	CRT_Switch	
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SSID = Debug

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Title: CPU_XDP;PCH_XDP

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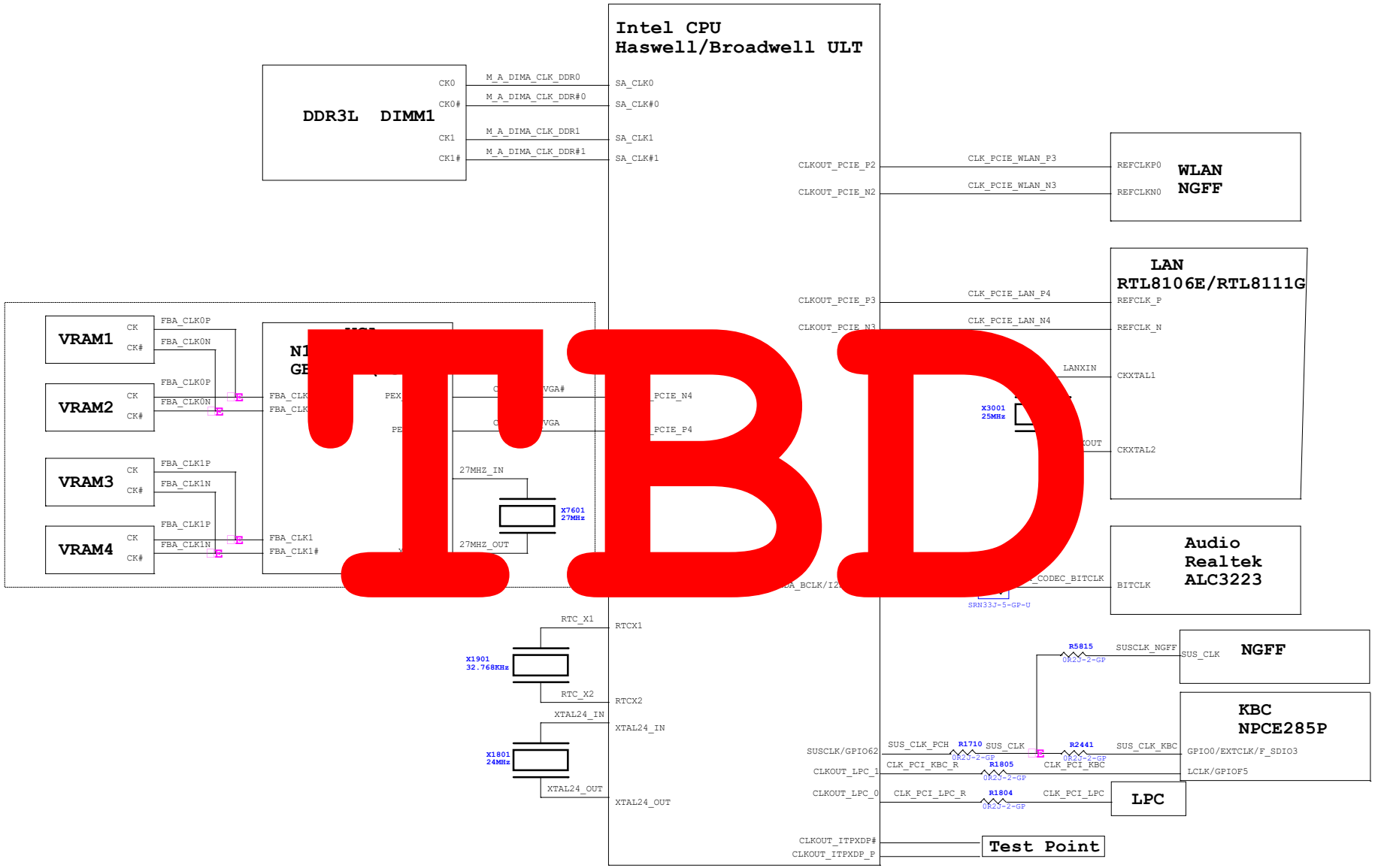
CLK Block Diagram



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Title: CLK Block Diagram

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Change notes -

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Title: **Change History**

Size: A | Document Number: **WASP 13" WHL-U** | Rev: **A00**

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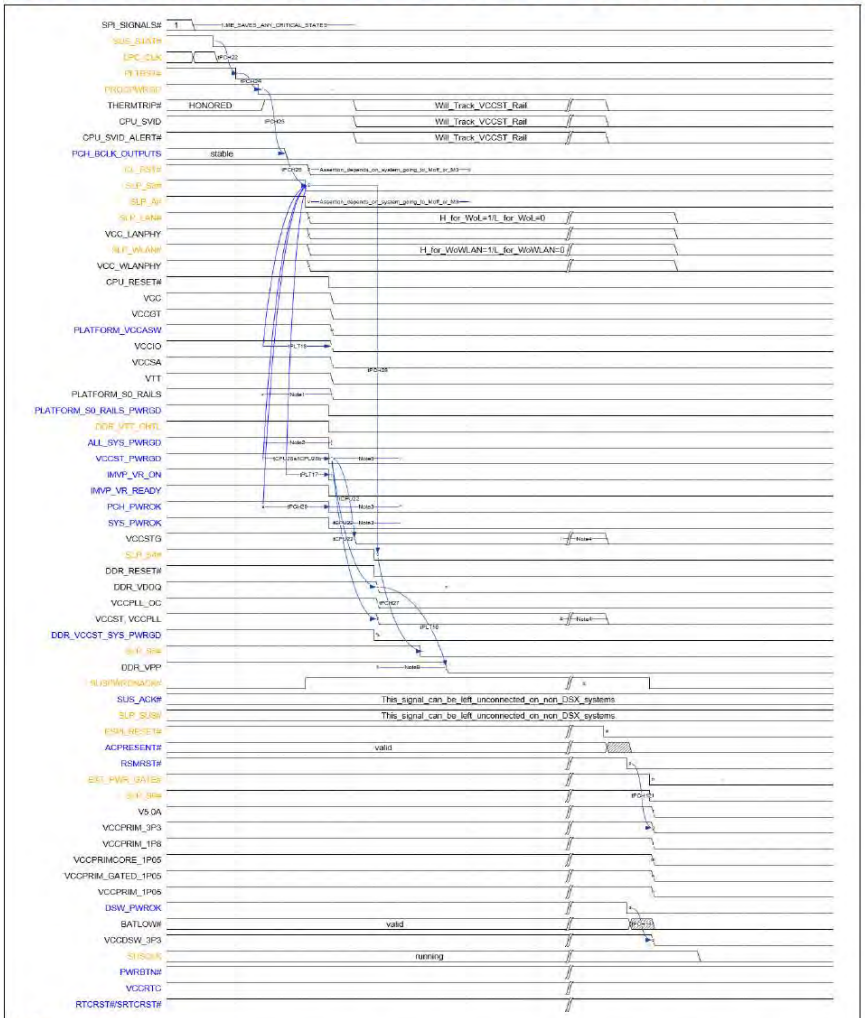
Figure 12-21.WHL-U Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]



Notes:

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST, VCCSTG, and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must deassert in all Sx / DSx states, regardless of the status of the VCCST / VCCSTG rails
6. Present on LPDDR3 and DDR4 systems only. Must ramp down **AFTER** VDDQ has ramped down

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Title: *Power Sequence*

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Title: Power Block Diagram

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Title: SMBUS Block Diagram

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Title: Thermal/Audio Block Diagram

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Title

CLK Block

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