

COMPAL CONFIDENTIAL

MODEL NAME : DAZ40

PCB NO : LA-F322P

BOM P/N : 431A8U31L0X

Steamboat MLK 14" NonAR

Kabylake-U U22 & Kabylake-R U42

2017-12-29

REV : 2.0 (A01)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESDComponent

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

ESPI@ : ESPI interface Component

LPC@ : External ESPI Component (SHD)

INFI@ : Inf i n i t y S K U C o m p o n e n t

U42@ : KBL-R U42 Component

U22@ : KBL-R U22 Component

DS3@ : Deep sleep Component

NDS3@ : Non Deep sleep Component

546@ : TI TUSB546 Component

8743@ : PARADE PS8743 Component

MB PCB

Part Number	Description
DA8001CH010	PCB 265 LA-F322P REV0 MB NAR 1

Layout Dell logo



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REV:A01
PWB: YWCKR

Power CKT : 0920

GPIO map : 0821

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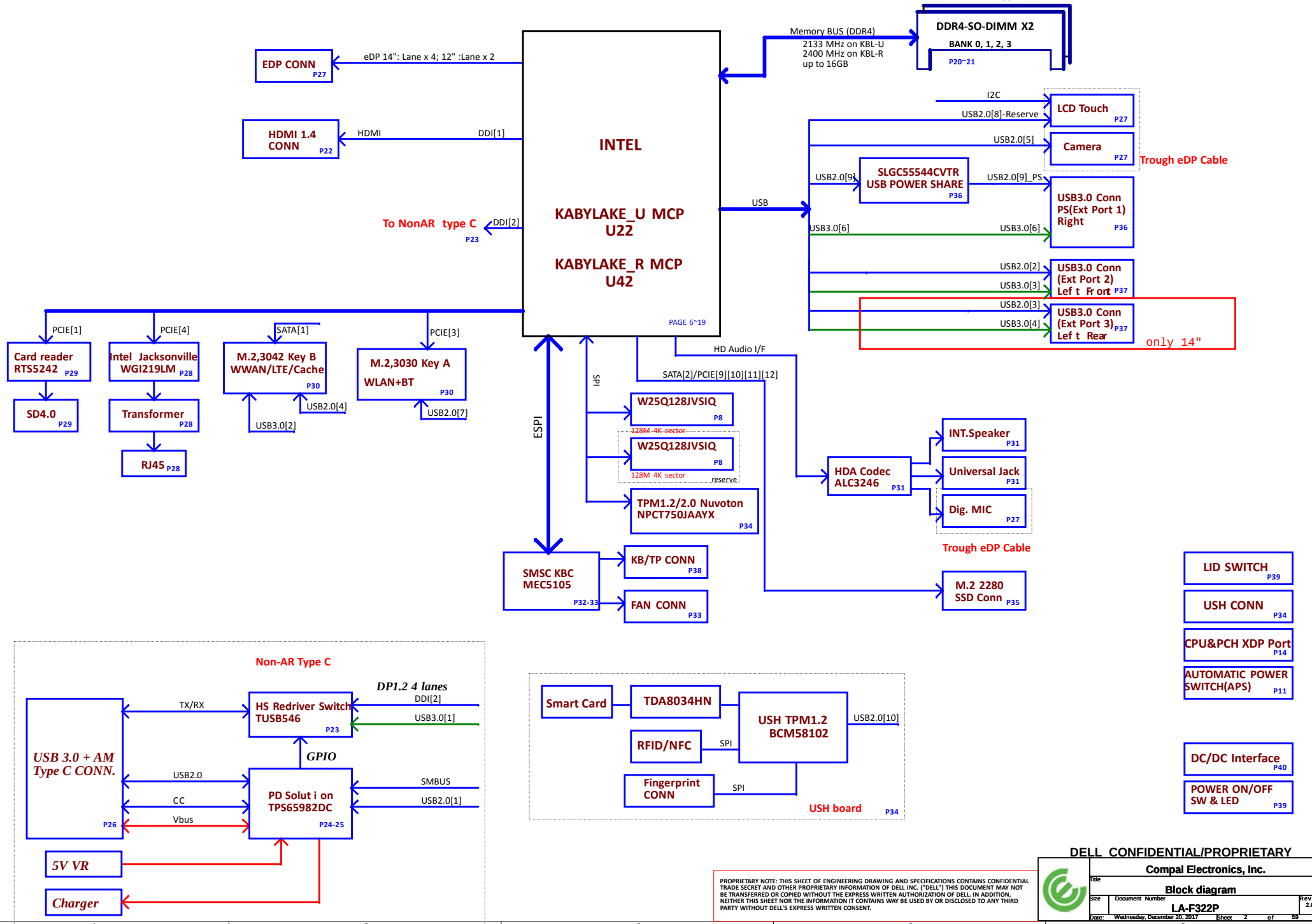
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Steamboat MLK 14 w/o AR Block Diagram

Steamboat MLK 12&13 only support one DIMM
Reverse Type



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1 (mm) ± 10%)				39.4	41.40000

AR use 1086PP (10L)
Non AR use 1080PP (8L)

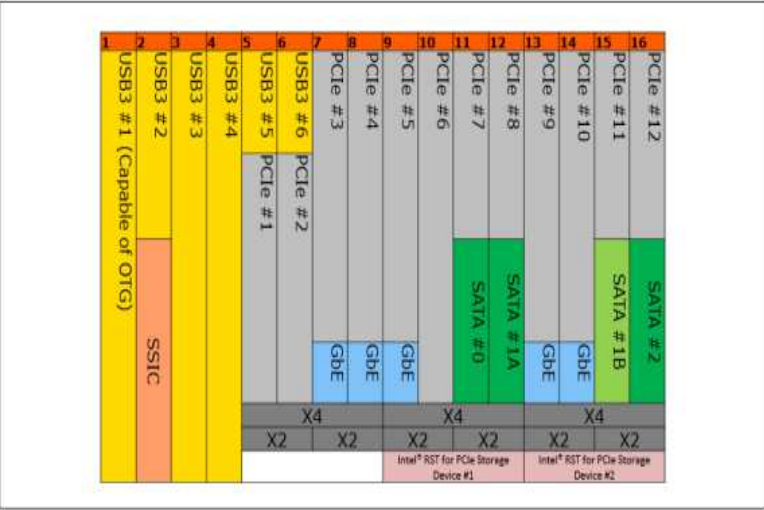
NonAR config

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Typce-C(Non AR)
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t Frort
USB3.0-4				JUSB3-->Lef t Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	M.2 3042(SATA Cache)
		PCIE-9		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	Typce-C(Non AR)
2	JUSB2-->Lef t Frort
3	JUSB3-->Lef t Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

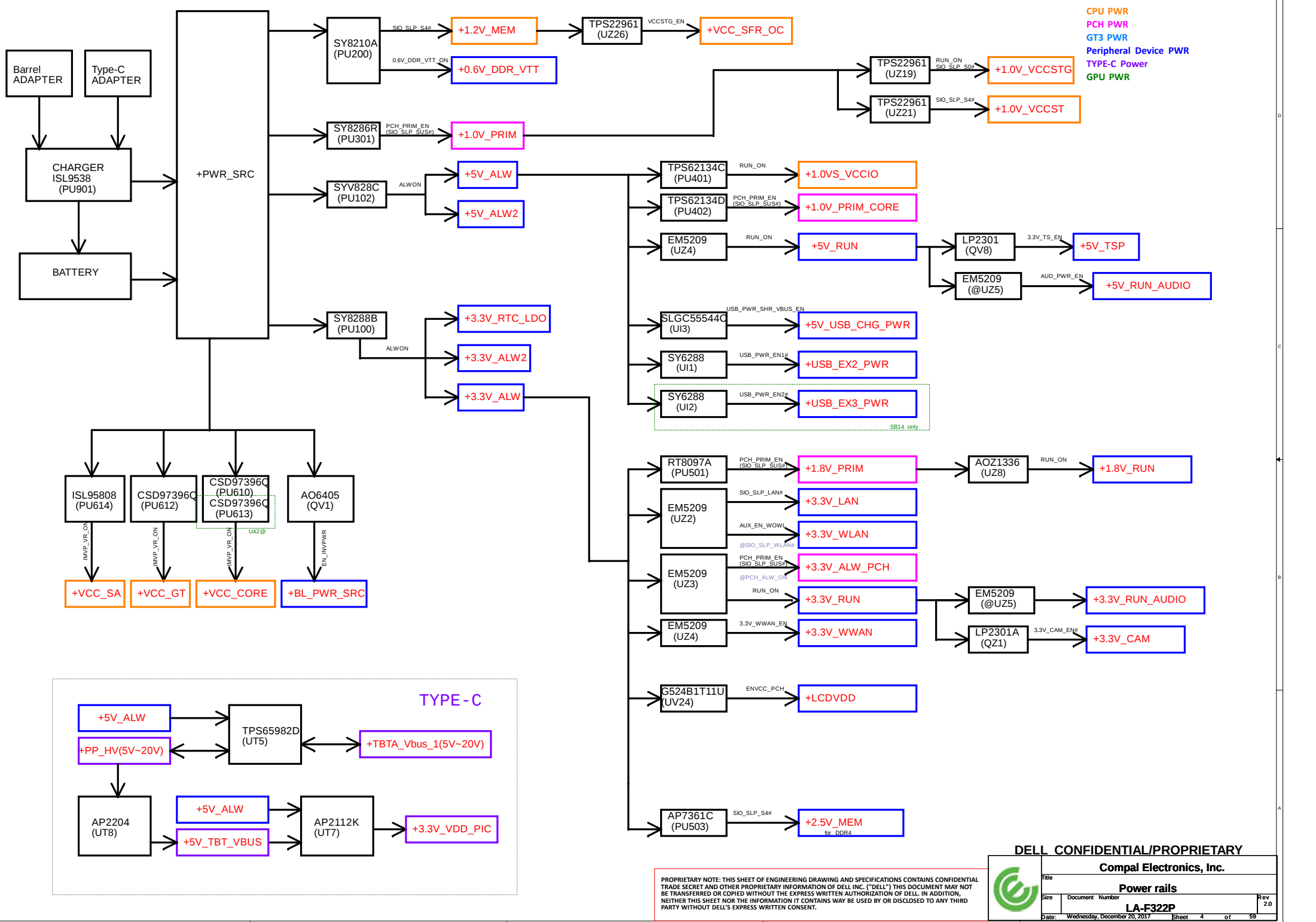
High Speed I/O (HSIO) Lane Multiplexing in KBL U



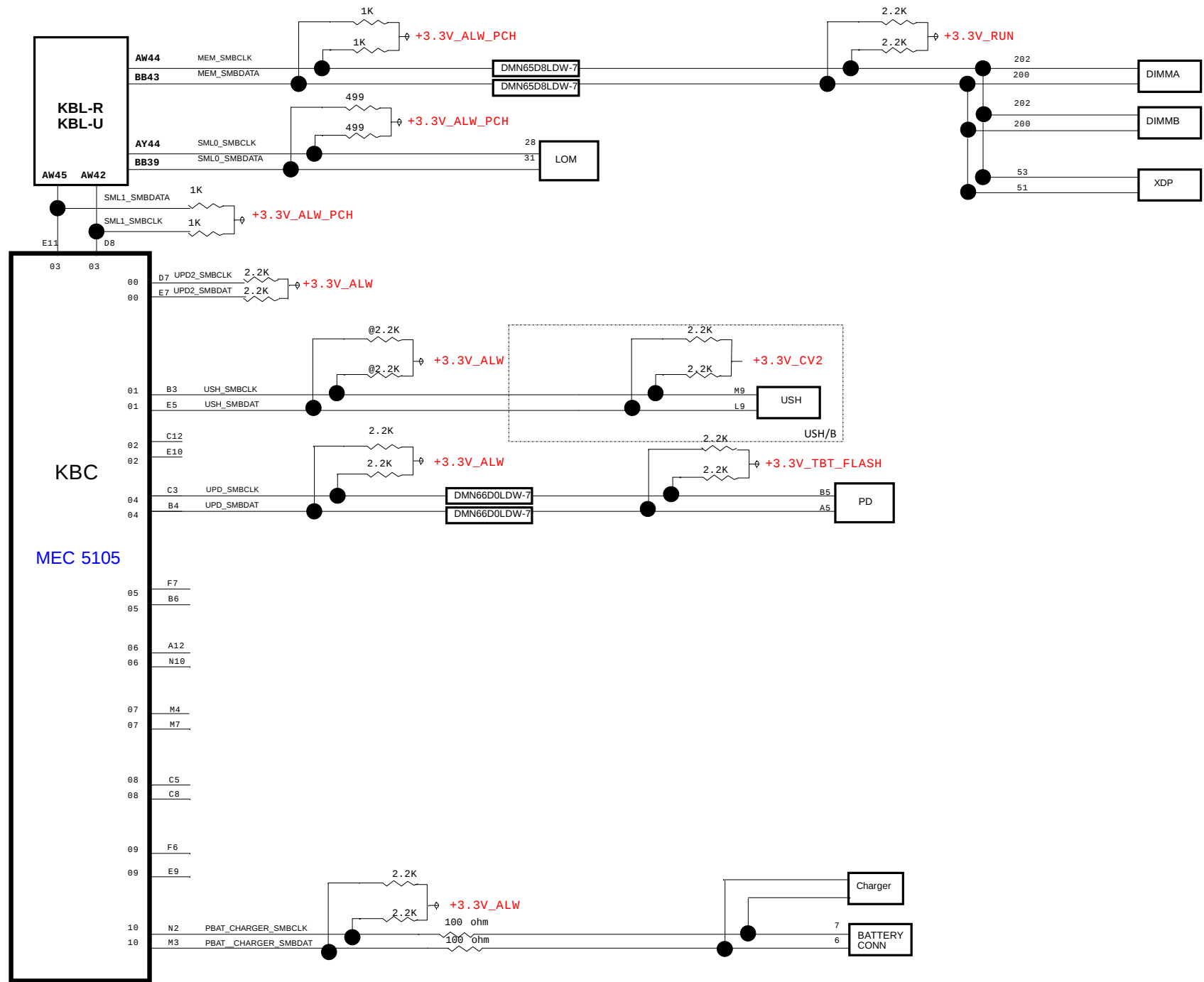
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Port assignment			
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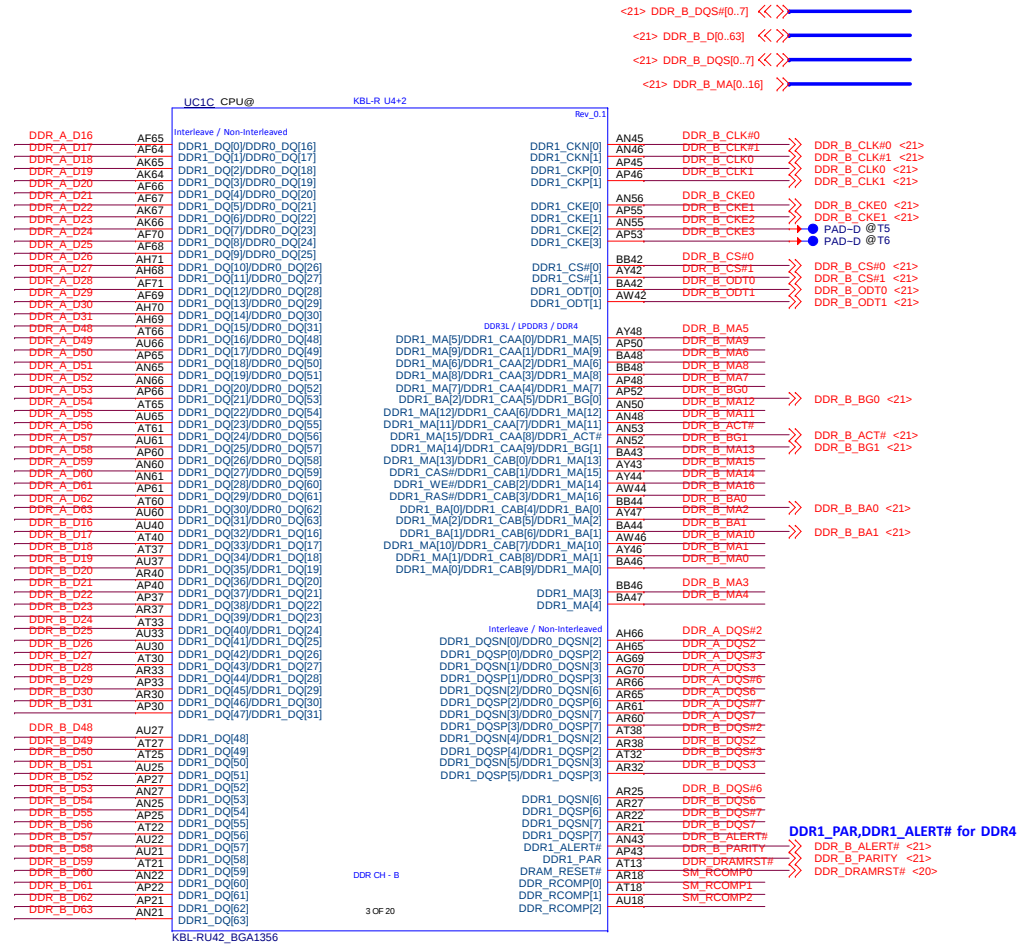
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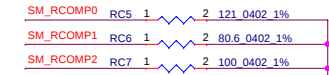
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For DDR4

DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

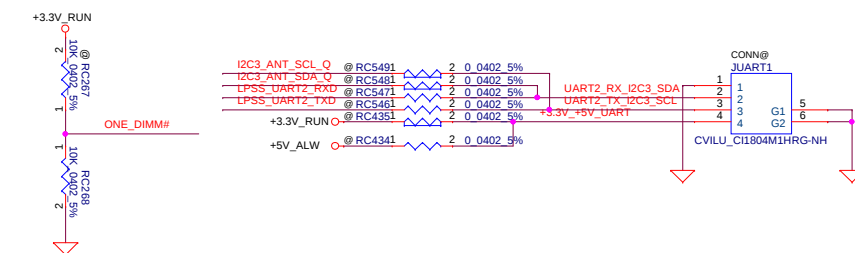
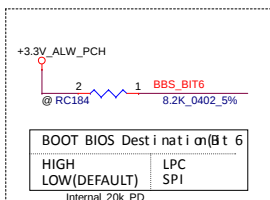
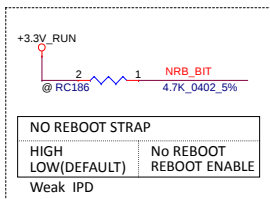
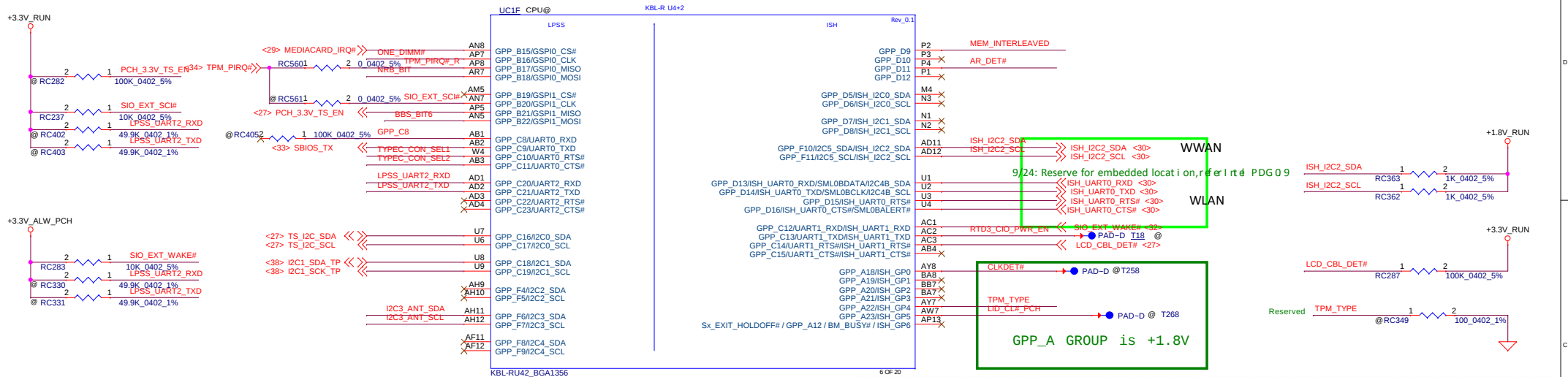
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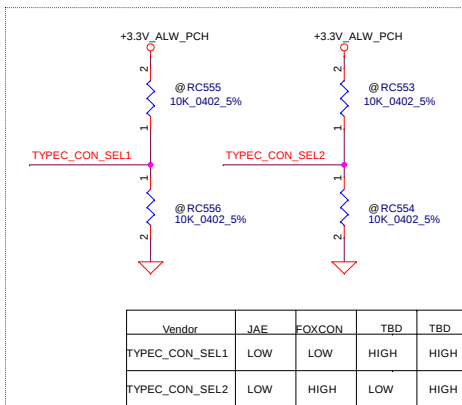
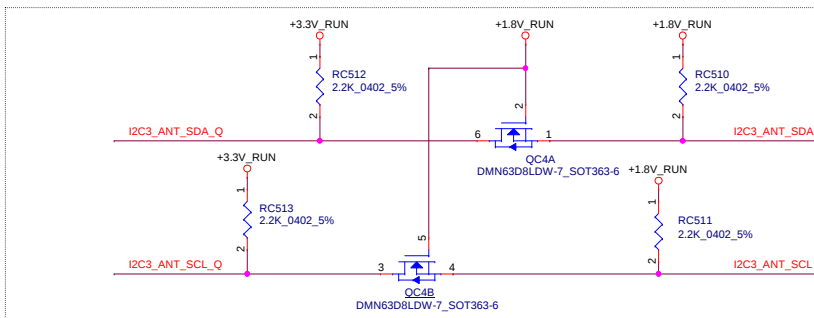
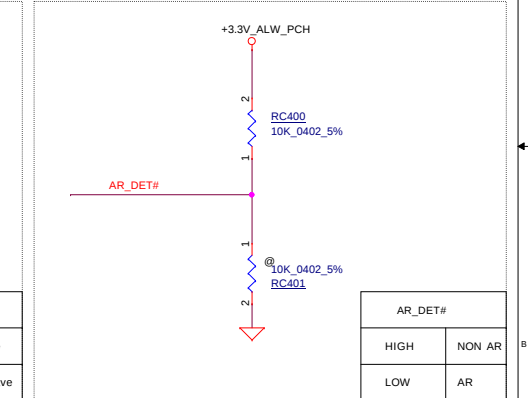
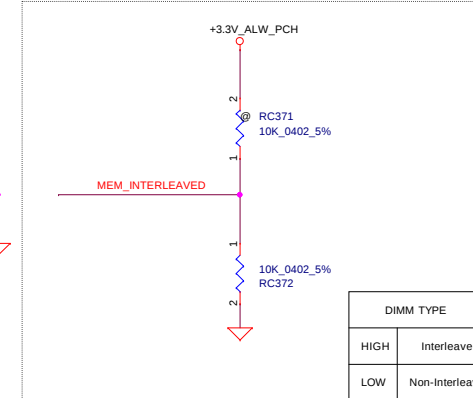
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For BR/SB



DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

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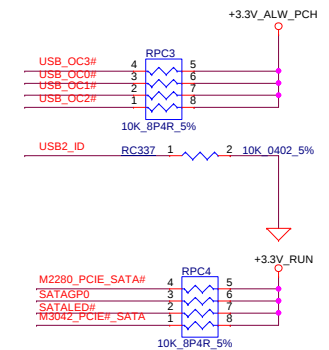
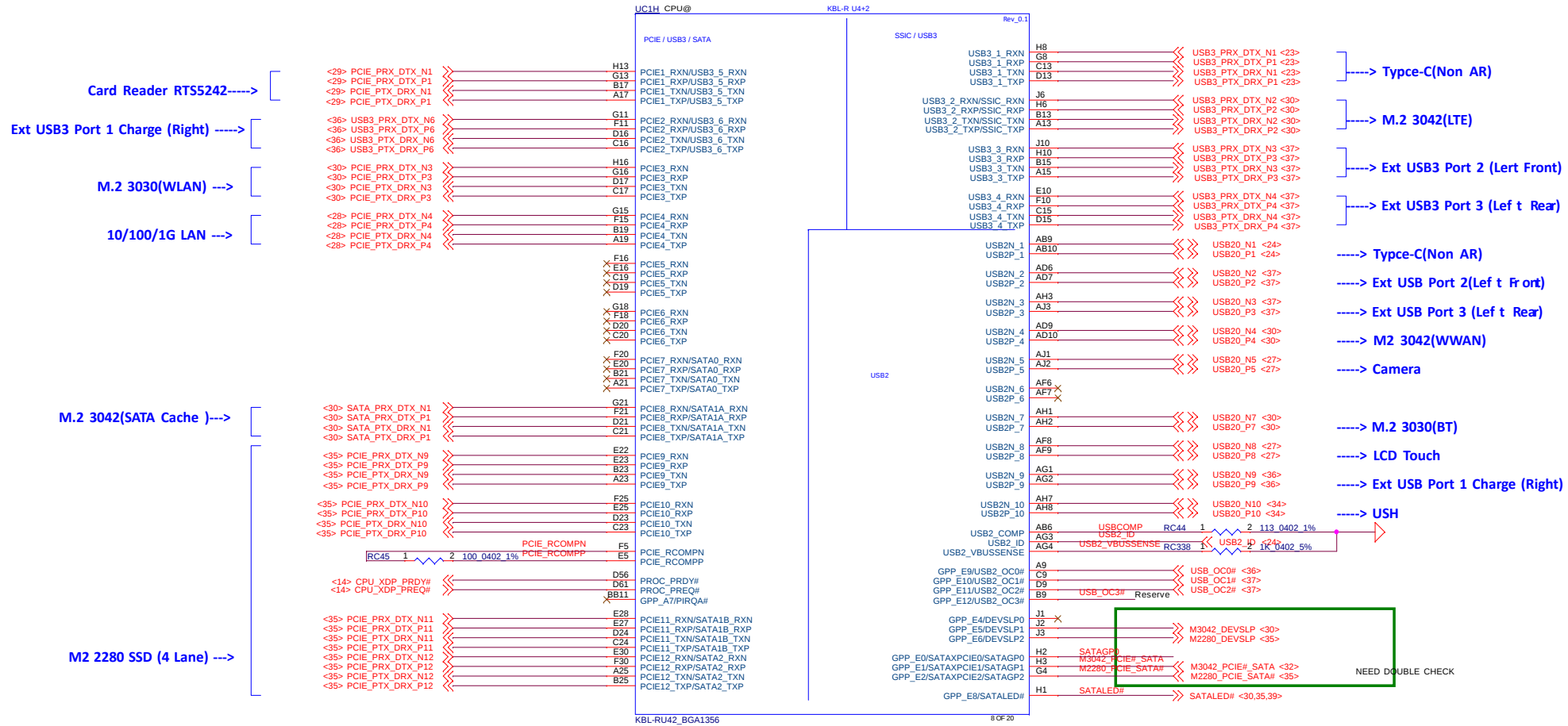
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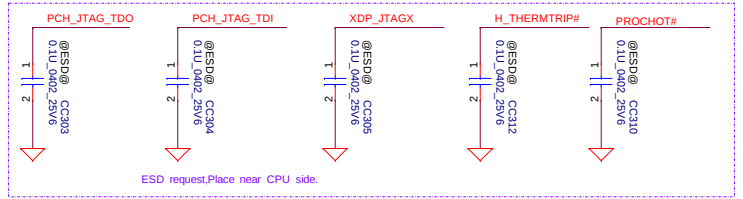
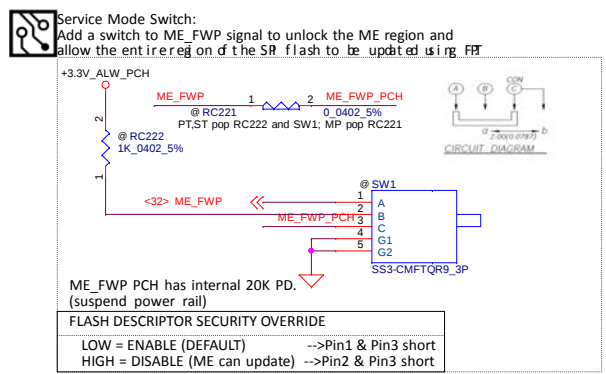
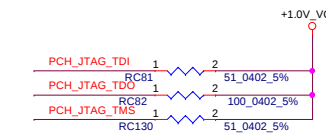
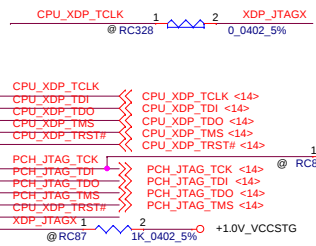
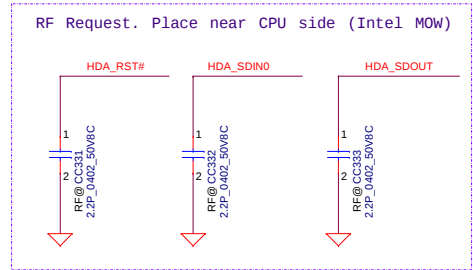
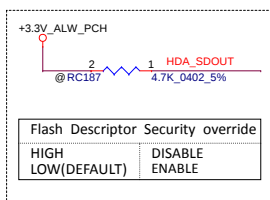
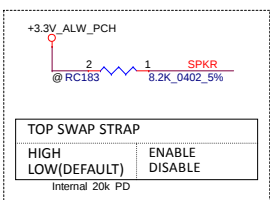
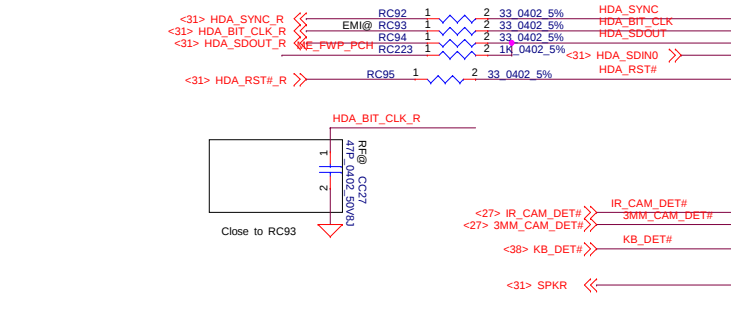
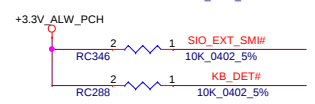
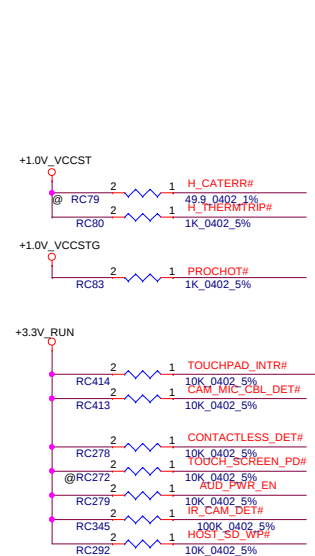
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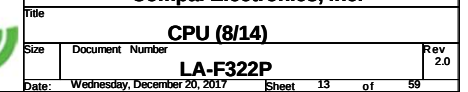
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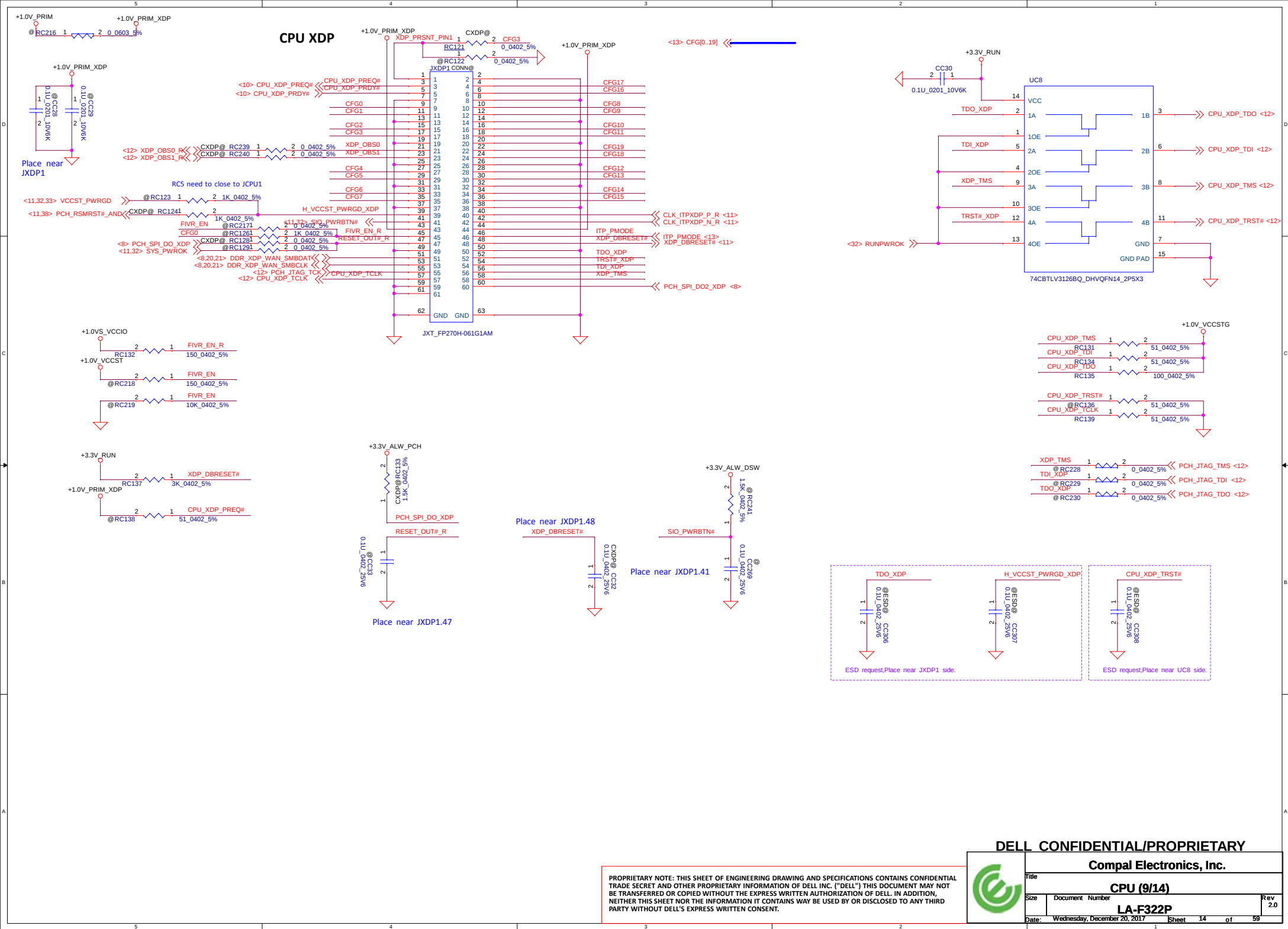
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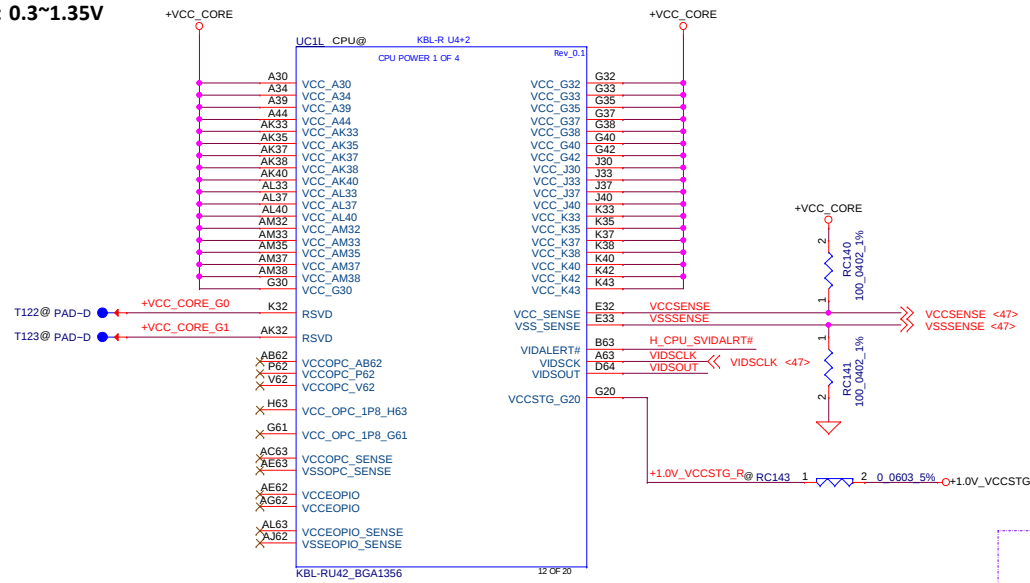


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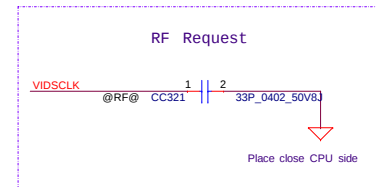


+VCC_CORE: 0.3~1.35V

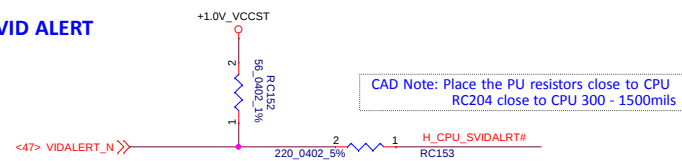


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

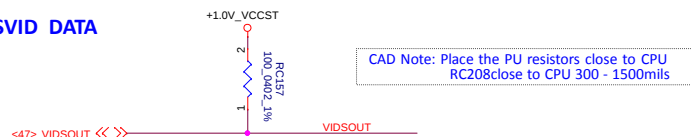
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source



SVID ALERT



SVID DATA



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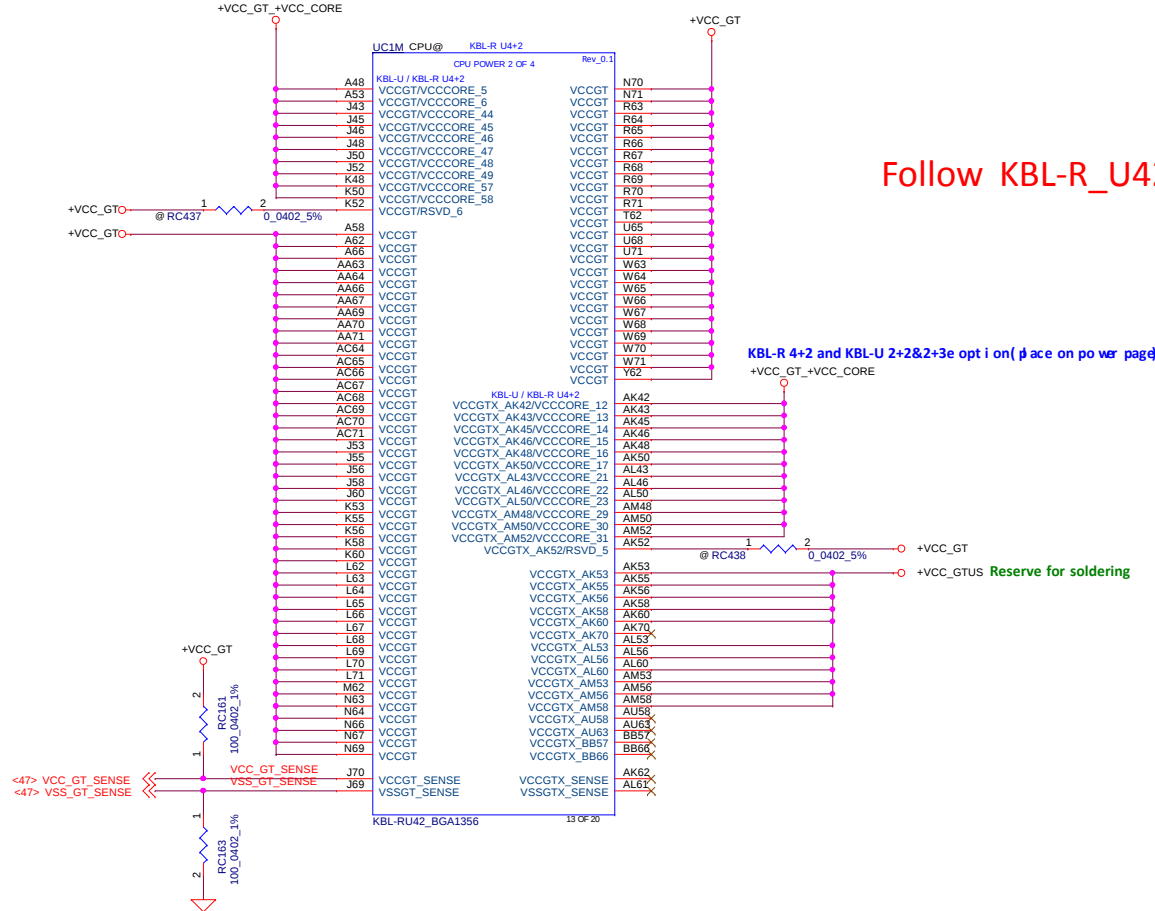


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+VCCGT: 0.3~1.35V
+VCCGTx : 0.3~1.35V

KBL-R 4+2 and KBL-U 2+2&2+3e opt i on(place on po wer pag e)

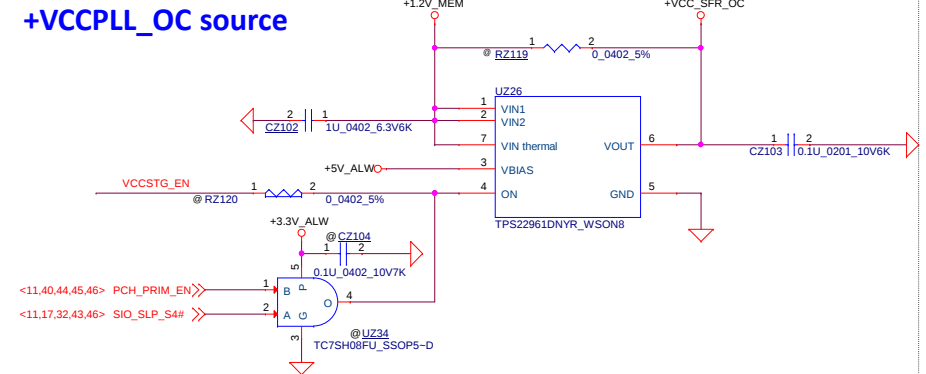
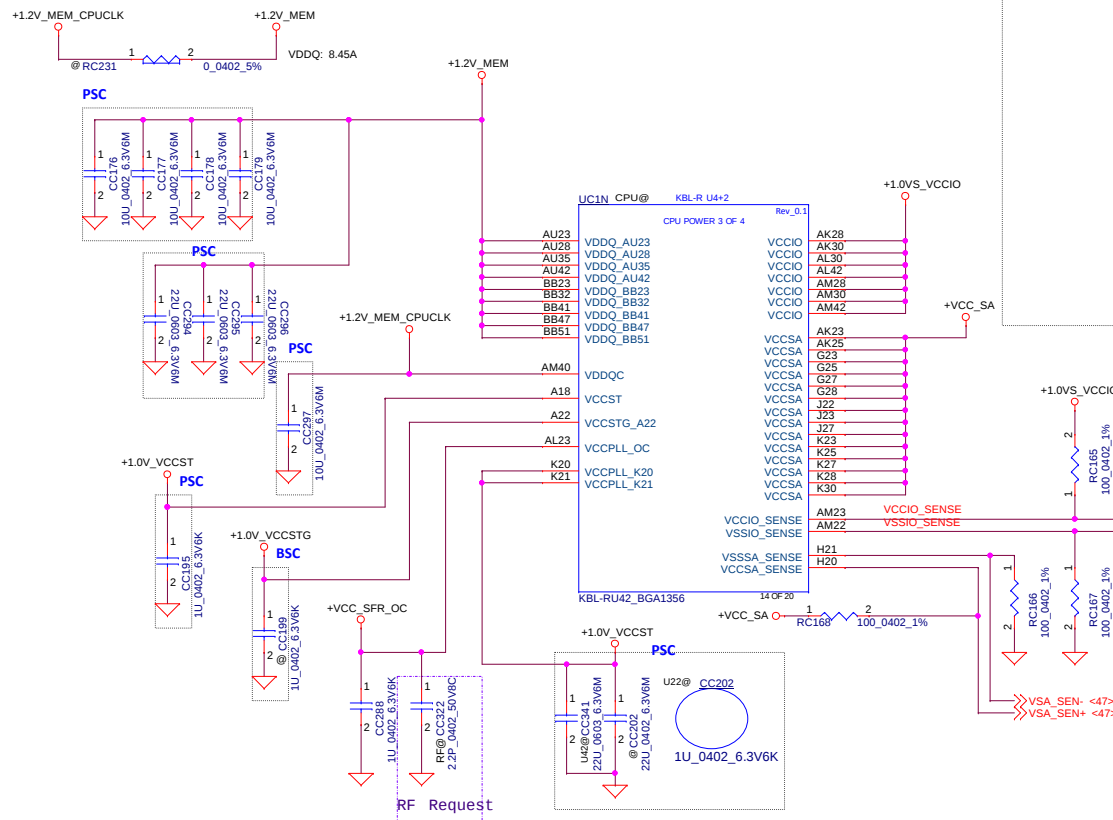


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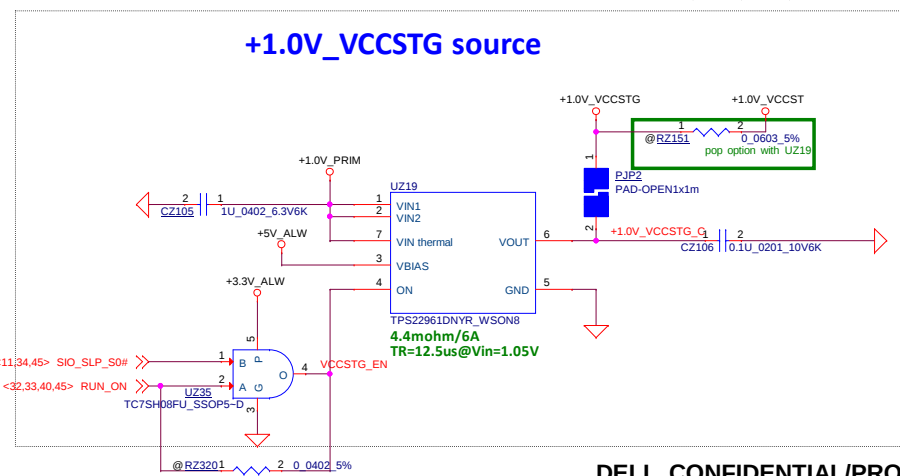
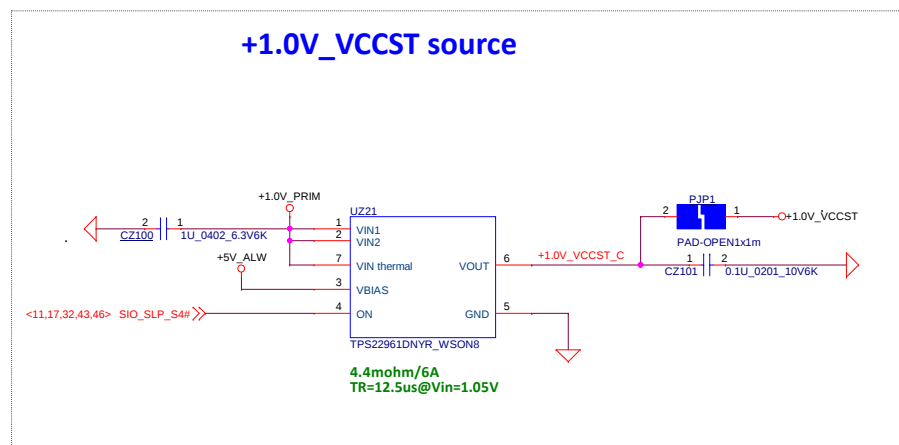
KBL-R 4+2 and KBL-U 2+2&2+3e opt i on(place on po wer pag e)

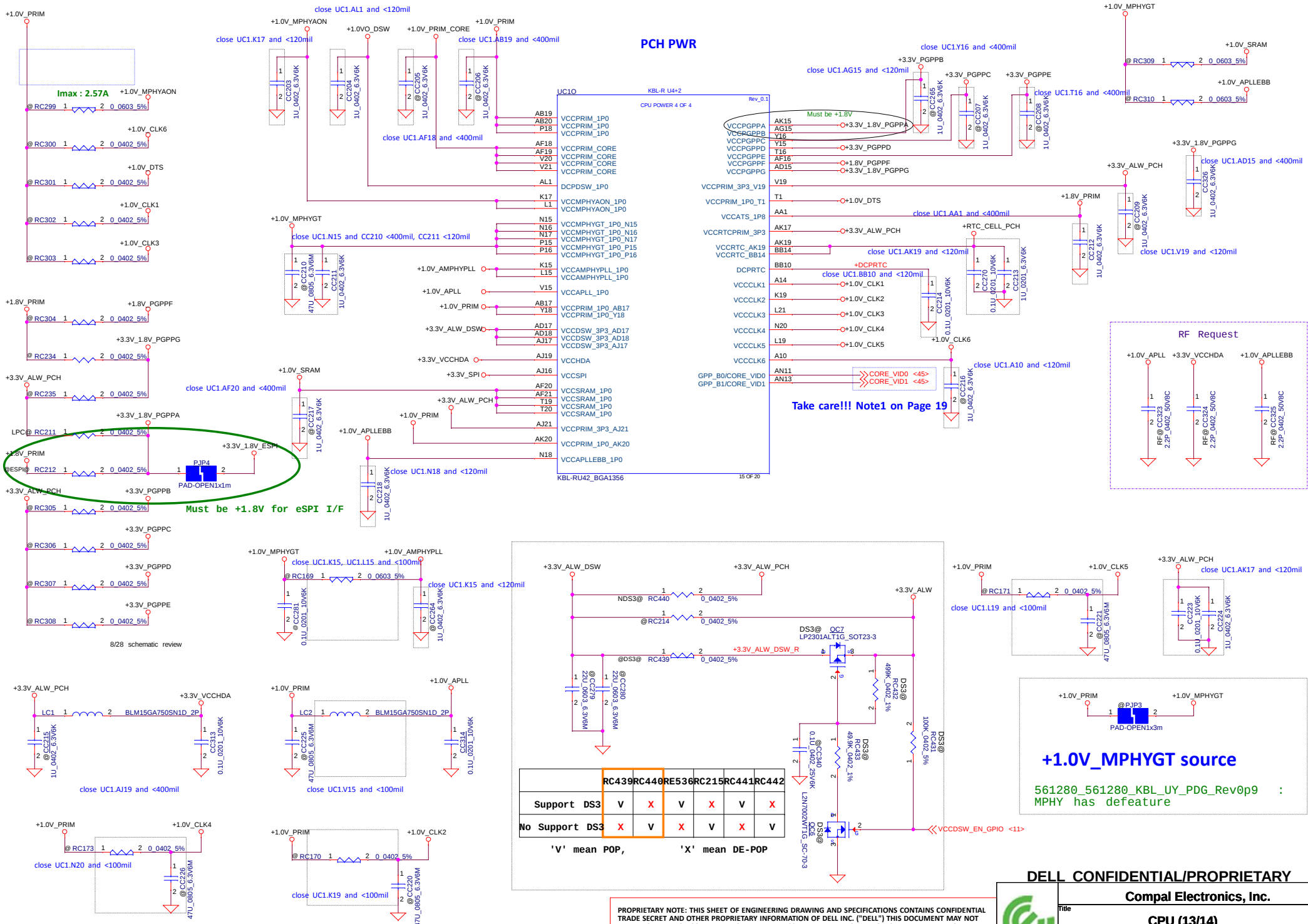
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	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW





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CPU (13/14)

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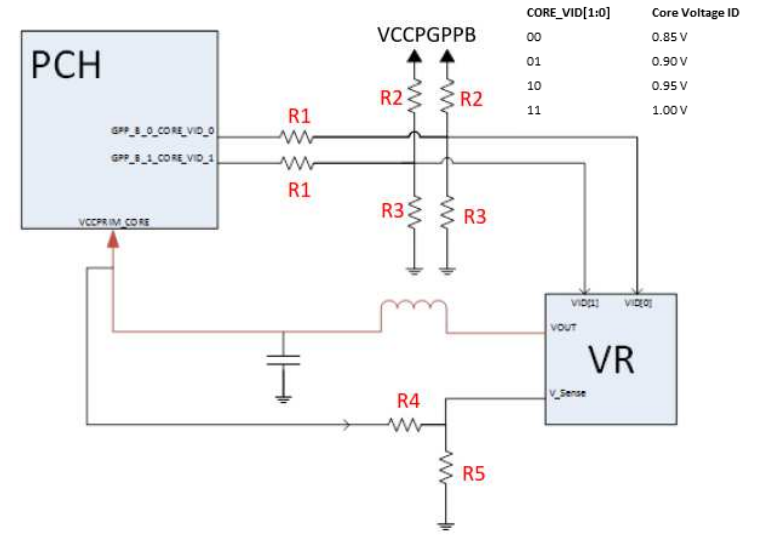
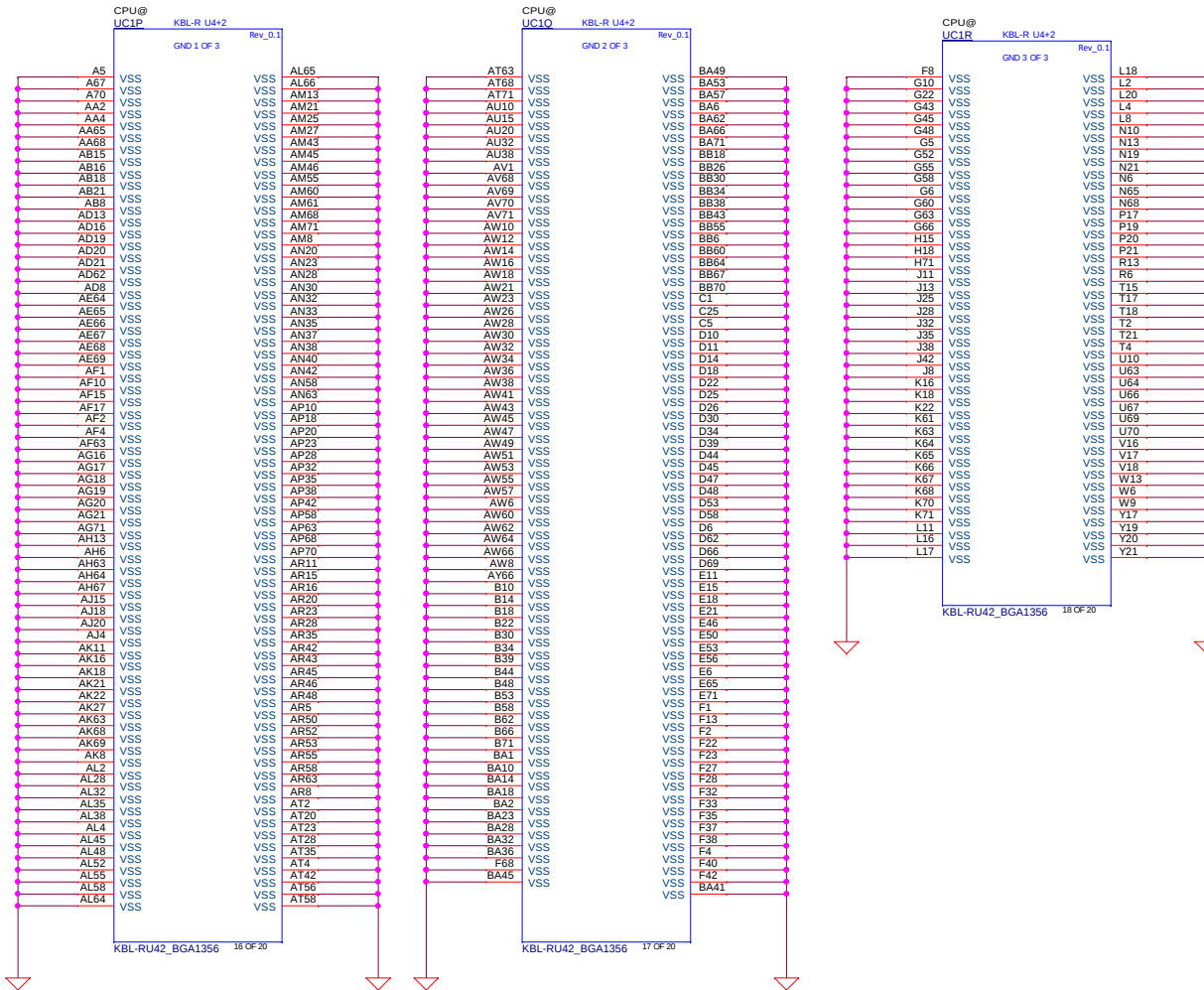
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Note1: VCCPRIM_CORE Implementat i on út h PCH CORE_V D Reco mnendat i on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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CPU (14/14)			Rev
LA-F322P			2.0
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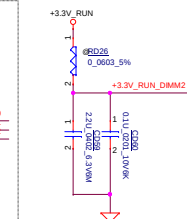
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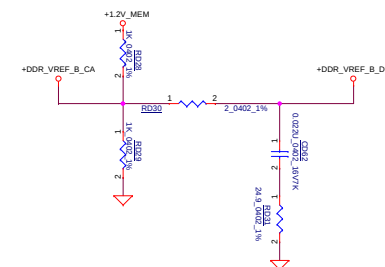
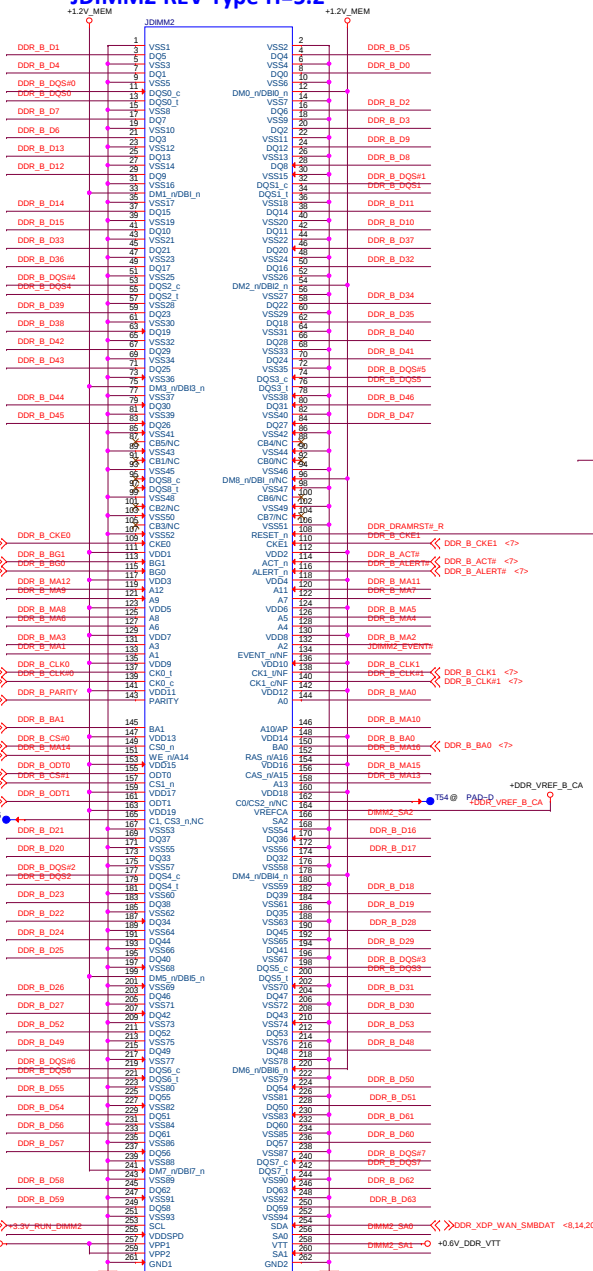
Note:
var JDIMM2



Diagram illustrating a 2D grid of vias for a power plane. The grid is defined by three columns and two rows of vias. Each column is connected to a 3.3V RUN source. Each row is connected to a DIMM2 signal line (SA0, SA1, SA2). The vias are labeled with resistor values (RD20, RD22, RD24, RD21, RD23, RD25) and a tolerance of 0.0402_5%.



LINK SP07001D200 DONE



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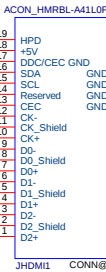
Compal Electronics, Inc.

DDR4

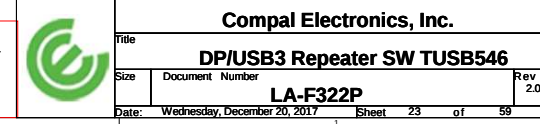
Size	Document Number
	LA-E322P

LA-F322P

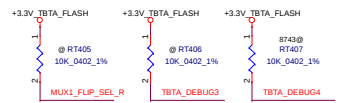
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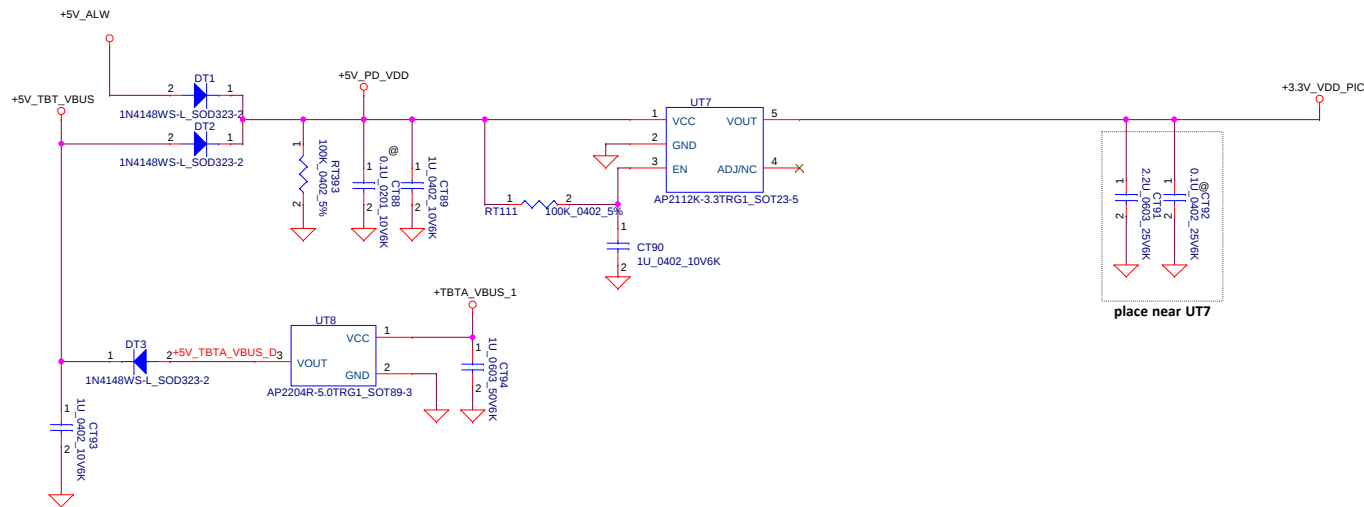
TUSB546: Pop RT300,Depop RT145,RT301
PS8743:Depop RT301,Pop RT145,RT300(change to 0.1uf)(VDD_DCI)



				Compal Electronics, Inc.			
Title				[Type C]PD Controller TI			
Size		Document Number		LA-F322P		Rev 2.0	
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[illegible]

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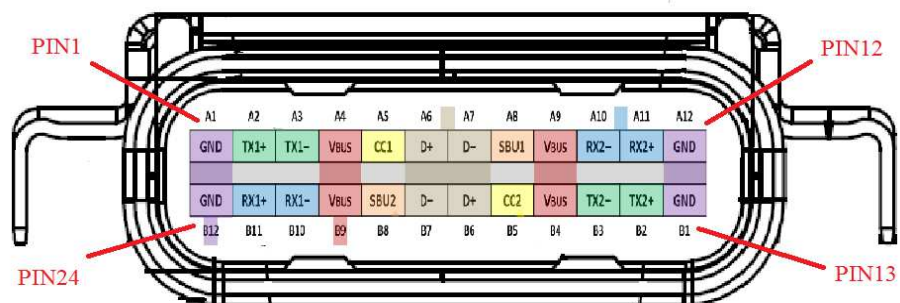
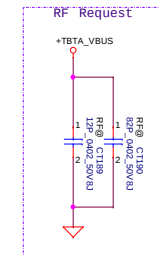
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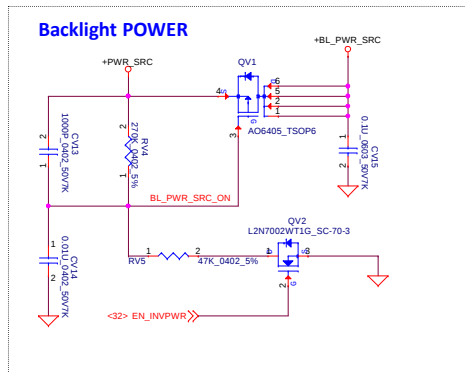
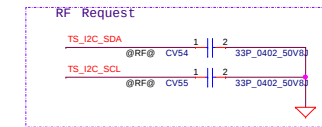
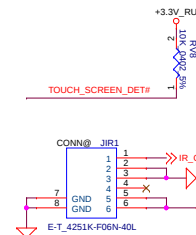
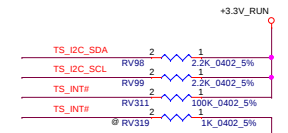
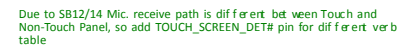
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Title		
[Type C]PD Power		
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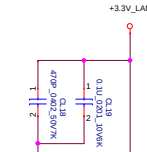
For Touchscreen

The schematic diagram illustrates the touchscreen interface circuit. It features two NPN transistors, QV7 and QV8, both of type LP2301ALT1G, SOT23-3. QV7's base is connected to the PCH_3.3V_TS_EN signal through a 100K resistor (RV324). Its emitter is connected to ground, and its collector is connected to the +3.3V_RUN supply through a 100K resistor (RV323). QV8's base is connected to the <32> 3.3V_TS_EN signal through a 100K resistor (RV400). Its emitter is connected to ground, and its collector is connected to the +5V_TSP supply through a 50K resistor (RV6). The diagram also shows various power supply connections: +5V_RUN, +5V_TSP, +3.3V_RUN, and +5V_RUN.

LCDVDD POWER

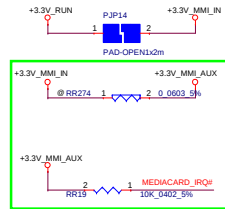
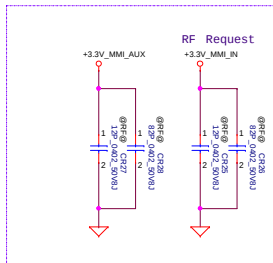
The schematic diagram illustrates the LCDVDD power supply circuit. It features a 10uF/0603/10V6M capacitor connected to a CV16 pin. The signal from CV16 passes through a PAD-OPEN1x1m component to a P3P12 pin. The P3P12 pin is connected to the VOUT pin of an LV24 component. The LV24 component has a GND pin connected to a common ground and an EN pin connected to a divider network. The divider network consists of a 10k resistor (R3) and a 50k resistor (R4) connected to a 3.3V ALW supply. The output of the divider is connected to the EN pin of the LV24 component. The LV24 component has an I/O pin connected to a common ground. The output of the LV24 component is connected to a 0.01uF/0602/25V6K capacitor, which is then connected to the LCDVDD pin. The LCDVDD pin is also connected to a 3.3V ALW supply. The LCDVDD pin is connected to the LCDVDD pin of the LCD module. The LCD module also has a GND pin connected to a common ground. The LCD module has a PCH pin connected to a divider network. The divider network consists of a 10k resistor (R5) and a 50k resistor (R6) connected to a 3.3V ALW supply. The output of the divider is connected to the PCH pin of the LCD module. The LCD module also has a TEST_EN pin connected to a common ground.

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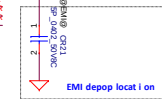
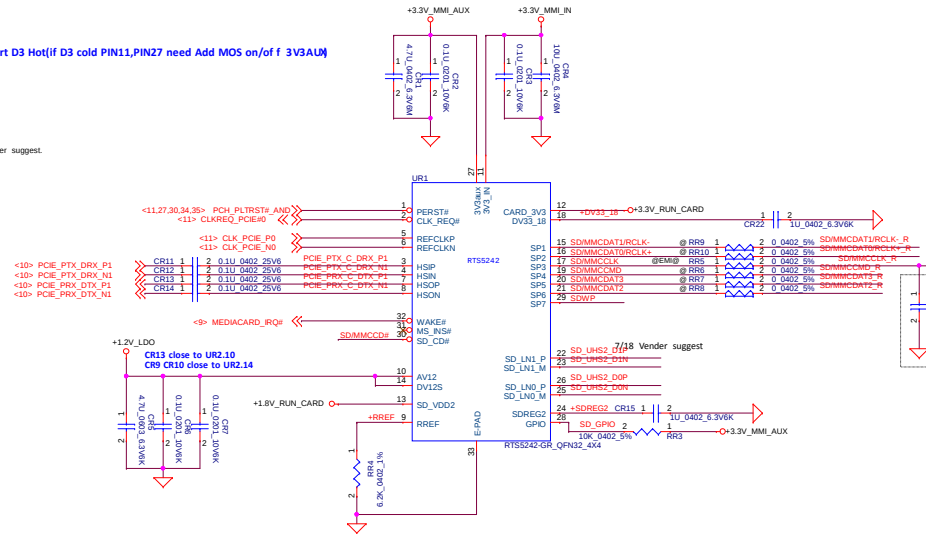
The diagram shows a capacitor with value 10P_1808_3KV(J) connected between a signal line (pin 2) and a ground plane (pin 1). The ground plane is labeled GND CHASSIS. A red arrow points from the signal line to the capacitor, and a red arrow points from the capacitor to the ground plane. A red line connects the signal line to a red label +GND_CHASSIS. A red line also connects the signal line to a red label RL15.2. A red line connects the ground plane to a red label use 40mil trace if necessary. A red line connects the ground plane to a red label 0601:EMI ask to change 150pF.

For PCIE Interface

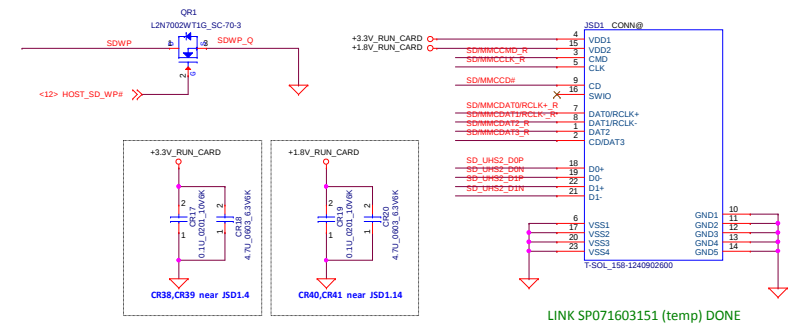


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)



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Card Reader RTS5242

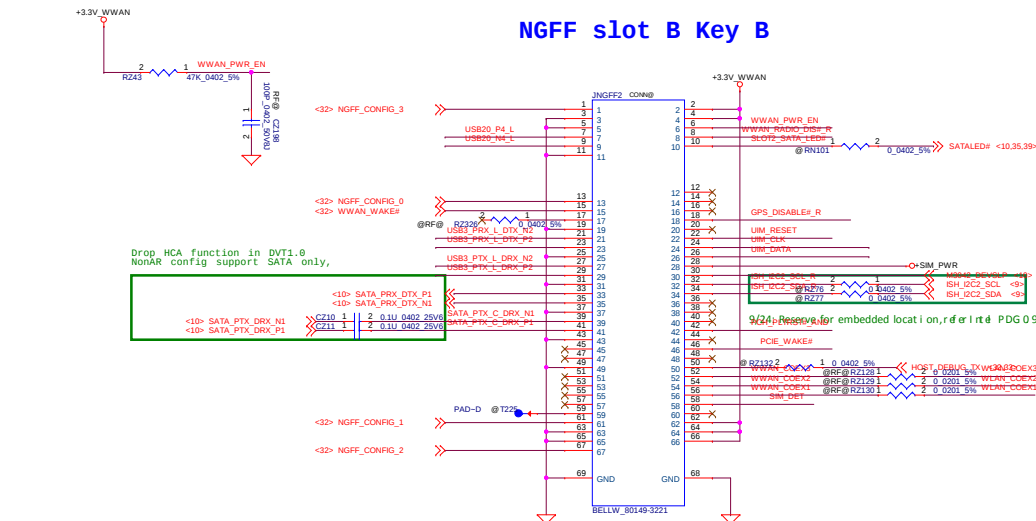
LA-F322P

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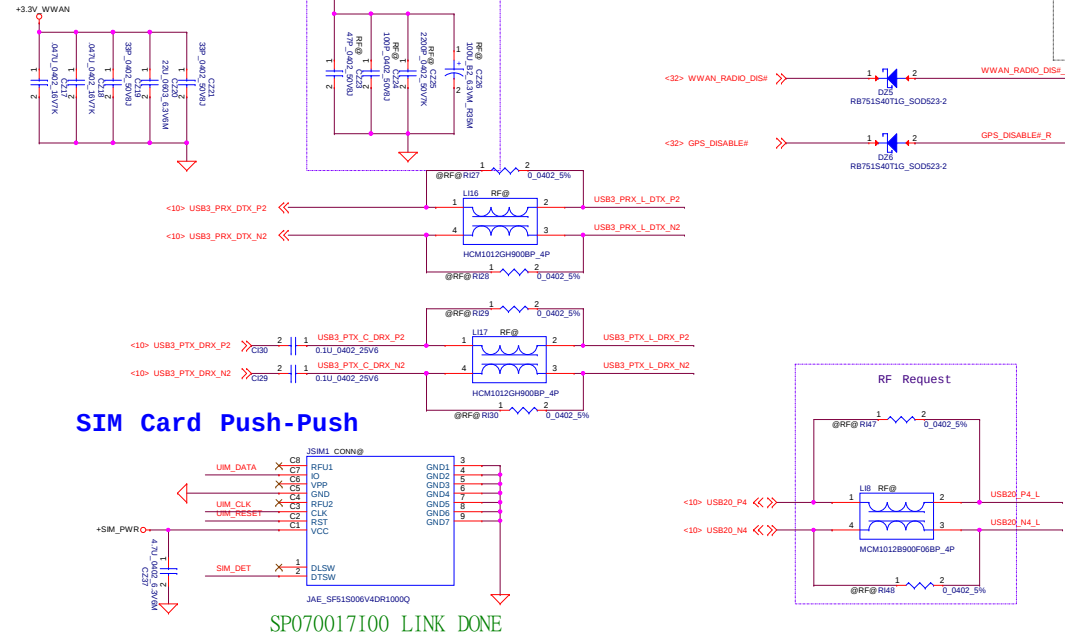
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NGFF slot B Key B



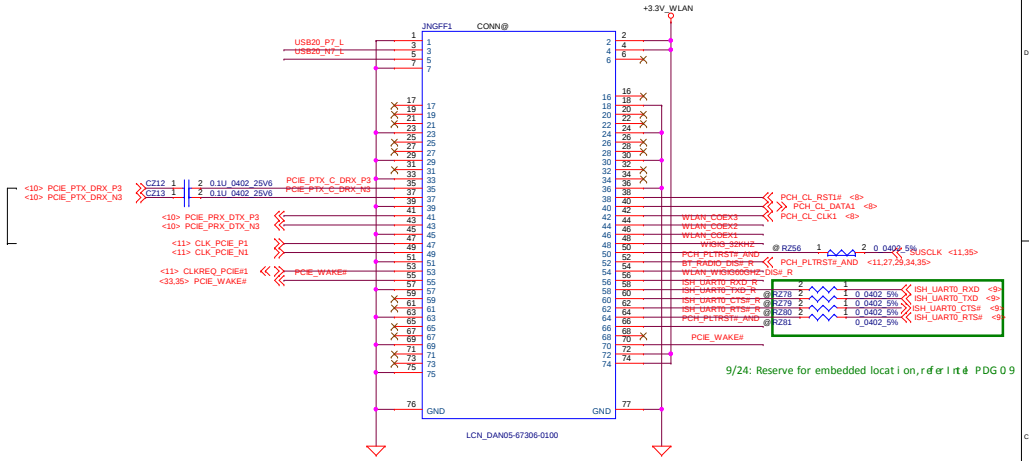
80149-3221 LINK DONE



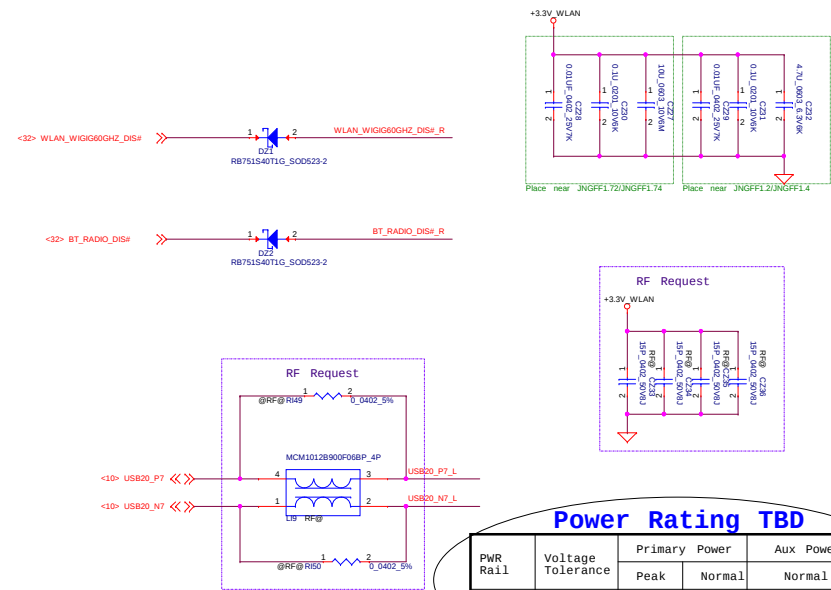
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

for no AR, Breckenridge 12/14/15 UMA/Steamboat

NGFF slot A Key A



SP070019F00 LINK DONE



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power Peak	Aux Power Normal	Aux Power Normal
+3.3V				

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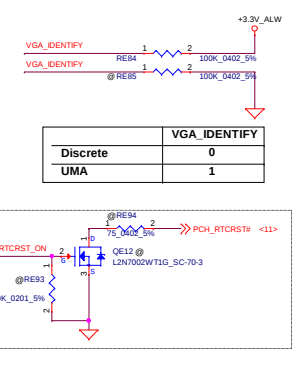
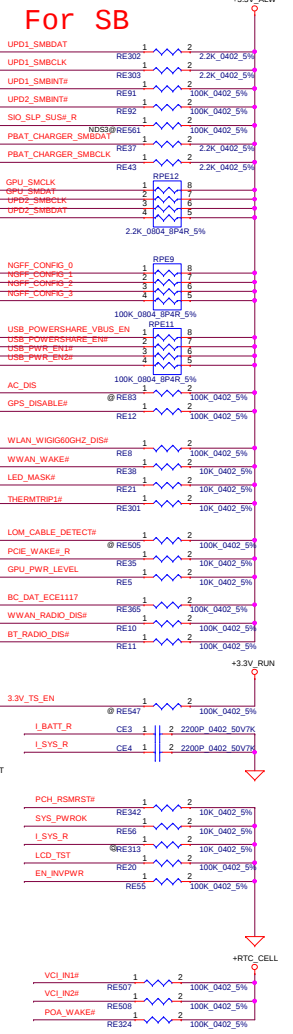
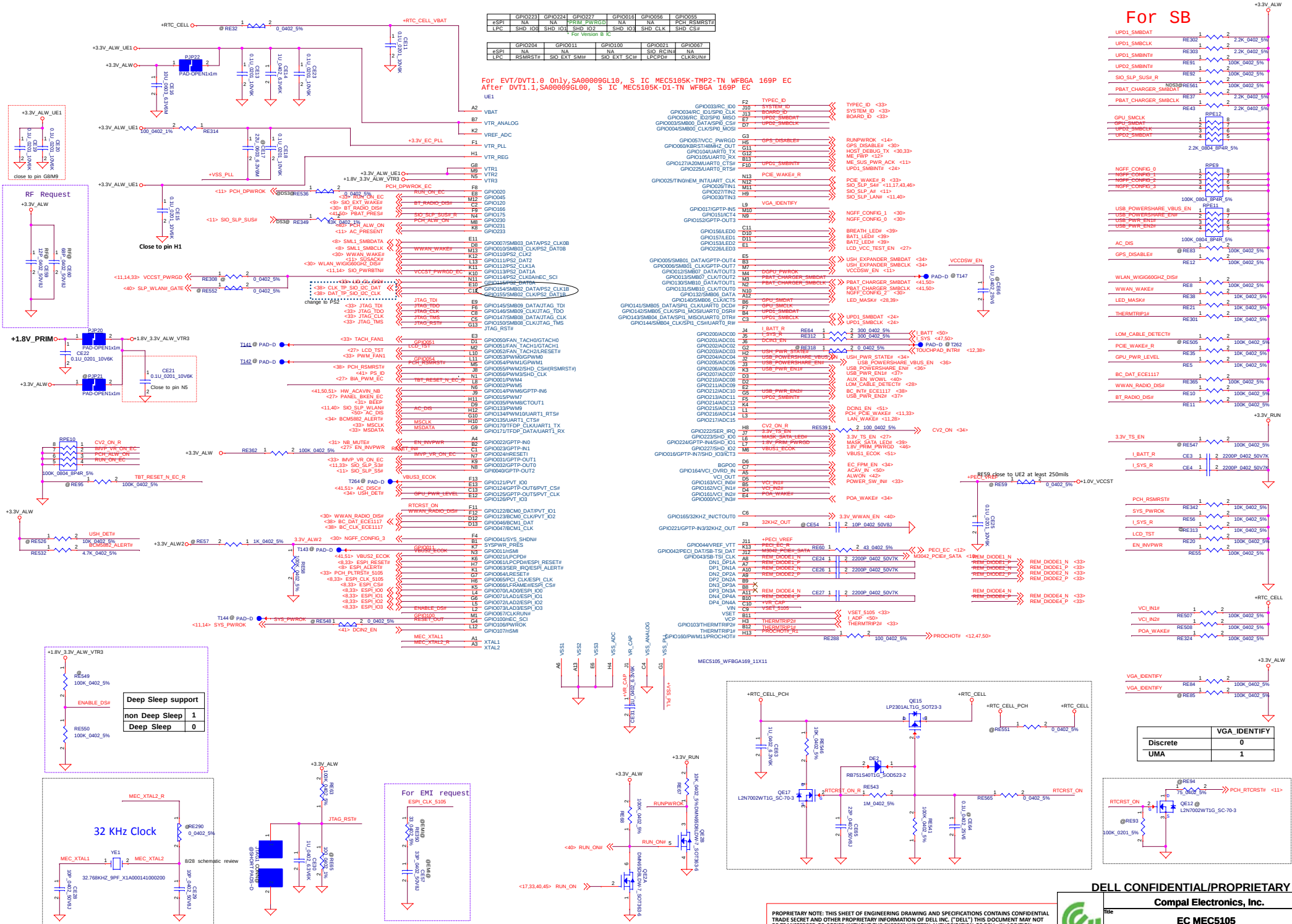
Compal Electronics, Inc.

NGFF Card

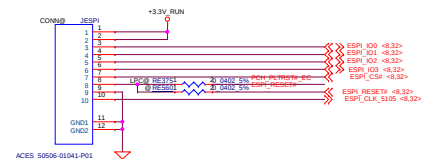
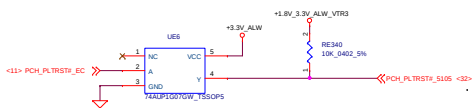
LA-F322P

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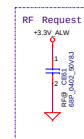
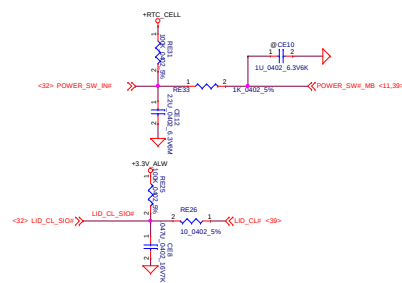


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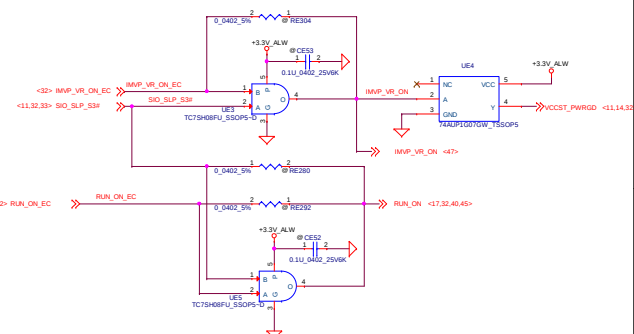
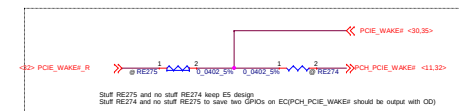
LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRSTH	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR + w/o AR)
4.3K	4700p	.
2K	4700p	.
1K	4700p	.

PD_ACE_DET# rise t1 nEIS measured from 5% to 68%

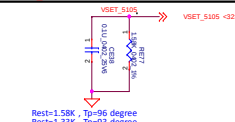
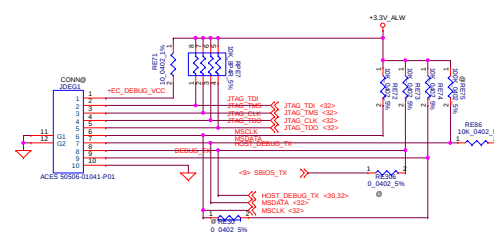


RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	A01
1K	4700p	.

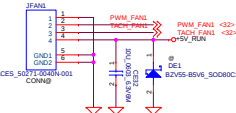
BOARD_ID rise t1 nEIS measured from 5% to 68%

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	.

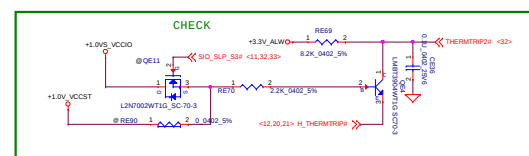
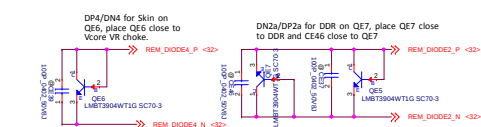
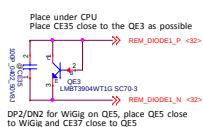
SYSTEM_ID rise t1 nEIS measured from 5% to 68%



Link 50271-0040N-001 DONE



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

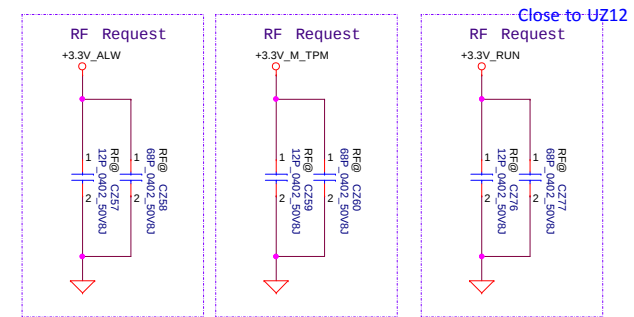


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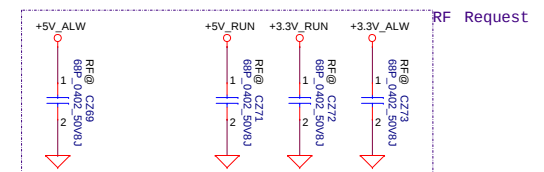
Rev	Document Number	Rev
1	MEC5105 support	2.0
1	LA-F322P	2.0

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ESD@ CZ61
.047U .0402 .16V7K

For ESD solution



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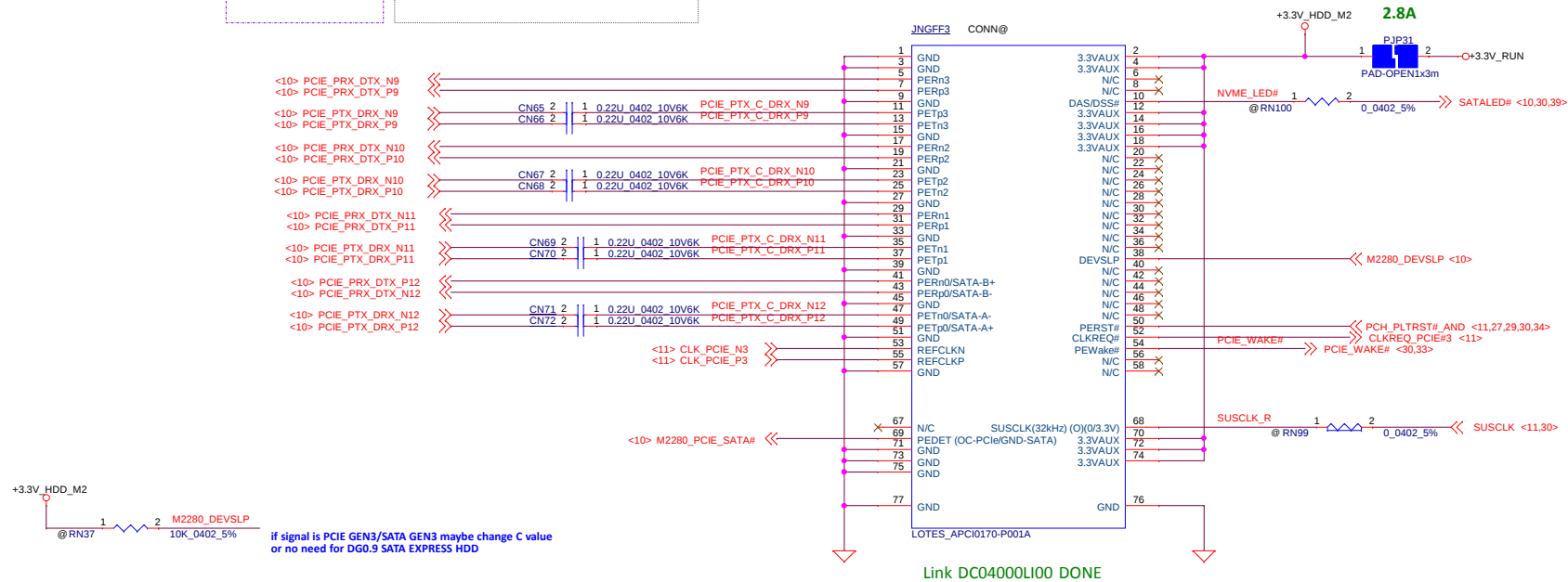
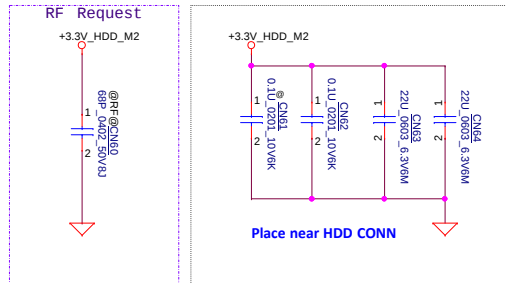
USH & TPM

LA-F322P

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2280 SSD

NGFF slot C Key M



Link DC04000LI00 DONE

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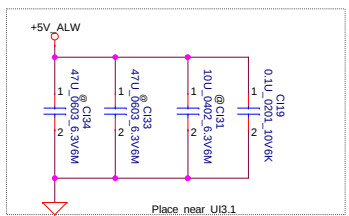
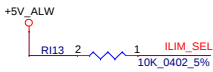
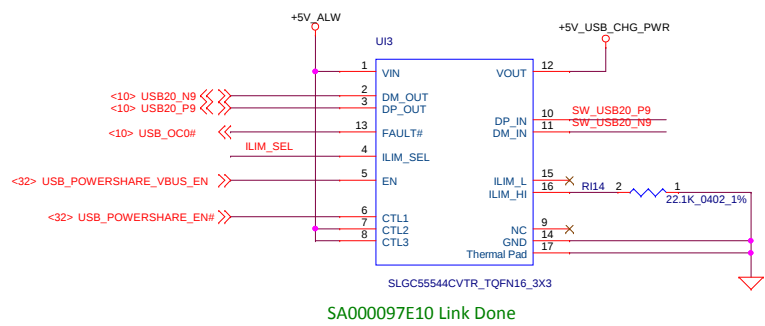
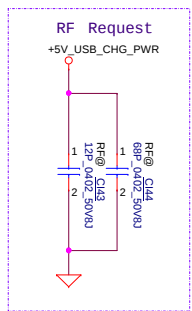
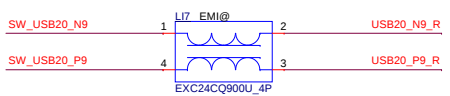
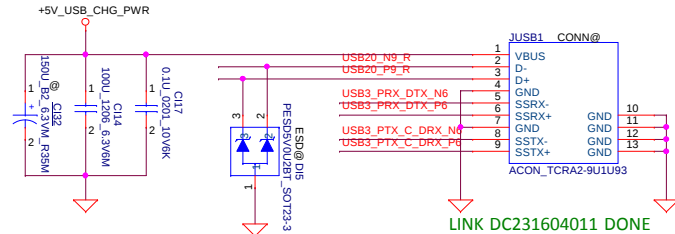
M2 2280 Socket

LA-F322P

2.0

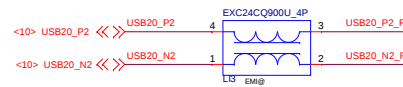
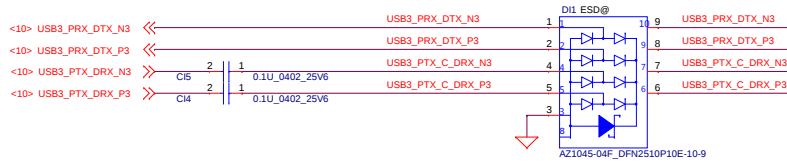
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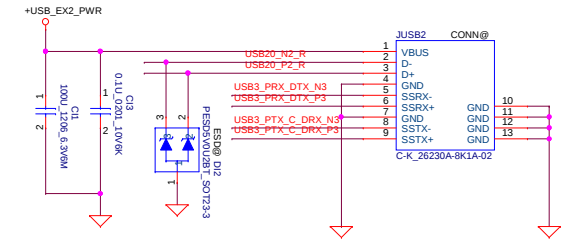
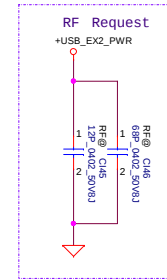


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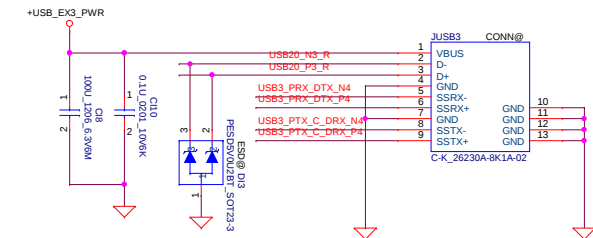
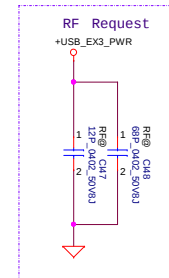
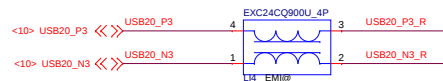
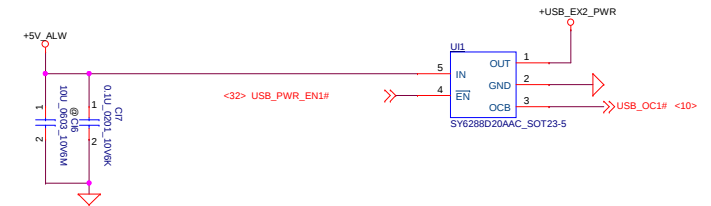
For Breckenridge 14&15/Steamboat 14



DfB request:
main SM070003200 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

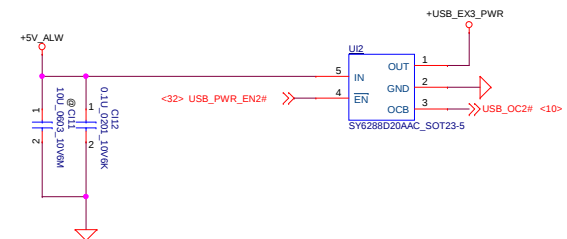


Link DC231604112(Temp) DONE



12" not support

Link DC231604112(Temp) DONE

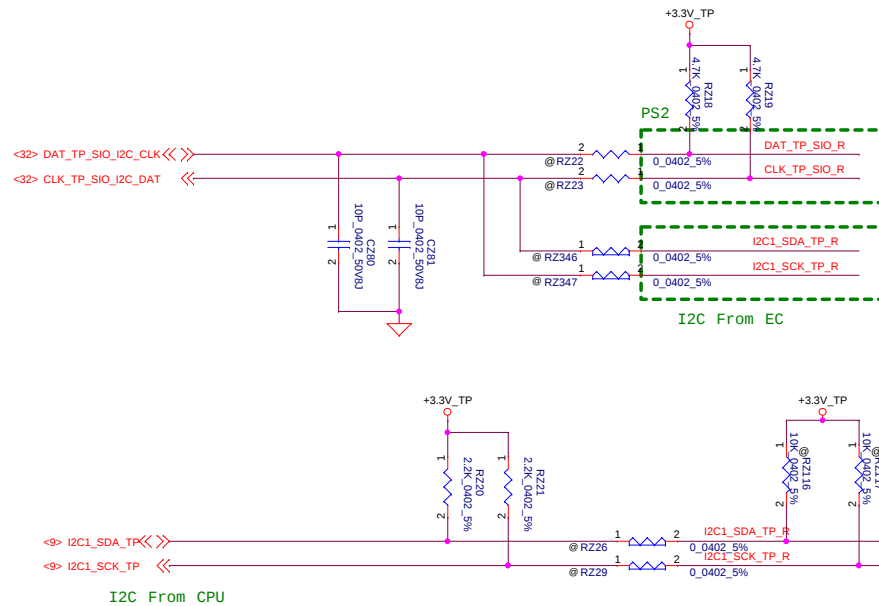


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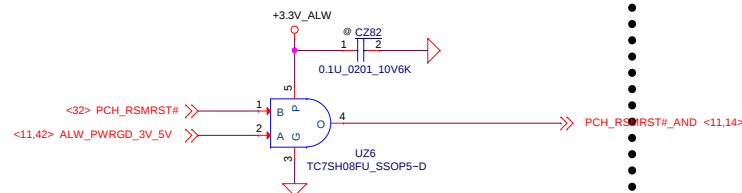
Compal Electronics, Inc.	
JUSB2&JUSB3	
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Touch Pad

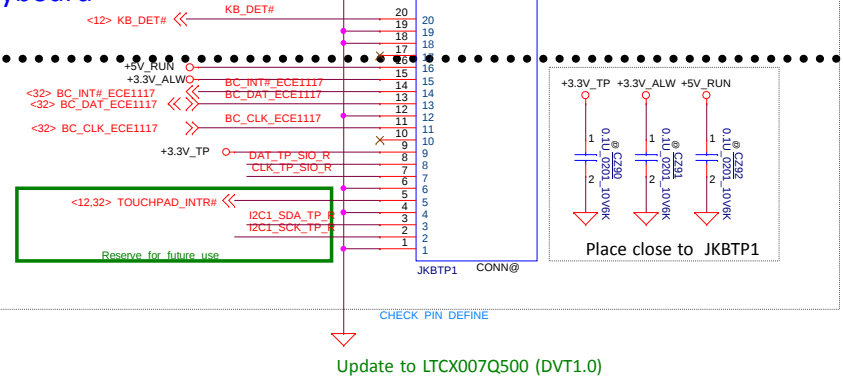


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

RSMRST circuit



Keyboard



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Place C294 near UZ1.

Hall sensor: 5A00009EM00
(MAX height is 1.45mm)



LED Circuit Control Table		
	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



<32,35> BAT2_LED# >>>

<32> BAT1_LED# >>>

LED P/N change to SC5000FL00 from SC5000BA00

Breath LED

Q27B
DMN560BLDW-7, SOT363-6

BREATH_LED#_Q

R232
330_0402_5%

BREATH_WHITE_LED_SNFF#

LED3
LTW-C180DC-C WHITE

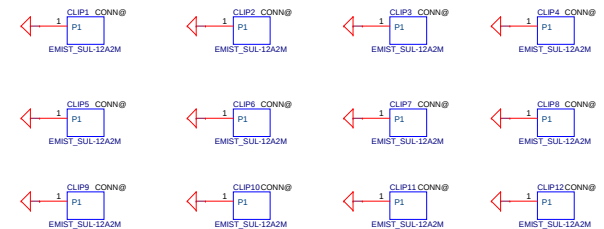
+5V_ALW

Place LED3 close to SW3

GND

MASK_BASE_LED5#

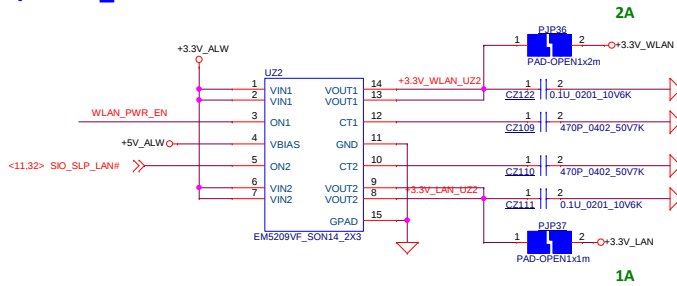
Pin 1-8 connection diagram for the ACES_50209-0060N-P01 module. The diagram shows connections for +5V_ALW, BATT_YELLOW#, BATT_WHITE#, <33,39> LID_GL#, and +3.3V_ALW#. The module pins are numbered 1 to 8, with GND and GND pins at the bottom. The module is labeled ACES_50209-0060N-P01.



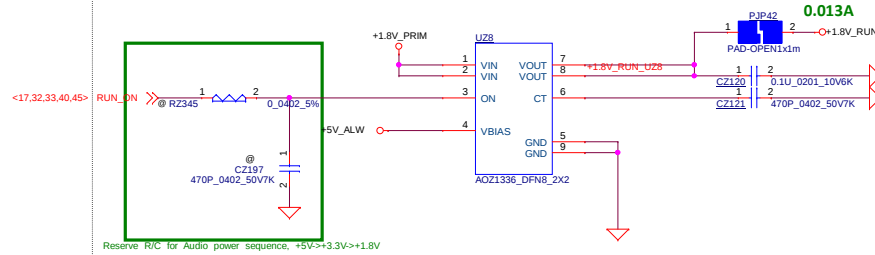
	Compal Electronics, Inc.		
	Title		
	PAD, LED		
	Size	Document Number	Rev
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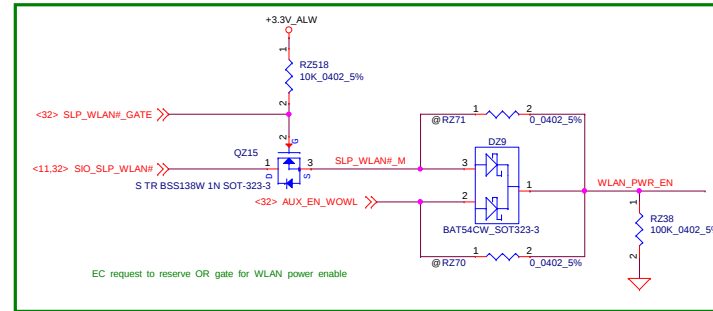
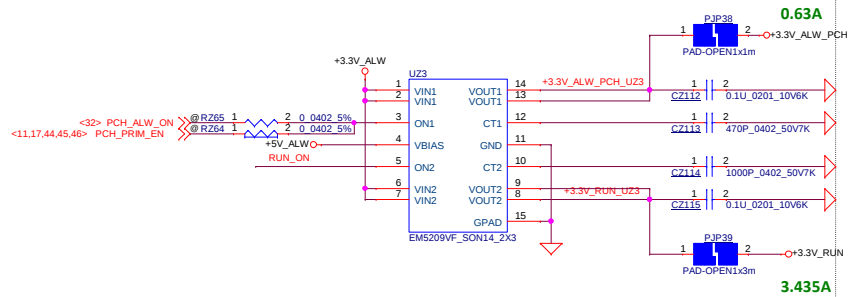
+3.3V_WLAN/+3.3V_LAN source



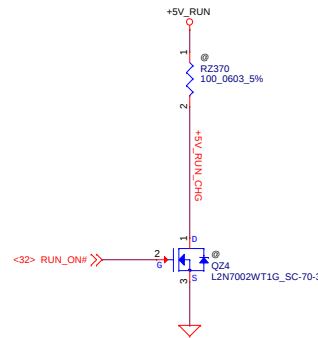
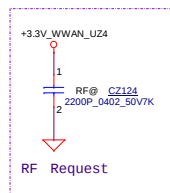
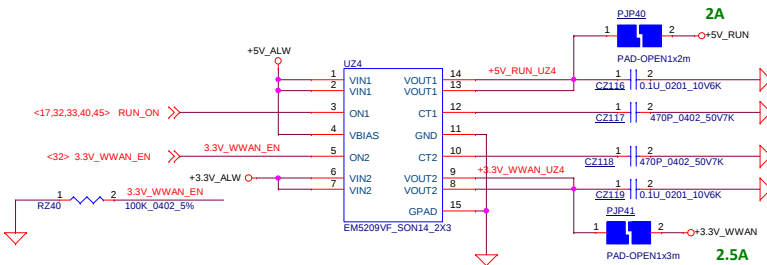
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source



Reserve for S3 no power issue (+5V_RUN discharge circuit)

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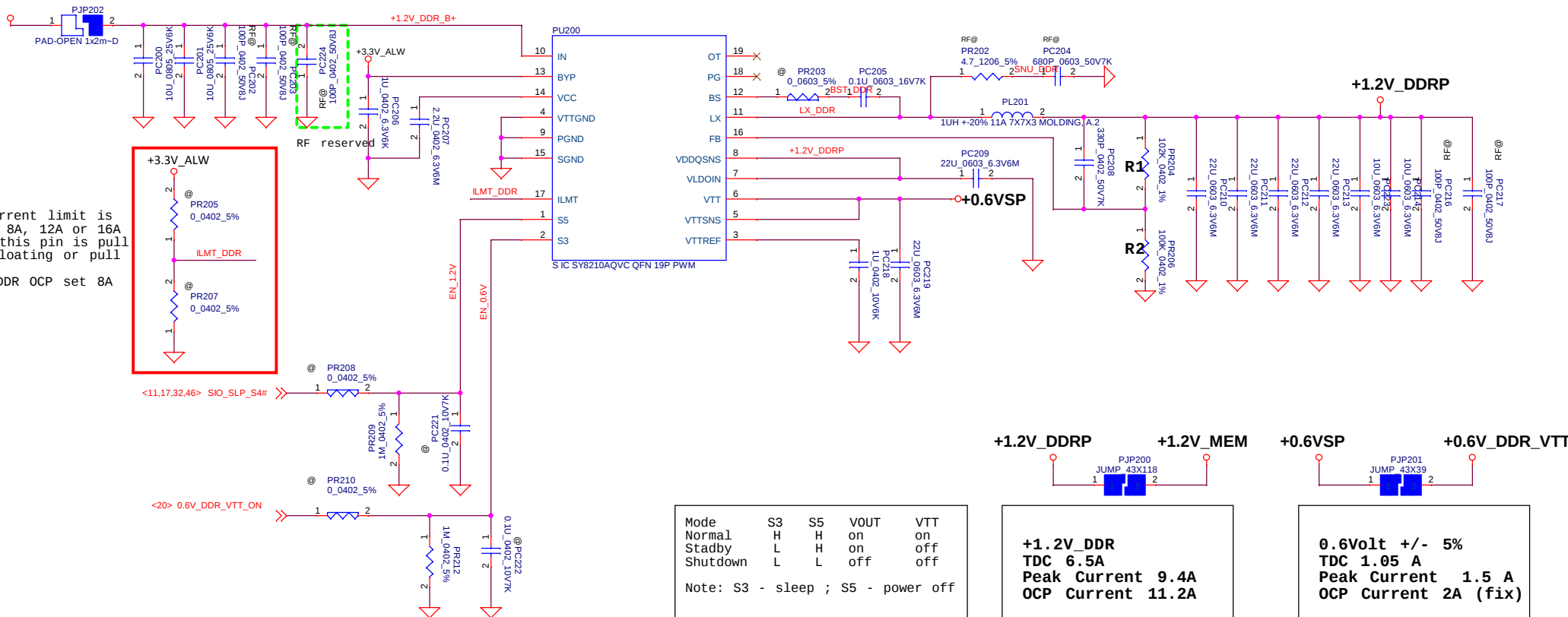
Power control

LA-F322P

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+PWR_SRC



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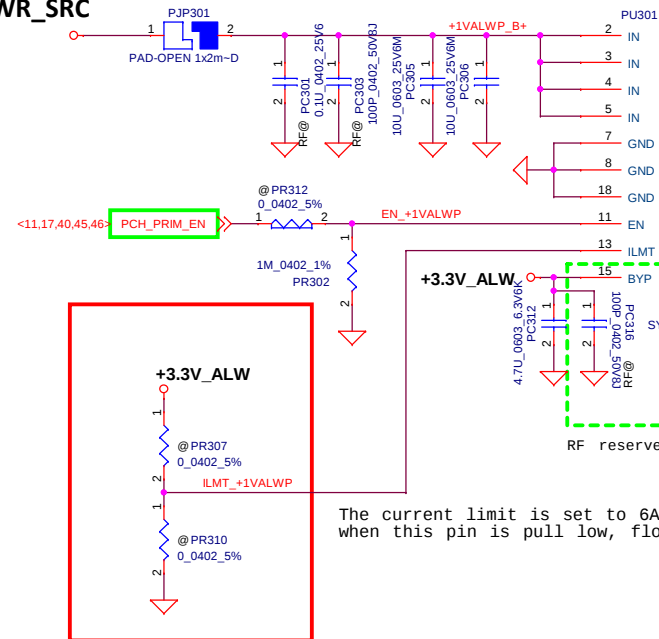


Compal Electronics, Inc.

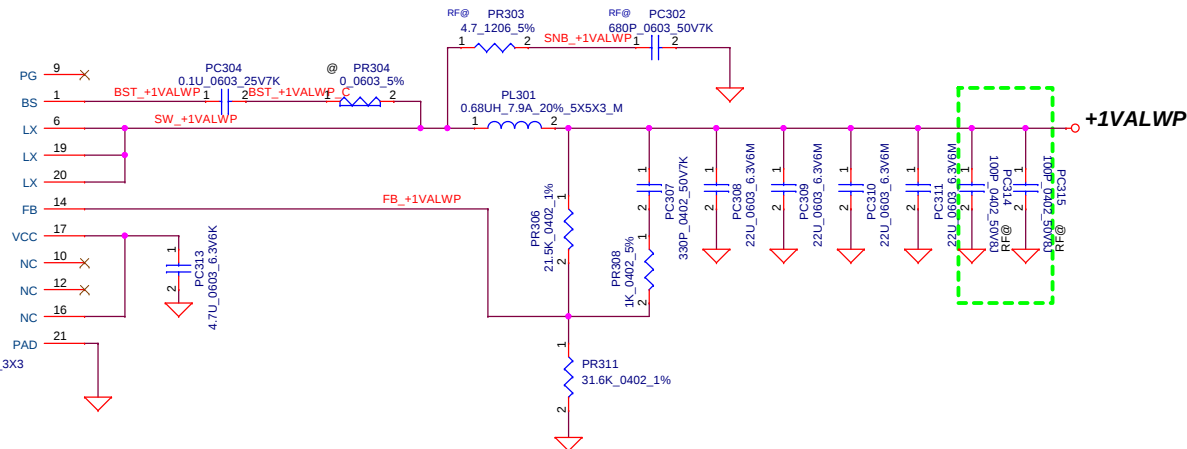
Title		
+1.2V_MEN/+0.6V_DDR_VTT		
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+PWR_SRC



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

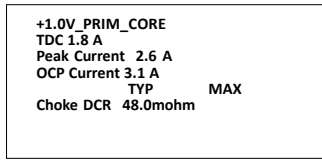
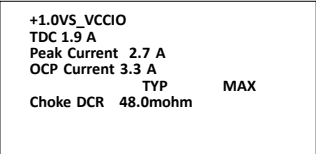


+1.0V_PRIM
TDC 4.9A
Peak Current 7.1 A
OCP Current 8.6A
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

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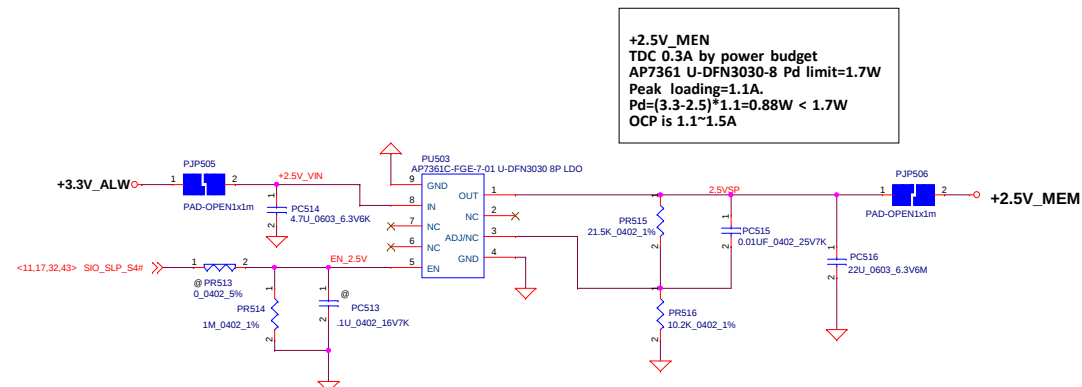
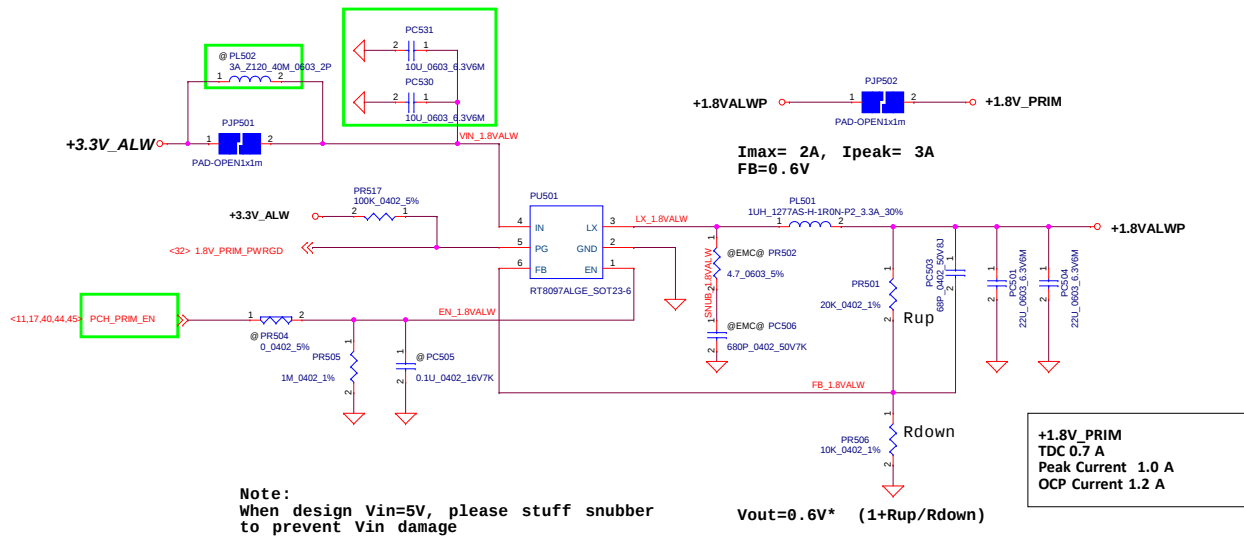
Compal Electronics, Inc.		
Title		
+1VALWP		
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	Title			
	+1VS VCCIOP/+1.0V PRIM COREP			
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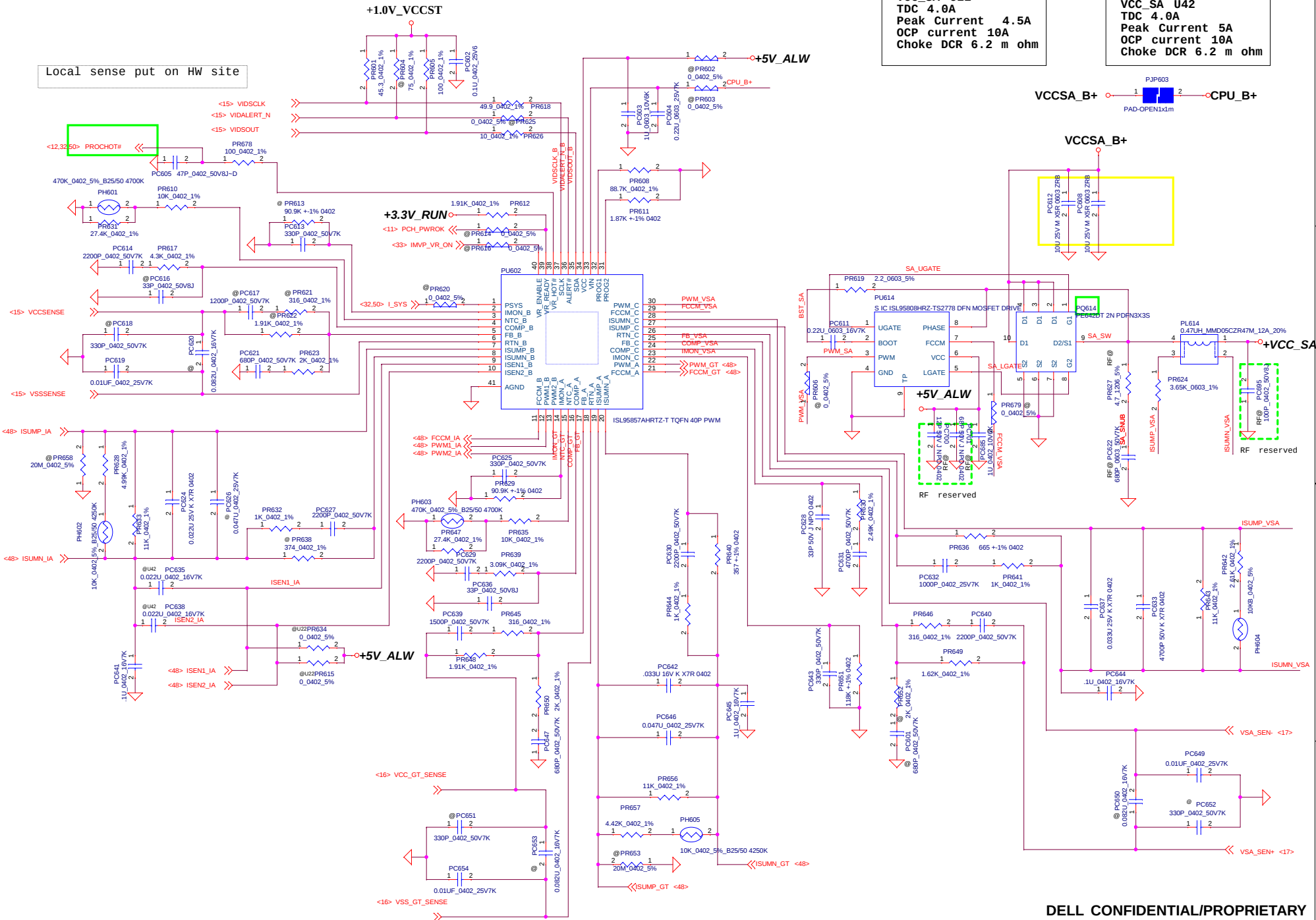


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Compal Electronics, Inc.		
+1.8VALWP/+1.5VSP		
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Local sense put on HW site



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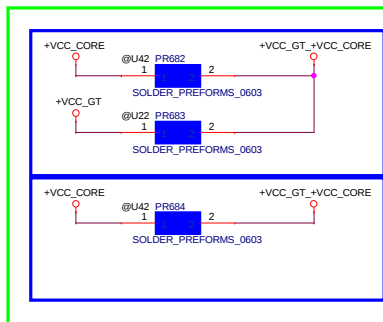
PWR_VCORE_ISL95857

Size Document Number LA-F322P Rev 2.0

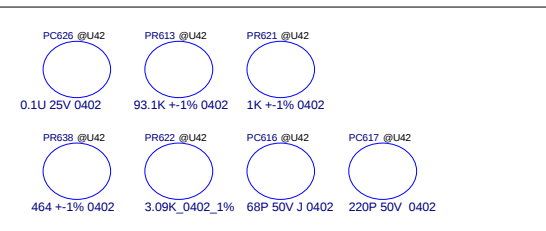
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VCC_core (U42)
TDC 42A
Peak Current 64A
OCP current 76.8A
Choke DCR 0.9 +-5% ohm



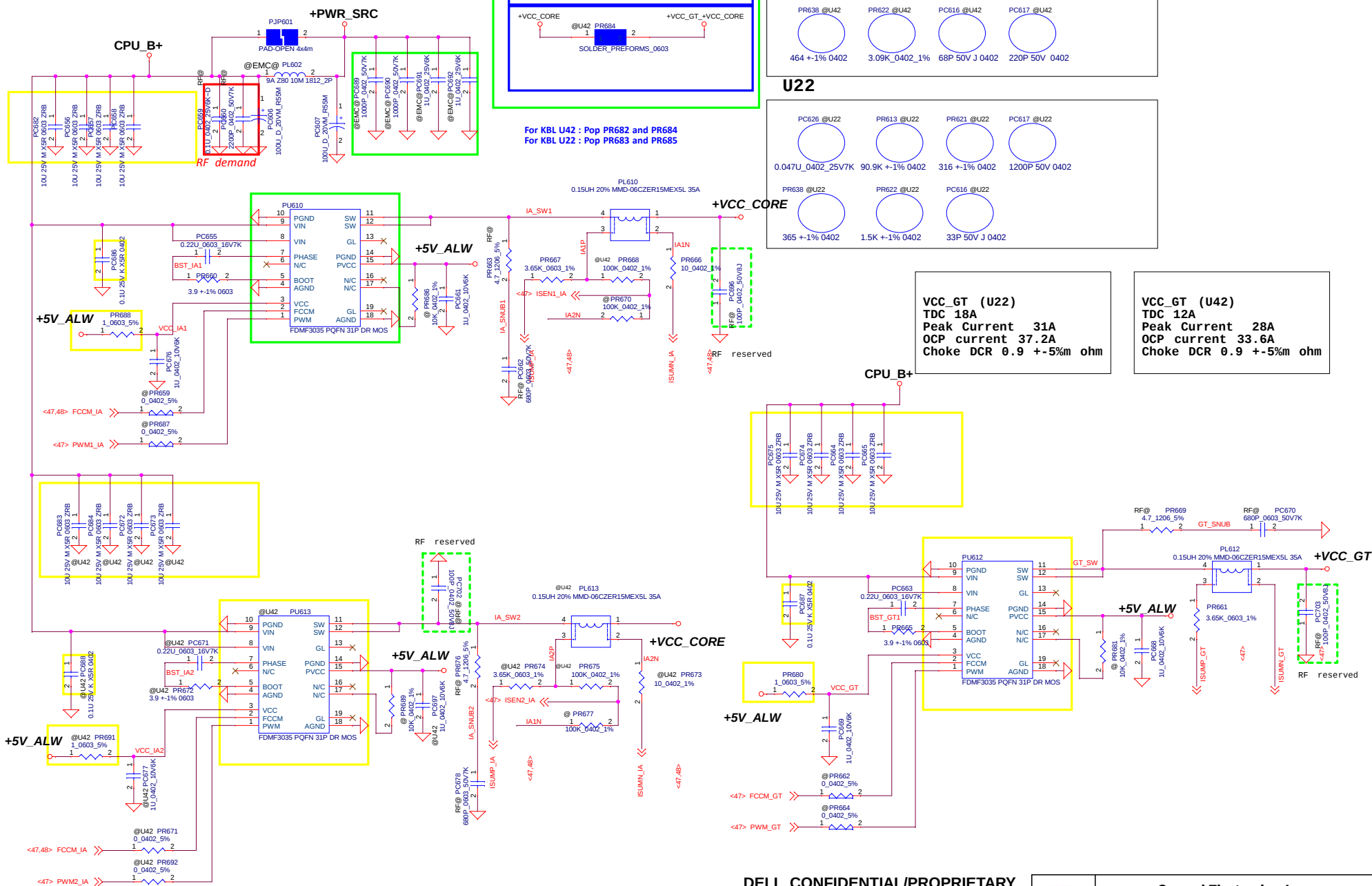
For KBL U42 : Pop PR682 and PR684
For KBL U22 : Pop PR683 and PR685



ORE

VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-5% ohm

VCC_GT (U42)
TDC 12A
Peak Current 28A
OCP current 33.6A
Choke DCR 0.9 +-5% ohm



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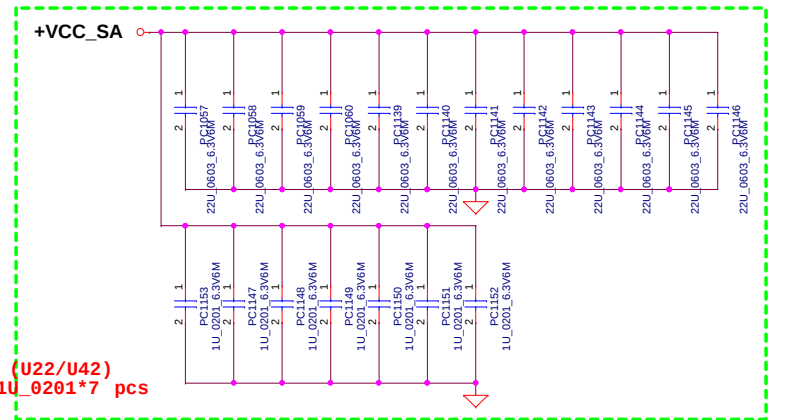
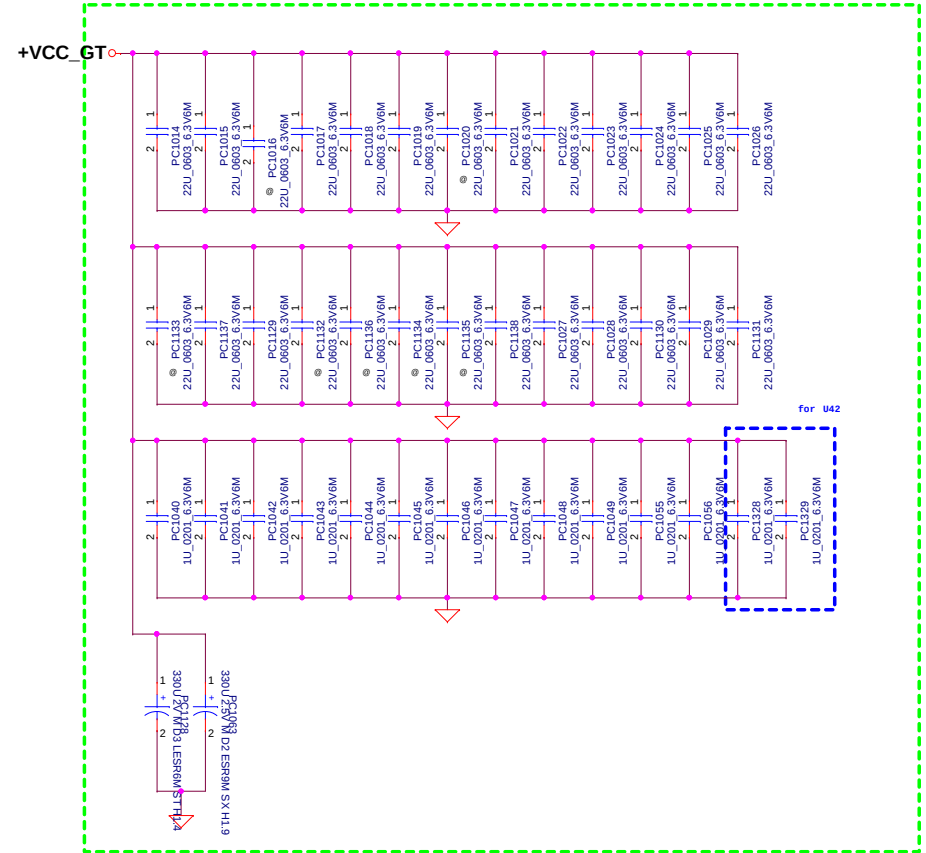
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Size	Document Number
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	Rev 2.0
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VCC_GT Place on CPU (U22/U42)
22U_0603 * 19 pcs +1U_0201*14 pcs
+330u_D3*2 pcs

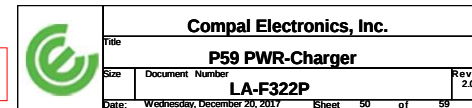


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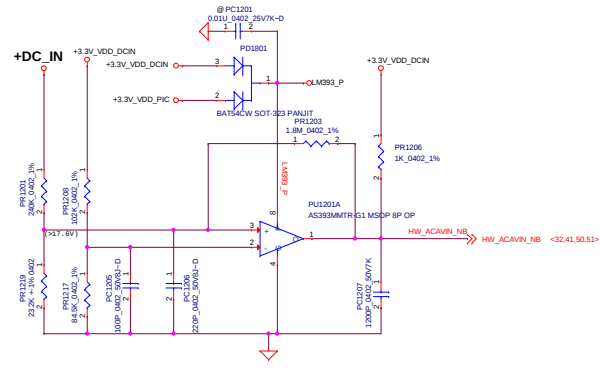


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Title			
PROCESSOR DECOUPLING			
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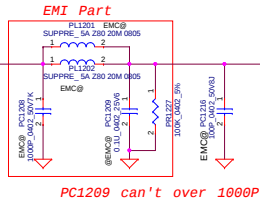


DCIN_AC_Detector

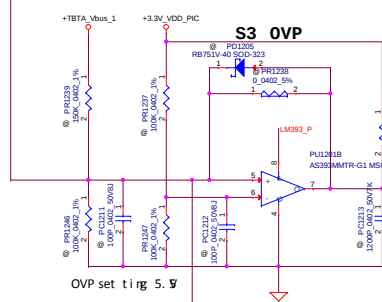


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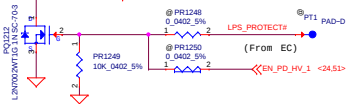
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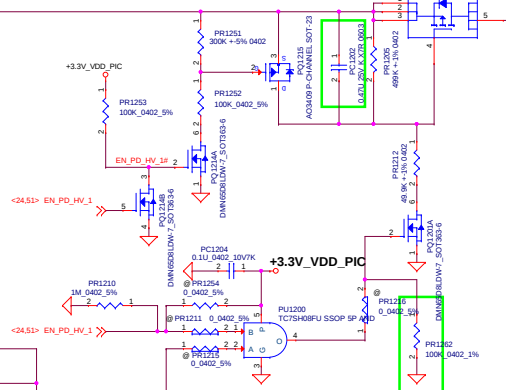
PC1209 can't over 1000P



OVP set ting 5.9



+AC_IN



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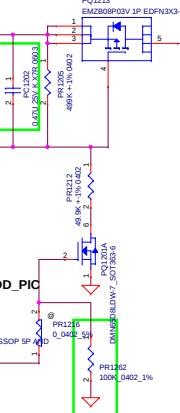
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S4



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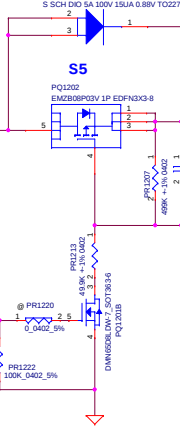
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+VBUS_DC_SS



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TypeC_PD			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	TI DrMOS (CSD97396) material shortage	PU610/ PU612/ PU613 change to FDMF3035 (SA00000AXX00)	X01
2	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	Acoustic solution	Pop 2pcs 100uf (PC606 ,PC607)	X01
3	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	Acoustic solution	VCORE input change to low noise MLCC (SE00000X210)	X01
4	59	Charger	2017 06/08	Compal	Acoustic solution	charger output emove 10uf*4 (PC916,PC917,PC918,PC919,PC920) and replace 1pcs 15uf_POSCAP(PC921)	X01
5	51,56 57,59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Compal	EMI request	Remove PC130,PC134,PC135,PC136,PC137,PC138,PC139,PC140 Remove PC689,PC690,PC691,PC692 Pop PL901 ,depop PJP901 Remove PC956,PC957,PC958,PC959	X01
6	51,56 57,59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Compal	RF request	reservePC12,PC141,PC142,CP143,PC224,PC314,PC315,PC316,PC693, PC694,PC695,PC696,PC697,PC706,PC960,PC961,PC962	X01
7	59	charger	2017 08/04	Compal	for PU901 burn out issue	New add TVS Diode PD906 before PL901	X02
8	59	charger	2017 08/04	Compal	intersil FAE suggest	Change PR015,PR909,PR910,PR937,PR938 from 0402 to 0603.	X02
9	60	Type-C PD selector	2017 08/04	Compal	EMC request Type C bead change to 80 ohm	Type-C PD Bead EOL ,so change PL1201/PL1202 Bead to 80 ohm bead, CPW:SM01000P200-->SM01000U200 (2nd) CPW:SM01000P200-->SM01000U400 (main)	X02
10	510	charger	2017 08/04	Compal	intersil FAE suggest	For ISL9538 Pays resistance change value 1.UMA R-U42 UMA change to 11.0K 2.UMA U22 UMA keep use 12.7K	X02
11				Compal			
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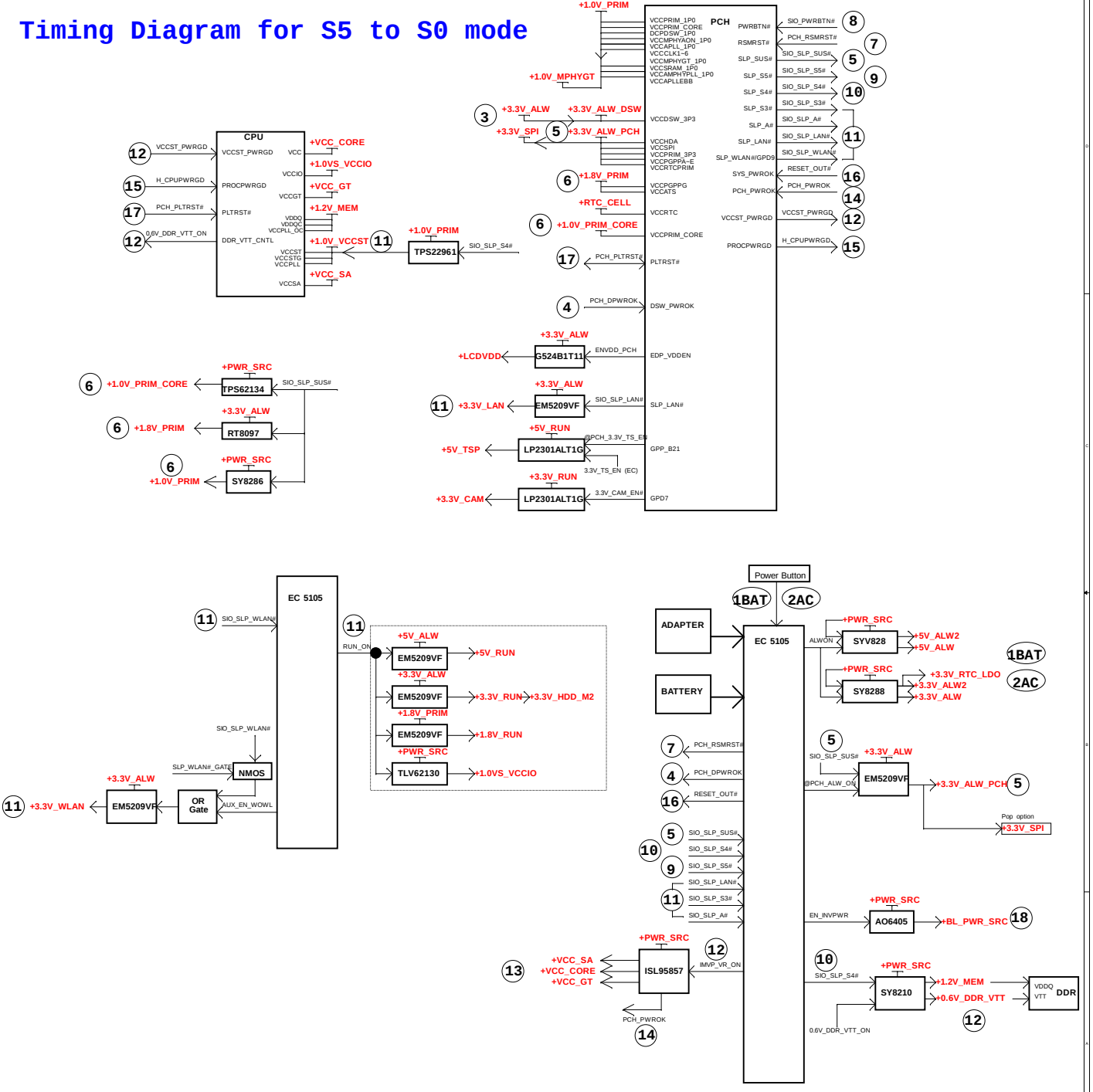
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Timing Diagram for S5 to S0 mode



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A	1	8	CPU (3/14)	2017/03/21	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
	2	8	CPU (3/14)	2017/03/21	ME	JSPI1 connector change vendor	Change JSPI1 to SP010022Q00	0.1(X00)
	3	11	CPU (6/14)	2017/03/21	EE	KBL-R U42 X'tal	Add RC415~RC420,CC334,CC335,YC3	0.1(X00)
	4	13	CPU (8/14)	2017/03/21	EE	KBL-R CRB schematic	Add RC436 0ohm to GND	0.1(X00)
C	5	14	CPU (9/14)	2017/03/21	ME	JXDP1 connector change vendor	Change JXDP1 to SP01001VB00	0.1(X00)
	6	16	CPU (11/14)	2017/03/21	EE	Follow KBL-R U42 Processor Line BGA1356_Ballout_Rev1p0	Reserve RC437, RC438	0.1(X00)
	7	18	CPU (13/14)	2017/03/21	EE	RTC Power Gate Circuit for +3.3V_DSW	Add RC431~RC433, RC439, RC440, QC6, QC7	0.1(X00)
	8	33	EC MEC5105	2017/03/21	EE	RTC Power Gate Circuit for RTCRST	Add QE14~QE17, RE540~RE546, RE551, CE63, RC441, RC442, DC1, DC2, RC445	0.1(X00)
	9	34	EC MEC5105 Support	2017/03/21	EE	Remove IO expander	Remove UE2 relating circuit	0.1(X00)
	10	28	eDP CONN & Touch screen	2017/03/21	ESD	ESD request	Remove DV7, DV8	0.1(X00)
	11	35	USH & TPM	2017/03/21	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
	12	31	NGFF Card	2017/03/21	RF	RF request to align w/ BR MLK	LI8, LI9 change to SM070003Z00, LI16, LI17 change to SM070003V00	0.1(X00)
	13	33	EC MEC5105	2017/03/21	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
	14	All	All	2017/03/21	EE	Port map change	JUSB1 change to USB30_port6 and USB20_port9 USB20_port1 BOM option to Type-C(PD UT5) Delete PS8338 and WIGIG circuit and connect DDI2 to UT1 (Add RC446~RC448 for CPU_DP2_HPD/CPU_DP2_AUXP/CPU_DP2_AUXN)	0.1(X00)
B	15	27	eDP CONN & Touch screen	2017/03/21	EE	I2C touch screen for SB14 only	Change JTS1 to 10pin and add TS_I2C_SDA,TS_I2C_SCL,TS_INT#	0.1(X00)
	16	24	[Type C]PD Controller TI	2017/03/28	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
	17	33	EC MEC5105 Support	2017/03/28	EE	Panel ID define change	RE300 change to 33K ohm	0.1(X00)
	18	34	USH & TPM	2017/03/28	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
	19	34	USH & TPM	2017/03/28	EE	Prevent Contactless_det# backdrive	Add DZ8	0.1(X00)
	20	26	[Type C]USB3.0 CONN	2017/03/28	ESD	ESD request	Change DT7, DT8, DT11, DT12 to DT39 Change DT15, DT16, DT19, DT20 to DT40	0.1(X00)
	21	11	CPU (6/14)	2017/03/28	EE	RTC Power Gate Circuit option	Add RC441, RC442, DC1, DC2, RC445	0.1(X00)

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22	A11	A11	2017/03/28	EE	GPIO map change	PCH_RSMRST# GPIO204 -> USH_PWR_STATE# (delete RE363) PORT80_DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD_I03 -> VBUS1_ECOK SHD_I01 -> SATA_LED_EN ENVDD_PCH -> DCIN2_EN SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBCLK Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 -> RESET_IN# 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_I00 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option	0.1(X00)
23	27	eDP CONN & Touch screen	2017/03/30	EE	3MM_CAM detection	Add 3MM_CAM_DET# GPIO and add PU RV325	0.1(X00)
24	A11	A11	2017/03/30	EE	GPIO map change	PANEL_ID -> SYSTEM_ID SHD_I01 -> SATA_LED_EN -> MASK_SATA_LED# EXPANDER_GPU_SMDAT -> VCCDSW_EN_GPIO and delete RE524 EXPANDER_GPU_SMCLK -> free and delete RE525 THERMATRIP1# -> THERMATRIP1# THERMATRIP2# -> THERMATRIP2# SIO_EXT_SCI#_EC -> free and delete RE341 FAN1_TACH -> TACH_FAN1 LCD_TST -> free WWAN_RADIO_DIS# -> LCD_TST EC_GPIO123 (UE1.F12) -> WWAN_RADIO_DIS# DCIN3_EN -> EC_GPIO202 (UE1.J6) (SBMLK 12/13 only) FAN1_PWM -> PWM_FAN1 PS_ID -> free SHD_CLK -> PS_ID and delete RE374 AUD_NB_MUTE# -> NB_MUTE#	0.1(X00)
25	A11	A11	2017/03/30	EE	GPIO map change	UE1.B1 -> add net name 3.3V_ALW2 and depop RE57 (Microchip suggest) RESET_IN# -> Remove RE361 (Microchip suggest) SLOT2_CONFIG_3 -> NGFF_CONFIG_3 ME_FWP -> ME_FWP_PCH ME_FW_EC -> ME_FWP HW_GPS_DISABLE# -> GPS_DISABLE# VGA_ID -> BEEP H_PROCHOT# -> PROCHOT# USB_PWR_SHR_VBUS_EN -> USB_POWERSHARE_VBUS_EN USB_PWR_SHR_LFT_EN# -> USB_POWERSHARE_EN# SIO_EXT_SMI#_EC -> free and delete RE338 CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 SHD_I02 -> 1.8V_PRIM_PWRGD and delete RE360 BEEP -> VGA_IDENTIFY (rename from VGA_ID) SHD_CS# -> PCH_RSMRST# and delete RE364 SLOT2_CONFIG_0 -> NGFF_CONFIG_0 SLOT2_CONFIG_1 -> NGFF_CONFIG_1 SLOT2_CONFIG_2 -> NGFF_CONFIG_2 ACAV_IN_NB -> HW_ACAVIN_NB LID_CL#_NB -> LID_CL_SIO# SYS_PWR0K->reserved 0ohm RE548 and add netname to RESET_OUT	0.1(X00)

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26	All	All	2017/03/30	EE	Port map change	NGFF3 (SSD 4 Lane)*add PCIE port 9 and port 10 LOM change to PCIE port 4	0.1(X00)
27	11 32	CPU (6/14) EC MEC5105	2017/04/05	EE	Intel PDG for DSx and NonDSx	Add RC443, RC444 for SUSACK#, ME_SUS_PWR_ACK Add BOM structure DS3@ for RE349 and RE536	0.1(X00)
28	17 40	CPU (12/14) Power control	2017/04/05	EE	PCH_PRIM_EN net name change	Change net name from SIO_SLP_SUS# to PCH_PRIM_EN	0.1(X00)
29	33	EC MEC5105 Support	2017/04/05	EE	Microchip suggest	Change RE71 to 10 ohm	0.1(X00)
30	40	Power control	2017/04/05	EE	+5V_RUN discharge circuit for S3 no power issue	Add QZ4 and RZ370	0.1(X00)
31	9	CPU (4/14)	2017/04/06	EE	RF need to validate Active Steering Antenna for SB14 only	Change JUART1 to SP01002LL00 and add RC434, RC435 for power option	0.1(X00)
32	33	EC MEC5105 Support	2017/04/11	EE	+5V_RUN for FAN	Change DE1 to SC400002J00	0.1(X00)
33	40	Power control	2017/04/14	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9	0.1(X00)
34	33	EC MEC5105 Support	2017/04/14	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1(X00)
35	32	EC MEC5105	2017/04/14	EE	Schmatic align	Add GPU_SMCLK/GPU_SMDAT PU to RPE12	0.1(X00)
36	11	CPU (6/14)	2017/04/14	EE	WIGIG feature remove	Add back RC50 and depop	0.1(X00)
37	31	CodeC ALC3246	2017/04/14	EE	Realtek request	CA54 change back to 10pf and depop	0.1(X00)
38	32 11	EC MEC5105 CPU (6/14)	2017/04/14	EE	RTC power Gate circuit rev.2 (0411)	Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)
39	11	CPU (6/14)	2017/04/14	EE	RTC Power Gate Circuit option (0411)	RC445 change to connect to VCCDSW_EN and pop	0.1(X00)
40	9	CPU (4/14)	2017/04/14	RF	I2C interface for Active Steering Antenna (SB14 only)	Add RC510~RC513, QC4 (1.8v level shift), RC546~RC549	0.1(X00)
41	10 24	CPU (5/14) [Type C]PD Controller TI	2017/04/14	EE	OTG support	Pop RT74, Depop RC337	0.1(X00)
42	13	CPU (8/14)	2017/04/19	EE	KBL-R CRB schematic	Add BOM structure for RC436 U42@	0.1(X00)
43	All	All	2017/04/19	EE	GPIO map change	RC443 BOM structure change to @ GPIO126->GPU_PWR_LEVEL Add RTCRST_ON_R net neme for QE17.2 Add SIO_SLP_SUS#_R net name and PU RE561 SYS_LED_MASK#->LED_MASK# RC27.2->NC for CLKRUN# HDD_DET#->SATAGP0 Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN	0.1(X00)
44	34	USH & TPM	2017/04/19	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1(X00)
45	9	CPU (4/14)	2017/04/19	RF	I2C interface for Active Steering Antenna (SB14 only)	Swap I2C3_SDA and I2C3_SCL	0.1(X00)

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46	32	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->DCIN3_EN Add test point T147 for UE1.M4->GPIO013	0.1(X00)
47	All	All	2017/04/20	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#->UPD1_SMBINT# UPD1_SMBUS_ALERT#->UPD1_SMBINT#_R	0.1(X00)
48	11	CPU (6/14)	2017/04/20	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1(X00)
49	32	EC MEC5105	2017/04/26	EE	GPIO map change	UPD2_ALERT#->UPD2_SMBINT#	0.1(X00)
50	11	CPU (6/14)	2017/05/03	EE	CLKREQ align	Pop RC50 and RC190	0.1(X00)
51	10	CPU (5/14)	2017/05/03	EE	OTG support	RC337 pop and change to 10K ohm	0.1(X00)
52	40	Power control	2017/06/02	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Add SLP_WLAN#_GATE net and RE552 to UE1.K10	0.2(X01)
53	24	[Type C]PD Controller TI	2017/06/02	EE	PD ROM main source change	UT6 change to SA000095R10 (6D)	0.2(X01)
54	11	CPU (6/14)	2017/06/02	EE	Schematic align	Reserve RC551 for SUSACK#_R	0.2(X01)
55	34	USH & TPM	2017/06/02	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM_PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resistors and CZ75 change to 10U	0.2(X01)
56	All	All	2017/06/02	ESD	Main source change	DI1,DI4,DT39,DT40,DI6 change to SC300001Y00 DI2,DI3,DI5 change to SCA00000T00 DA2 change to SCA00001A00 DT4 change to SCA00002Q00	0.2(X01)
57	All	All	2017/06/02	EE	DFX request	DA8, DC1, DC2, DE2, DZ1, DZ2, DZ5-DZ8 footprint change to AZ5125-01HPR7G_SOD523-2	0.2(X01)
58	All	All	2017/06/02	EE	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2(X01)
59	31	CodeC ALC3246	2017/06/12	EE	DFX request	LA13 footprint change to TAI-T_HCB2012KF-121T50_2P	0.2(X01)
60	34	USH & TPM	2017/06/12	RF	RF request	Add CZ76/CZ77 (12pf/68pf) for +3.3V_RUN of UZ12 Add CZ78 (100pf) for +PWR_SRC of JUSH1	0.2(X01)
61	33	EC MEC5105 Support	2017/06/12	EE	Board ID	Change RE79 to 130Kohm (rev. X01)	0.2(X01)
62	9	CPU (4/14)	2017/06/12	RF	ASA for I2C interface	Pop RC549, RC548 and depop RC546, RC547 (14" only)	0.2(X01)
63	9	CPU (4/14)	2017/06/14	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2(X01)
64	40	Power control	2017/06/14	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2(X01)
65	23	TUSB546	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213	0.2(X01)
66	24	[Type C]PD Controller TI	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT405, RT406, RT407, RT417, RT418	0.2(X01)

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67	31	CodeC ALC3246	2017/06/15	RF	RF request	Reserve CA78 for +5V_RUN_AUDIO	0.2(X01)
68	24	[Type C]PD Controller TI	2017/06/21	EE	PD change to rer.C	UT5 change to SA0000AX700	0.2(X01)
69	6	CPU (1/14)	2017/06/21	EE	AUX voltage level shift	Depop RC448, RC447	0.2(X01)
70	23	TUSB546	2017/06/21	EE	TUSB546 DPEQ set to level 5	Depop RT248, RT140 and pop RT303 and RT306	0.2(X01)
71	24	[Type C]PD Controller TI	2017/08/02	EE	PS8743-B1 colay (SA00009E910)	Change RT405-RT407 to 10K	0.3(X02)
72	26	[Type C]USB3.0 CONN	2017/08/02	EE	Schematic align	CT99-CT102 change to 0.01uf (SE00000YH00)	0.3(X02)
73	23	TUSB546	2017/08/02	EE	TUSB546 new version IC	UT9 change to SA00009R720	0.3(X02)
74	27 32 18	eDP CONN EC MEC5105 CPU (13/14)	2017/08/04	EE	Reserve soft start solution	Reserve RV400, CV635 for QV8 Reserve CZ200, RZ380 for QZ1 Reserve CC340 for QC7 Reserve RE565 for QE15	0.3(X02)
75	31	CodeC ALC3246	2017/08/04	RF	RF request to pop CA54 for 2MHz/4MHz noise	Change CA54 to 82pf and pop	0.3(X02)
76	22	HDMI Conn	2017/08/04	EMI/EE	HDMI EA for NonAR only	Change RV35 to 100ohm Change LV37, LV38 to SHI0000M500 Change LV31-LV36 to SHI00003F0L	0.3(X02)
77	27	eDP CONN	2017/08/04	EE	Touch screen support I2C interface	Depop LV27	0.3(X02)
78	33	EC MEC5105 Support	2017/08/07	EE	Board ID	Change RE79 to 62Kohm (rev. X02)	0.3(X02)
79	9	CPU (4/14)	2017/08/09	EE	TPM_PIRQ# GPIO map change	Add RC560 and reserve RC561 to TPM_PIRQ#	0.3(X02)
80	33	EC MEC5105 Support	2017/09/15	EE	Board ID	Change RE79 to 4.2Kohm (rev. A00)	1.0(A00)
81	12	CPU (7/14)	2017/09/15	EE	ME SW depop	Depop RC222, SW1, RC221 change to 0 ohm short pad	1.0(A00)
82	34	USH & TPM	2017/09/15	EE	TPM change to MP version	UZ12 change to SA0000AQ220	1.0(A00)
83	9	CPU (4/14)	2017/09/15	EE	GPIO map change	Depop RC330, RC331	1.0(A00)
84	8	CPU (3/14)	2017/09/15	EE	Add solder mask	Add UC6 -NPM	1.0(A00)
85	A11	A11	2017/09/15	EE	0 ohm change to short pad	0 ohm change to short pad	1.0(A00)
86	A11	A11	2017/09/15	EE	Only support DS3 (0 ohm change to short pad)	Only support DS3 (0 ohm change to short pad)	1.0(A00)
87	23	TUSB546	2017/09/15	EE	TUSB546 DPEQ set to default	Depop RT303, RT306, Pop RT140, RT248	1.0(A00)
88	22 31	HDMI CONN NGFF card	2017/09/18	EE	DFX request	Add LV3, LV6, LV9, LV12 RI27, RI28, RI29, RI30, RI47, RI48, RI49, RI50 -NPM	1.0(A00)

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89	25	[Type C]PD Power	2017/10/03	EE	X1 Code	DT1,DT2,DT3 Change from SC1N4148180 to SC100005500	1.0(A00)
90	24	[Type C] PD Controller TI	2017/11/10	EE	Main vendor EOL	CT74,CT83 Change from SE000000U00 to SE00000QL10	1.0(A00)
91	24	[Type C] PD Controller TI	2017/11/10	EE	PD just change part number	UT5 Change from SA0000AX700 to SA0000BIJ00	1.0(A00)
92	17	CPU (12/14)	2017/12/08	EE	WHEA BSOD Intel request	CC202 change to 22uf for 4+2 CPU, but keep 1uf for 2+2 CPU	1.0(A00)
93	17	CPU (12/14)	2017/12/20	EE	WHEA BSOD	Add CC341 22uf 0603,Depop CC202 22uf 0402	2.0(A01)
94	33	MEC5105 support	2017/12/29	EE	Board ID	Change RE79 to 2Kohm (rev. A01)	2.0(A01)

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