COMPAL CONFIDENTIAL

MODEL NAME : Loki-G 15/17
MB PCB PN : DAA000FC010
PWR/B PCB PN : DA4002L3010
IO/B PCB PN : DA6001XF010

PCB R1
ZZZ
DAA000FC010
PCB@

CPU R1
UC1
SA0000BPJ1L
i5@
UC1
SA0000BPZ1L
i7@

CPU R3
UC1
SA0000BPJ2L
i5@
UC1
SA0000BPZ2L
i7@

Dell/Compal Confidential

Schematic Document

COFFEE LAKE H
N17P-G0/G1
Loki-G 15/17

2018-03-22

REV : 1.0 (A00)

Layout Dell logo

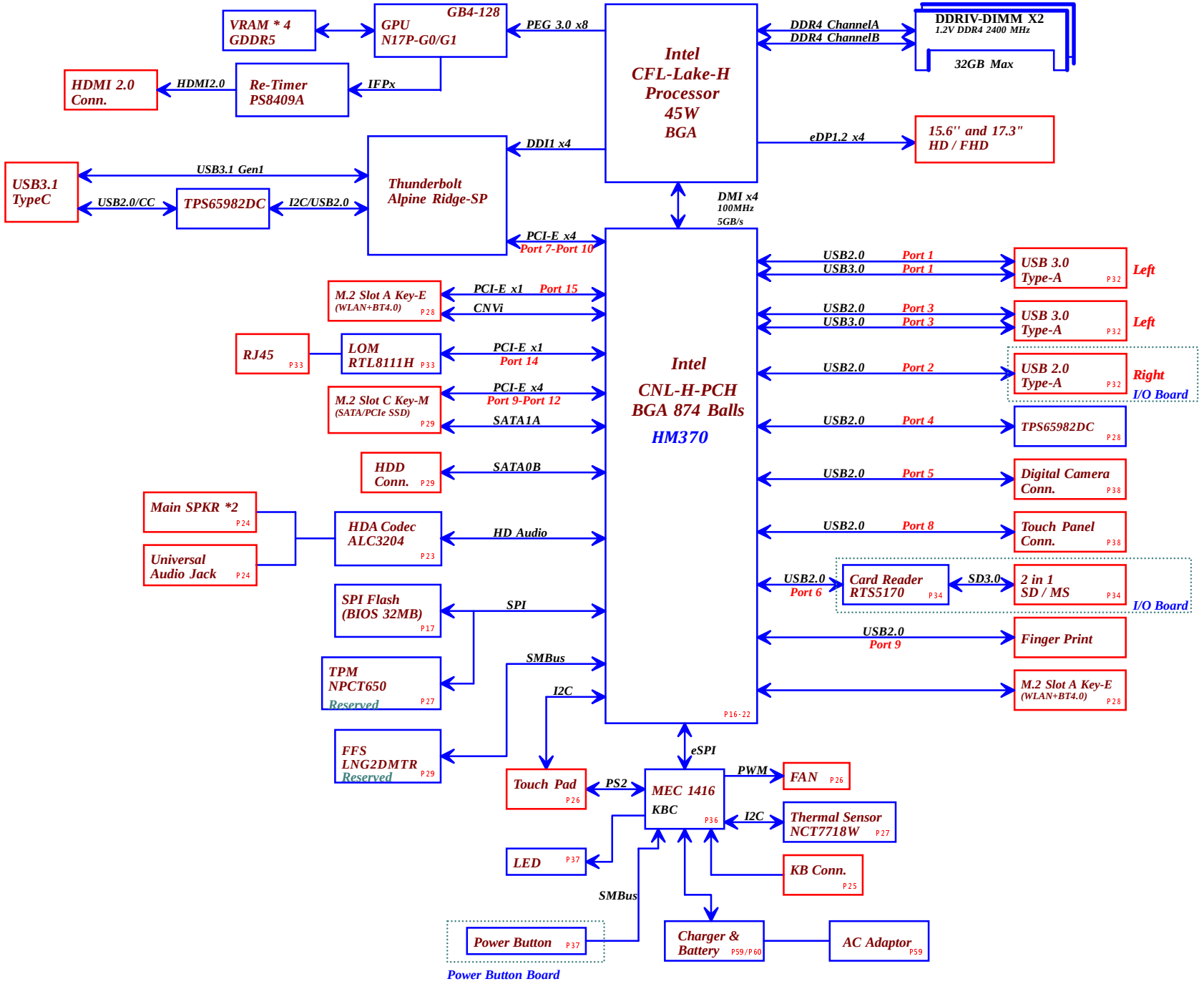
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Cover Page**

Size | Document Number: **LA-F611P** | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 1 of 78



128M*32 x4 =2G
256M*32 x4 =4G

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: Block Diagram

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 2 of 78

Refer Page 26

Board ID	Resistor
X00	10K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

HSIO port Allocation

USB3	DESTINATION
1	USB JUSB1 (Left Side)
2	None
3	USB JUSB3 (Left Side)
4	None
5	None
6	None

USB2	DESTINATION
1	USB JUSB1 (Left Side)
2	USB JUSB2 (I/O)
3	USB JUSB3 (Left Side)
4	TYPEC PD
5	CAMERA
6	Card Reader (I/O)
7	BT & CNVi BRI
8	Touch Screen
9	Finger Print
10	None
11	None
12	None
13	None
14	None

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	None	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	NGFF - NVMe SSD	SATA	DESTINATION
Lane 10		0a	None (NVMe)
Lane 11		1a	NGFF - SSD
Lane 12		0b	HDD
Lane 13	None (HDD)	1b	None (LAM)
Lane 14	LAN	2	None (WLAN)
Lane 15	NGFF - WLAN	3	None
Lane 16	None	4	None
Lane 17	None	5	None
Lane 18	None	6	None
Lane 19	None	7	None
Lane 20	None		
Lane 21	Alpine Ridge - SP		
Lane 22			
Lane 23			
Lane 24			

Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

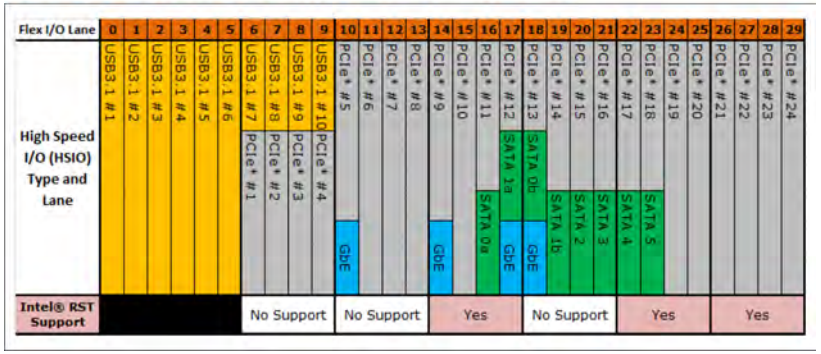
Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI2.0 LSPCON PS175

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	TBT-AR	0	TBT-AR
1	None	1	None
2	None	2	None
3	None	3	None
4	None	4	None
5	None	5	None
6	None	6	None
7	GPU	7	GPU
8	None	8	None
9	NGFF - SSD	9	NVMe
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	LAN	14	LAN
15	WLAN	15	WLAN

13.2.1 Coffee Lake PCH-H

Figure 13-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

Symbol Note :

: means Digital Ground

: means Analog Ground

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Issued Date	2017/01/06	Deciphered Date	2018/01/06

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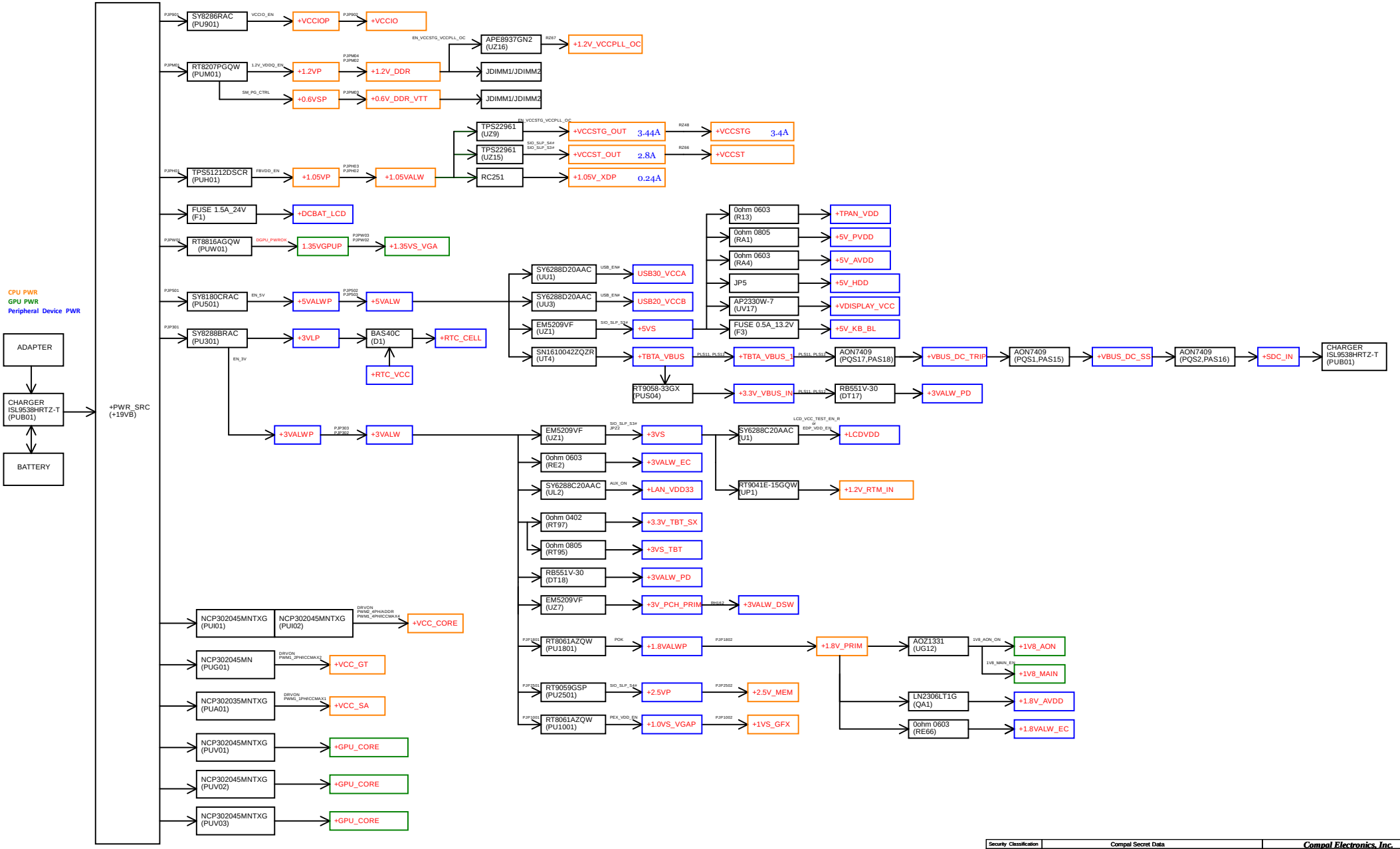
Title: Notes List

Size | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 3 of 78



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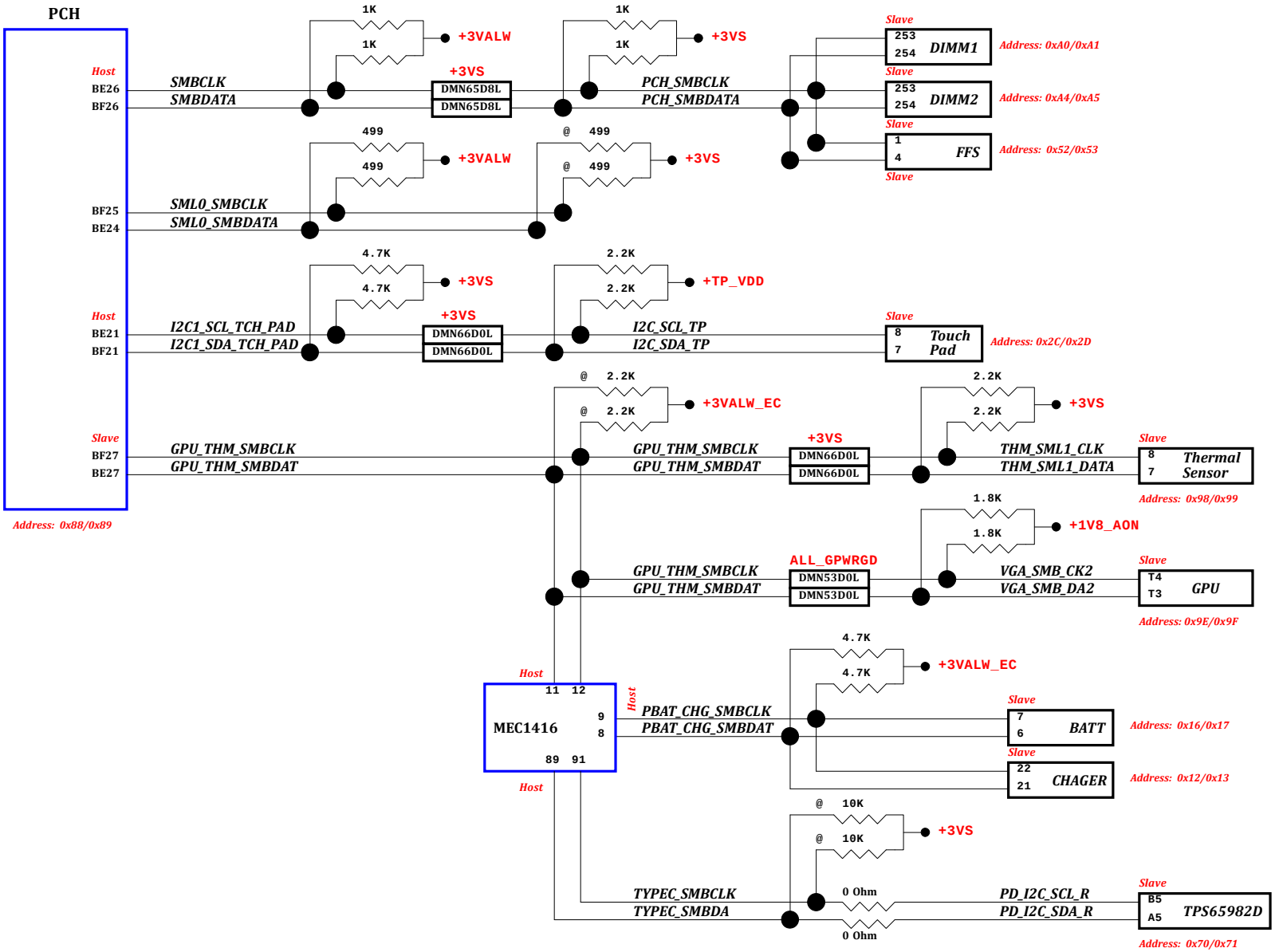
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: Power Rail			
Size	Document Number: LA-F611P		Rev: 0.3
Date: Thursday, March 22, 2018	Sheet 4 of 78		



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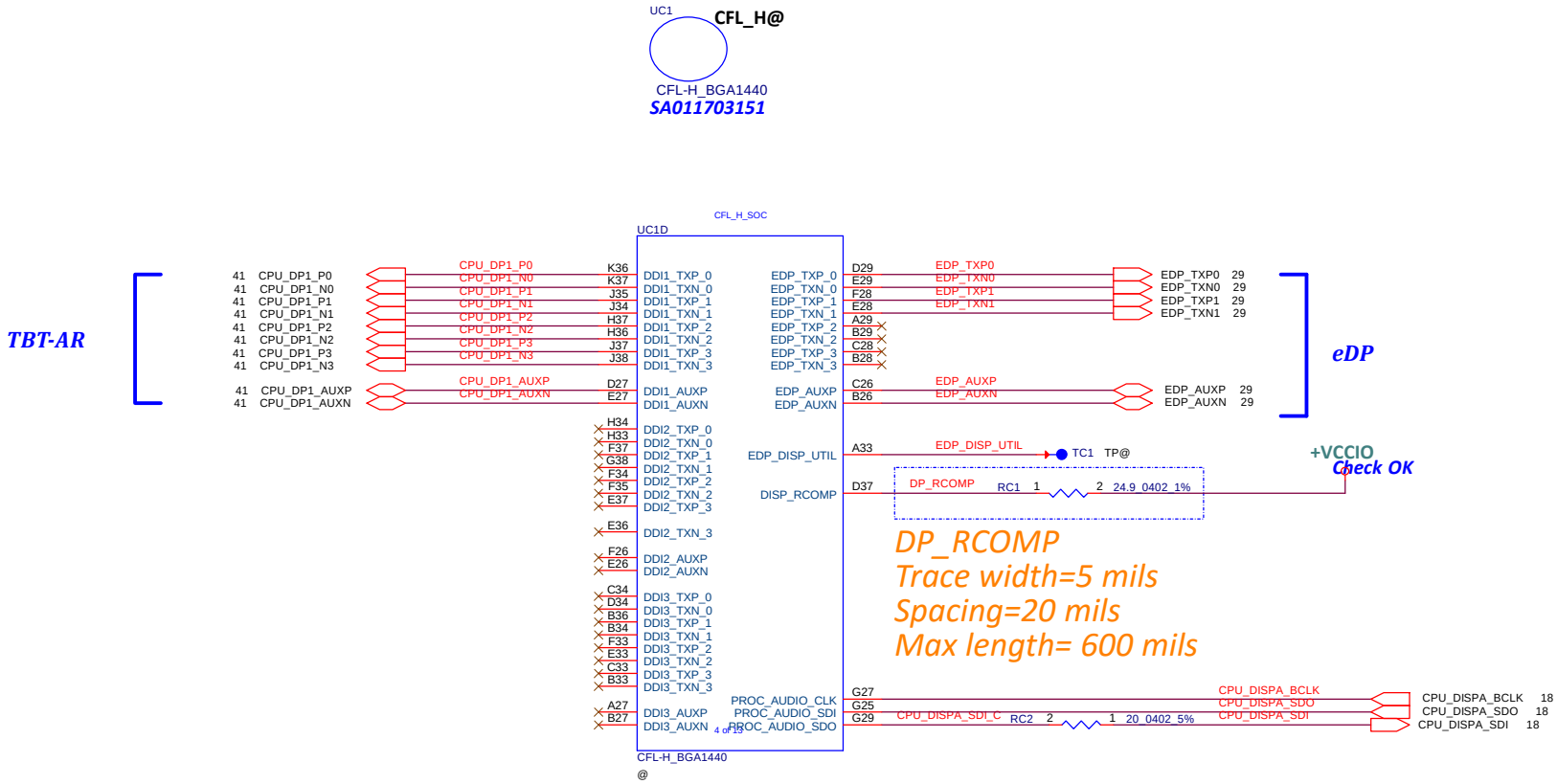
Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
Custom	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 5 of 78

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

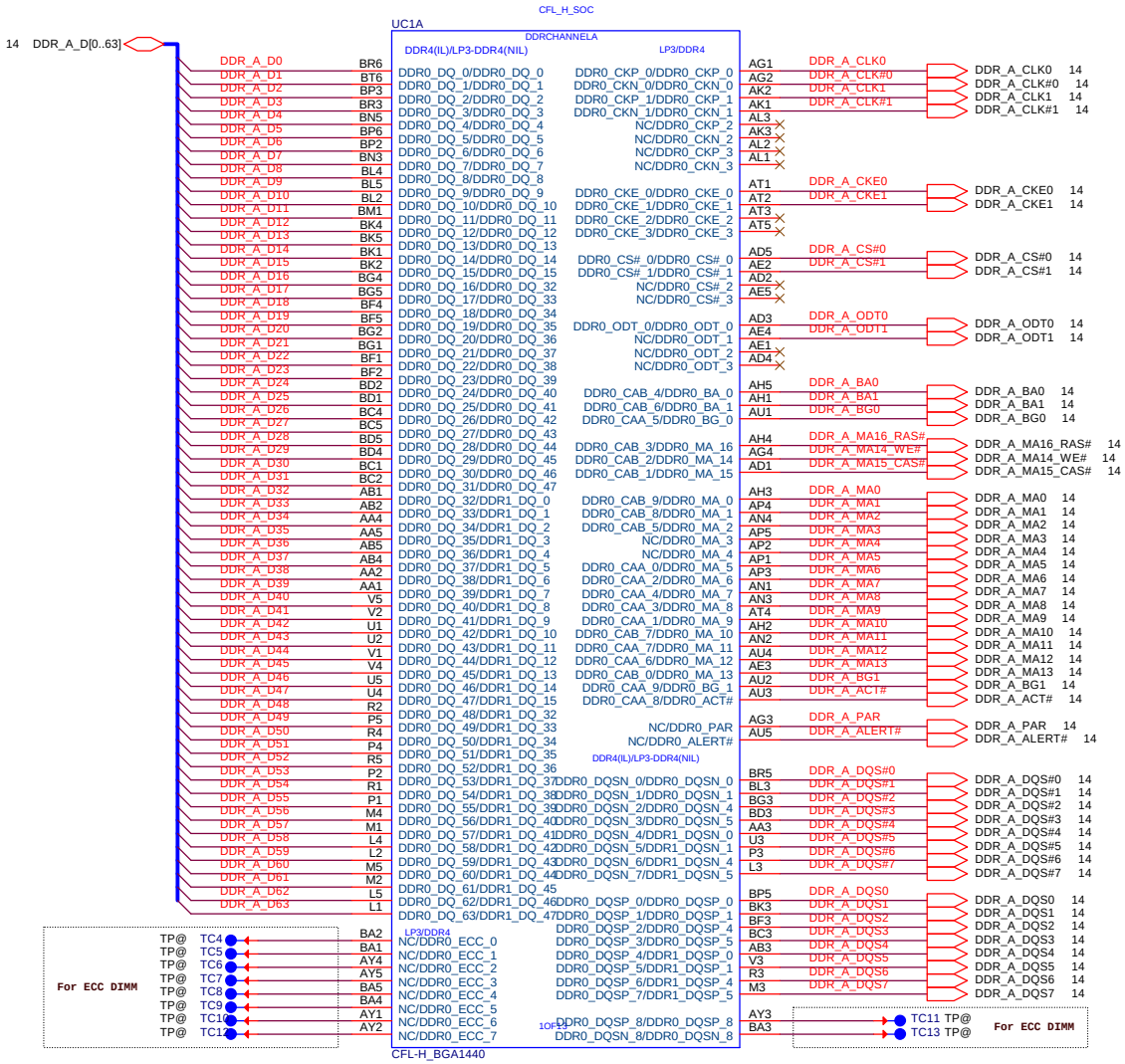
Compal Electronics, Inc.

Title: CFL-H(1/8)DDI/eDP

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 6 of 78

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

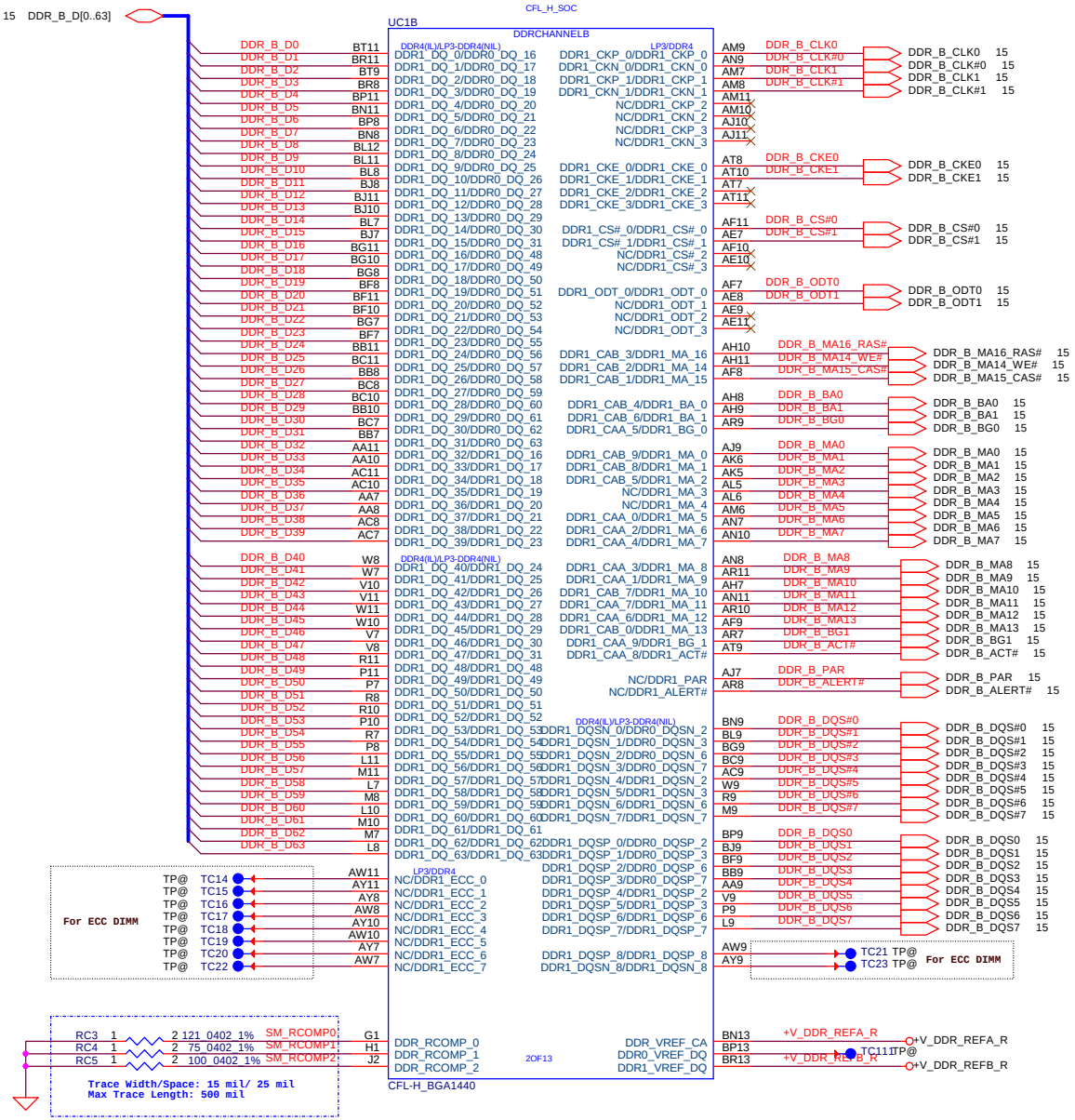
Compal Electronics, Inc.

Title: **CFL-H(2/8)DIMMA**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 7 of 78

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

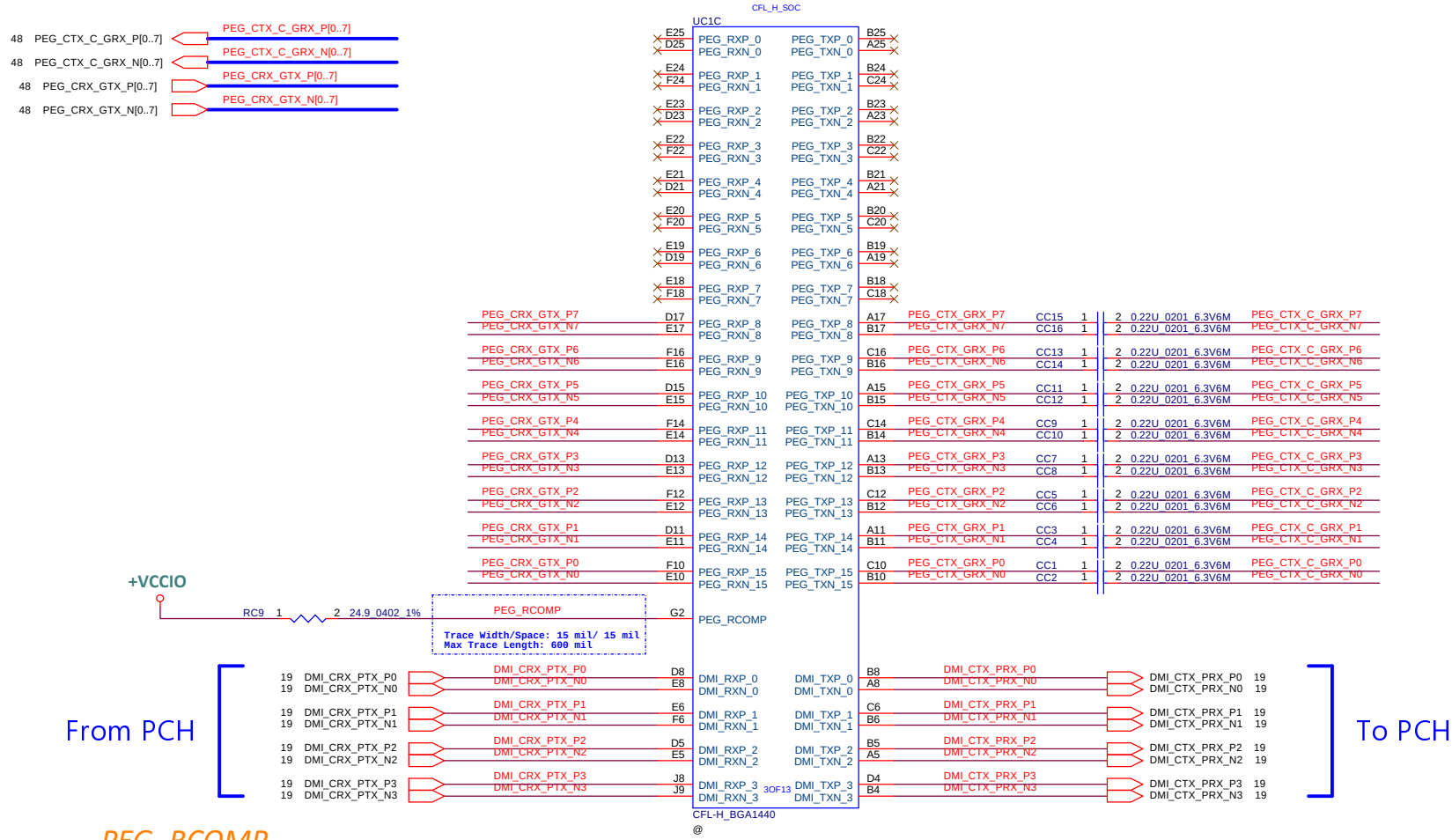
Compal Electronics, Inc.

Title: **CFL-H(3/8)DIMMB**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 8 of 78

Main Func = CPU



PEG_RCOMP
Trace width=15 mils
Spacing=15 mils
Max length= 600 mils

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

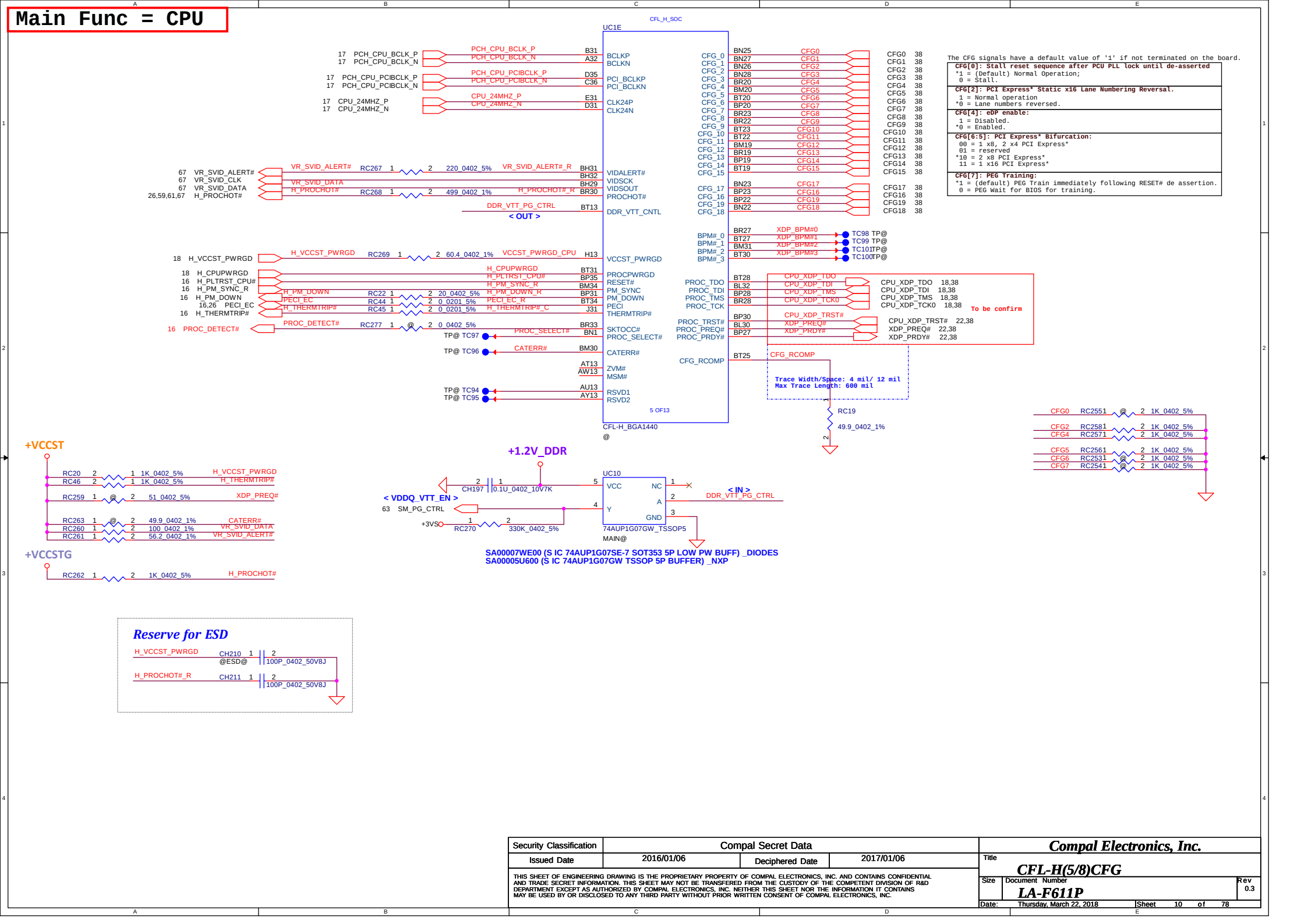
Compal Electronics, Inc.

Title: **CFL-H(4/8)PEG**

Size | Document Number: **LA-F611P** | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 9 of 78

Main Func = CPU



The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
*1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
*0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
*0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
*1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

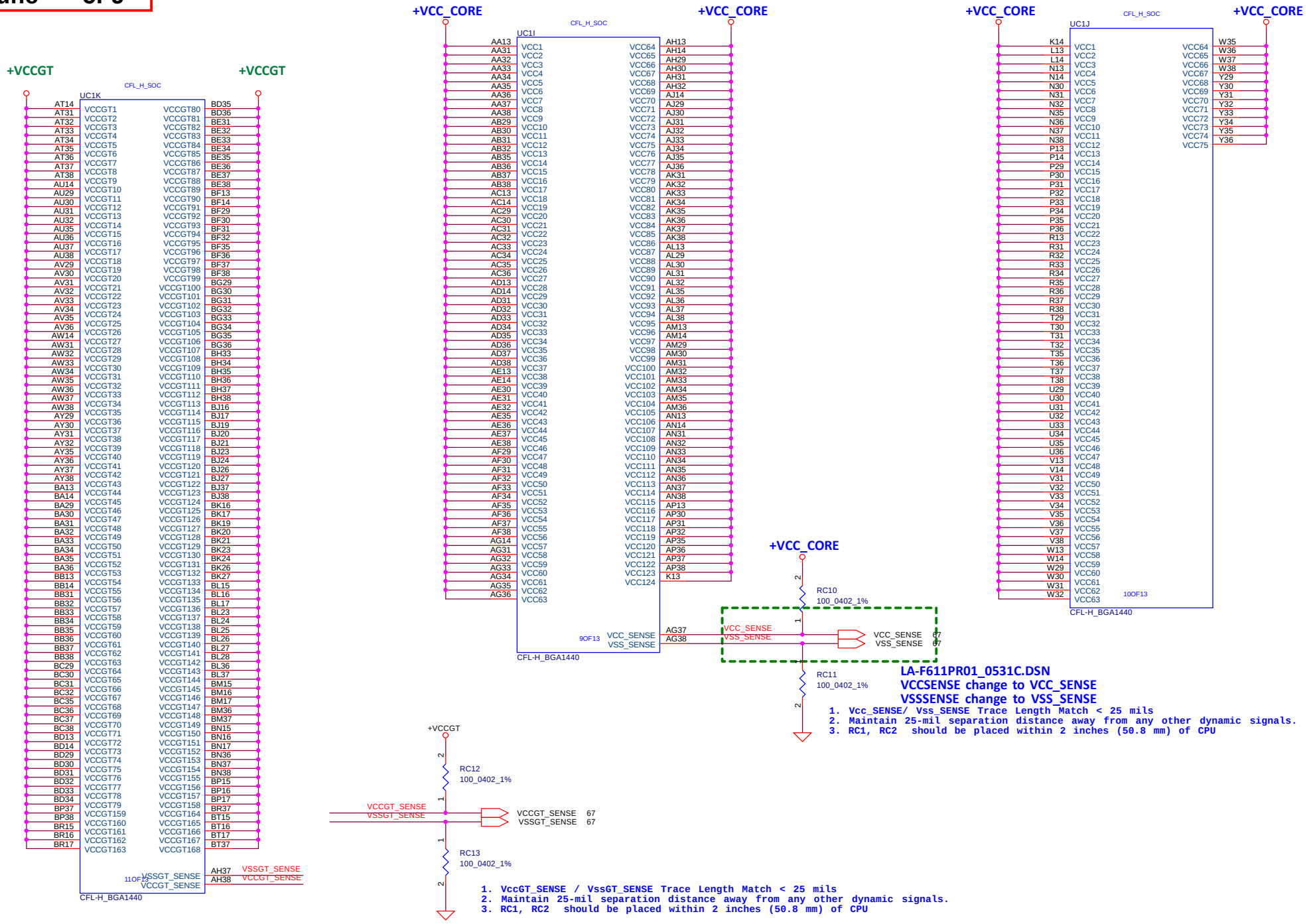
Compal Electronics, Inc.

Title: CFL-H(5/8)CFG

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 10 of 78

Main Func = CPU



LA-F611PR01_0531C.DSN
VCCSENSE change to VCC_SENSE
VSSSENSE change to VSS_SENSE

1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

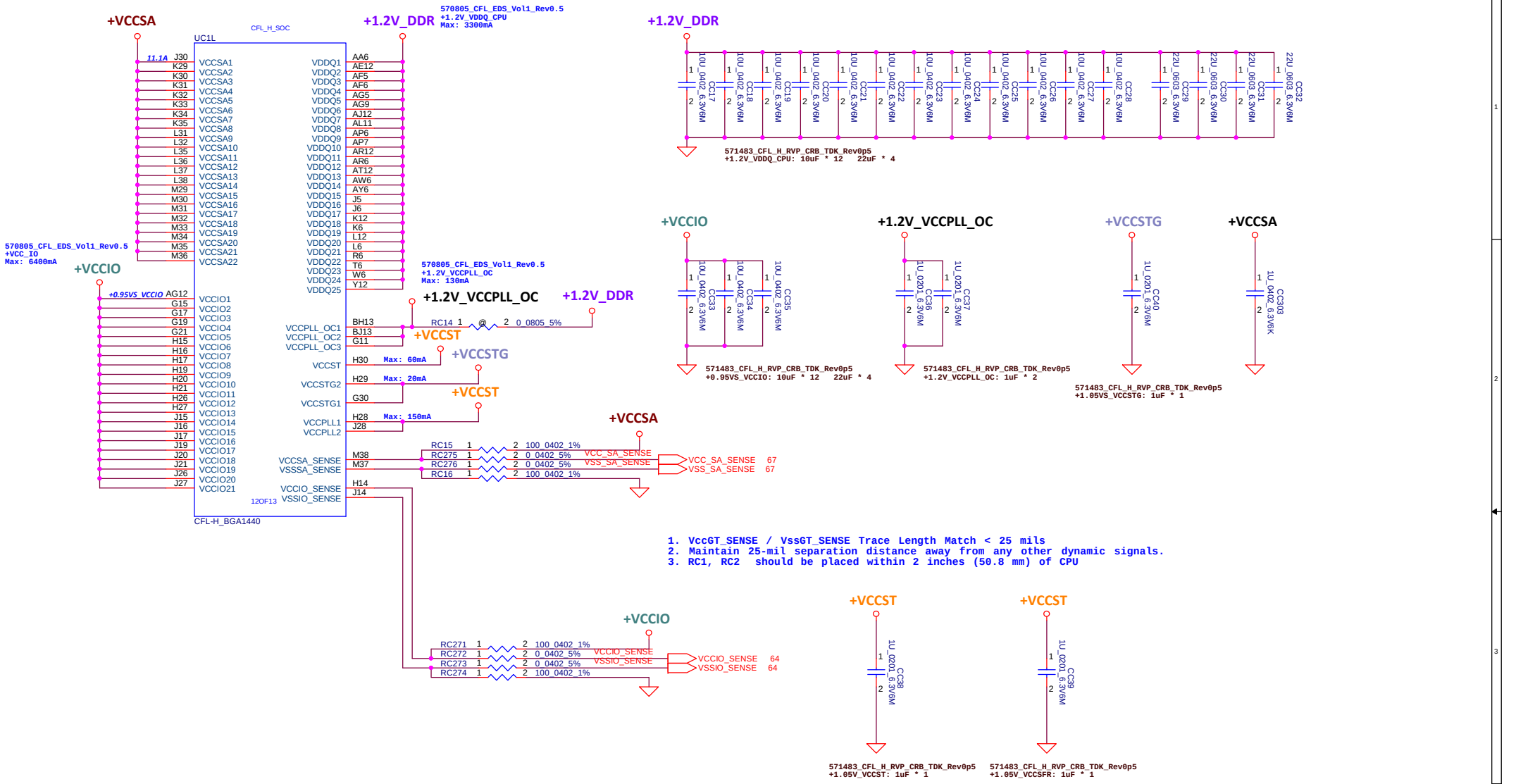
Compal Electronics, Inc.

Title: CFL-H(6/8)VCC_CORE/GT

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 11 of 78

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

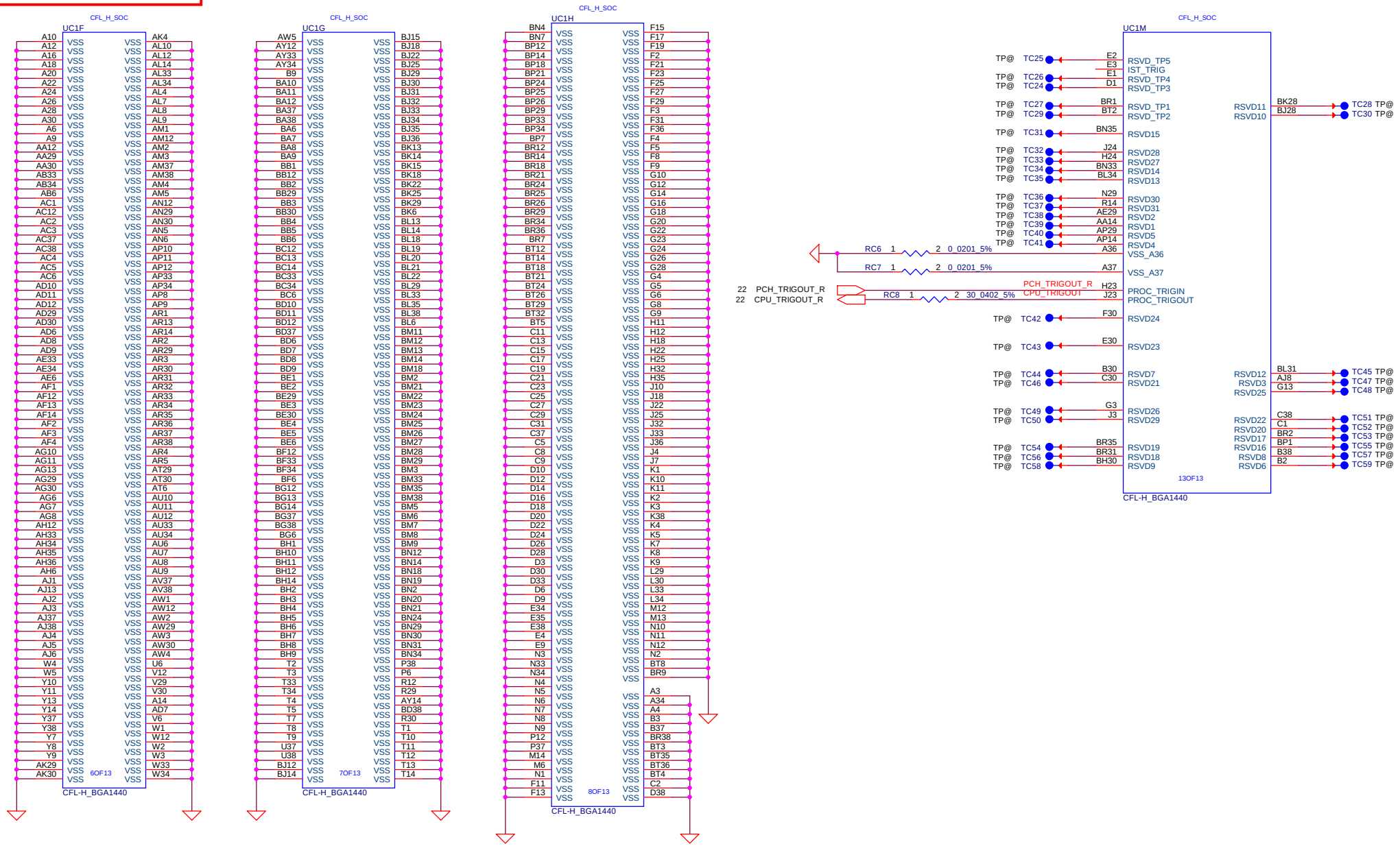
Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 12 of 78

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 13 of 78

Main Func = DDR

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

7 DDR_A_D[0..63]
7 DDR_A_MA[0..13]
7 DDR_A_DQS#[0..7]
7 DDR_A_DQS[0..7]

+2.5V_MEM
CD1 10U_0603_6.3V6M-D
CD2 10U_0603_6.3V6M-D
CD3 1U_0402_6.3V6K-D
CD4 1U_0402_6.3V6K-D

+0.6V_DDR_VTT
CD5 1U_0402_6.3V6K-D
CD6 10U_0603_6.3V6M-D
CD7 10U_0603_6.3V6M-D
CD8 1U_0402_6.3V6K-D
CD9 1U_0402_6.3V6K-D

+3VS
CD10 2.2U_0603_6.3V6K-D
CD30 0.022U_0402_25V7K

+1.2V_DDR
CD11 1U_0402_6.3V6K-D
CD12 1U_0402_6.3V6K-D
CD13 1U_0402_6.3V6K-D
CD14 1U_0402_6.3V6K-D
CD15 1U_0402_6.3V6K-D
CD16 1U_0402_6.3V6K-D
CD17 1U_0402_6.3V6K-D
CD18 1U_0402_6.3V6K-D

+1.2V_DDR
CD19 10U_0603_6.3V6M-D
CD20 10U_0603_6.3V6M-D
CD21 10U_0603_6.3V6M-D
CD22 10U_0603_6.3V6M-D
CD23 10U_0603_6.3V6M-D
CD24 10U_0603_6.3V6M-D
CD25 10U_0603_6.3V6M-D
CD26 10U_0603_6.3V6M-D
CD27 330U_D2_2V_Y MAIN@

CD28 0.1U_0402_16V7K-D
CD29 0.1U_0402_16V7K-D

RD1 0_0402_5%
RD2 0_0402_5%
RD3 0_0402_5%
RD4 0_0402_5%
RD5 0_0402_5%
RD6 0_0402_5%
RD7 470_0402_1%
RD8 0_0402_5%
RD9 2_0402_1%
RD10 1K_0402_1%~D
RD11 24.9_0402_1%
RD12 1K_0402_1%~D
RD23 240_0402_1%

DIMM_CHA_SA0
DIMM_CHA_SA1
DIMM_CHA_SA2
DDR_DRAMRST#
H_DRAMRST# 18
+V_DDR_REFA_R
+V_DDR_REFA
20mil

JDIMM1 SP07001CY0L

DDR_A_D1	VSS1	VSS2	DDR_A_D0
DDR_A_D5	DQ5	DQ4	DDR_A_D4
	VSS3	VSS4	
	DQ1	DQ0	
DDR_A_DQS#0	VSS5	VSS6	
DDR_A_DQS0	DQS0_c	DM0_n/DBI0_n	
	DQS0_t	VSS7	DDR_A_D6
DDR_A_D7	VSS8	DQ6	
	DQ7	VSS9	DDR_A_D2
DDR_A_D3	VSS10	DQ2	
	DQ3	VSS11	DDR_A_D12
DDR_A_D9	VSS12	DQ12	
	DQ13	VSS13	DDR_A_D13
DDR_A_D8	VSS14	DQ8	
	DQ9	VSS15	DDR_A_DQS#1
	VSS16	DQS1_c	DDR_A_DQS1
	DM1_n/DBI_n	DQS1_t	
DDR_A_D10	VSS17	VSS18	DDR_A_D15
	DQ15	DQ14	
DDR_A_D11	VSS19	VSS20	DDR_A_D14
	DQ10	DQ11	
DDR_A_D16	VSS21	VSS22	DDR_A_D21
	DQ21	DQ20	
DDR_A_D17	VSS23	VSS24	DDR_A_D20
	DQ17	DQ16	
DDR_A_DQS#2	VSS25	VSS26	
DDR_A_DQS2	DQS2_c	DM2_n/DBI2_n	
	DQS2_t	VSS27	DDR_A_D19
DDR_A_D23	VSS28	DQ22	
	DQ23	VSS29	DDR_A_D22
DDR_A_D18	VSS30	DQ18	
	DQ19	VSS31	DDR_A_D28
DDR_A_D24	VSS32	DQ28	
	DQ29	VSS33	DDR_A_D25
DDR_A_D29	VSS34	DQ24	
	DQ25	VSS35	DDR_A_DQS#3
	VSS36	DQS3_c	DDR_A_DQS3
	DM3_n/DBI3_n	DQS3_t	
DDR_A_D31	VSS37	VSS38	DDR_A_D26
DDR_A_D30	DQ30	DQ31	
	VSS39	VSS40	DDR_A_D27
	DQ26	DQ27	
	VSS41	VSS42	
	CB5/NC	CB4/NC	
	VSS43	VSS44	
	CB1/NC	CB0/NC	
	VSS45	VSS46	
	DQS8_c	DM8_n/DBI_n/NC	
	DQS8_t	VSS47	
	VSS48	CB6/NC	
	CB2/NC	VSS49	
	VSS50	CB7/NC	
	CB3/NC	VSS51	DDR_DRAMRST#
	VSS52	RESET_n	DDR_A_CKE1
DDR_A_CKE0	CKE0	CKE1	
	VDD1	VDD2	
DDR_A_BG1	BG1	ACT_n	DDR_A_ALERT#
DDR_A_BG0	BG0	ALERT_n	
	VDD3	VDD4	DDR_A_MA11
DDR_A_MA12	A12	A11	DDR_A_MA7
DDR_A_MA9	A9	A7	
	VDD5	VDD6	DDR_A_MA5
DDR_A_MA8	A8	A5	DDR_A_MA4
DDR_A_MA6	A6	A4	
	VDD7	VDD8	DDR_A_MA2
DDR_A_MA3	A3	A2	
DDR_A_MA1	A1	EVENT_n/NF	
	VDD9	VDD10	DDR_A_CLK1
DDR_A_CLK0	CK0_t	CK1_t/NF	DDR_A_CLK#1
DDR_A_CLK#0	CK0_c	CK1_c/NF	
	VDD11	VDD12	DDR_A_MA0
DDR_A_PAR	PARITY	A0	DDR_A_MA10
DDR_A_BA1	BA1	A10/AP	
	VDD13	VDD14	DDR_A_BA0
DDR_A_CS#0	CS0_n	BA0	DDR_A_MA16_RAS#
DDR_A_MA14_WE#	WE_n/A14	RAS_n/A16	
	VDD15	VDD16	DDR_A_MA15_CAS#
DDR_A_ODT0	ODT0	CAS_n/A15	DDR_A_MA13
DDR_A_CS#1	CS1_n	A13	
	VDD17	VDD18	
DDR_A_ODT1	ODT1	C0/CS2_n/NC	TP40
	VDD19	VREFCA	+V_DDR_REFA
TP41	C1, CS3_n,NC	SA2	DIMM_CHA_SA2
	VSS53	VSS54	
DDR_A_D36	DQ37	DQ36	DDR_A_D33
DDR_A_D37	VSS55	VSS56	DDR_A_D32
	DQ33	DQ32	
	VSS57	VSS58	
DDR_A_DQS#4	DQS4_c	DM4_n/DBI4_n	
DDR_A_DQS4	DQS4_t	VSS59	DDR_A_D38
DDR_A_D39	VSS60	DQ39	
	DQ38	VSS61	DDR_A_D35
DDR_A_D34	VSS62	DQ35	
	DQ34	VSS63	DDR_A_D45
DDR_A_D41	VSS64	DQ45	
	DQ44	VSS65	DDR_A_D44
DDR_A_D40	VSS66	DQ41	
	DQ40	VSS67	DDR_A_DQS#5
	VSS68	DQS5_c	DDR_A_DQS5
	DM5_n/DBI5_n	DQS5_t	
DDR_A_D43	VSS69	VSS70	DDR_A_D47
DDR_A_D42	DQ42	DQ47	
	VSS71	VSS72	DDR_A_D46
DDR_A_D48	VSS73	DQ43	
	DQ52	VSS74	DDR_A_D50
DDR_A_D52	VSS75	DQ53	
	DQ49	VSS76	DDR_A_D49
DDR_A_DQS#6	VSS77	DQ48	
DDR_A_DQS6	DQS6_c	VSS78	
	DQS6_t	DM6_n/DBI6_n	
DDR_A_D55	VSS80	VSS79	DDR_A_D54
	DQ55	DQ54	
DDR_A_D53	VSS82	VSS81	DDR_A_D51
	DQ51	DQ50	
DDR_A_D59	VSS84	VSS83	DDR_A_D58
	DQ61	DQ60	
DDR_A_D56	VSS86	VSS85	DDR_A_D57
	DQ56	DQ57	
	VSS88	VSS87	DDR_A_DQS#7
	DM7_n/DBI7_n	DQS7_c	DDR_A_DQS7
	VSS89	DQS7_t	
DDR_A_D60	DQ62	VSS90	DDR_A_D62
DDR_A_D61	VSS91	DQ63	
PCH_SMBCLK	DQ58	VSS92	DDR_A_D63
	VSS93	DQ59	
	SCL	VSS94	PCH_SMBDATA
	VDDSPD	SDA	DIMM_CHA_SA0
	VPP1	SA0	
	VPP2	VTT	DIMM_CHA_SA1
	GND1	SA1	
		GND2	

LOTES_ADDR0206-P001A02~D
DEREN_40-42271-26001RHF
CONN@

15,18,32 PCH_SMBCLK
PCH_SMBDATA 15,18,32
+0.6V_DDR_VTT
DDR_DRAMRST# 15
DDR_A_CKE1 7
DDR_A_ACT# 7
DDR_A_ALERT# 7
DDR_A_CLK1 7
DDR_A_CLK#1 7
DDR_A_BA0 7
DDR_A_MA16_RAS# 7
DDR_A_MA15_CAS# 7

All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: DDR4 DIMMA_RVS

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 14 of 78

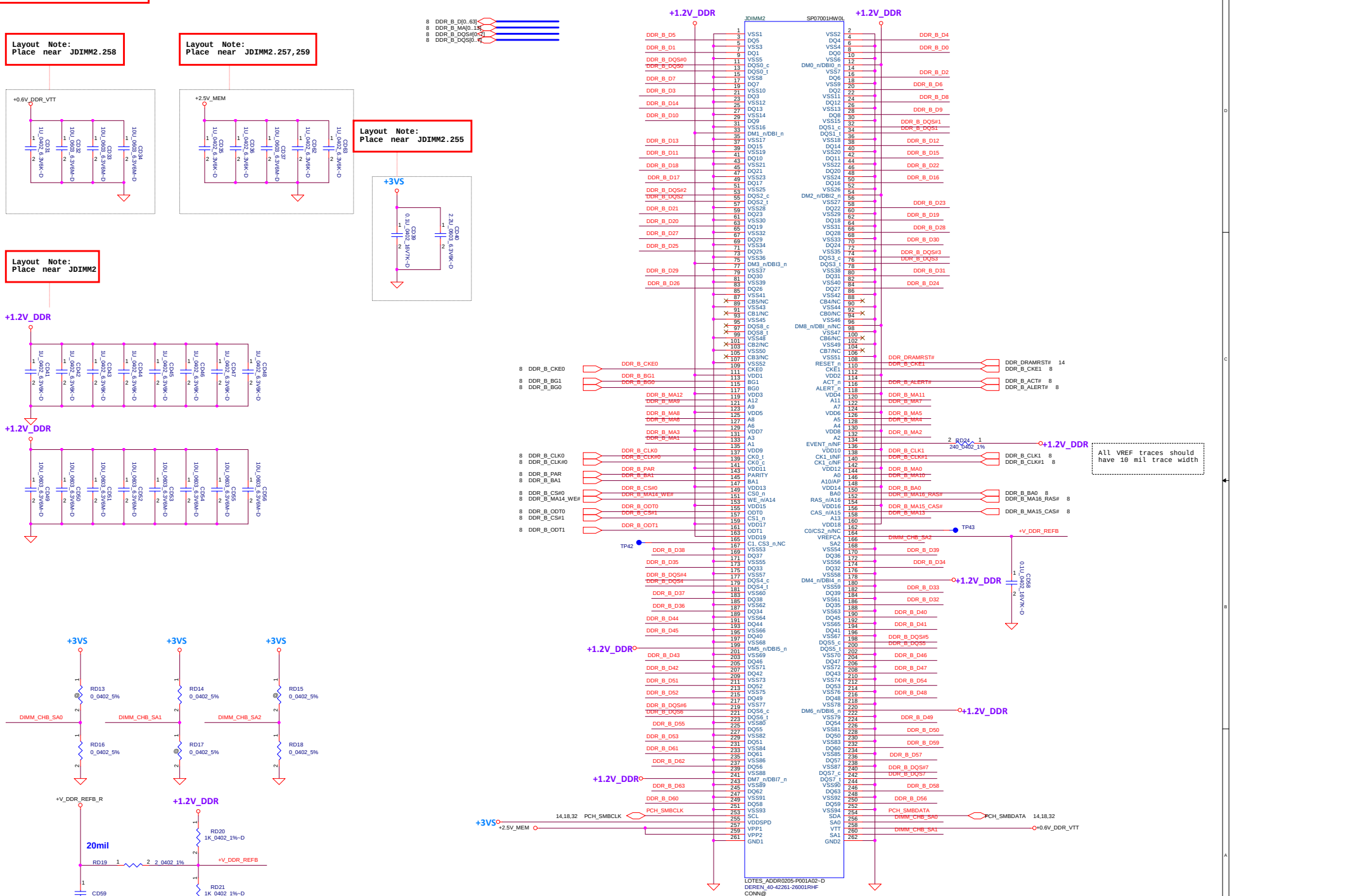
Main Func = DDR

Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: DDR4 DIMMB_STD

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 15 of 78

Main Func = PCH

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe

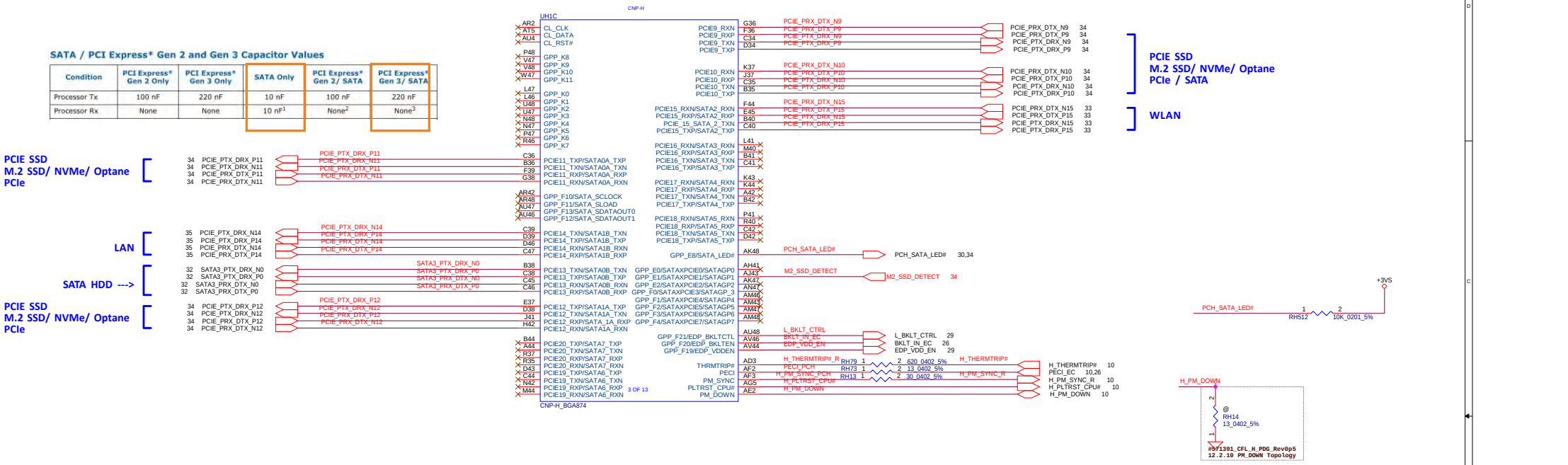
LAN

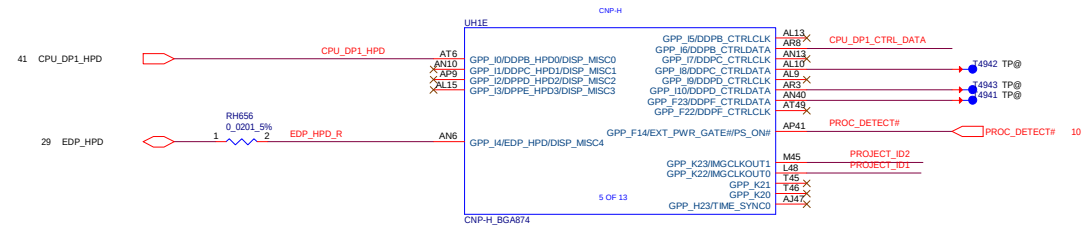
SATA HDD --->

PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe

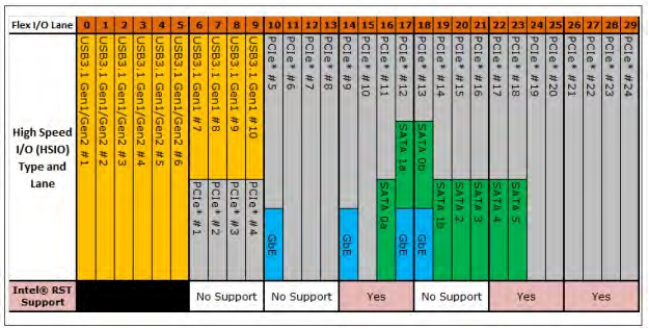
PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe / SATA

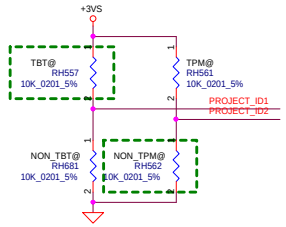
WLAN





eDP_HPD pull down 100K





PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

PROJECT ID	PROJECT ID1 (GPP_K22)
Non-TBT	0
TBT	1

TPM ID	PROJECT ID2 (GPP_K23)
SW TPM	0
HW TPM	1

Compal Electronics, Inc.

Title: PCH (1/7) SATA,DDC,PCIE

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 16 of 78

Main Func = PCH

Update OK

YH1 CH45 CH46 Main X76 control
X7676731L91

YH2 CH47 CH48 Main X76 control
X7676731L74

GPU
LAN
WLAN
NVMe

TBT

XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

RTC CRYSTAL
Max Crystal ESR
= 50k Ohm.

Reserve for RF immunity

Metal Shielding Type

CFL-H PDG rev0.7
pop 20K for SPI0_IO2/3

CNL- PCH EDS rev0.5
Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V

RH1 close to UH4

SPI ROM

PCH

SPI ROM FOR ME (32MByte)
PN: SA00009RI10

Co-lay with UH4

Close UH4

Reserve for ESD

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PCH (2/7) CLK,SPI,PLTRST

Size | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 17 of 78

Main Func = PCH

PCH to DDR, XDP, FFS

DVT1.0
Change QH6 to SB00000PU00

CLRP1 in DIMM Door

GPU_THM_SMBCLK
GPU_THM_SMBDAT
GPU_THM_EC

PCH to DDR / FFS

VALW
VS

Buffer with Open Drain Output For VTT power control

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated)
Enable ME Protect (ME cannot be updated)(Default posit i on)

GPU ID	GPU ID2 (GPP_D6)	GPU ID1 (GPP_D5)
UMA	0	0
N17P-G0	0	1
N17E-G1	1	0
N17P-G1	1	1

RH552 UMA@ / RH551 N17P_G0@ / RH553 N17E_G1@ / RH551 N17P_G1@
10K_0201_5% — SD043100280

RH554 UMA@ / RH554 N17P_G0@ / RH552 N17E_G1@ / RH553 N17P_G1@
10K_0201_5% — SD043100280

Reserve for ESD

Reserve for RF please close to UH1

TLS CONFIDENTIALITY	
HIGH	Enable
LOW(DEFAULT)	Disable

EC interface	
HIGH	ESPI*
LOW(DEFAULT)	LPC

Top Swap Override (internal PD)	
HIGH	Enable
LOW(DEFAULT)	Disable

PCHHOT#	
HIGH	Enable
LOW(DEFAULT)	Disable

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

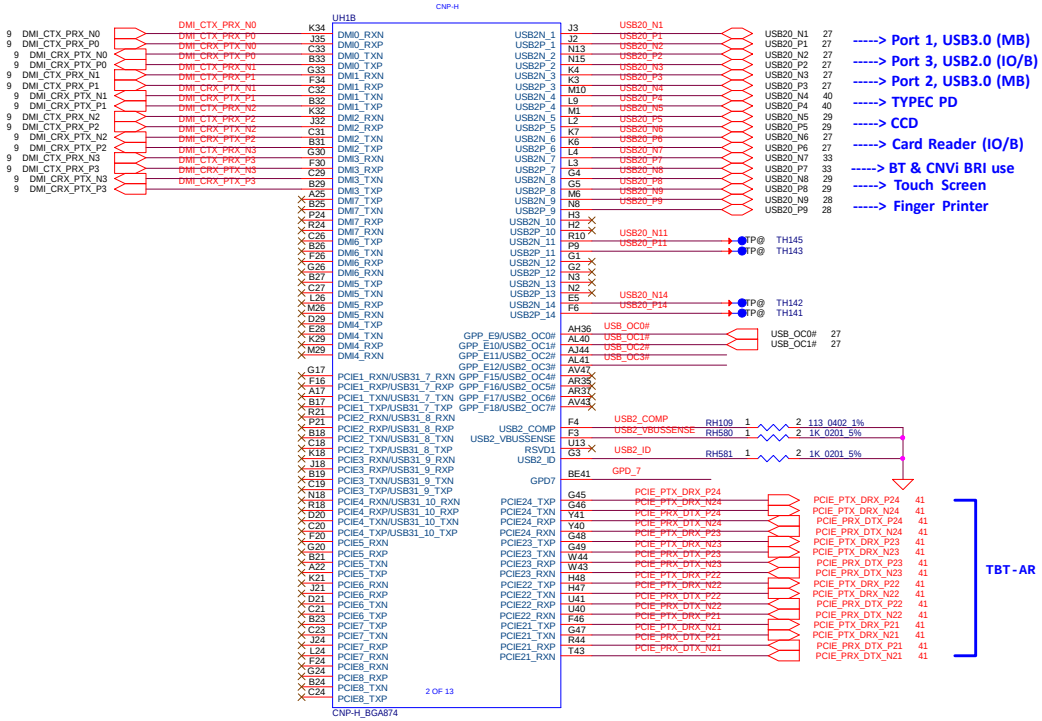
Title: PCH (3/7) PM,HDA,SMB,JTAG

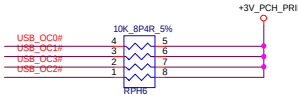
Size: — Document Number: LA-F611P — Rev: 0.3

Date: Thursday, March 22, 2018 — Sheet 18 of 78

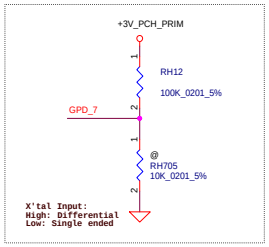
Main Func = PCH

Update OK

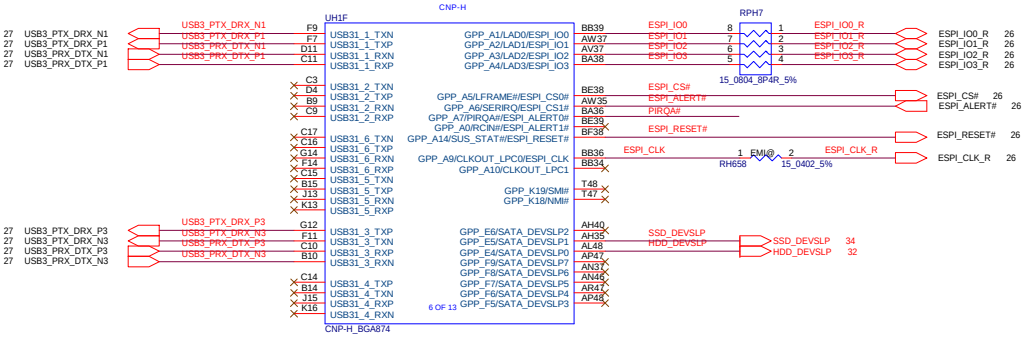




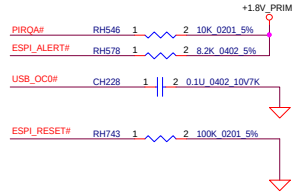
USB2_COMP
50ohm single-ended and as short as possible
Spacing=15 mils
Max length= 1000 mils

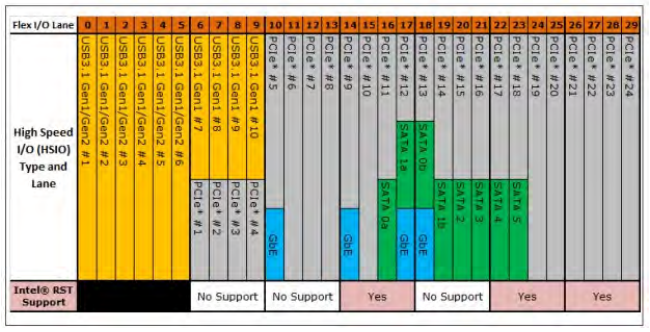


USB3.0 Port1



USB3.0 Port2





Reserve for EMI

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 19 of 78

Main Func = PCH

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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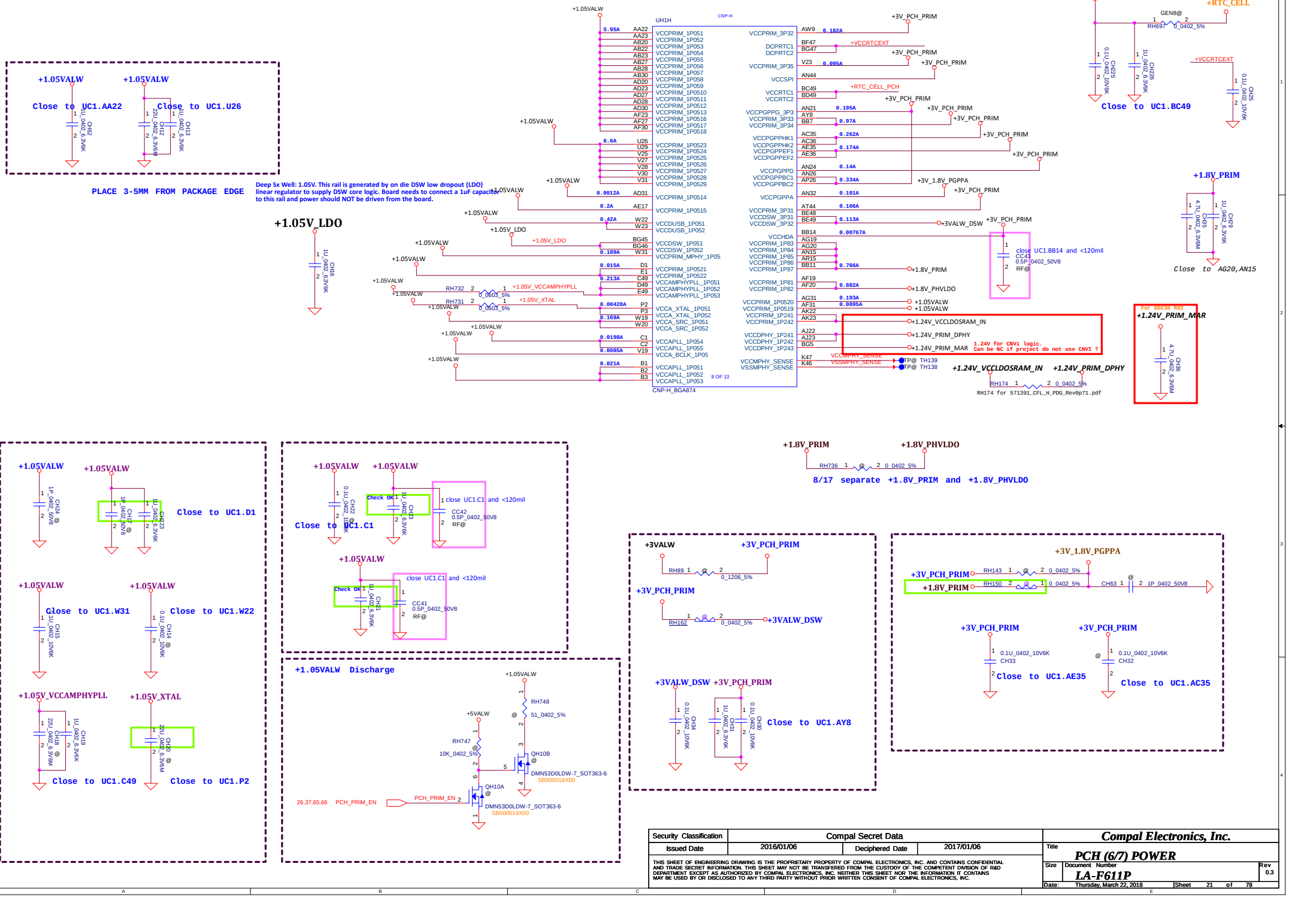
Compal Electronics, Inc.

Title: PCH (5/7) I2C,GPIO,CNVI

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 20 of 78

Main Func = PCH



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

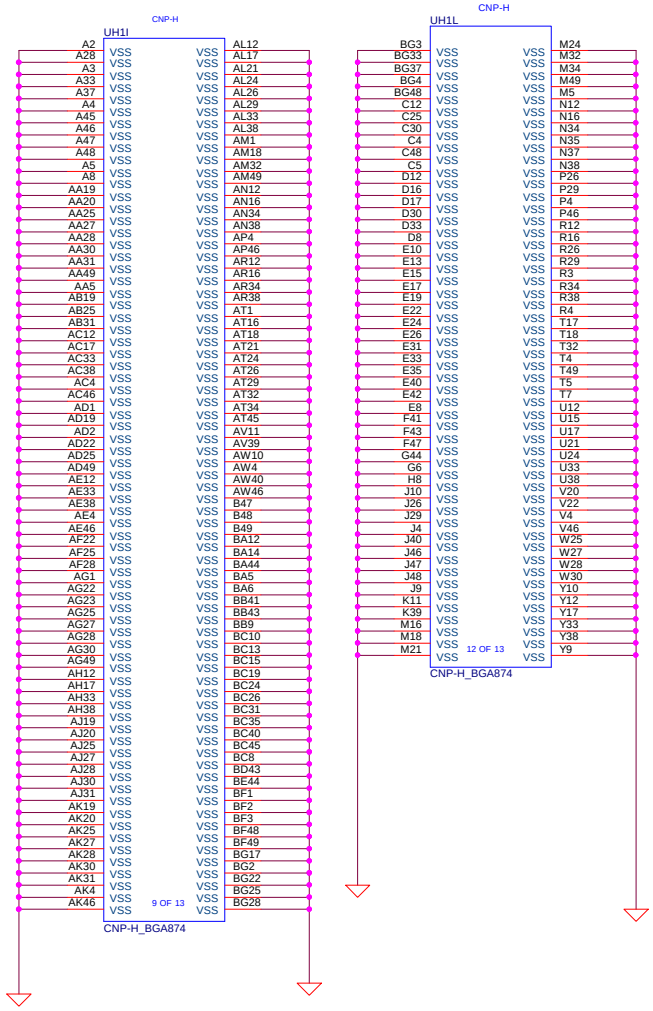
Compal Electronics, Inc.

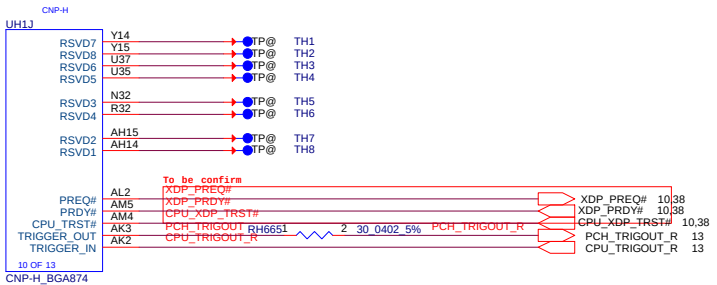
Title: **PCH (6/7) POWER**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 21 of 78

Main Func = PCH





Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

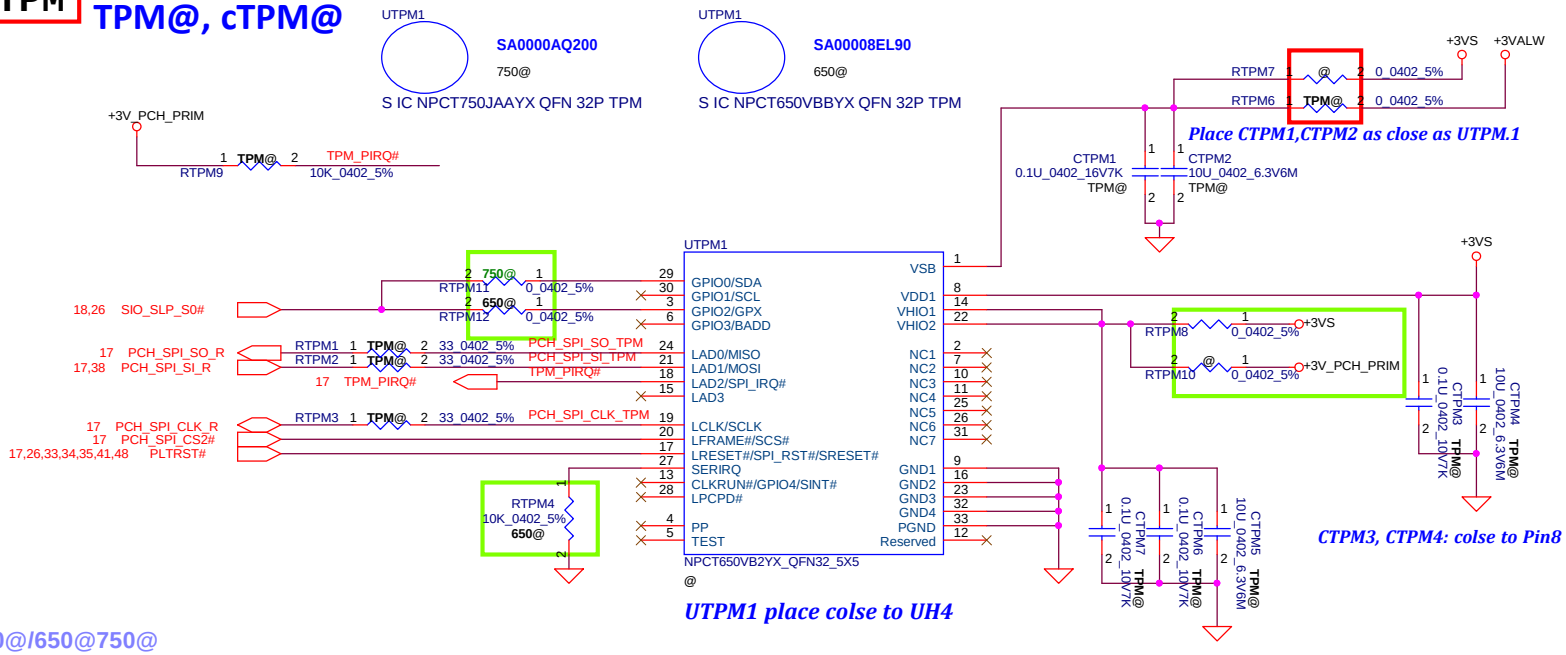
Title: **PCH (7/7) VSS**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 22 of 78

Main Func = TPM

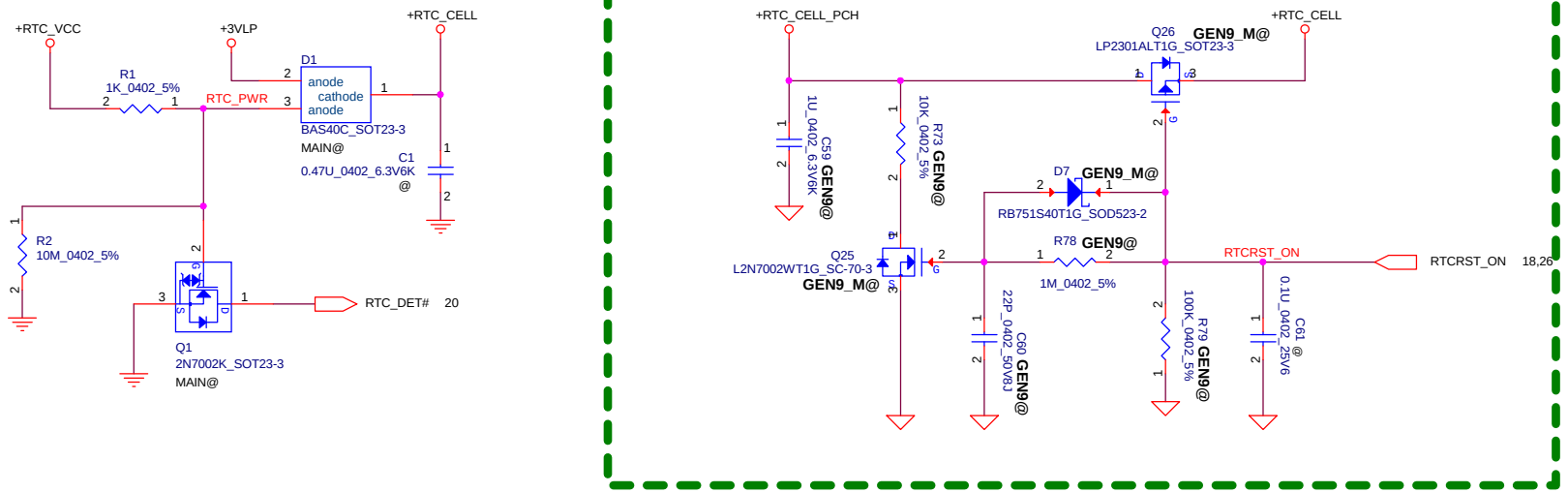
TPM@, cTPM@



NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@

Main Func = RTC

GEN9@



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **TPM/RTC/Screw Holes**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 23 of 78

Main Func = Audio

EMI@, RF@, @EMI@, @ESD@, @RF@

+5VS 2A

+3VS 25mA

Layout Note: Close pin39

Layout Note: Close pin34

Close pin8

CA9,L5 place colse to UA1.3

moat

+1.8V_PRIM

Place close to Pin 26

Close pin33

Close pin29

CLOSE TO UA1

RA43,CA38: close to UA1.6

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

Layout Note: Place close to Pin 12

Layout Note: Width>40mil, to improve Headphone Crosstalk noise Change it to sharp will be better. Add 2 vias (>0.5A) when trace layer change.

Layout Note: Tied at point only under Codec or near the Codec

Place on the moat between GND & GNDA.

Speaker

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: Audio Codec ALC3204

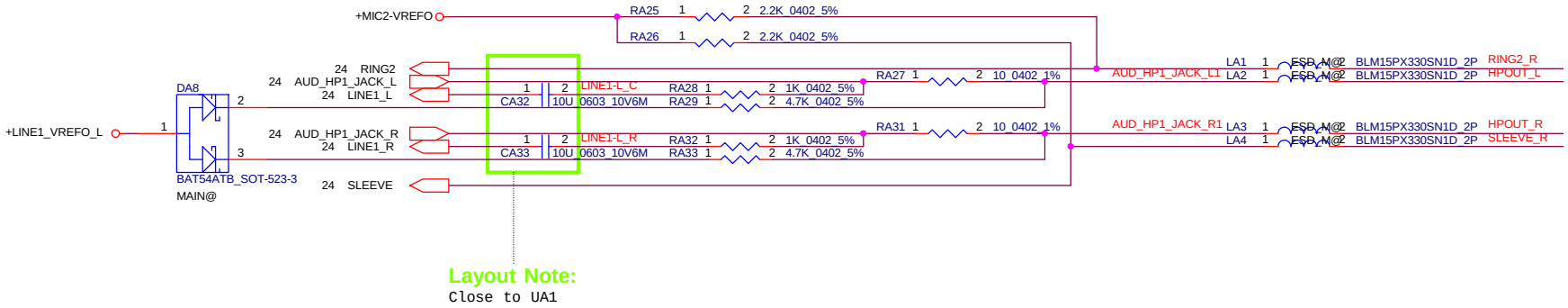
Size | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 24 of 78

Main Func = Audio Jack

ESD@

Universal Jack
(Global Headset Jack + mic phone in + line in support)

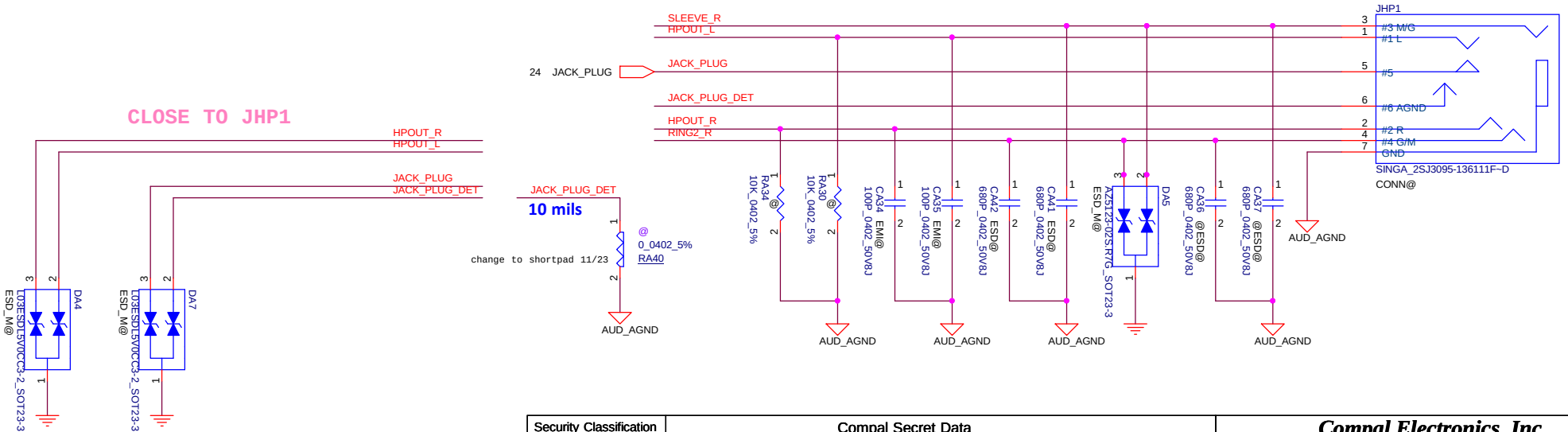


Layout Note:
Close to UA1

Main Func = Audio Jack

EMI@, @ESD@, ESD@

Universal Jack
(Global Headset Jack + mic phone in + line in support)



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Audio Jack**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 25 of 78

Main Func = EC

RE3 For SKU ID Select

N17P_G0 w/o TBT	17.8K	
N17P_G1 w/o TBT	27K	
N17E_G1 w/o TBT	37.4K	
N17P_G0 w/ TBT	49.9K	
N17P_G1 w/ TBT	64.9K	
N17E_G1 w/ TBT	82.5K	

RE3 N17P_G0@NON_TBT@ — 17.8K_0402_1% — SD034178280
RE3 N17P_G1@NON_TBT@ — 27K_0402_1% — SD034270280
RE3 N17E_G1@NON_TBT@ — 37.4K_0402_1% — SD034374280
RE3 N17P_G0@TBT@ — 49.9K_0402_1% — SD034499280
RE3 N17P_G1@TBT@ — 64.9K_0402_1% — SD034649280
RE3 N17E_G1@TBT@ — 82.5K_0402_1% — SD000002780

RE1 EC@ — 49.9K_0402_1% — SD034499280

SD034100280 10K_0402_1%
SD034178280 17.8K_0402_1%
SD034270280 27K_0402_1%
SD034374280 37.4K_0402_1%
SD034499280 49.9K_0402_1%
SD034649280 64.9K_0402_1%
SD000002780 82.5K_0402_1%
SD034107380 107K_0402_1%
SD034154380 154K_0402_1%
SD034200380 200K_0402_1%

For Board ID Select

EVT	10K
DVT1	17.8K
DVT2	27K
Pilot	49.9K

Model ID

+3VALW_EC — RE3 100K_0402_1% @ — MODEL_ID — Ra / Rb — CE1 0.1U_0402_10V7K — EC_AGND

Board ID

+3VALW_EC — RE1 100K_0402_1% @ — BOARD_ID — Ra / Rb — CE2 0.1U_0402_10V7K — EC_AGND

EC Chip CPN

UE1 EC@ — MEC1416-NU-D0_VTQFP128_14X14 — SA0000A8L00

Power Inputs

+3.3V_ADP_DCIN — DT19 — RB551V-30_SOD323-2
+3.3V_VBUS_IN — DT21 — RB551V-30_SOD323-2
+3VALW — RE2 0_0603_5% — DT20 — RB551V-30_SOD323-2

+3VALW — 100P_0402_50V8J CE25 — 0.1U_0402_10V7K CE6 — 2.2U_0603_6.3V6M CE7 — 100P_0402_50V8J CE8 — 0.1U_0402_25V6 CE9 — 0.1U_0402_25V6 CE10 — 0.1U_0402_25V6 CE11 — 0.1U_0402_25V6 CE12 — 0.1U_0402_25V6 CE13

+3VALW_EC — 0.1U_0402_25V6 CE14 — 0.1U_0402_25V6 CE15

+3VALW_EC — 68P_0402_50V8J CE36 — 10P_0201_50V8J CE37 — PAD RF@
+1.8VALW_EC — 68P_0402_50V8J CE38 — 10P_0201_50V8J CE39 — PAD RF@

+3VALW_EC — +RTC_CELL — RE7 0_0603_5% — +RTC_CELL_VBAT — CE16 0.1U_0402_10V7K

+1.8V_PRIM — RE66 0_0603_5% — +1.8VALW_EC

RTC Circuit

+RTC_CELL — RE141 0_0201_5% — PRIM_PWRGD_R — RE160 0_0201_5% — PRIM_PWRGD

Keyboard Matrix

31 KSI[0..7] — KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
31 KSO[0..16] — KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16

RPE1 10K_8P4R_5% — KSI0 KSI1 KSI2 KSI3
RPE2 10K_8P4R_5% — KSI7 KSI6 KSI5 KSI4
RPE3 100K_8P4R_5% — KSO0 KSO1 KSO2 KSO3
RPE4 100K_8P4R_5% — KSO4 KSO5 KSO6 KSO7
RPE5 100K_8P4R_5% — KSO10 KSO11 KSO13 KSO8
RPE6 100K_8P4R_5% — KSO8 KSO15 KSO14 KSO16

MEC1416

UE1 — MEC1416

GPIO027/KSO00/PVT_IO1
GPIO015/KSO01/PVT_CS#
GPIO016/KSO02/PVT_SCLK
GPIO017/KSO03/PVT_IO0
GPIO045/BCM_INT1#/KSO04
GPIO046/BCM_DAT1/KSO05
GPIO047/BCM_CLK1/KSO06
GPIO025/KSO07/PVT_IO2
GPIO055/PWM2/KSO08/PVT_IO3
GPIO102/KSO09[CR_STRAP]
GPIO106/KSO10
GPIO110/KSO11
GPIO111/KSO12
GPIO112/PS2_CLK1A/KSO13
GPIO113/PS2_DAT1A/KSO14
GPIO125/KSO15
GPIO132/KSO16
GPIO140/KSO17

GPIO143/KSI0/DTR#
GPIO144/KSI1/DCD#
GPIO005/SMB00_DATA/SMB00_DATA18/KSI2
GPIO006/SMB00_CLK/SMB00_CLK18/KSI3
GPIO147/KSI4/DSR#
GPIO150/KSI5/RI#
GPIO151/KSI6/RTS#
GPIO152/KSI7/CTS#

GPIO114/PS2_CLK0
GPIO115/PS2_DAT0
GPIO026/PS2_CLK1B
GPIO127/PS2_DAT1B

GPIO040/LAD0/ESPI_IO0
GPIO041/LAD1/ESPI_IO1
GPIO042/LAD2/ESPI_IO2
GPIO043/LAD3/ESPI_IO3
GPIO044/LFRAME#/ESPI_CS#
GPIO064/LRESET#/
GPIO034/PCI_CLK/ESPI_CLK
GPIO067/CLKRUN#
GPIO063/SER_IRQ/ESPI_ALERT#
GPIO011/nSMI/nEMI_INT
GPIO060/KBRST
GPIO061/LPCPD#/ESPI_RESET#
GPIO100/nEC_SCI

GPIO126/SMD_SCLK
GPIO133/SMD_IO0
GPIO134/SMD_IO1
GPIO135/SMD_IO2
GPIO136/SMD_IO3
GPIO123/SMD_CS#[BSS_STRAP]
GPIO001/SPI_CS#/32KHZ_OUT

GPIO101/SPI_CLK
GPIO103/SPI_IO0
GPIO105/SPI_IO1
GPIO052/SPI_IO2
GPIO062/SPI_IO3
GPIO001/SPI_CS#/32KHZ_OUT

nRESET_IN/GPIO014
GPIO057/VCC_PWRGD
GPIO107/nRESET_OUT
XTAL2
XTAL1

GPIO007/SMB01_DATA/SMB01_DATA18
GPIO010/SMB01_CLK/SMB01_CLK18
GPIO012/SMB02_DATA/SMB02_DATA18
GPIO013/SMB02_CLK/SMB02_CLK18
GPIO130/SMB03_DATA/SMB03_DATA18
GPIO131/SMB03_CLK/SMB03_CLK18
GPIO141/SMB04_DATA/SMB04_DATA18
GPIO142/SMB04_CLK/SMB04_CLK18

GPIO050/TACH0
GPIO051/TACH1

GPIO053/PWM0
GPIO054/PWM1

GPIO056/PWM3
GPIO030/BCM_INT0#/PWM4
GPIO031/BCM_DAT0/PWM5
GPIO032/BCM_CLK0/PWM6
GPIO002/PWM7

GPIO157/LED0/TST_CLK_OUT
GPIO156/LED1
GPIO104/LED2

GPIO116/TFDP_DATA/UART_RX
GPIO117/TFDP_CLK/UART_TX

GPIO035/SB-TSI_CLK
GPIO033/PECI_DAT/SB_TSI_DAT

VREF_CPU

GPIO145/(ICSP_CLOCK)
GPIO146/(ICSP_DATA)
ICSP_MCLR

BGPO/GPIO004
SYSPWR_PRES/GPIO003
VCI_OUT/GPIO036
VCI_IN1#/GPIO162
VCI_IN0#/GPIO163
VCI_OVRD_IN/GPIO164

GPIO160/DAC_0
GPIO161/DAC_1
DAC_VREF

GPIO124/CMP_VOUT0
GPIO020/CMP_VIN0
GPIO165/CMP_VREF0

GPIO120/CMP_VOUT1
GPIO021/CMP_VIN1
GPIO166/CMP_VREF1/UART_CLK

GPIO024/ADC7
GPIO023/ADC6/A20M
GPIO022/ADC5
GPIO153/ADC4
GPIO154/ADC3
GPIO155/ADC2
GPIO122/ADC1
GPIO121/ADC0
ADC_VREF

VTR_33_18 — CE15 0.1U_0402_25V6

PBAT_CHG_SMBDAT — PBAT_CHG_SMBDAT 59,61
PBAT_CHG_SMBCLK — PBAT_CHG_SMBCLK 59,61
GPU_THM_SMBCLK — GPU_THM_SMBCLK 18,31,48
GPU_THM_SMBDAT — GPU_THM_SMBDAT 18,31,48
TYPEC_SMBCLK — TYPEC_SMBCLK 40
TYPEC_SMBDA — TYPEC_SMBDA 40
TBTA_HRESET — TBTA_HRESET 40
TBT_RESET_N_EC# — TBT_RESET_N_EC# 40,41

Modify 5/2
GPU_THM_SMBCLK
GPU_THM_SMBDAT

FAN1_TACH — FAN1_TACH 31
FAN2_TACH — FAN2_TACH 31

KB_LED_PWM 31
BEEP 24

FAN1_PWM — FAN1_PWM 31
FAN2_PWM — FAN2_PWM 31
LANWAKE# 18
PS_ID 59
PCIE_WAKE# 18,33,34,35,41

BAT2_LED# — BAT2_LED# 30
BAT1_LED# — BAT1_LED# 30
AUX_EN_WOWL
TP74

ME_FWP — ME_FWP 18
HOST_DEBUG_TX — HOST_DEBUG_TX 33

PTP_DIS# — PTP_DIS# 31
PECI_EC — PECI_EC 10,16

ICSP_CLK
ICSP_DAT
ICSP_CLR

NB_MUTE# — EC_MUTE# — EC_MUTE# 24
SYSPWR_PRES
ALWON 61,62
VCI_IN1
POWER_SW_IN# — RE70 100K_0402_5% — +RTC_CELL
HW_ACAV_IN 18,59,60,61

GC6_THM_DIS# — GC6_THM_DIS# 17
HW_ACAVIN_NB_EC 60

CMP_VOUT0 — CMP_VOUT0 56,62
CMP_VIN0 — RE37 0_0402_5% — VCIN0_PH 31
VCREF0

PROCHOT
WLAN_PWR_EN — WLAN_PWR_EN 33
LCD_TST 29

CMP_STRAP0

PANEL_BKEN_EC 29
SIO_EXT_WAKE# 20
MODEL_ID
I_ADP
BOARD_ID
LCD_VCC_TEST_EN — LCD_VCC_TEST_EN 29
I_BATT

+3VALW_EC

MEC1416-NU-D0_VTQFP128_14X14

TP44

VR_CAP — CE24 1U_0603_16V7 — ESR <100m ohms — Close UE1

EC_AGND

Power Rails

+1.05VALW — 0_0402_5% RE162 — VREF_CPU — 0.1U_0402_25V6 CE17

+3VALW — 10K_0402_5% RE35 — 0.047U_0402_16V4Z CE19 — LID_CL_SIO#

+3VALW — 10K_0402_5% RE90 — SIO_SLP_S0#

VCCDSW_ON — RE163 2_GEN8@ 1_0_0402_5% — SIO_PWRBTN#

+3VALW — 10K_0402_5% RE61 — POWER_SW_IN#

+3VALW — 2.2U_0402_6.3V6M CE23 — RE43 100_0402_5% — POWER_SW_MB 27

RE161 DOCK@ 10K_0402_5% — PWR_TB_DOCK# 40

+3VLP — RE29 1K_0402_5% — RE32 100K_0402_5%

+3VALW_EC — 0.1U_0402_25V6 CE20

+3V_PCH_PRIM — GPU_THM_SMBDAT — RE10 2.2K_0402_5% — GPU_THM_SMBCLK — RE11 2.2K_0402_5%

+3VALW_EC — RE49 100K_0402_5% — CMP_VIN0 — RE52 100K_0402_5% — CMP_VOUT0

+3VALW_EC — RE46 10K_0402_1% — RE167 10K_0402_1% — VCREF0 — 0.1U_0402_25V6 CE23 — RE48 10K_0402_1%

+3VALW_EC — I_ADP — RE51 300_0402_5% — I_ADP_R 61 — CE25 2200P_0402_25V7K — EC_AGND

+3VALW — I_BATT — RE54 300_0402_5% — I_BATT_R 61 — CE30 2200P_0402_25V7K — EC_AGND

+3VALW — RE164 100K_0402_5% — VCCDSW_ON — GEN9@ RC442 — 0_0402_5% — PCH_PRIM_EN 21,37,65,66

59,62,66 POK — DC2 RB751S40T1G_SOD523-2 — GEN9_M@

PECI_EC — DE1 AZ5125-01H.R7G_SOD523-2 @

Thermal Sensor

PBAT_CHG_SMBDAT — RE8 4.7K_0402_5%
PBAT_CHG_SMBCLK — RE9 4.7K_0402_5%
CMP_STRAP0 — RE165 100K_0402_5%
TP_WAKE_KBC# — RE14 100K_0402_5%
TYPEC_SMBDA — RE30 2.2K_0402_5%
TYPEC_SMBCLK — RE31 2.2K_0402_5%
UPD1_ALERT — RE155 10K_0402_5%
USB_EN# — RE17 100K_0402_5%
KSO9 — RE15 100K_0402_5%
CMP_VIN0 — RE166 100K_0402_5%
USB_POWERSHARE_VBUS_EN — RE169 10K_0402_5%

+3VS — FPR_SCAN# — RE156 100K_0402_5%
SYS_PWROK — RE68 10K_0402_5%
IMVP_VR_ON — RE16 10K_0402_5%
ME_FWP — RE19 1K_0402_5%
BKLT_IN_EC — RE157 100K_0402_5%
USB_POWERSHARE_VBUS_EN — RE168 10K_0402_5%

Debug Connector

+3VALW_EC — JESPI1 CONN@ — ESPI_IO0_R ESPI_IO1_R ESPI_IO2_R ESPI_IO3_R ESPI_CS# ESPI_CLK_R — RE65 0_0402_5% — PLTRST# 17,23,33,34,35,41,48 — JXT_FP241AH-010GAAM — SP010021O00

+3VALW — RPE7 10K_0804_8P4R_5% — RE59 49.9_0402_1% — JDEG1 CONN@ — JTAG_TDI JTAG_TMS JTAG_CLK JTAG_TDO MSCLK MSDATA — RE60 RE61 RE63 0_0201_5% — ICSP_CLK ICSP_CLR ICSP_DAT — HOST_DEBUG_TX — JXT_FP241AH-010GAAM — SP010021O00

+3VALW — RE58 RE59 RE62 RE63 10K_0402_5% — RE2 10K_0402_5%

Pin8 5085_TXD for EC Debug
pin9 5048_TXD for SBIOS debug

32 KHz Clock

MEC_XTAL1 — YE1 MAIN@ — MEC_XTAL2 — 32.768KHZ_9PF_X1A000141000200 — 20ppm / 9pF — ESR <50kohm (MAX) — CE3 10P_0402_50V8J — CE4 12P_0402_50VBJ

UE2 — VCC OUT NC GND — NL17SZ06DFT2G_SC70-5 MAIN@ — CE26 47P_0402_50V8J — RE53 10K_0402_1%

10,59,61,67 H_PROCHOT# — PROCHOT

+3VS — CE22 0.1U_0402_10V7K

RE67,CE35: close to UE1.57

Clock Circuit

ESPI_CLK_R — 28 FPR_SCAN# — RE85 0_0402_5% — 30.1K_0402_1% RE87 @EMI@ — 33P_0402_50V8J CE27 @EMI@

27 USB_EN# — RE42 0_0402_5% — RUNPWROK — 18 IMVP_VR_ON — RE158 0_0402_5% — RESET_OUT#

18 SUSCLK_EC — RE45 0_0402_5% — MEC_XTAL2 — MEC_XTAL1 — RE47 0_0402_5% — MEC_XTAL1_R

Need to change 0201

SMBus address 0x40

Close to UE1 each pin

FAN1_TACH — CE28 220P_0402_50V8J
HW_ACAVIN_NB_EC — CE34 100P_0402_50V8J
IMVP_VR_ON — CE31 1000P_0402_50V7K
HW_ACAV_IN — CE32 100P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

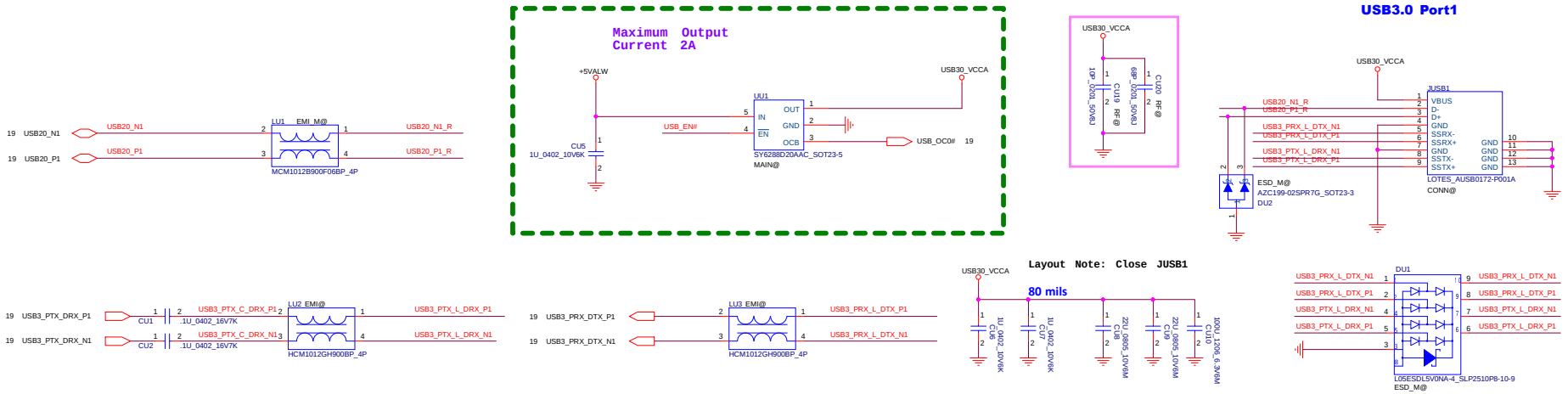
Compal Electronics, Inc.

Title: EC MEC1416

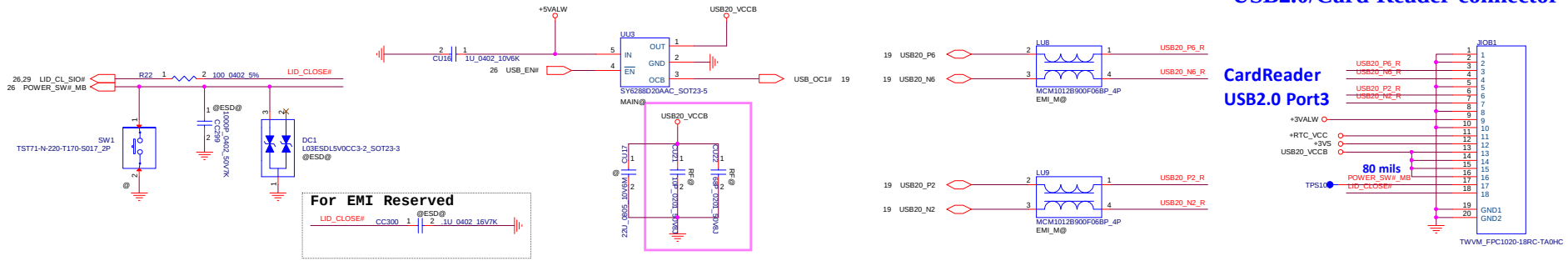
Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 — Sheet 26 of 78

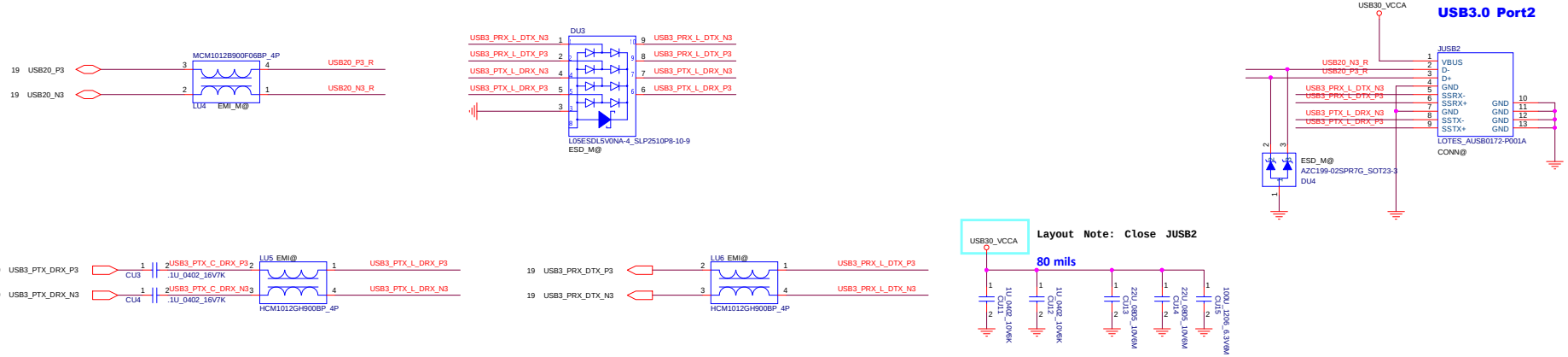
Main Func = USB3.0 Port1



Main Func = USB2.0 Port2 + Card Reader+Power BTN on IO/B



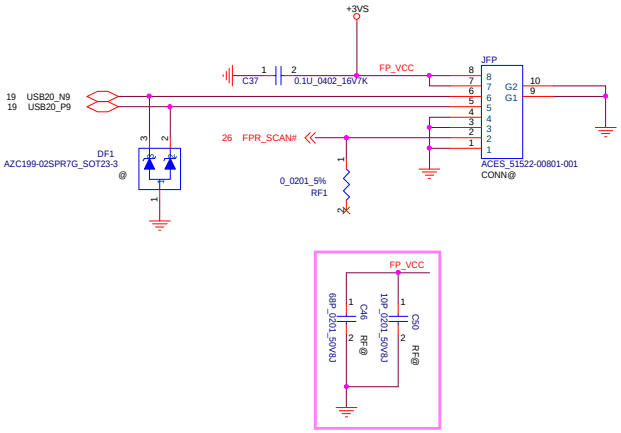
Main Func = USB3.0 Port2



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: USB3.0 & I/O			
Size	Document Number: LA-F611P		Rev: 0.3
Date: Thursday, March 22, 2018	Sheet 27 of 78		

Main Func = Finger Printer



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

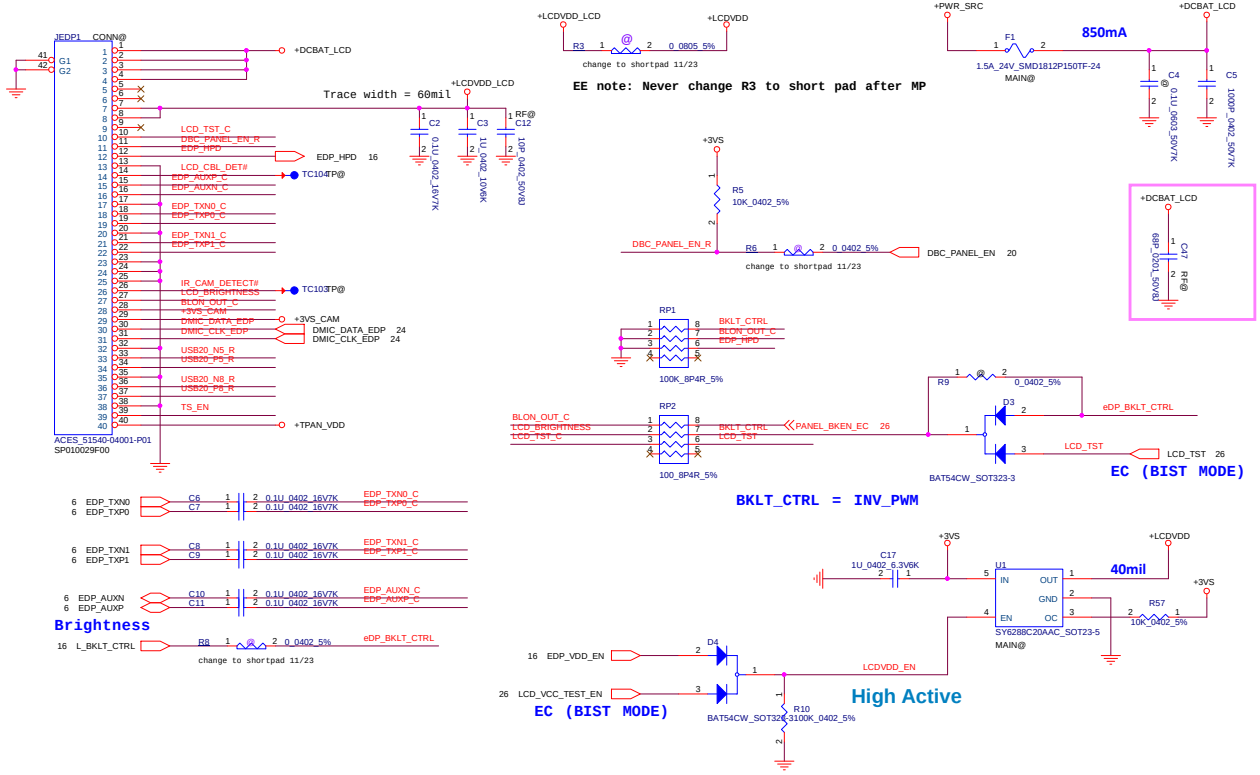
Title: **Finger Print**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 28 of 78

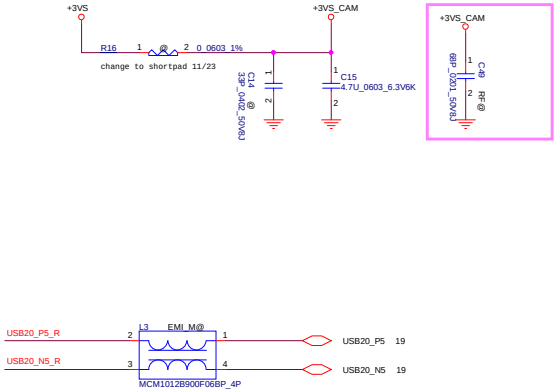
Main Func = LCD

INVERTER POWER

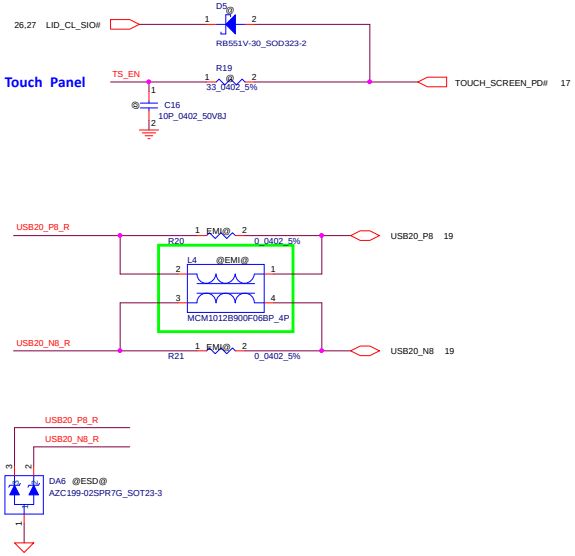


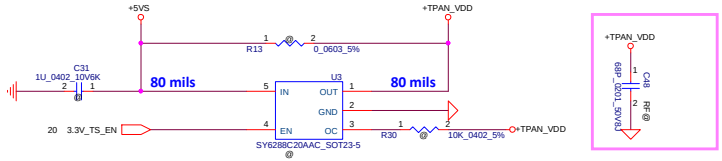
Main Func = CAM

EE note: Never change R16 to short pad after MP



Main Func = TS





Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: LCD/Camera/Mic

Size | Document Number: LA-F611P | Rev: 0.3

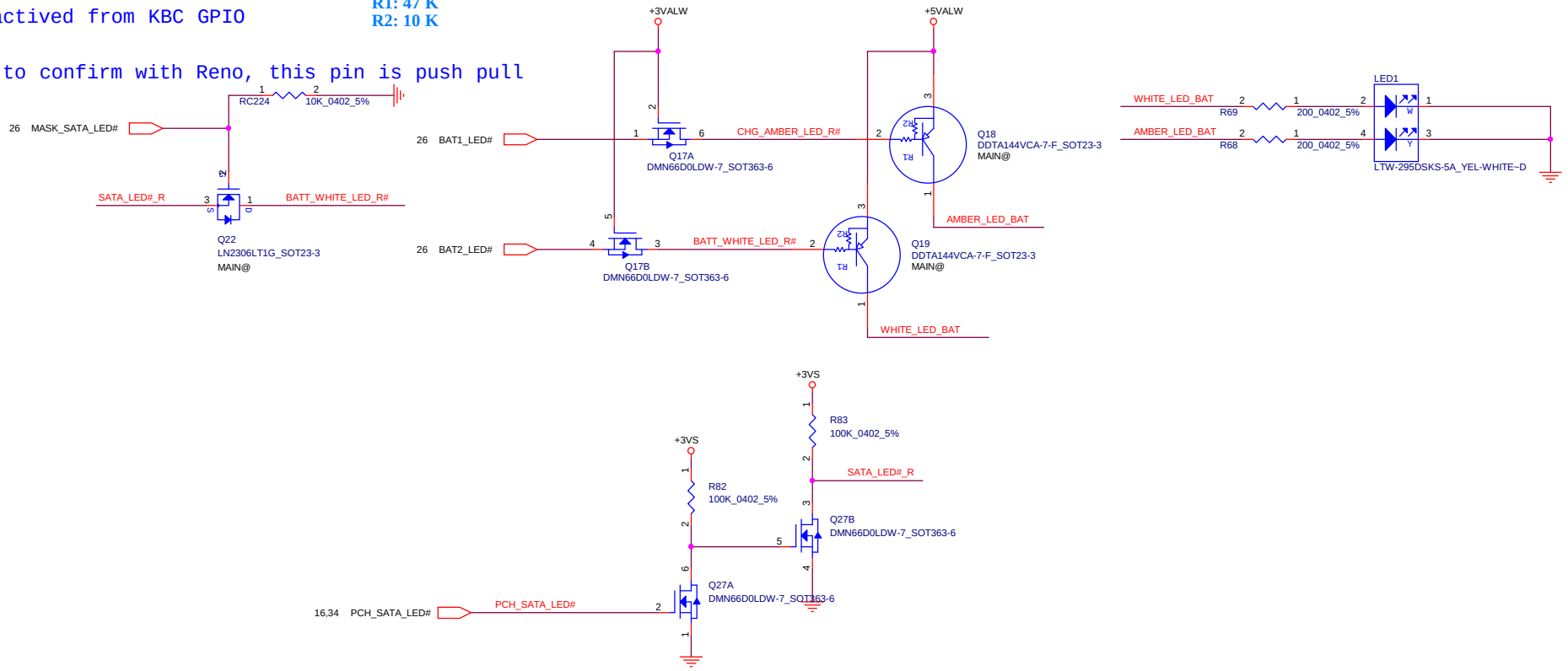
Date: Thursday, March 22, 2018 | Sheet 29 of 78

Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K

Need to confirm with Reno, this pin is push pull



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Power Button/LED**

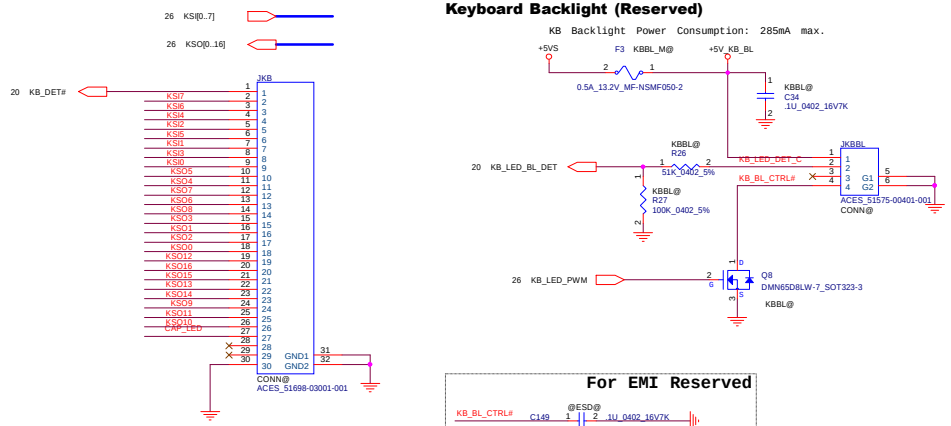
Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 30 of 78

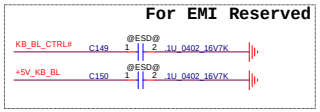
Main Func = KB

Keyboard Backlight (Reserved)

KB Backlight Power Consumption: 285mA max.

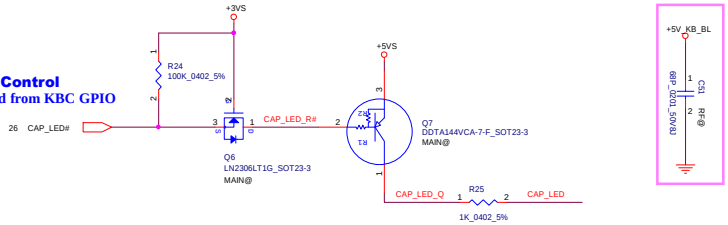


For EMI Reserved



CAP LED Control

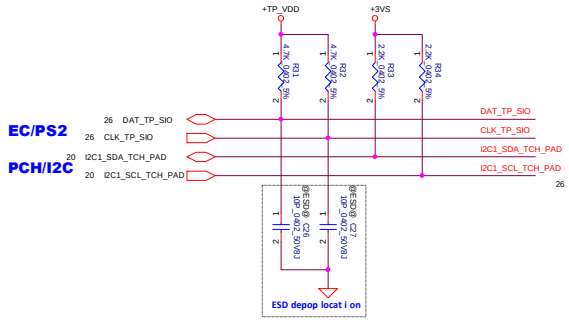
LOW actived from KBC GPIO

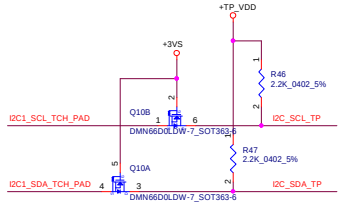


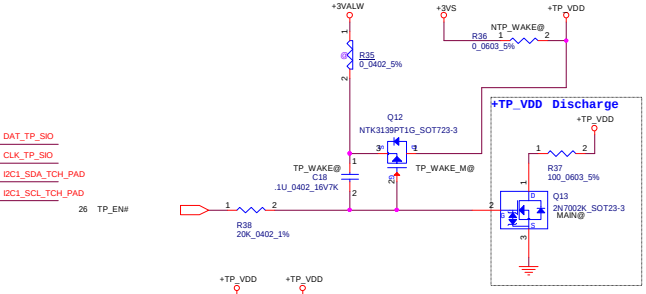
Main Func = TPAD

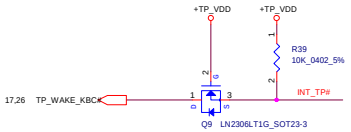
EC/PS2

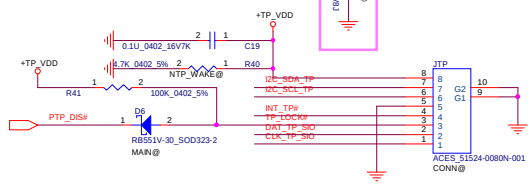
PCH/I2C







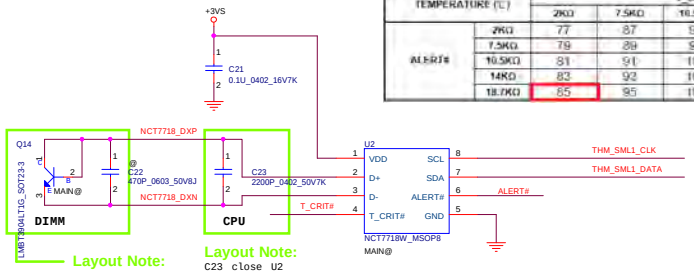




Main Func = Thermal

TEMPERATURE (℃)	T_CRIT# 2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
2KΩ	77	87	97	107	117
7.5KΩ	79	89	99	109	119
10.5KΩ	81	91	101	111	121
14KΩ	83	92	103	113	123
18.7KΩ	85	95	105	115	125

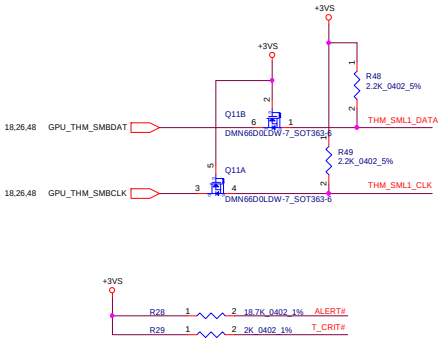
ALERT#



Layout Note:

Layout Note:
C23 close U2

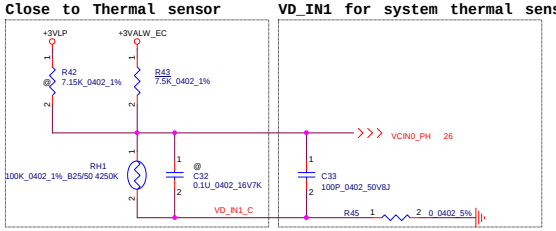
DXN and DXP routing width and spacing is 10 mil / 10 mil.



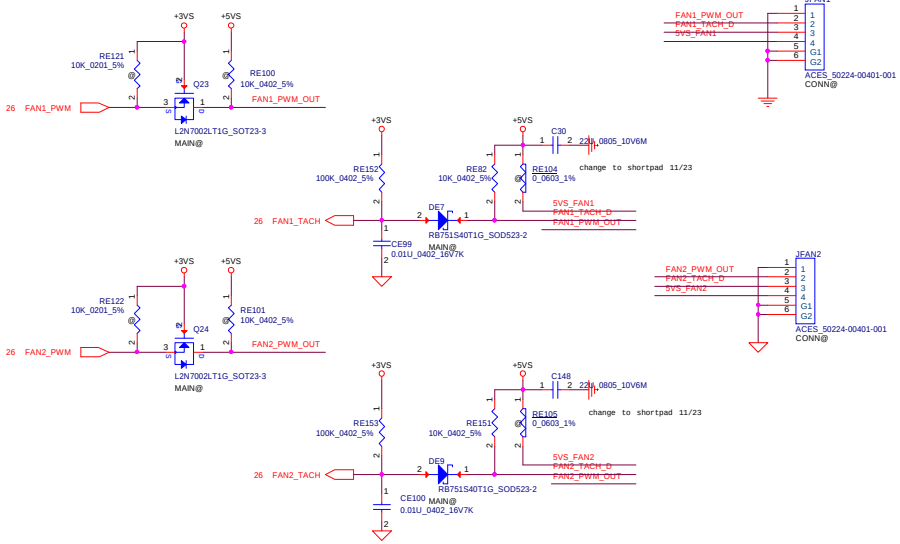
Main Func = OTP

Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor



PWM FAN



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

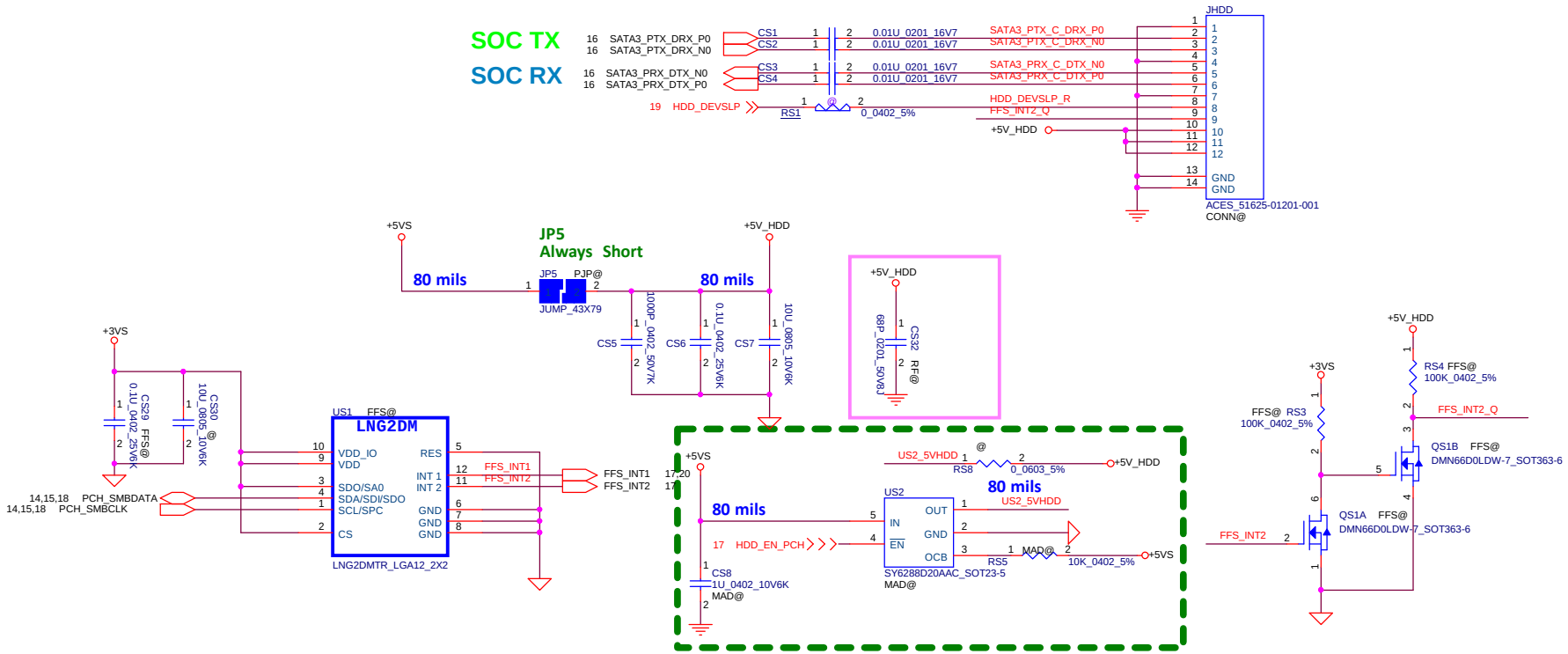
Compal Electronics, Inc.

Title: KB/KBBL/TP/Thermal/FAN

Size: Document Number: LA-F611P Rev: 0.3

Date: Thursday, March 22, 2018 Sheet 31 of 78

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

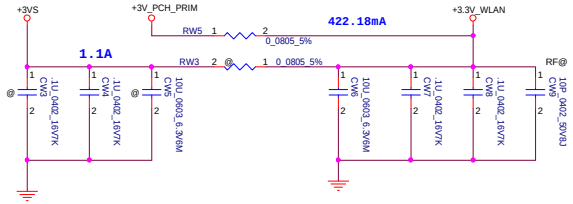
Compal Electronics, Inc.

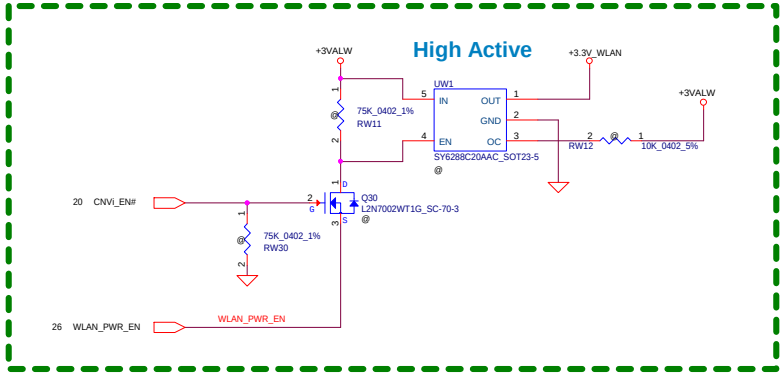
Title: **HDD/FFS**

Size | Document Number: **LA-F611P** | Rev: 0.3

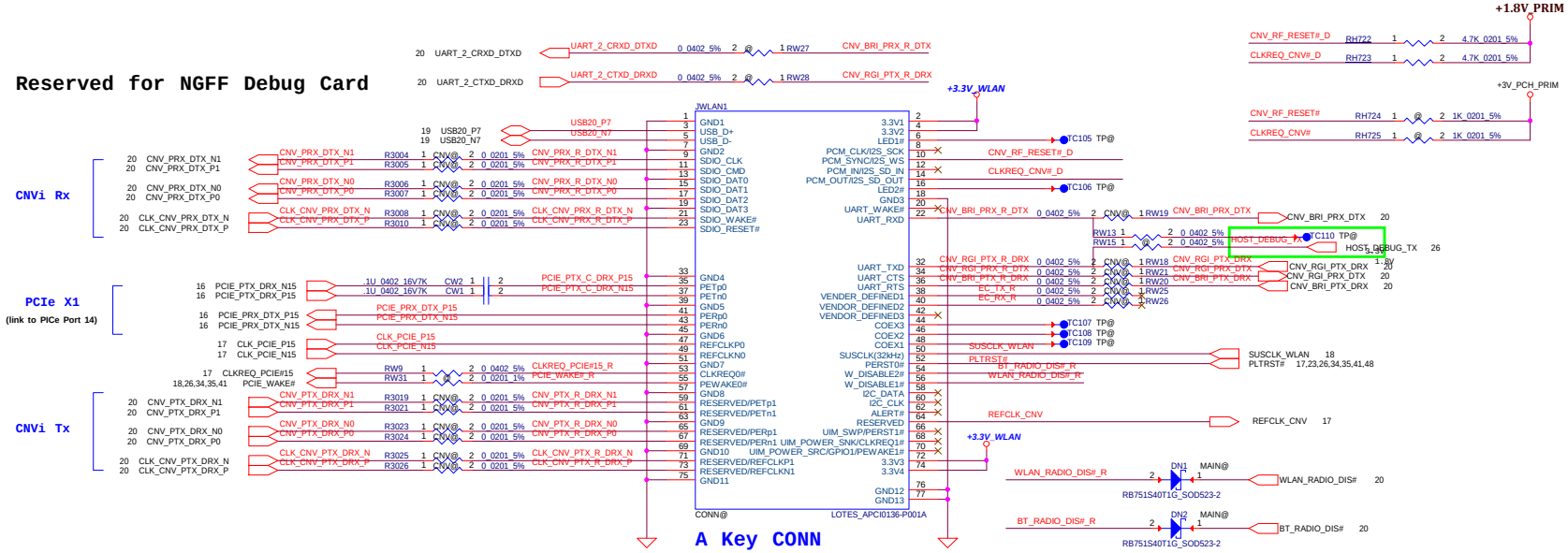
Date: Thursday, March 22, 2018 | Sheet 32 of 78

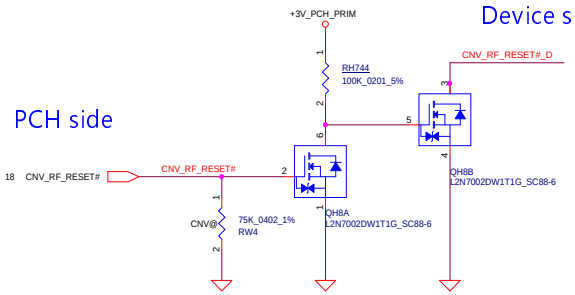
Main Func = WLAN / CNVi

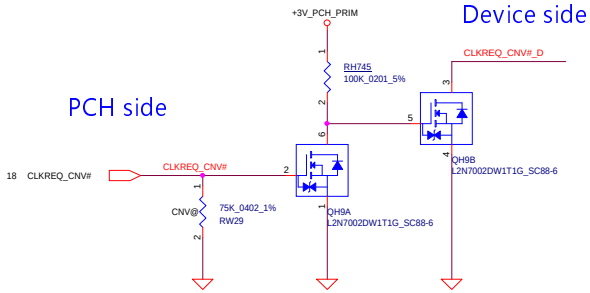




Reserved for NGFF Debug Card







Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **NGFF WLAN**

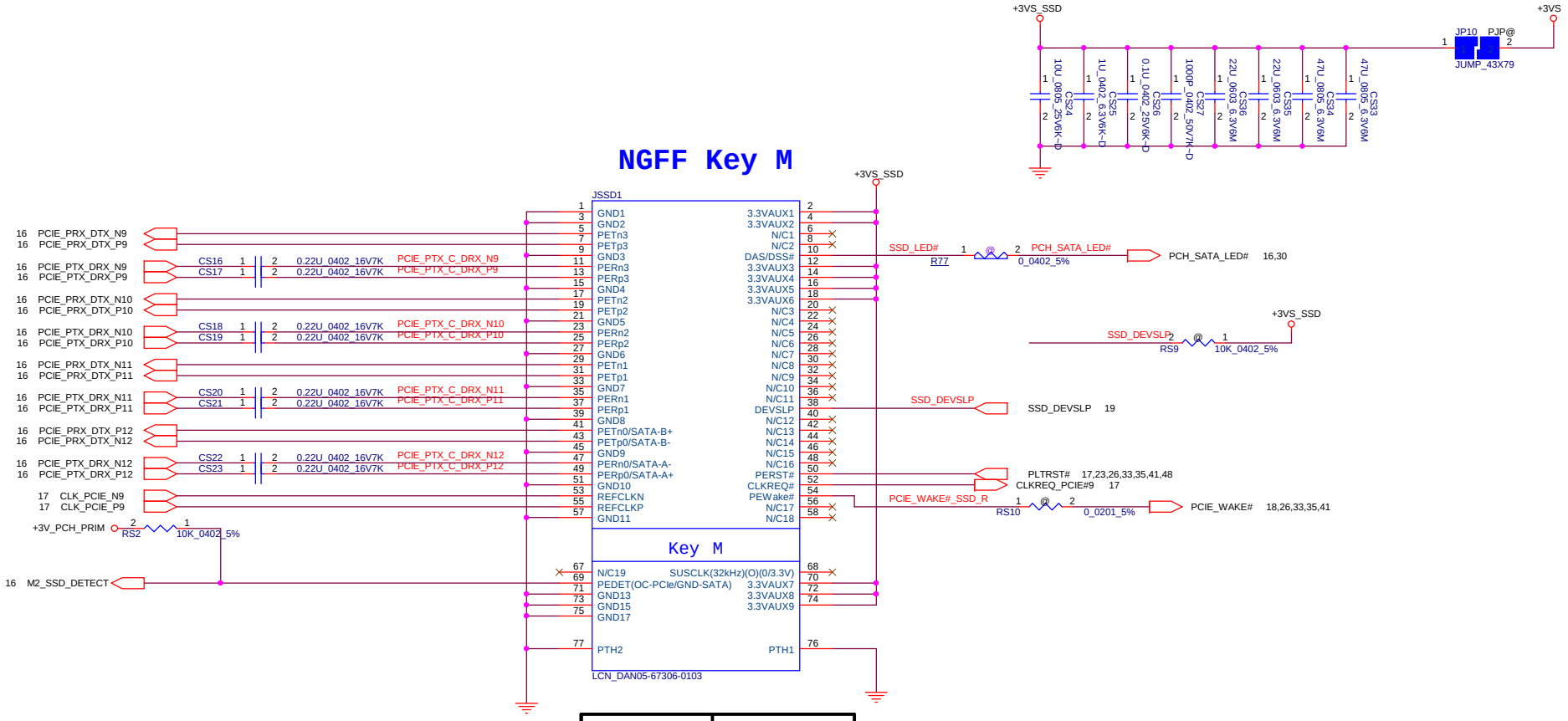
Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 33 of 78

Main Func = SSD

M Key CONN

Update OK



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: NVMe SSD

Size | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 34 of 78

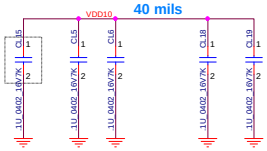
Main Func = LAN

Update OK

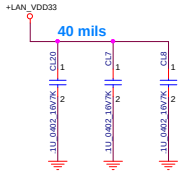
Layout:
For RTL8111H-CG
* Place CL5,CL6,CL18,CL19 close to each VDD10 pin 8, 30, 3, 22
For RTL8106E
* Place CL5,CL6 close to each VDD10 pin 8, 30

CL5: close to Pin8
CL6: close to Pin30
CL18: close to Pin3
CL19: close to Pin22

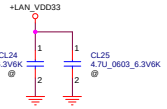
CL15, RL1:
Only for
RTL8111 LDO mode.



Layout:
For RTL8111H-CG
* Place CL20 and CL7 and CL8 close to each VDD33 pin 11, 32 ,23
For RTL8106E
* Place CL7 and CL8 close to each VDD33 pin 23, 32

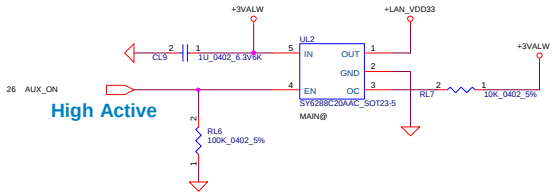


CL8: close to Pin23
CL20: close to Pin11
CL7: close to Pin32



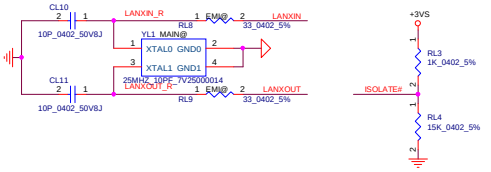
Layout:
CL24: close to Pin32
CL25: close to Pin11

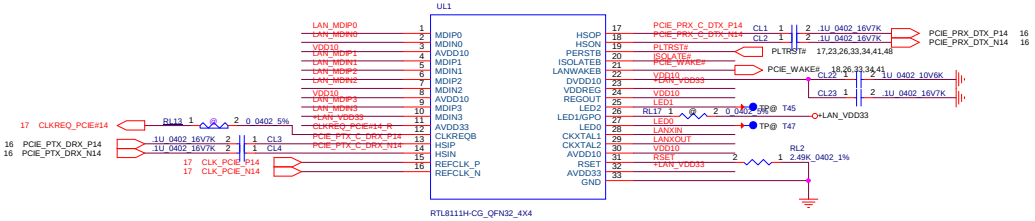
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



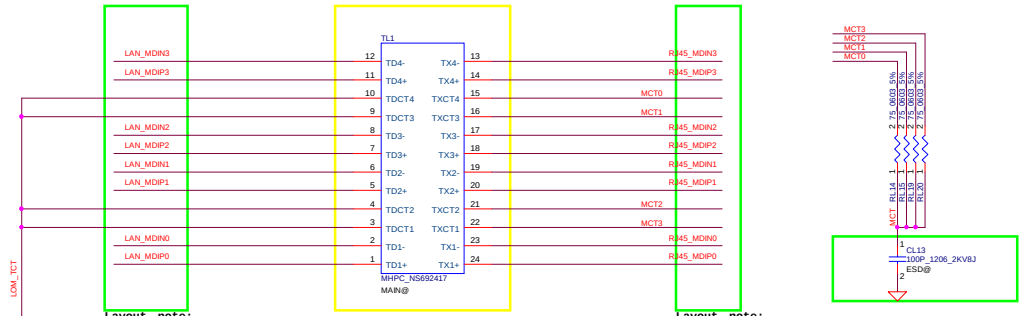
LAN Chip (10/100/1000M & 10/100M co-layout)

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M





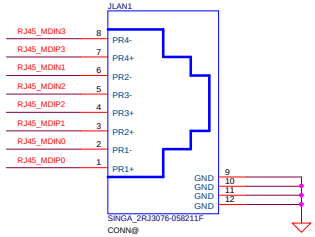
LAN TransFormer (10/100/1000M & 10/100M co-layout)



Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.

	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: LAN RTL8111

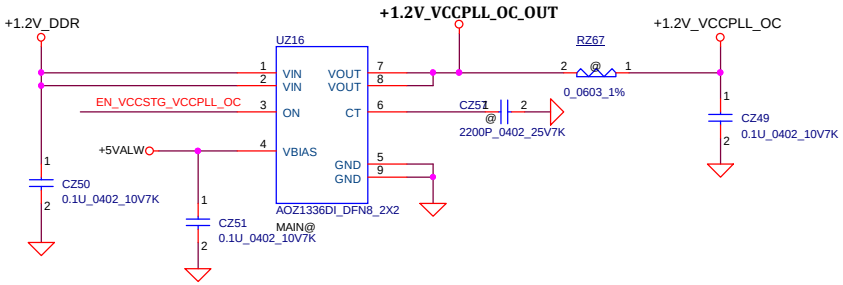
Size | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 35 of 78

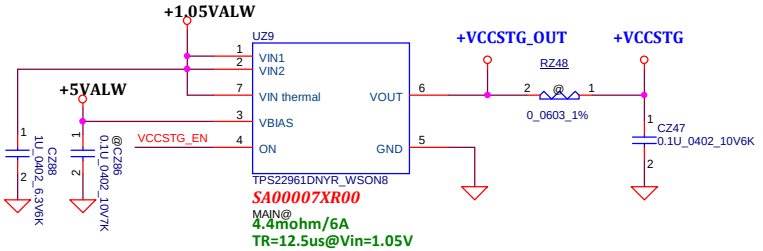
Main Func = DC/DC

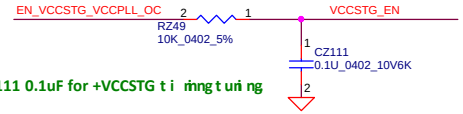
+VCCPLL_OC Load Switch

H-Processor Line - Quad Core GT2
Max : 130 mA



+VCCSTG Load Switch

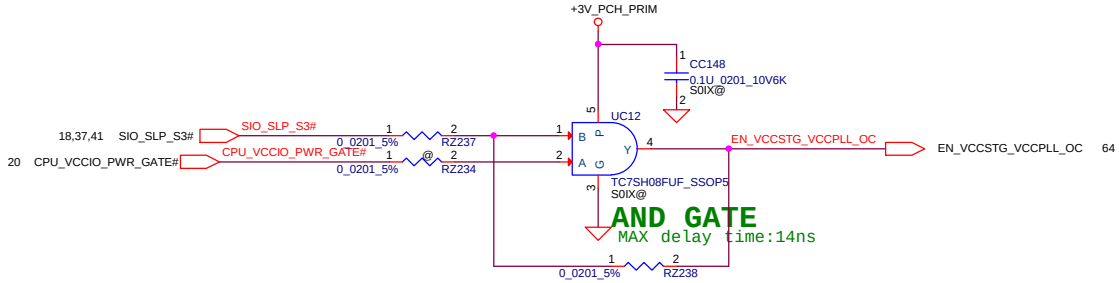




DVT1.
Add RZ49 10K, CZ111 0.1uF for +VCCSTG t i ming t uni ng

Power Gating by Modern Standby Control

+1.05VALW TO +1.0VS_VCCSTG



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

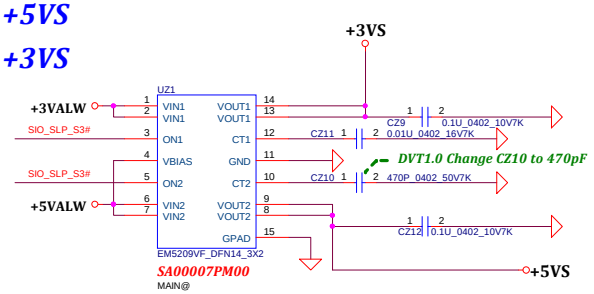
Title: DC/DC(1/2)

Size | Document Number: LA-F611P | Rev: 0.3

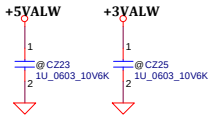
Date: Thursday, March 22, 2018 | Sheet 36 of 78

Main Func = DC/DC

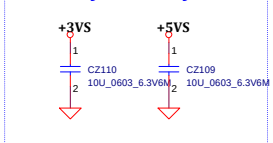
+5VALW to +5VS
+3VALW to +3VS

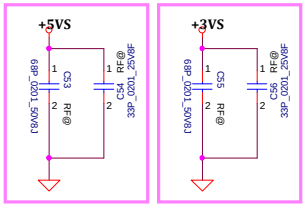


Close UZ1

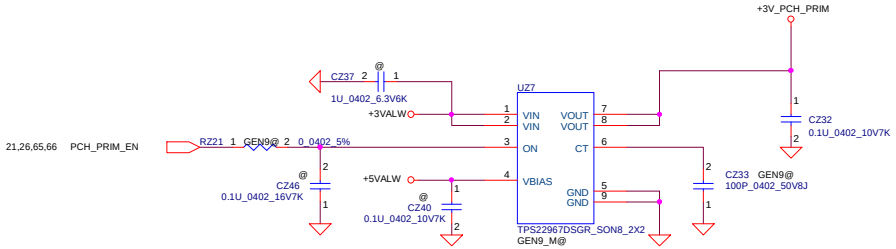


Close JPZ1 and JPZ2

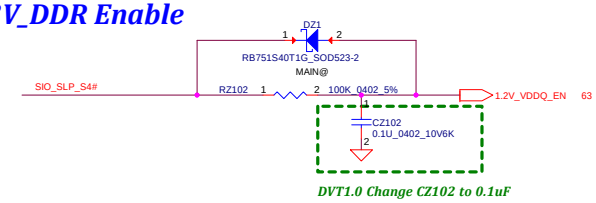




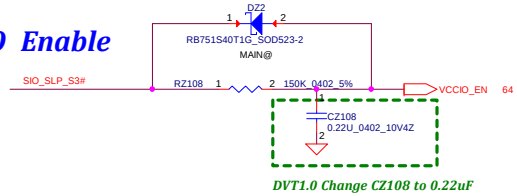
+3V_PCH_PRIM Load Switch



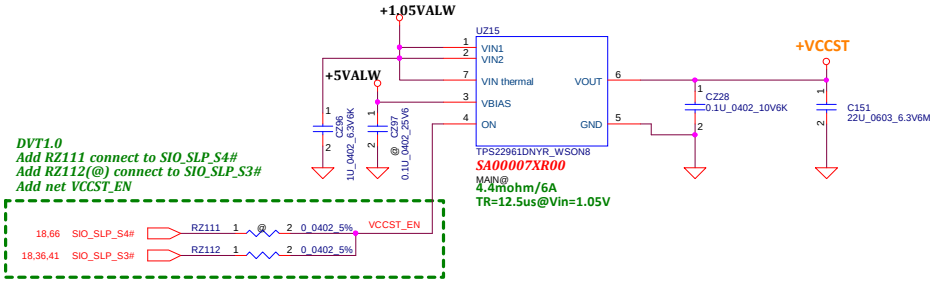
+1.2V_DDR Enable



+VCCIO Enable



+VCCST Load Switch



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

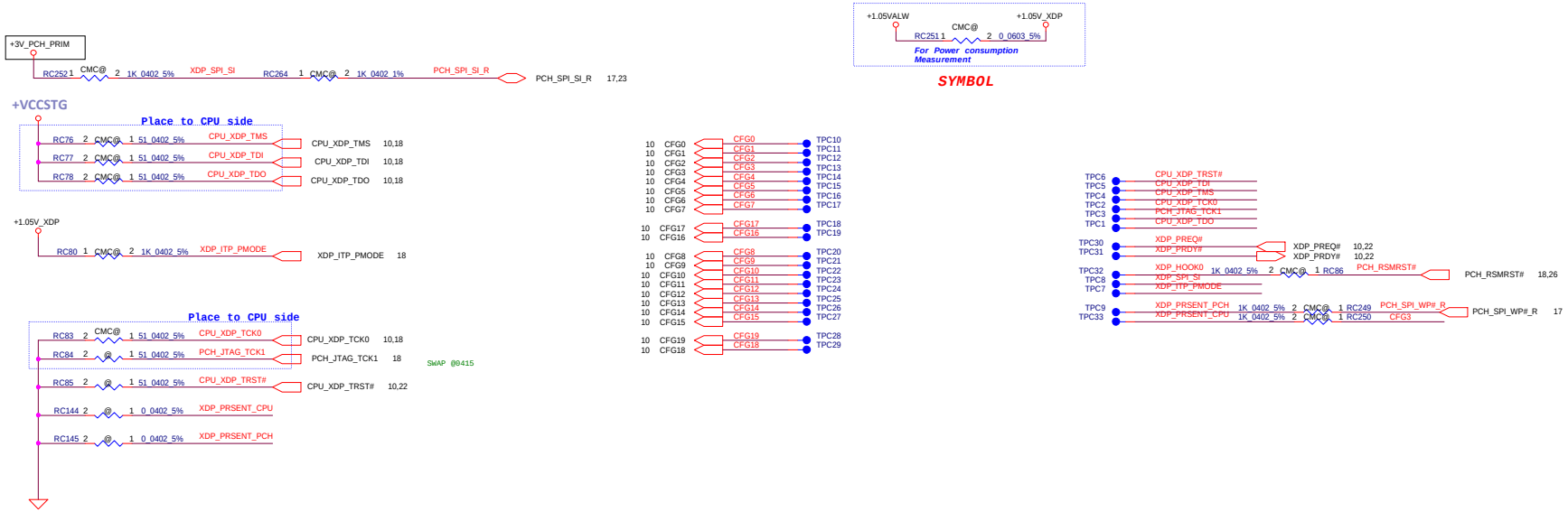
Title: **DC/DC(2/2)**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 37 of 78

Main Func = CMC

PRIMARY CMC CONN.



Compal Electronics, Inc.

Title: CMC

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 38 of 78

Main Func = Reserved

Reserved

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title	Reserved	
Size	Document Number	Rev
	LA-F611P	0.3
Date:	Thursday, March 22, 2018	Sheet 39 of 78

Main Func = PD + TYPE C

Update OK

+3VALW_PD

+3VALW

+5VALW

60mil 3A

60mil 3A

+TBTA_VBUS

Change DT1 and add DT15 follow E-team's design for DELL dat.04/07

Close to UT4

Co-Lay PCH USB2.0 for AR USB2 issue

+3.3V_TBT_SX

+3VS

Master0: 0 ohm
Slave1:93.1K ohm

+3VALW_PD

DVT1.0
Change net INT#_TYPEC to UPD_SMBINT#

Change RT123.2 connect to net PD_EE_CLK_R

+3.3V_FLASH

+3.3V_TBT_SX_R

+3.3V_TBT_SX

+TBTA_VBUS

+3.3V_FLASH

Differential Signal

DVT1.0
Un-pop RT102

SA0000AX700

SN161004ZQZR BGA 96P_BGA96

BUSPOWERZ
Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kohm resistor to disable PP_EXT power path during dead-battery or no-battery boot conditions.

TBTA_HRESET might be connected to EC or PCH to allow TPS65982 FW load

Active high hardware reset input. Will re-load settings from optional external flash memory. Ground pin when HRESET functionality will not be used.

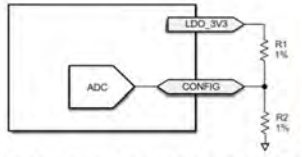
DVT1.0
Add RT125(3.3K), RT126(3.3K), RT127(3.3K), RT128(3.3K), UT5, CT117(0.1u)

Close UT3

SA00003GM30

W25X20CLSNIG_SO8

c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).



If External SPI Connected use "Infinite Retry" Setting by pulling CONFIG (GPIO 8) to LDO_3V3

Figure 78. Factory Configuration Resistor Divider

Table 13. Factory Device Configuration Selection

DIV = R2/(R1+R2)(1)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

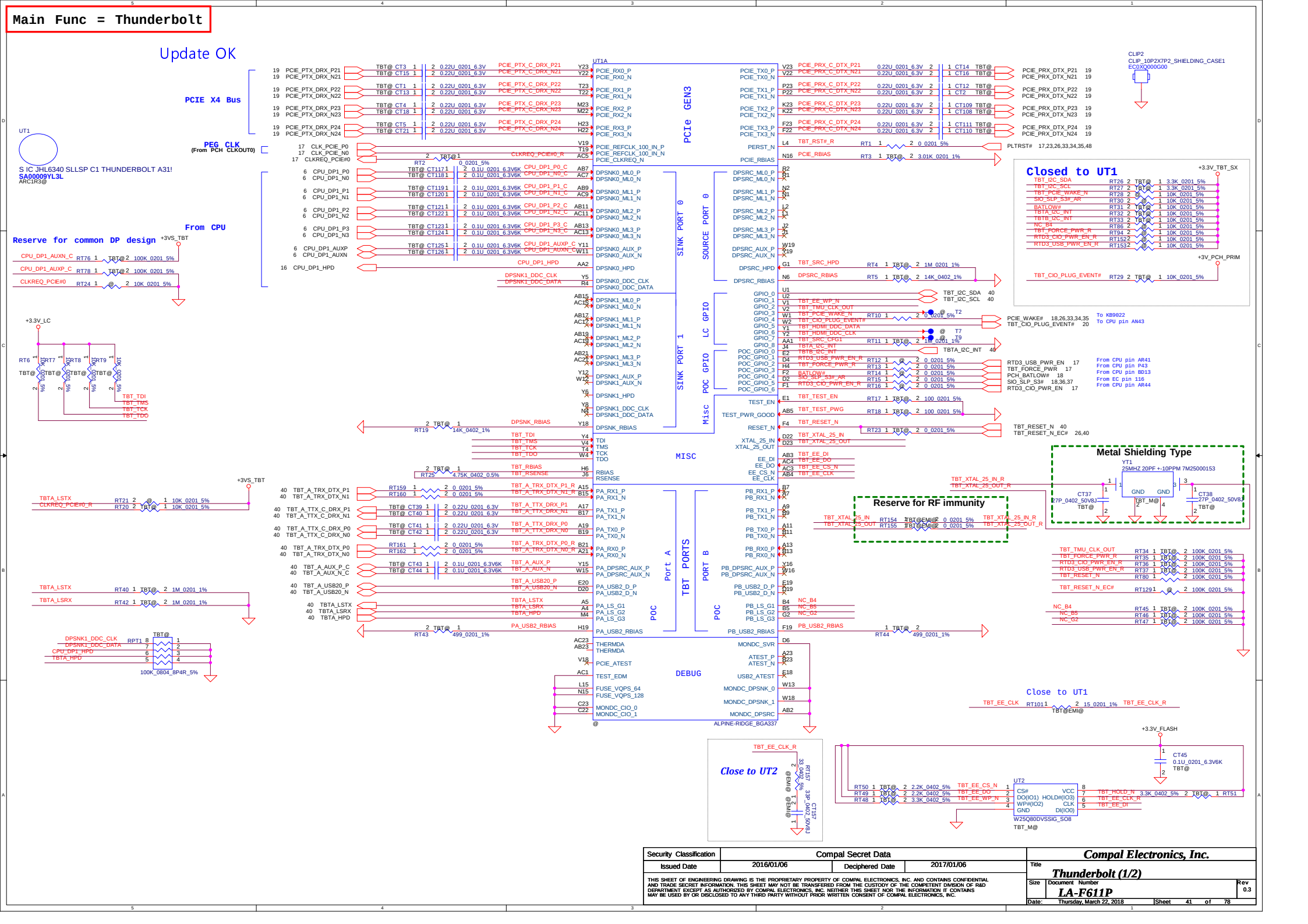
Title: PD+USB3.1 TypeC

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 40 of 78

Main Func = Thunderbolt

Update OK



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Thunderbolt (1/2)**

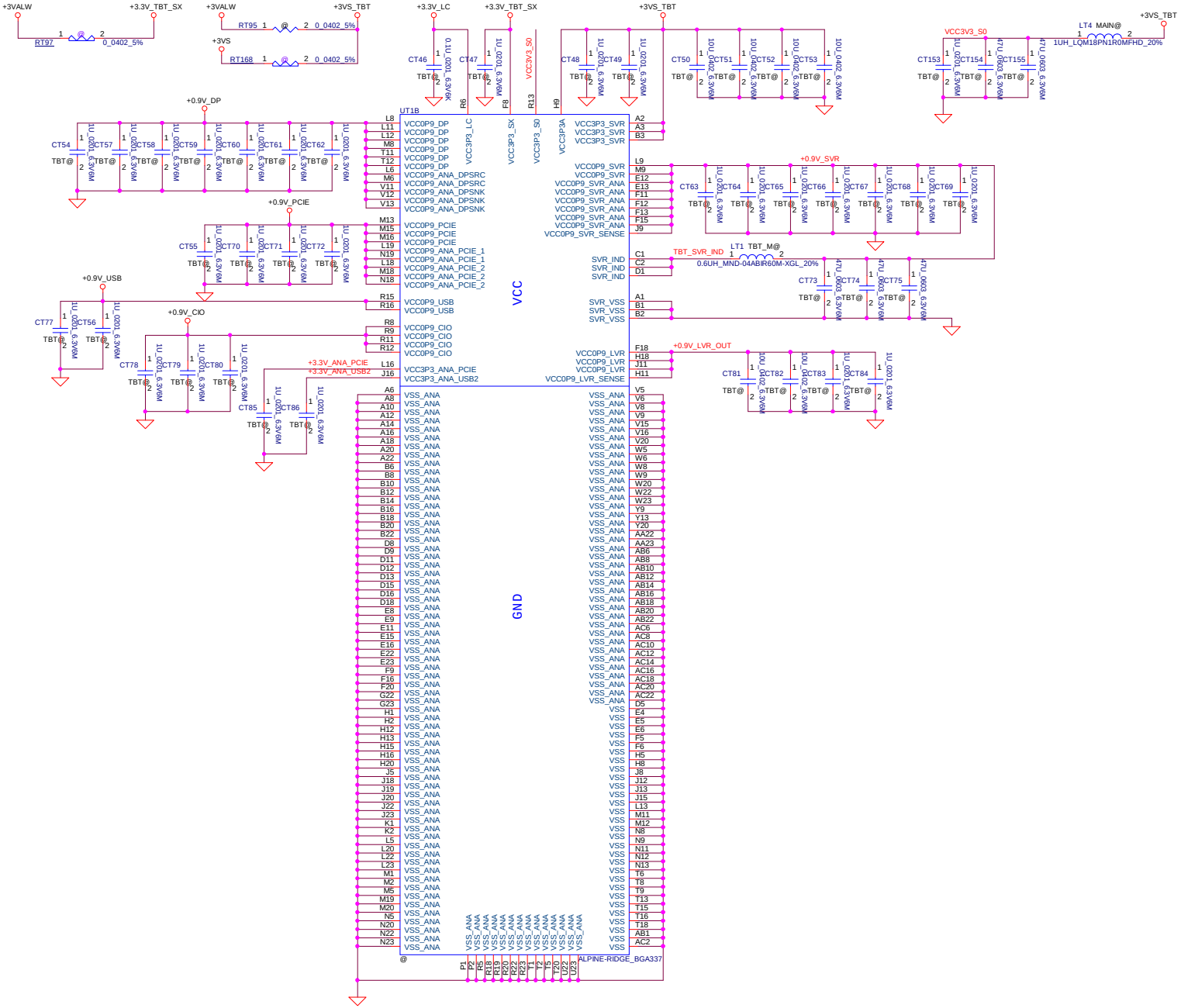
Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 41 of 78

Main Func = Thunderbolt

Delete RT104 for layout @12/31

Delete RT52 for layout @12/31



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

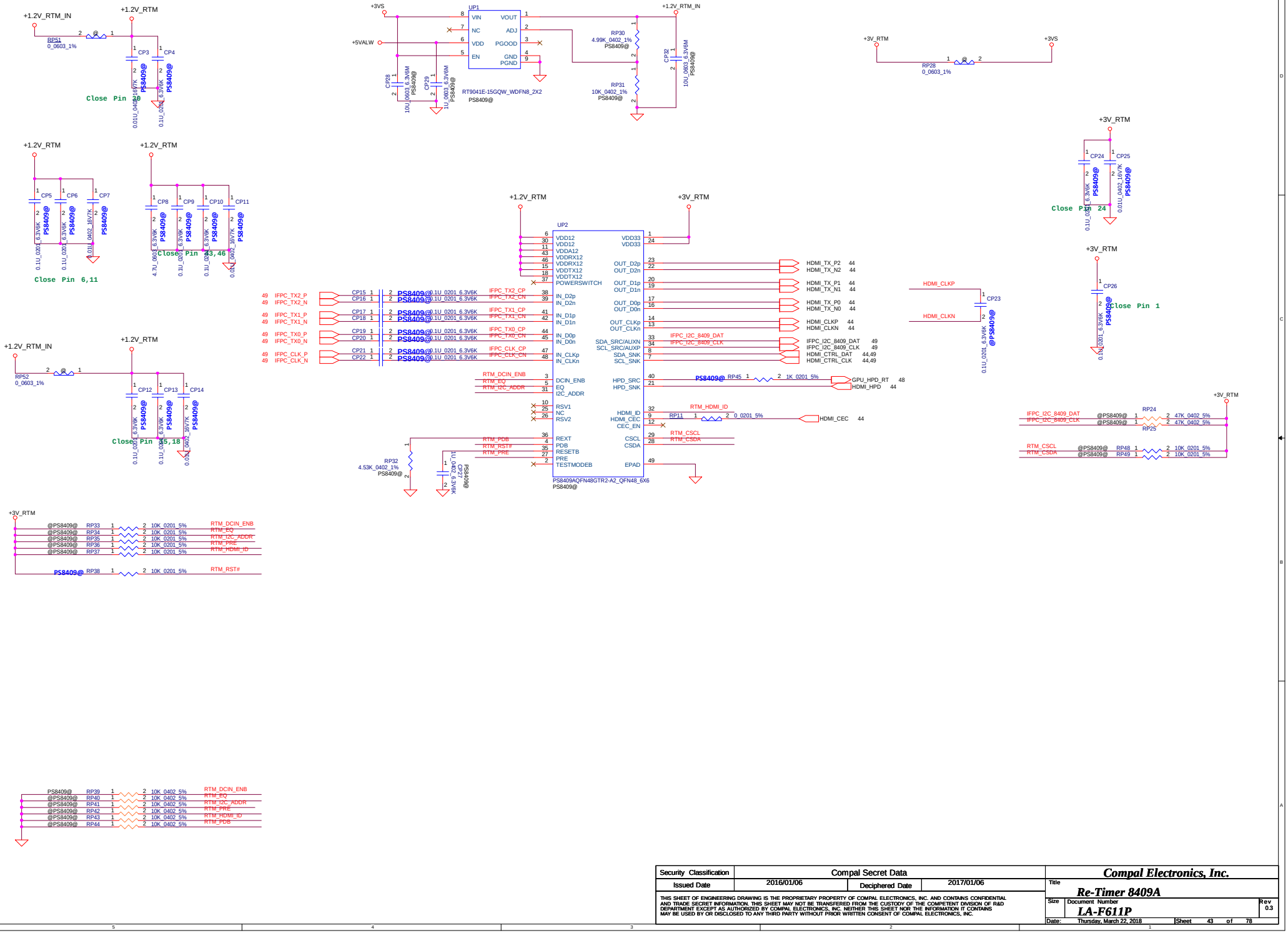
Compal Electronics, Inc.

Title: **Thunderbolt (2/2)**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 42 of 78

Main Func = Retimer



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Re-Timer 8409A**

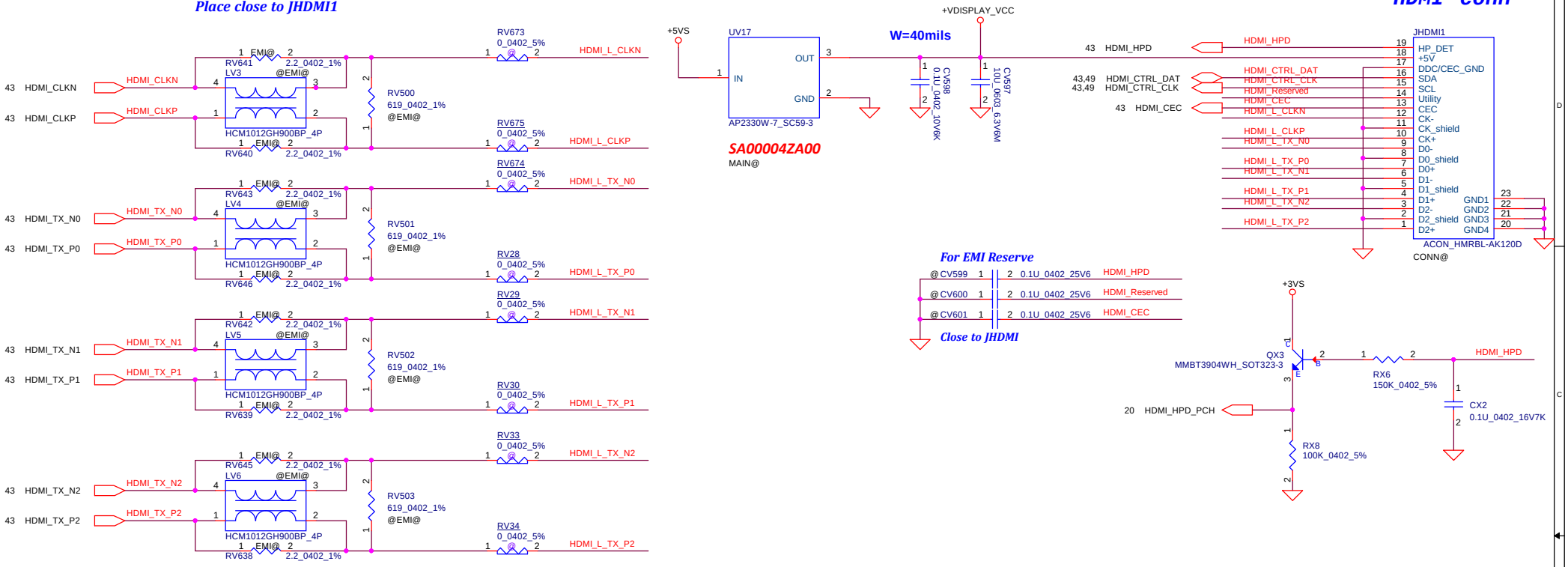
Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 43 of 78

Main Func = HDMI

Place close to JHDMI1

HDMI conn



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-F611P** | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 44 of 78

Main Func = 2nd source list

UG25 2ND@ SA00001OF00 S IC TC7SZ32FU SSOP 5P OR 0.65A
UG27 2ND@ SA00001OF00 S IC TC7SZ32FU SSOP 5P OR 0.65A

UG22 2ND@ SA00001DG90 S IC TC7SZ08FU SSOP 5P AND
UG31 2ND@ SA00001DG90 S IC TC7SZ08FU SSOP 5P AND
UV14 2ND@ SA00001DG90 S IC TC7SZ08FU SSOP 5P AND
UV19 2ND@ SA00001DG90 S IC TC7SZ08FU SSOP 5P AND
UV20 2ND@ SA00001DG90 S IC TC7SZ08FU SSOP 5P AND

UE2 2ND@ SA00004H300 S IC TC7SZ05FU SSOP 5P INVERTER OD

UV17 2ND@ SA000080300 S IC G5250Q1T73U SOT-23 3P POWER SWITCH

UG12 2ND@ SA00007QK00 S IC G5016KD1U TDFN2X3 14P LOAD SWITCH

UZ16 2ND@ SA00009PI00 S IC FA7607OTR DFN 8P LOAD SWITCH

UZ7 GEN9_2@ SA00009PI00 S IC FA7607OTR DFN 8P LOAD SWITCH

U1 2ND@ SA00008R900 S IC EM5203AJ-20 SOT23 5P LOAD SWITCH
UL2 2ND@ SA00008R900 S IC EM5203AJ-20 SOT23 5P LOAD SWITCH

UU1 2ND@ SA00008RA00 S IC EM5203J-20 SOT23 5P LOAD SWITCH
UU3 2ND@ SA00008RA00 S IC EM5203J-20 SOT23 5P LOAD SWITCH

UZ1 2ND@ SA00007QK00 S IC G5016KD1U TDFN2X3 14P LOAD SWITCH

UC10 2ND@ SA00005U600 S IC 74AUP1G07GW TSSOP 5P BUFFER
UC16 2ND@ SA00005U600 S IC 74AUP1G07GW TSSOP 5P BUFFER

UZ9 2ND@ SA00008A800 S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW
UZ15 2ND@ SA00008A800 S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW

UH3 2ND@ SA007080180 S IC SN74AHC1G08DCKR SC-70 5P AND

DU2 ESD_2@ SCA00001L00 S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD
DU4 ESD_2@ SCA00001L00 S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD

Q1 2ND@ SB00000M700 S TR ME2N7002D-G 1N SOT-23-3 ESD 2KV
Q13 2ND@ SB00000M700 S TR ME2N7002D-G 1N SOT-23-3 ESD 2KV

Q12 TP_WAKE_2@ SB00000PJ00 S TR DMG2301U-7 1P SOT23-3

Q14 2ND@ SB000006A00 S TR MMBT3904 NPN SOT23-3 T/R-3K

D1 2ND@ SCS00009E00 S SCH DIO LBAS40-05LT1G SOT23

YV1 N17P_2@ SJ10000B300 S CRYSTAL 27MHZ 10PF X3G027000BA1H-U

Q25 GEN9_2@ SB00000UO00 DMN65D8LW-7 1N SOT323-3

D7 GEN9_2@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DC2 GEN9_2@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DV9 N17P_2@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DV11 N17P_2@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2

DE7 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DE9 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DG3 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DG4 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DG7 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2

DG10 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DH2 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DN1 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DN2 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DZ1 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2
DZ2 2ND@ SCS00008100 S SCH DIO LRB521S-40T1G SOD523-2

YL1 2ND@ SJ10000DE00 S CRYSTAL 25MHZ 10PF X3G025000DA1H-X

YE1 2ND@ SJ10000SX00 S CRYSTAL 32.768KHZ 9PF EXS00A-MU00688

F1 2ND@ SP040001G00 S FUSE 1812L150/24MR 1.5A 24V UL/TUV

TL1 2ND@ SP050006P00 S XFORM_ IH-115-F LAN

CD27 2ND@ SGA00002680 S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9

DU1 ESD_2@ SC300001Y00 AZ1045-04F
DU3 ESD_2@ SC300001Y00 AZ1045-04F

DA5 ESD_2@ SCA00003400 S ZEN ROW L18E3V3CC3-2C 3P C/A SOT-23

DA4 ESD_2@ SCA00002M00 MESC5V02BD03
DA7 ESD_2@ SCA00002M00 MESC5V02BD03

RA13 EMI_2@ SM01000NX00 S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA14 EMI_2@ SM01000NX00 S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA15 EMI_2@ SM01000NX00 S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA16 EMI_2@ SM01000NX00 S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402

L5 EMI_2@ SM01000Q500 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402

LA1 ESD_2@ SM01000OZ00 S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA2 ESD_2@ SM01000OZ00 S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA3 ESD_2@ SM01000OZ00 S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA4 ESD_2@ SM01000OZ00 S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402

L3 EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U
LU1 EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U
LU4 EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U
LU8 EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U
LU9 EMI_2@ SM070004400 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402

LT2 TBT@EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U
LT3 TBT@EMI_2@ SM070004400 S COM FI_ PANASONIC EXC24CQ900U

Q7 2ND@ SB00001H300 S TR LDTA144VLT1G PNP SOT23-3
Q18 2ND@ SB00001H300 S TR LDTA144VLT1G PNP SOT23-3
Q19 2ND@ SB00001H300 S TR LDTA144VLT1G PNP SOT23-3

D6 2ND@ SCS00007H00 S SCH DIO LRB551V-30T1G SOD323-2

DT2 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT3 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT4 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT5 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT6 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT7 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT8 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF
DT9 TBT@ESD_2@ SC40000DM00 PESD5V0C1BSF

QV10 2ND@ SB000013D00 S TR BSS138PS 2N SC88-6

QG502 2ND@ SB00001DD00 S TR PJT138K 2N SOT363-6
QG503 2ND@ SB00001DD00 S TR PJT138K 2N SOT363-6
QG504 2ND@ SB00001DD00 S TR PJT138K 2N SOT363-6
QG505 2ND@ SB00001DD00 S TR PJT138K 2N SOT363-6

QV1 N17P_2@ SB00001DD00 S TR PJT138K 2N SOT363-6

LT1 TBT_2@ SH00001BK00 S COIL 0.6UH TMPC404012HB-R60MG-Z02 6.6A

LT4 2ND@ SHI0000NV00 S INDUC_ 1UH +-20% CPI160809UF-1R0M-0A7

LG8 N17P_2@ SM01000HU00 S SUPPRE_ TAI-TECH HCB1608KF-300T20 0603

UH14 2ND@ SA007080120 S IC TC7SH08FU SSOP 5P AND
UZ21 2ND@ SA007080120 S IC TC7SH08FU SSOP 5P AND

U2 2ND@ SA007810140 S IC G781P8F MSOP 8P TEMP. SENSOR

Q6 2ND@ SB00000QM00 S TR AP2324GN-HF 1N SOT-23-3
Q9 2ND@ SB00000QM00 S TR AP2324GN-HF 1N SOT-23-3
Q22 2ND@ SB00000QM00 S TR AP2324GN-HF 1N SOT-23-3
QA1 2ND@ SB00000QM00 S TR AP2324GN-HF 1N SOT-23-3

F3 KBBL_2@ SP040006R00 S FUSE 1206L050/15YR 0.5A 15V UL/TUV

QV3 N17P_2@ SB00000S700 S TR MESS138W-G 1N SOT323-3
QV20 N17P_2@ SB00000S700 S TR MESS138W-G 1N SOT323-3
QV21 N17P_2@ SB00000S700 S TR MESS138W-G 1N SOT323-3

Q23 2ND@ SB00000EN00 S TR 2N7002K 1N SOT23-3 PANJIT
Q24 2ND@ SB00000EN00 S TR 2N7002K 1N SOT23-3 PANJIT

Q26 GEN9_2@ SB00000T900 S TR PJ2301 1P SOT23-3

QH4 2ND@ SB00000PV00 S TR L2N7002DW1T1G 2N SC88-6

QG23 N17P_2@ SB00001FN00 S TR LBSS139DW1T1G 2N SOT-363-6 ESD

DT10 TBT@ESD_2@ SC300002C00 S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD
DT11 TBT@ESD_2@ SC300002C00 S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD

LV7 N17P_2@ SM01000NV00 S SUPPRE_ TAI-TECH HCB1005KF-300T25 0402
LV13 N17P_2@ SM01000NV00 S SUPPRE_ TAI-TECH HCB1005KF-300T25 0402

YH2 CH47 CH48 2nd X76 control
X7676731L78

YH2 XTAL_2@ SJ10000YS00 S CRYSTAL 24MHZ 12PF X3S024000BC1H-HU
CH47 XTAL_2@ SE071120J80 S CER CAP 12P 50V J NPO 0402
CH48 XTAL_2@ SE071120J80 S CER CAP 12P 50V J NPO 0402

UT2 TBT_2@ SA000041O00 S IC FL 8M MX25L8006EM2I-12G SOP 8P 3V

QG10 N17P_2@ SB00001GC00 S TR LBSS139WT1G 1N SC70-3

DT16 ESD_2@ SCA00000R00 S ZEN ROW PESD24VS2UT 3P C/A SOT23

DA8 2ND@ SCS00009K00 S SCH DIO BAT54AT-7-F SOT-523

YH1 CH45 CH46 2nd X76 control
X7676731L92

YH1 XTAL_2@ SJ10000SX00 S CRYSTAL 32.768KHZ 9PF EXS00A-MU00688
CH45 XTAL_2@ SE07168AC80 S CER CAP 6.8P 50V C NPO 0402
CH46 XTAL_2@ SE07168AC80 S CER CAP 6.8P 50V C NPO 0402

YT1 TBT_2@ SJ10000U200 S CRYSTAL 25MHZ 20PF X3S025000BK1H-CHV

UH15 2ND@ SA0000A8J10 S IC FL 128M GD25B127DSIGR SOP 8P SPI

UT3 PD_2@ SA00007XO10 S IC FL 2M GD25Q20CTIGR SOP 8P SPI ROM

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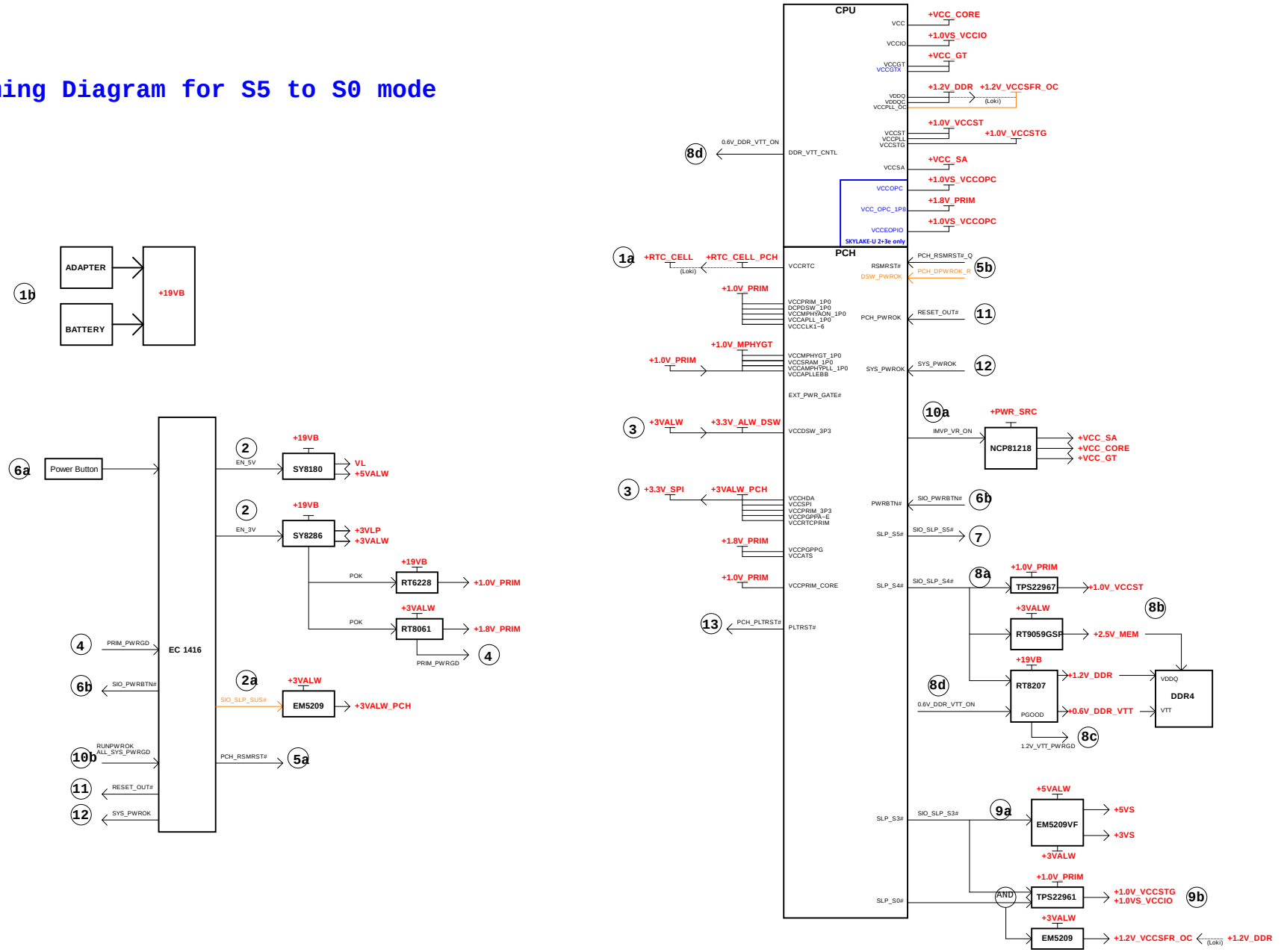
				Date: Thursday, March 22, 2018 / Sheet 45 of 78

Timing Diagram for S5 to S0 mode



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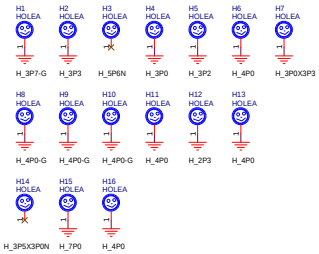
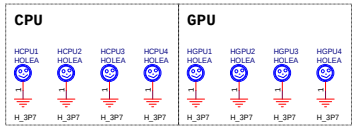
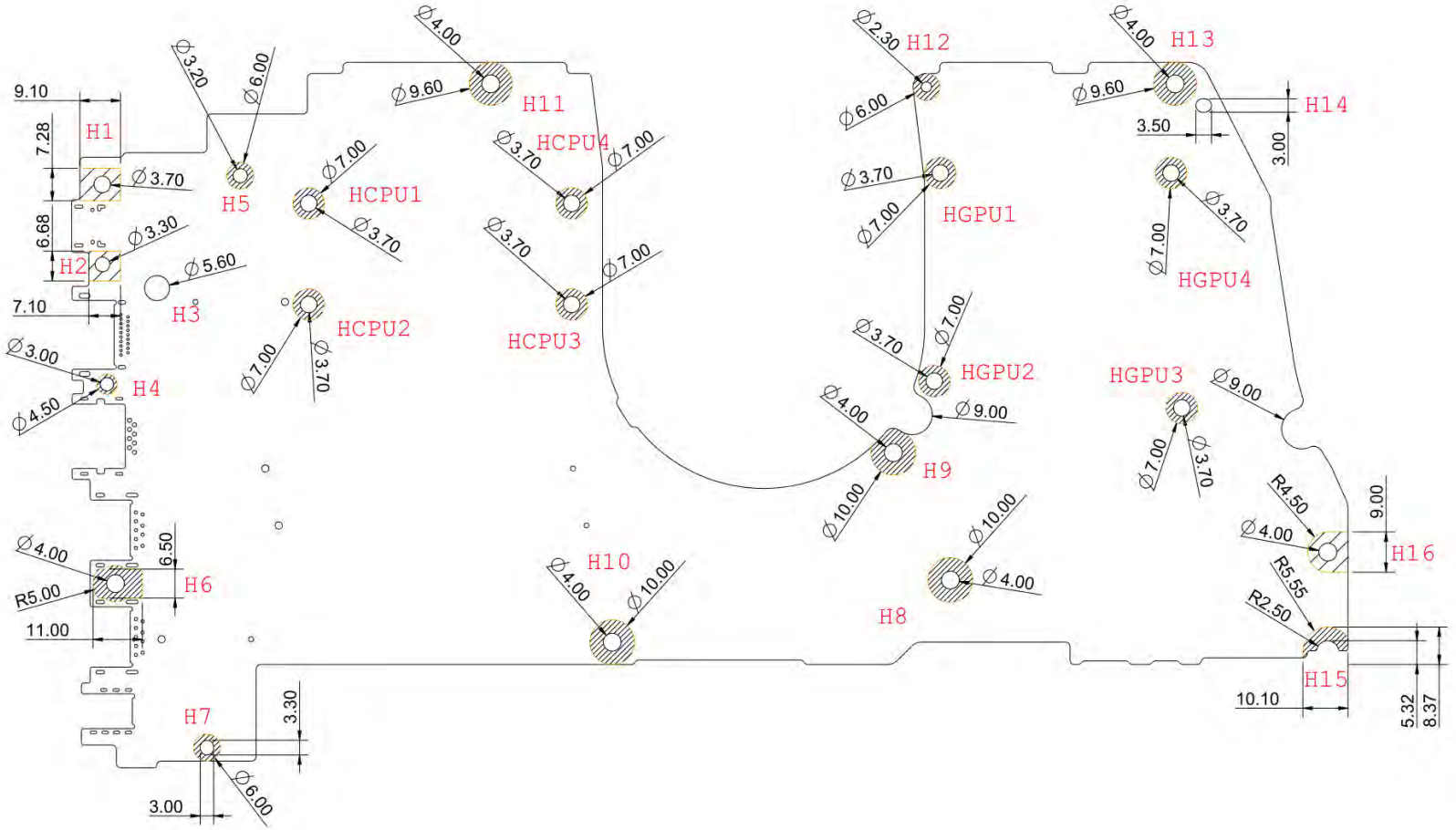
			Size: Document Number: LA-F611P Rev: 0.3
			Date: Thursday, March 22, 2018 Sheet 46 of 78

Main Func = Screw hole

Screw hole/FD



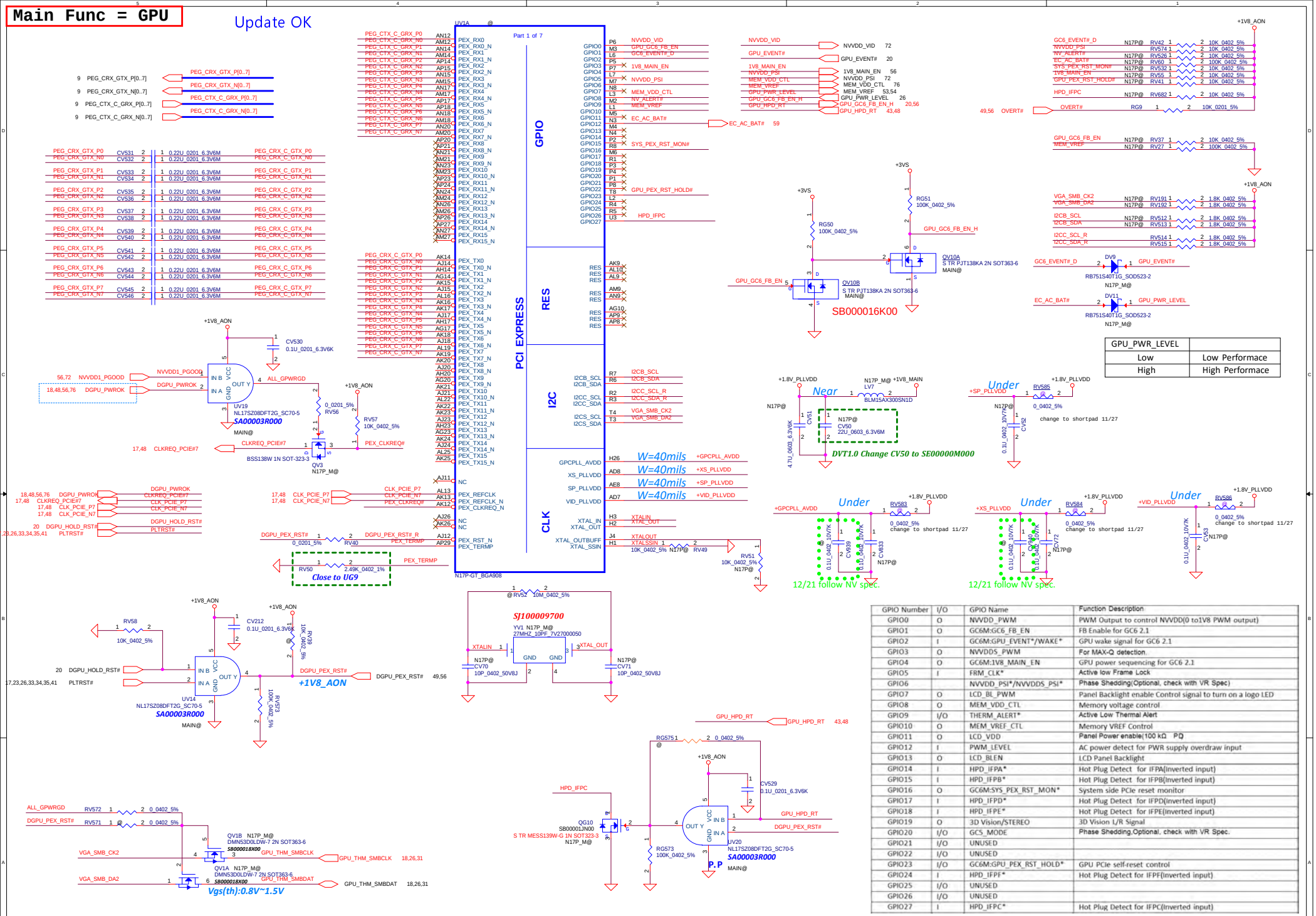




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2017/01/06	Title: Reserved
			Size: Document Number: LA-F611P Rev: 0.3
			Date: Thursday, March 22, 2018 Sheet 47 of 78

Main Func = GPU

Update OK



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

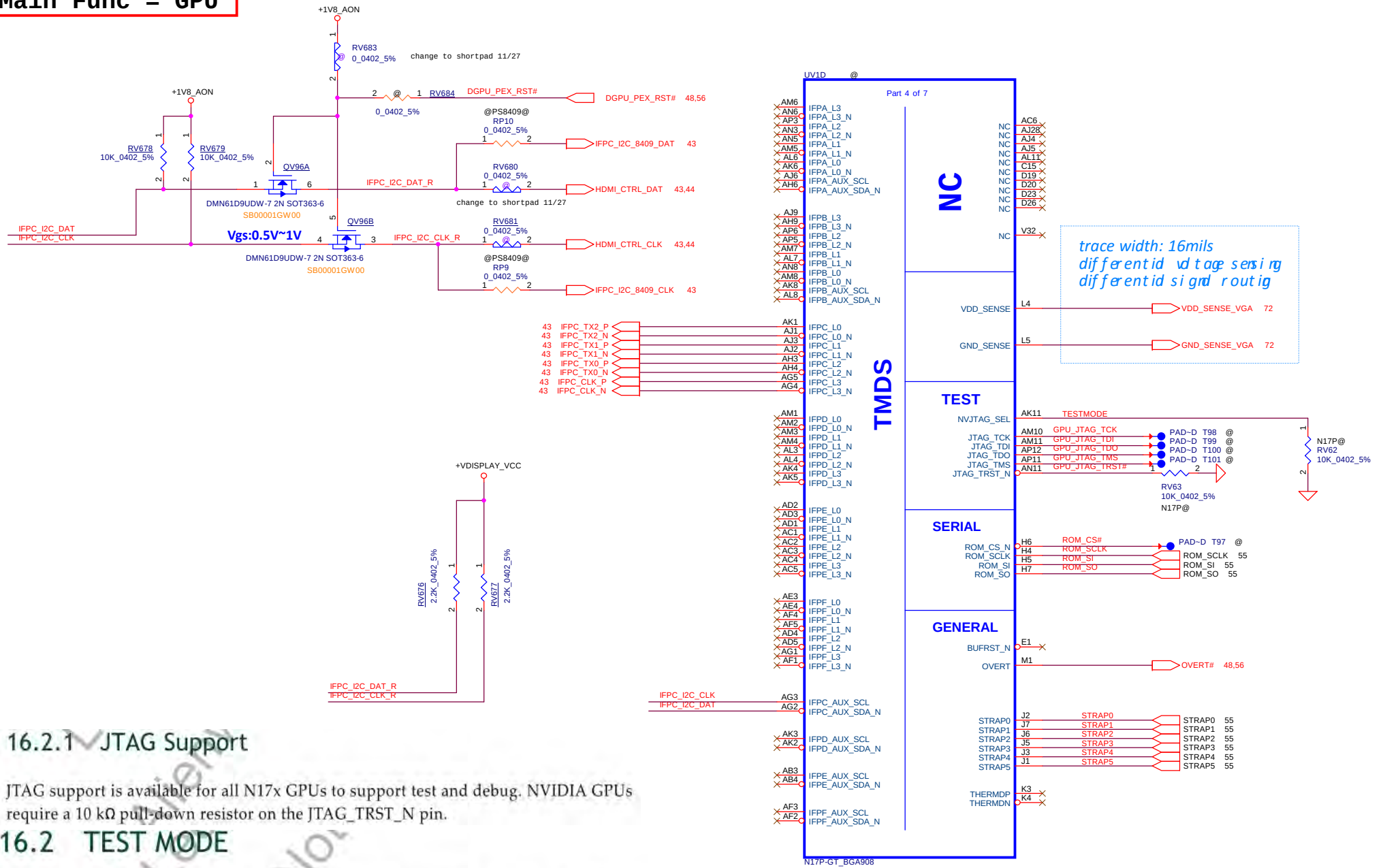
Compal Electronics, Inc.

Title: N17P-G1(1/9)PCIE/DAC/GPIO

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 48 of 78

Main Func = GPU



16.2.1 JTAG Support

JTAG support is available for all N17x GPUs to support test and debug. NVIDIA GPUs require a 10 kΩ pull-down resistor on the JTAG_TRST_N pin.

16.2 TEST MODE

By default, pull-down the TESTMODE pin (pin name is NVJTAG_SEL in some N17x pinouts) to GND with a 10 kΩ resistor. For ICT/boundary scan requirements, contact your NVIDIA AE.

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

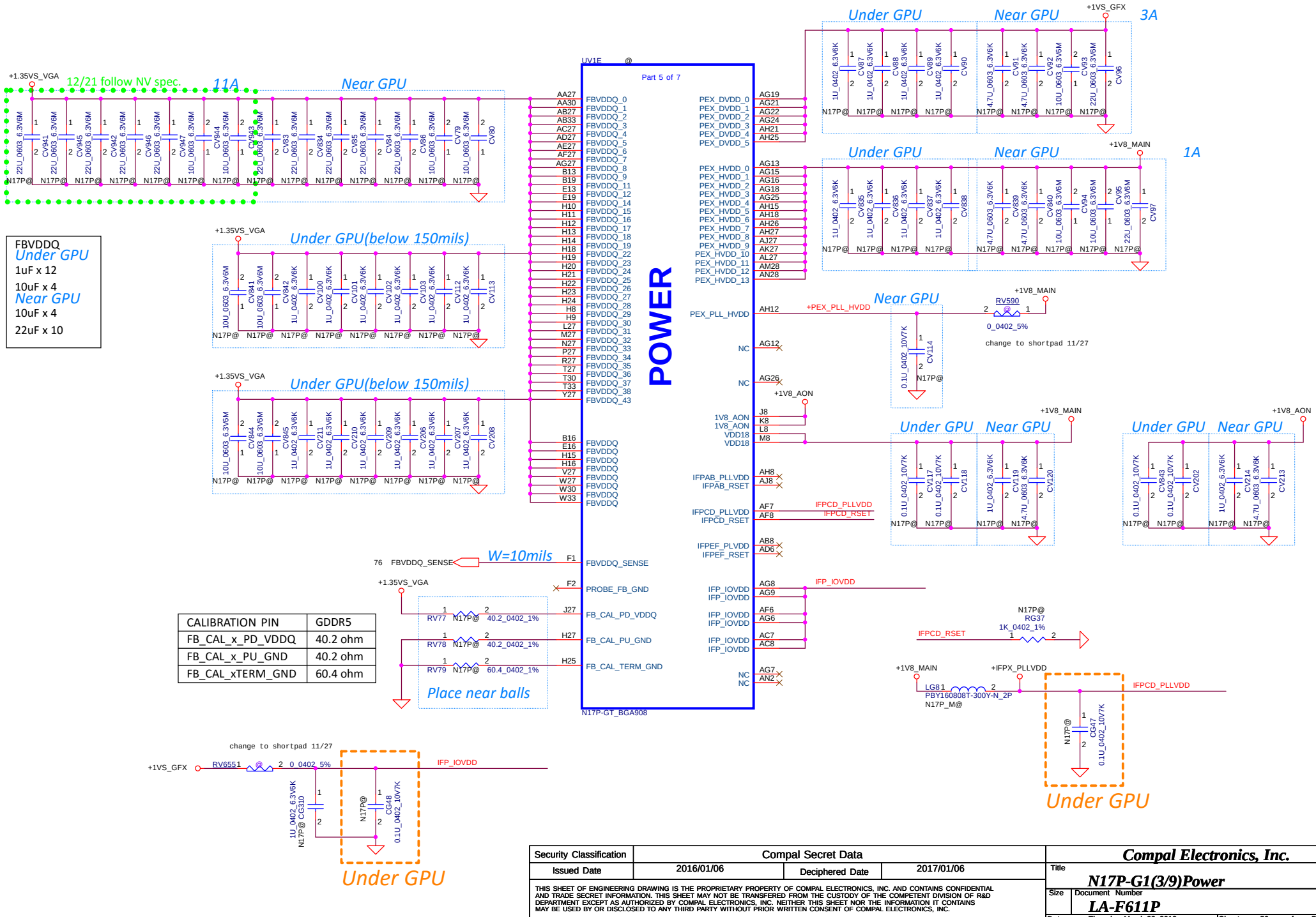
Compal Electronics, Inc.

Title: **N17P-G1(2/9)eDP/HDMI/mDP**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 49 of 78

Main Func = GPU



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

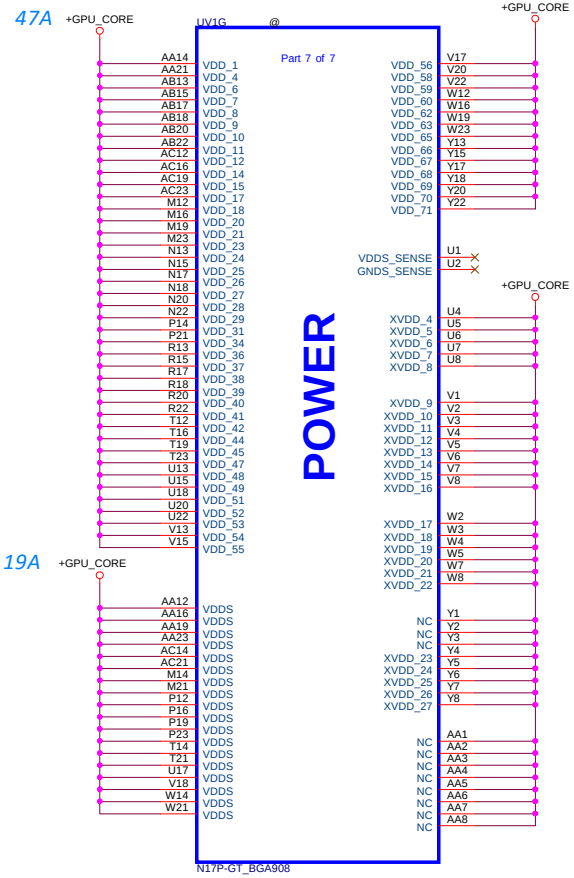
Compal Electronics, Inc.

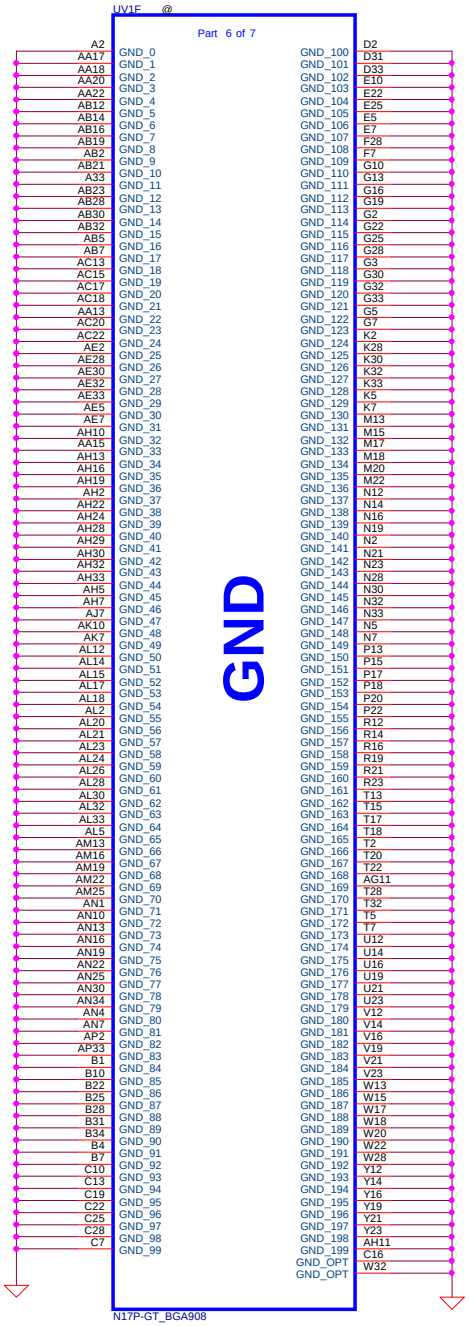
Title: N17P-G1(3/9)Power

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 50 of 78

Main Func = GPU





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Issued Date	2016/01/06	Deciphered Date	2017/01/06

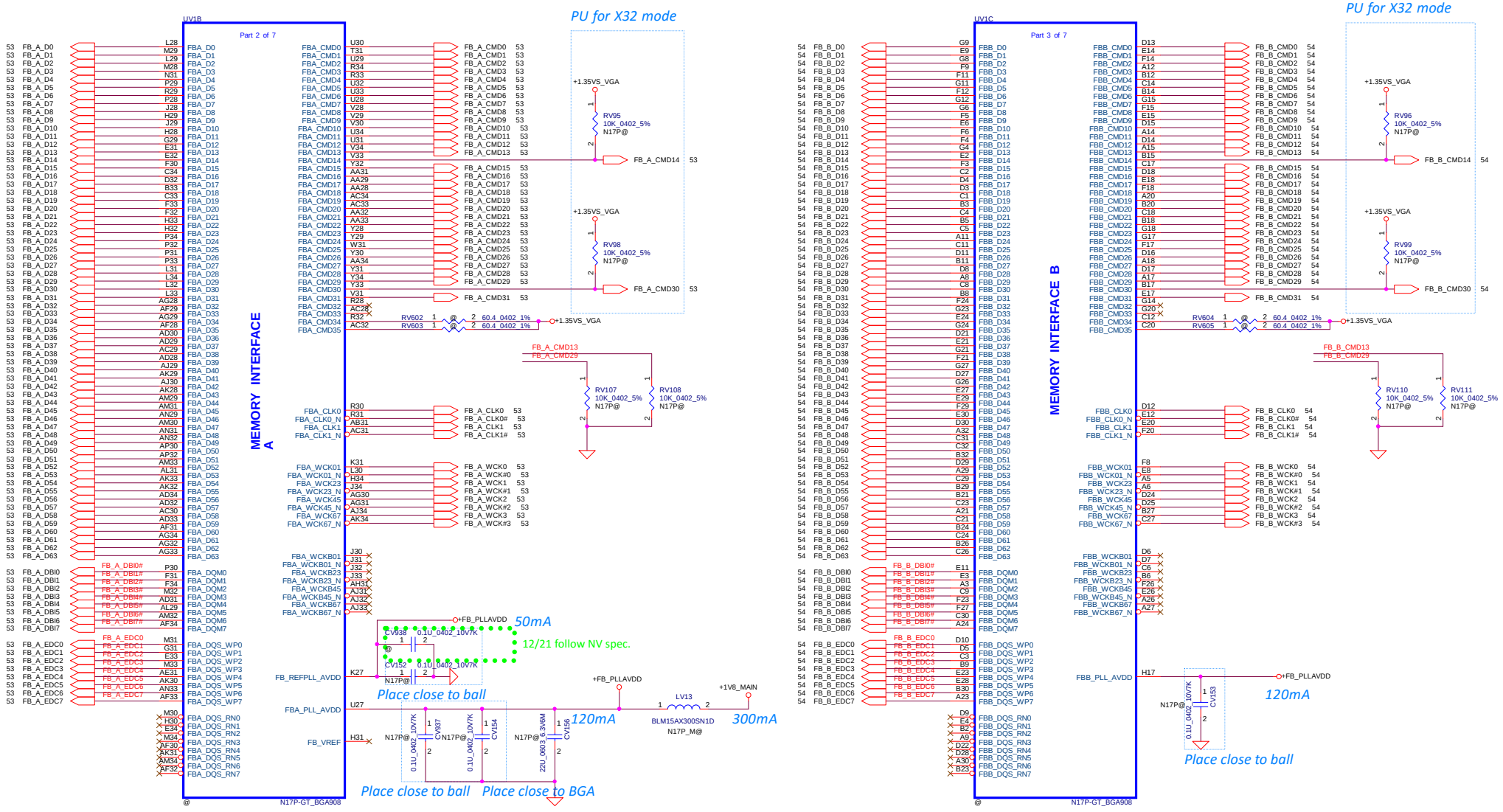
Compal Electronics, Inc.

Title: **N17P-G1(4/9)VGA CORE/GND**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 Sheet 51 of 78

Main Func = GPU



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Compal Electronics, Inc.

Title: **N17P-G1(5/9)MEM Interface**

Size	Document Number	Rev
	LA-F611P	0.3

Date: Thursday, March 22, 2018 | Sheet 52 of 78

Main Func = GDDR5

Memory Partition A- Lower 32 bit

MF=0

UV6

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

W=16mils

Around DRAM

Close to DRAM

Under DRAM

VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

MF=1

UV7

Under DRAM

VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

Around DRAM

Close to DRAM

Security Classification	Compal Secret Data	
Issued Date	2016/01/06	Deciphered Date 2017/01/06

Compal Electronics, Inc.

Title: N17P-G1(6/9)GDDR5_A

Size: | Document Number: LA-F611P | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 53 of 78

Main Func = GDDR5

Memory Partition A- Lower 32 bit

MF=0

UV8

MF=1

UV9

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

W=16mils

Around DRAM

Close to DRAM

Under DRAM

VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

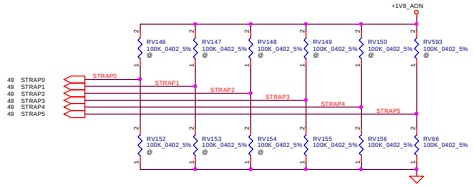
Security Classification	Compal Secret Data	
Issued Date	2016/01/06	Deciphered Date 2017/01/06

Compal Electronics, Inc.

Title: N17P-G1(7/9)GDDR5_B

Size: LA-F611P | Document Number | Rev 0.3

Date: Thursday, March 22, 2018 | Sheet 54 of 78



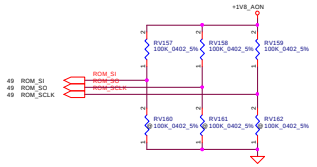


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

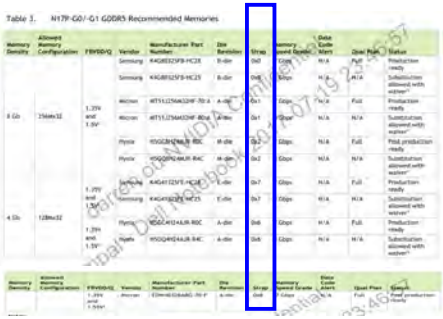
Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

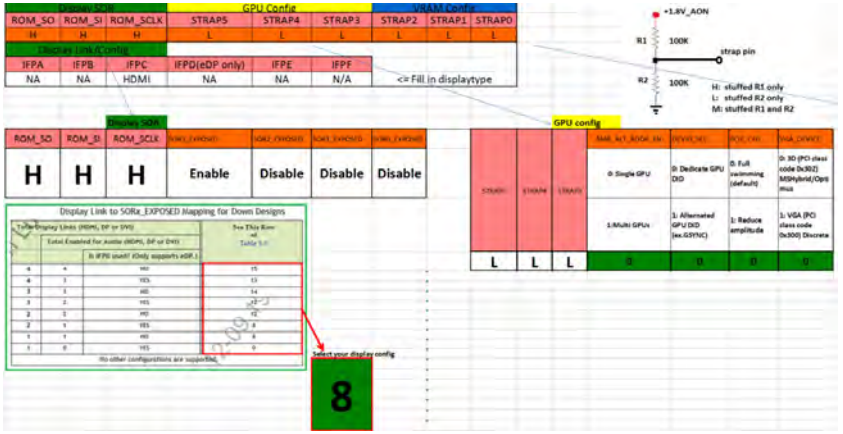
SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude





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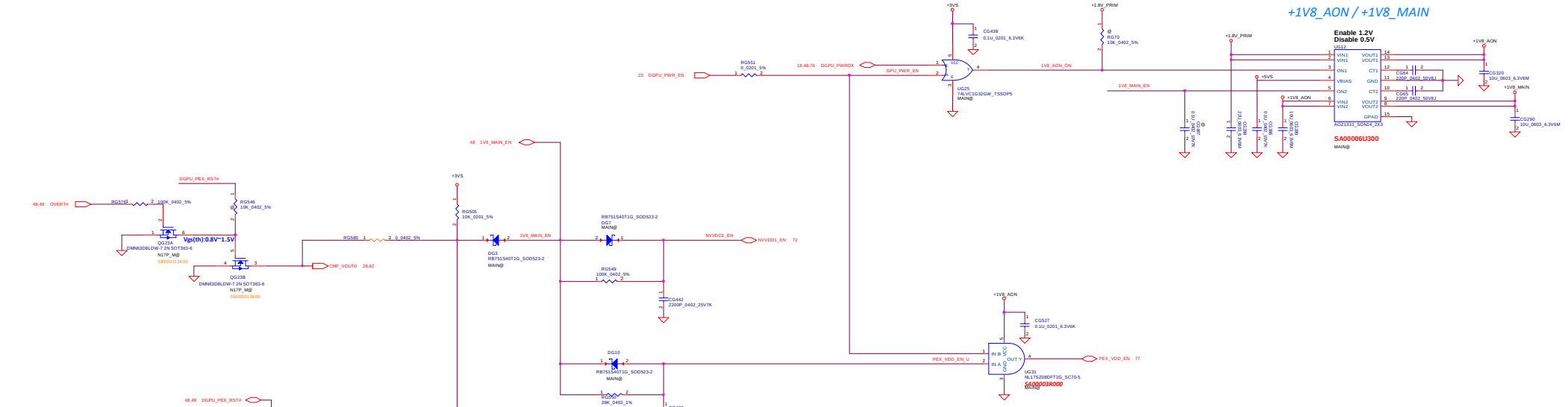
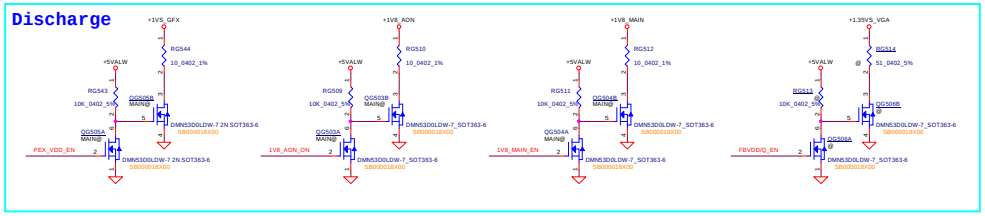
				Size Document Number LA-F611P Rev 0.3
				Date: Thursday, March 22, 2018 Sheet 55 of 78

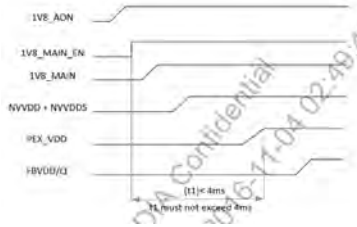
Main Func = DC/DC



Discharge



GPU Power Up Sequence



GPU Power Down Sequence

GPU GC6 Entry/Exit Sequence

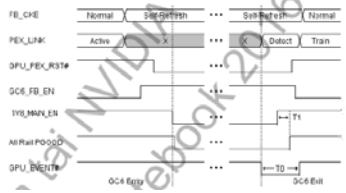


Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Optimus Sequence

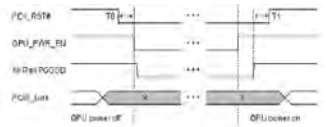


Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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Compal Electronics, Inc.			
Title	GPU power control		
Size	Document Number		Rev 0.3
	LA-F611P		
Date: Thursday, March 22, 2018	Sheet 56 of 78		

MODEL NAME : *CALXX/CALXX*

PCB NO : *LA-F611P*

Bom Structure

GPU

UV1 N17P_G0_R1@ — R1 — N17P-G0-A1 — *SA0000A050L*

UV1 N17P_G0_R3@ — R3 — N17P-G0-A1 — *SA0000A051L*

UV1 N17P_G1_R1@ — R1 — N17P-G1-A1 — *SA0000A060L*

UV1 N17P_G1_R3@ — R3 — N17P-G1-A1 — *SA0000A061L*

X76 : S4G@ X76XXXXXLXX

Samsung 4G

UV6 S4G@	UV7 S4G@	UV8 S4G@	UV9 S4G@
R3	R3	R3	R3
K4G80325FB-HC28	K4G80325FB-HC28	K4G80325FB-HC28	K4G80325FB-HC28
SA000092D1L	*SA000092D1L*	*SA000092D1L*	*SA000092D1L*

RV152 S4G@	RV153 S4G@	RV154 S4G@
L	L	L
100K_0402_5%	100K_0402_5%	100K_0402_5%
SD028100380	*SD028100380*	*SD028100380*

X76 : M4G@ X76XXXXXLXX

Micron 4G

UV6 M4G@	UV7 M4G@	UV8 M4G@	UV9 M4G@
R3	R3	R3	R3
MT51J256M32HF-70:A	MT51J256M32HF-70:A	MT51J256M32HF-70:A	MT51J256M32HF-70:A
SA00009TV1L	*SA00009TV1L*	*SA00009TV1L*	*SA00009TV1L*

RV146 M4G@	RV153 M4G@	RV154 M4G@
H	L	L
100K_0402_5%	100K_0402_5%	100K_0402_5%
SD028100380	*SD028100380*	*SD028100380*

X76 : H4G@ X76XXXXXLXX

Hynix 4G

UV6 H4G@	UV7 H4G@	UV8 H4G@	UV9 H4G@
R3	R3	R3	R3
H5GC8H24MJR-R0C	H5GC8H24MJR-R0C	H5GC8H24MJR-R0C	H5GC8H24MJR-R0C
SA00009U11L	*SA00009U11L*	*SA00009U11L*	*SA00009U11L*

RV152 H4G@	RV147 H4G@	RV154 H4G@
L	H	L
100K_0402_5%	100K_0402_5%	100K_0402_5%
SD028100380	*SD028100380*	*SD028100380*

Samsung 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
0	L	L	L

Micron 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
1	L	L	H

Hynix 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
2	L	H	L

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[1]	Samsung	K4G80325FB-HC28	B-die	0x0	Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	Gbps	N/A	N/A	Substitution allowed with waiver[2]
4 Gb	128Mx32	1.35V and 1.5V[1]	Samsung	K4G41325FE-HC28	E-die	0x7	Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	Gbps	N/A	Full	Production ready
		1.35V and 1.5V[1]	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	Gbps	N/A	N/A	Substitution allowed with waiver[2]

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
		1.35V and 1.55V[1]	Micron	EDW4032BABG-70-F	A-die	0x8	Gbps	N/A	Full	Post production ready

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-F611P** | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 57 of 78

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

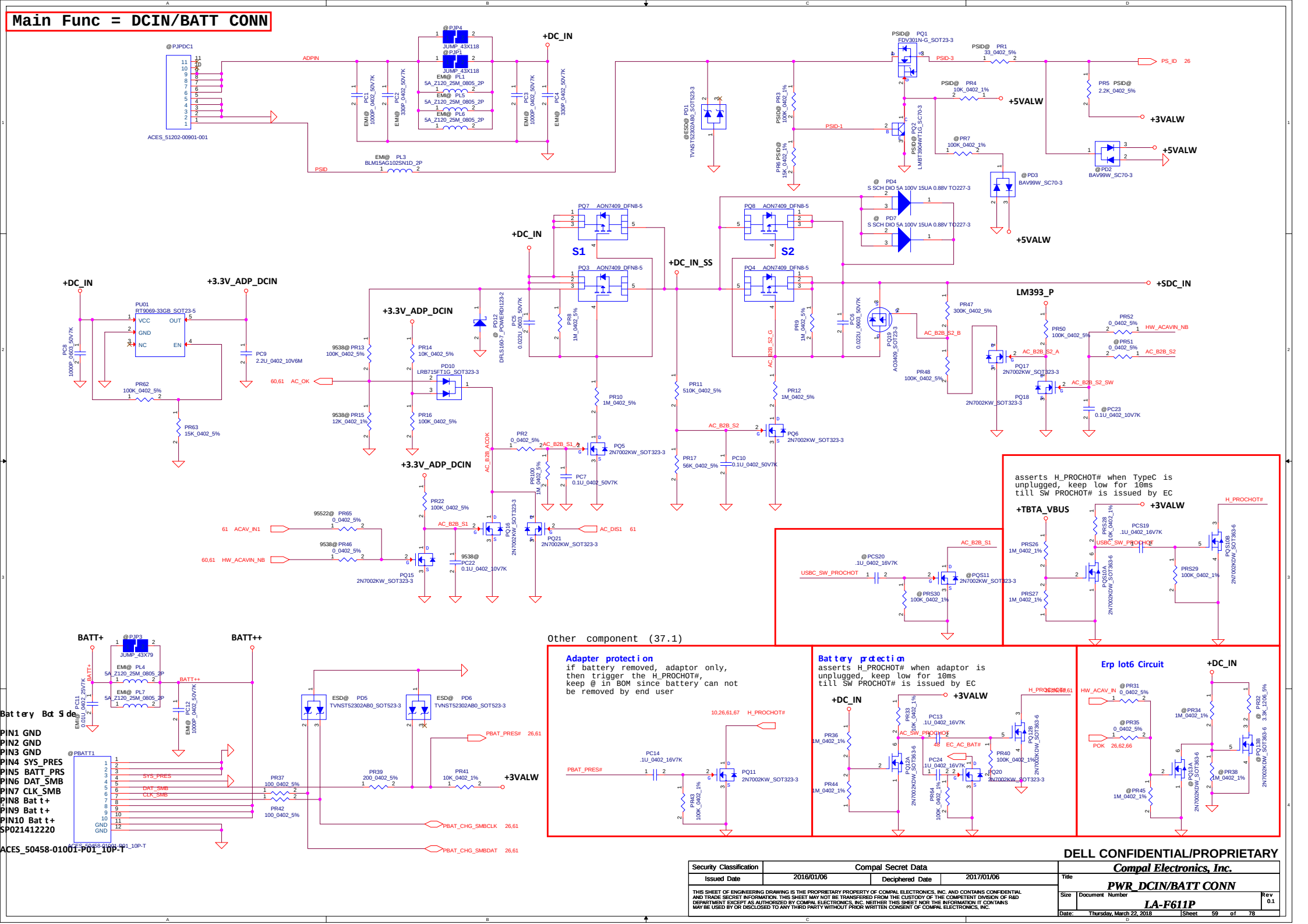
Compal Electronics, Inc.

Title: **NOTE**

Size | Document Number: **LA-F611P** | Rev: 0.3

Date: Thursday, March 22, 2018 | Sheet 58 of 78

Main Func = DCIN/BATT CONN



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Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

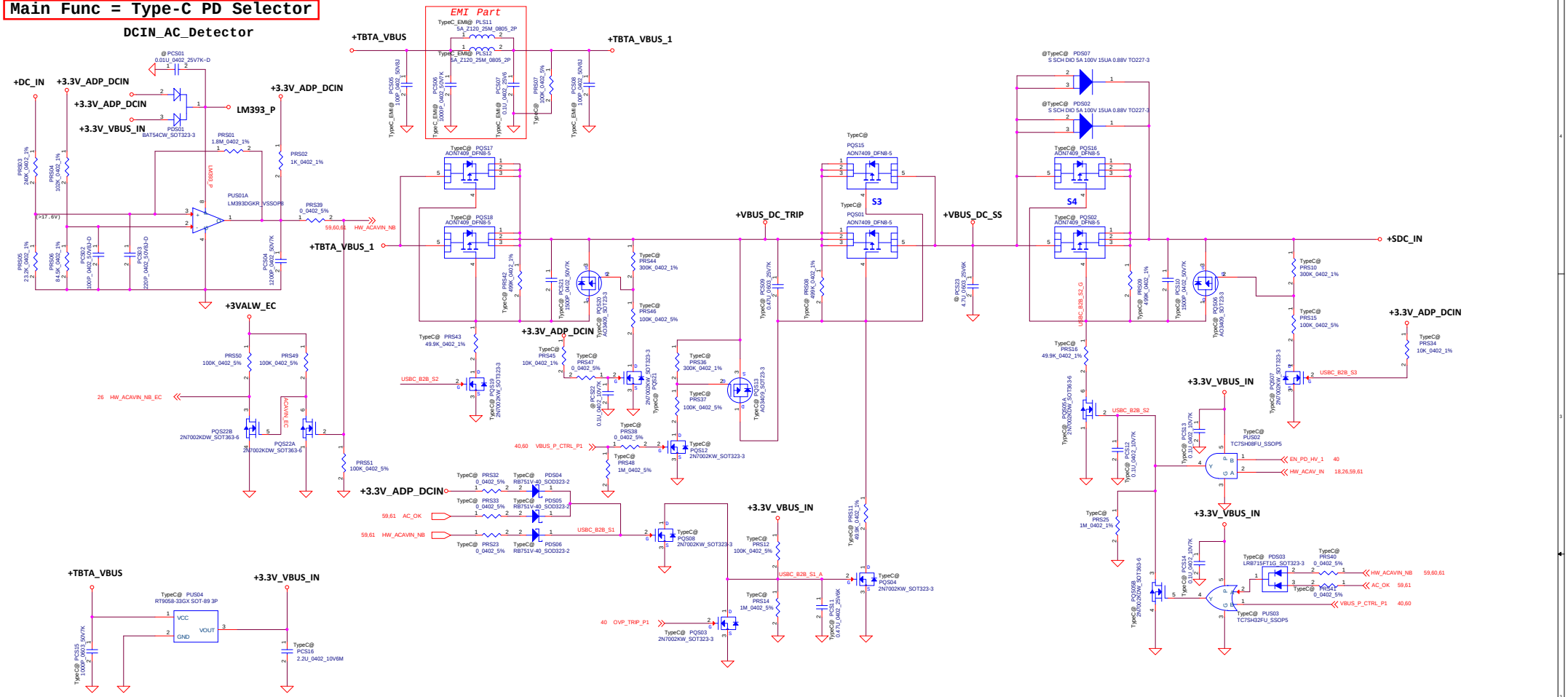
Title: PWR_DCIN/BATT CONN

Size | Document Number: LA-F611P | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 59 of 78

Main Func = Type-C PD Selector

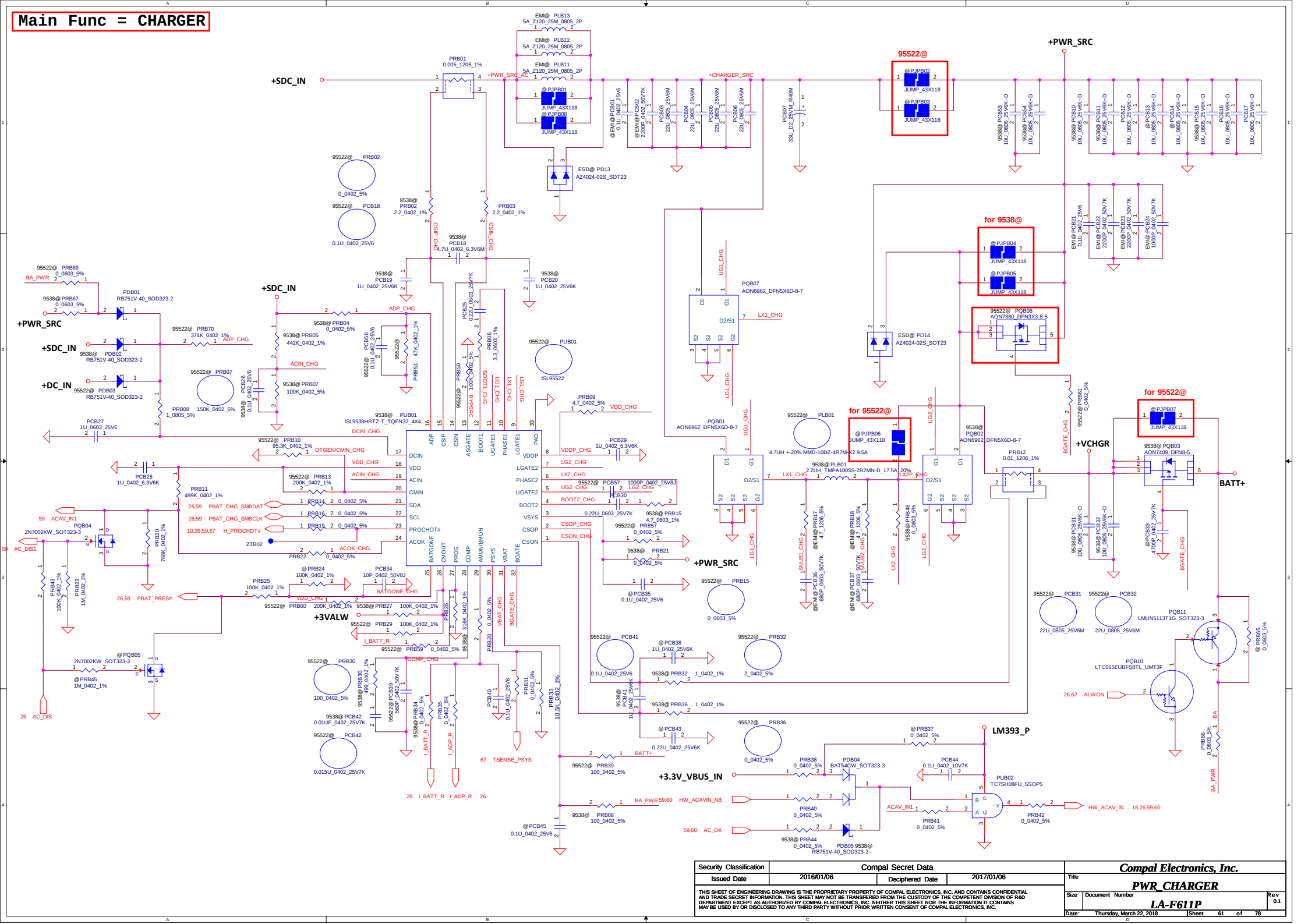
DCIN_AC_Detector



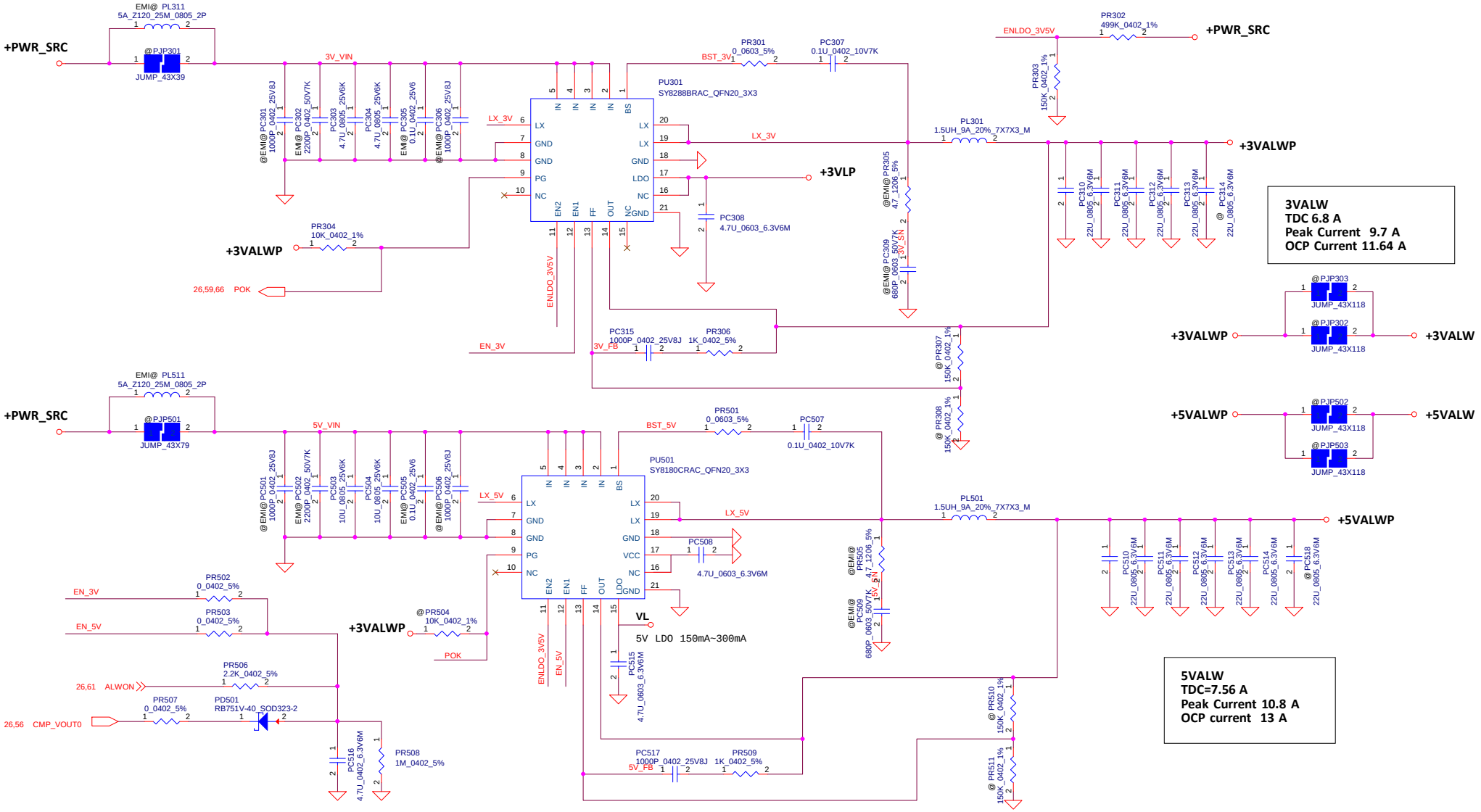
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR Type-C PD Selector			
Size	Document Number: LA-F611P		Rev: 0.1
Date: Thursday, March 22, 2018	Sheet 60 of 78		

Main Func = CHARGER



Main Func = 3.3VALW/5VALW



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

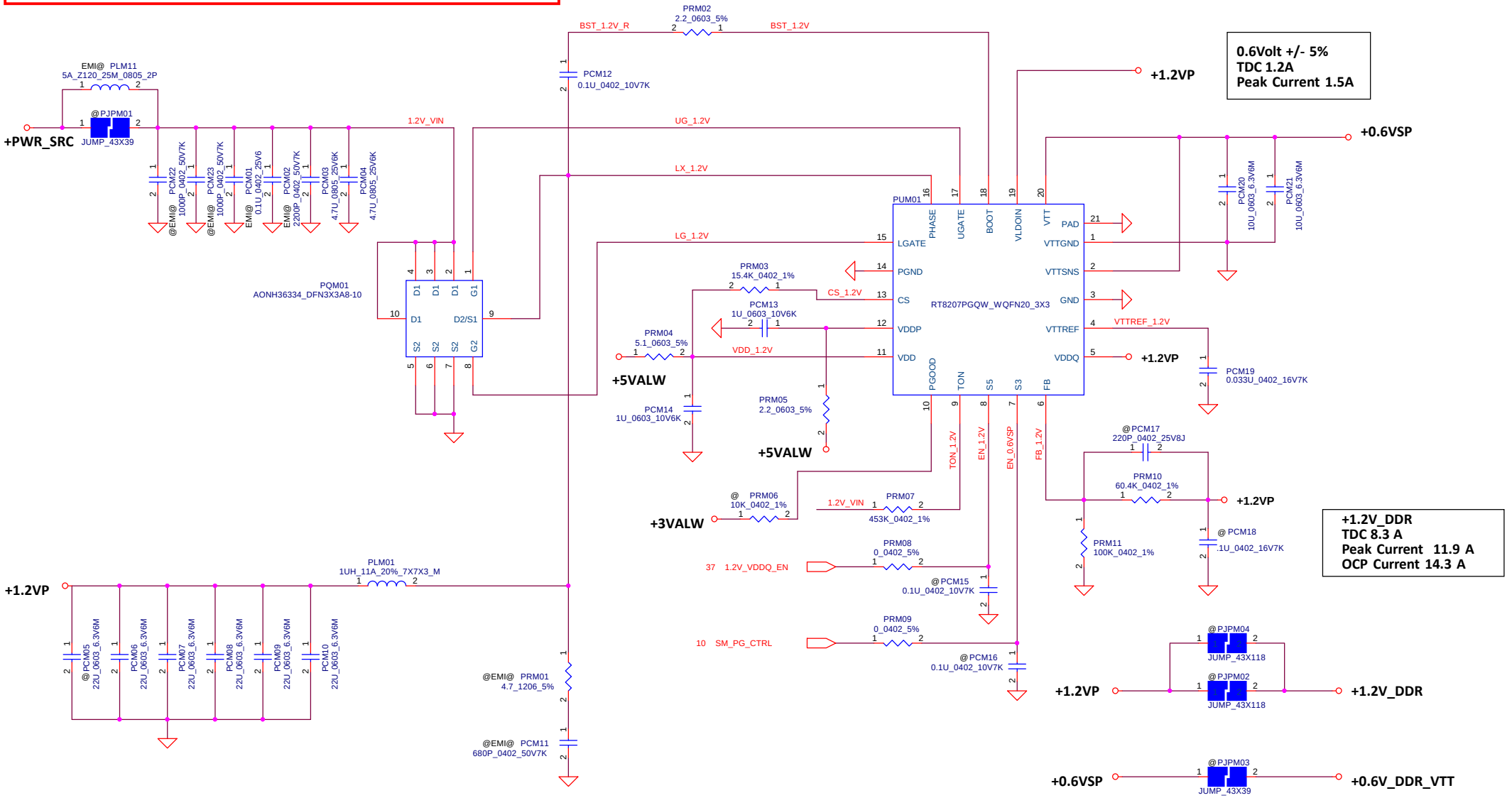
Compal Electronics, Inc.

Title: PWR_3.3VALW/5VALW

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 Sheet 62 of 78

Main Func = 1.2V_DDR/+0.6V_DDR_VTT



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

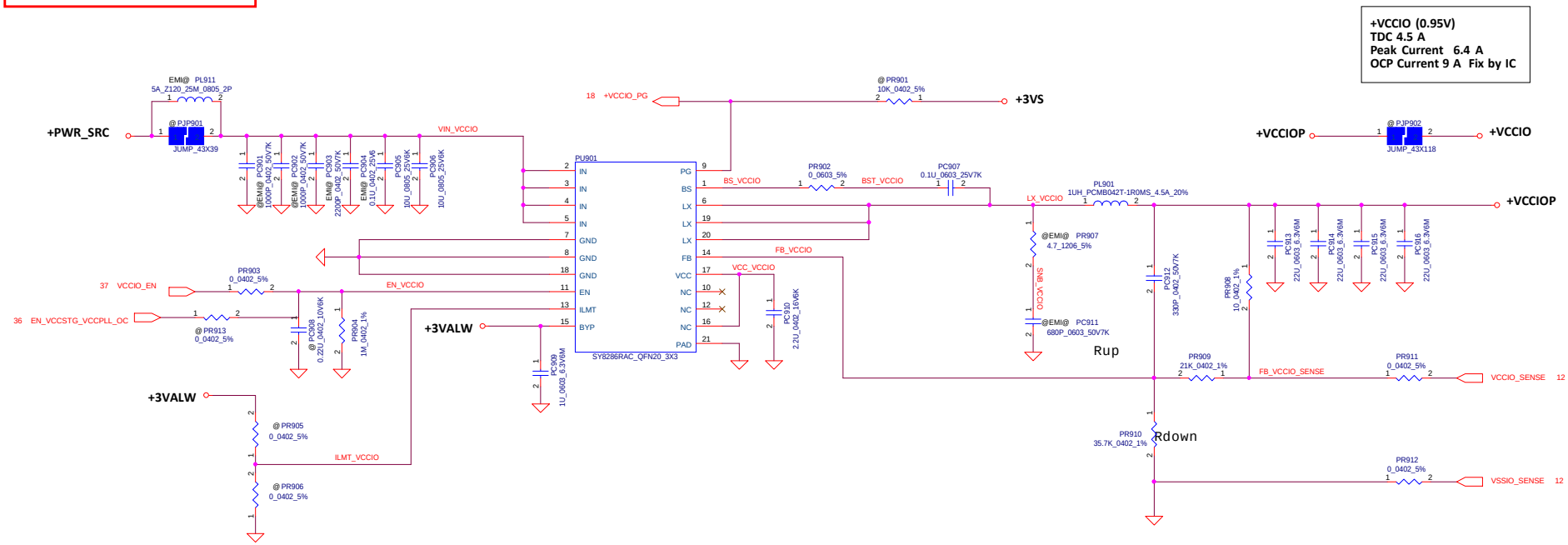
Compal Electronics, Inc.

Title: PWR_+1.2V_DDR/+0.6V_DDR_VTT

Size | Document Number: LA-F611P | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 63 of 78

Main Func = VCCIO



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

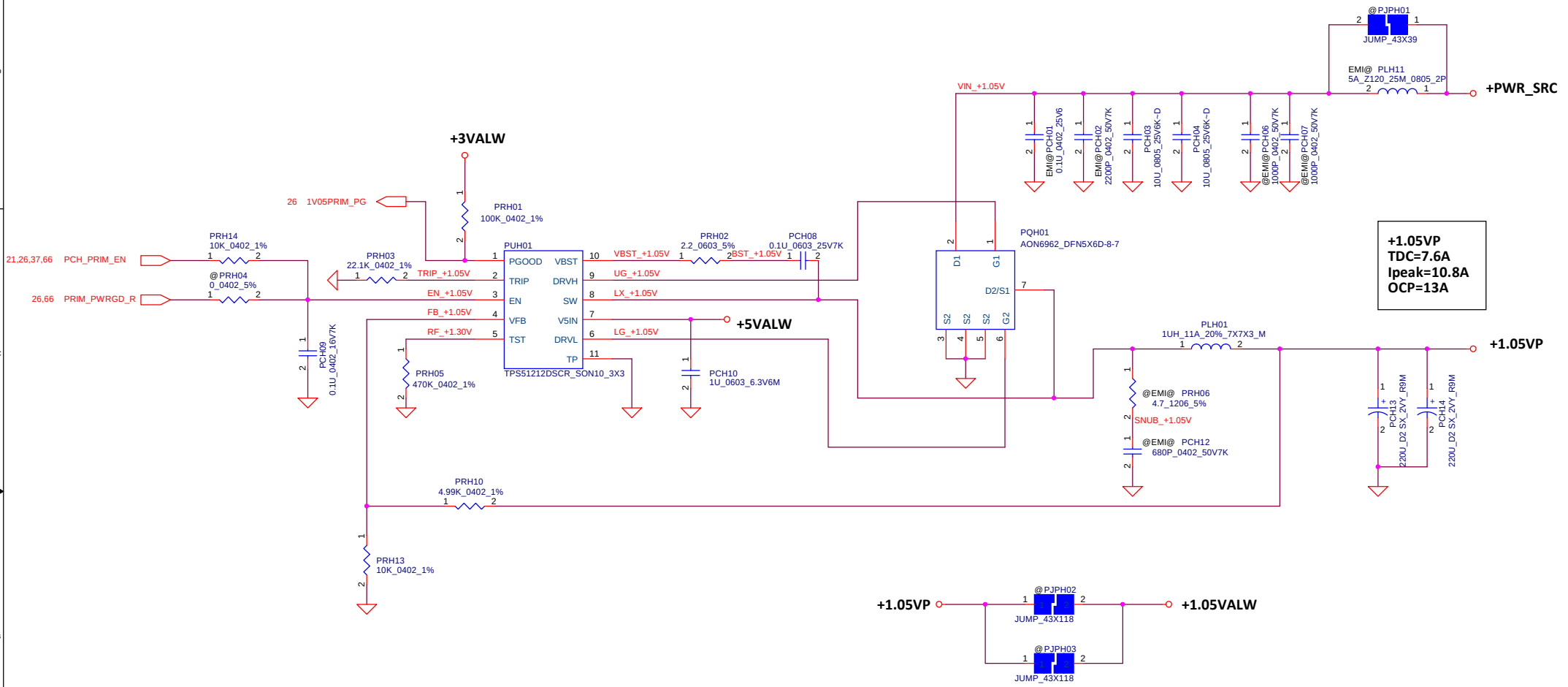
Compal Electronics, Inc.

Title: **PWR_+VCCIO**

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 Sheet 64 of 78

Main Func = 1.05VALW



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

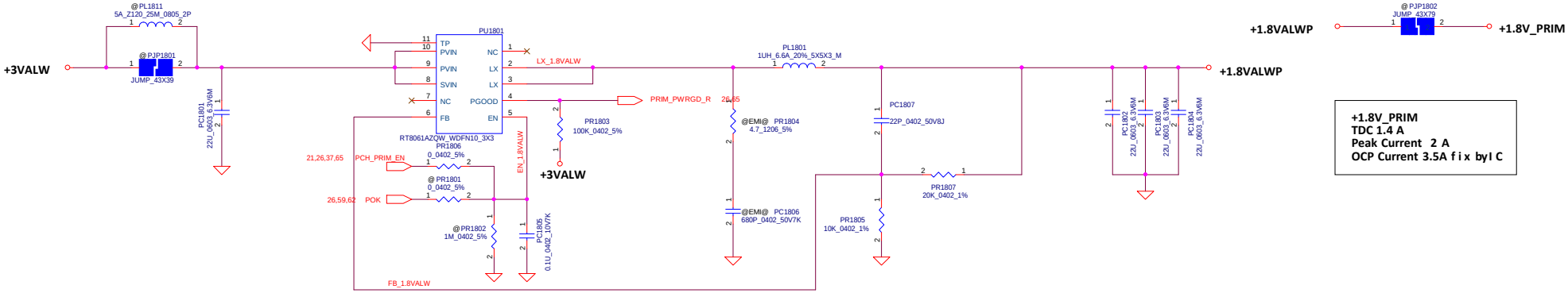
Compal Electronics, Inc.

Title: **PWR-1.05VALW**

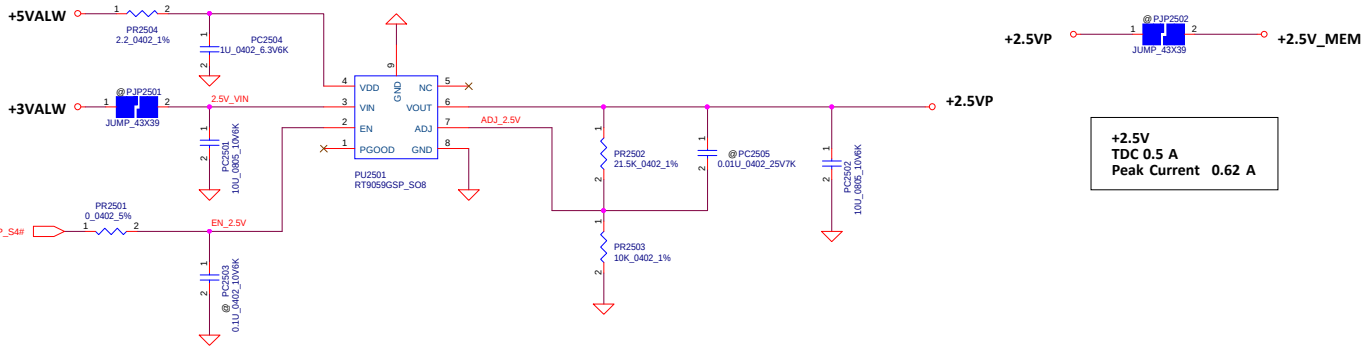
Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 | Sheet 65 of 78

Main Func = +1.8V_PRIM/+2.5V_MEM



+1.8V_PRIM
TDC 1.4 A
Peak Current 2 A
OCP Current 3.5A fix by I C



+2.5V
TDC 0.5 A
Peak Current 0.62 A

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

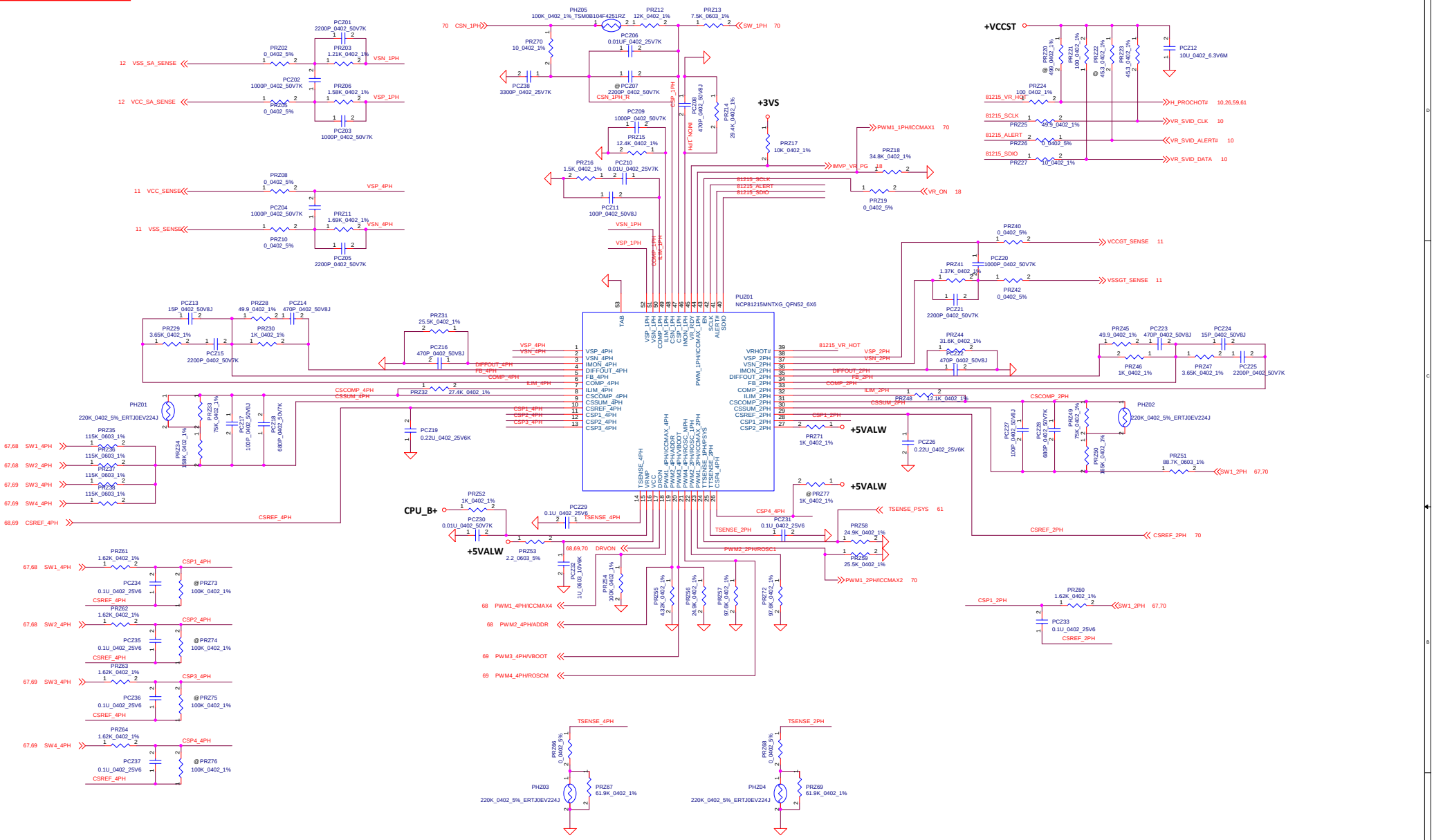
Compal Electronics, Inc.

Title: PWR_+1.8V_PRIM/+2.5V_MEM

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 Sheet 66 of 78

Main Func = VCORE

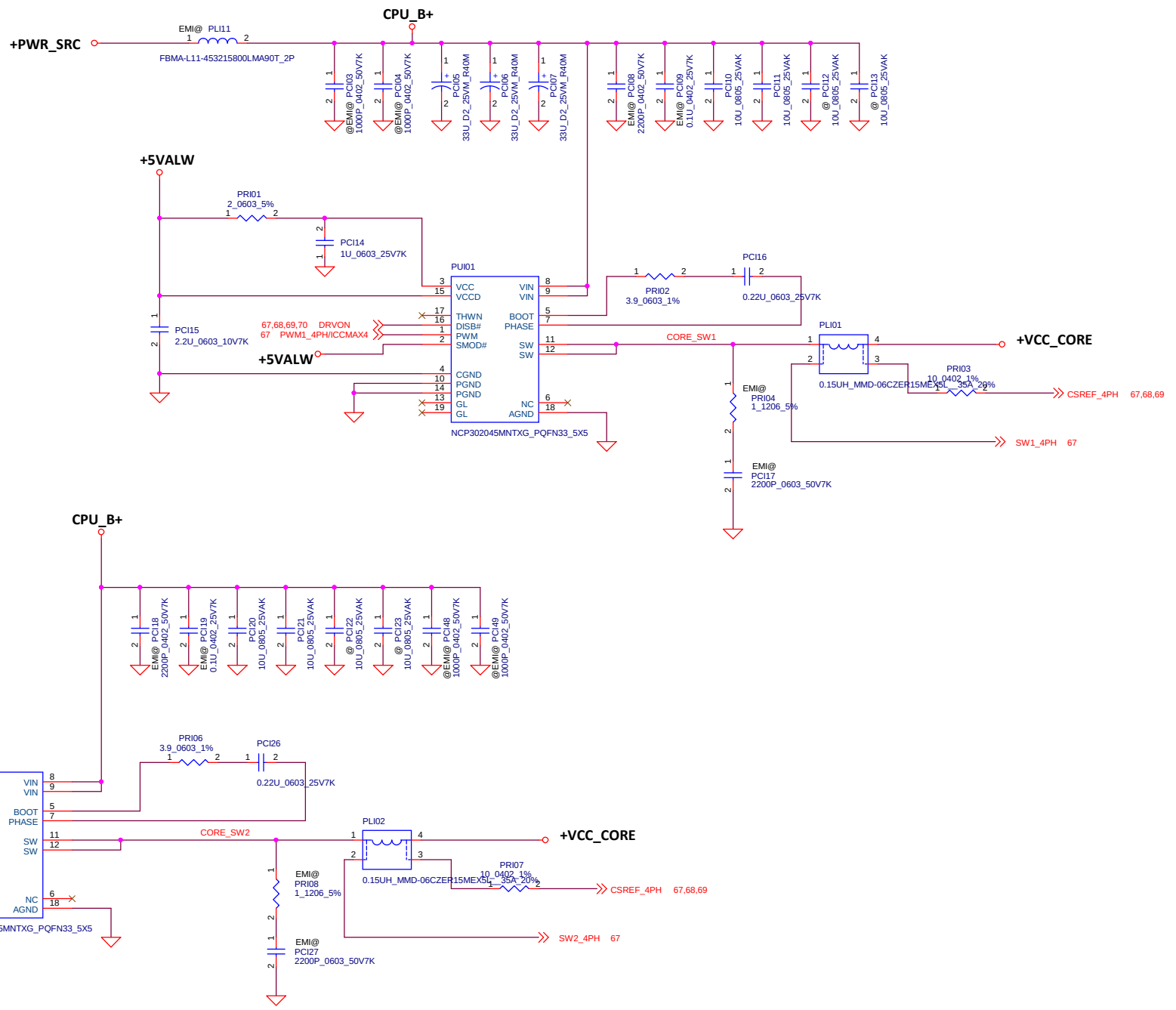


Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	+VCORE_NCP81215		
Size	Document Number	LA-F611P	Rev 0.1
Date: Thursday, March 22, 2018	Sheet 67 of 78		

Main Func = CORE_Phase1&2

+VCC_CORE
TDC PL2 :80A
Peak Current 128A
OCP Current 154A
DCR 0.9mohm +/-5%
Load Line 1.8mV/A



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

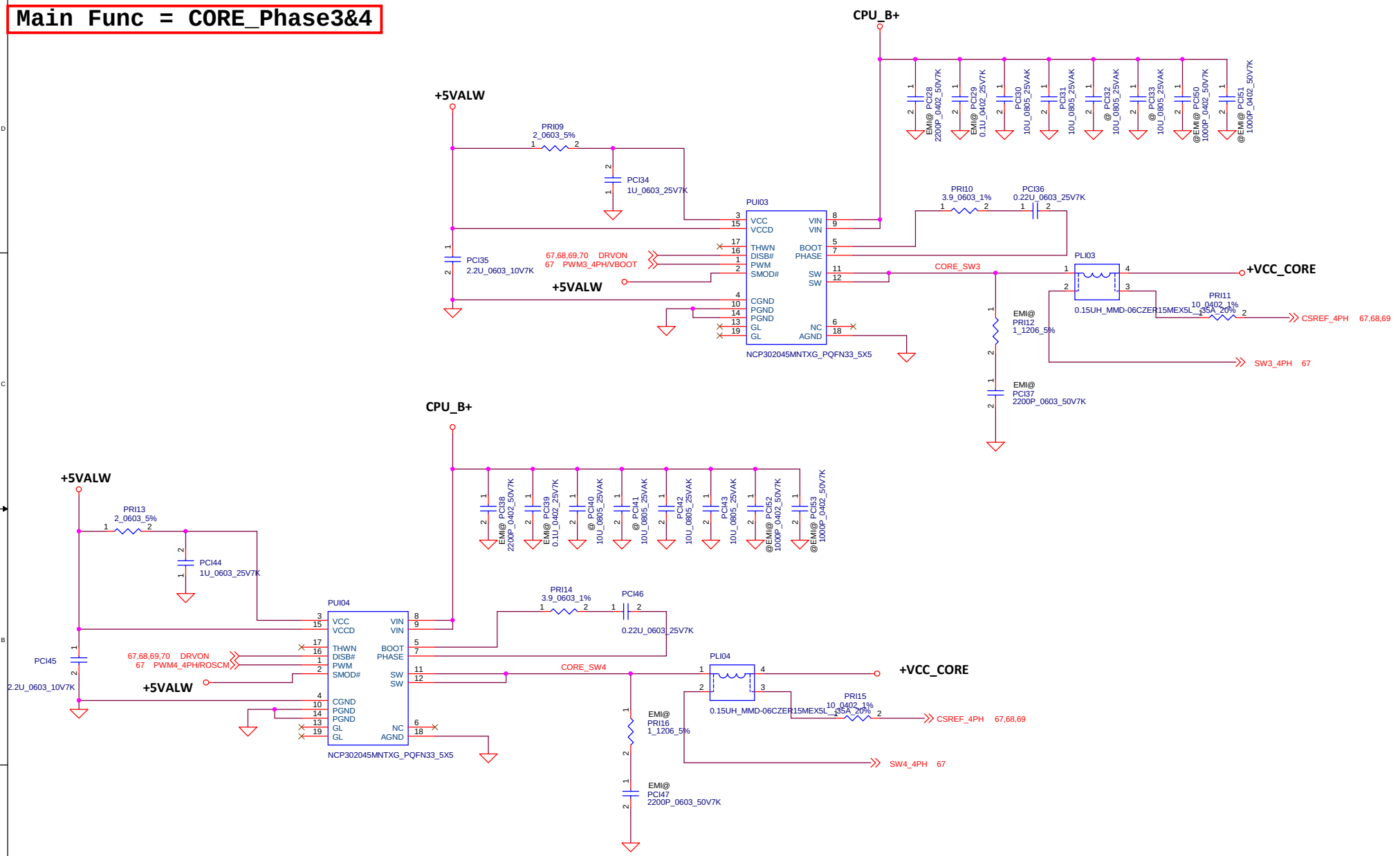
Compal Electronics, Inc.

Title: +VCC_CORE_Phase1&2

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 | Sheet 68 of 78

Main Func = CORE_Phase3&4



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

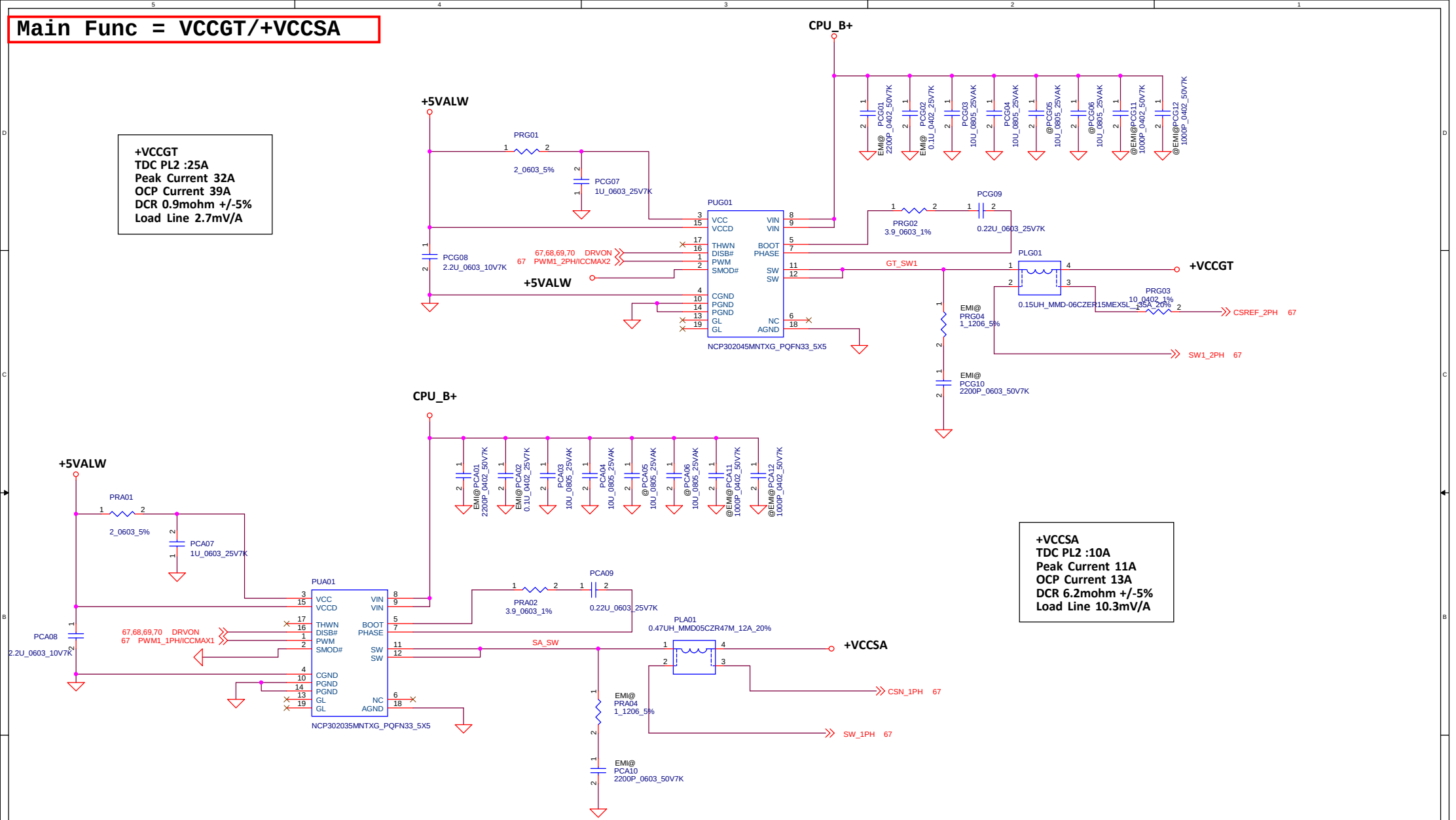
Compal Electronics, Inc.

Title: +VCC_CORE_Phase3&4

Size | Document Number: LA-F611P | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 69 of 78

Main Func = VCCGT/+VCCSA



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

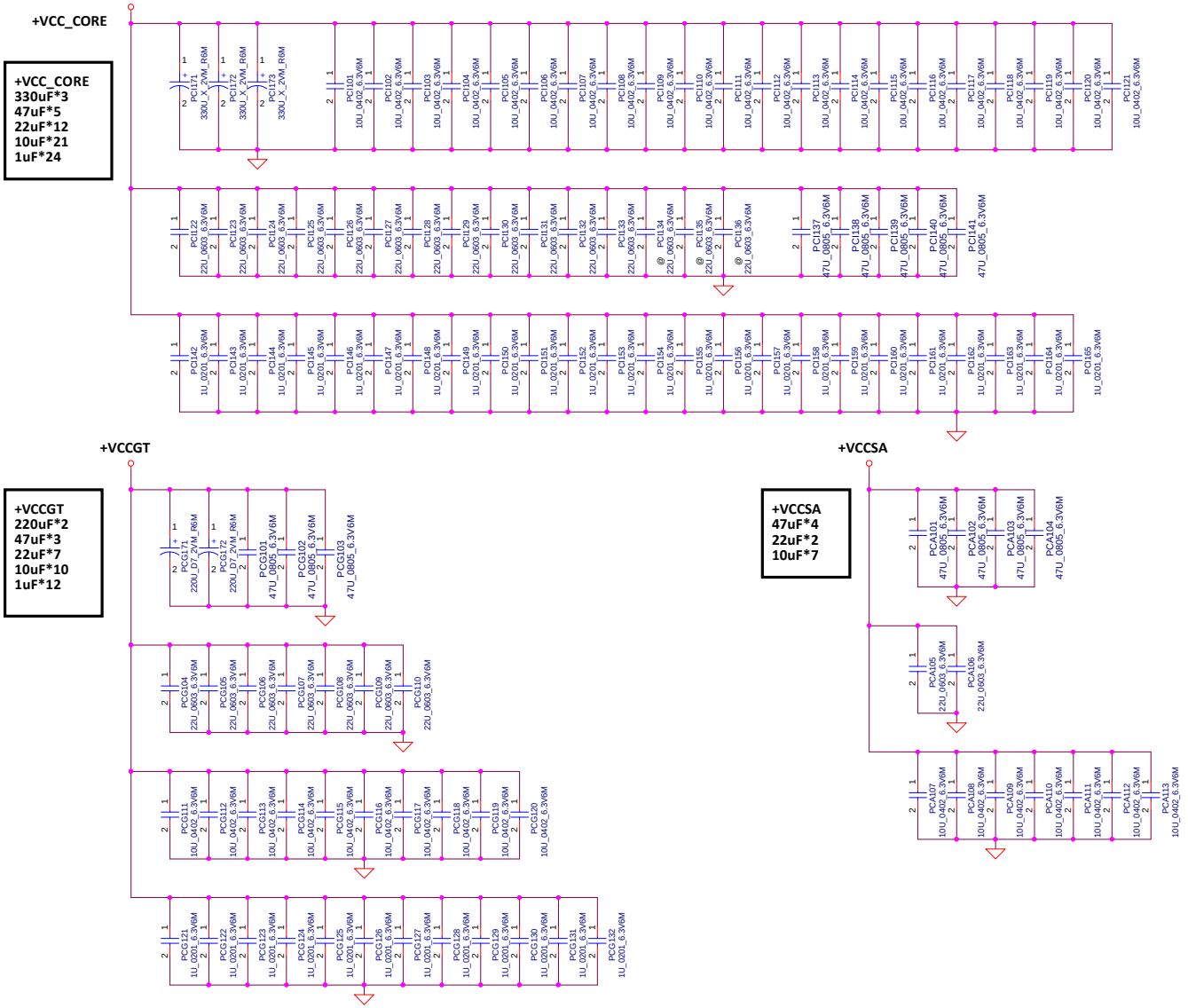
Compal Electronics, Inc.

Title: +VCC_GT/+VCC_SA

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 | Sheet 70 of 78

Main Func = PWR_CPU DECOUPLING



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

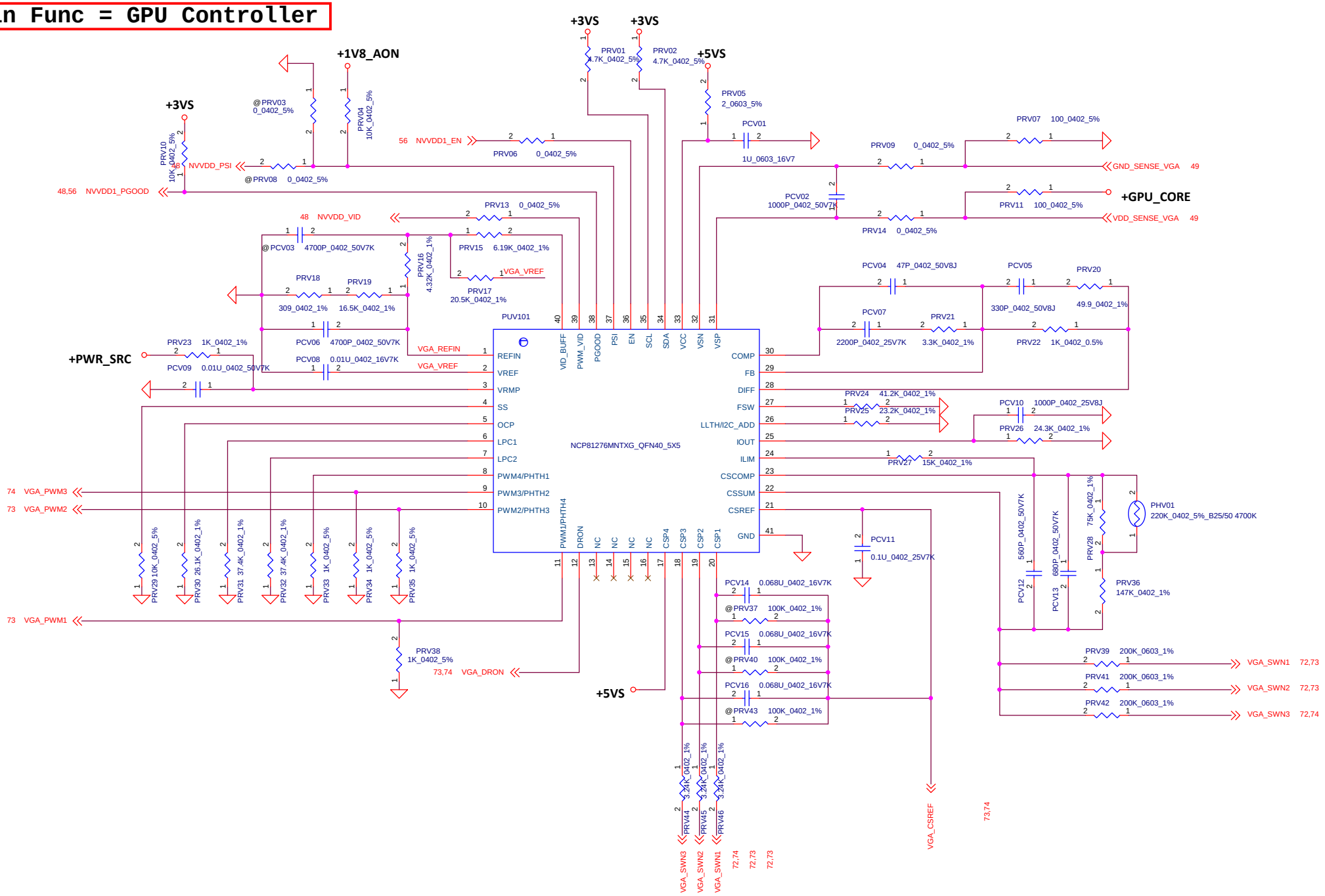
Compal Electronics, Inc.

Title: **PWR-CPU DECOUPLING**

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 | Sheet 71 of 78

Main Func = GPU Controller



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

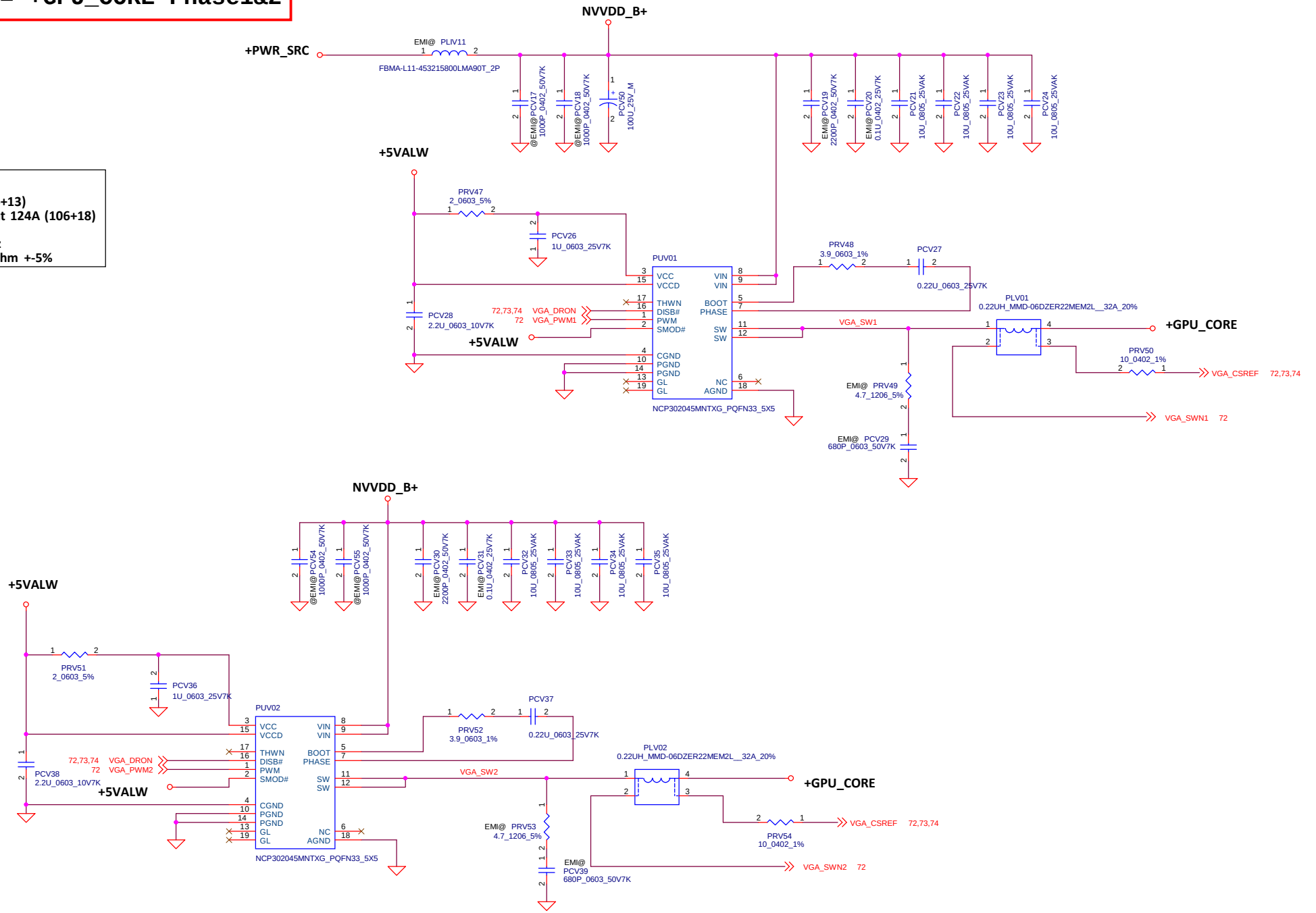
Title: **PWR_GPU Controller**

Size	Document Number	Rev
	LA-F611P	0.1

Date: Thursday, March 22, 2018 | Sheet 72 of 78

Main Func = +GPU_CORE Phase1&2

+GPU_CORE
TDC 59A (46+13)
Peak Current 124A (106+18)
OCP=149A
Fsw=305KHz
DCR:0.98mohm +-5%



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

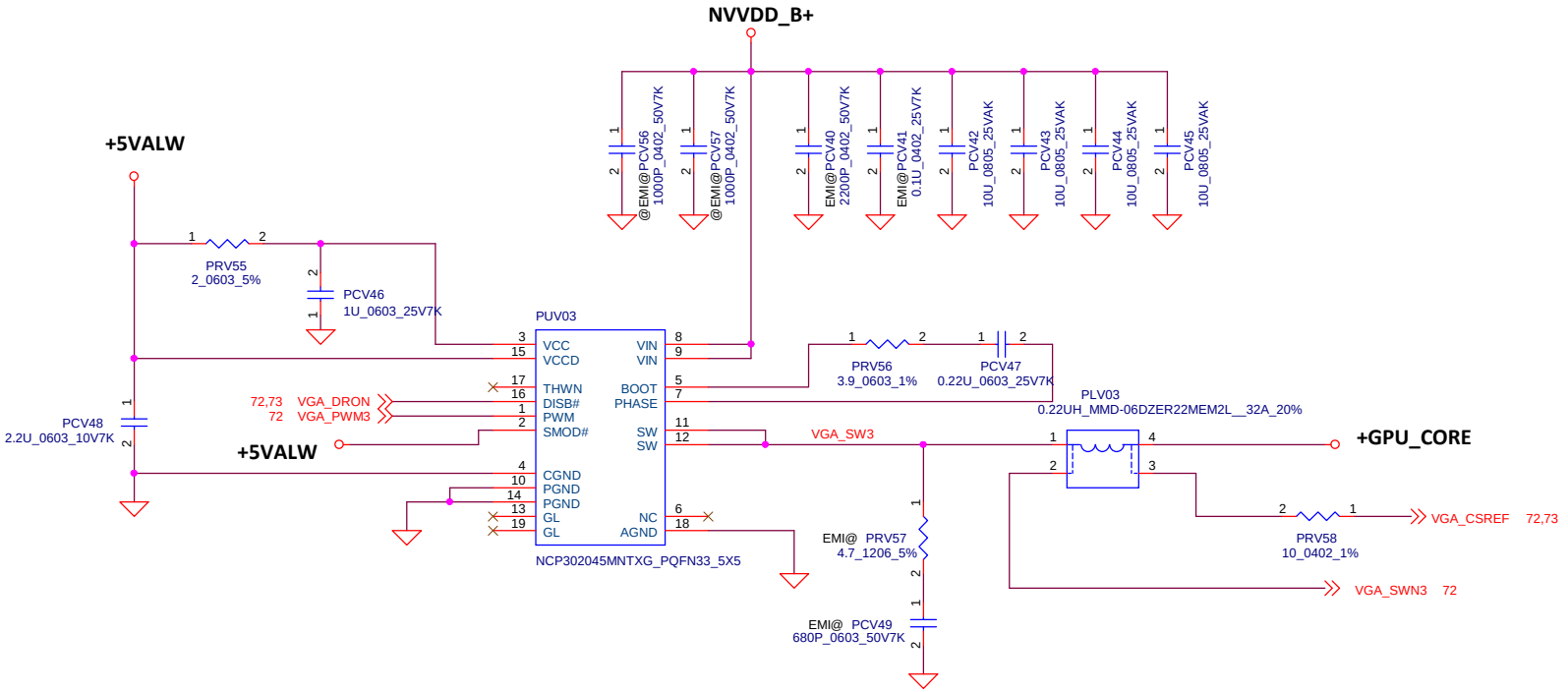
Compal Electronics, Inc.

Title: PWR_+GPU_CORE Phase1&2

Size | Document Number: LA-F611P | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 73 of 78

Main Func = +GPU_CORE Phase3



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

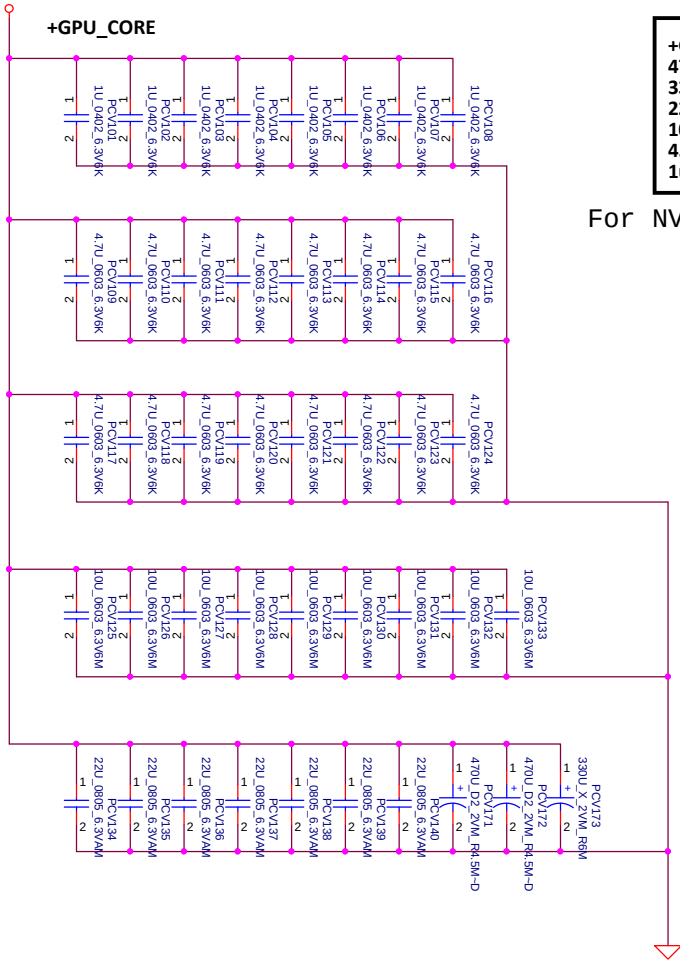
Compal Electronics, Inc.

Title: **PWR_+GPU_CORE Phase3**

Size	Document Number	Rev
	LA-F611P	0.1

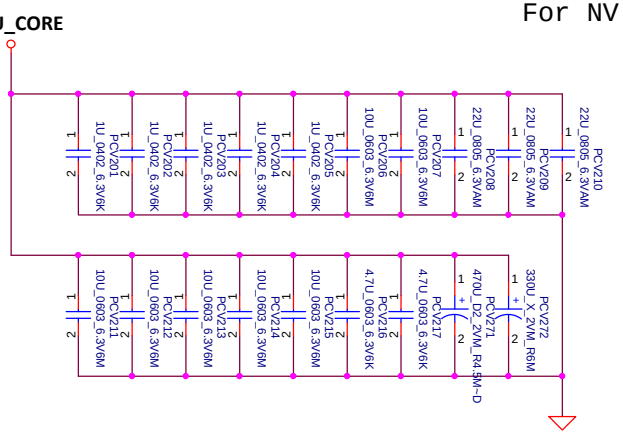
Date: Thursday, March 22, 2018 Sheet 74 of 78

Main Func = VGA DECOUPLING



+GPU_CORE (NVVDD)
470uF X 2
330uF X 1
22uF_0805 X 7
10uF_0603 X 9
4.7uF_0603 X 16
1uF_0402 X 8

For NV N17P latest spec



+GPU_CORE (NVVDDS)
470uF X 1
330uF X 1
22uF_0805 X 3
10uF_0603 X 7
4.7uF_0603 X 2
1uF_0402 X 5

For NV N17P latest spec

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

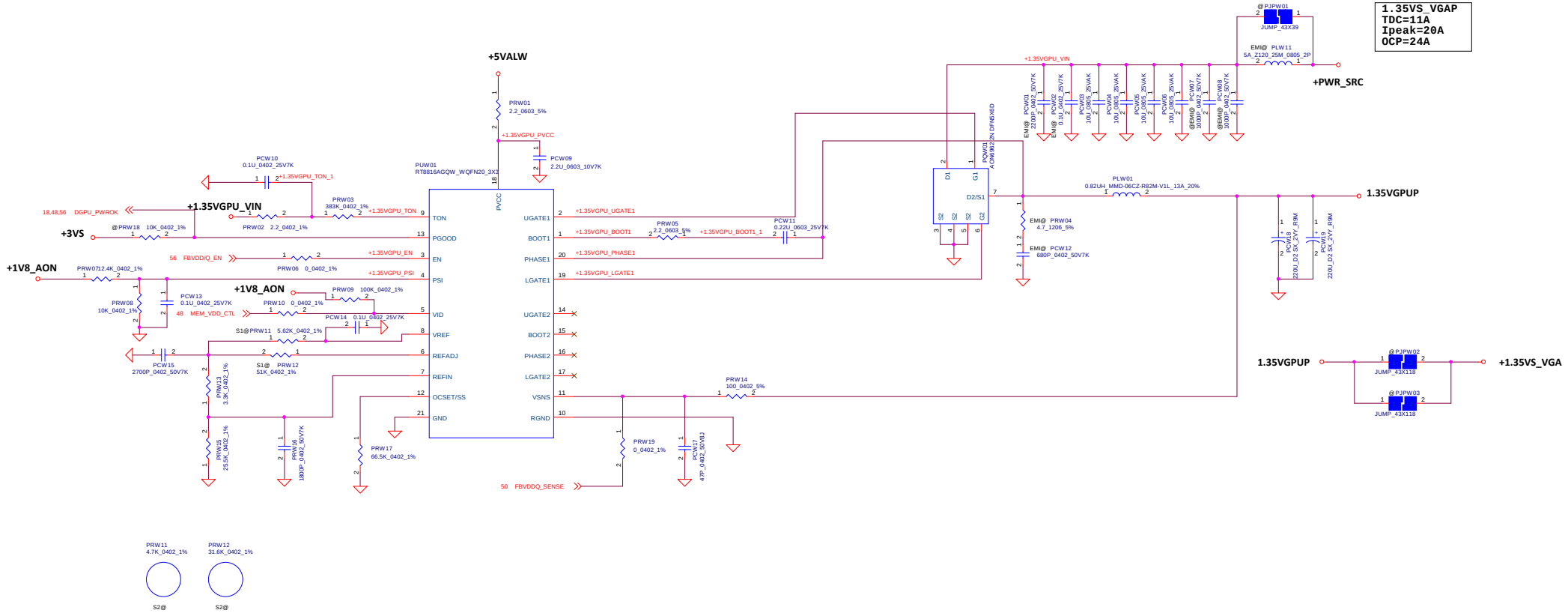
Compal Electronics, Inc.

Title: **VGA DECOUPLING**

Size | Document Number: **LA-F611P** | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 75 of 78

Main Func = +1.35VGPUP



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW11	PRW12
S1@ (4G)	N17P-G0/G1	256Mx32	Micron	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Hynix	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Samsung	1.35V & 1.5V	5.62K	51K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Hynix	1.35V & 1.55V	4.7K	31.6K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Samsung	1.35V & 1.55V	4.7K	31.6K

MEM_VDD_CTL	+MVDD
L	1.35V
H	1.5V/1.55V

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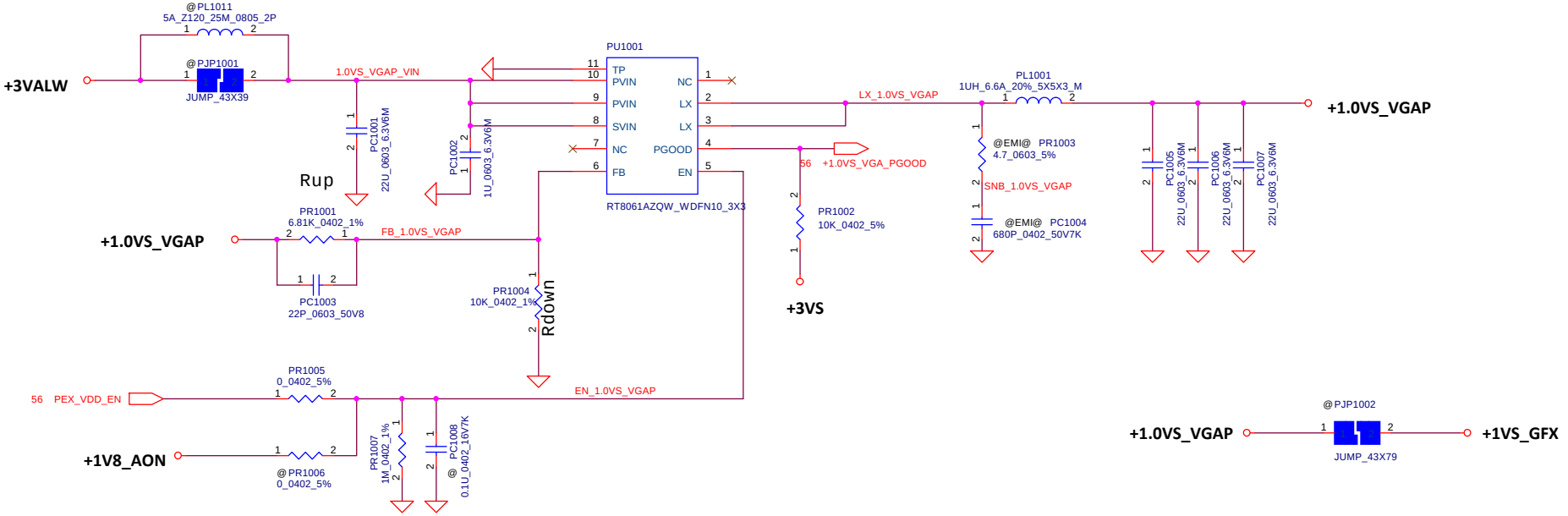
Title: +1.35VGPUP

Size | Document Number: LA-F611P | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 76 of 78

Main Func = 1VS_GFX

+1VS_GFX
TDC 0.88A
Peak Current 1.1A
OCP current 4A



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+1VS_GFX**

Size | Document Number: **LA-F611P** | Rev: 0.1

Date: Thursday, March 22, 2018 | Sheet 77 of 78

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							
5							
6							
7							
8							

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **Changed-List PWR History**

Size	Document Number	Rev
		0.1

Date: Thursday, March 22, 2018 Sheet 78 of 78