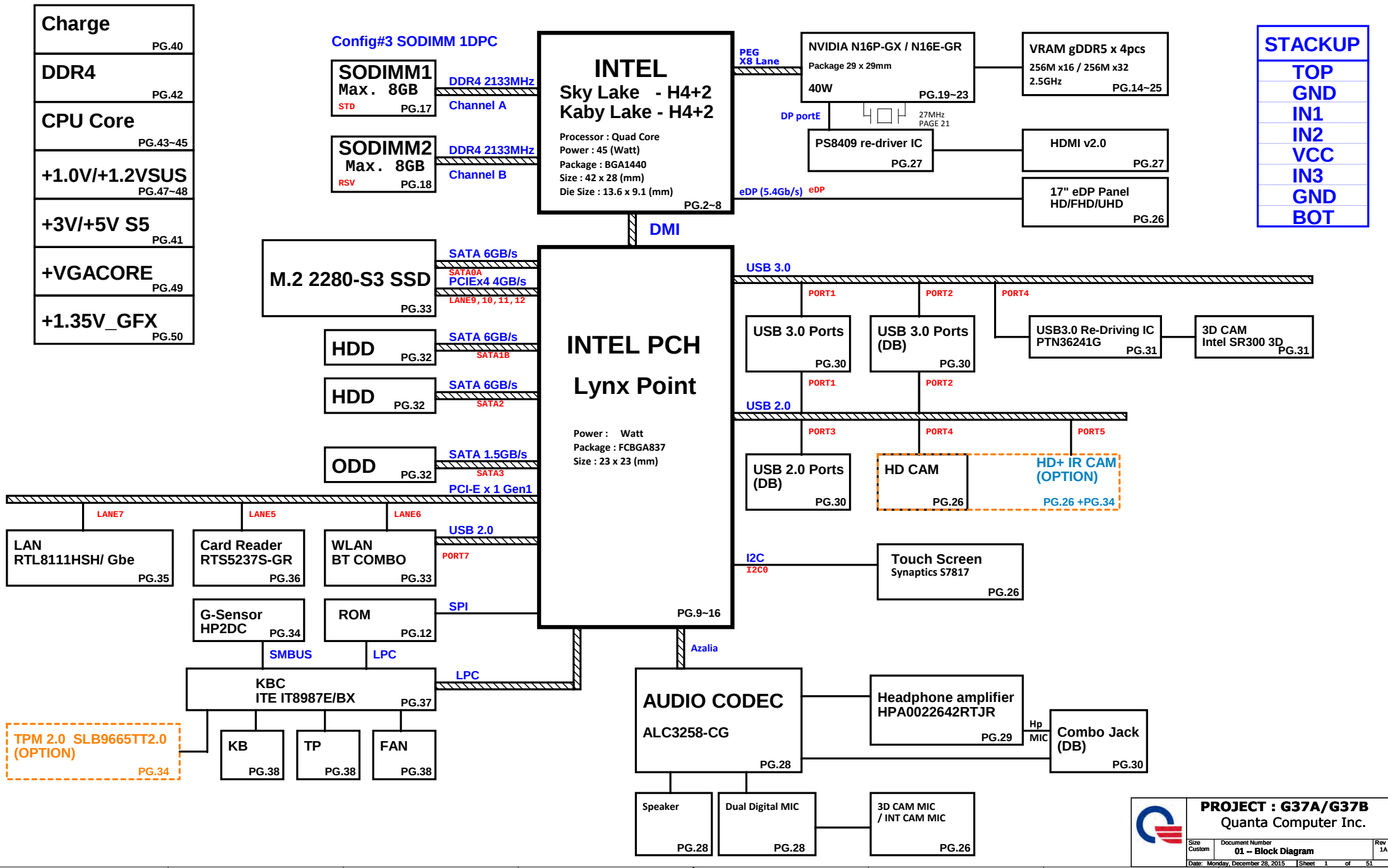
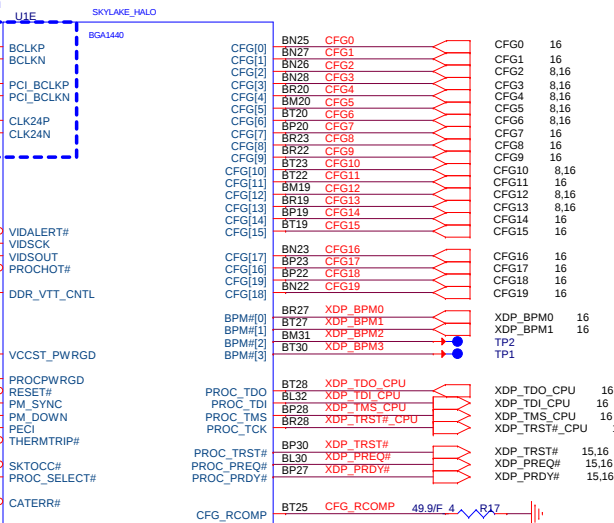
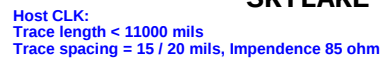
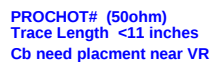
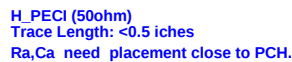


# POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM

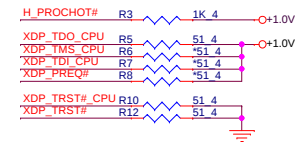
01





**Design Note(CFG\_RCOMP):**  
**DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)**

### Processor pull-up (CPU)

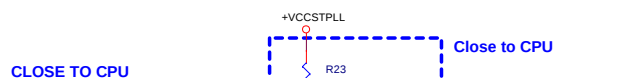


## CPU CORE SVID

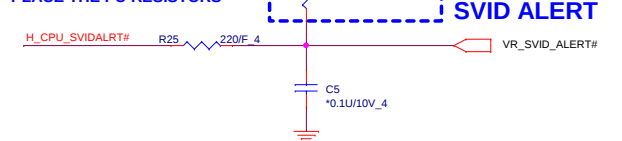
Layout note:

1. Need routing together
2. ALERT need between CLK and DATA.

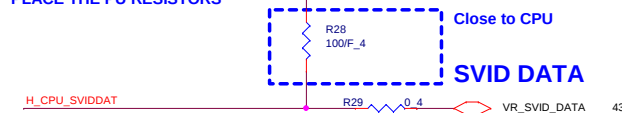
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



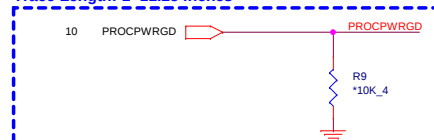
CLOSE TO CPU  
PLACE THE PU RESISTORS



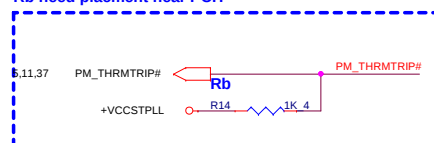
**CLOSE TO CPU  
PLACE THE PU RESISTORS**



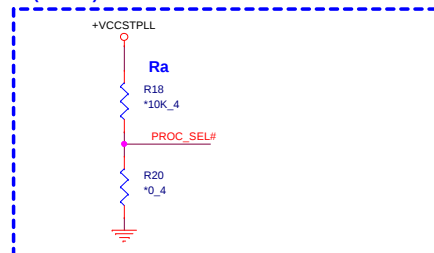
PROCPWRGD (50ohm)  
Trace Length: 1~11.25 inches



**THERMTRIP# (50ohm)**  
Trace Length: 1.1~12 inches  
Rb need placment near PCH

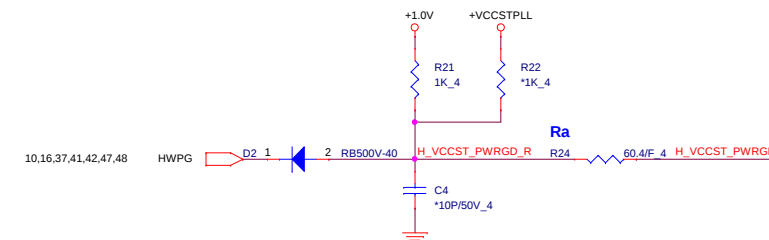


**Ra(R10804) Not install in SKL-H**



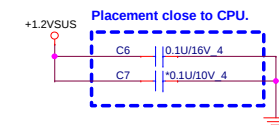
## HWPD

Ra close to CPU side  
H VCCST PWRGD trace 0.3" - 1.5"



## CPU VDDQ

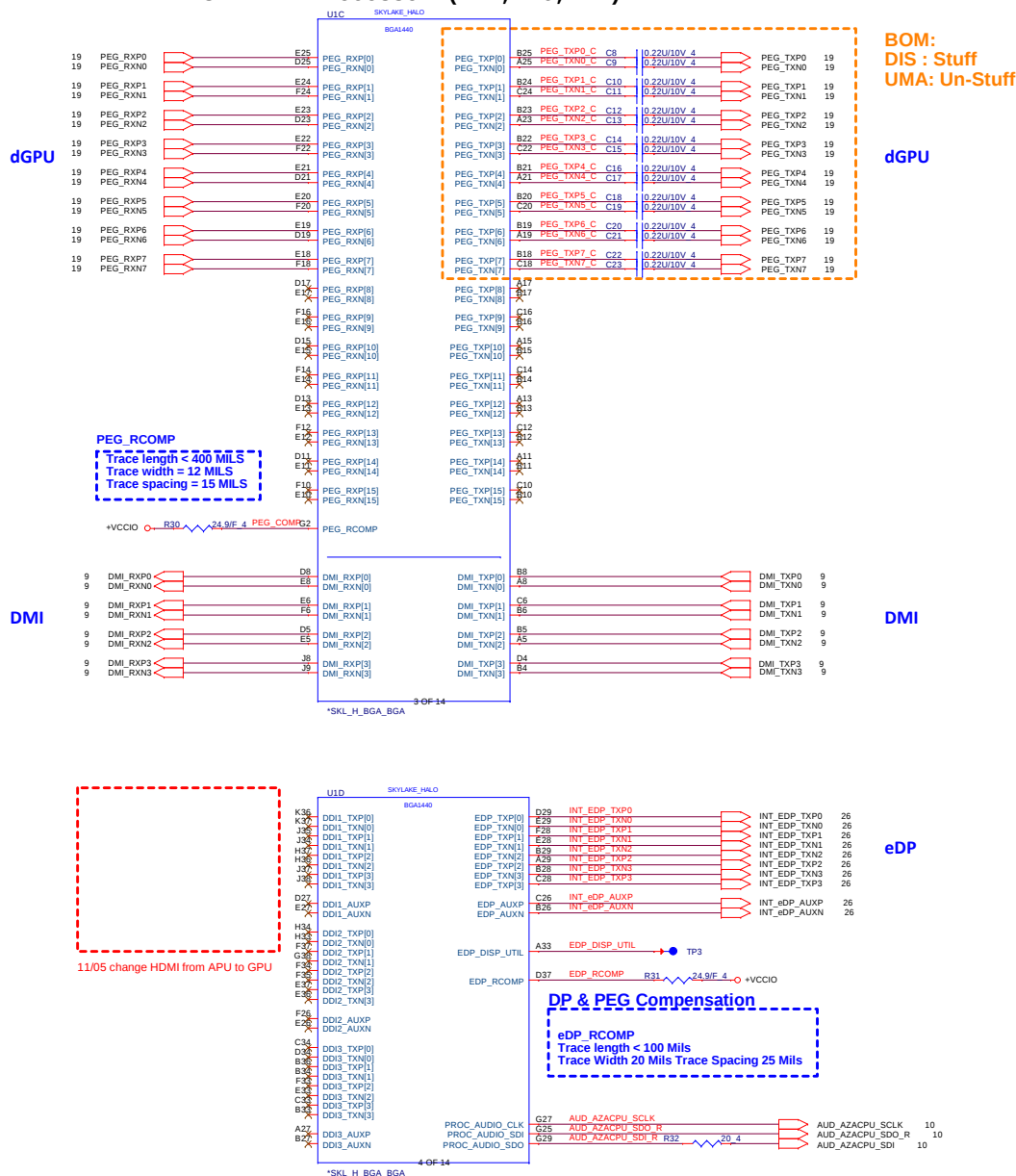
Note: please keep plane is enough for VDDQ 2.8A



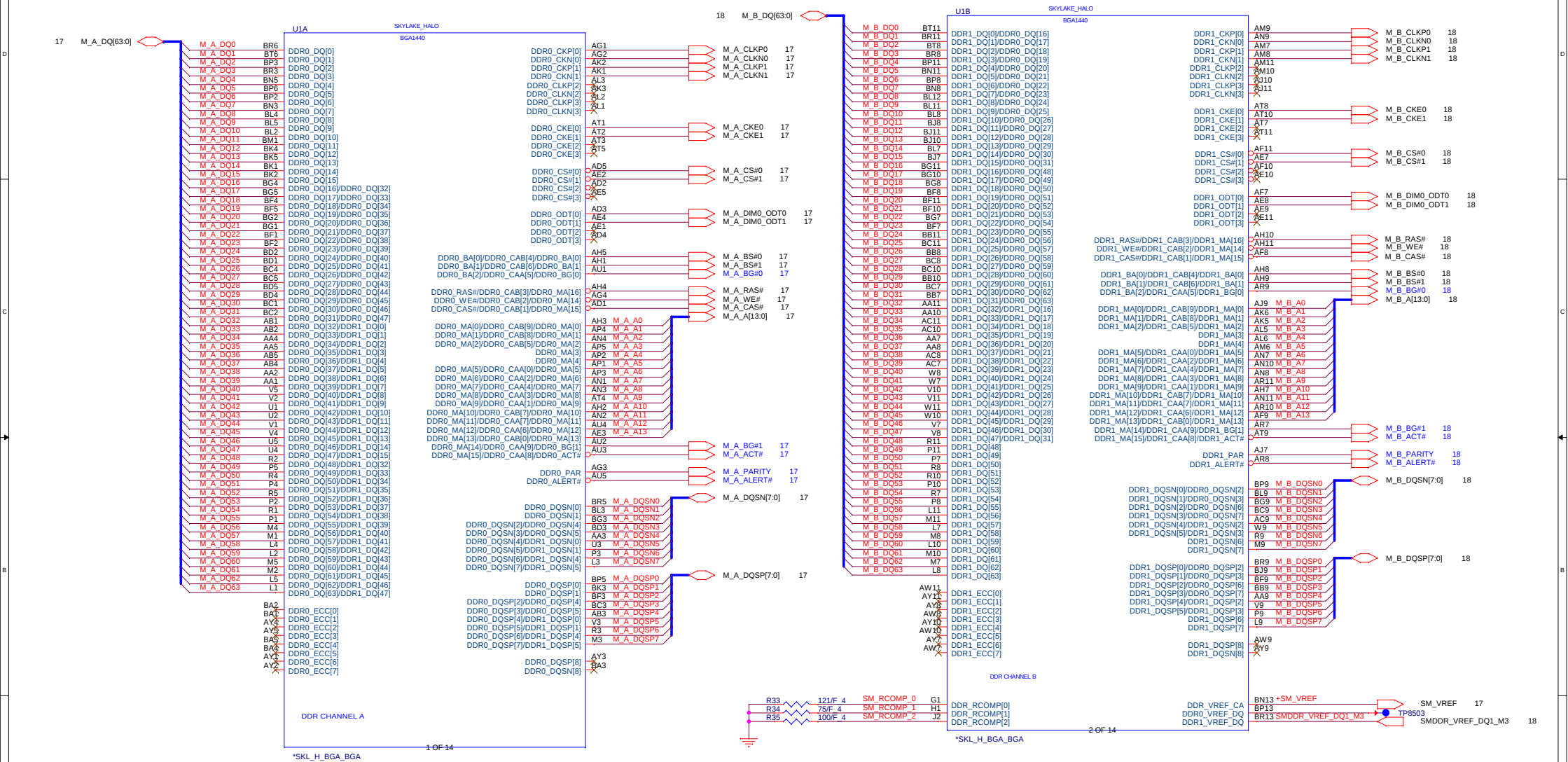
**PROJECT : G37A/G37B**  
Quanta Computer Inc.

|                                 |                                                     |               |
|---------------------------------|-----------------------------------------------------|---------------|
| Size Custom                     | Document Number<br><b>02 -- SKL 1/7 (JTAG/MISC)</b> | Rev 1A        |
| Date: Monday, December 28, 2015 |                                                     | Sheet 2 of 51 |

## SKYLAKE Processor (DMI, PEG, FDI)



## SKYLAKE Processor (DDR4)



+3VPCU 10,30,33,37,38,40,41  
 +3V 9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +1.0V 2,6,10,16,37,48  
 +VCCGT 7,43,45

## SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

1123 Change C27, C29, C33 PN and FP from 0805 to 0603

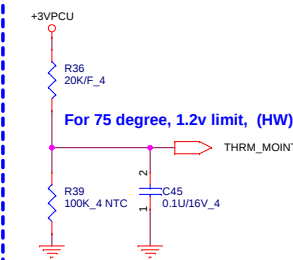
1022 Change C27, C29, C33 PN and FP from 0603 to 0805



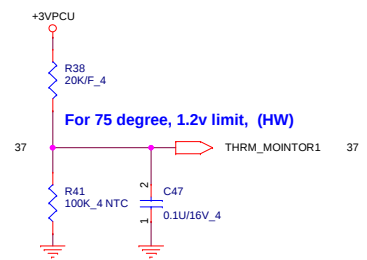
### IO Thrm Protect

Location need thermal confirm

For CPU USE

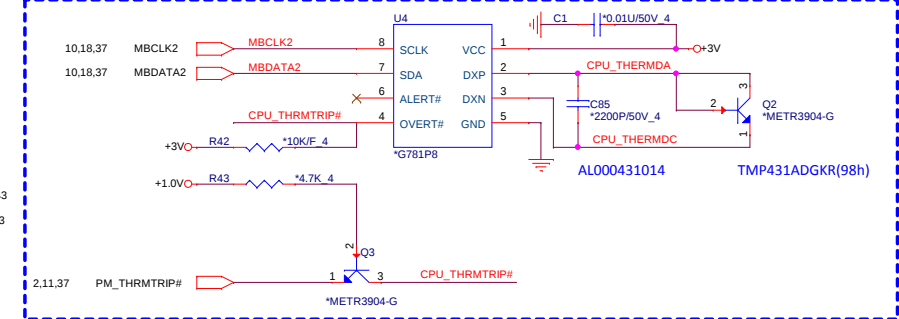


For PIPE USE



### CPU Thermal Sensor

Location need thermal confirm

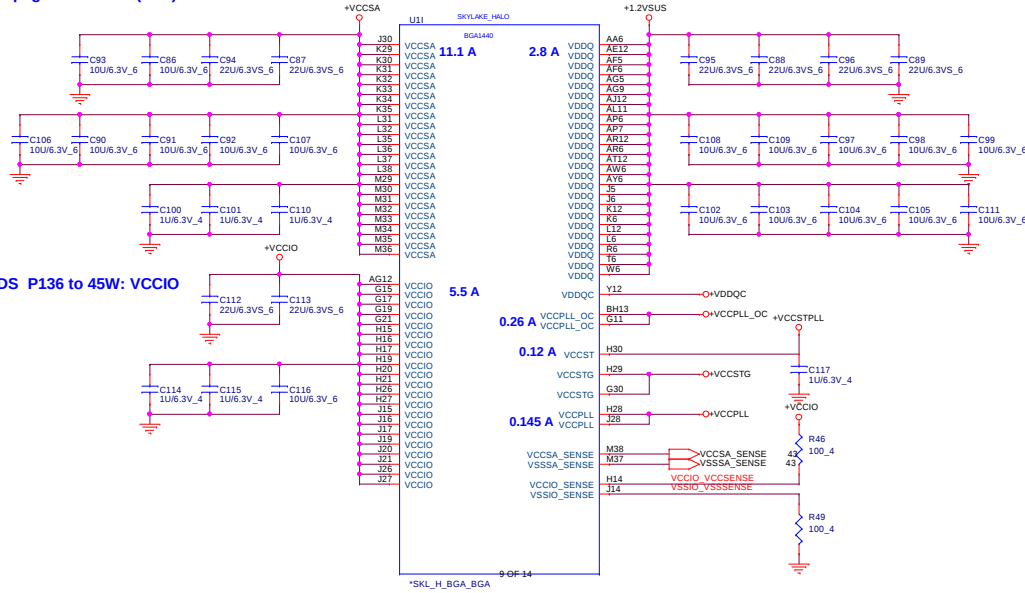


|           |                        |
|-----------|------------------------|
| +1.2VSUS  | 2,10,17,18,42,46,48,51 |
| +VCCIO    | 3,16,48                |
| +VCCSTPLL | 2,43,47                |
| +VCCSA    | 43,49                  |

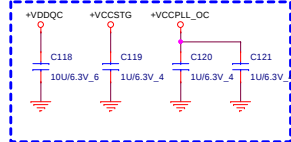
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A

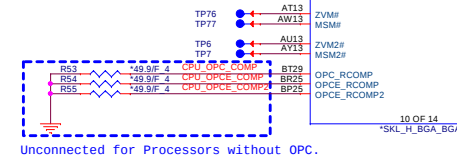
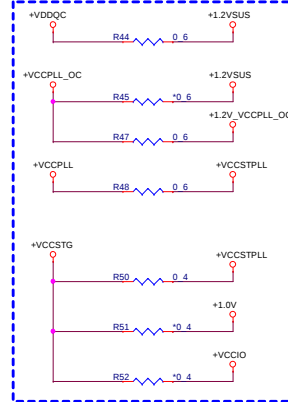
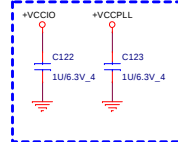
Follow SKL H EDS P136 to 45W: VCCIO  
+VCCIO = 0.95V



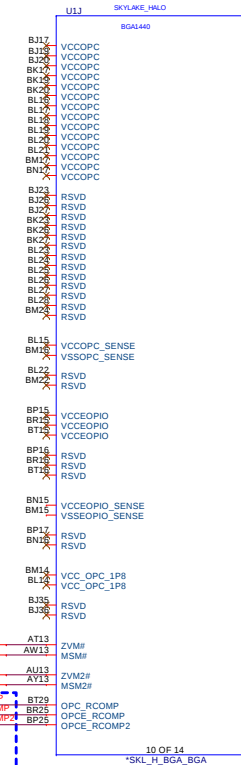
#### Under CPU



#### Close CPU

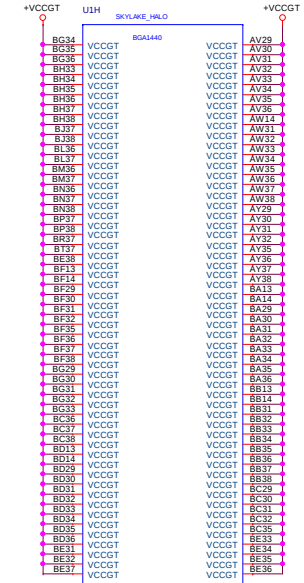
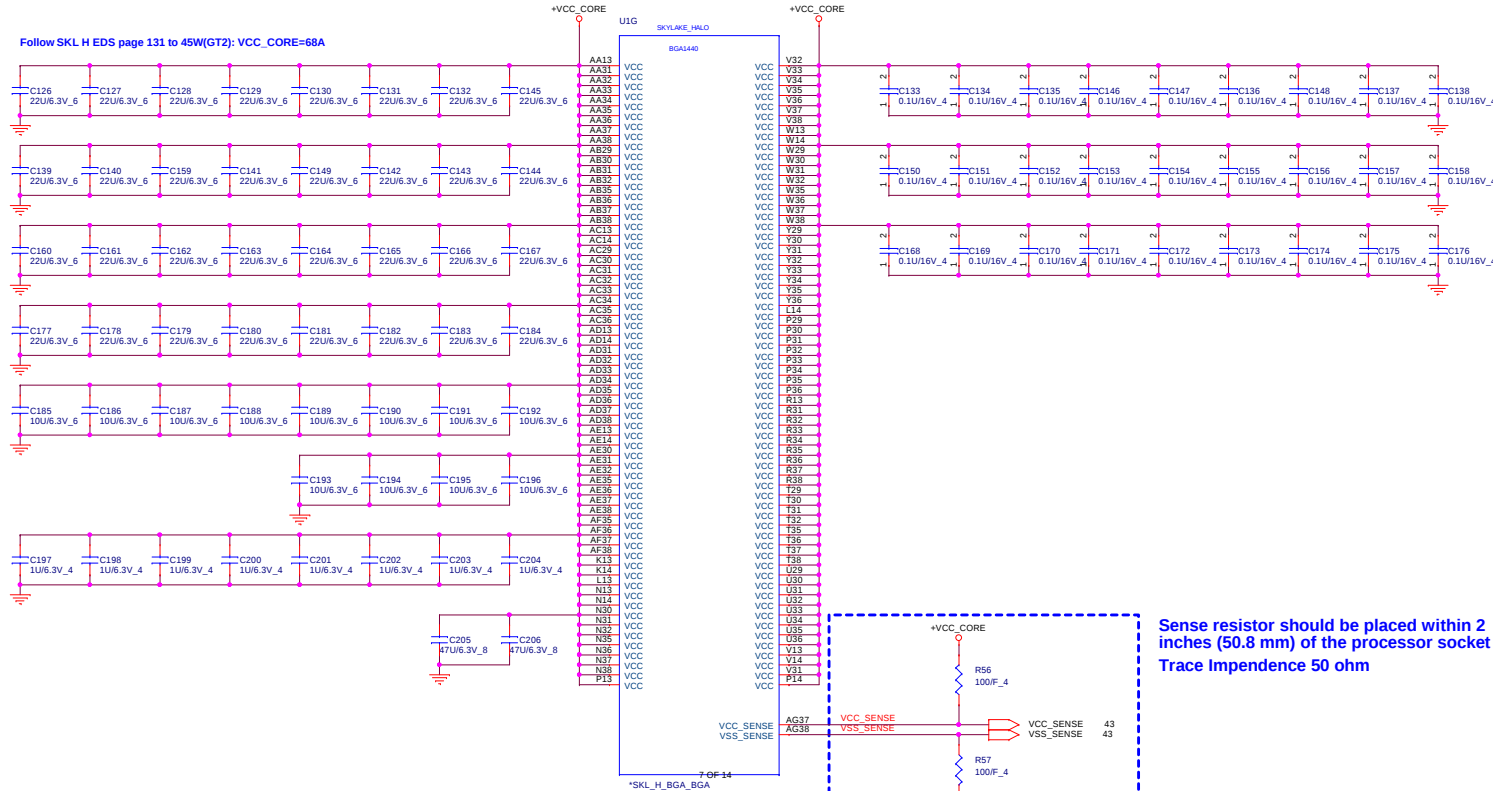


Unconnected for Processors without OPC.



+VCC\_CORE 44  
+VCCGT 5,43,45

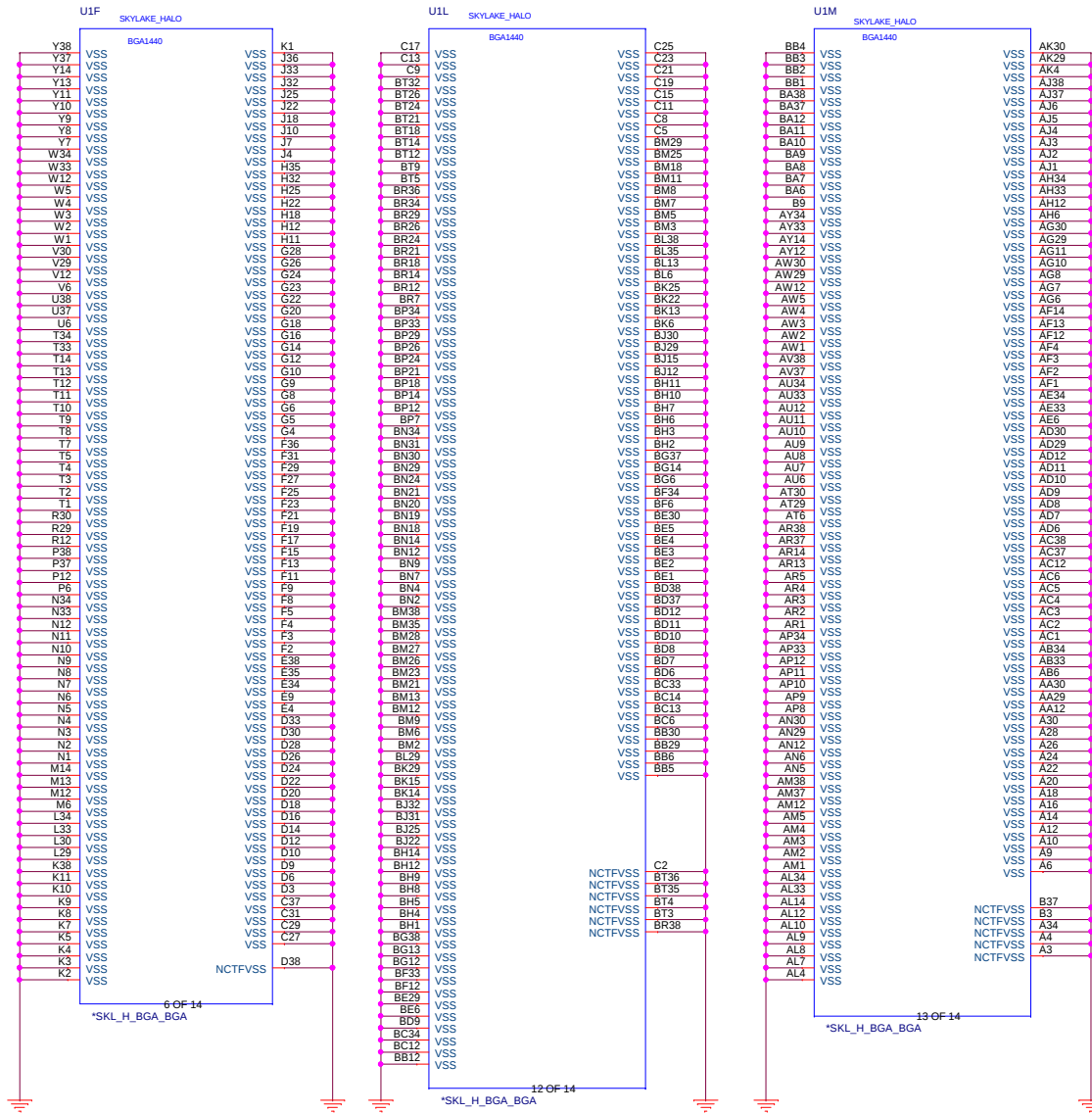
Follow SKL H EDS page 131 to 45W(GT2): VCC\_CORE=68A



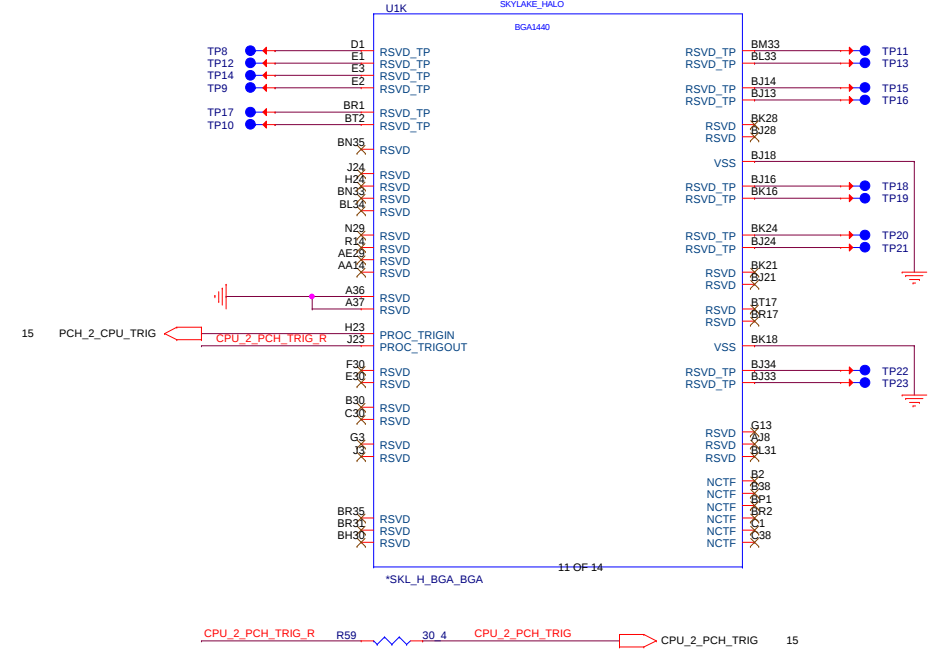
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

| Size                            | Document Number            | Rev           |
|---------------------------------|----------------------------|---------------|
| Custom                          | 07 -- SKL 6/7 (POWER&GND ) | 1A            |
| Date: Monday, December 28, 2015 |                            | Sheet 7 of 51 |

# SKL-HProcessor (GND)



# SKL-H Processor (RESERVED, CFG)

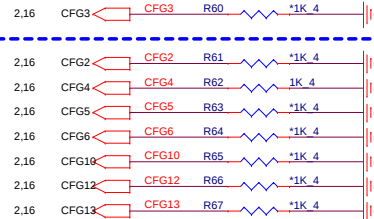


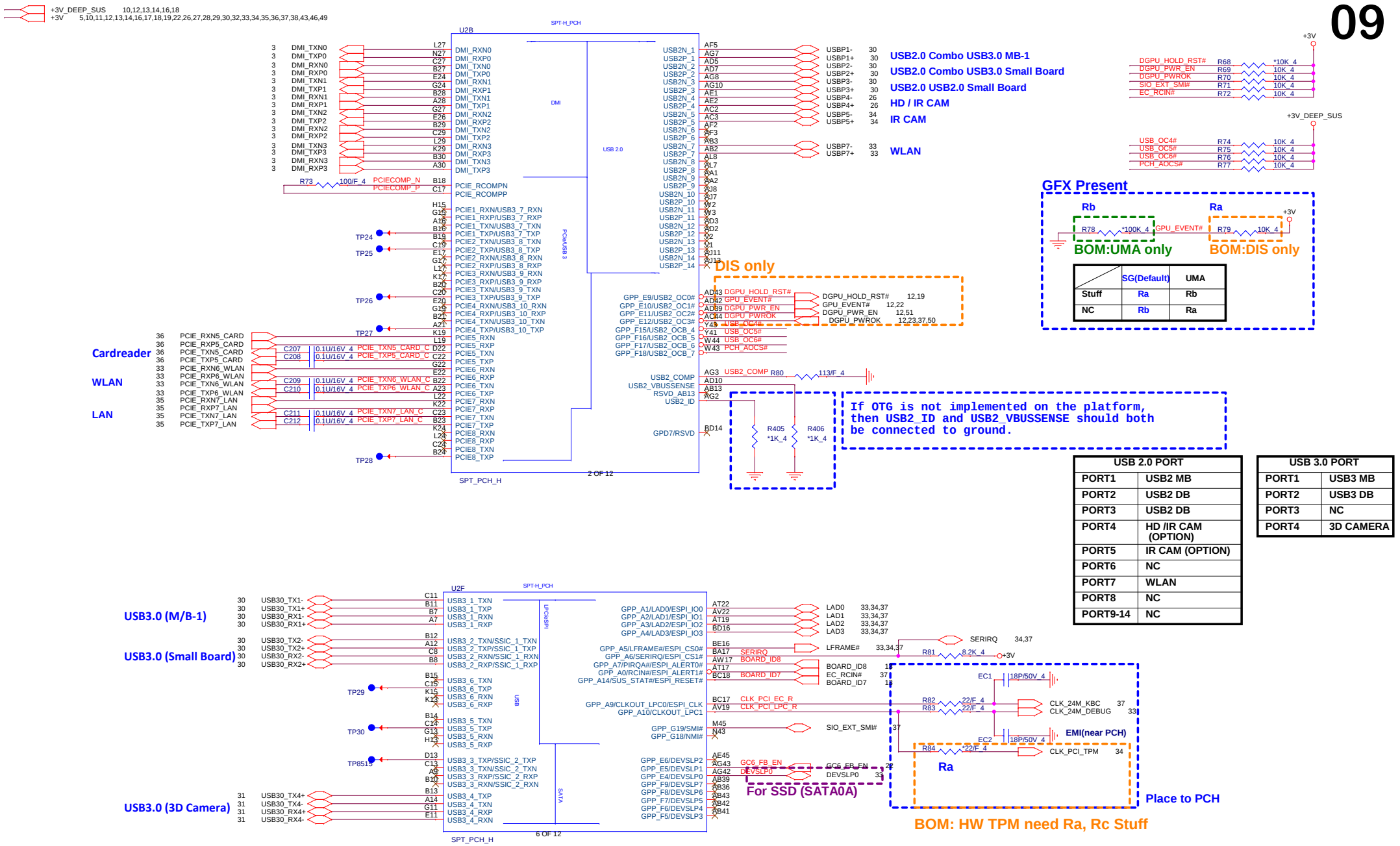
## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX\_ENABLED BIT IN DEBUG

1, Disable;







+3V 5,9,10,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
+1.0V\_DEEP\_SUS 10,14,16,47,49

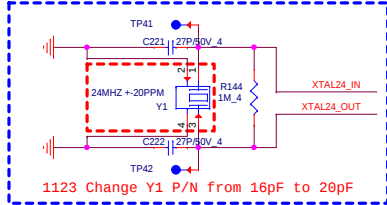
| HSIO MUX PORT |              |
|---------------|--------------|
| PCIE1-4       | NC           |
| PCIE5         | Cardreader   |
| PCIE6         | Wlan         |
| PCIE7         | Lan          |
| PCIE8         | NC           |
| PCIE9/SATA0A  | SSD PCIE x 4 |
| PCIE10        |              |
| PCIE11        |              |
| PCIE12        |              |
| PCIE13        | NC           |
| PCIE14        | HDD-1        |
| PCIE15        | HDD-2        |
| PCIE16        | ODD          |
| PCIE17        | NC           |
| PCIE18-20     | NC           |

SSD PCIE x4 LANE

HDD-1 (SATA1B 6Gb/s)

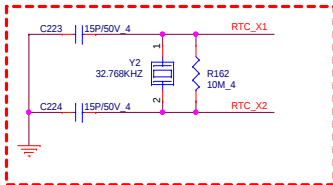
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

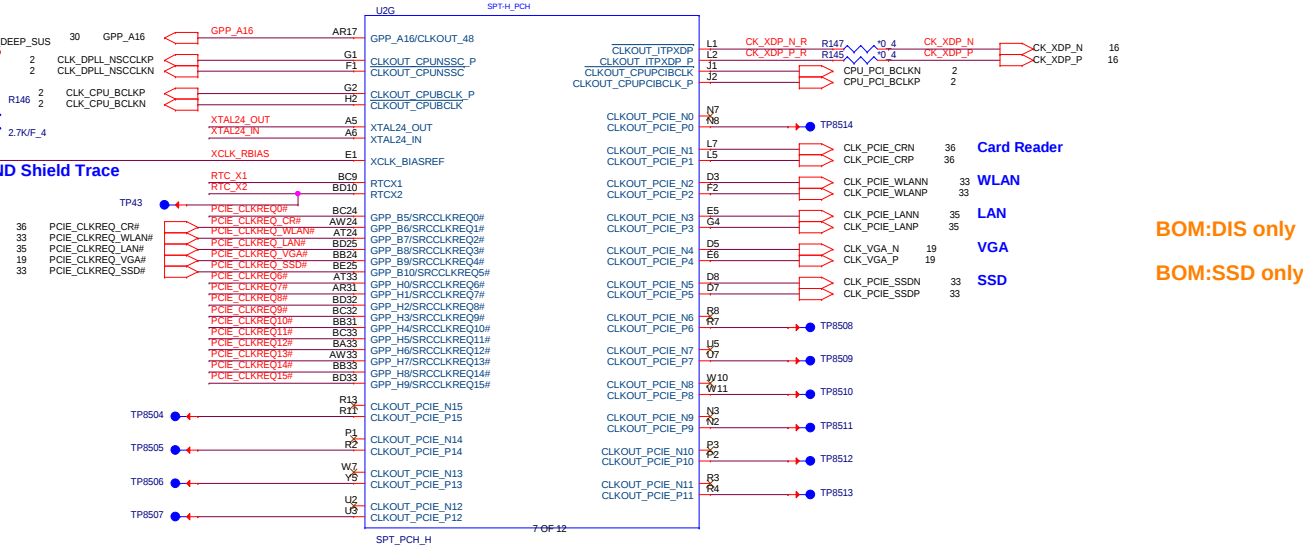
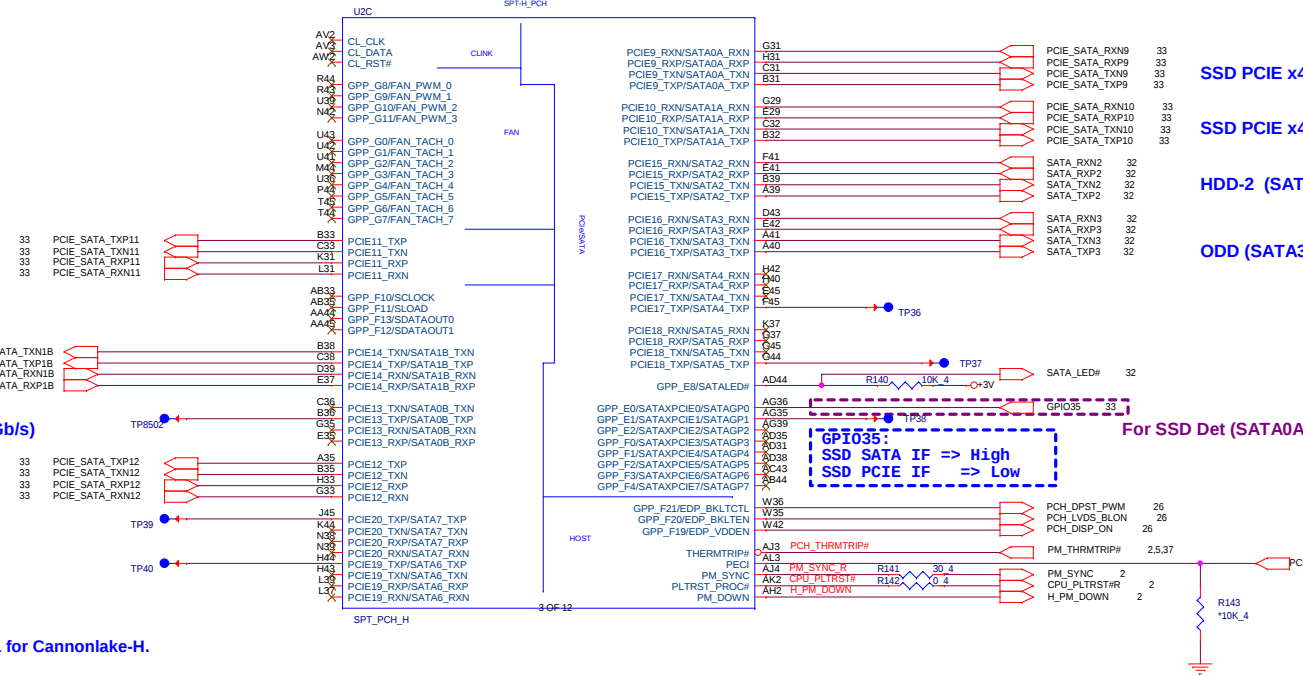


Crystal Components with Surrounding 10 mil Wide GND Shield Trace  
Break Out:4-10 mil Wide GND Shield Trace

### RTC Clock 32.768KHZ



12/28 Change C223, C224 PN from CH01806JB07 to CH01506JB06 for XTAL vendor suggest

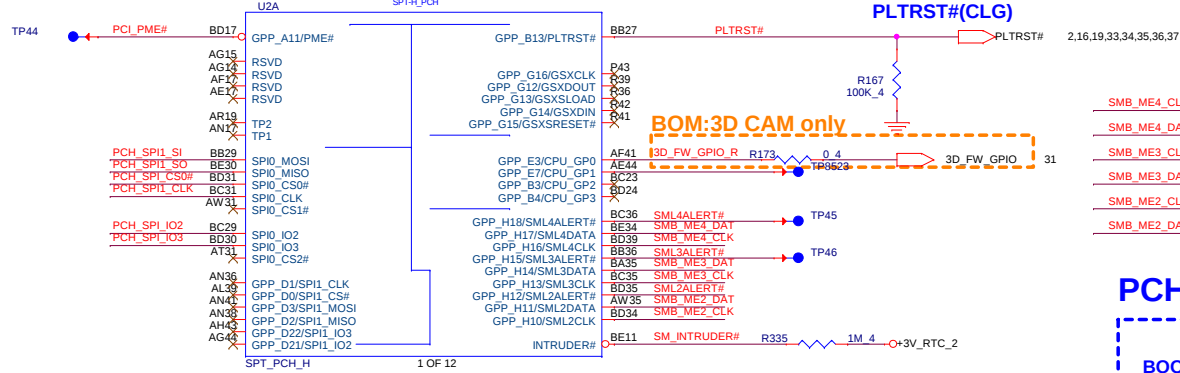




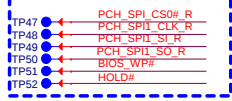
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

|                                 |                                             |        |
|---------------------------------|---------------------------------------------|--------|
| Size Custom                     | Document Number 11 - PCH 3/7 (SATA/LPC/CLK) | Rev 1A |
| Date: Monday, December 28, 2015 | Sheet 11 of 51                              |        |

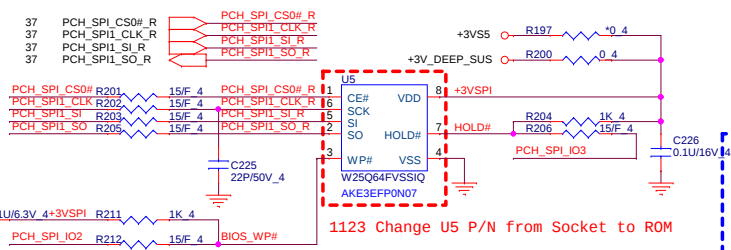
+3V\_RTC\_2 10,14  
+3VSS 10,14,16,26,33,37,41,42,46,47,48,51  
+3V\_DEEP\_SUS 9,10,13,14,16,18  
+3V 5,9,10,11,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49



## PCH SPI ROM (CLG)

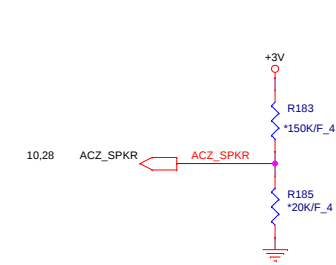


## Place to BOT



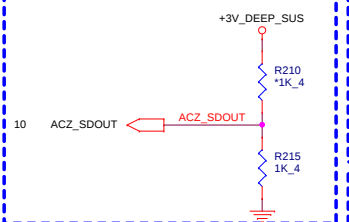
## TOP SWAP OVERRIDE STRAP

HIGH: TOP SWAP ENABLED (CRB)  
LOW: TOP SWAP DISABLED (DEFAULT)



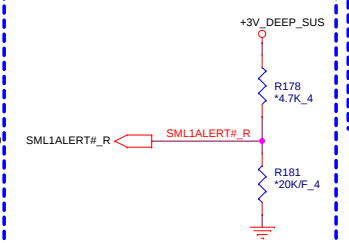
## TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)  
LOW: security measures defined in the Flash Descriptor. (Default)



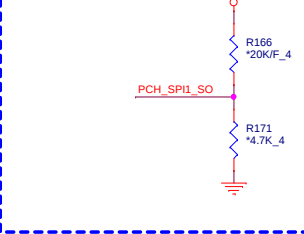
## RESERVED

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



## RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



## ESPI FLASH SHARING MODE

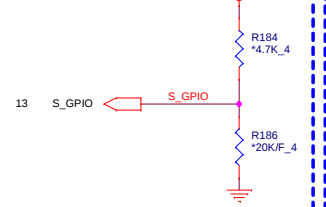
HIGH: SLAVE ATTACHED FLASH SHARING  
LOW: 0: MASTER ATTACHED FLASH SHARING  
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



## PCH Strap Pin

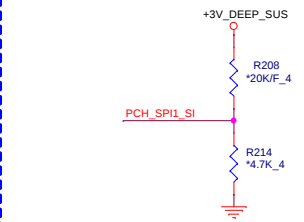
## BOOT SELECT STRAP

HIGH: LPC  
LOW: SPI. (Default)

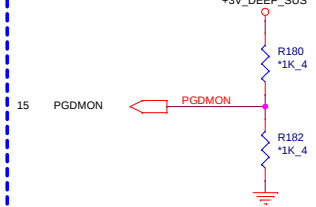


## RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

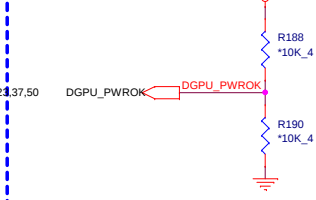


## DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW

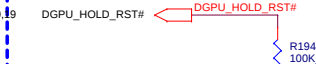


## DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



## RING OSCILLATOR BYPASS



## XTAL INPUT FREQUENCY[0]

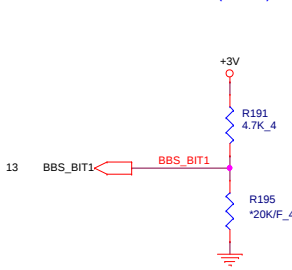


## XTAL INPUT FREQUENCY[1]



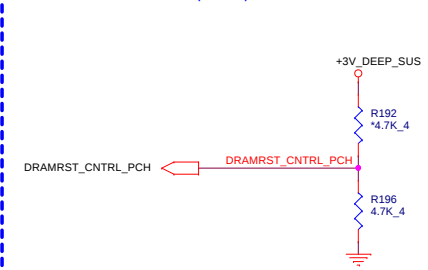
## NO REBOOT IF SAMPLED HIGH

HIGH: TOP SWAP ENABLED (CRB)  
LOW: Disable "No Reboot" mode. (Default)



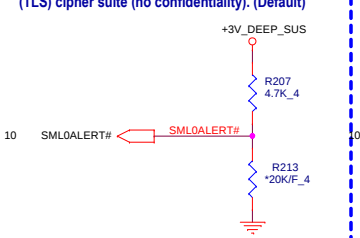
## ESPI/LPC SELECT STRAP

HIGH: eSPI is selected for EC.  
LOW: LPC is selected for EC. (Default)



## TLS CONFIDENTIALITY ENABLED

HIGH: Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)  
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



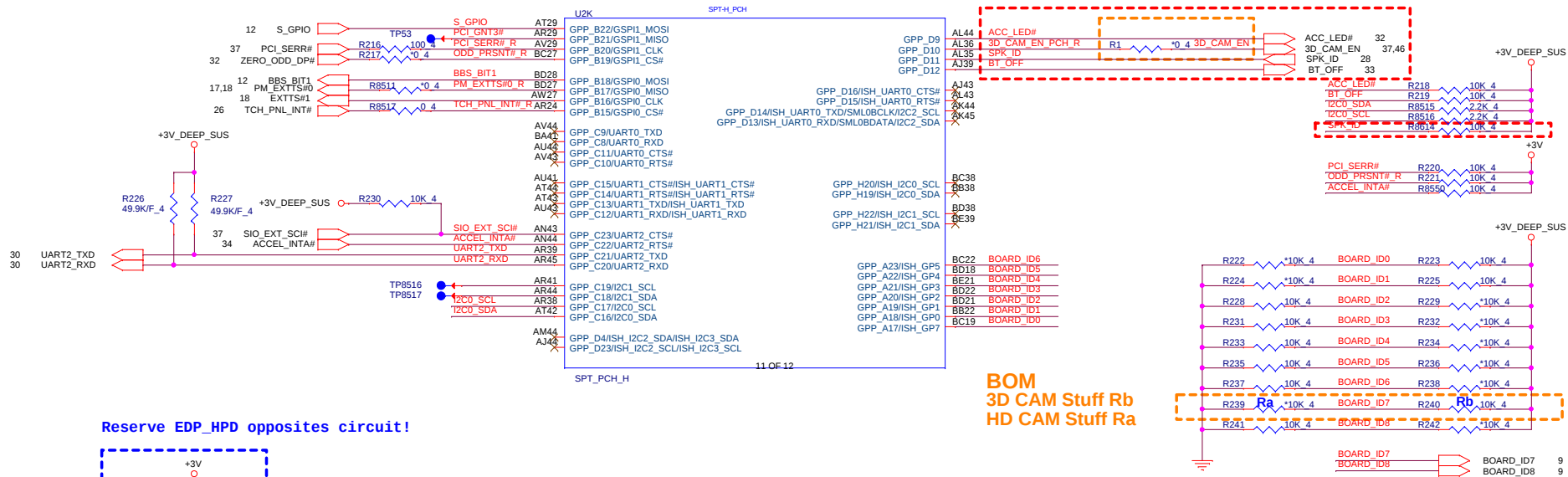
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

| Size                            | Document Number           | Rev |
|---------------------------------|---------------------------|-----|
| Custom                          | 12 -- PCH 4/7 (GPIO/MISC) | 1A  |
| Date: Monday, December 28, 2015 | Sheet 12 of 51            |     |

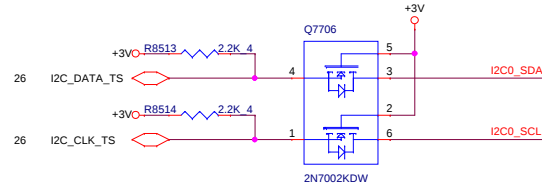
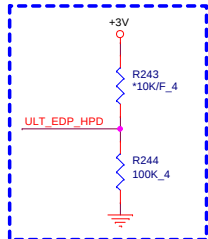
+3V\_DEEP\_SUS 9.10.12.14.16.18  
+3V 5.9.10.11.12.14.16.17.18.19.22.26.27.28.29.30.32.33.34.35.36.37.38.43.46.49

1123 Change PCH GPP\_D11 Net name from RF\_OFF to SPK\_ID and  
PU10K to +3V\_DEEP\_SUS for SPK Vendor ID used

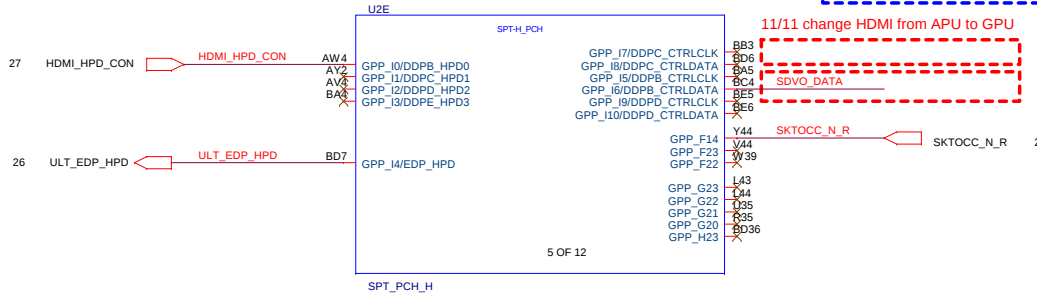
### 3D CAMERA BOM: 3D CAM Un-Stuff (EN will from EC control)

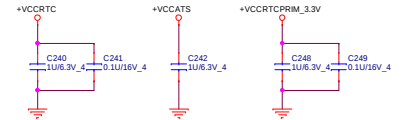


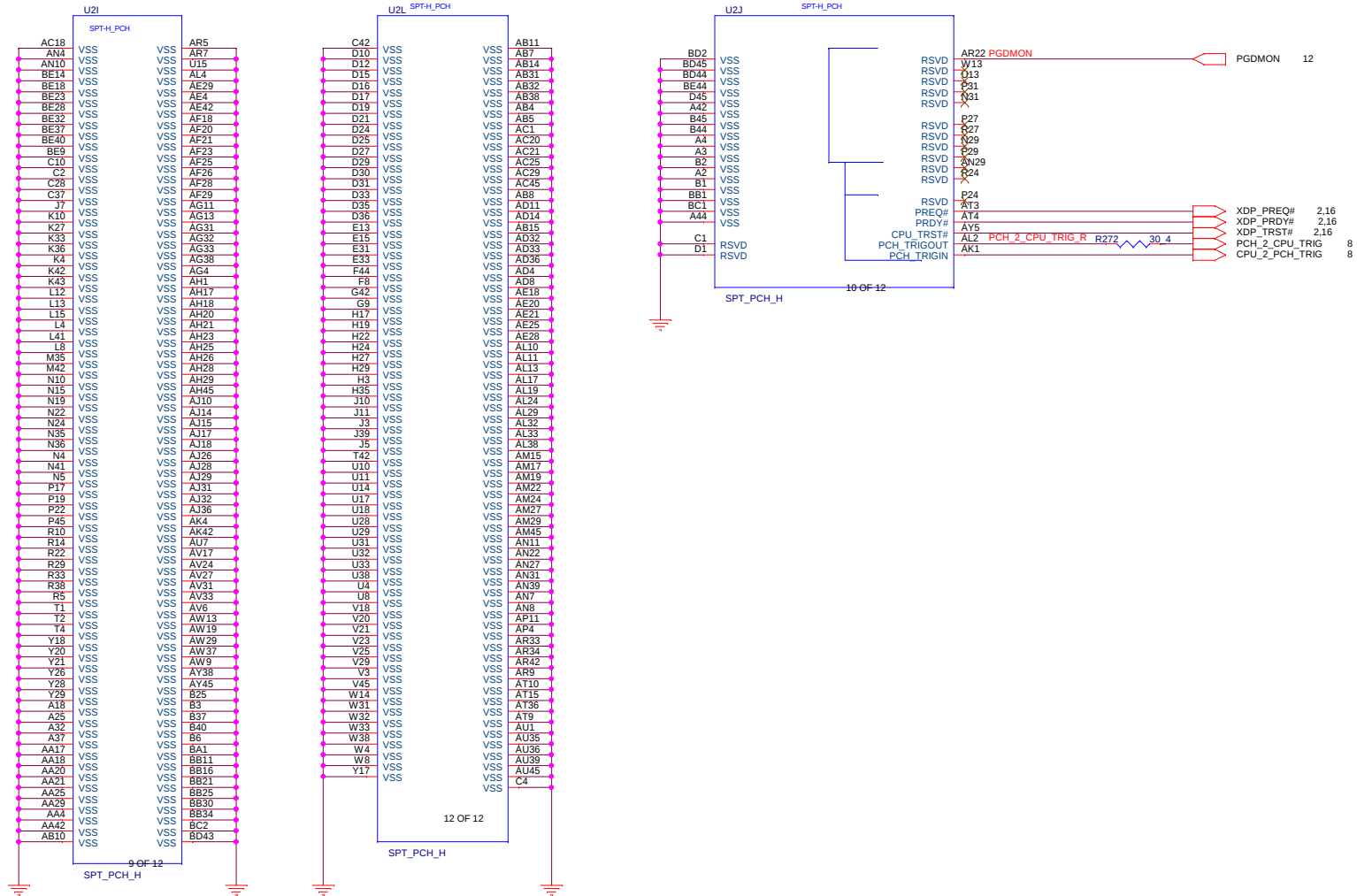
Reserve EDP\_HPD opposites circuit!



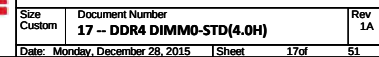
This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.





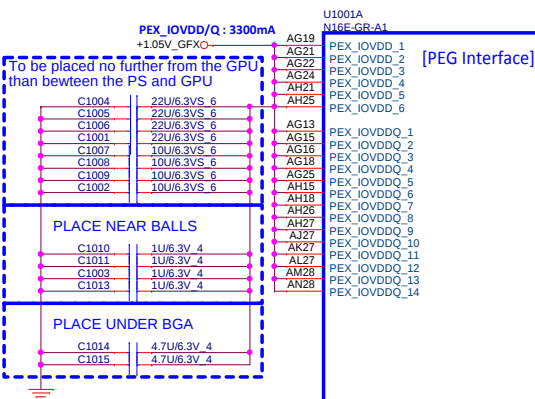




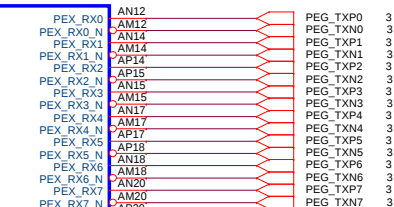
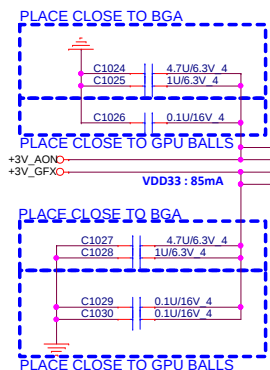




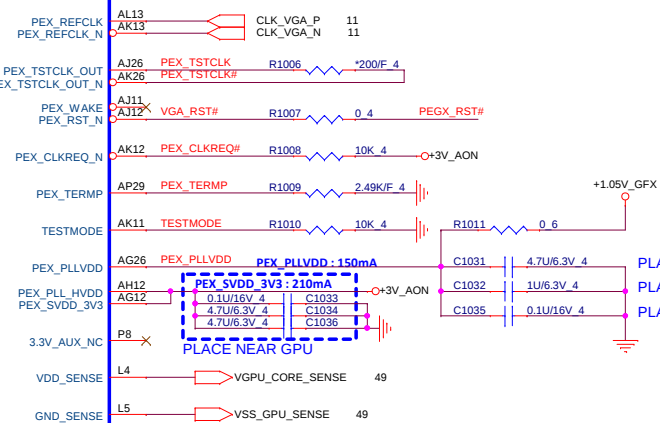
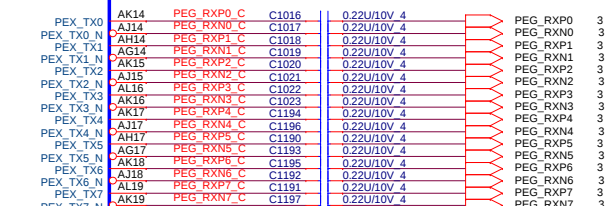
+3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +3V\_AON 22,23,27,51  
 +3V\_GFX 20,21,22,23,49,51  
 +1.05V\_GFX 20,21,23,51



AC6 NC.1  
 AJ28 NC.2  
 AJ4 NC.3  
 AJ5 NC.4  
 AL11 NC.5  
 C15 NC.6  
 D19 NC.7  
 D20 NC.8  
 D23 NC.9  
 D26 NC.10  
 H31 NC.11  
 T8 NC.12  
 V32 NC.13



1126 Change D1004, R1124 from I to NI  
 Change U1002, R1002, C1012 from NI to I

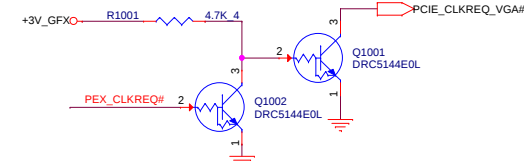
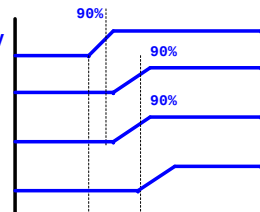


All 3.3V

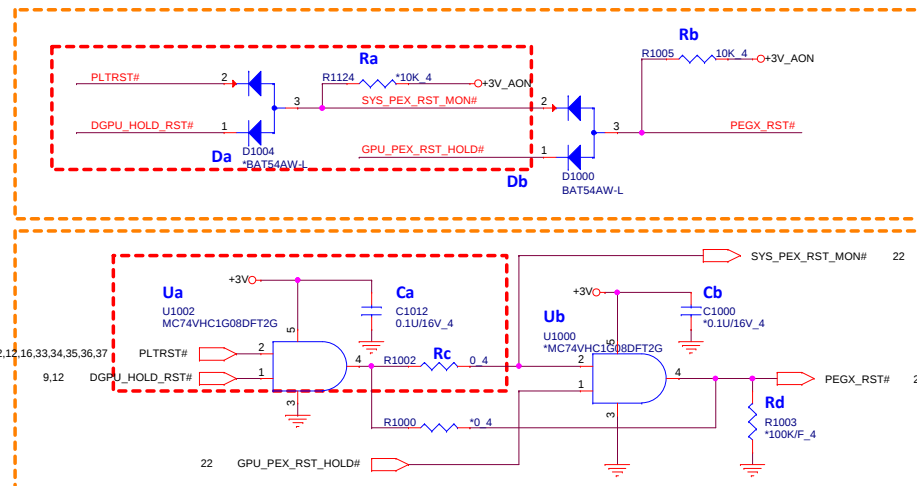
NVVDD

PEX\_VDD  
1.05V

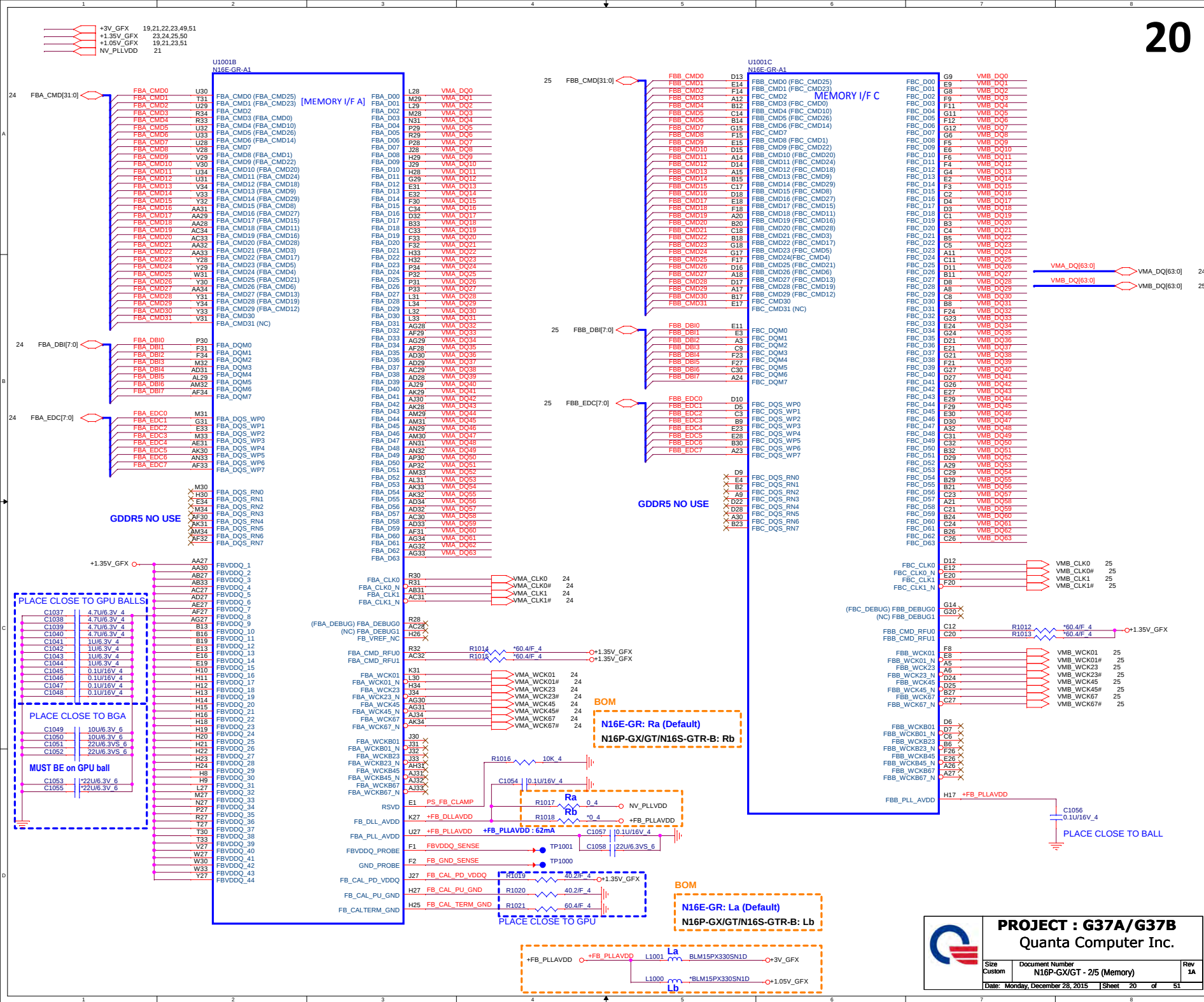
FBVDD/Q

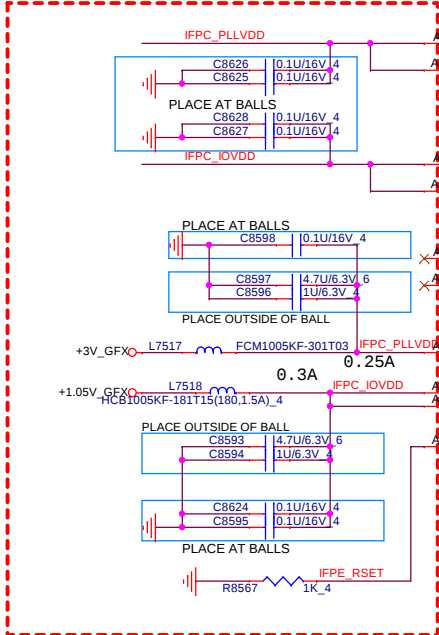


If stuff Da, Db, Ra, Rb, do not stuff Ua, Ub, Ca, Cb, Rc, Rd



| GPU type | Part Number | Part Description                   | Where Used  |
|----------|-------------|------------------------------------|-------------|
| N16P-GT  | AJ0N16P0T05 | IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ | G35A        |
|          | AJ0N16P0T06 | IC CTRL(908P)N16P-GT-A2(BGA)QBCON  |             |
| N16P-GX  | AJ0N16P0T14 | IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ | G35A / G37A |
|          | AJ0N16P0T15 | IC CTRL(908P)N16P-GX-A2(BGA)QBCON  |             |
| N16E-GR  | AJ0N16E0T02 | IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ | G35A / G37A |
|          | AJ0N16E0T03 | IC CTRL(908P)N16E-GR-A1(BGA)QBCON  |             |



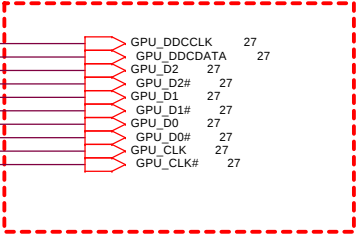
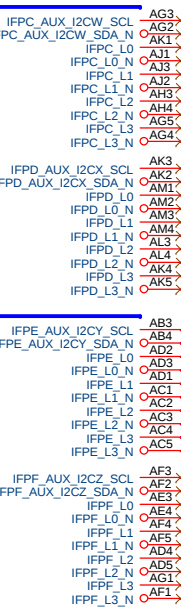


[IFPC/D\_TMSD]

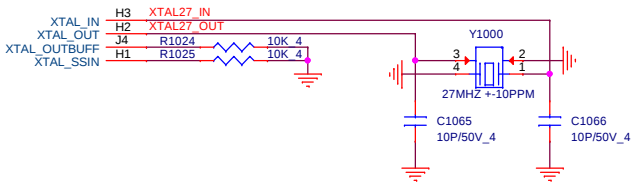
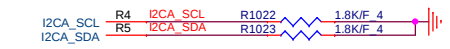
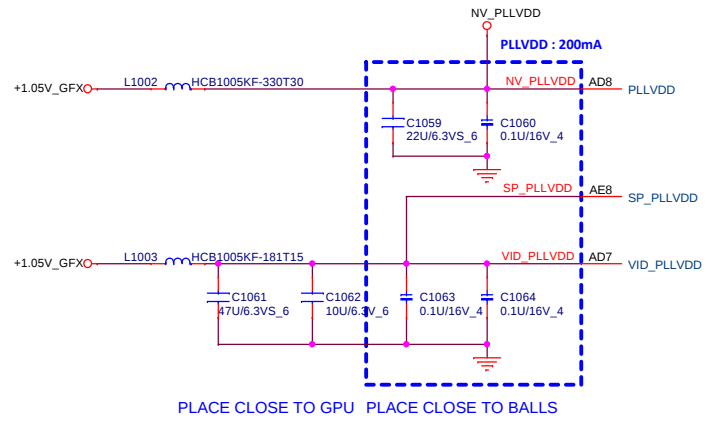
[IFPE/F\_DP]

[DACA/B\_CRT]

[XTAL IN]



11/05 change HDMI from APU to GPU



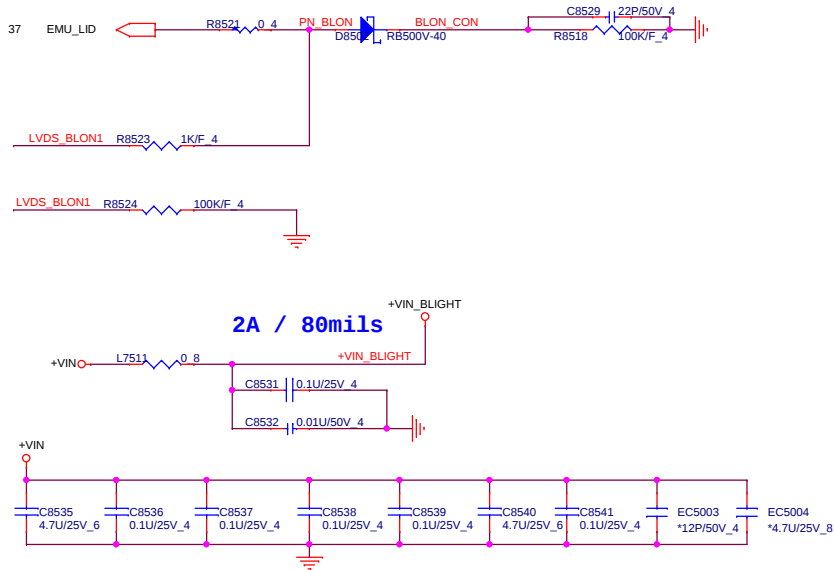




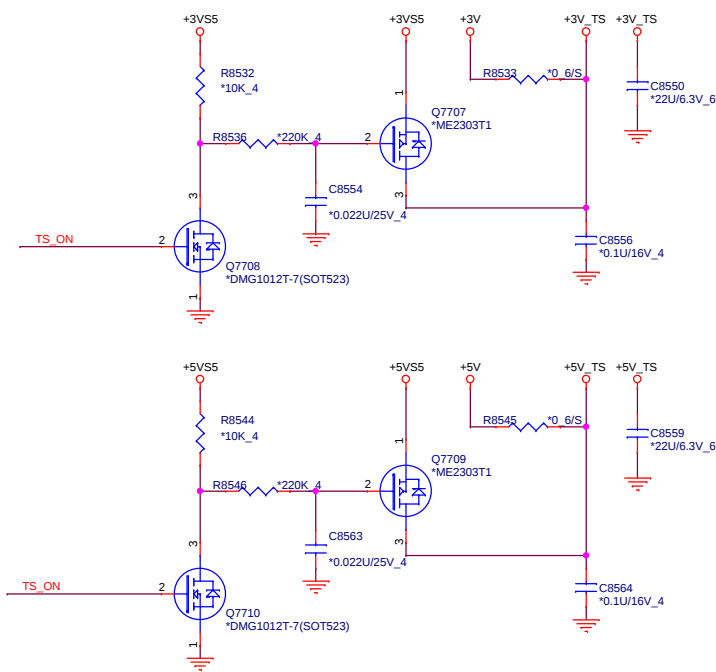




# LID Switch



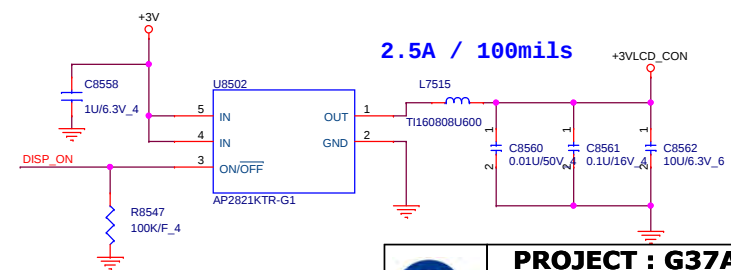
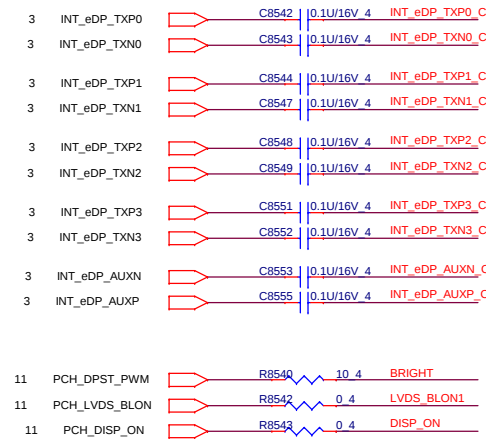
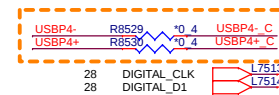
# Touch screen



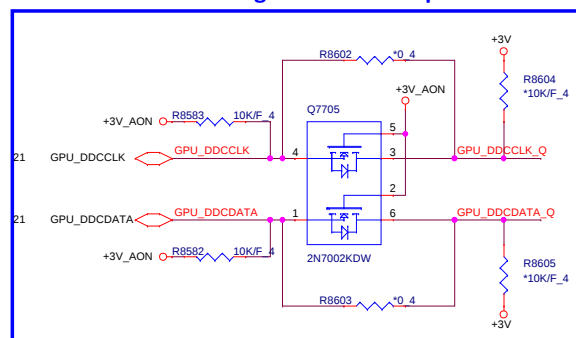
## eDP Conn.

| MB              | TS (I/F: I2C) |
|-----------------|---------------|
| +3V_TS          | VDD33         |
| I2C_DATA_TS     | SDA           |
| I2C_CLK_TS      | SCL           |
| TCH_PNL_RST#_EC | EXRESETN      |
| TCH_PNL_INT#    | ATTN          |
| TS_ON           | Report_Switch |
| GND             | GND           |

BOM: HD CAM Stuff  
BOM: 3D CAM Un-Stuff



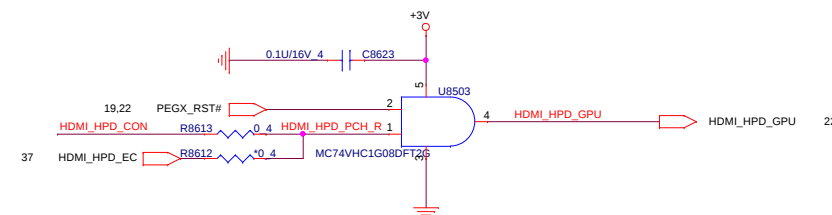
## Prevent current leakage when GPU is power off



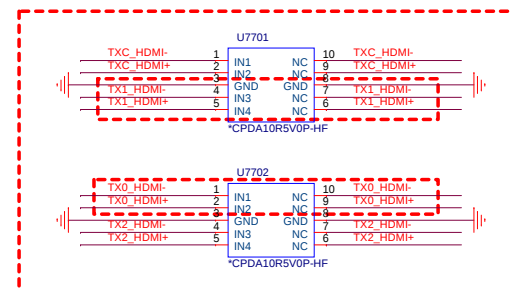
## EMI Solution



1127 Change P/N from CH+7506XB02 to CH+7506TB01

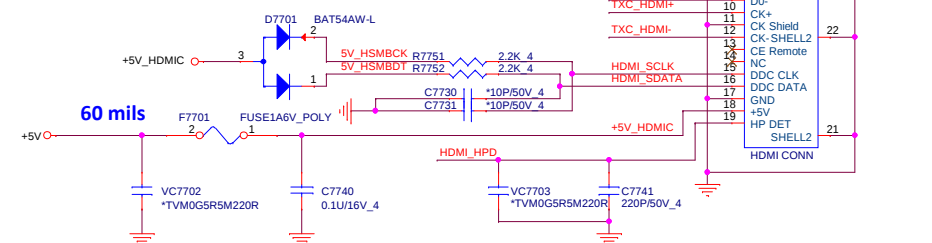


## ESD

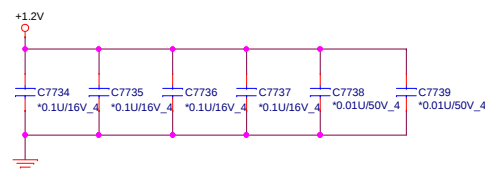
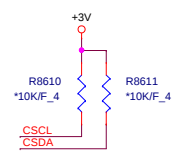


1124 Reserve ESD protection component

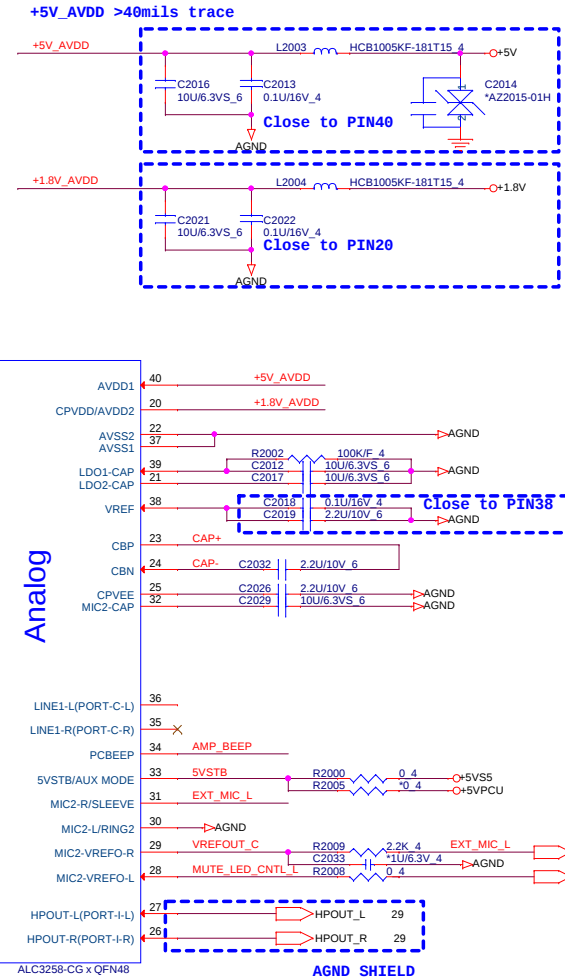
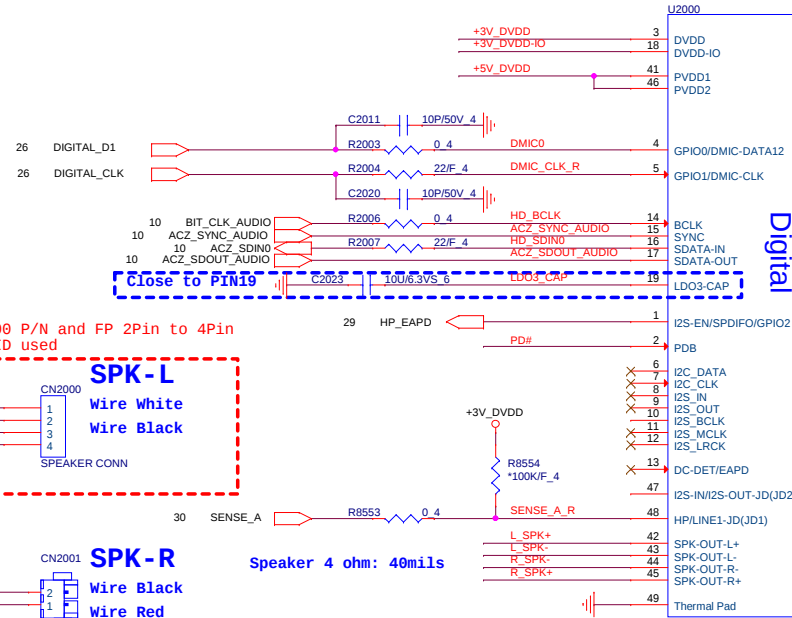
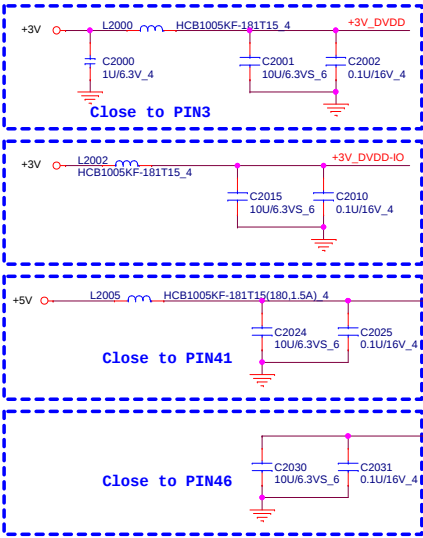
1124 SWAP for Layout



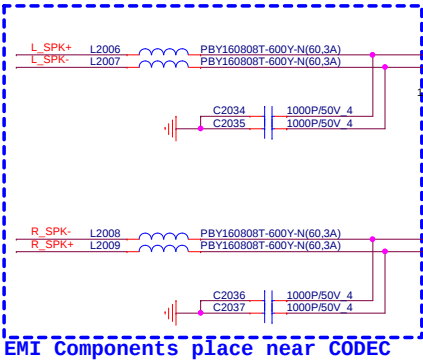
## Optional



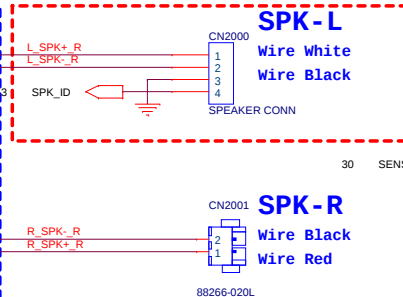
+5V 26,27,29,31,32,38,46,49  
+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,29,30,32,33,34,35,36,37,38,43,46,49  
+1.8V 31,47



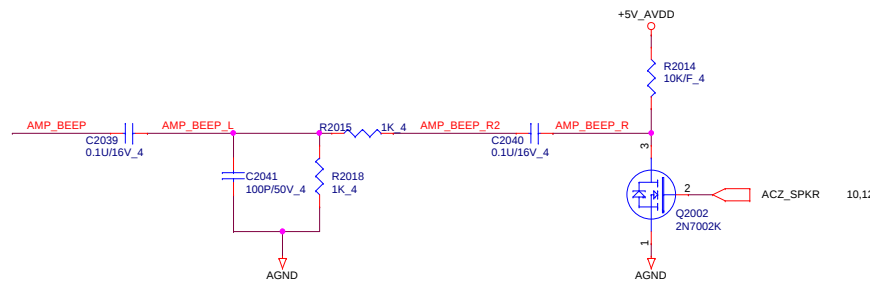
Speaker 4 ohm: 40mils



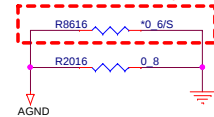
1123 Change CN2000 P/N and FP 2Pin to 4Pin for SPK Vendor ID used

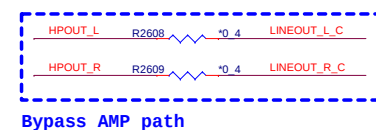
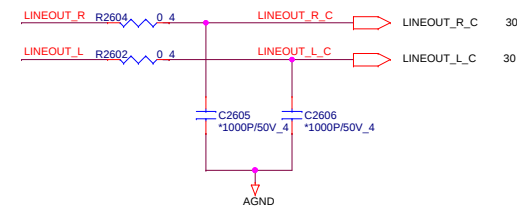


Speaker 4 ohm: 40mils

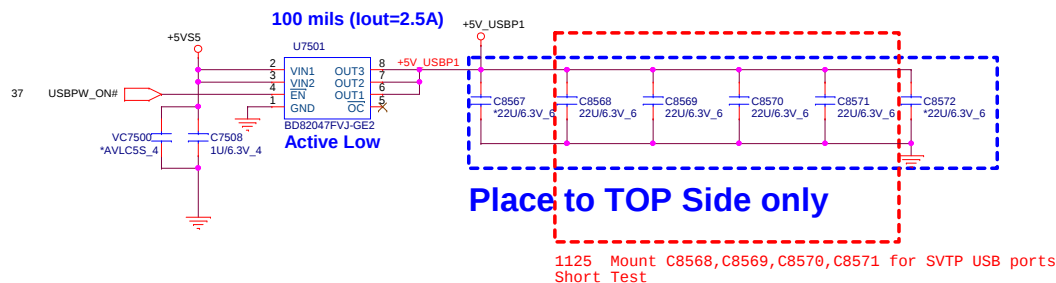


place to near or under codec  
1125 Add R8616 0603size short pad under codec for EMI request

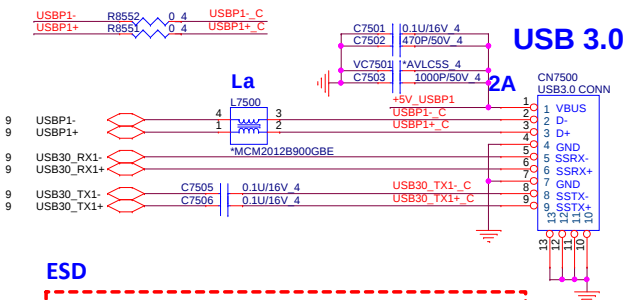




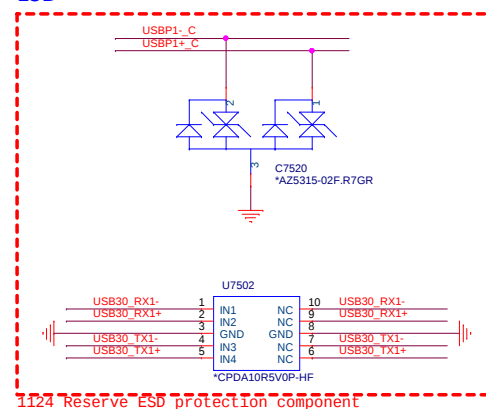
|        |                                                                             |
|--------|-----------------------------------------------------------------------------|
| +5VSS  | 10,26,28,41,42,43,44,45,46,47,48,49,50,51                                   |
| +3VPCU | 5,10,33,37,38,40,41                                                         |
| +3V    | 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,32,33,34,35,36,37,38,43,46,49 |
| +1.8V  | 28,31,47                                                                    |



## USB 2.0/3.0 Combo



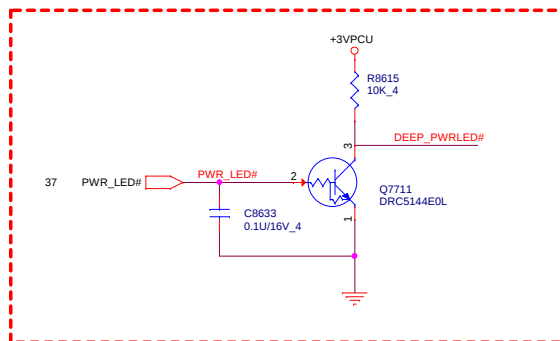
## ESD



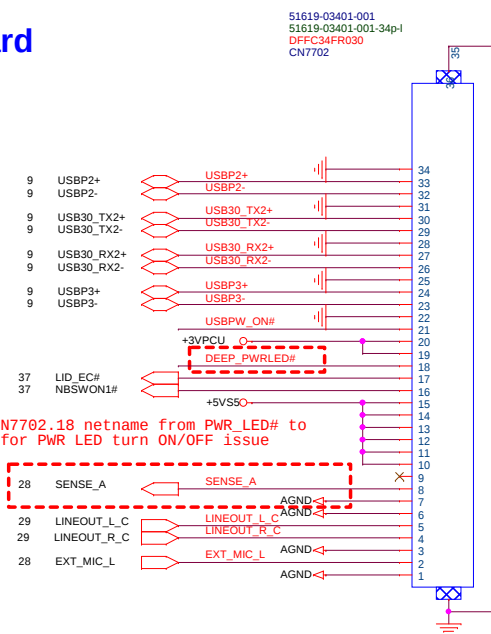
1124 Reserve ESD protection component

## Daughter Board

1123 Add PWR LED MOS Circuit

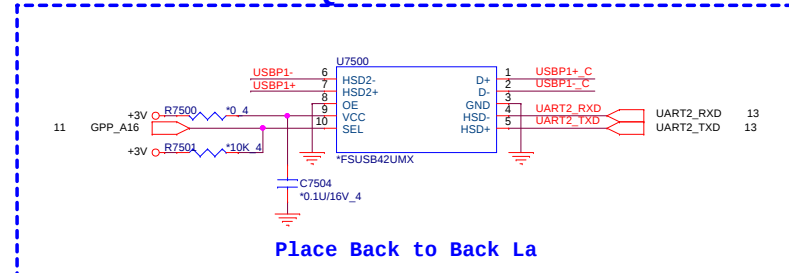


1123 Change CN7702.18 netname from PWR\_LED# to DEEP\_PWRLD# for PWR LED turn ON/OFF issue



1124 Pin7 and Pin8 need SWAP due to SENSE\_A is refer to DGND so

## UART for Win7 WHQL DEBUG

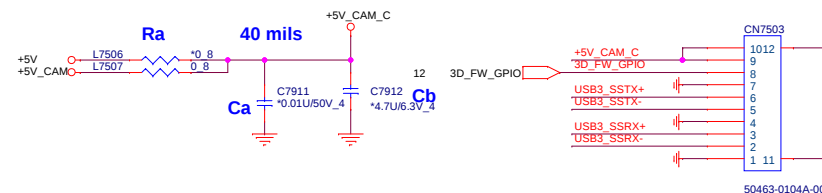


Place Back to Back La

|        |                                                                                |
|--------|--------------------------------------------------------------------------------|
| +5V    | 26,27,28,29,32,38,46,49                                                        |
| +3VPCU | 5,10,30,33,37,38,40,41                                                         |
| +3V    | 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49 |
| +1.8V  | 28,47                                                                          |

BOM: 3D CAM Stuff (except Ra, Ca, Cb)  
BOM: HD CAM Un- Stuff

### 3D Camera Conn.



BOM: 3D CAM Stuff (except Rb, Rc)

BOM: HD CAM Un-Stuff

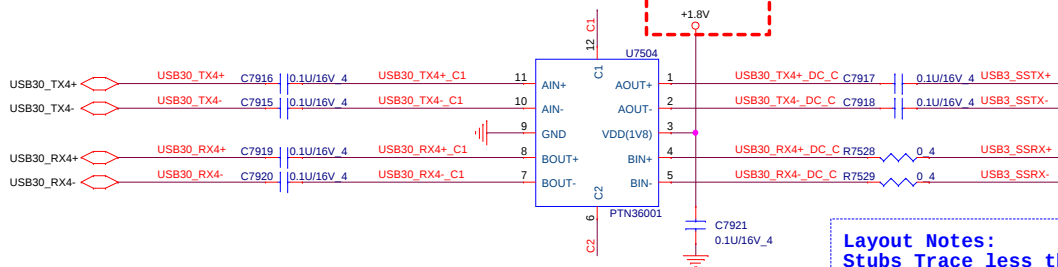
### USB3.0

#### USB3.0 Re-driver IC

HOST

USB3.0 re-driver IC

DEVICE



Layout Notes:  
Stubs Trace less than 150mil

1123 Change UB3 re driver power rail  
from +1.8V\_DEEP\_SUS to +1.8V

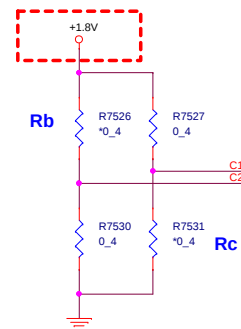


Table 4. C1 pin controls long/medium/short traces

| State  | Channel type | Pin C1 state | Channel B | Channel A |
|--------|--------------|--------------|-----------|-----------|
| H      | Long         | H            | EQ[1]     | DE[2]     |
| high-Z | Medium       | high-Z       | 6 dB      | -5.3 dB   |
| L      | Short        | L            | 3 dB      | 0 dB      |

Table 5. C2 pin controls long/medium/short traces

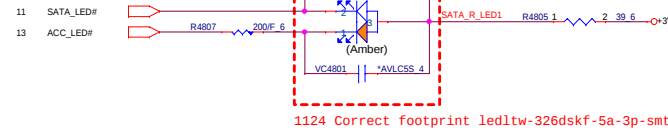
| State  | Channel type | Pin C2 state | Channel A | Channel B |
|--------|--------------|--------------|-----------|-----------|
| H      | Long         | H            | 9 dB      | -5.3 dB   |
| high-Z | Medium       | high-Z       | 6 dB      | -3.1 dB   |
| L      | Short        | L            | 3 dB      | 0 dB      |



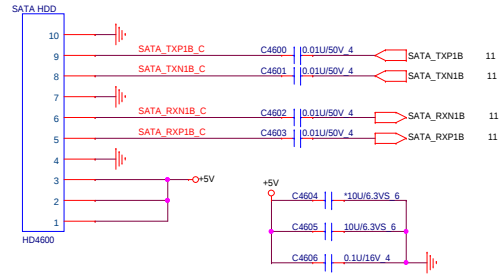
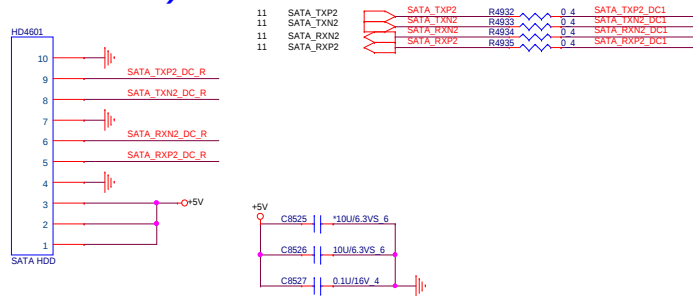
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

|                                 |                                                |           |
|---------------------------------|------------------------------------------------|-----------|
| Size<br>Custom                  | Document Number<br><b>31 – 3D CAM/REDRIVER</b> | Rev<br>1A |
| Date: Monday, December 28, 2015 | Sheet 31 of 51                                 |           |

## SATA LED



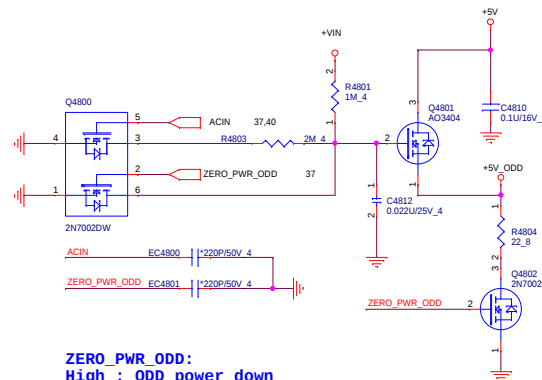
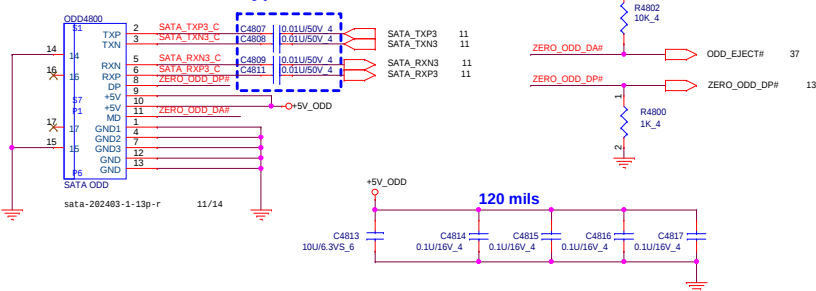
## HDD

HDD  
(Close to ODD)

|               |       |             |                |
|---------------|-------|-------------|----------------|
| SATA_TXP2_DC1 | C4924 | 0.01U/50V 4 | SATA_TXP2_DC_R |
| SATA_TXN2_DC1 | C4925 | 0.01U/50V 4 | SATA_TXN2_DC_R |
| SATA_RXN2_DC1 | C4926 | 0.01U/50V 4 | SATA_RXN2_DC_R |
| SATA_RXP2_DC1 | C4927 | 0.01U/50V 4 | SATA_RXP2_DC_R |

## SATA ODD

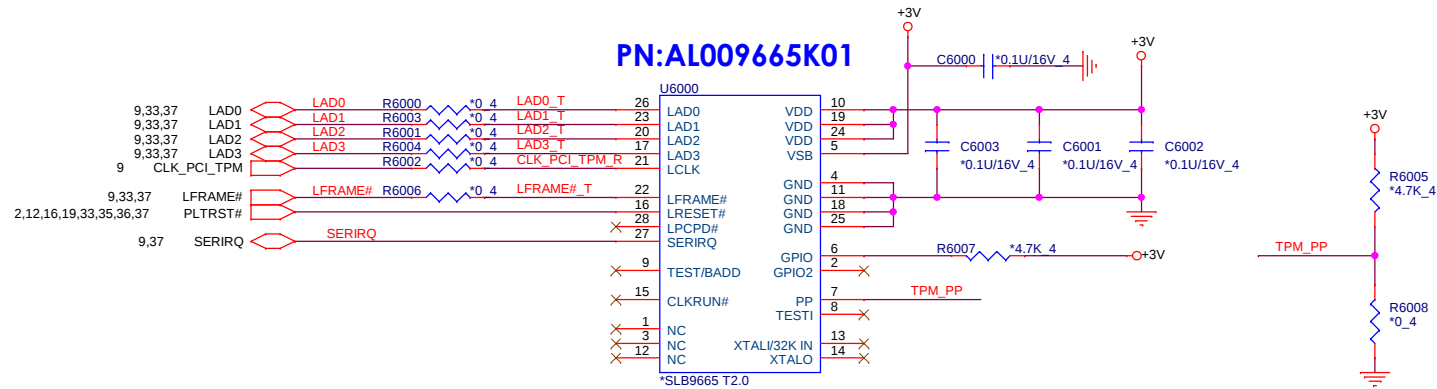
## Bypass CAP close CON



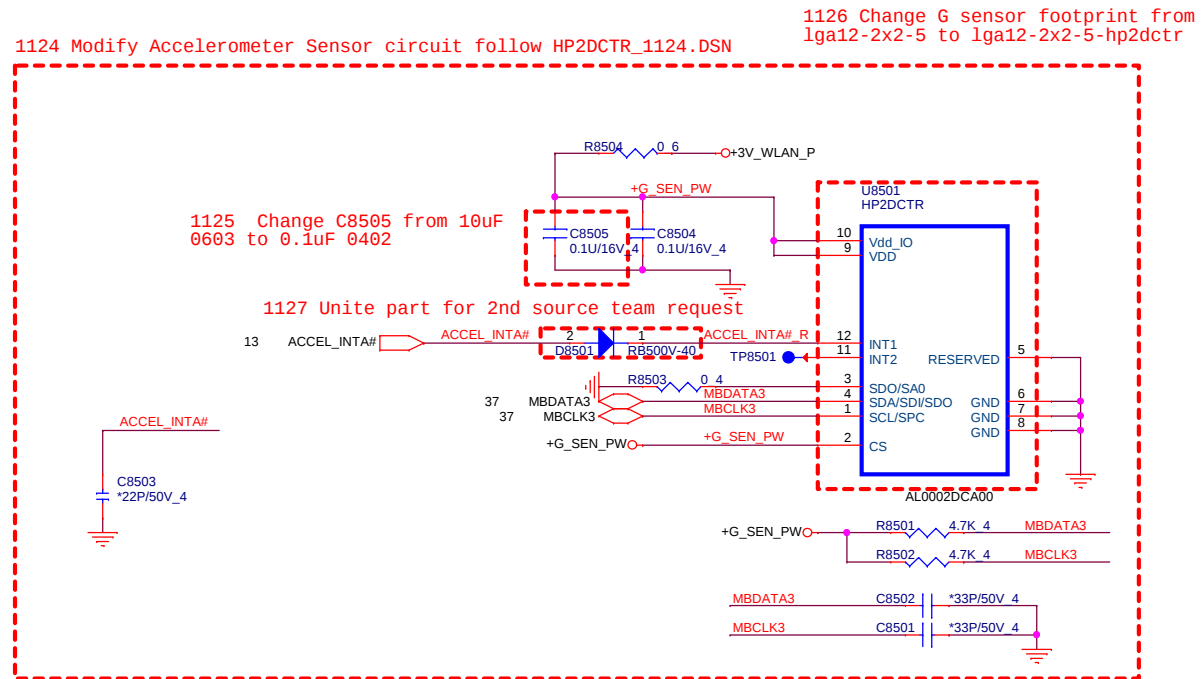
ZERO\_PWR\_ODD:  
High : ODD power down  
Low : ODD power on



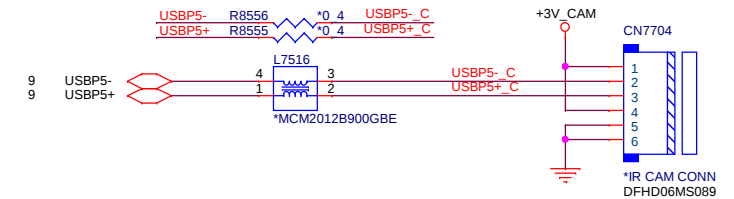
## TPM (2.0)



## Accelerometer Sensor



## IR CAM



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

| <Title> |                                    |                |
|---------|------------------------------------|----------------|
| Size B  | Document Number 34 -- TPM/G-Sensor | Rev 1A         |
| Date:   | Monday, December 28, 2015          | Sheet 34 of 51 |

+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,36,37,38,43,46,49  
+3VLANVCC 46

## LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH

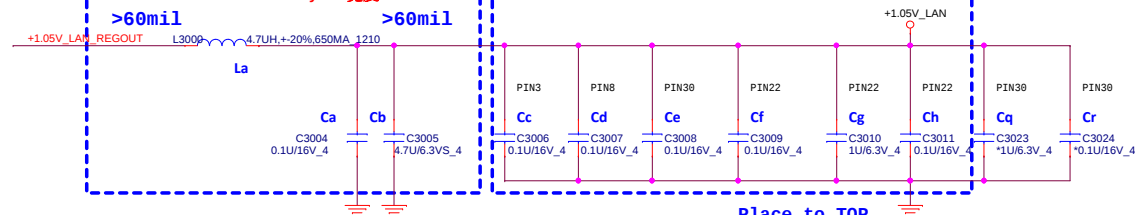
Stuff La, Ca, Cb

\* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S)  
close to each VDD10 pin-- 3, 22, 8, 30

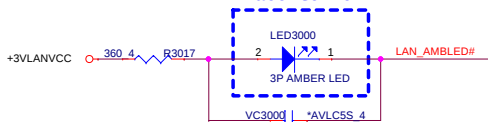
\* Place Cg,Ch for RTL8111H(S) & RTL8107E(S)  
close to each VDD10 pin-- 22(reserved)

Power trace Layout 宽度 > 60mil

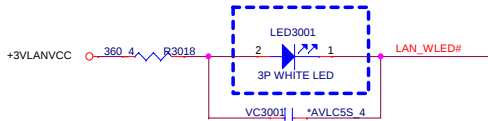
>60mil >60mil



Place to TOP

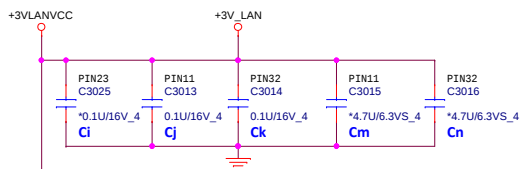


Place to BOT



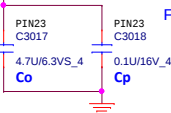
\* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

\* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

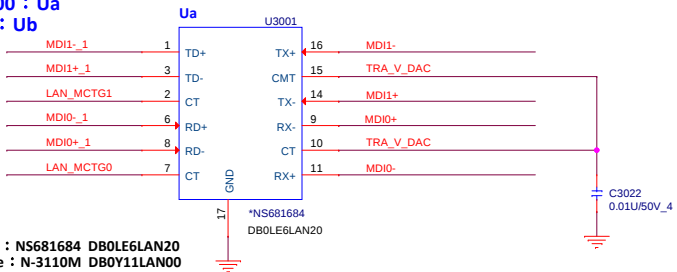


For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp



For 10/100 : Ua  
For Giga : Ub

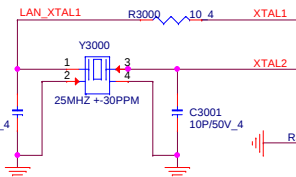
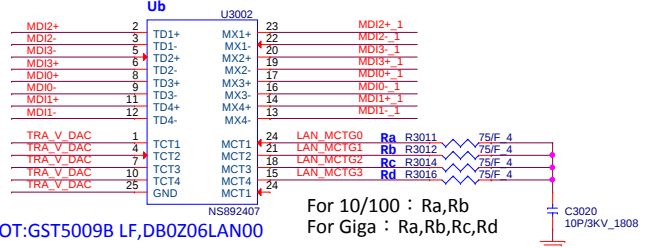


1st source : NS681684 DB0LE6LAN20  
2nd source : N-3110M DB0Y11LAN00

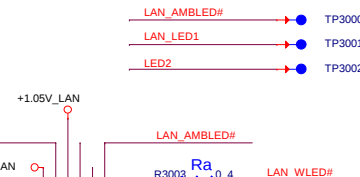
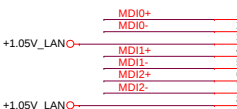
For GIGA BOT:GST5009B LF,DB0Z06LAN00

FCE : NS892407 , DB0LL1LAN00

For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd



Please add 9 GND VIAS  
connection with thermal PAD



For GbE

\* Place Ra

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

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\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

\* Place Rb

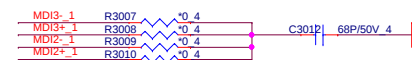
\* Place Rb

\* Place Rb

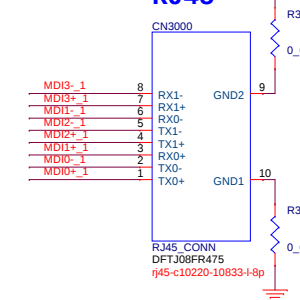
\* Place Rb

\* Place Rb

For 10/100 stuff only



RJ45

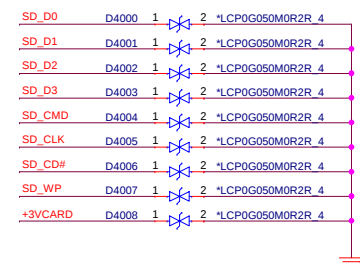


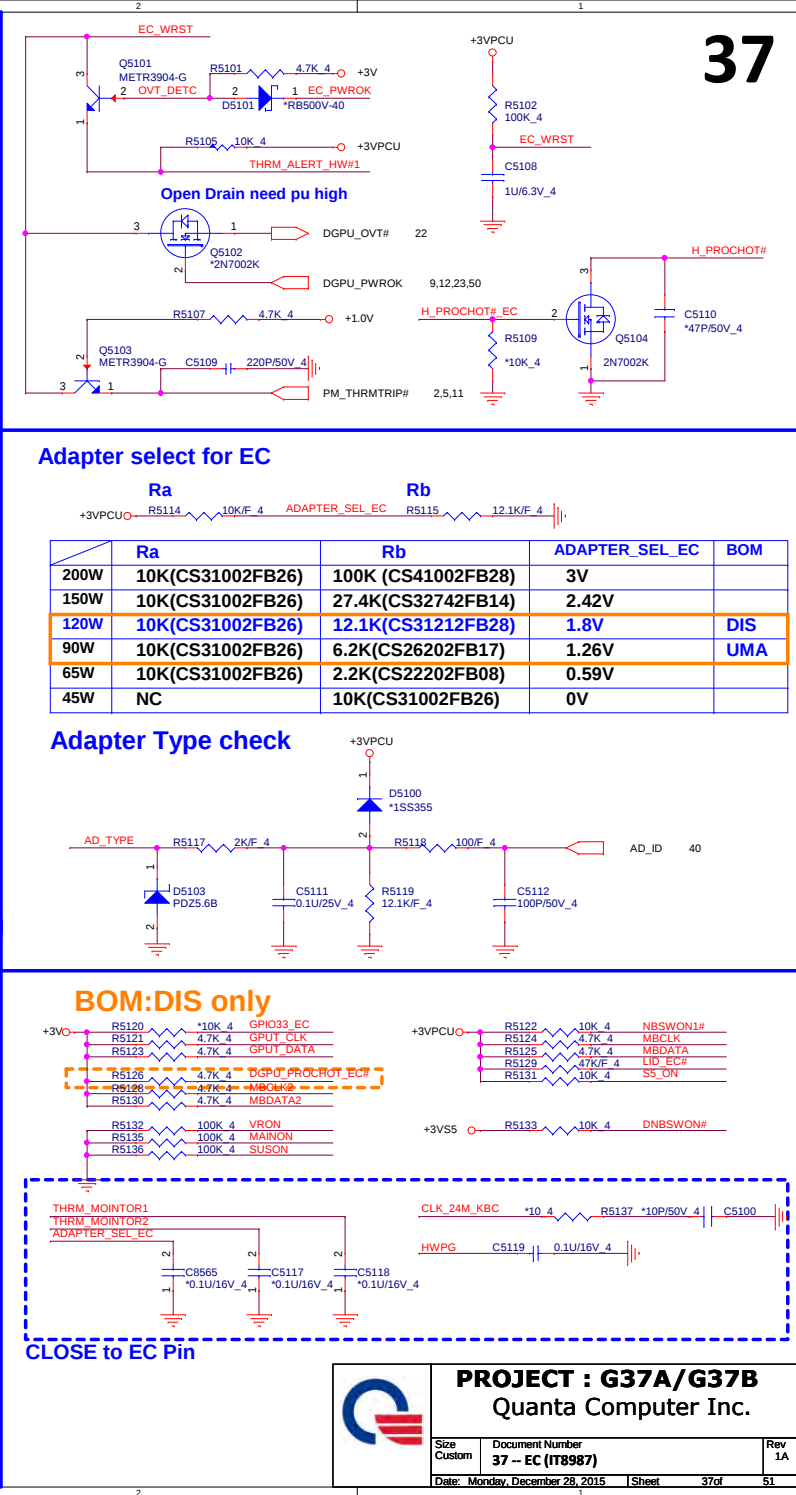
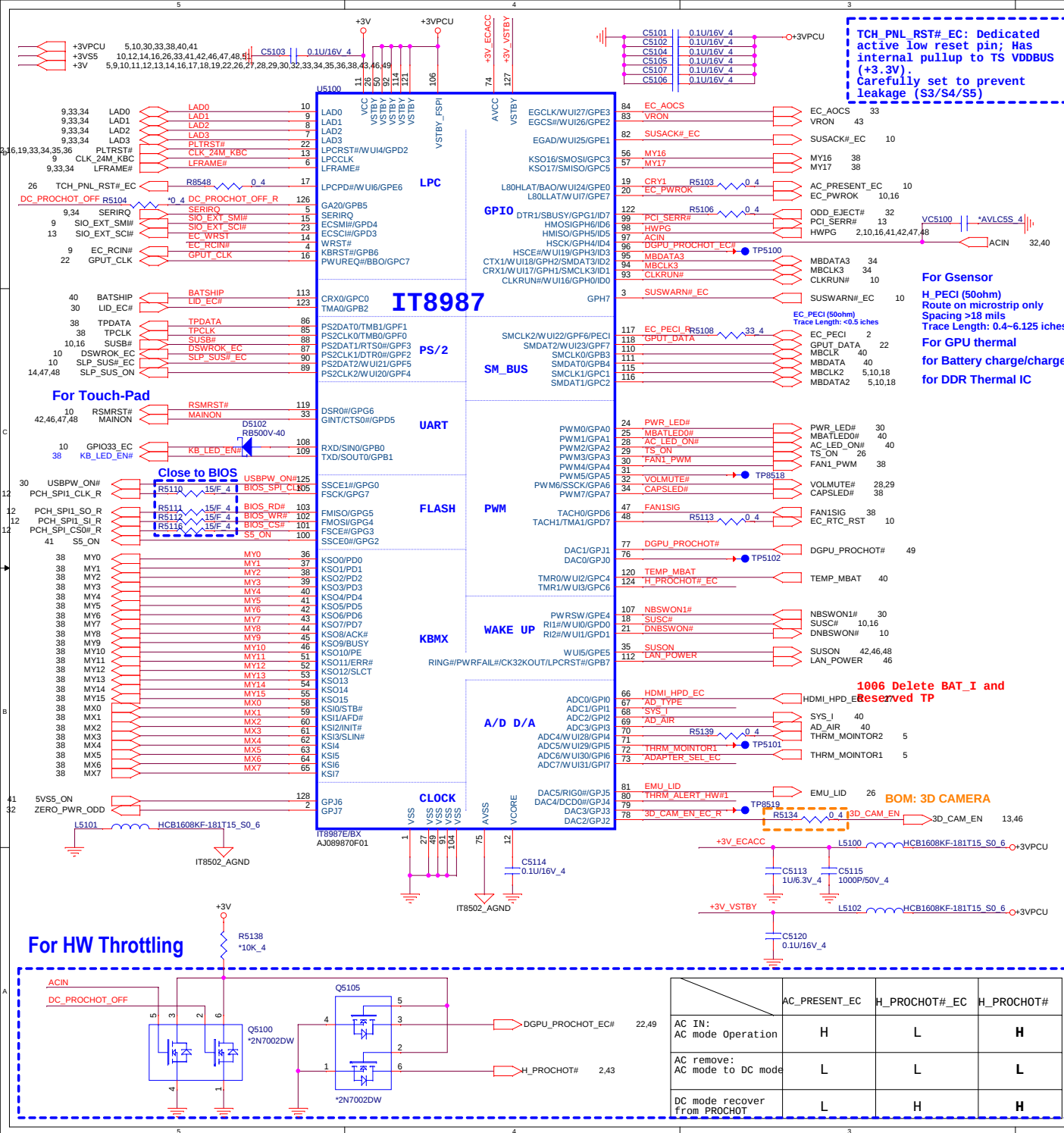
1125 Change CN3000 PN T from DFTJ08FR335 to DFTJ08FR475



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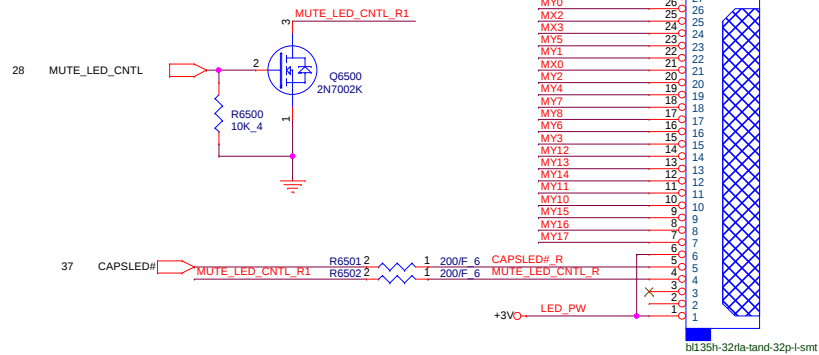
| Size                            | Document Number             | Rev |
|---------------------------------|-----------------------------|-----|
| Custom                          | 35 - LAN RTL8107ESH-CG/RJ45 | 1A  |
| Date: Monday, December 28, 2015 | Sheet 35 of 51              |     |



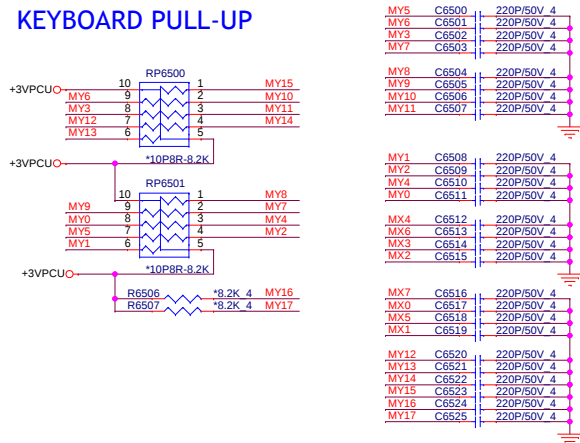


+VIN 26,32,39,40,41,42,43,44,45,47,48,49,50  
 +5V 26,27,28,29,31,32,46,49  
 +3VPCU 5,10,30,33,37,40,41  
 +3VSS 10,12,14,16,26,33,37,41,42,46,47,48,51  
 +3VSUS 46  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,43,46,49

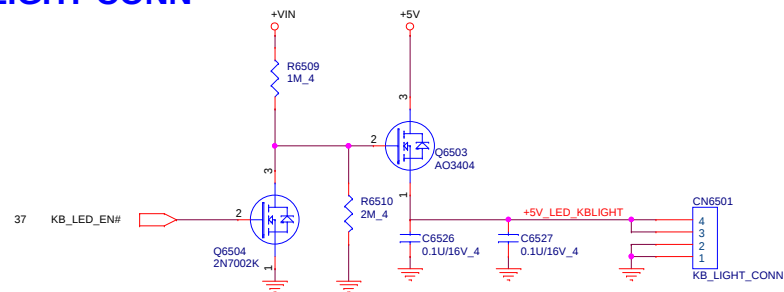
## KEYBOARD Con.



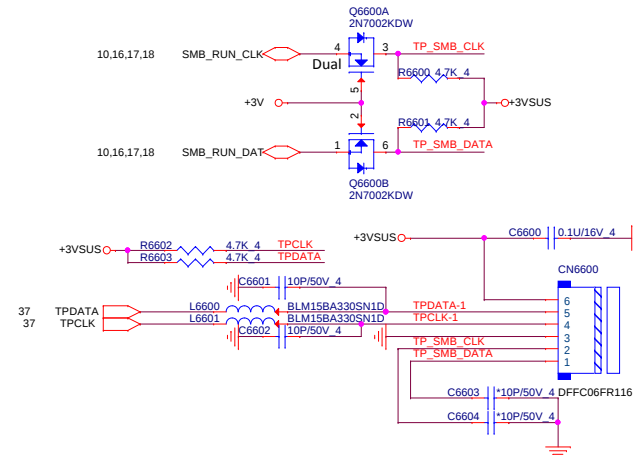
## KEYBOARD PULL-UP



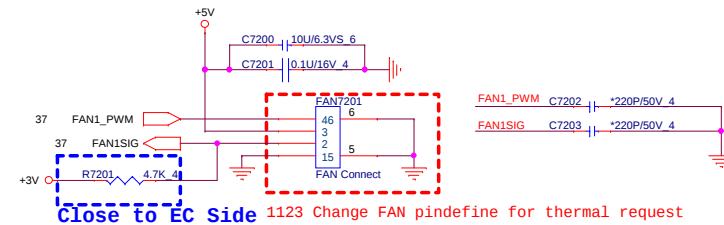
## KB LIGHT CONN



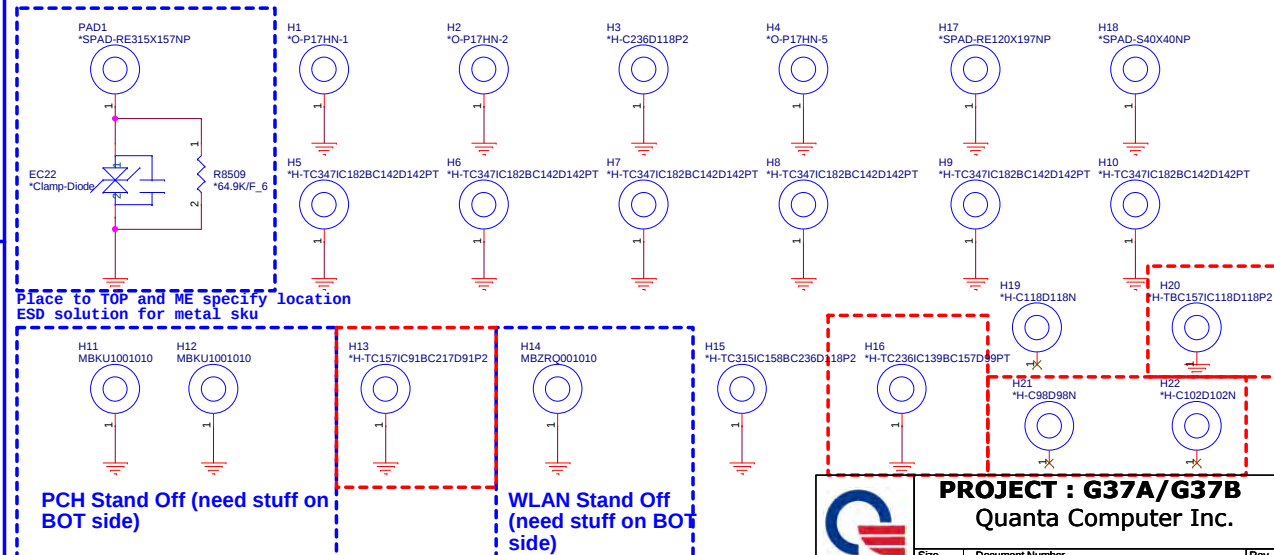
## Touch Pad Connector

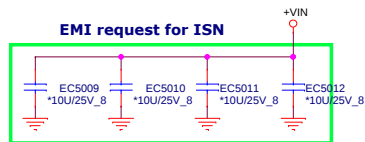
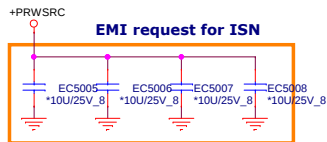


## FAN



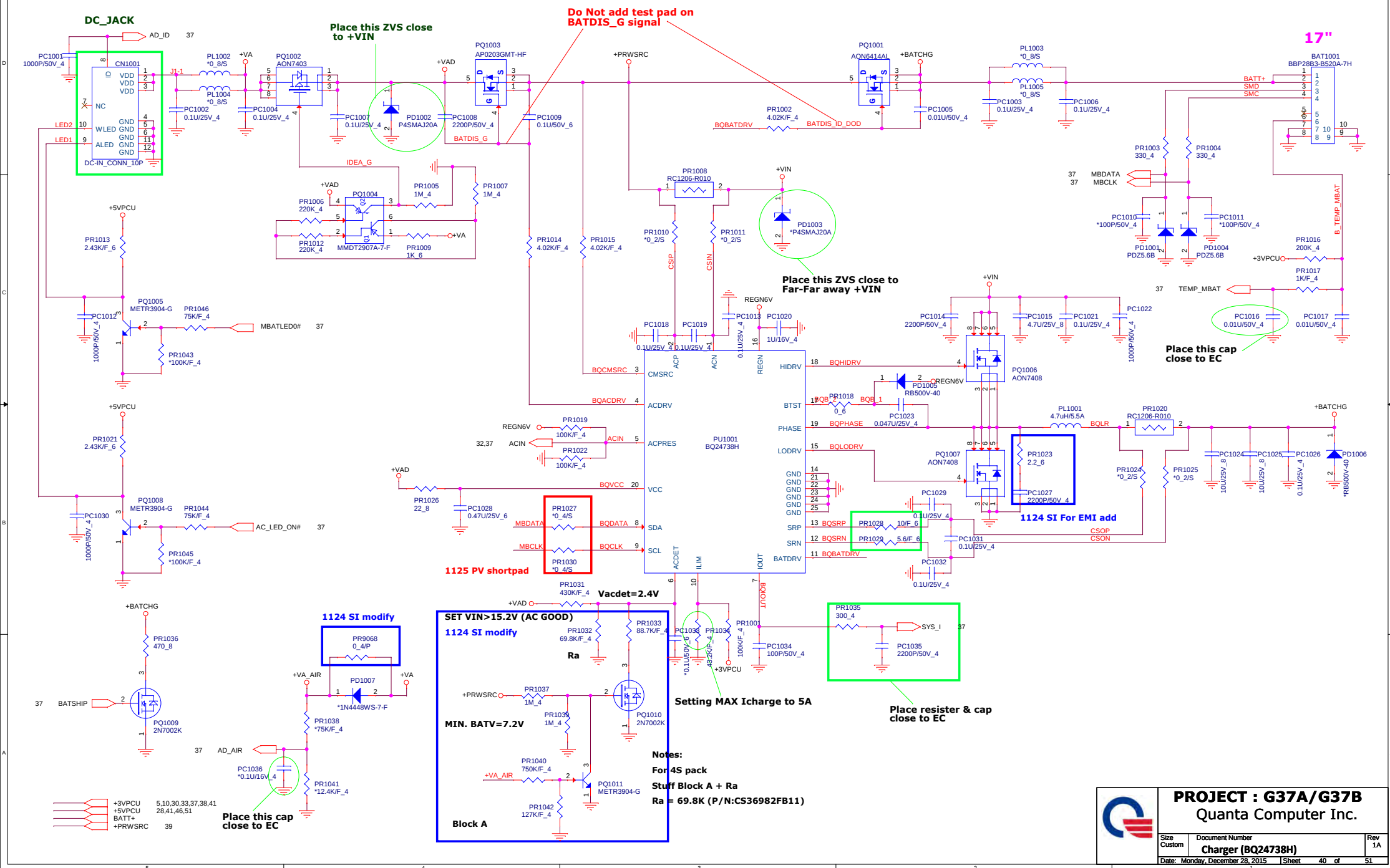
## HOLE

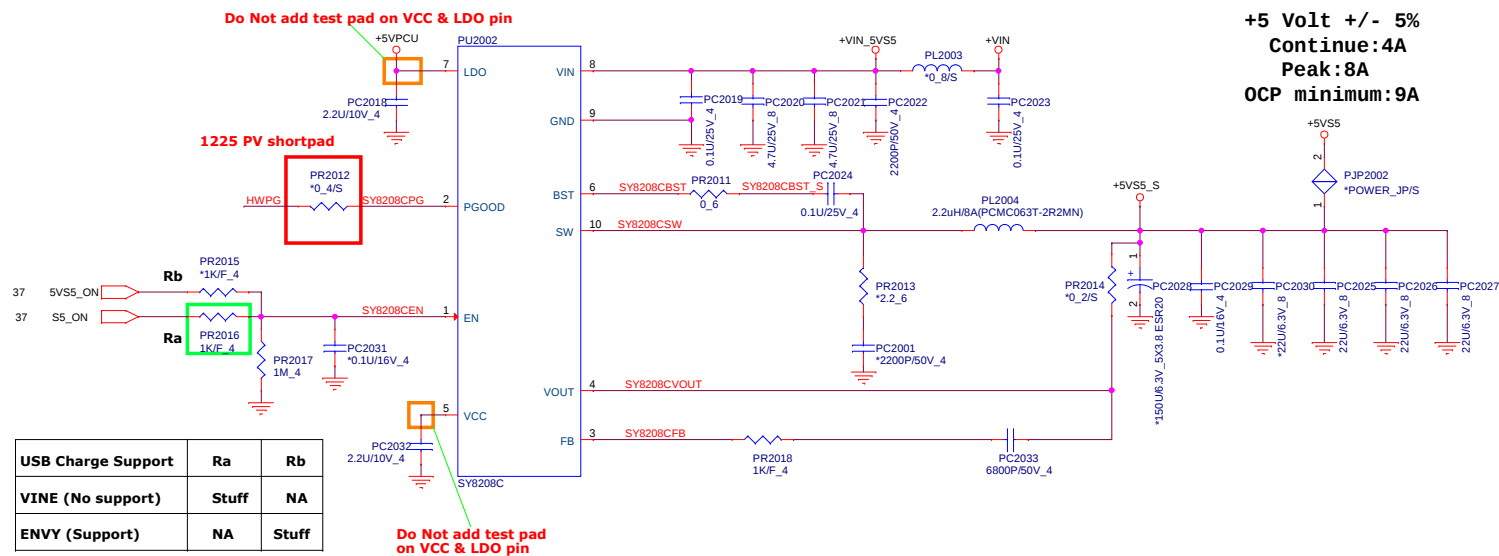
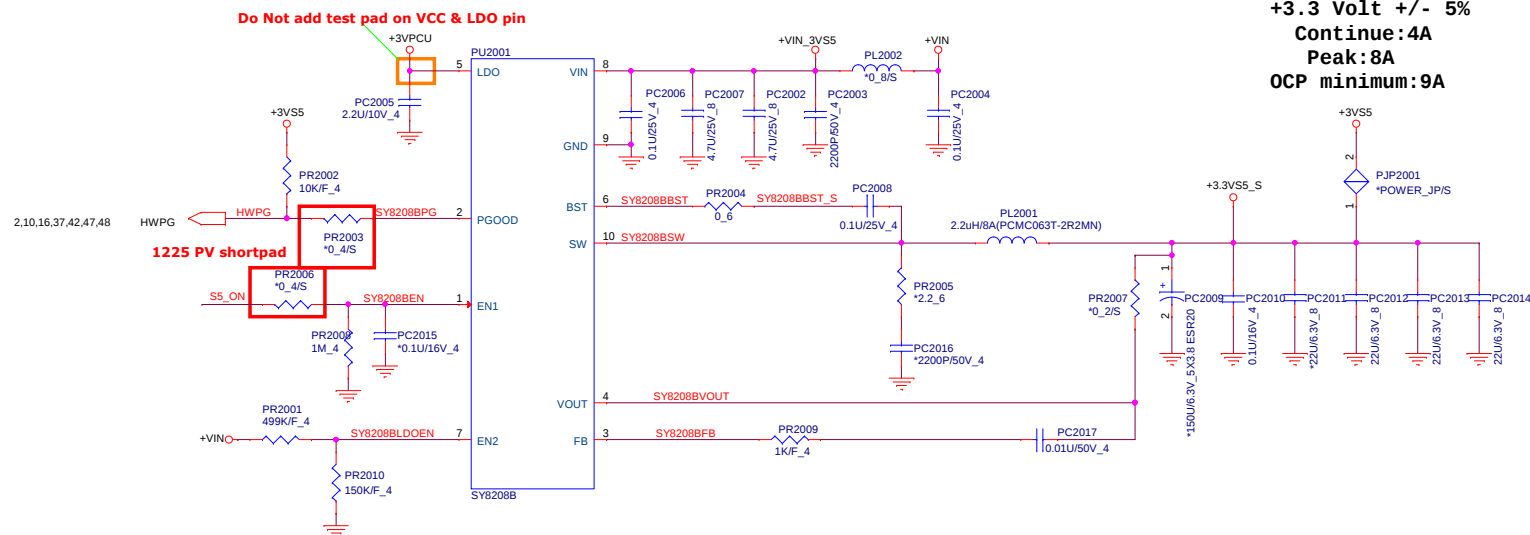




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|                                 |                                       |                |
|---------------------------------|---------------------------------------|----------------|
| Size<br>Custom                  | Document Number<br><b>RF Solution</b> | Rev<br>1A      |
| Date: Monday, December 28, 2015 |                                       | Sheet 39 of 51 |



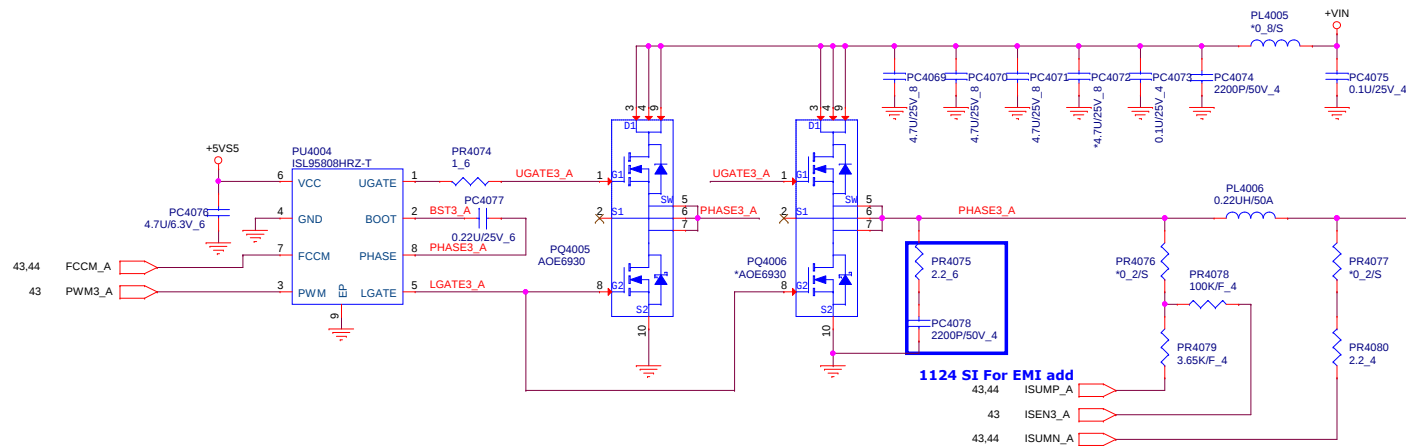
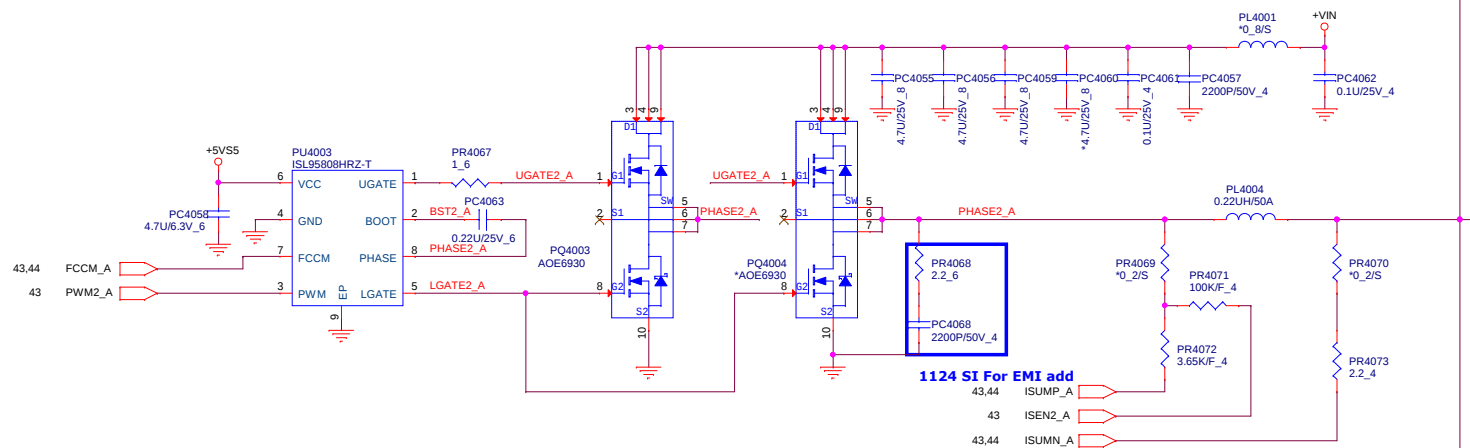
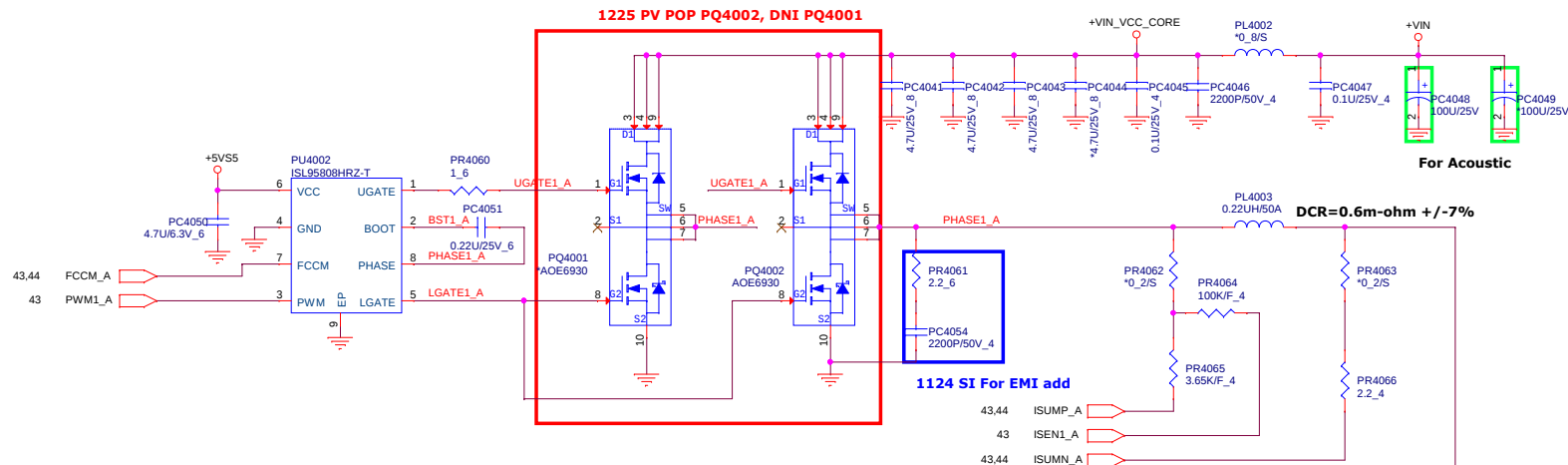


| USB Charge Support | Ra    | Rb    |
|--------------------|-------|-------|
| VINE (No support)  | Stuff | NA    |
| ENVY (Support)     | NA    | Stuff |

|        |                                           |
|--------|-------------------------------------------|
| +VIN   | 26,32,38,39,40,42,43,44,45,47,48,49,50    |
| +3VS5  | 10,12,14,16,26,33,37,42,46,47,48,51       |
| +5VS5  | 10,26,28,30,42,43,44,45,46,47,48,49,50,51 |
| +3VPCU | 5,10,30,33,37,38,40                       |
| +5VPCU | 28,40,46,51                               |

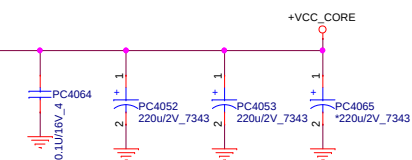


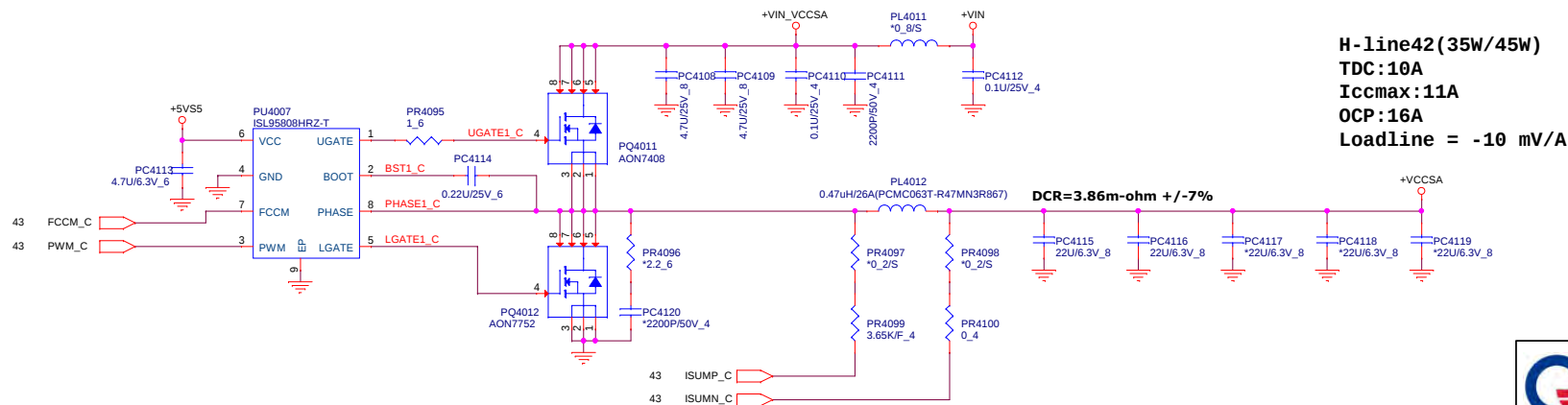
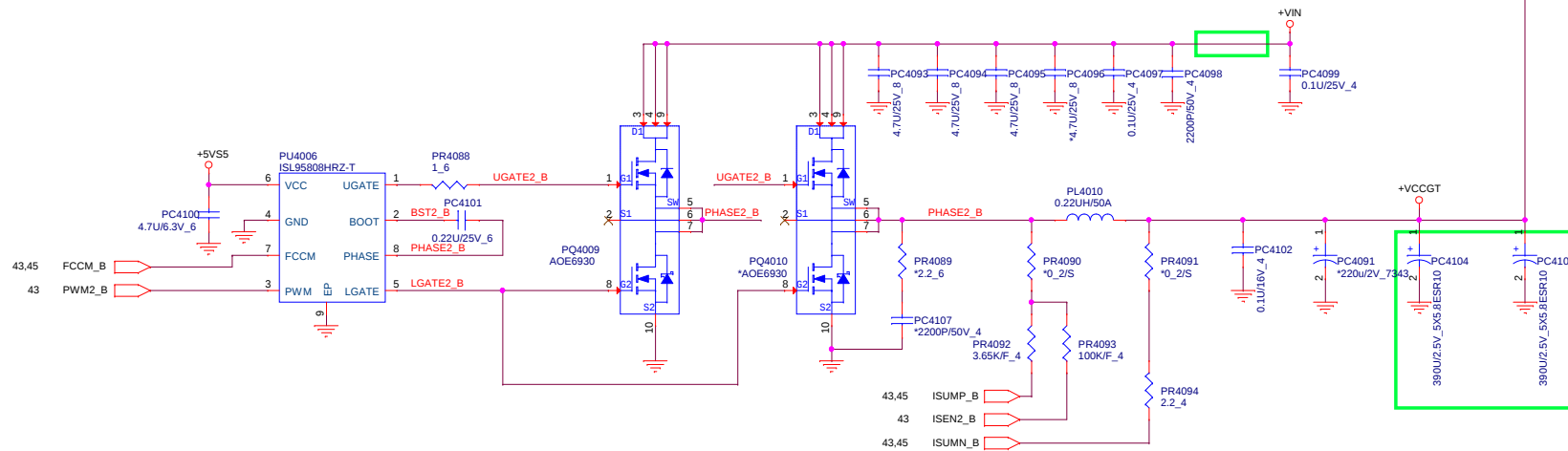
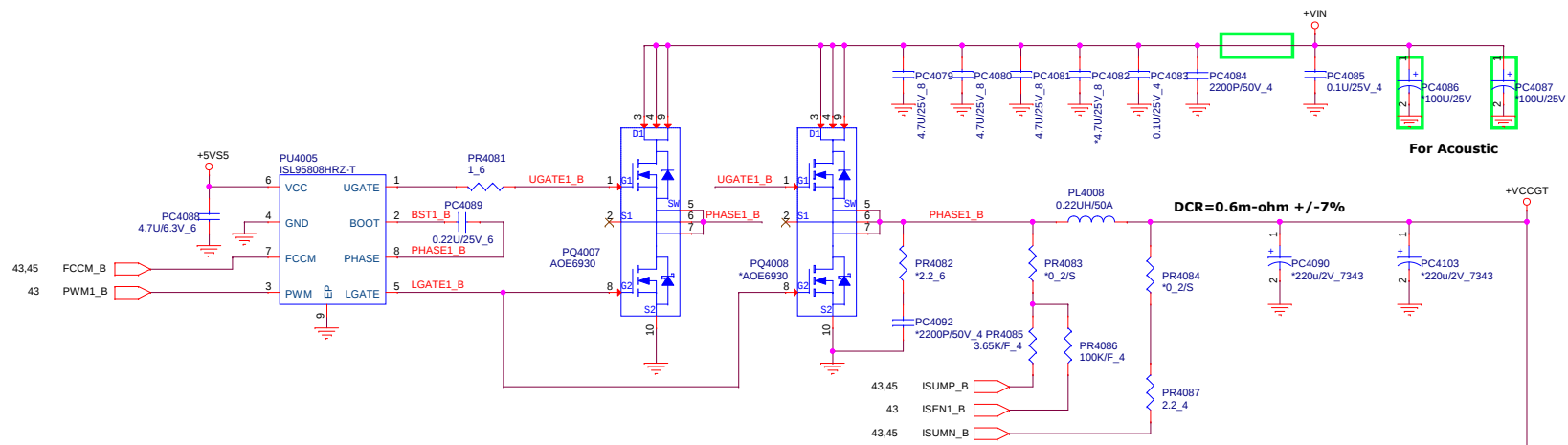




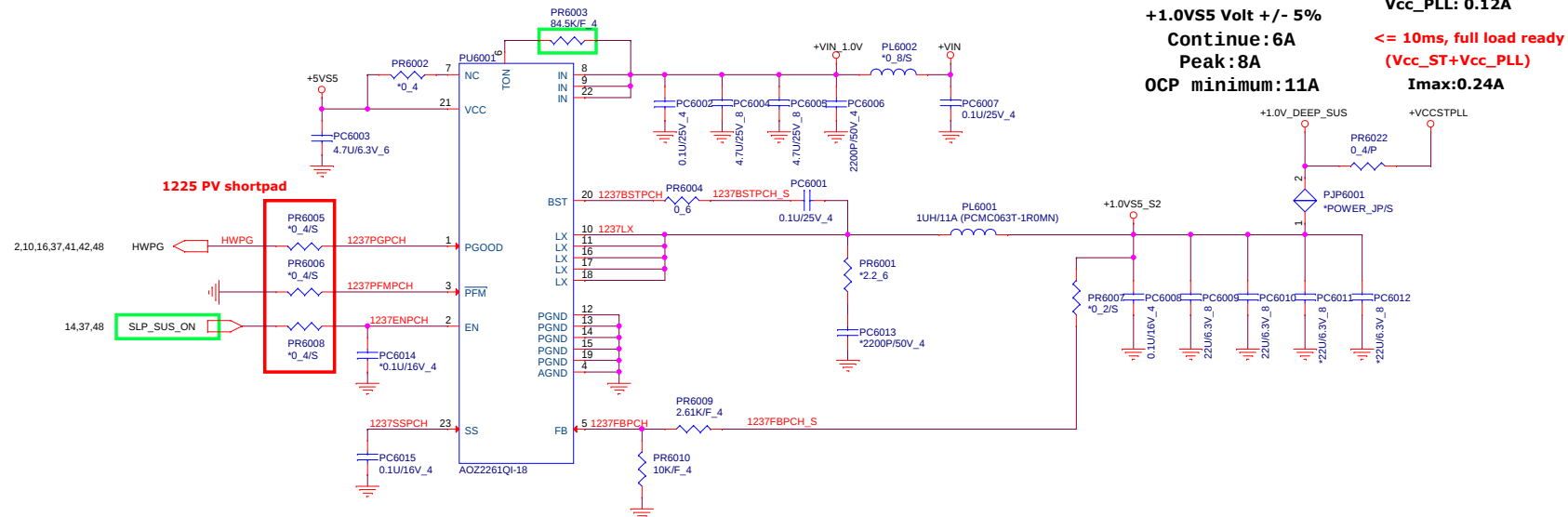
H-line42(35W)  
TDC:49A  
Iccmax:60A  
OCP:86A  
Loadline = -1

H-line42(45W)  
TDC:56A  
Iccmax:68A  
OCP:86A  
Loadline = -1.8 mV/A

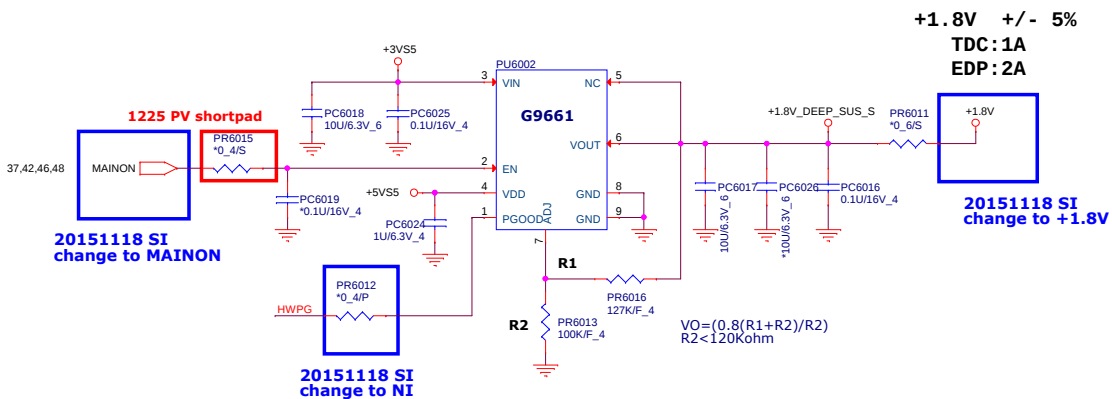








20151118 SI del

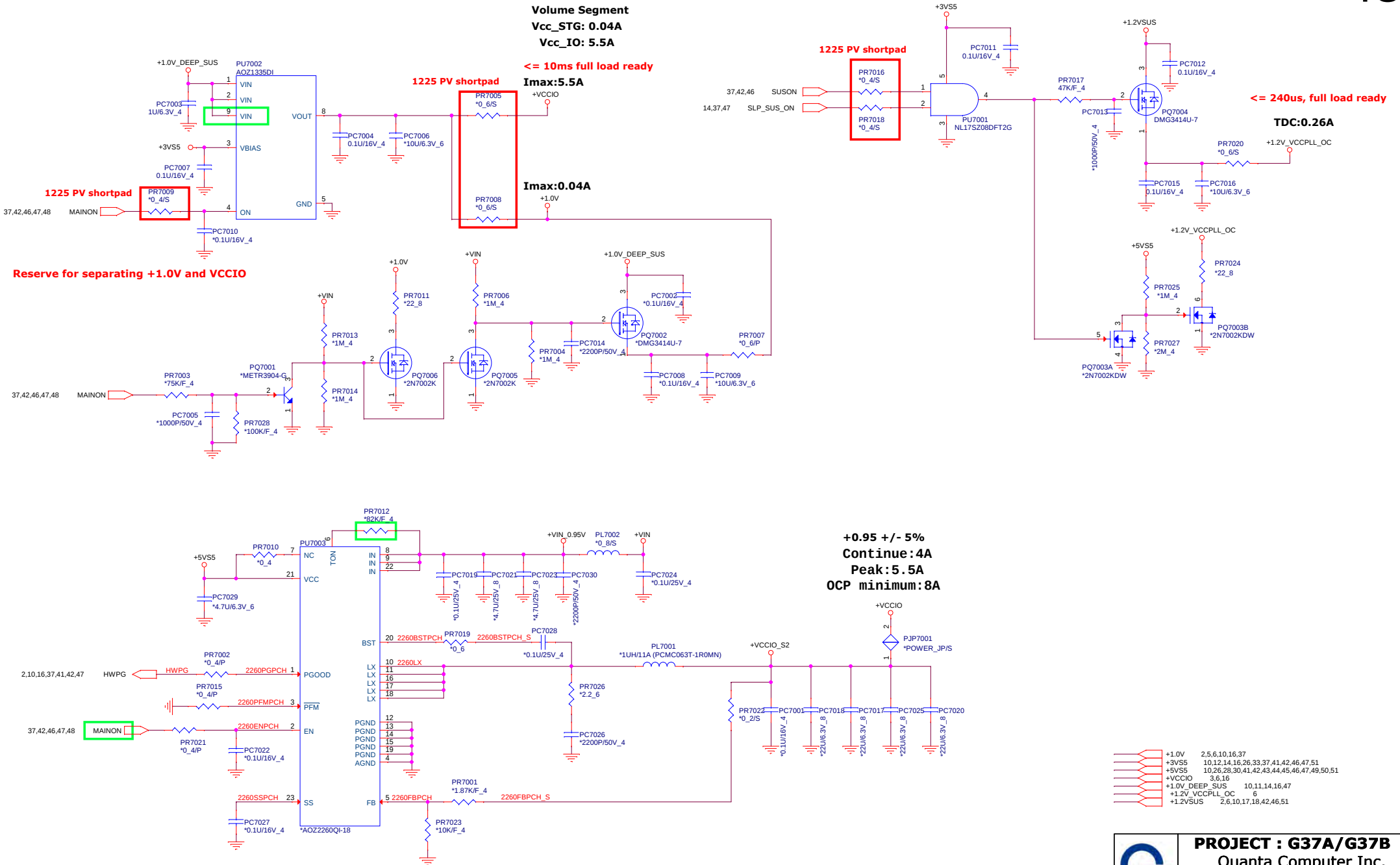


|                |                                           |
|----------------|-------------------------------------------|
| +VIN           | 26,32,38,39,40,41,42,43,44,45,48,49,50    |
| +3VS5          | 10,12,14,16,26,33,37,41,42,46,48,51       |
| +5VS5          | 10,26,28,30,41,42,43,44,45,46,48,49,50,51 |
| +1.0V_DEEP_SUS | 10,11,14,16,48                            |
| +1.8V          | 28,31                                     |
| +VCCSTPLL      | 2,6,43                                    |



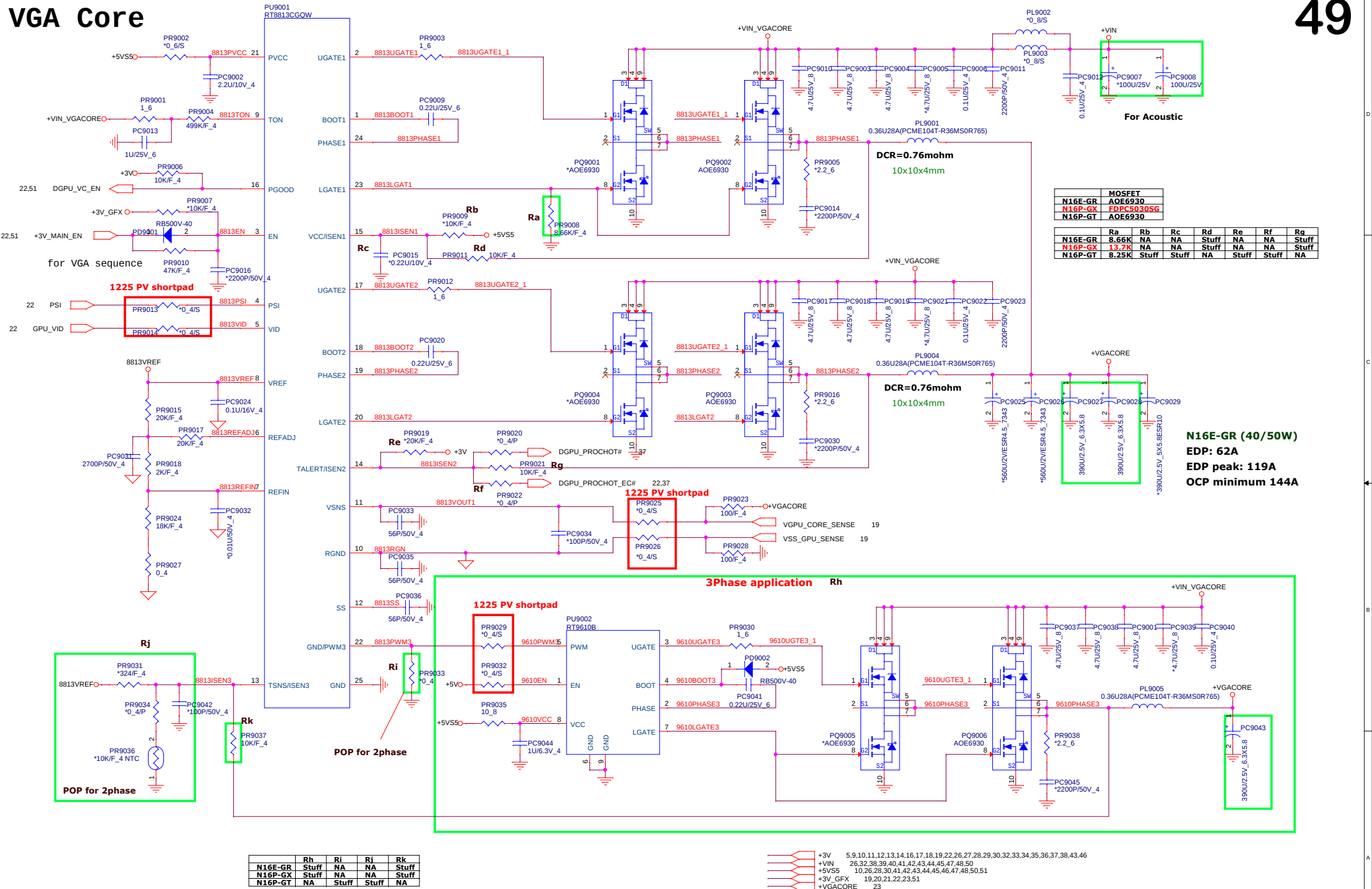
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

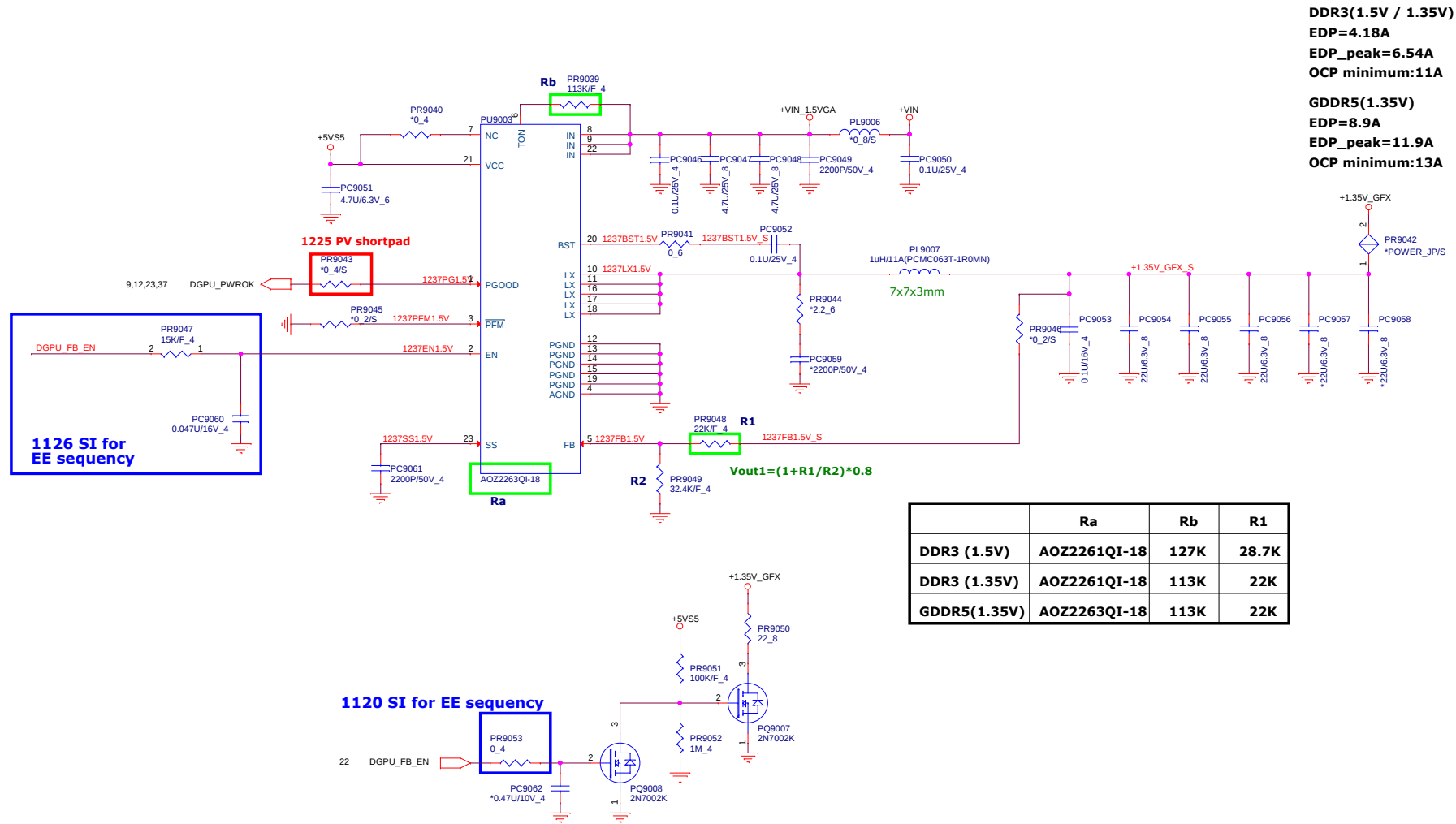
|                |                                         |                  |
|----------------|-----------------------------------------|------------------|
| Size<br>Custom | Document Number<br><b>+1.0_DEEP_SUS</b> | Rev<br>1A        |
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# VGA Core

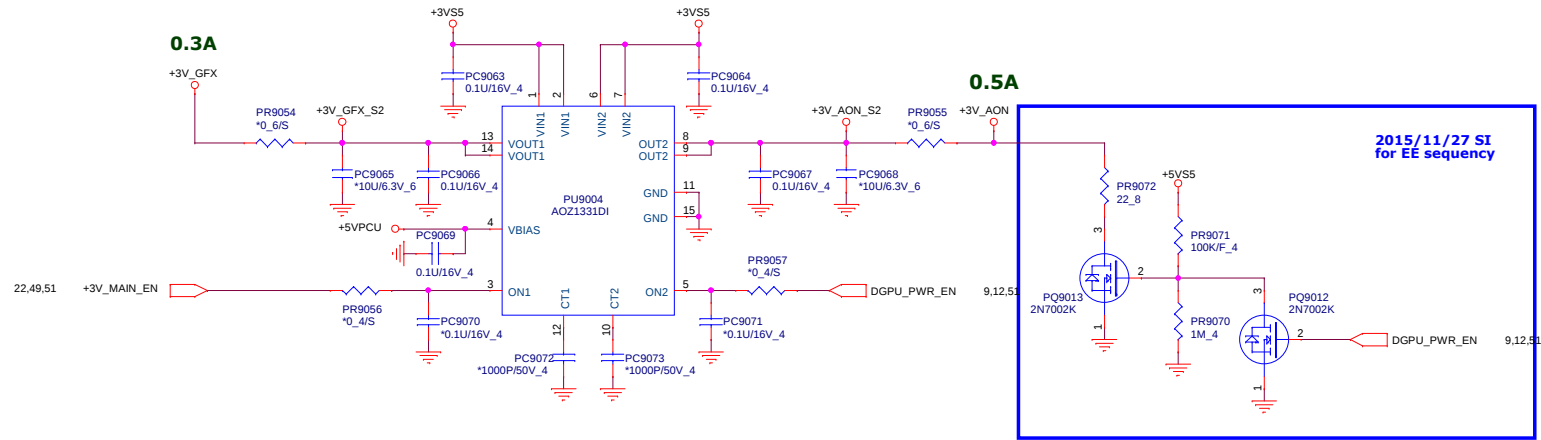
49



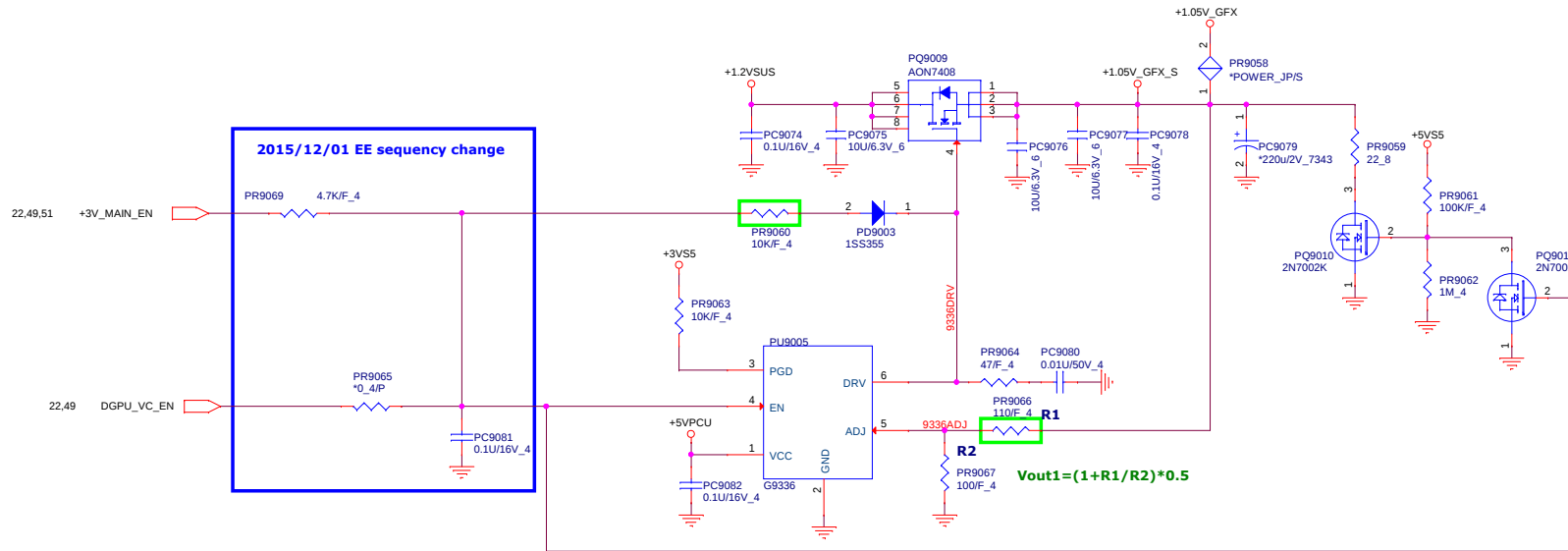


|              | Ra           | Rb   | R1    |
|--------------|--------------|------|-------|
| DDR3 (1.5V)  | AOZ2261QI-18 | 127K | 28.7K |
| DDR3 (1.35V) | AOZ2261QI-18 | 113K | 22K   |
| GDDR5(1.35V) | AOZ2263QI-18 | 113K | 22K   |

+VIN 26,32,38,39,40,41,42,43,44,45,47,48,49  
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,49,51  
+1.35V\_GFX 20,23,24,25



**+1.05V\_GFX Volt +/- 5%**  
**EDP=2.38A**  
**EDP\_peak = 2.45A**



|            |                                           |
|------------|-------------------------------------------|
| +VIN       | 26,32,38,39,40,41,42,43,44,45,47,48,49,50 |
| +3VS5      | 10,12,14,16,26,33,37,41,42,46,47,48       |
| +5VS5      | 10,26,28,30,41,42,43,44,45,46,47,48,49,50 |
| +3V_GFX    | 19,20,21,22,23,49                         |
| +3V_AON    | 19,22,23,27                               |
| +1.2VSUS   | 2,6,10,17,18,42,46,48                     |
| +1.05V_GFX | 19,20,21,23                               |



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|                                |                                  |        |
|--------------------------------|----------------------------------|--------|
| Size Custom                    | Document Number                  | Rev 1A |
|                                | <b>+3V/+1.05V_GFX(AOZ1331DI)</b> |        |
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