

Compal Confidential

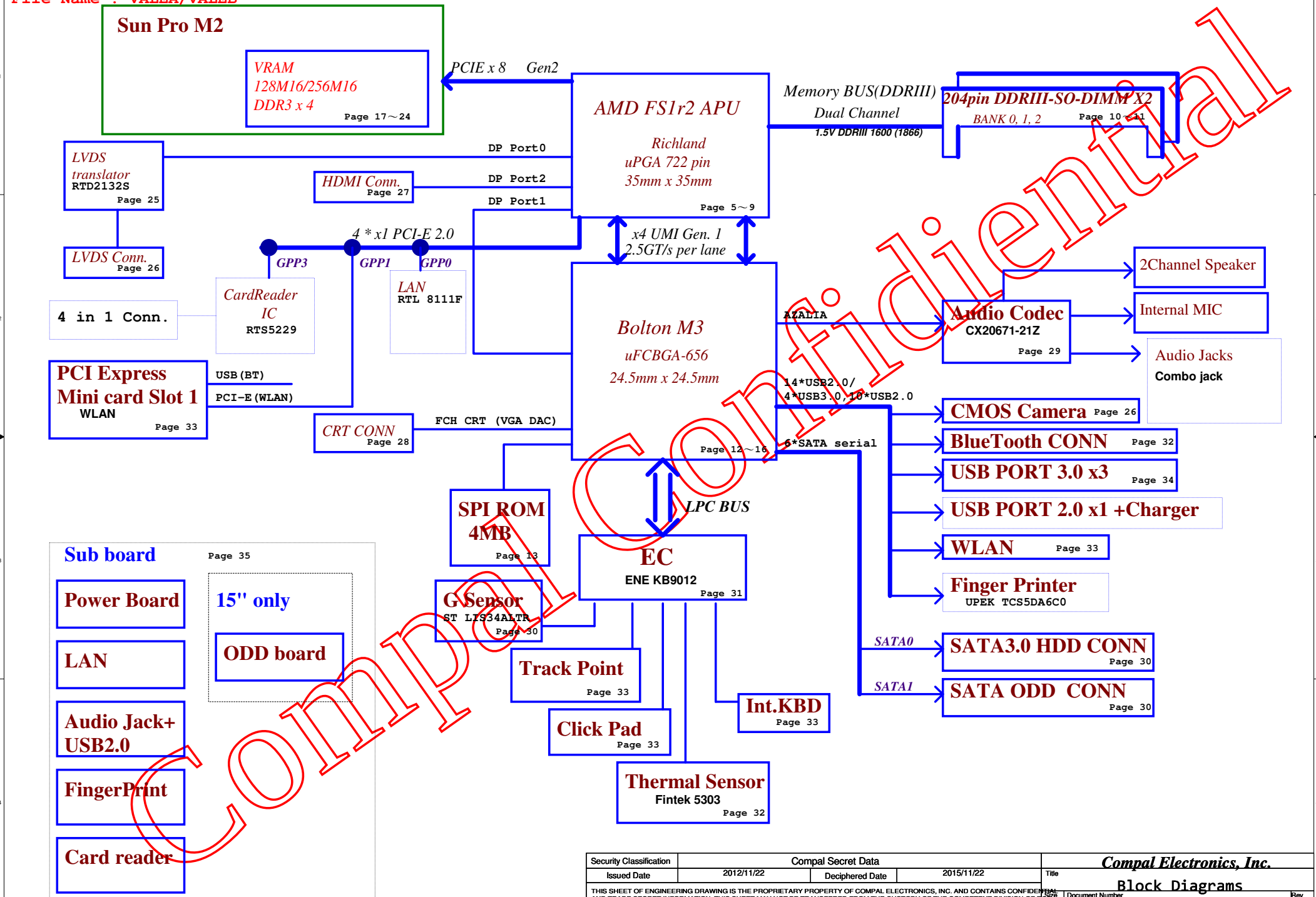
VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Cover Page
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				LA-8126P	1.0
				Date	Tuesday, March 12, 2013
				Sheet	1 of 51



Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Sun Pro M2	1000-0010b	82H
			LVDS translator		

FCH SMB0

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxless
CMOS@ : USB camera
CONN@ : ME components
X76@, H1G@, SIG@ : VRAM

BOM option and stencil

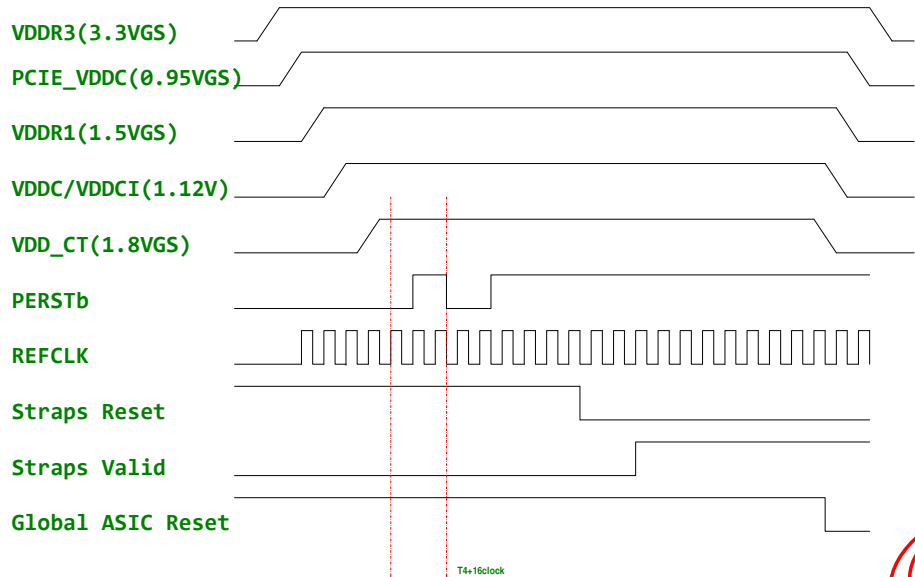
SDV:
CMOS@/DIS@ + X76@

PJ201, PJ401, PJ502, PJ503, PJ504, PJ601, PJ603, PJ604,
PJ701, PJ702, PJ703, PJ704, J1, J2301, J2401, J2402, J2403
PJ402, PJ403, PJ501, PJ602, PJ801, PJ802, PJ803, PJ805

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				Custom	LA-8126P	1.0
				Date:	Tuesday, March 12, 2013	Sheet 3 of 51

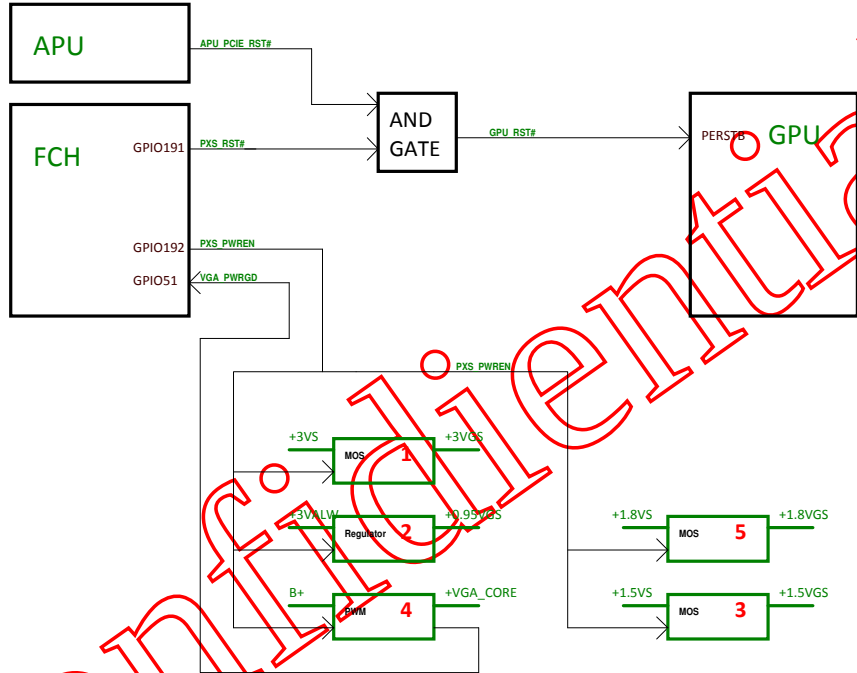
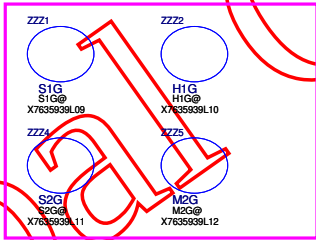
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



SUN PRO VRAM STRAP

Vendor	PS 3[2]	PS 3[1]	PS 3[0]	R pu	R pd
H5TQ2G63DFR-11C SA00003Y070	0	0	0	R1430 NC	R1436 4.75K
K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
K4W4G1646B-BC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53K	R1436 4.99K
MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24K	R1436 5.63K
K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 3.24K	R1436 10k
	1	1	1	R1430 4.75K	R1436 NC



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				Custm	LA-8126P	10
				Date	Tuesday, March 12, 2013	Sheet 4 of 51

[17] PCIE_CRX_GTX_P[0..7]

[17] PCIE_CRX_GTX_N[0..7]

PCIE_CTX_GRX_P[0..7] [17]

PCIE_CTX_GRX_N[0..7] [17]



JCPU1A

PCI EXPRESS

PCIE_CRX_GTX_P0 AB8
PCIE_CRX_GTX_N0 AB7
PCIE_CRX_GTX_P1 AA9
PCIE_CRX_GTX_N1 AA8
PCIE_CRX_GTX_P2 AA5
PCIE_CRX_GTX_N2 AA6
PCIE_CRX_GTX_P3 Y8
PCIE_CRX_GTX_N3 Y7
PCIE_CRX_GTX_P4 W9
PCIE_CRX_GTX_N4 W8
PCIE_CRX_GTX_P5 W5
PCIE_CRX_GTX_N5 W6
PCIE_CRX_GTX_P6 V8
PCIE_CRX_GTX_N6 V7
PCIE_CRX_GTX_P7 U9
PCIE_CRX_GTX_N7 U8

P.GFX_RXP0
P.GFX_RXN0
P.GFX_RXP1
P.GFX_RXN1
P.GFX_RXP2
P.GFX_RXN2
P.GFX_RXP3
P.GFX_RXN3
P.GFX_RXP4
P.GFX_RXN4
P.GFX_RXP5
P.GFX_RXN5
P.GFX_RXP6
P.GFX_RXN6
P.GFX_RXP7
P.GFX_RXN7
P.GFX_RXP8
P.GFX_RXN8
P.GFX_RXP9
P.GFX_RXN9
P.GFX_RXP10
P.GFX_RXN10
P.GFX_RXP11
P.GFX_RXN11
P.GFX_RXP12
P.GFX_RXN12
P.GFX_RXP13
P.GFX_RXN13
P.GFX_RXP14
P.GFX_RXN14
P.GFX_RXP15
P.GFX_RXN15

GRAPHICS

P.GFX_TXP0
P.GFX_TXN0
P.GFX_TXP1
P.GFX_TXN1
P.GFX_TXP2
P.GFX_TXN2
P.GFX_TXP3
P.GFX_TXN3
P.GFX_TXP4
P.GFX_TXN4
P.GFX_TXP5
P.GFX_TXN5
P.GFX_TXP6
P.GFX_TXN6
P.GFX_TXP7
P.GFX_TXN7
P.GFX_TXP8
P.GFX_TXN8
P.GFX_TXP9
P.GFX_TXN9
P.GFX_TXP10
P.GFX_TXN10
P.GFX_TXP11
P.GFX_TXN11
P.GFX_TXP12
P.GFX_TXN12
P.GFX_TXP13
P.GFX_TXN13
P.GFX_TXP14
P.GFX_TXN14
P.GFX_TXP15
P.GFX_TXN15

AB2 PCIE_CTX_C_GRX_P0 C1 DIS@ 1
AB1 PCIE_CTX_C_GRX_N0 C2 DIS@ 1
AA3 PCIE_CTX_C_GRX_P1 C3 DIS@ 1
AA2 PCIE_CTX_C_GRX_N1 C4 DIS@ 1
Y5 PCIE_CTX_C_GRX_P2 C5 DIS@ 1
Y4 PCIE_CTX_C_GRX_N2 C6 DIS@ 1
W3 PCIE_CTX_C_GRX_P3 C7 DIS@ 1
W2 PCIE_CTX_C_GRX_N3 C8 DIS@ 1
W5 PCIE_CTX_C_GRX_P4 C9 DIS@ 1
W4 PCIE_CTX_C_GRX_N4 C10 DIS@ 1
V5 PCIE_CTX_C_GRX_P5 C11 DIS@ 1
V4 PCIE_CTX_C_GRX_N5 C12 DIS@ 1
V2 PCIE_CTX_C_GRX_P6 C13 DIS@ 1
V1 PCIE_CTX_C_GRX_N6 C14 DIS@ 1
U3 PCIE_CTX_C_GRX_P7 C15 DIS@ 1
U2 PCIE_CTX_C_GRX_N7 C16 DIS@ 1

2 .1U 0402 16V7K PCIE_CTX_GRX_P0
2 .1U 0402 16V7K PCIE_CTX_GRX_N0
2 .1U 0402 16V7K PCIE_CTX_GRX_P1
2 .1U 0402 16V7K PCIE_CTX_GRX_N1
2 .1U 0402 16V7K PCIE_CTX_GRX_P2
2 .1U 0402 16V7K PCIE_CTX_GRX_N2
2 .1U 0402 16V7K PCIE_CTX_GRX_P3
2 .1U 0402 16V7K PCIE_CTX_GRX_N3
2 .1U 0402 16V7K PCIE_CTX_GRX_P4
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2 .1U 0402 16V7K PCIE_CTX_GRX_P5
2 .1U 0402 16V7K PCIE_CTX_GRX_N5
2 .1U 0402 16V7K PCIE_CTX_GRX_P6
2 .1U 0402 16V7K PCIE_CTX_GRX_N6
2 .1U 0402 16V7K PCIE_CTX_GRX_P7
2 .1U 0402 16V7K PCIE_CTX_GRX_N7

SDV/EVT, NO.1

SDV/EVT, NO.1

LAN

WLAN

[35] PCIE_CRX_DTX_P0
[35] PCIE_CRX_DTX_N0
[33] PCIE_CRX_DTX_P1
[33] PCIE_CRX_DTX_N1

Card Reader

[35] PCIE_CRX_DTX_P3
[35] PCIE_CRX_DTX_N3

[12] UMI_RXP0
[12] UMI_RXN0
[12] UMI_RXP1
[12] UMI_RXN1
[12] UMI_RXP2
[12] UMI_RXN2
[12] UMI_RXP3
[12] UMI_RXN3

+1.2VS 1 R1 2 P_ZVDDP 196_0402_1% AG11

P_ZVDDP

LOTES_ACA-ZIF-109-P12-A_FST1R2
CONN@

LAN

WLAN

Card Reader

Card Reader

Card Reader

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P.GPP_RXP0
P.GPP_RXN0
P.GPP_RXP1
P.GPP_RXN1
P.GPP_RXP2
P.GPP_RXN2
P.GPP_RXP3
P.GPP_RXN3

LAN

WLAN

Card Reader

Card Reader

Card Reader

Card Reader

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Card Reader

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AD5 PCIE_CTX_C_DRX_P0 C33 1
AD4 PCIE_CTX_C_DRX_N0 C34 1
AD2 PCIE_CTX_C_DRX_P1 C123 1
AD1 PCIE_CTX_C_DRX_N1 C124 1
AC3
AC2
AB5 PCIE_CTX_C_DRX_P3 C35 1
AB4 PCIE_CTX_C_DRX_N3 C36 1

AG2 UMI_TXP0 C C37 1
AG3 UMI_TXN0 C C38 1
AF4 UMI_TXP1 C C39 1
AF5 UMI_TXN1 C C40 1
AF7 UMI_TXP2 C C41 1
AF2 UMI_TXN2 C C42 1
AE3 UMI_TXP3 C C43 1
AE3 UMI_TXN3 C C44 1

AP11 P_ZVSS 1 R2 2 196_0402_1%

Power Sequence of APU

+1.5V

+2.5VS

+1.5VS

+APU_CORE

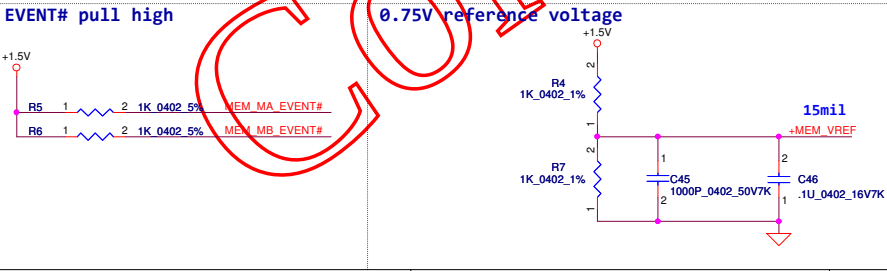
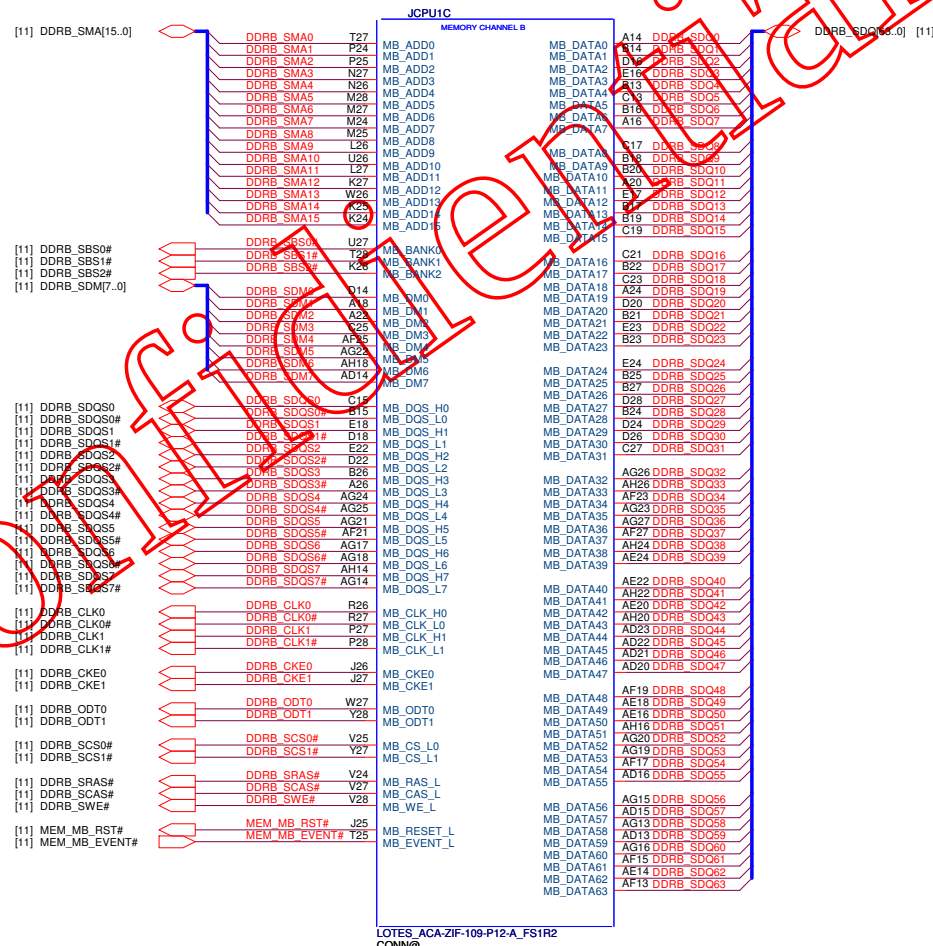
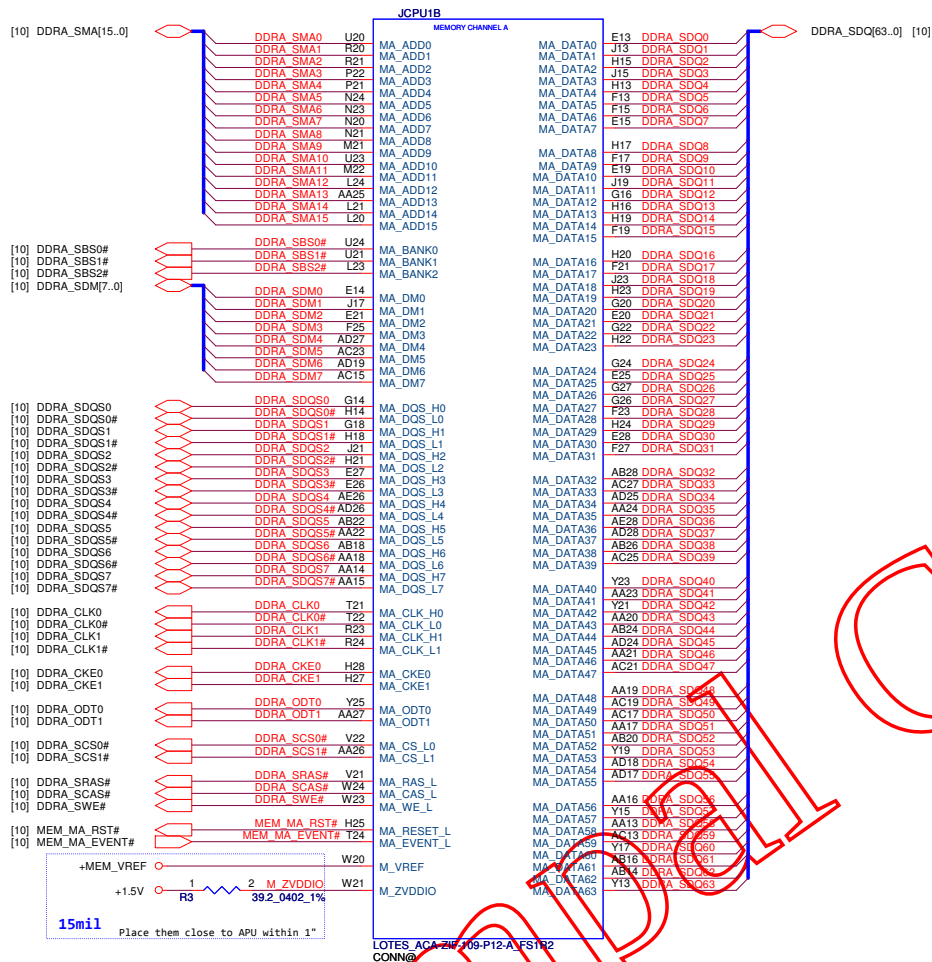
+APU_CORE_NB

+1.2VS

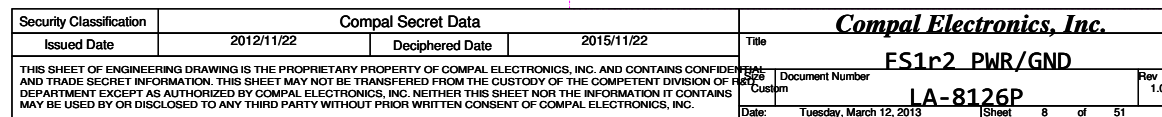
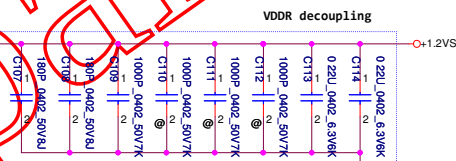
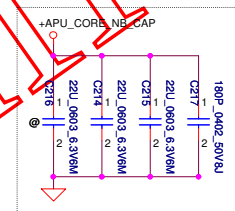
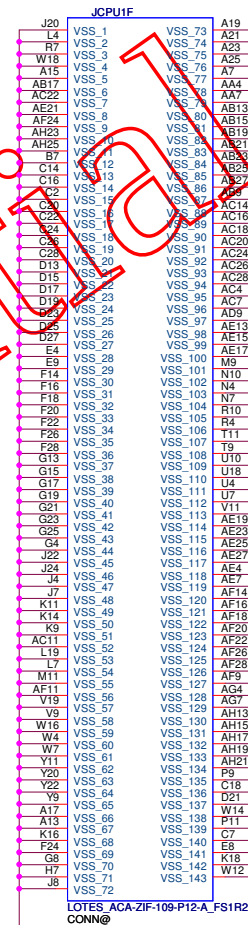
Group A

Group B

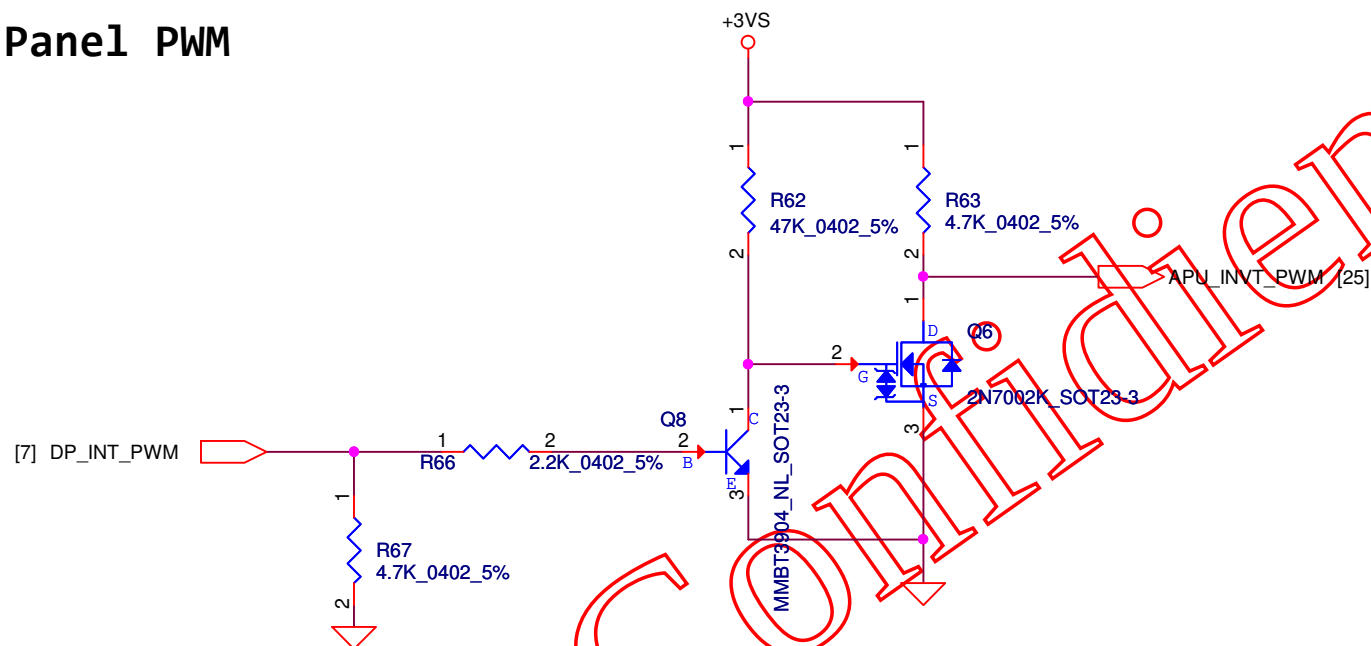
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						Document Number		Rev	
						Customer		1.0	
						Date		Tuesday, March 12, 2013	
						Sheet		5 of 51	
						LA-8126P			



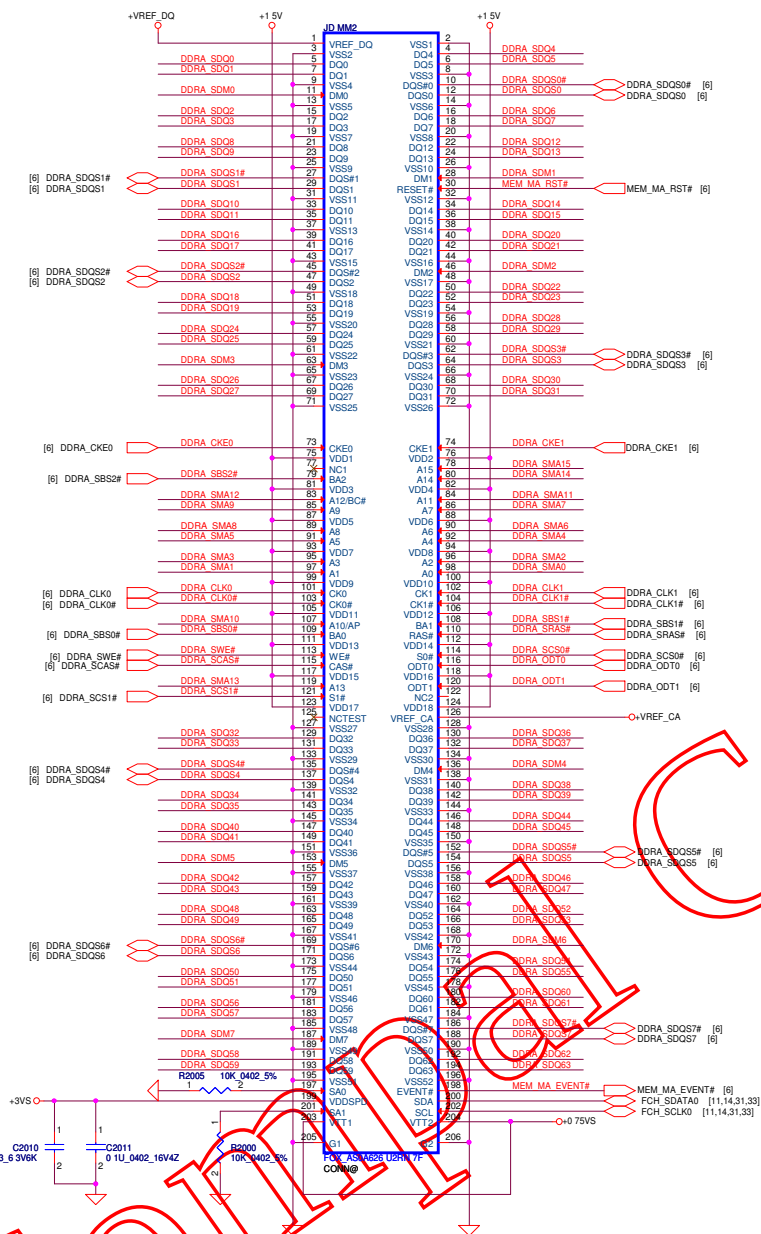
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				Document Number	
				Custom	LA-8126P
				Date:	Tuesday, March 12, 2013
				Sheet	6 of 51
				Rev	1.0



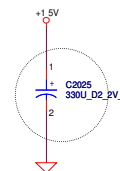
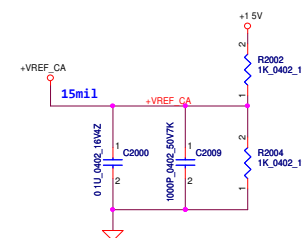
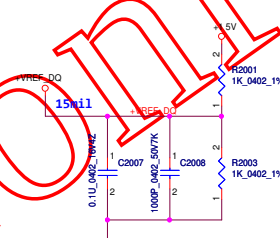
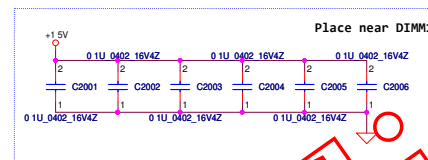
Panel PWM



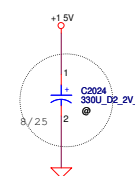
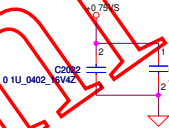
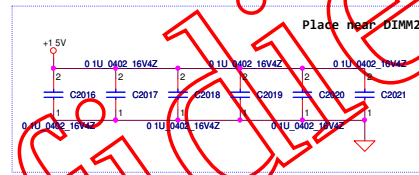
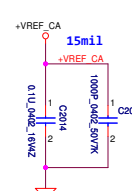
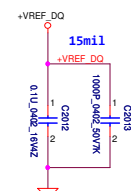
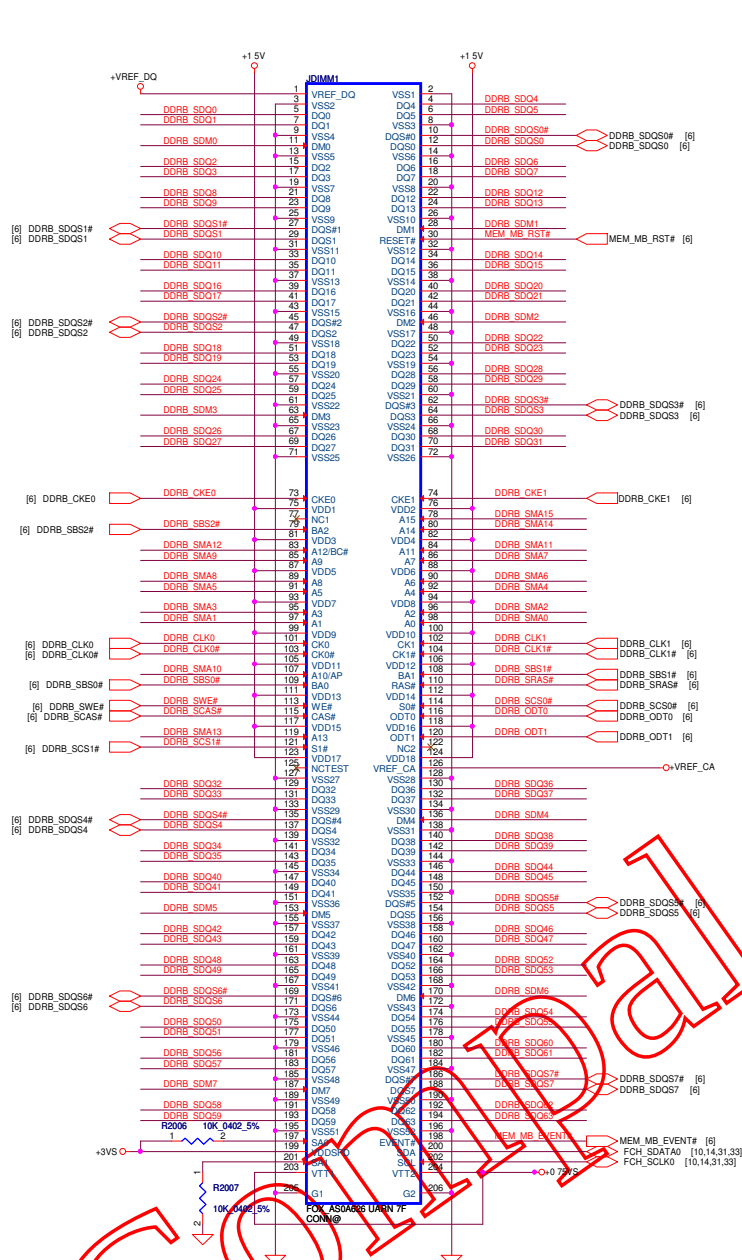
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				Rev	1.0
Date: Tuesday, March 12, 2013		Sheet 9 of 51			



DDRA_SDQ0 63# DDRA_SDQ0 63# [6]
 DDRA_SDM0 7# DDRA_SDM0 7# [6]
 DDRA_SMA0 15# DDRA_SMA0 15# [6]

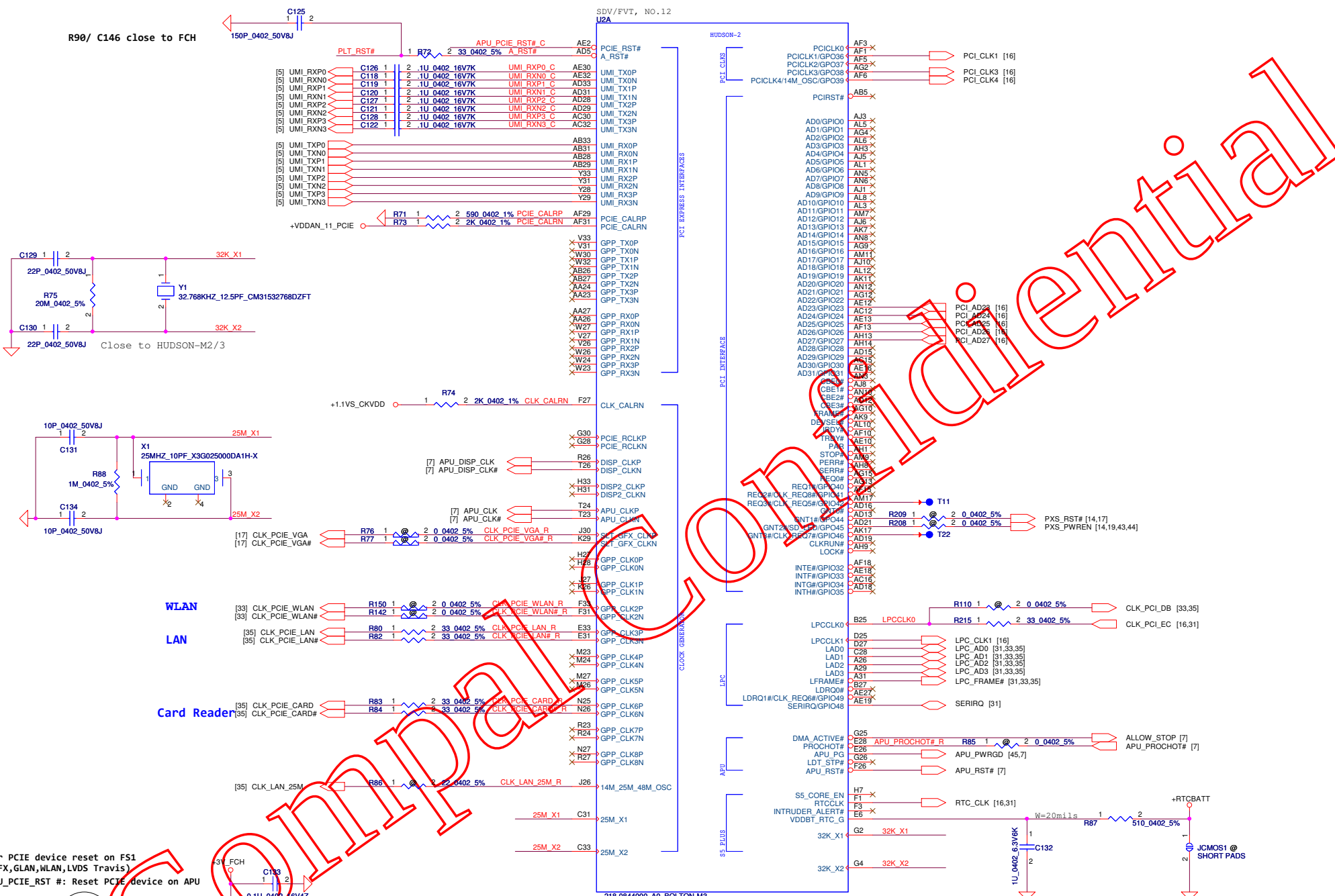


Reverse H:5.2mm

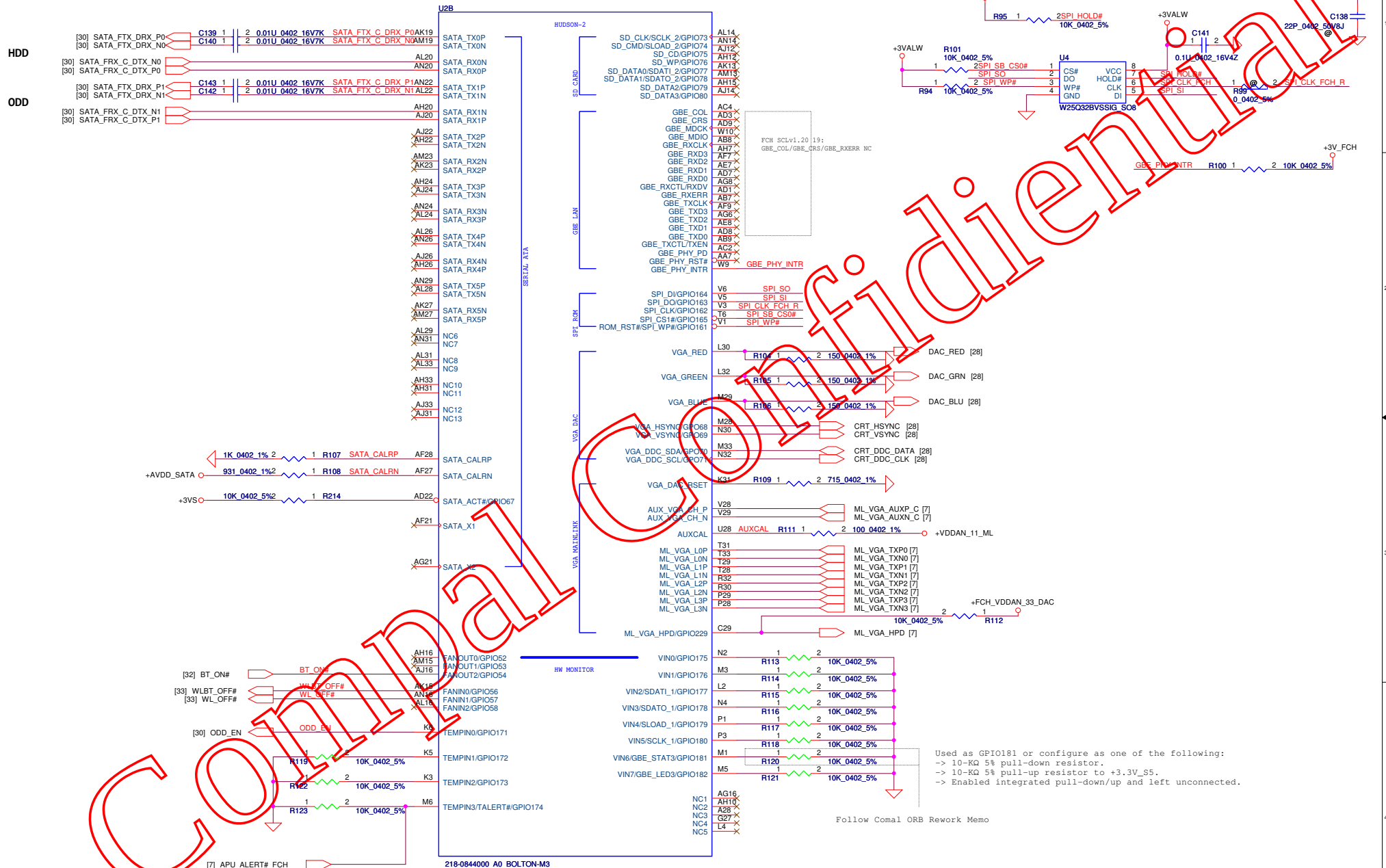


Reverse H:9.2mm

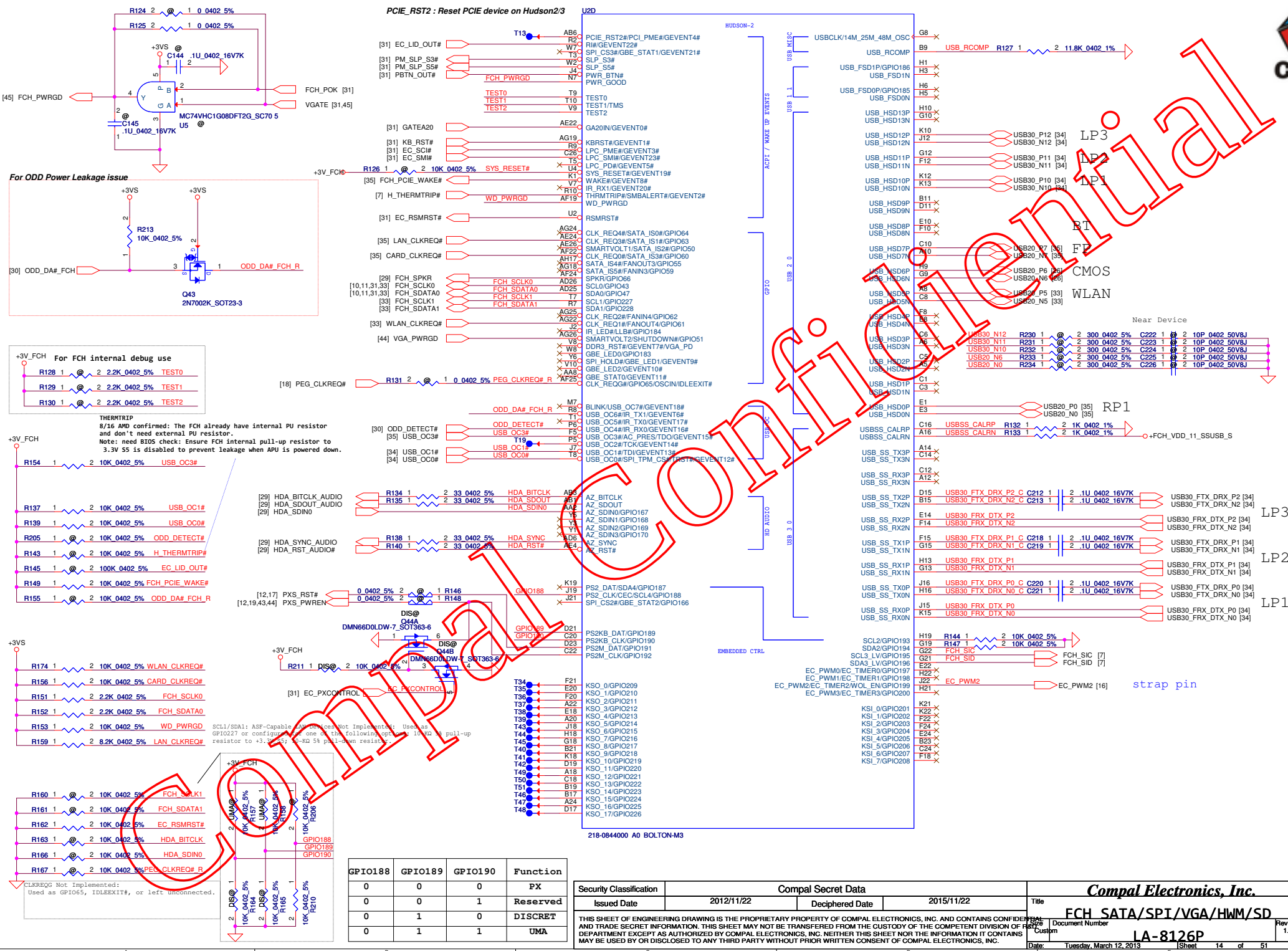
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Size	C	Document Number	LA-8126P	Rev 10
Date:	Tuesday, March 12, 2013	Sheet	11	of 51



4MB SPI ROM
& Non-share ROM.

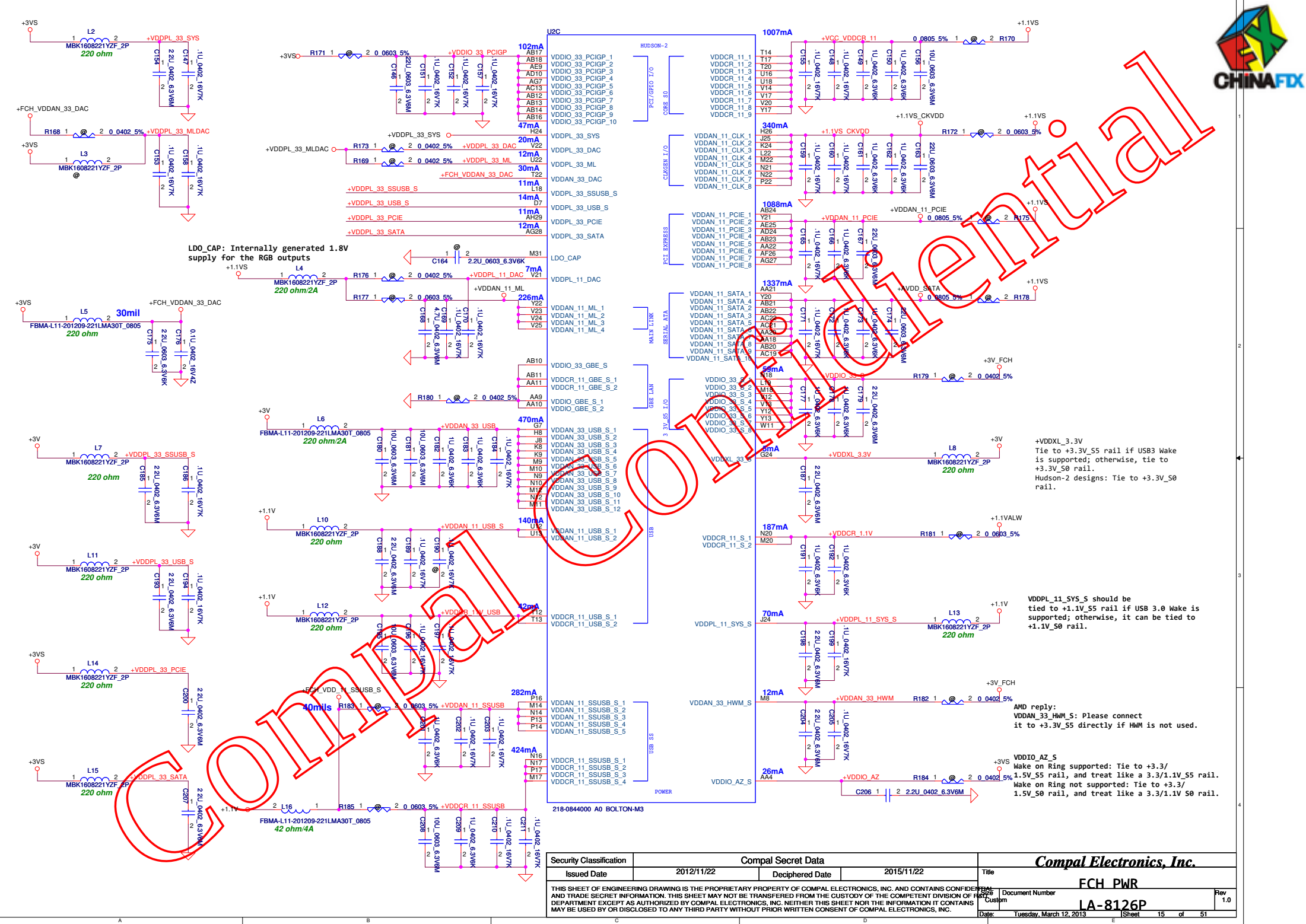


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FCH SATA/SPI/VGA/HWM/SD
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				Date	Tuesday, March 12, 2013
				Sheet	13 of 51



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

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Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FCH_SATA/SPI/VGA/HWM/SD
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				Customer	1.0
				Date: Tuesday, March 12, 2013	Sheet 14 of 51
				LA-8126P	

[illegible]

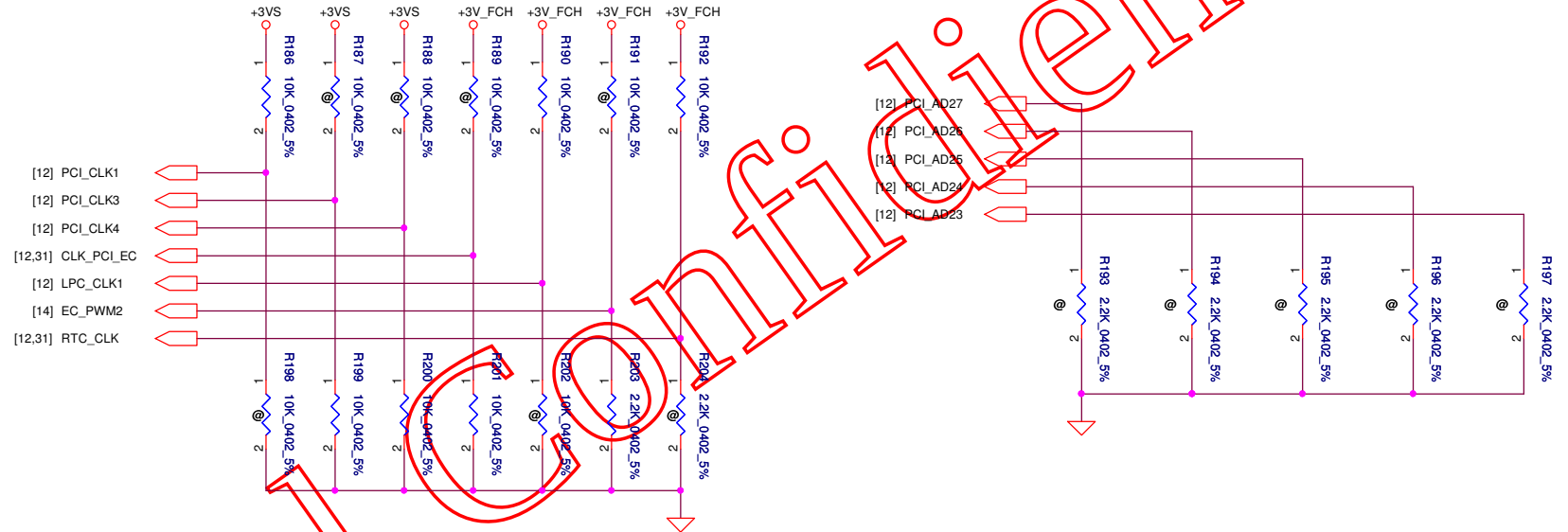
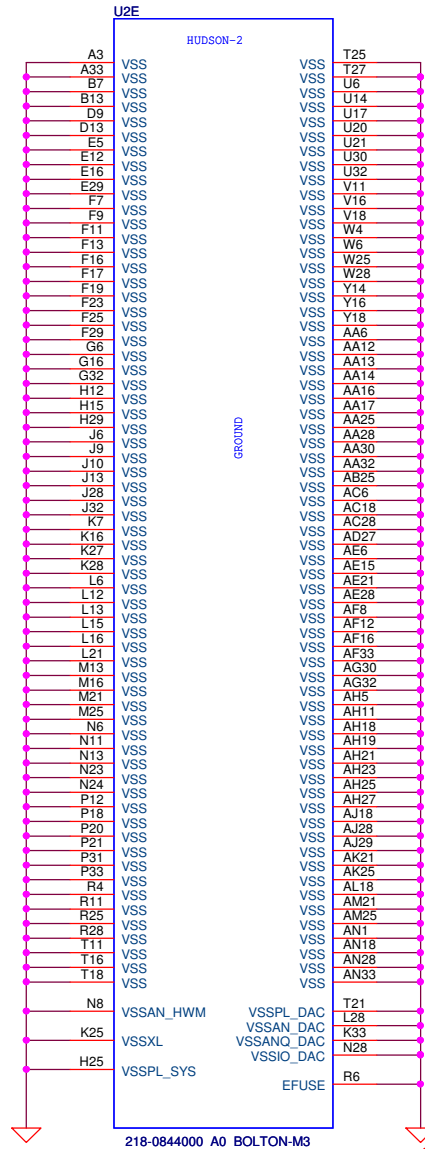
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS DEFAULT	NON FUSION CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

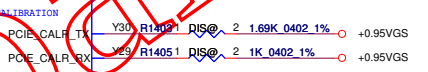
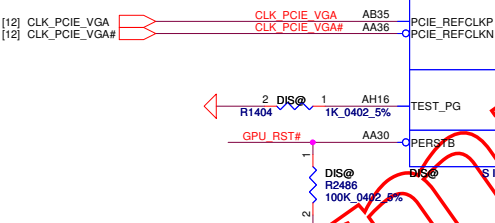
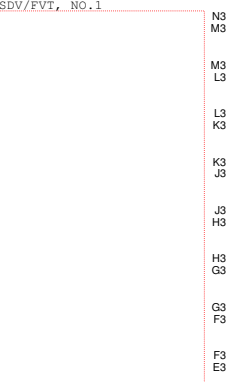
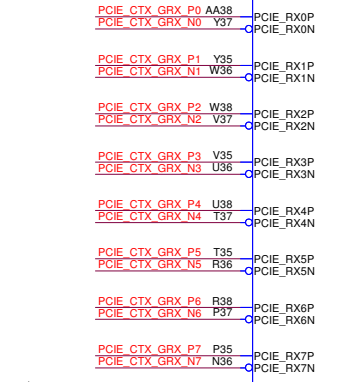


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				Date	Tuesday, March 12, 2013
				Sheet	16 of 51

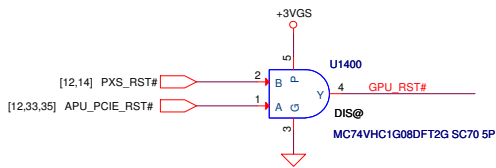
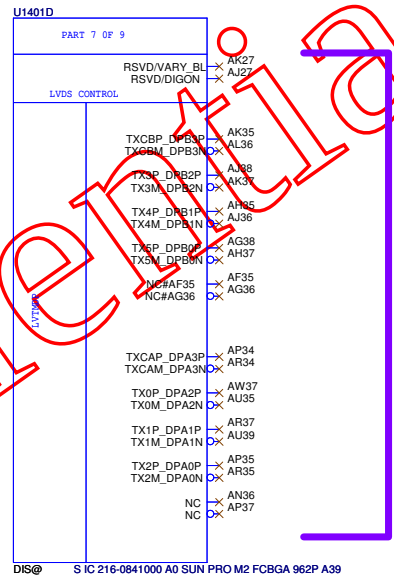
[5] PCIE_CTX_GRX_P[7..0] → PCIE_CTX_GRX_P[7..0]
 [5] PCIE_CTX_GRX_N[7..0] → PCIE_CTX_GRX_N[7..0]

SDV/FVT, NO.3
 U1401A
 PART 1 OF 9

PCIE_CRX_GTX_P[7..0] → PCIE_CRX_GTX_P[7..0] [5]
 PCIE_CRX_GTX_N[7..0] → PCIE_CRX_GTX_N[7..0] [5]



LVDS Interface

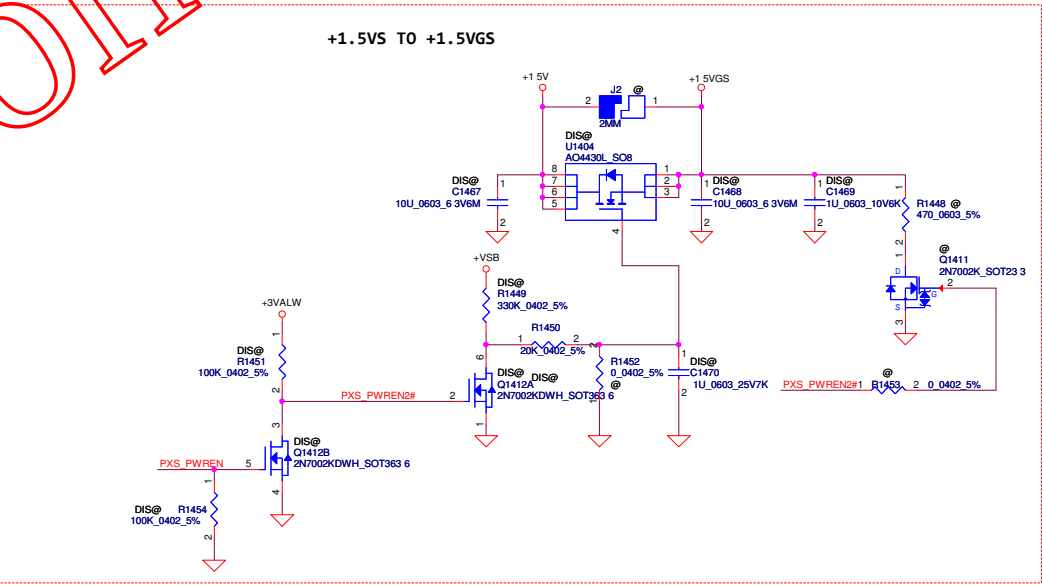
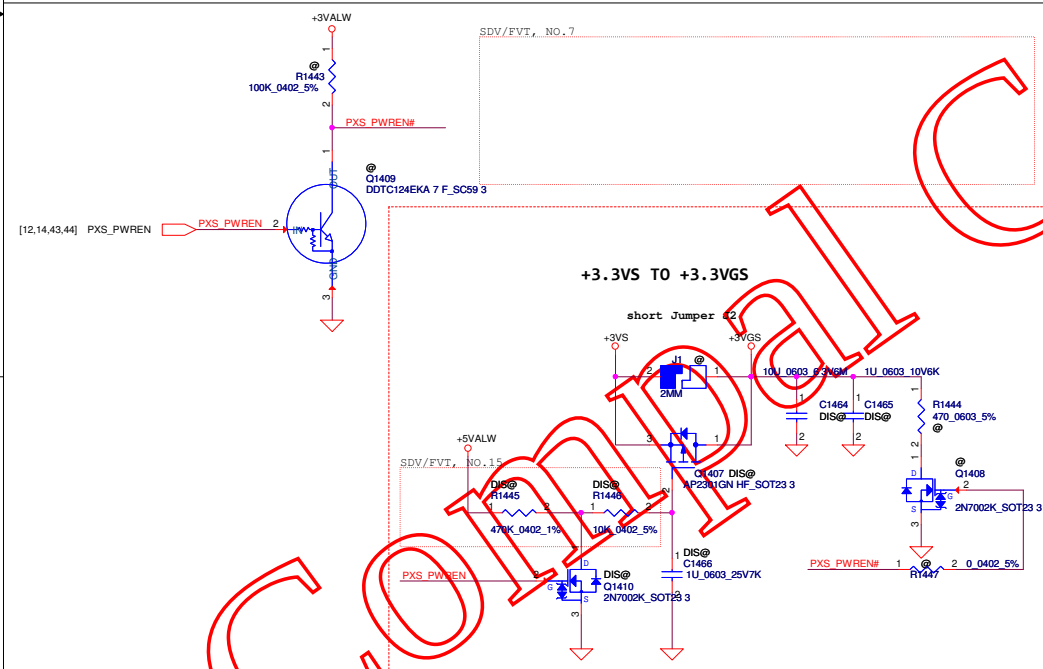
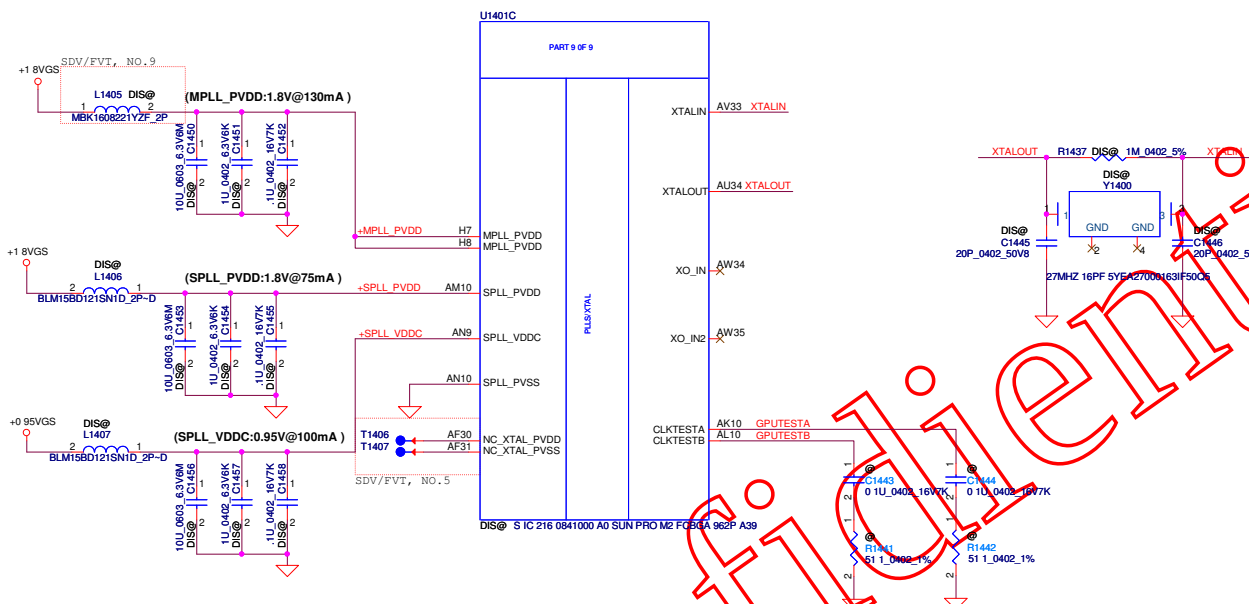


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				Document Number				LA-8126P			
				Date				Tuesday, March 12, 2013			
				Sheet				17 of 51			

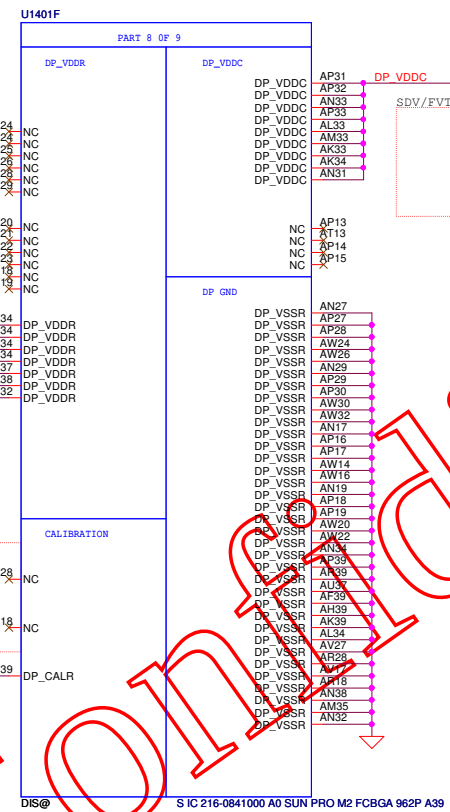
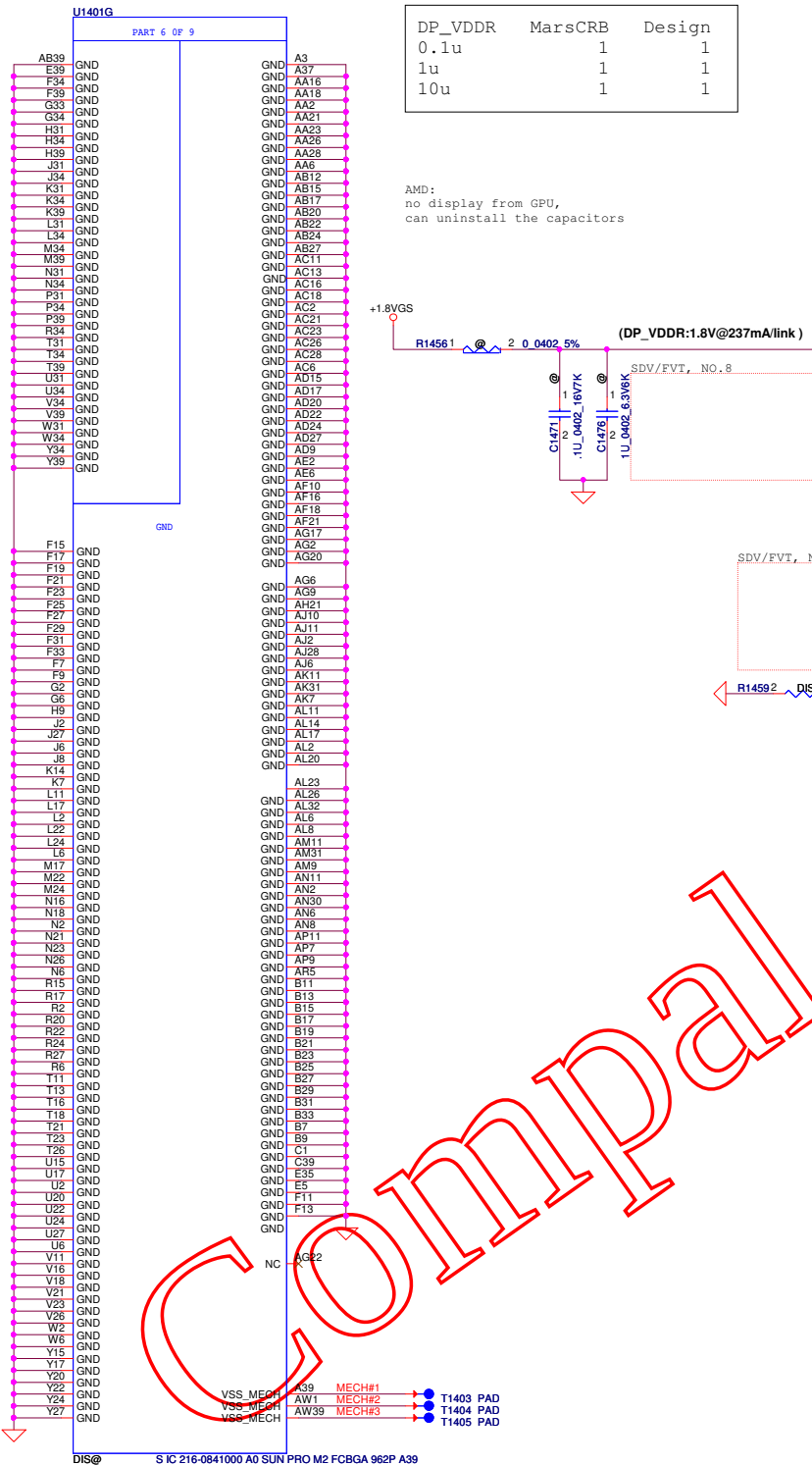
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



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DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

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										LA-8126P		1.0	
										Date: Tuesday, March 12, 2013		Sheet 20 of 51	

For GDDR5, MVDDQ = 1.5V

(VDDR1:1.5V@3A,GDDR5:1125MHz)

PCIE_VDDR	MarsCRB	Design
0.1u	5	0
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	5	5
10u		

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

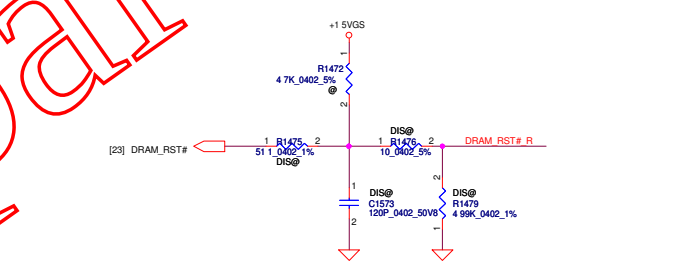
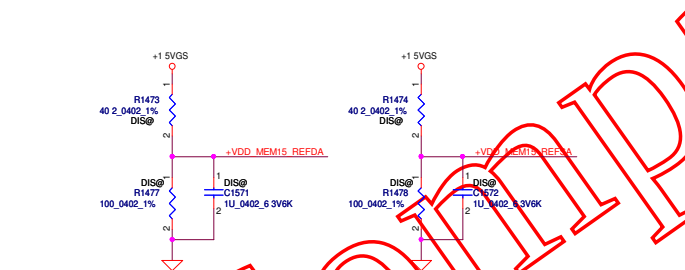
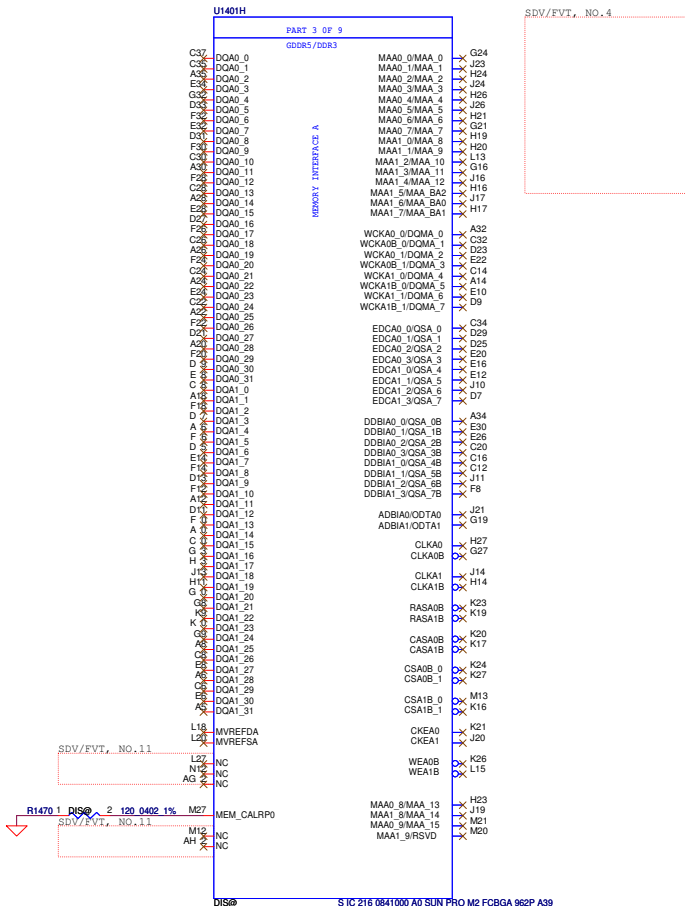
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

for Sun Pro Ball name AD12,AF11,AF12,AF13,AF15,AG11,AG13,AG15

Route as differential pair

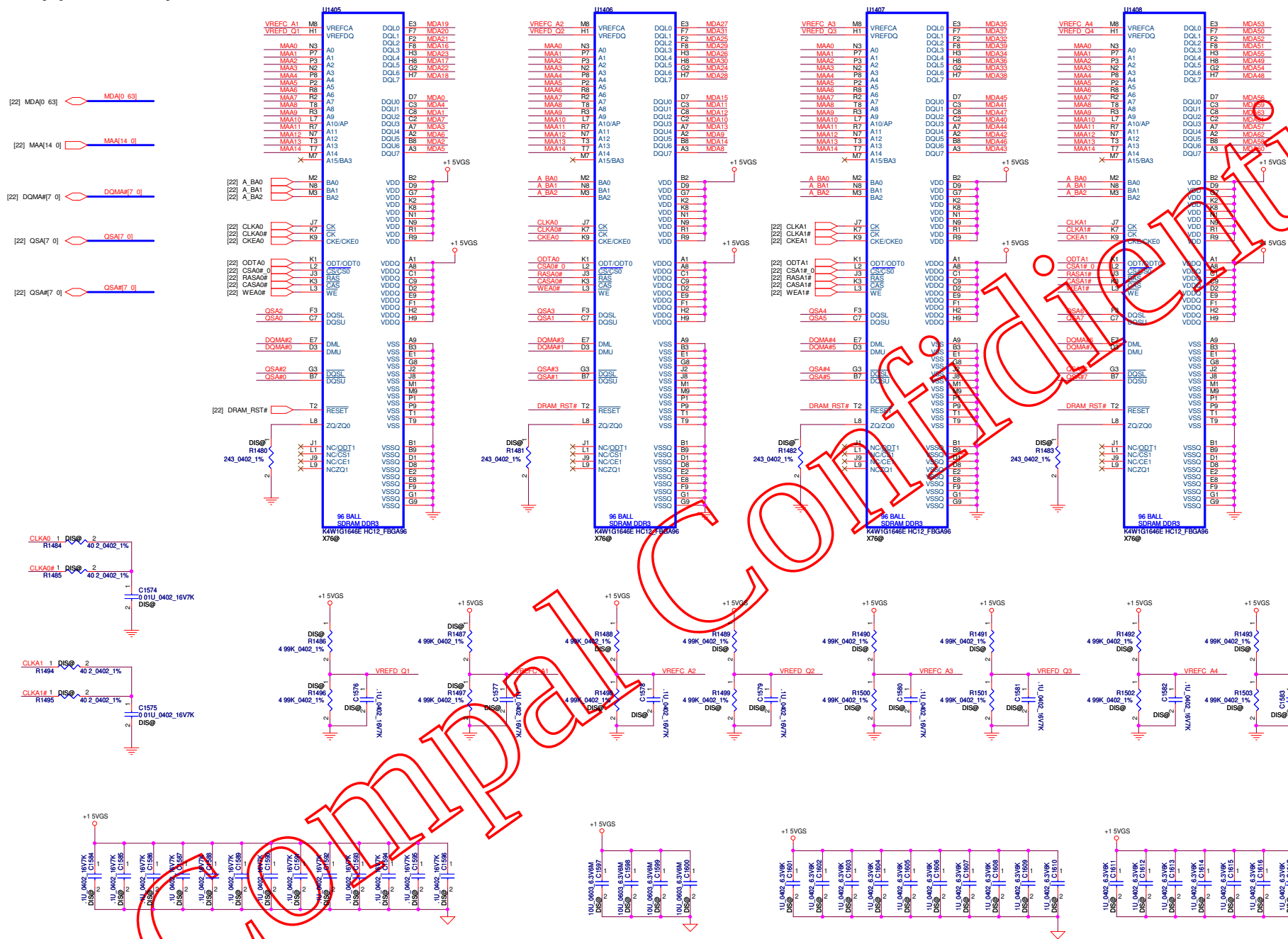


DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

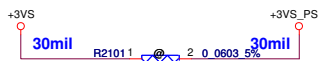
The Seymour M2 only support channel B (64 bit),
this page unmount all parts





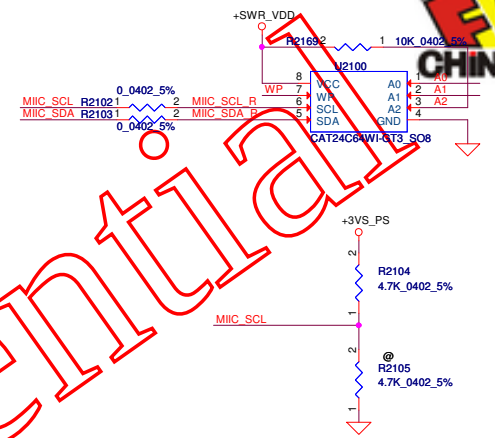
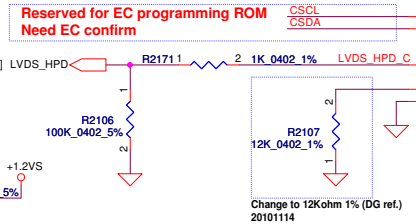
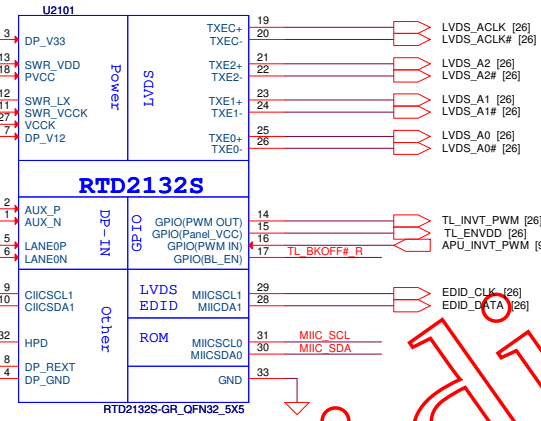
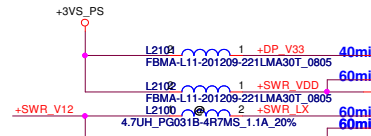
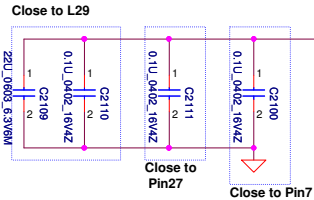
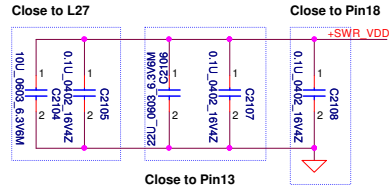
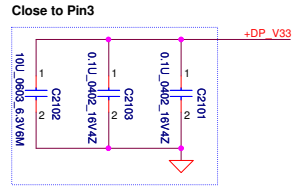
Compal Confidential

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2012/11/22		2015/11/22		ATT Sun Pro M2 VRAM_B	
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		C		LA-8126P	10
		Date:		Tuesday, March 12, 2013	Sheet 24 of 51

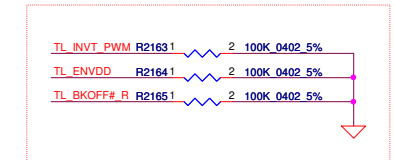
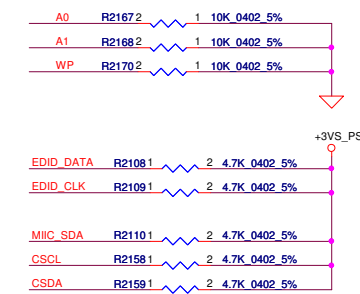


Part number: SA00004EU10

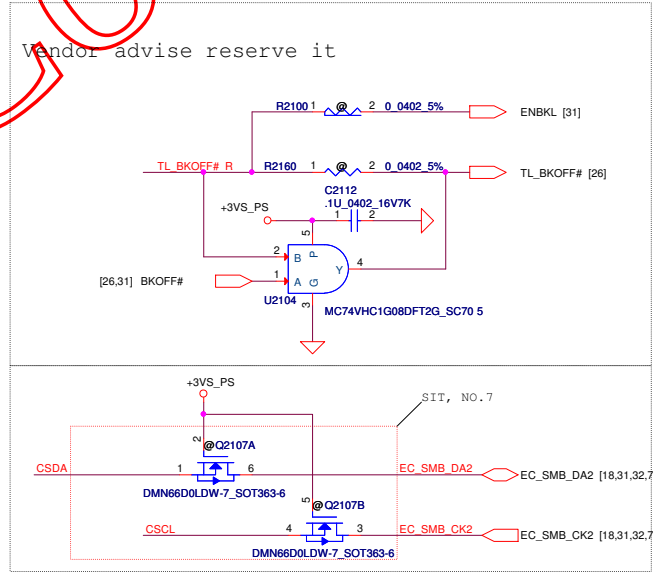
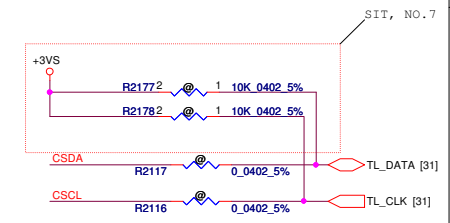
EEROM



2132S-Ver E: External ROM, pin31 PU +3VS
Internal RAM support, pin31 PD to GND
EEROM EEROM EEROM EEROM

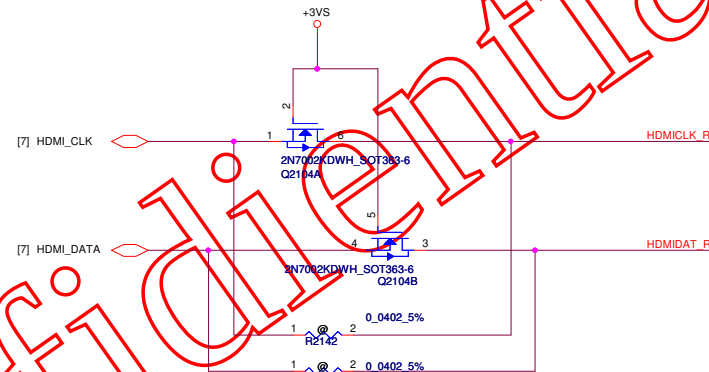
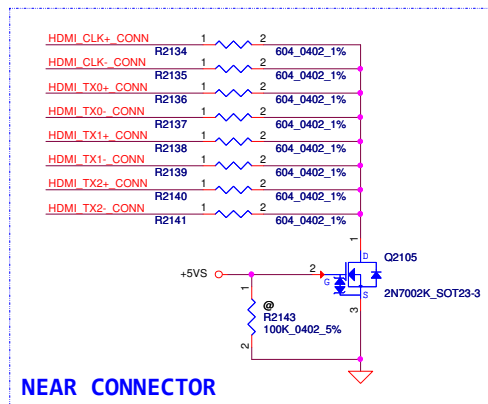
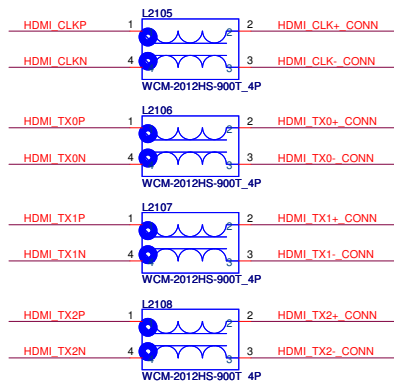


Vendor Suggest 2011.08.15

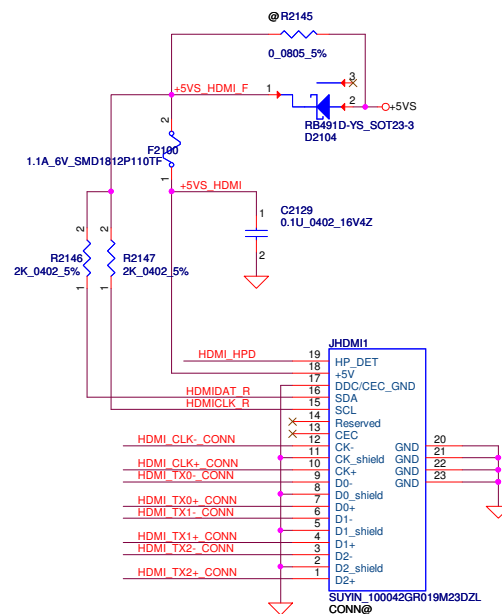
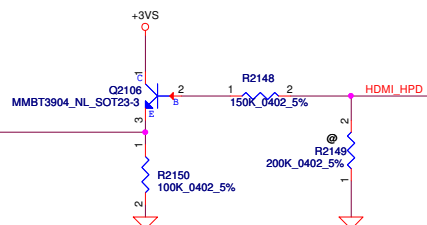
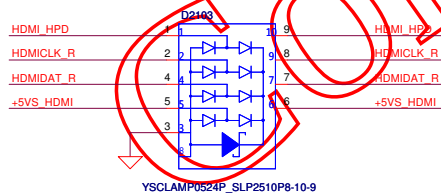
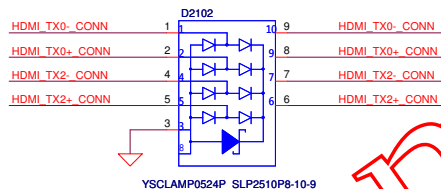
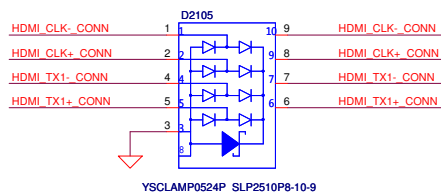


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				Date:	Tuesday, March 12, 2013
				Sheet	25 of 51

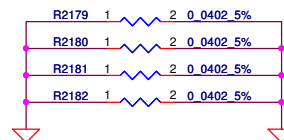
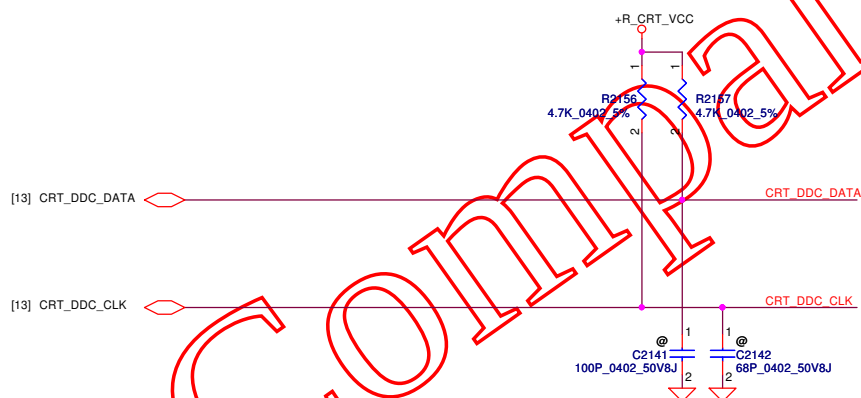
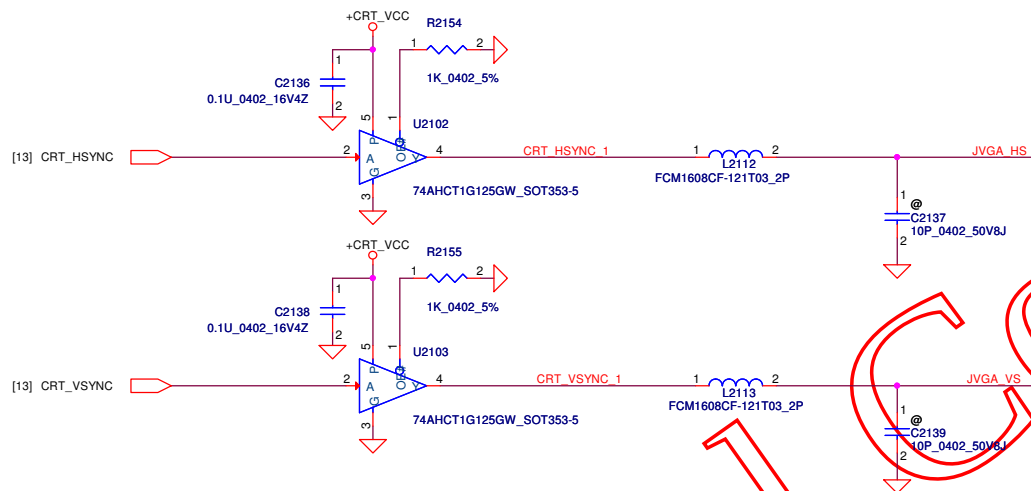
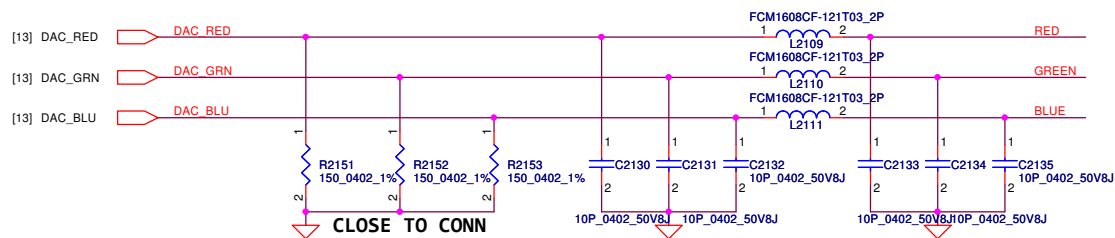
[7] HDMI_CLKP	R2126	1	2	0	0402_5%	HDMI_CLK+_CONN
[7] HDMI_CLKN	R2127	1	2	0	0402_5%	HDMI_CLK-_CONN
[7] HDMI_TX0P	R2128	1	2	0	0402_5%	HDMI_TX0+_CONN
[7] HDMI_TX0N	R2129	1	2	0	0402_5%	HDMI_TX0-_CONN
[7] HDMI_TX1P	R2130	1	2	0	0402_5%	HDMI_TX1+_CONN
[7] HDMI_TX1N	R2131	1	2	0	0402_5%	HDMI_TX1-_CONN
[7] HDMI_TX2P	R2132	1	2	0	0402_5%	HDMI_TX2+_CONN
[7] HDMI_TX2N	R2133	1	2	0	0402_5%	HDMI_TX2-_CONN



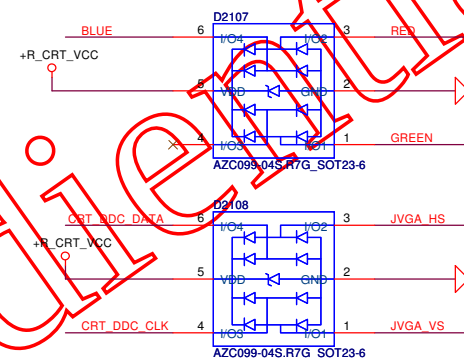
ESD Request



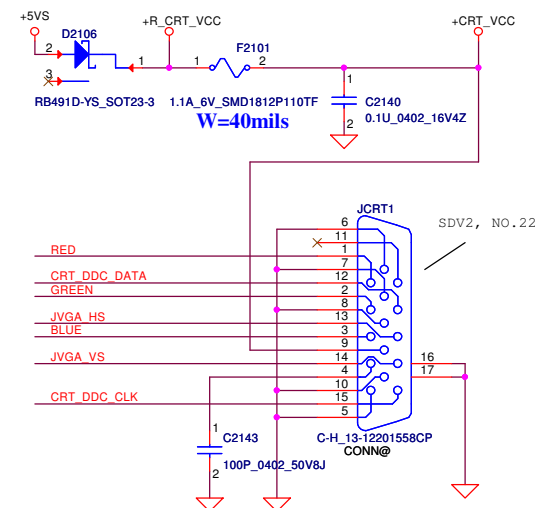
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						Internal Document Number		Rev 1.0	
						Customer		LA-8126P	
Date:						Tuesday, March 12, 2013		Sheet 27 of 51	



ESD Request



CRT Connector



AMD check list update
20101110

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				Size	Document Number	Rev
				Custom	LA-8126P	1.0
Date:		Tuesday, March 12, 2013		Sheet	28 of 51	

Compal Electronics, Inc.

CRT Connector

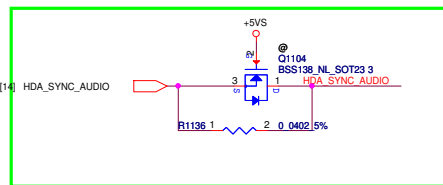
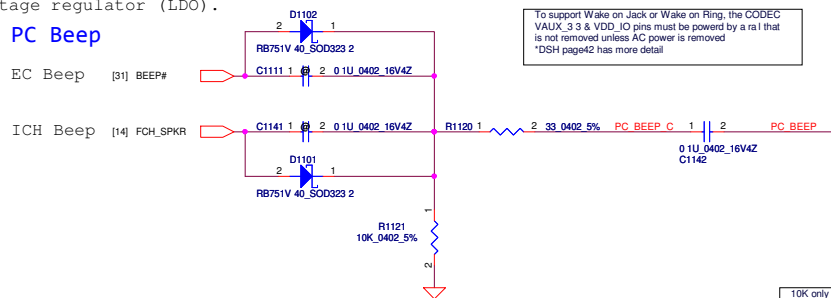
LA-8126P

1.0

An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).

An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

EC Beep

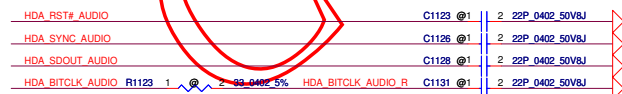


+CLASSD_5V

Signal	Value	Frequency	Label
C1115	1	2 0 1U_0402_16V4Z	Near Pin 12
C1117	1	2 10U_0603_6 3V6M	Near Pin 12
C1118	1	2 0 1U_0402_16V4Z	Near Pin 12
C1120	1	2 10U_0603_6 3V6M	Near Pin 15

EMI

Signal	Value	Frequency	Label
HDA_RST# AUDIO	1	2 22P_0402_50VB/J	C1123 @1
HDA_SYNC AUDIO	1	2 22P_0402_50VB/J	C1126 @1
HDA_SDOUT AUDIO	1	2 22P_0402_50VB/J	C1128 @1
HDA_BITCLK AUDIO	1	2 22P_0402_50VB/J	C1131 @1



To support Wake on Jack or Wake on Ring, the CODEC VAUX_3 3 & VDD_IO pins must be powered by a rail that is not removed unless AC power is removed
*DSH page42 has more detail

10K only needed if supply to VAUX_3 3 is removed during system re start

EAPD active low
0=power down ex AMP
1=power up ex AMP

Internal DMIC

Internal SPEAKER

potential leakage concern

Internal Speaker

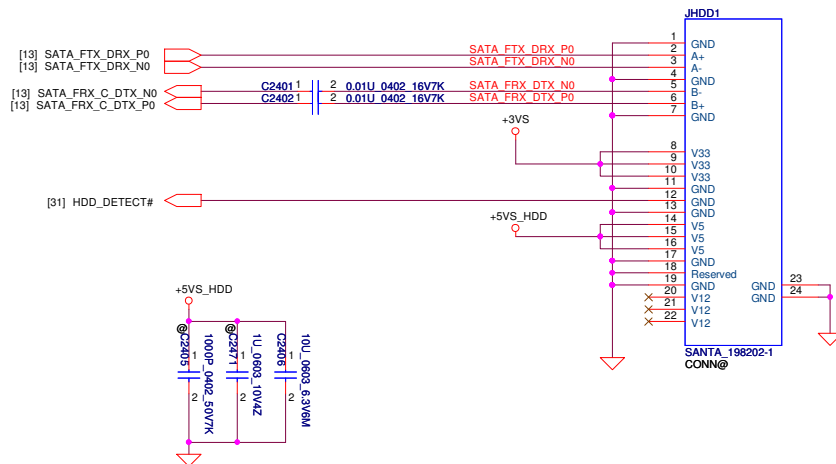
Width 20 mil

EMI

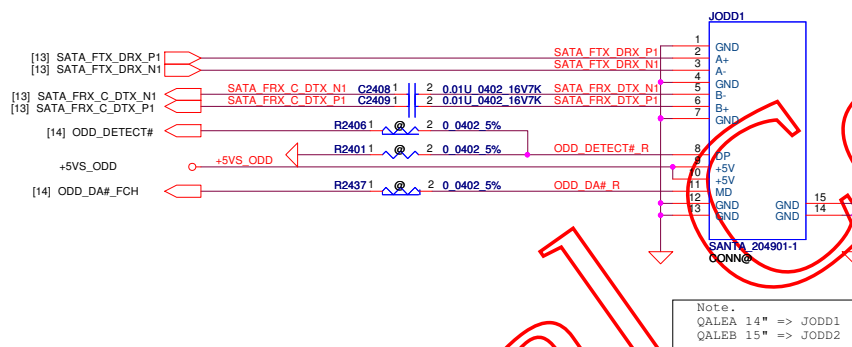
Note.
QALEA 14" => JSPK1 => 4Pin
QALEB 15" => JSPK1 => 6Pin

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				Custm		1
				LA-8126P		
Date	Tuesday, March 12, 2013			Sheet	29	of 51

SATA HDD Conn.

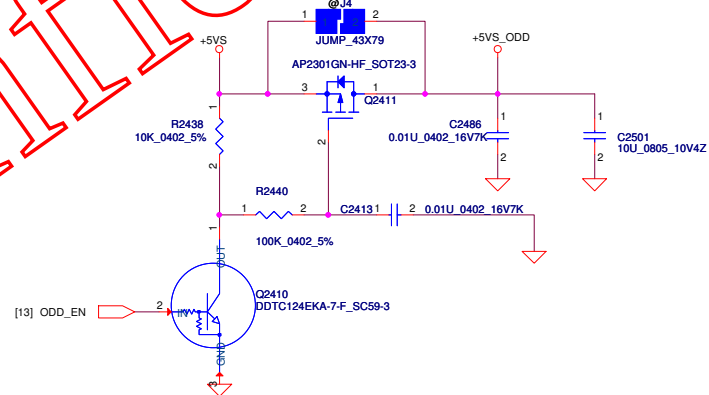


SATA ODD Conn.

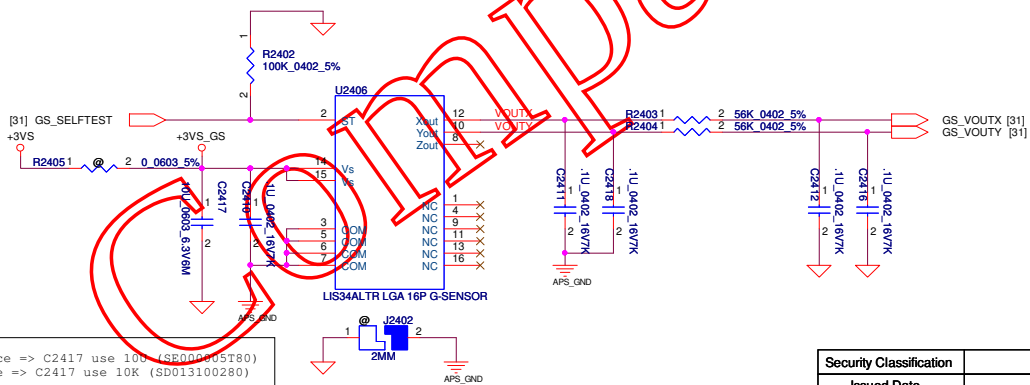


Note.
QALEA 14" => JODD1
QALEB 15" => JODD2

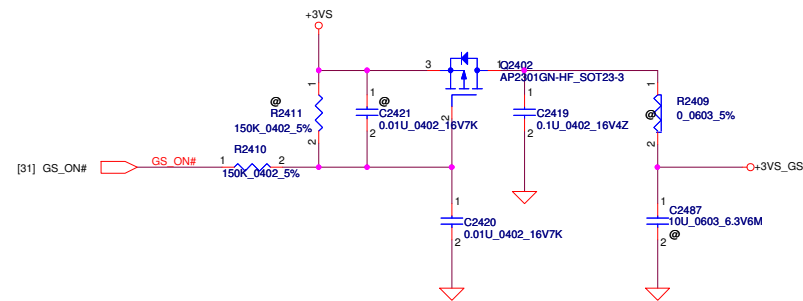
ODD Power Control1



APS G-Sensor

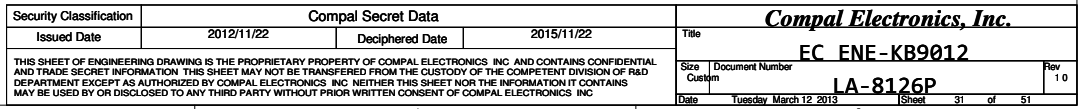


Note.
Main Source => C2417 use 10K (SD000005T80)
2nd Source => C2417 use 10K (SD013100280)

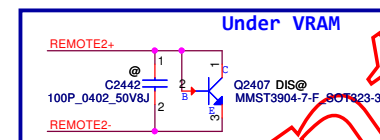
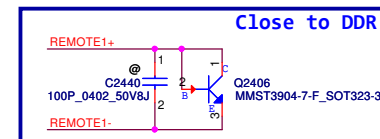
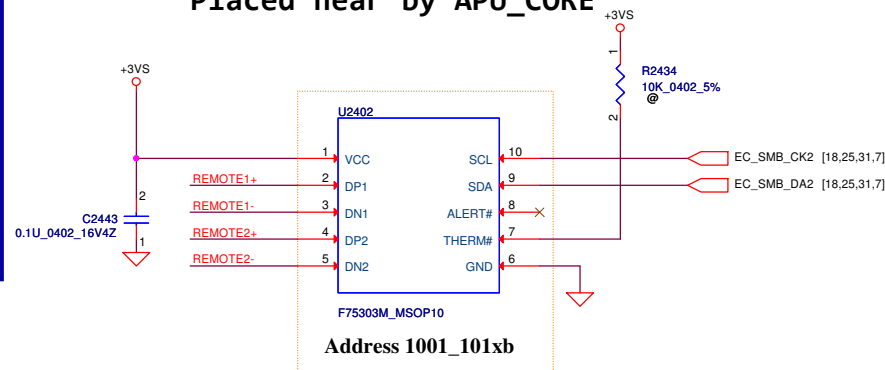
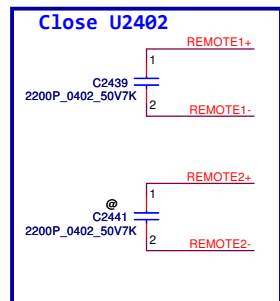


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HDD/ODD/G-Sensor				LA-8126P
Date: Tuesday, March 12, 2013				Sheet 30 of 51



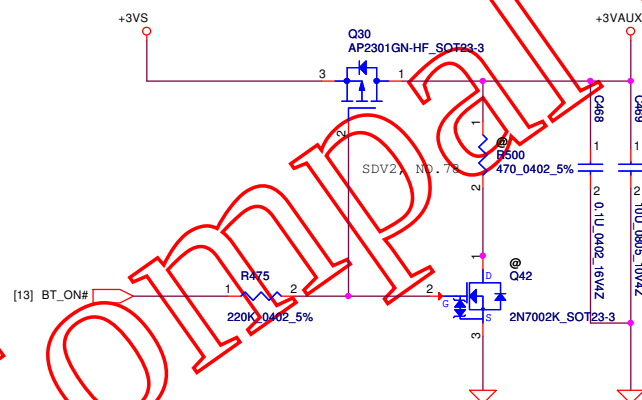
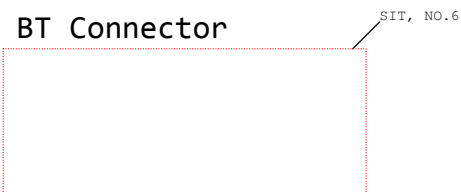


Fintek Thermal sensor Placed near by APU_CORE

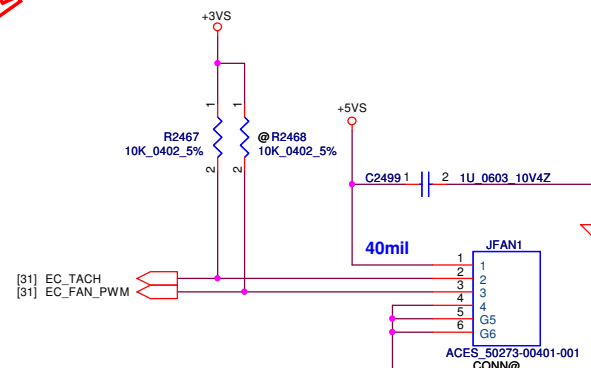


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

BT Connector

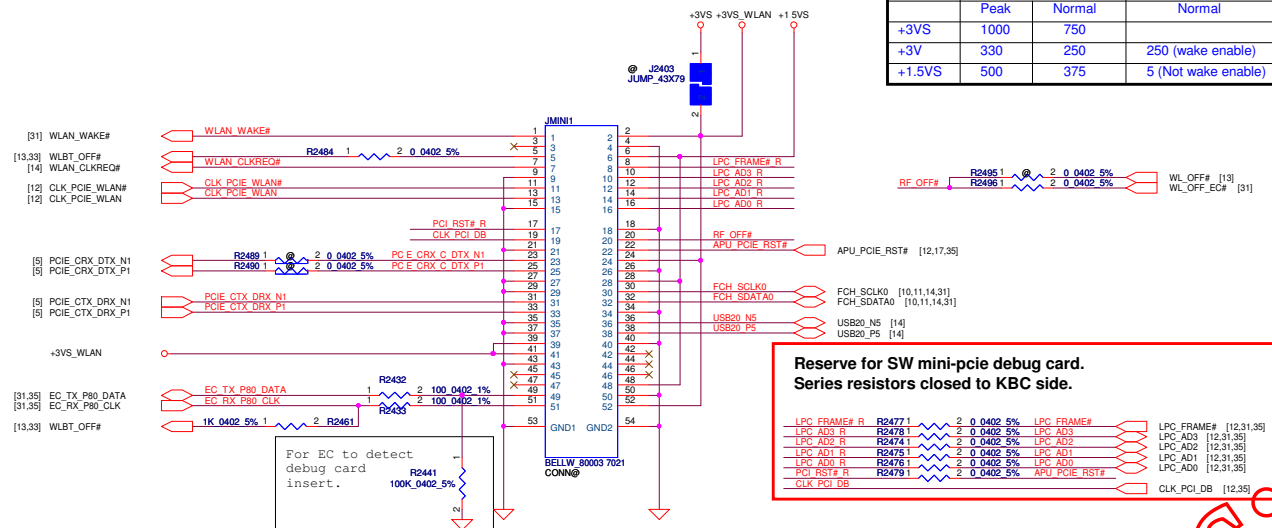


FAN1 Conn

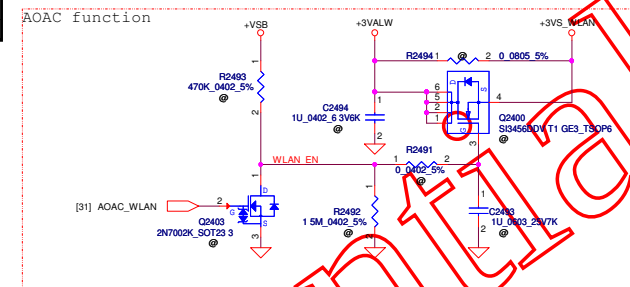


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				LA-8126P	
				Date	Rev
				Tuesday, March 12, 2013	1.0
				Sheet	32 of 51

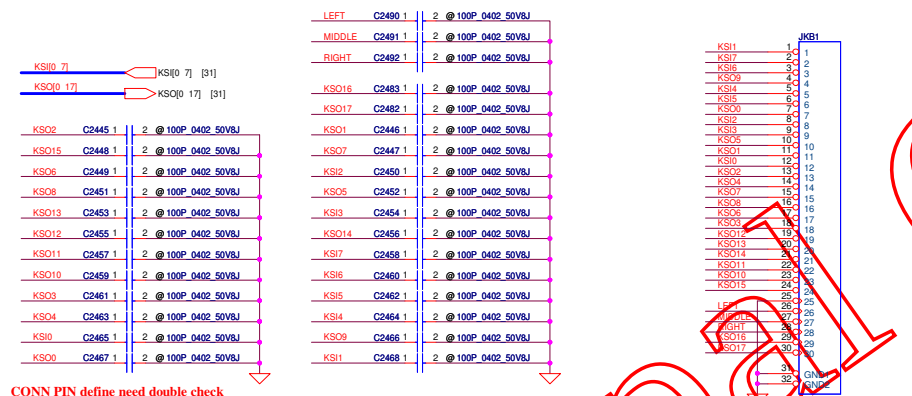
WLAN Conn



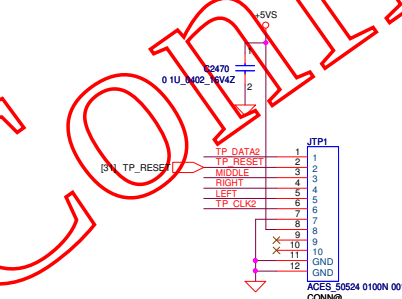
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



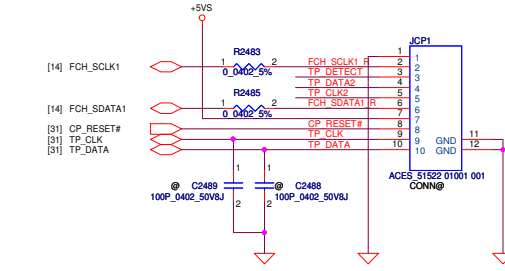
INT_KBD Conn.



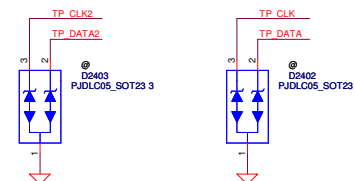
Track Point Conn



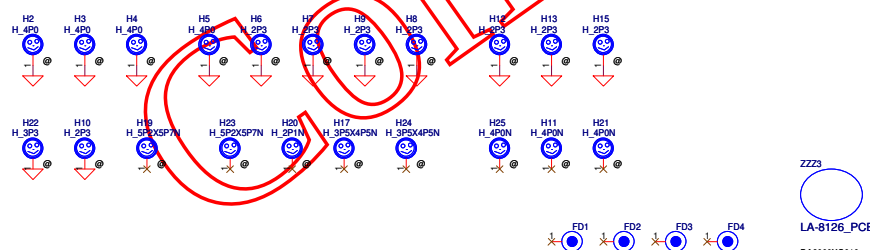
Click pad 10PIN

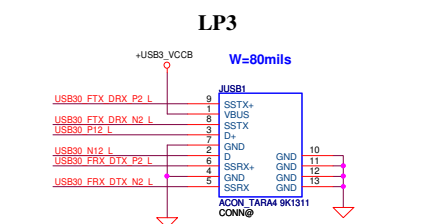
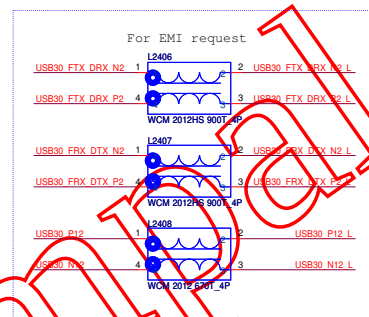


ESD Request



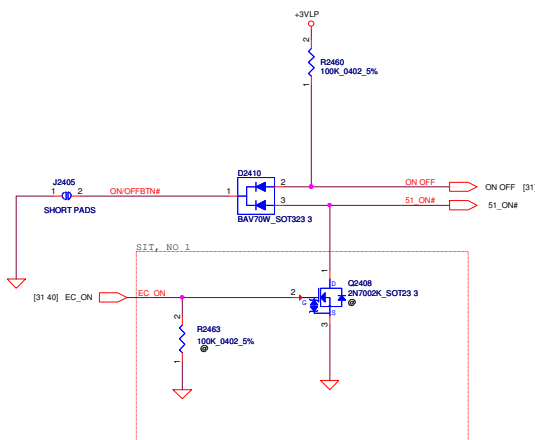
Screw Holes



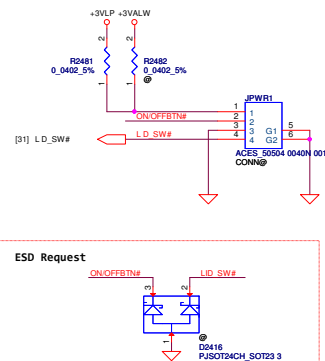
USB3.0 Conn *3

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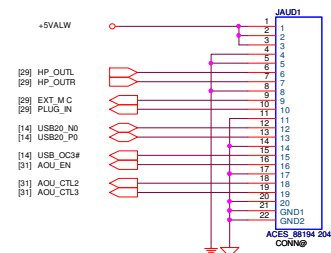
ON/OFF switch



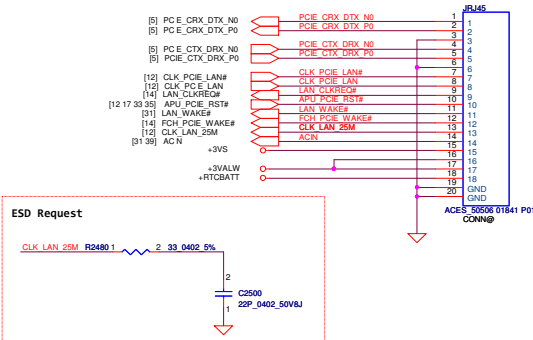
Power Button Board Conn



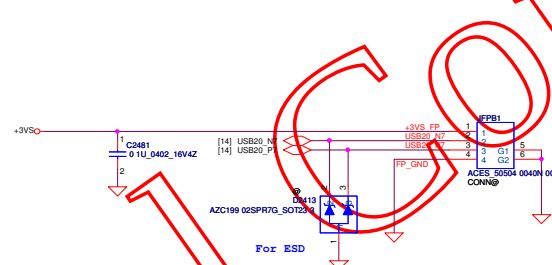
USB2.0/Audio Jack SB CONN



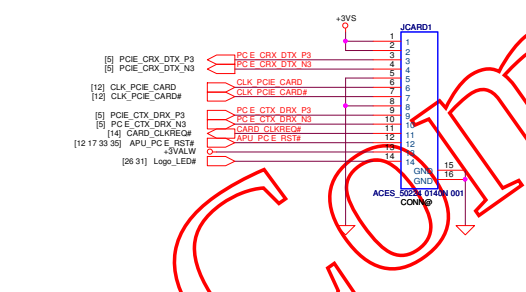
Lan Conn



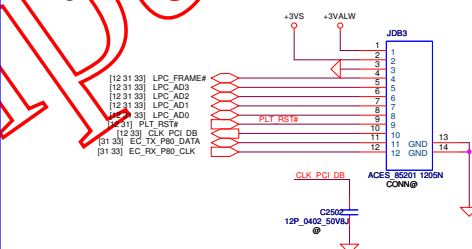
Finger Printer



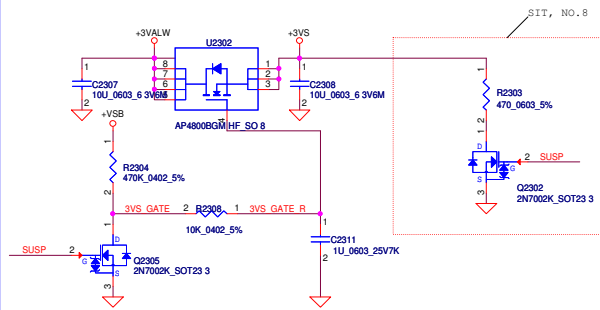
Card Reader



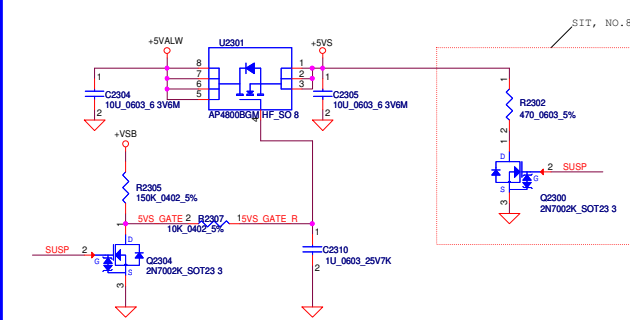
Debug Conn



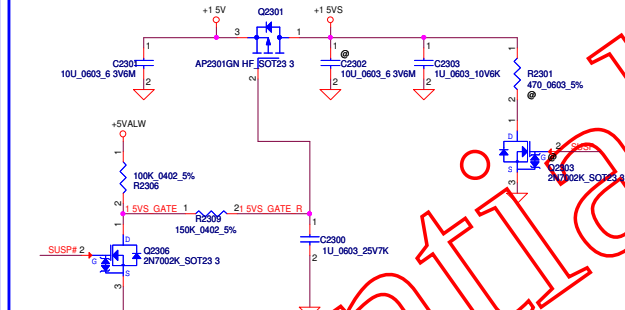
+3VALW TO +3VS



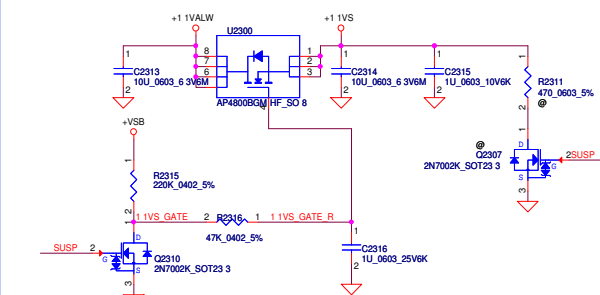
+5VALW TO +5VS



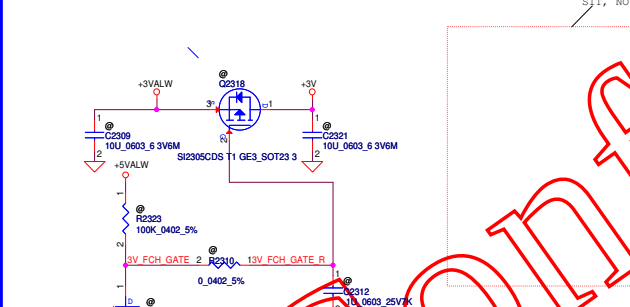
+1.5V to +1.5VS



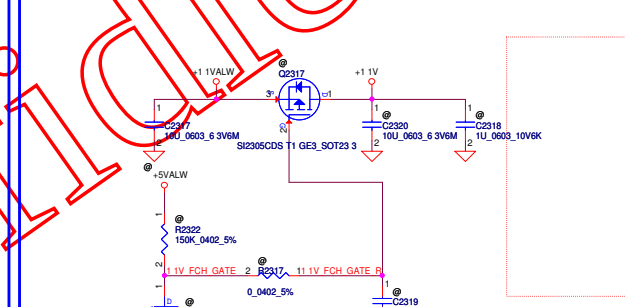
+1.1VALW to +1.1VS



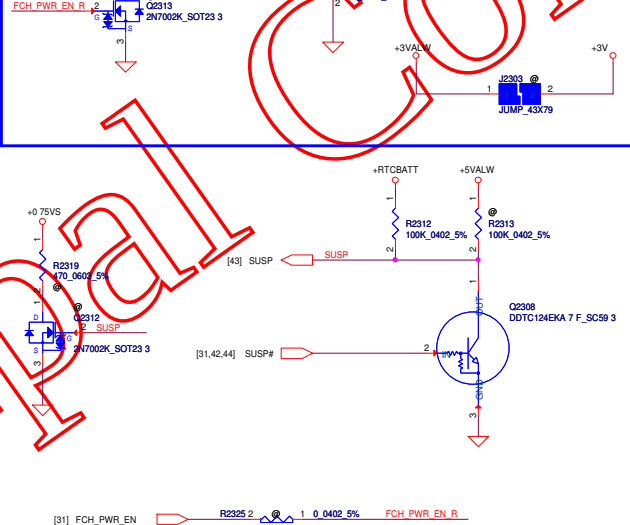
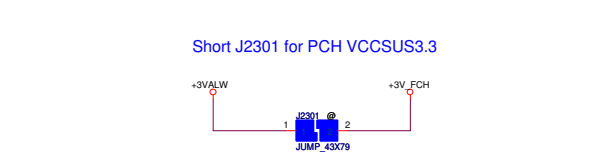
+3VALW TO +3V



+1.1VALW to +1.1V

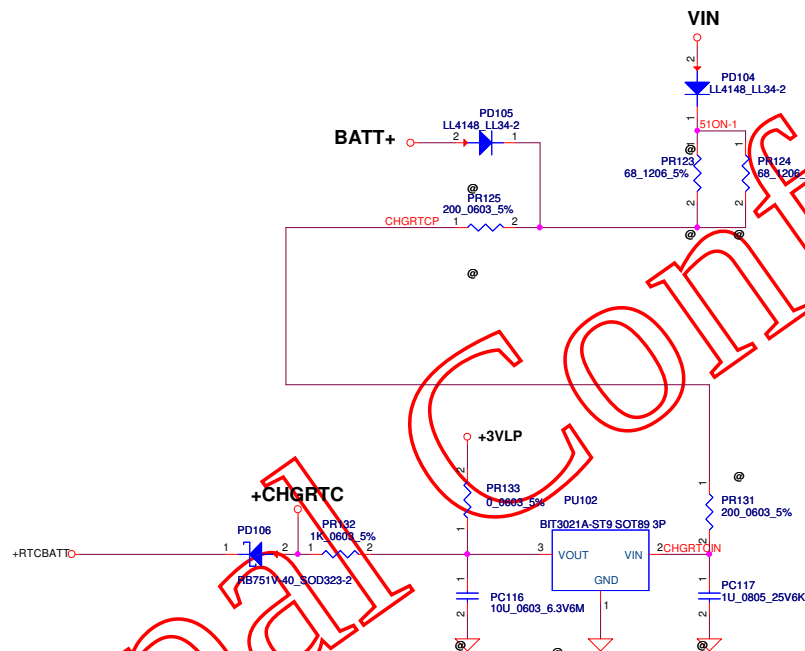
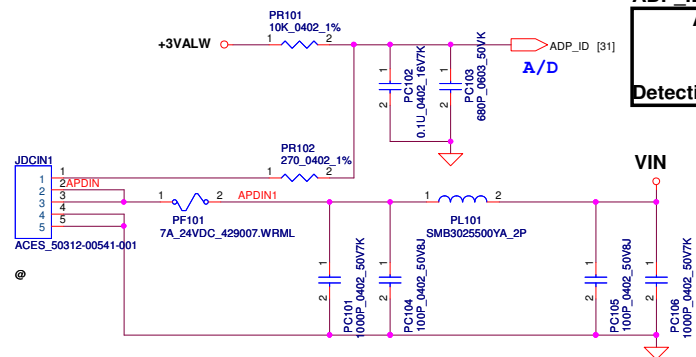


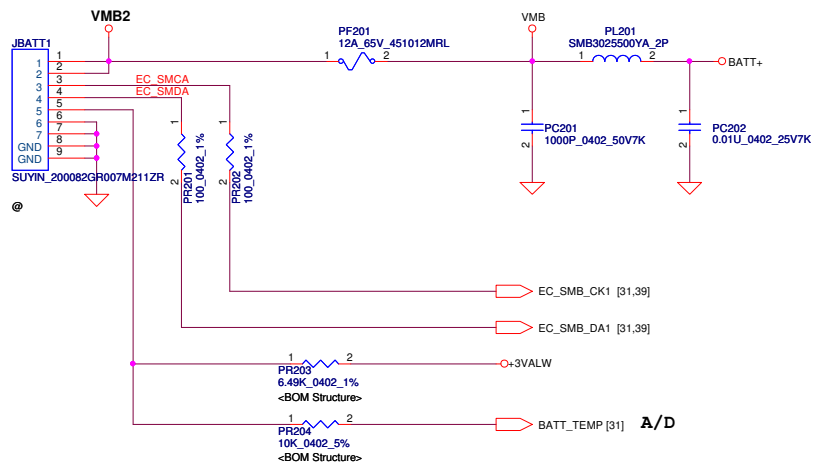
+3VALW TO +3V_FCH



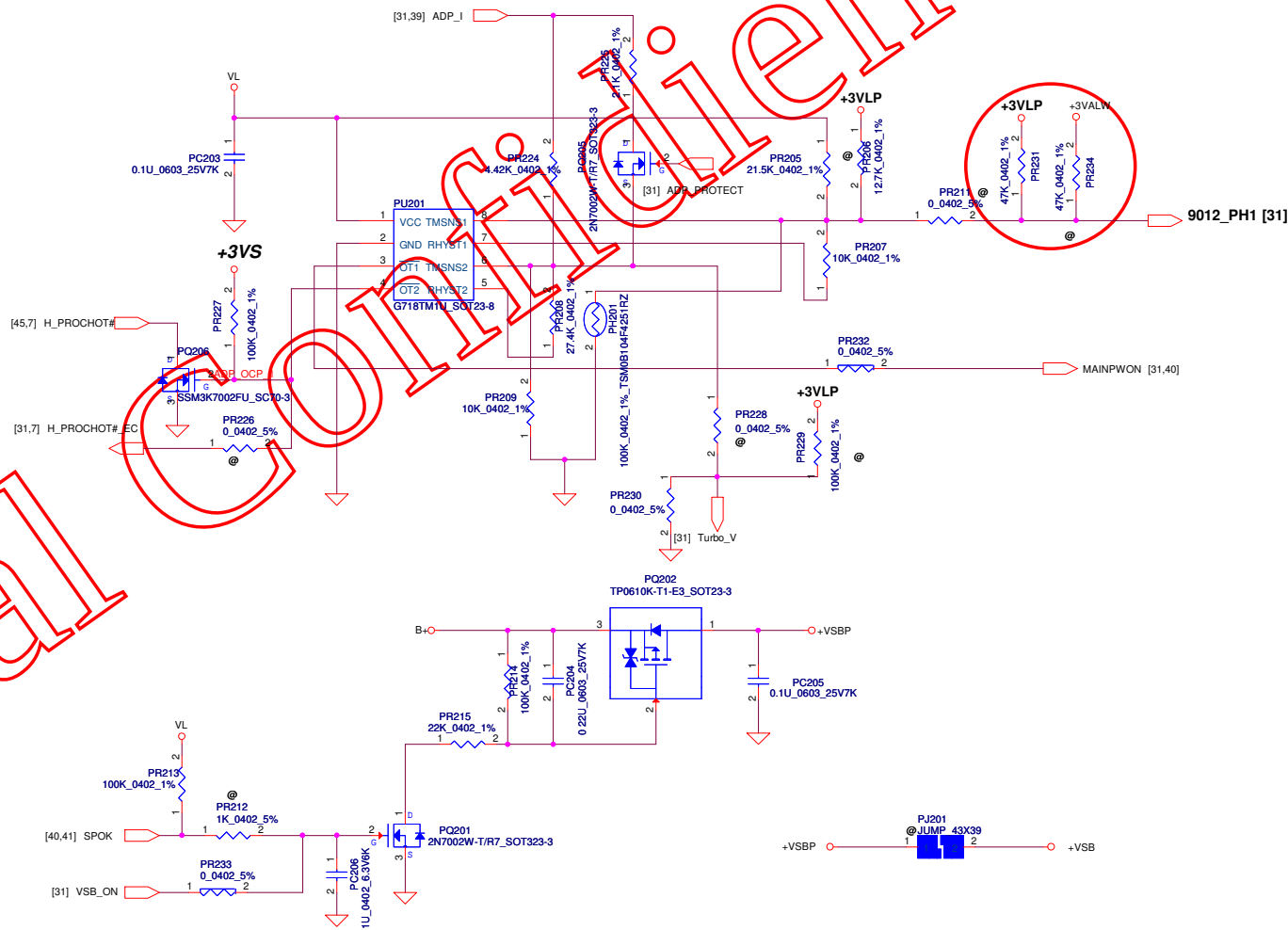
ADP_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98

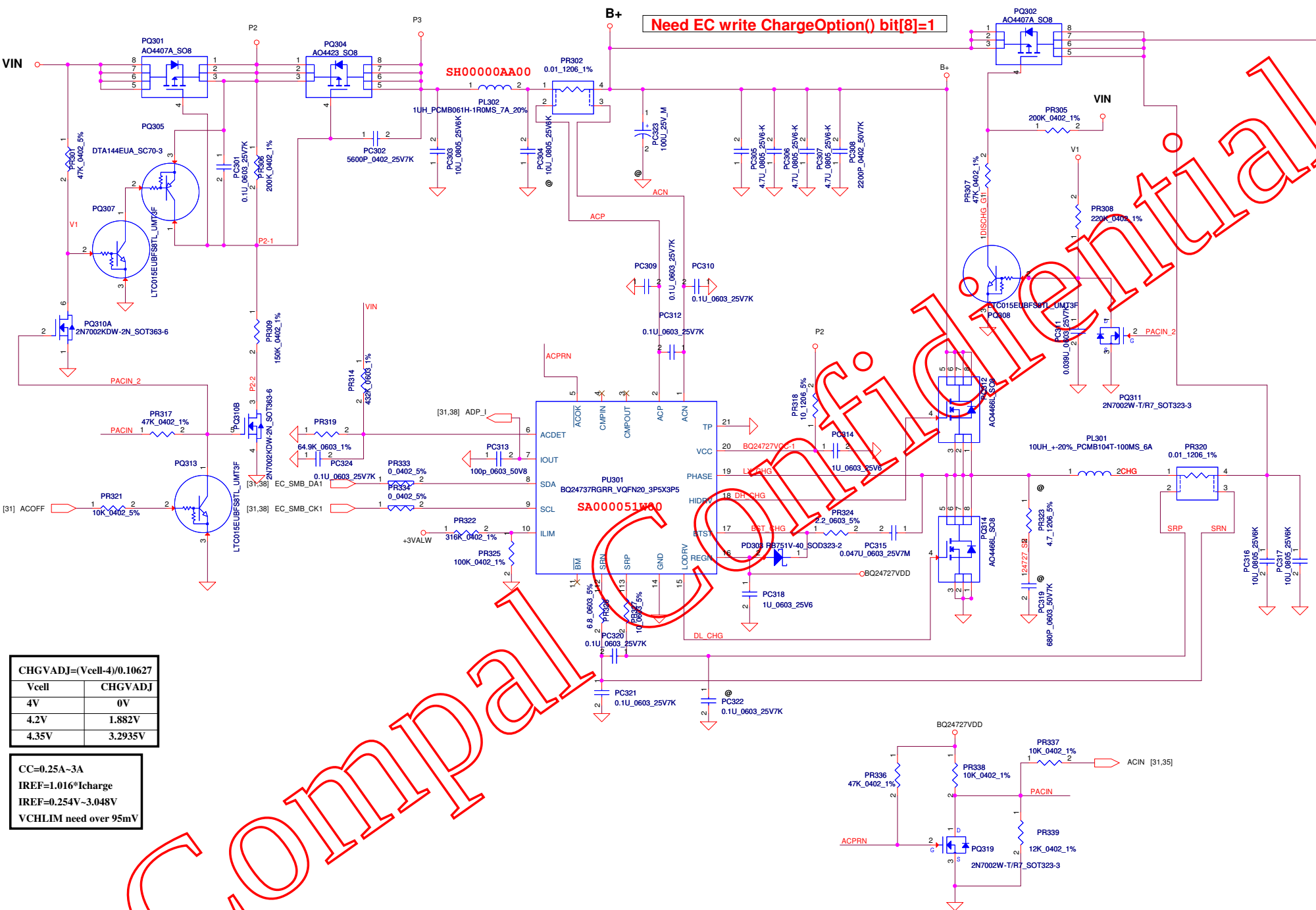




For KB930 --> Keep PU201 circuit
($V_{th} = 1.25V$)



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				Customer		1.0
				Date:	Tuesday, March 12, 2013	Sheet 38 of 51

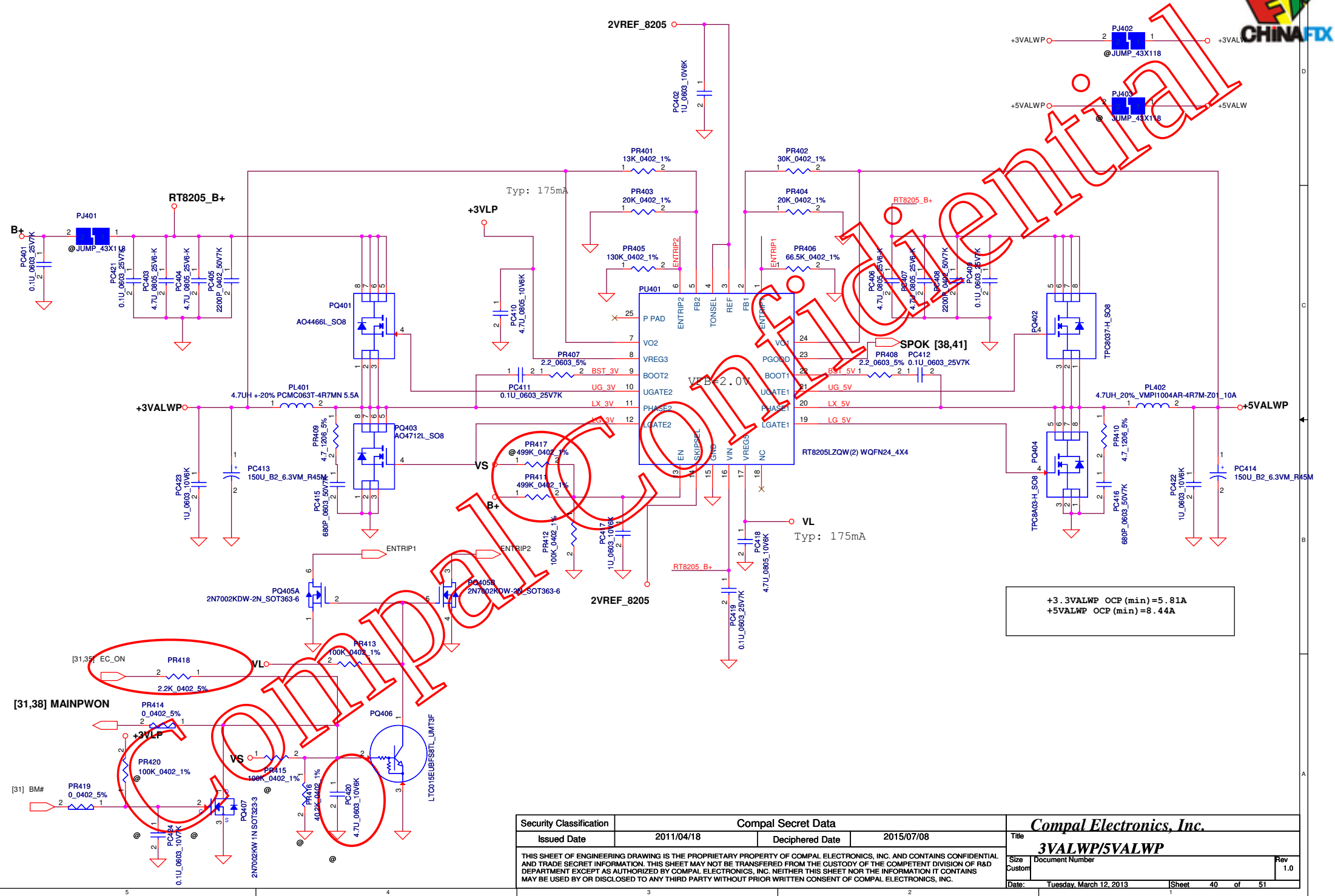


CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

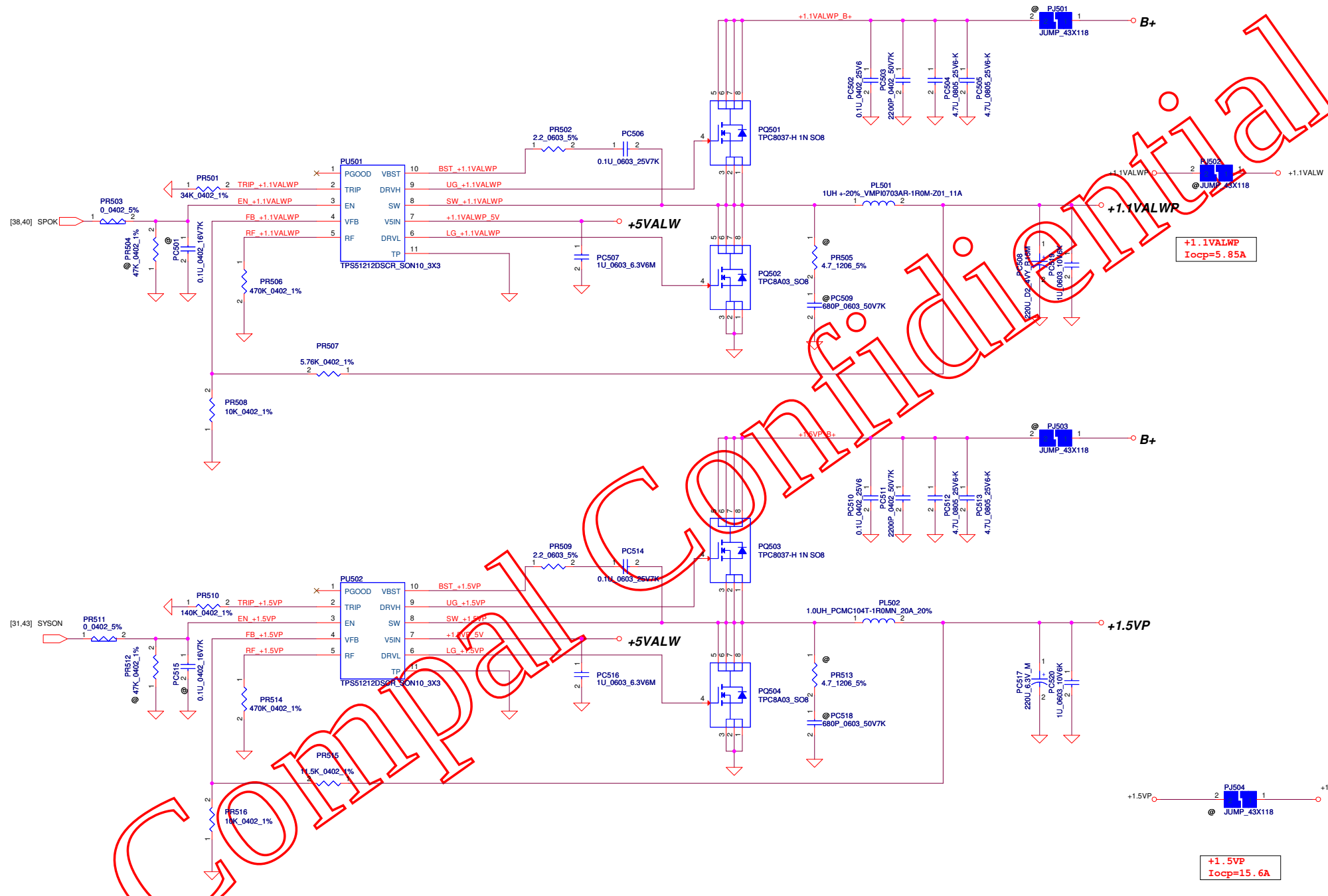
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				Date	Rev
				Tuesday, March 12, 2013	1.0
				Sheet	39 of 51

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



+3.3VALWP OCP (min)=5.81A
 +5VALWP OCP (min)=8.44A

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Date: Tuesday, March 12, 2013		Sheet 40		of 51	

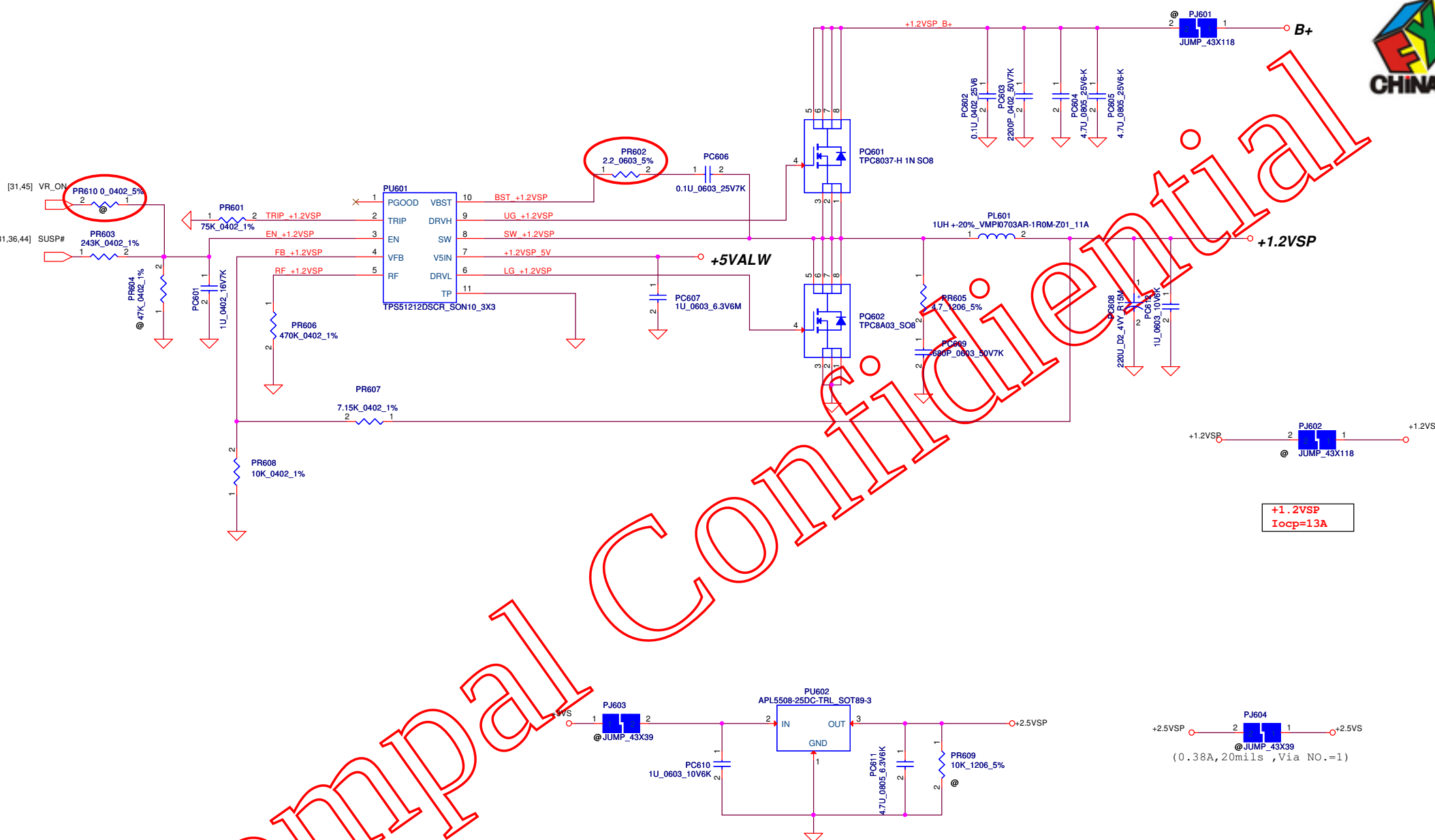


+1.1VALWP
I_ocp=5.85A

+1.5VP
I_ocp=15.6A

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				7407	1.0
Date: Tuesday, March 12, 2013				Sheet	41 of 51

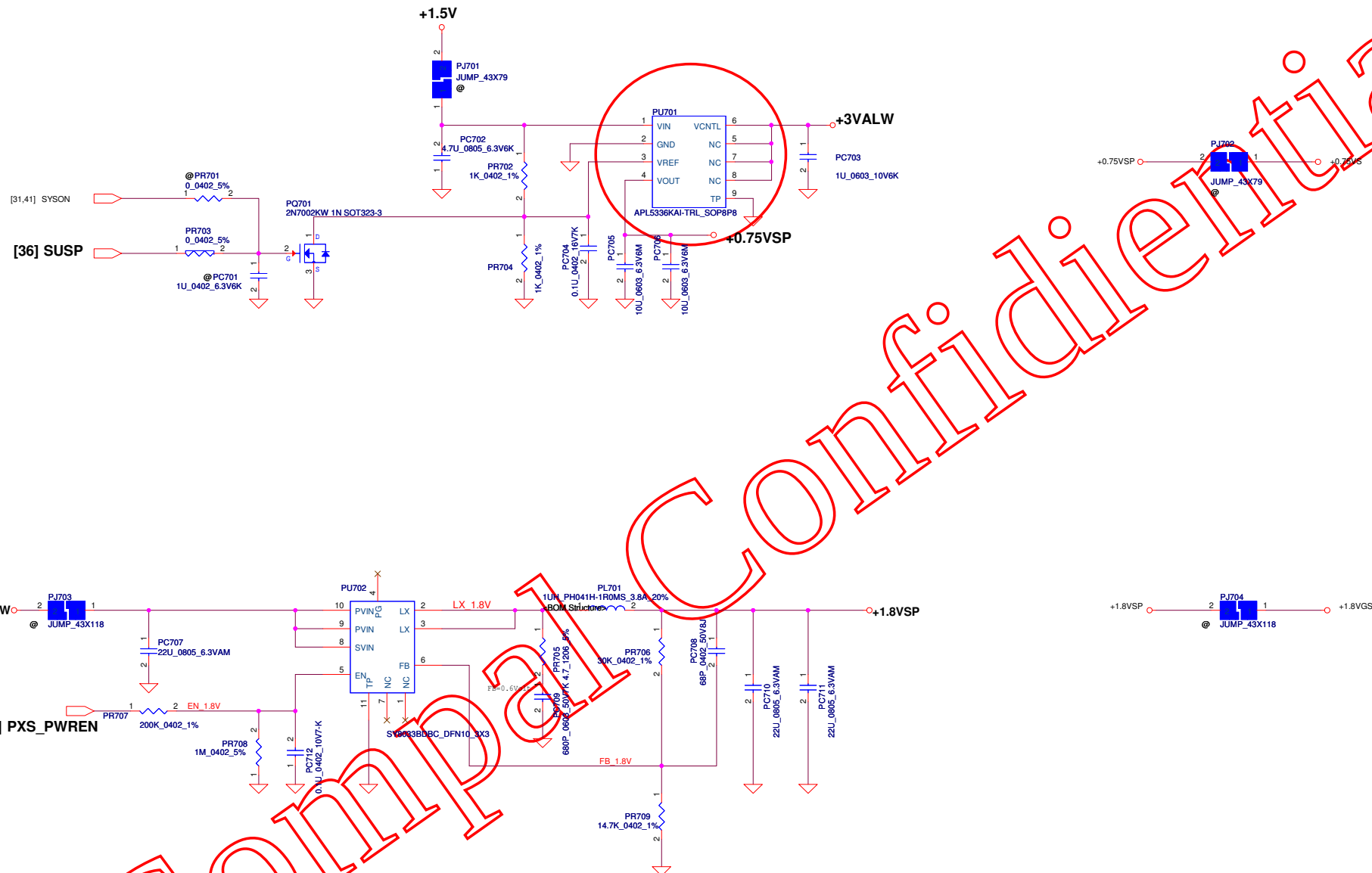
+1.1VALWP/+1.5VP



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						Size		Document Number		Rev
										1.0
Date:		Tuesday, March 12, 2013		Sheet		42 of 51				

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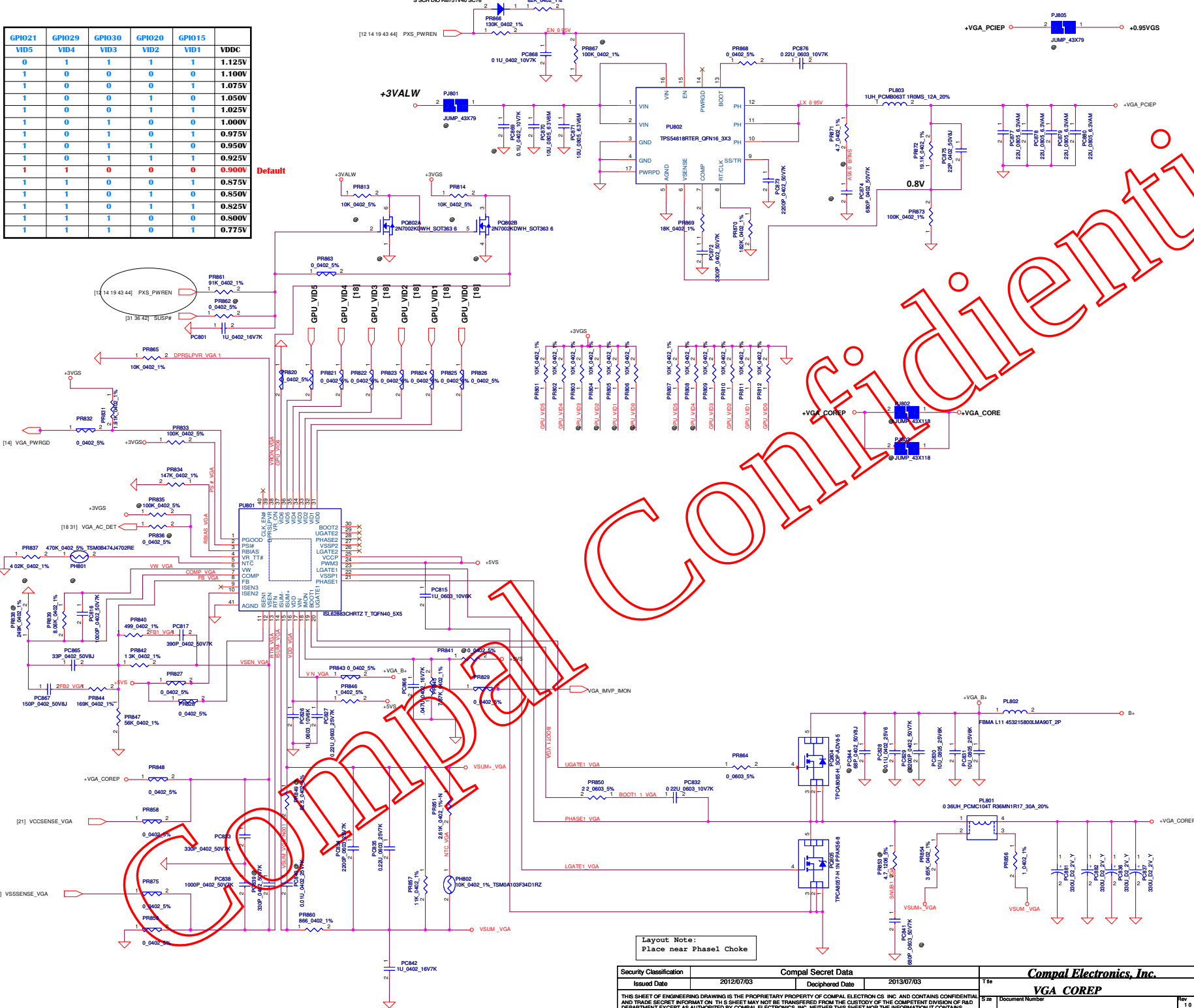
+1.2VSP/+2.5VSP



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				Date	Tuesday, March 12, 2013
				Sheet	43 of 51

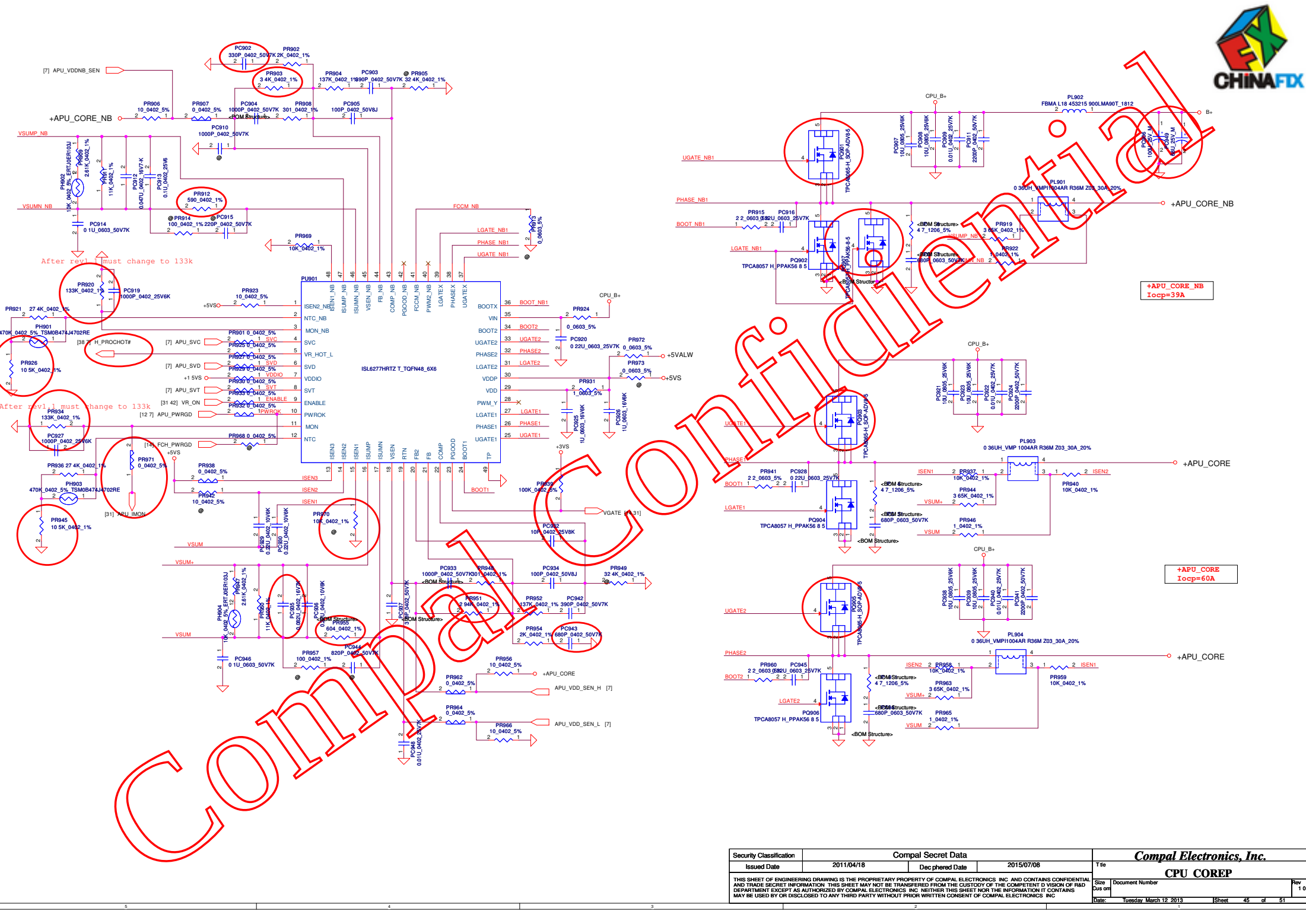
GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

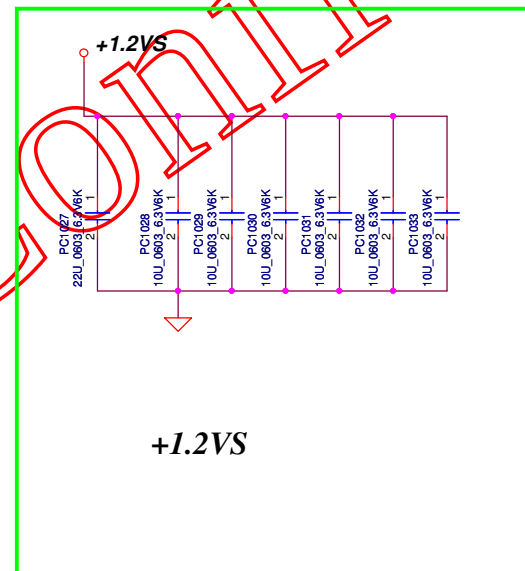
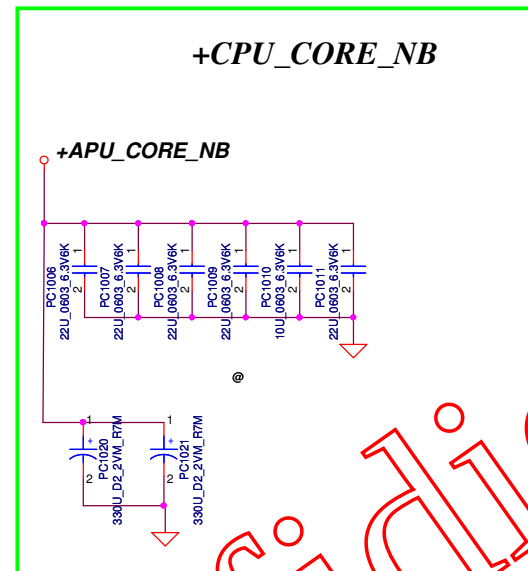
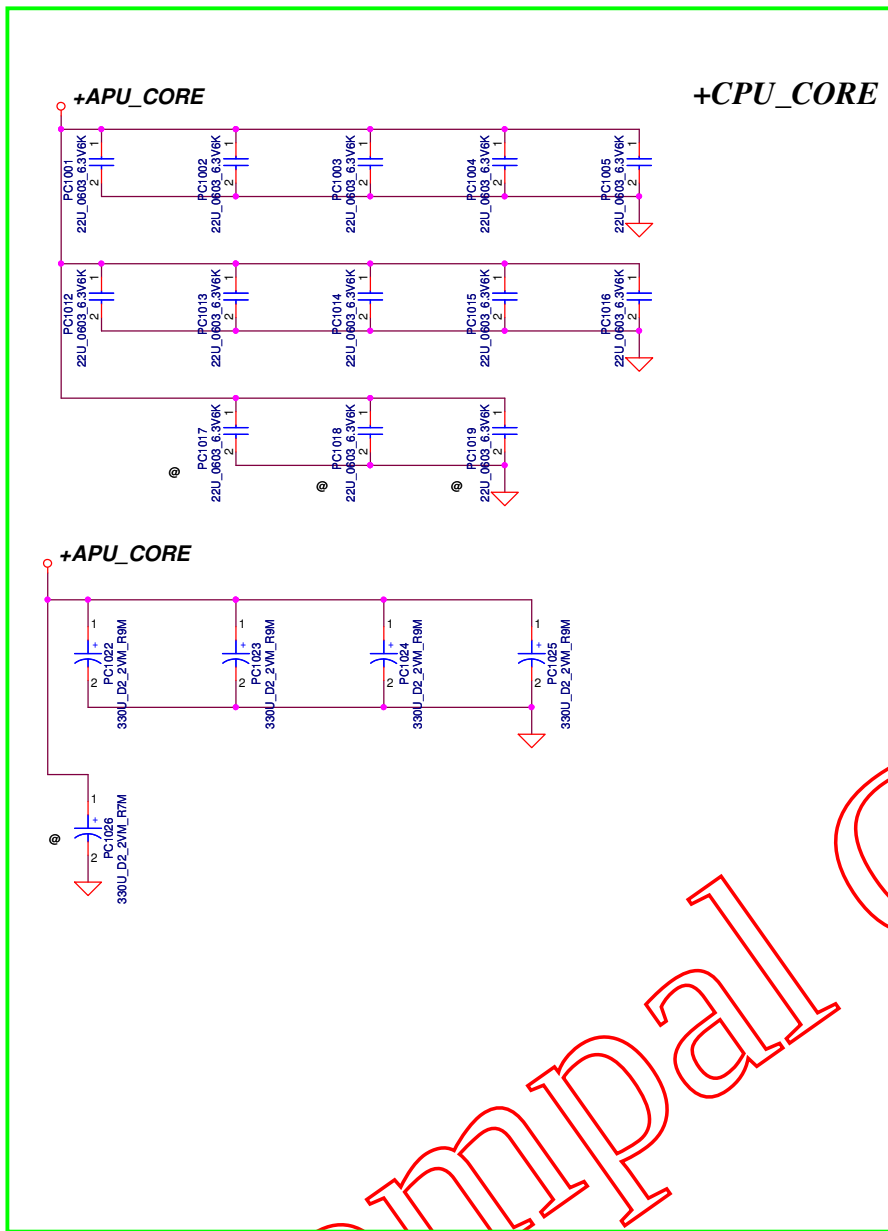


Layout Note:
Place near Phasel Choke

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Date: Tuesday, March 12, 2013 Sheet: 44 of 51					



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				A3	1.0
				Date:	Rev
				Tuesday, March 12, 2013	1.0
				Sheet	46 of 51

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107, PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR105, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	Remove PQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
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				C38-G series Chief River Schematic	
Date: Tuesday, March 12, 2013		Sheet 47 of 51		Rev 1.0	



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Phase	Date	No.	BOM	Sch	Layout	Description
SDV/FVT	2012/11/22	No.1	V	V	V	Page 5, Delete for Sun Pro M2 C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32 Delete PCIE_CRX_GTX_P8~15 PCIE_CTX_C_GRX_P8~15 PCIE_CTX_GRX_P8~15 PCIE_CRX_GTX_N8~15 PCIE_CTX_C_GRX_N8~15 PCIE_CTX_GRX_N8~15
SDV/FVT	2012/11/22	No.2	V	V	V	Page 17, Delete for Sun Pro M2 C1400,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431 Delet PCIE_CRX_C_GTX_P8~15 PCIE_CRX_C_GTX_N8~15
SDV/FVT	2012/11/22	No.3	V	V	V	Page 17 ,U1401 change Part Number from SA000047H50 to SA00006BA30 for Sun Pro M2
SDV/FVT	2012/11/22	No.4	V	V	V	Page 24, Delete for Sun Pro M2 no Channel B C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,R1462,R1463 C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,R1464,R1465 C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1569 C1666,C1667,R1504,R1504,R1505,R1505,R1506,R1507,R1508,R1509,R1510,R1510,R1511,R1511,R1512,C1570 R1513,R1514,R1515,R1516,R1517,R1518,R1519,R1520,R1521,R1522,R1523,R1524,R1525,R1526,R1527,U1409,U1410,U1411,U1412
SDV/FVT	2012/11/22	No.5		V	V	Page 19, Reserved T1406,T1407 for Sun Pro M2
SDV/FVT	2012/11/22	No.6	V	V	V	Page 18, Reserved D1401 for Sun Pro M2 PX5.5
SDV/FVT	2012/11/22	No.7	V	V	V	Page 19, Delete PX4.0 and PX5.0 schematic C1459,C1460,C1461,C1462,C1463,D1400,Q1401,Q1402,Q1403A,Q1403B,Q1404,Q1405,Q1406,R1401,R1438,R1439,,R1440, R1442,R1460,R1461,U1402,U1403
SDV/FVT	2012/11/22	No.8	V	V	V	Page 20, Delete DGPU Display Power not need reserved C1472,C1473,C1474,C1475,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1487,C1488
SDV/FVT	2012/11/22	No.9	V	V	V	Page 20, L1405 change Part Number from SM010009U00 to SM01000AX00 for Sun Pro M2 Spec Suggetion 120 to 220 ohm
SDV/FVT	2012/11/22	No.10	V	V	V	Page 20, Delete R1457,R1458 ,Because the Sun Pro M2 AW28,AW18 are NC.
SDV/FVT	2012/11/22	No.11	V	V	V	Page 20, Delete Thames&Seymour reserved R1407,R1408,R1409,R1410,R1411,R1412,R1413,R1414,R1415,R1416,R1417,R1466,R1467,R1468,R1469,R1471
SDV/FVT	2013/1/10	No.12	V	V	V	Page 12 U2 change Part Number from SA000066K10 to SA000066K60
SDV/FVT	2013/1/10	No.13		V	V	Page 31, for Power Eulot 6 modfiy Delete net FSTCHG,BATT_LEN#
SDV/FVT	2013/1/11	No.14	V	V	V	Page 18, for fine tune VGA Power saving Stuff C1441
SDV/FVT	2013/1/11	No.15	V	V	V	Page 19, for fine tune VGA Power Sequence R1445 change value from 20K to 470K R1446 change value from 20K to 10K

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				Date: Tuesday, March 12, 2013	Rev 1.0
				Sheet 48	of 51



Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2013/1/10	No.1	v	v	v	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	v	v	v	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	v	v	v	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	v	v	v	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		v	v	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		v	v	Page 32, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	v	v	v	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	v	v	v	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

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		Size	Document Number	Rev	
		Customer	LA-8126P	1.0	
		Date:	Tuesday, March 12, 2013	Sheet	49 of 51



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				Custom	LA-8126P
				Date	Tuesday, March 12, 2013
				Sheet	50 of 51
				Rev	1.0

Phase	Date	No.	BOM	Sch	Layout	Description
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				Custom	LA-8126P
				Date	Tuesday, March 12, 2013
				Sheet	51 of 51
				Rev	1.0