

LCFC Confidential

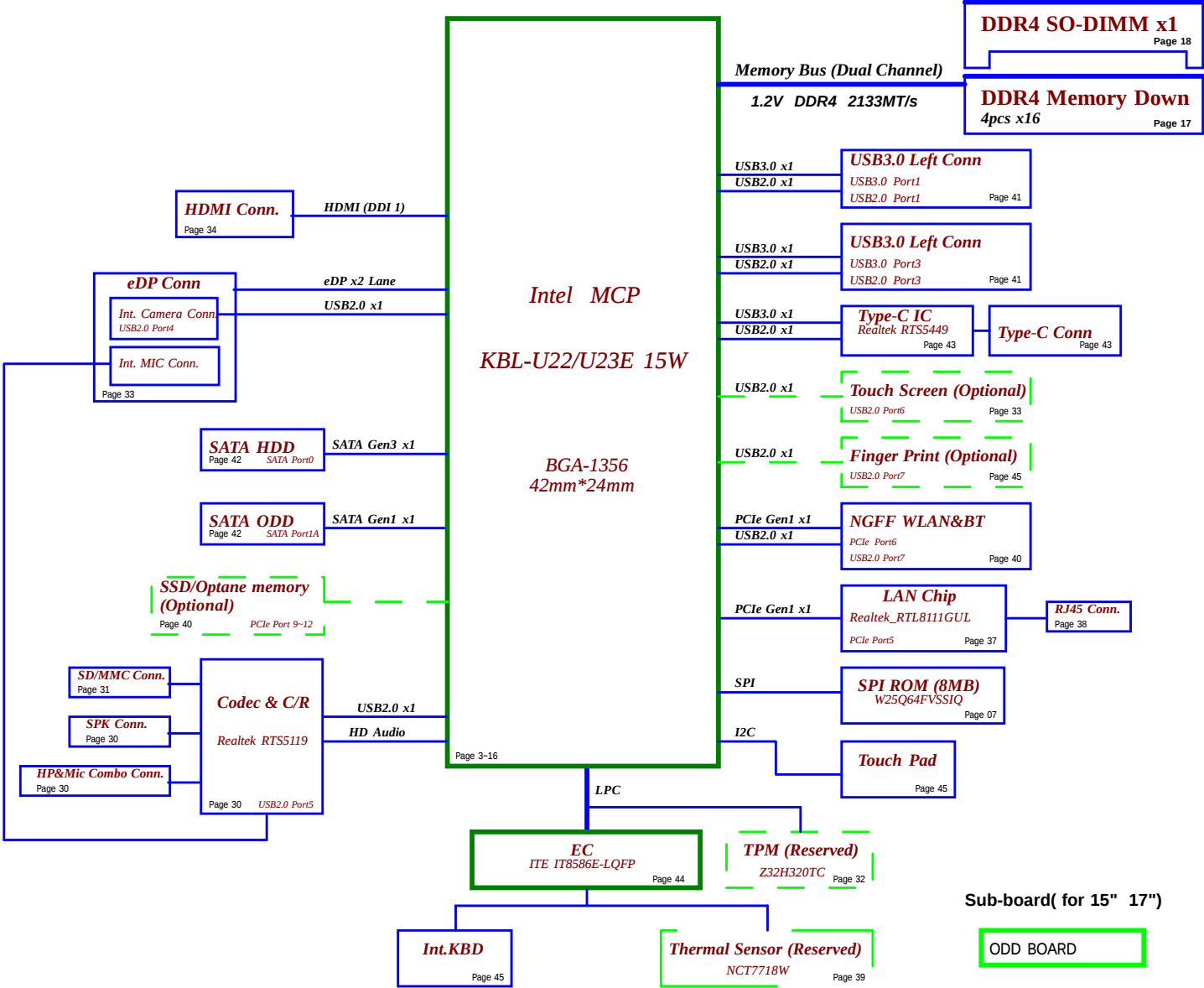
DG421/DG521/DG721 MB Schematics Document

Kabylake-U22/U23E with DDR4

2017-01-19

REV:1.0

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page			
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4 AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1~4 X4 PCIE
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9~12 X4 PCIE
	Optane Memory
	0 HDD
SATA	1A ODD
	1B used as PCIE
	2 used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EX0@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

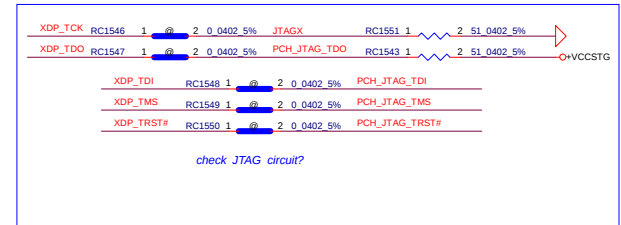
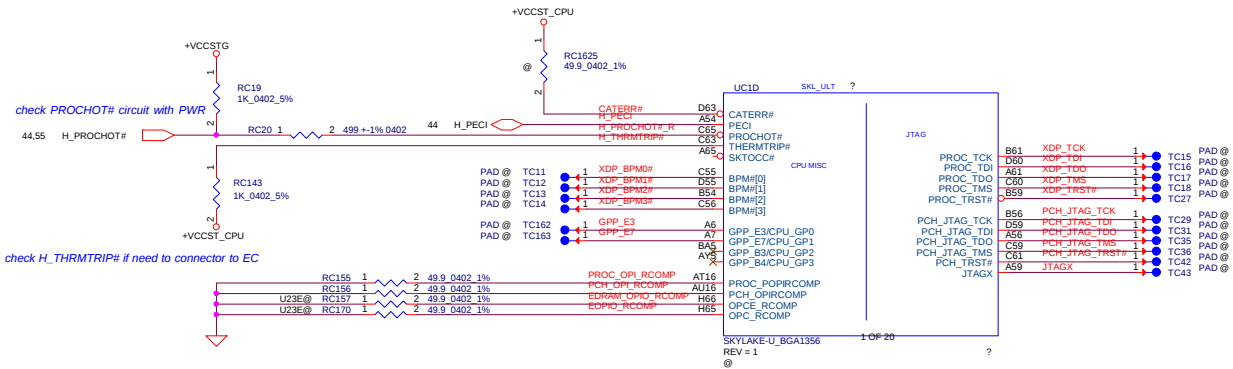
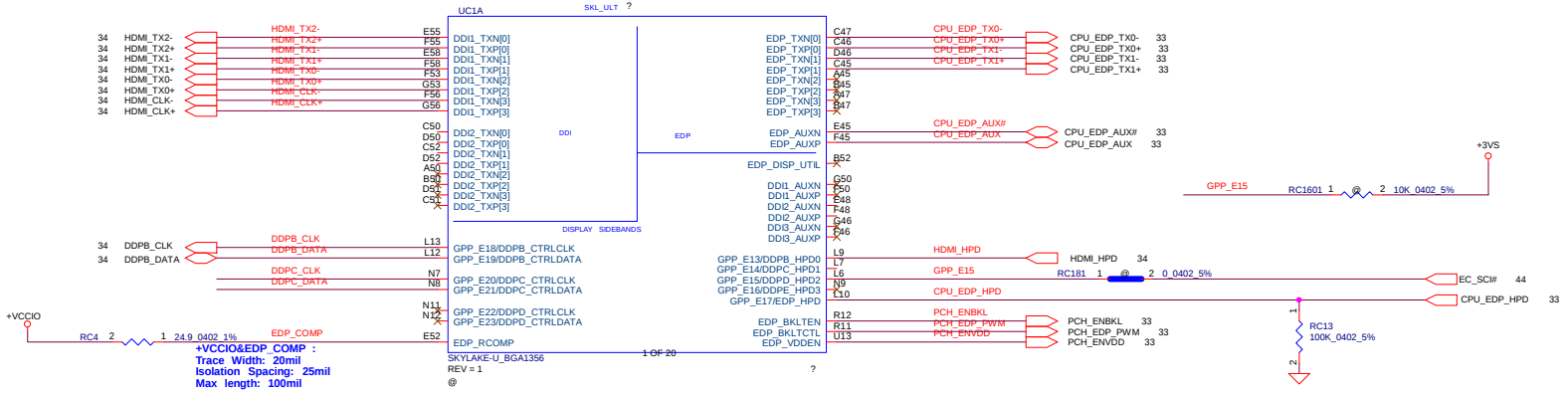
PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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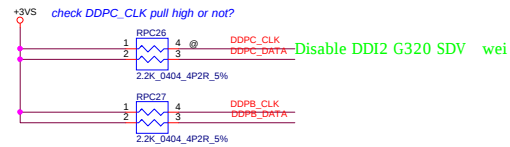


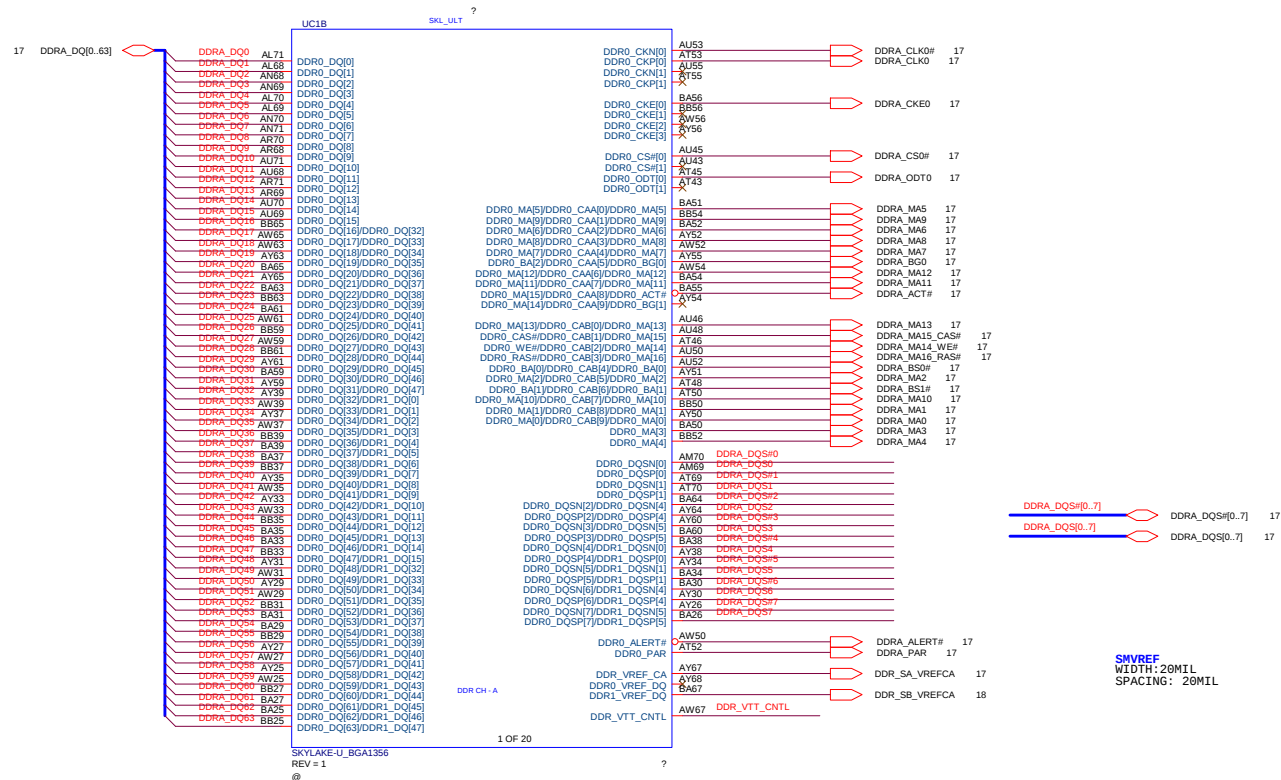
HDMI D2
HDMI D1
HDMI D0
HDMI CLK



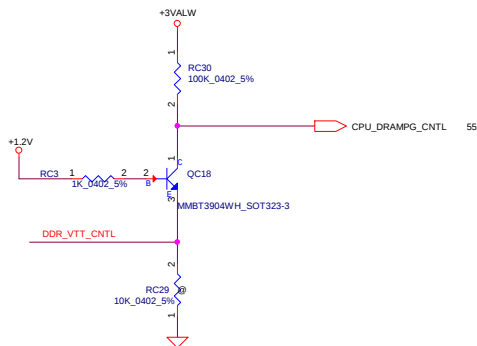
DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

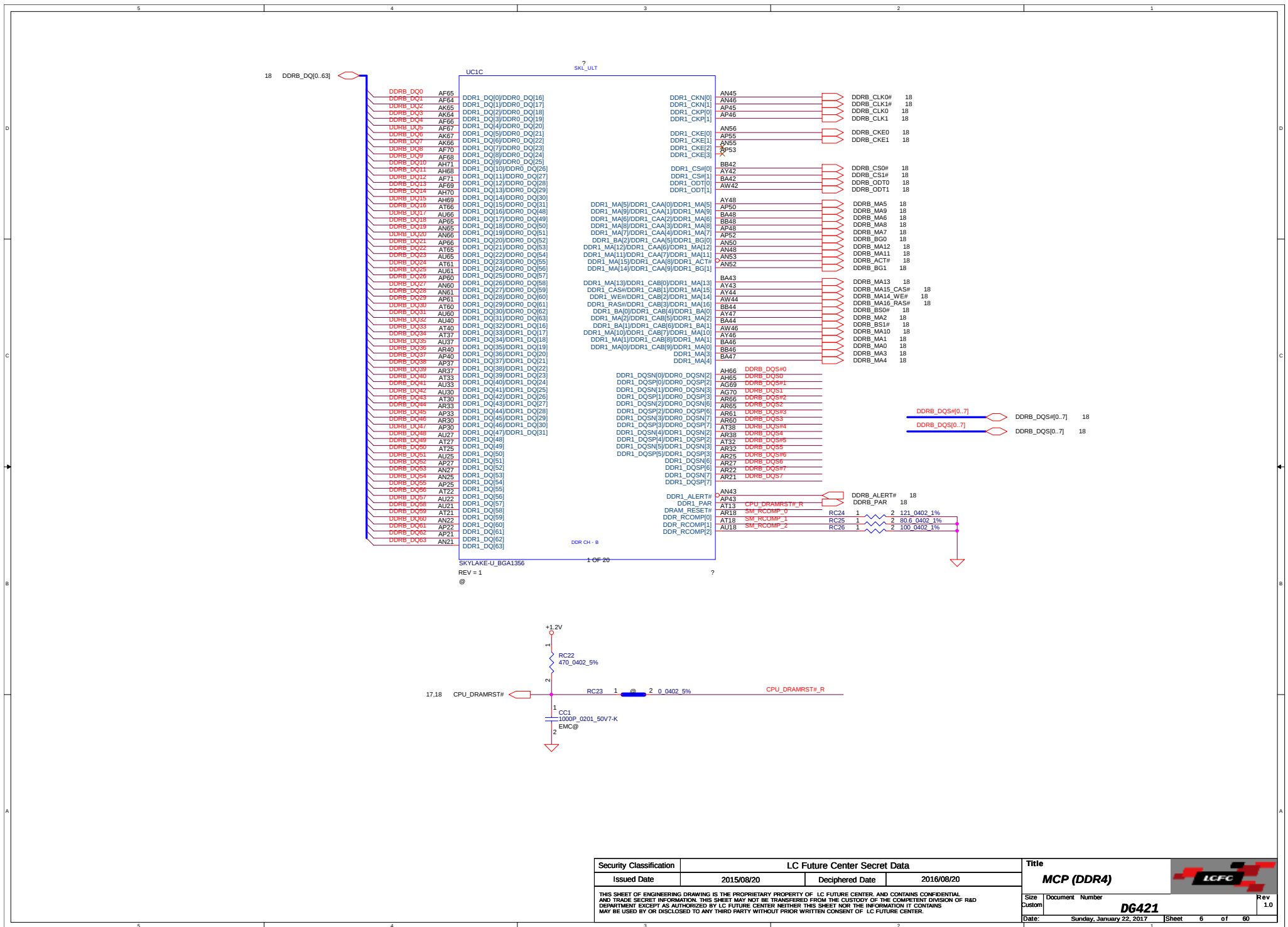


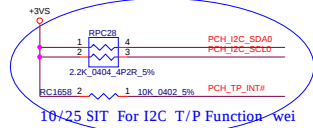


SKYLAKE-U, BGA1356
REV = 1
@

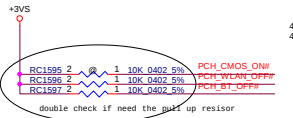


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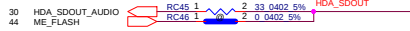
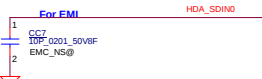
10/25 SIT For I2C T/P Function-wei



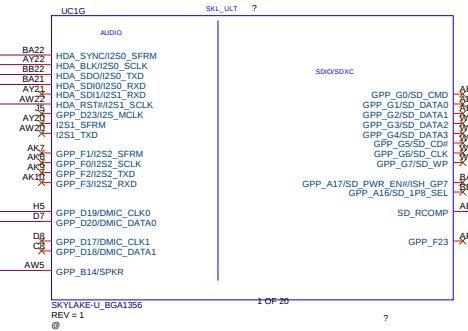
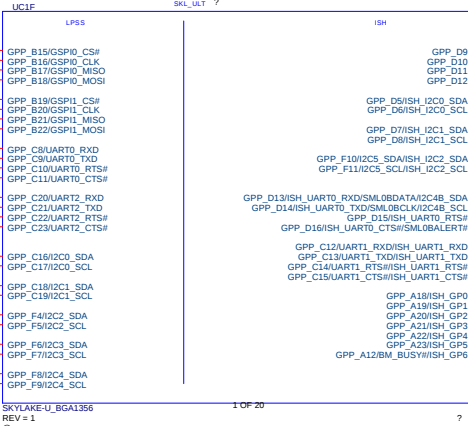
double check if need the pull up resistor



HDA SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

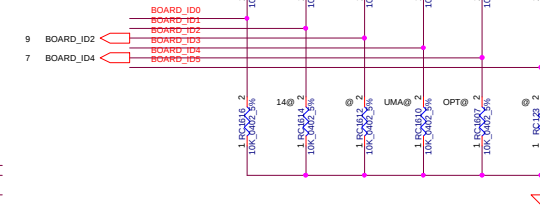


Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) * 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PwROK
GPIO8_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) * 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PwROK
GPIO11_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) * 1 = LPC	0	Rising edge of PCH_PwROK

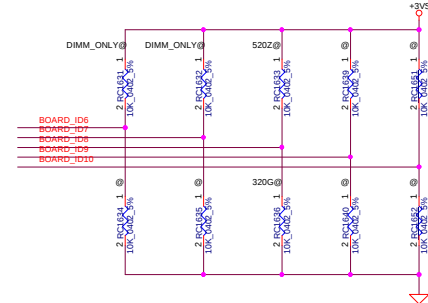


@UMA SKU

RC1558 1 10K 0402 5% DGPU_PwROK

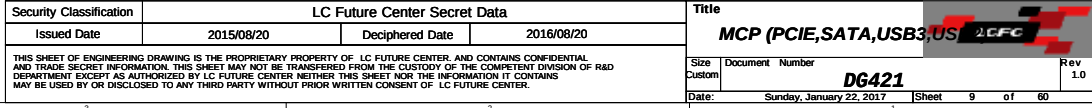


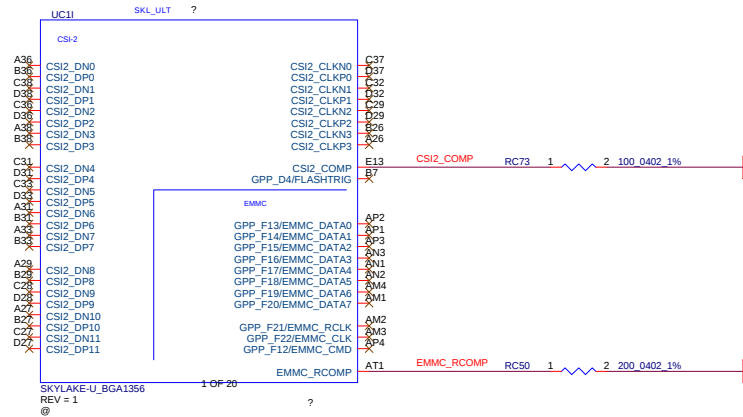
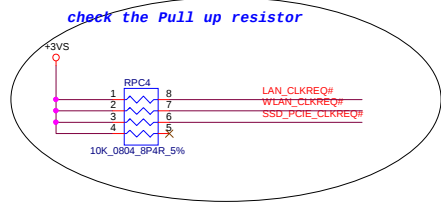
Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	RC1615 RC1613
Board_ID2	0 Reserved	RC1612
	1 Reserved	RC1611
Board_ID3	0 UMA	RC1619
	1 DIS	RC1609
Board_ID4	0 NV GPU	RC1607
	1 AMD GPU	RC1608
Board_ID5	0 Reserved	RC123
	1 Reserved	RC1606



Board ID	Description	Stuff R
Board_ID [6,7]	00 Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01 Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10 Micron 8Gb 2400 MT/s	RC1631 RC1635
	11 SO-DIMM Only	RC1631 RC1632
Board_ID8	0 3206	RC1636
	1 5202	RC1633
Board_ID9	0 Reserved	RC1640
	1 Reserved	RC1639
Board_ID10	0 Reserved	RC1652
	1 Reserved	RC1651

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Optane memory

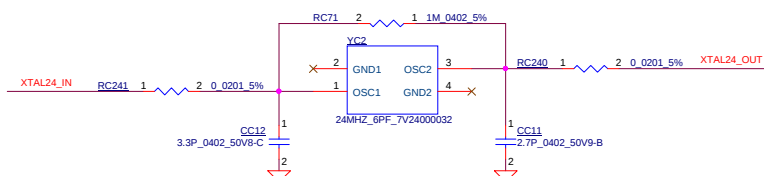
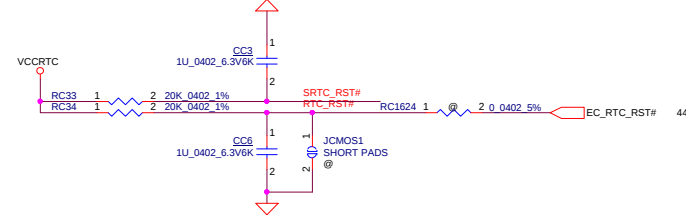
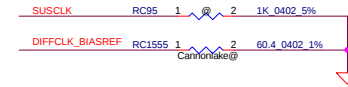
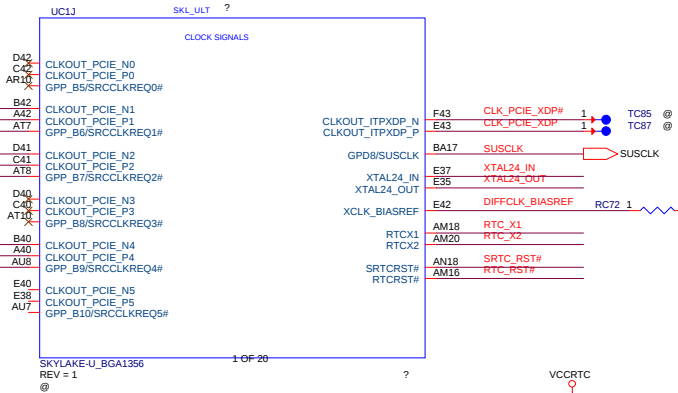
PCIE CLK5 WLAN

PCIE CLK4 LAN

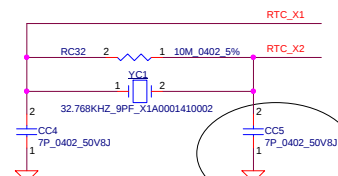
40 CLK_PCIE_SSD#
40 CLK_PCIE_SSD
40 SSD_PCIE_CLKREQ#

40 CLK_PCIE_WLAN#
40 CLK_PCIE_WLAN
40 WLAN_CLKREQ#

37 CLK_PCIE_LAN#
37 CLK_PCIE_LAN
37 LAN_CLKREQ#

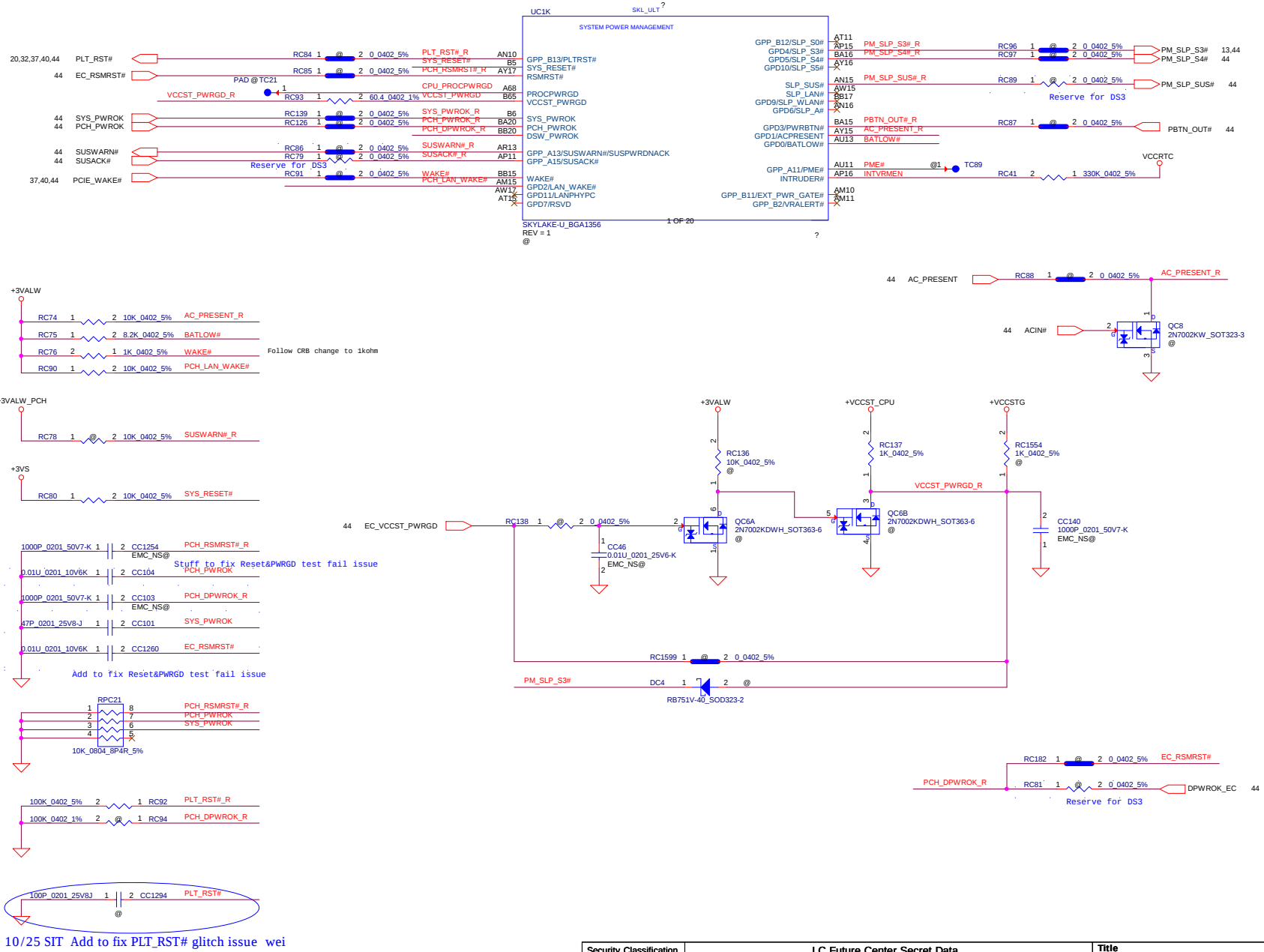


need to use 38.4MHz (30ohm) for Cannonlake-u



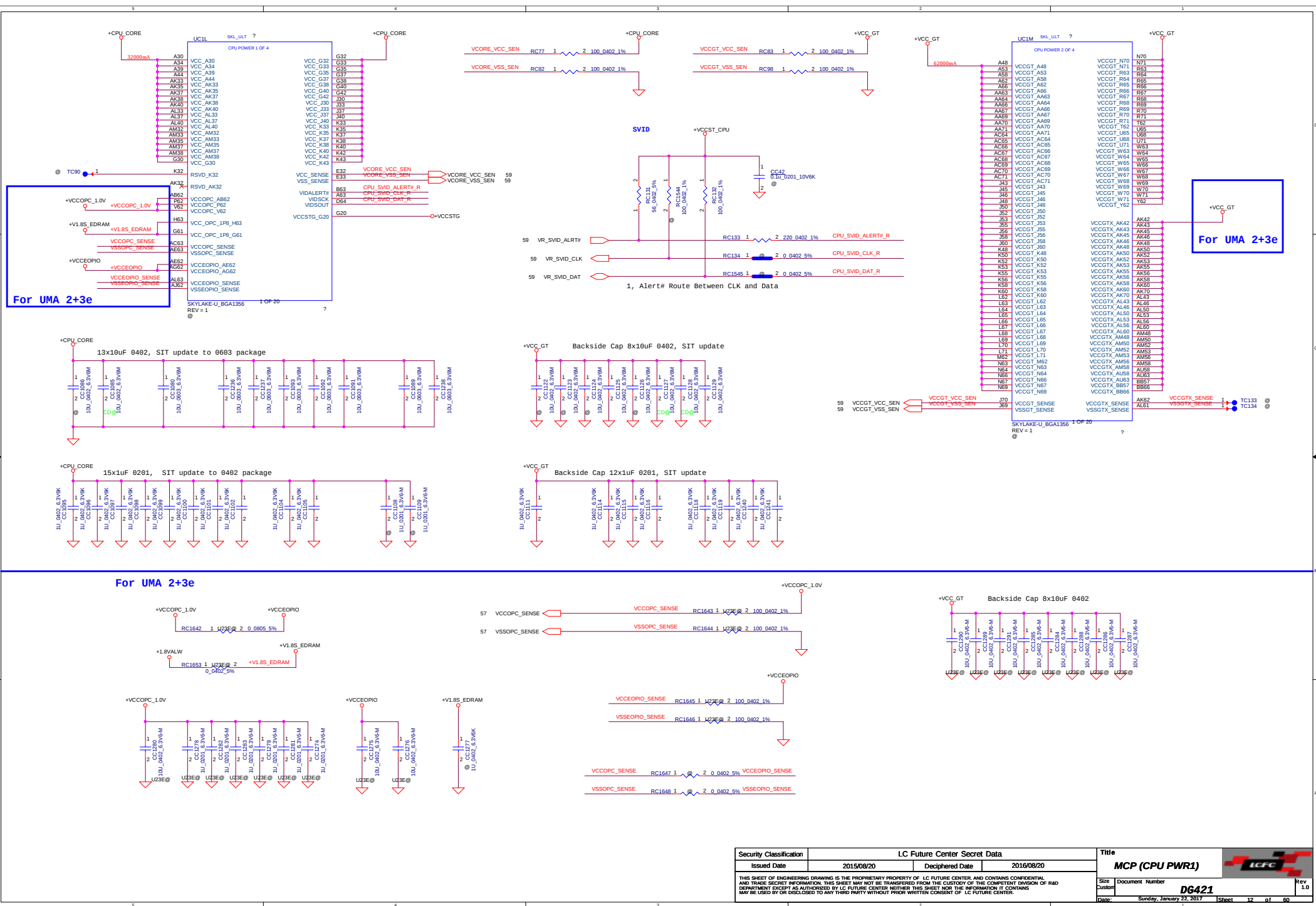
when single end external clock generator used, this pin should be grounded

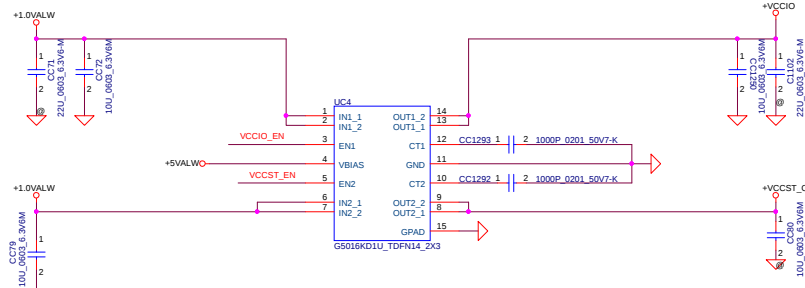
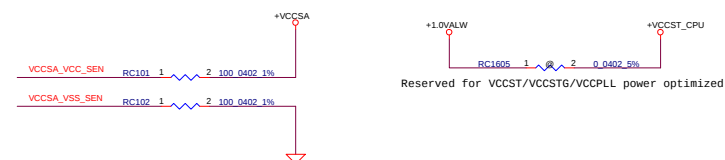
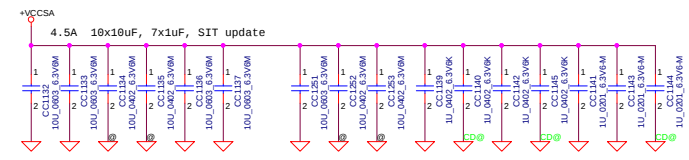
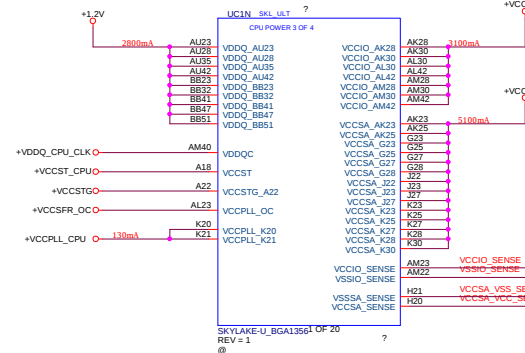
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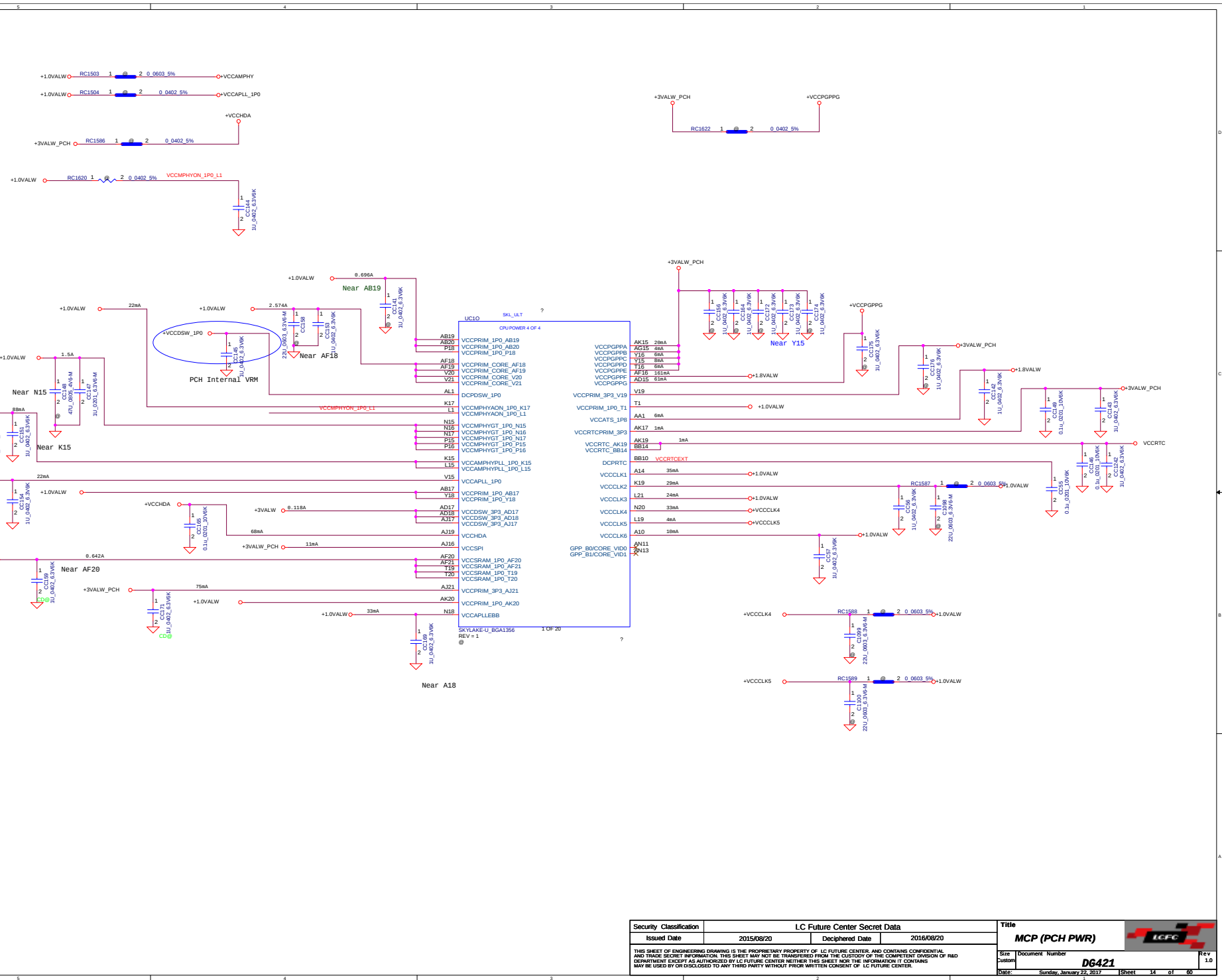
10/25 SIT Add to fix PLT_RST# glitch issue wei

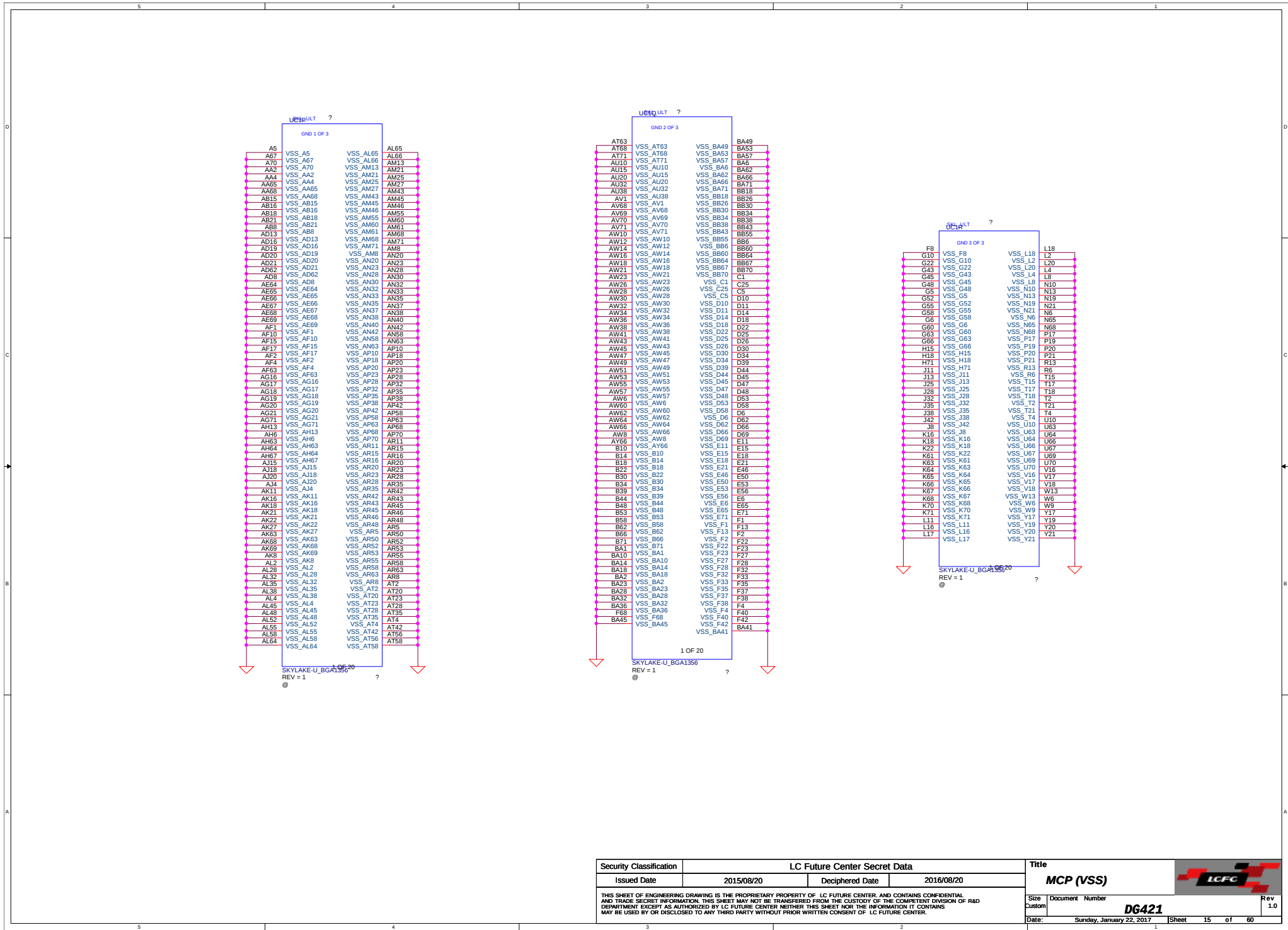
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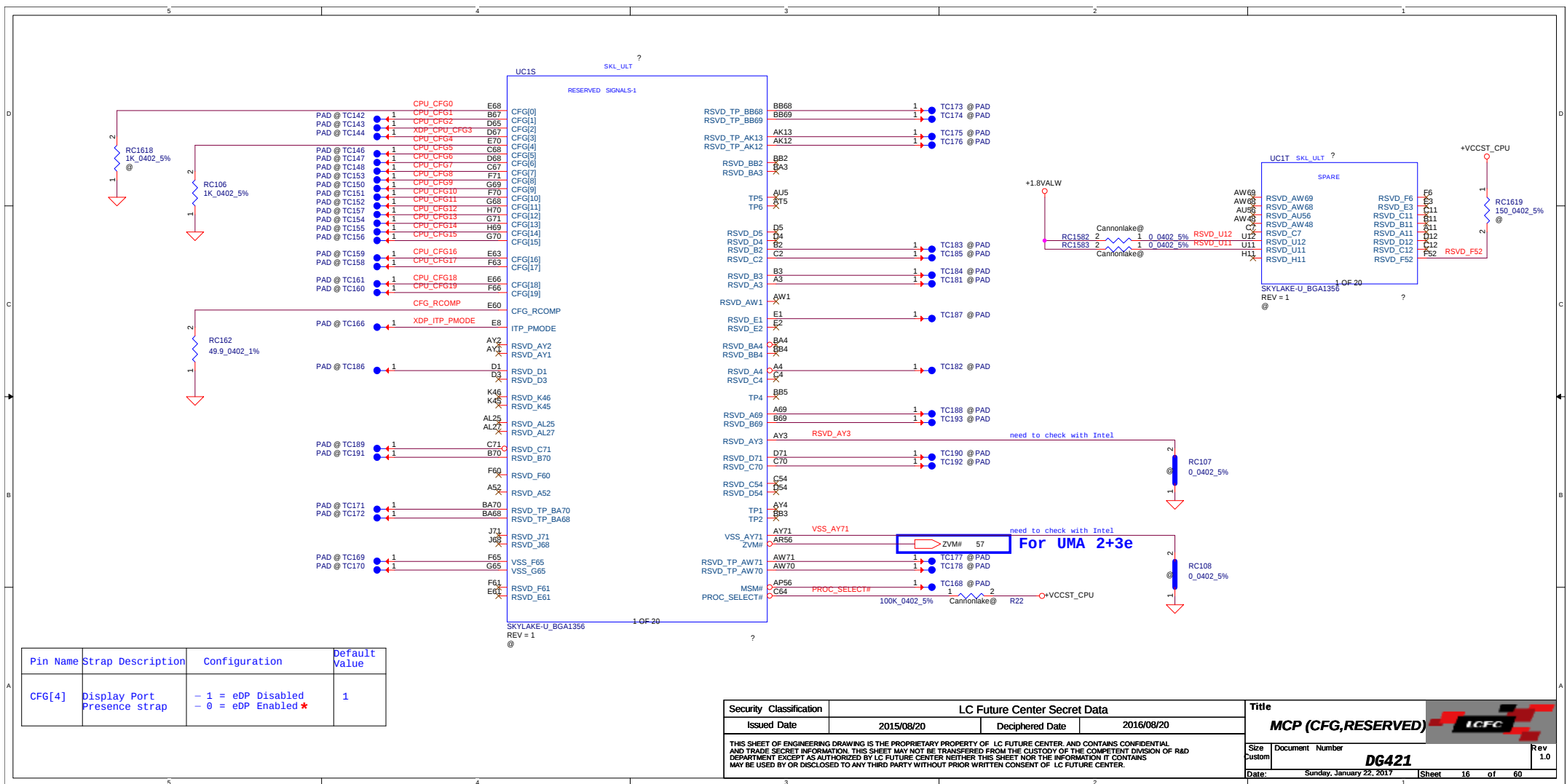


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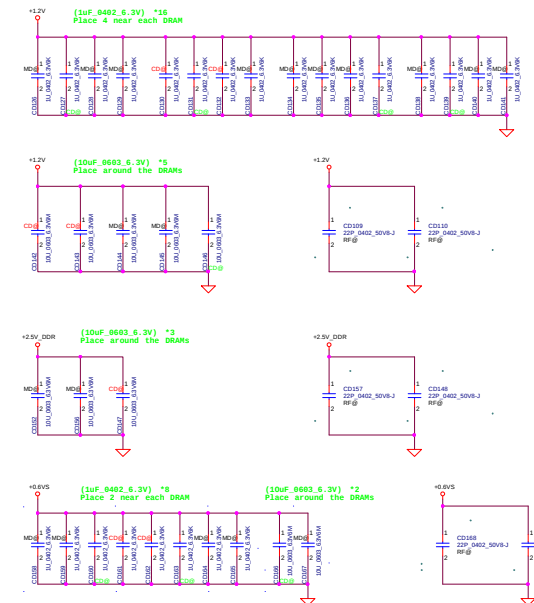


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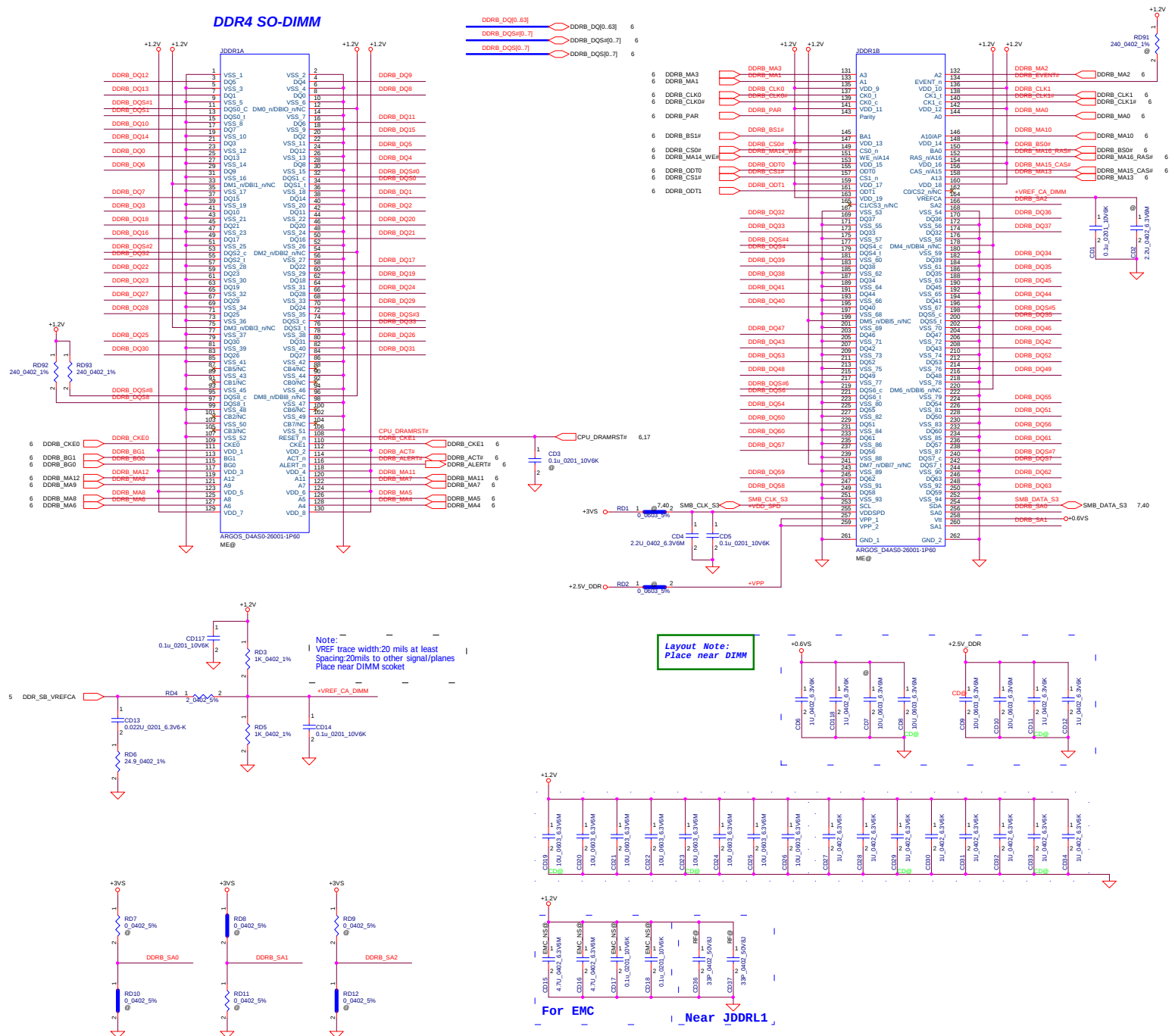


Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled*	1

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DDR4 SO-DIMM



SPD Address = 2H

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Date:				Sunday, January 22, 2017	Sheet 21 of 60	

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2015/08/20		Deciphered Date		2016/08/20		Blank			
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Size		Document Number		D6421		Date		Sunday, January 22, 2017		Sheet 22 of 60	

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2015/08/20		Deciphered Date		2016/08/20		Blank			
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Security Classification		LC Future Center Secret Data				Title							
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										DG421			
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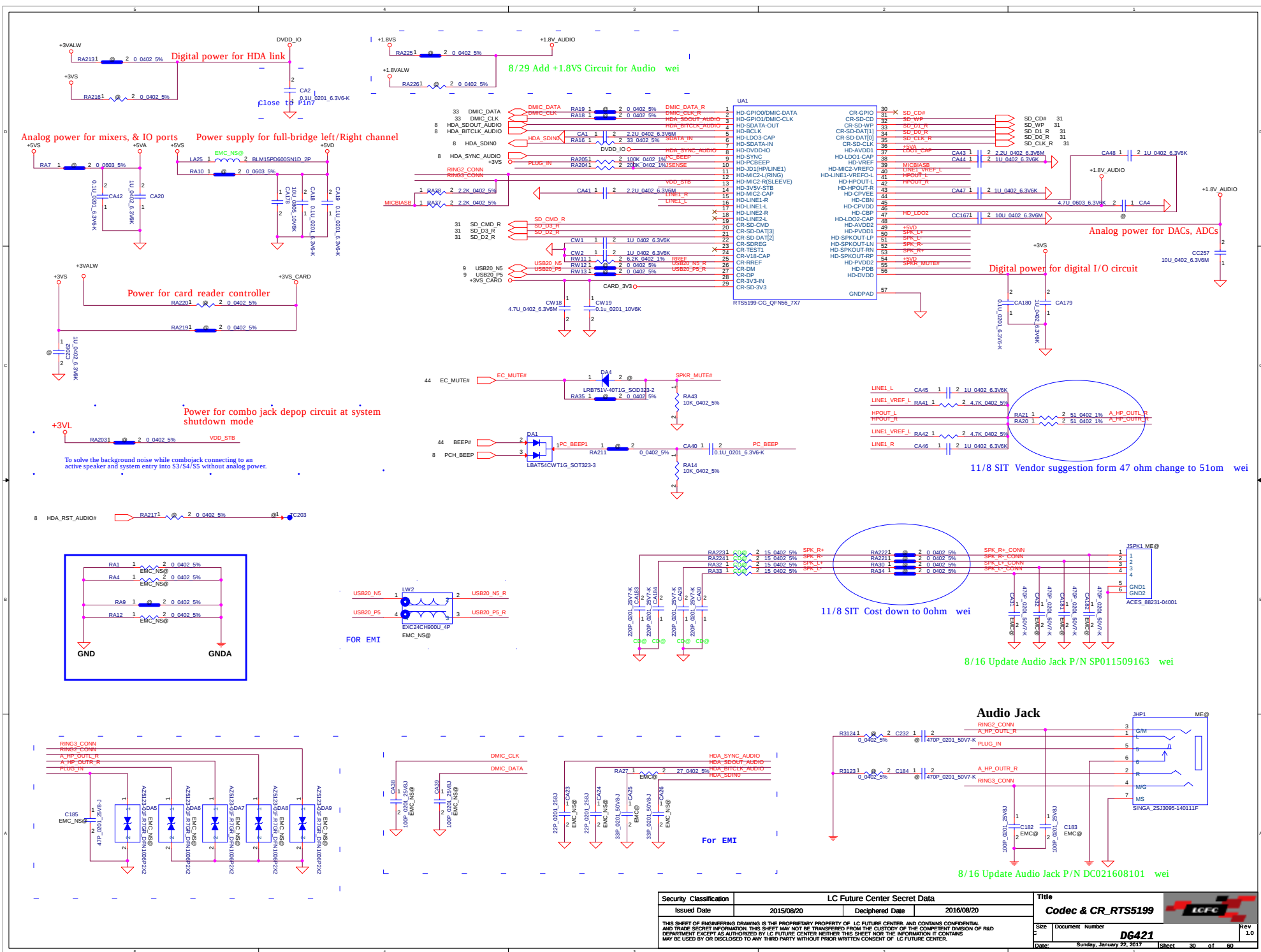
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Size		C		Document Number		D6421		Rev 1.0		
Date:		Sunday, January 22, 2017		Sheet		25 of 60				

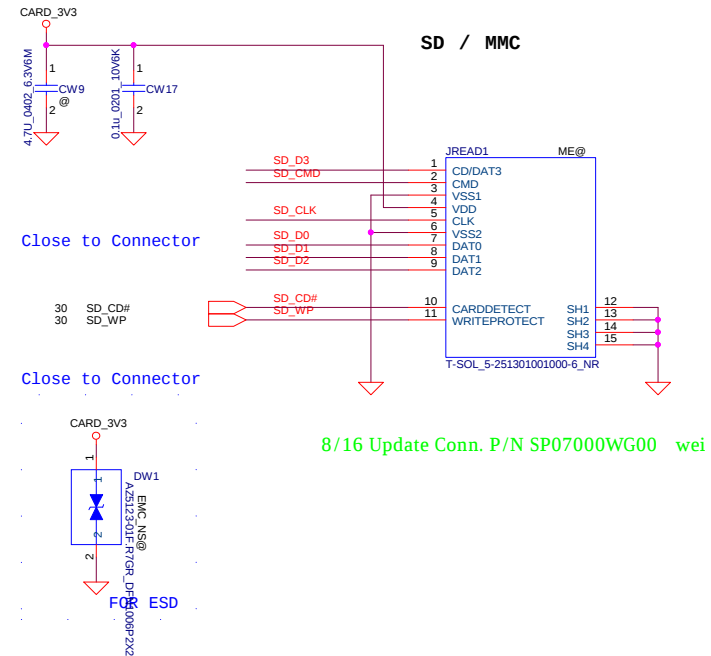
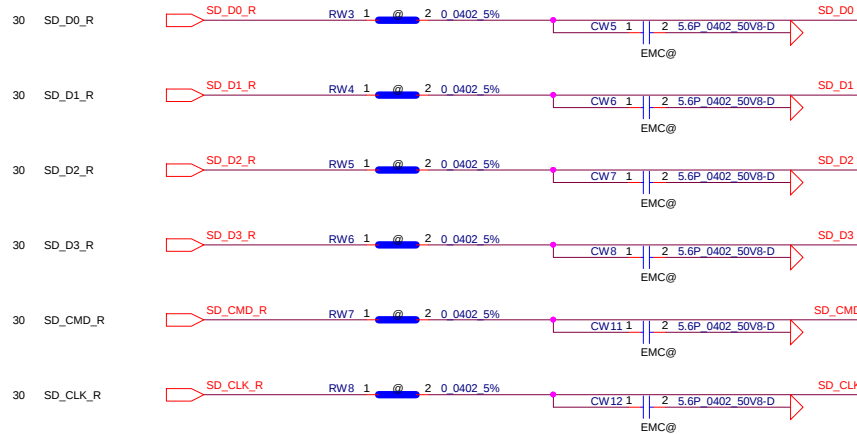
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								D6421			
Date:								Sunday, January 22, 2017		Sheet 26 of 60	

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Size		Document Number		D6421		Rev 1.0	
Date:		Sunday, January 22, 2017		Sheet 27 of 60			

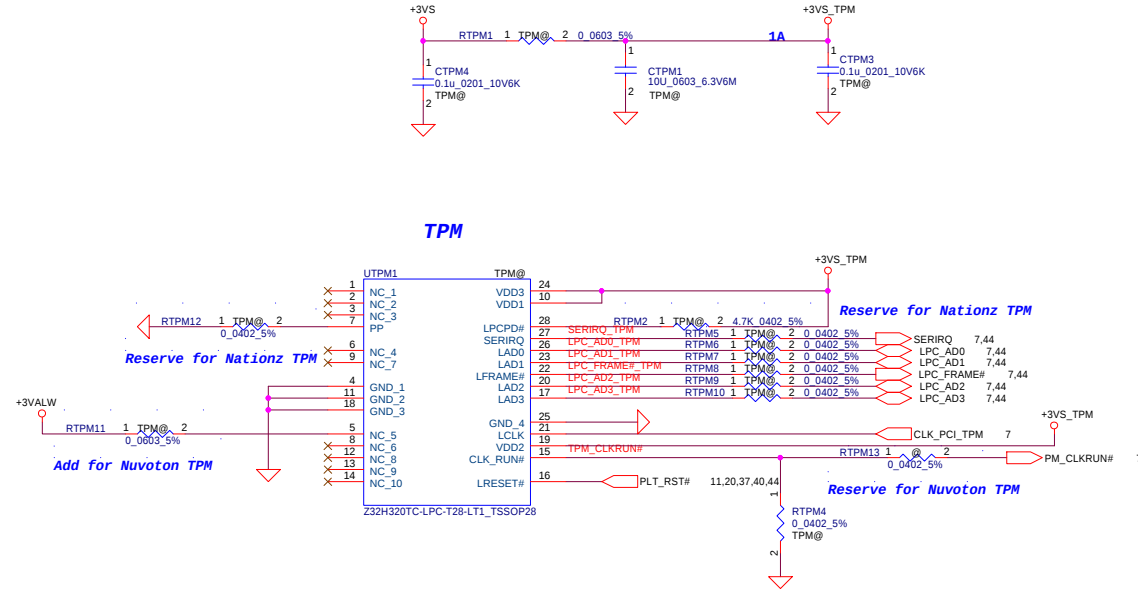
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Size		Document Number		D6421		Rev		1.0		
Date		Sunday, January 22, 2017		Sheet		28		of 60		

Security Classification		LC Future Center Secret Data		Title						
Issued Date		2015/08/20		Deciphered Date			2016/08/20		Blank	
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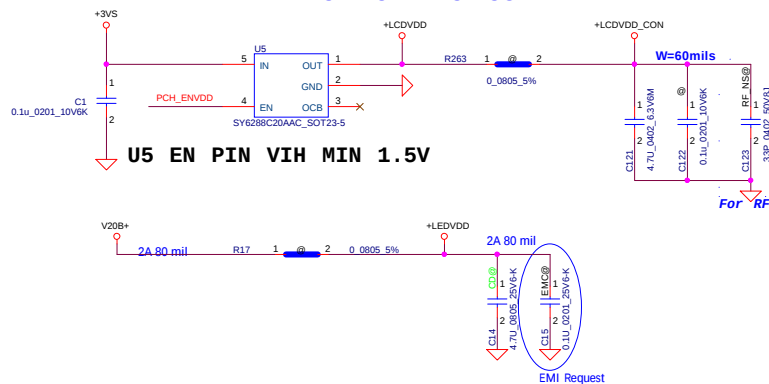
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cardreader	
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				Custom	DG421
				Date:	Sunday, January 22, 2017
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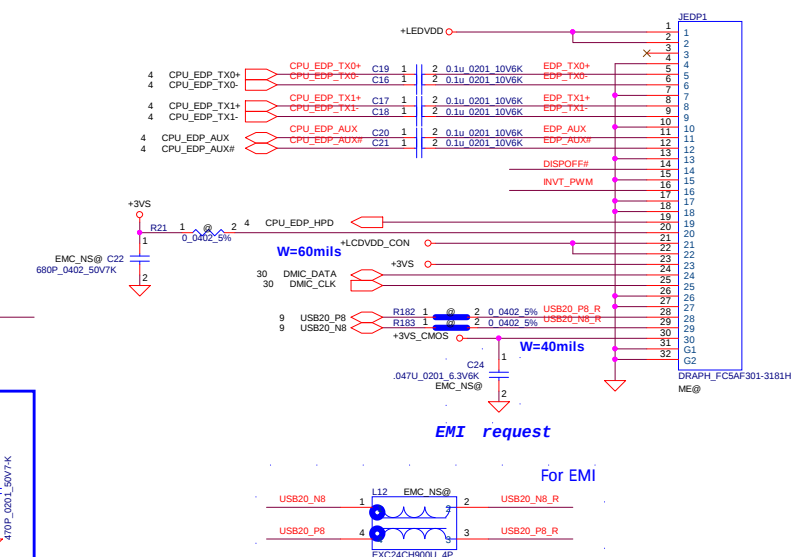
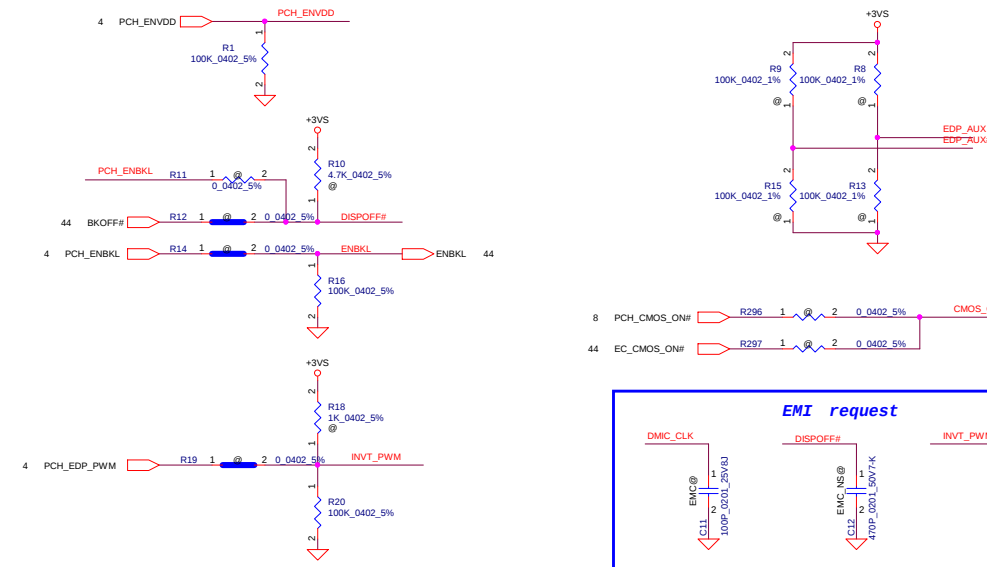
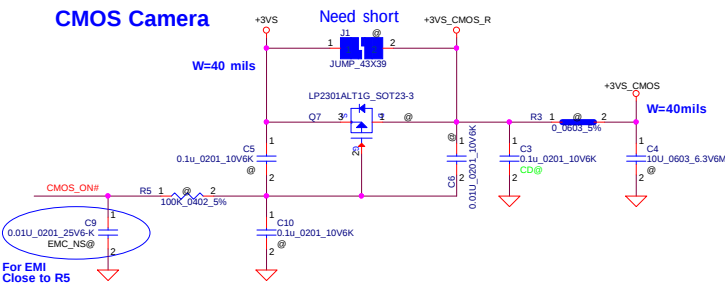
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RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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Issued Date		2015/08/20	Deciphered Date	2016/08/20			TPM				
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						Custom	DG421				
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LCD POWER CIRCUIT

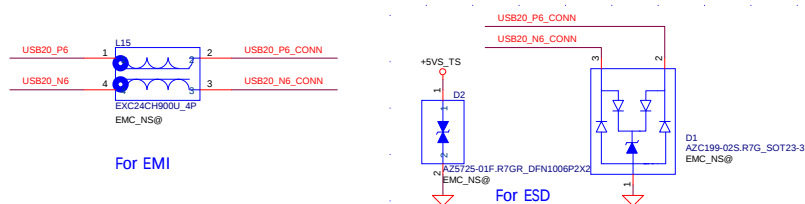


CMOS Camera

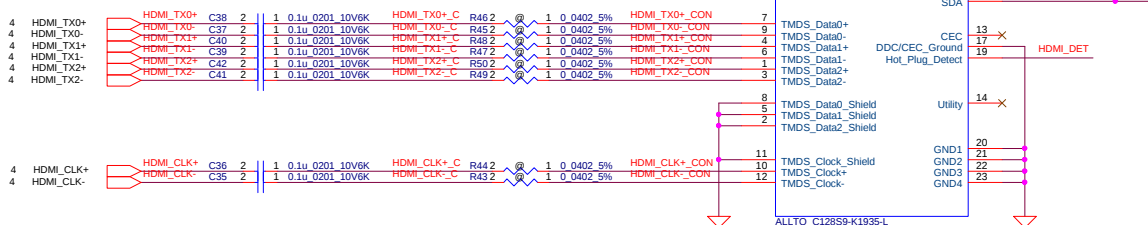
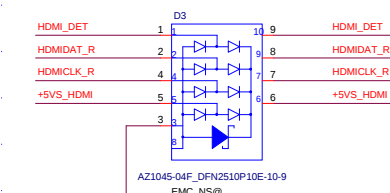


Touch Screen

Touch Screen



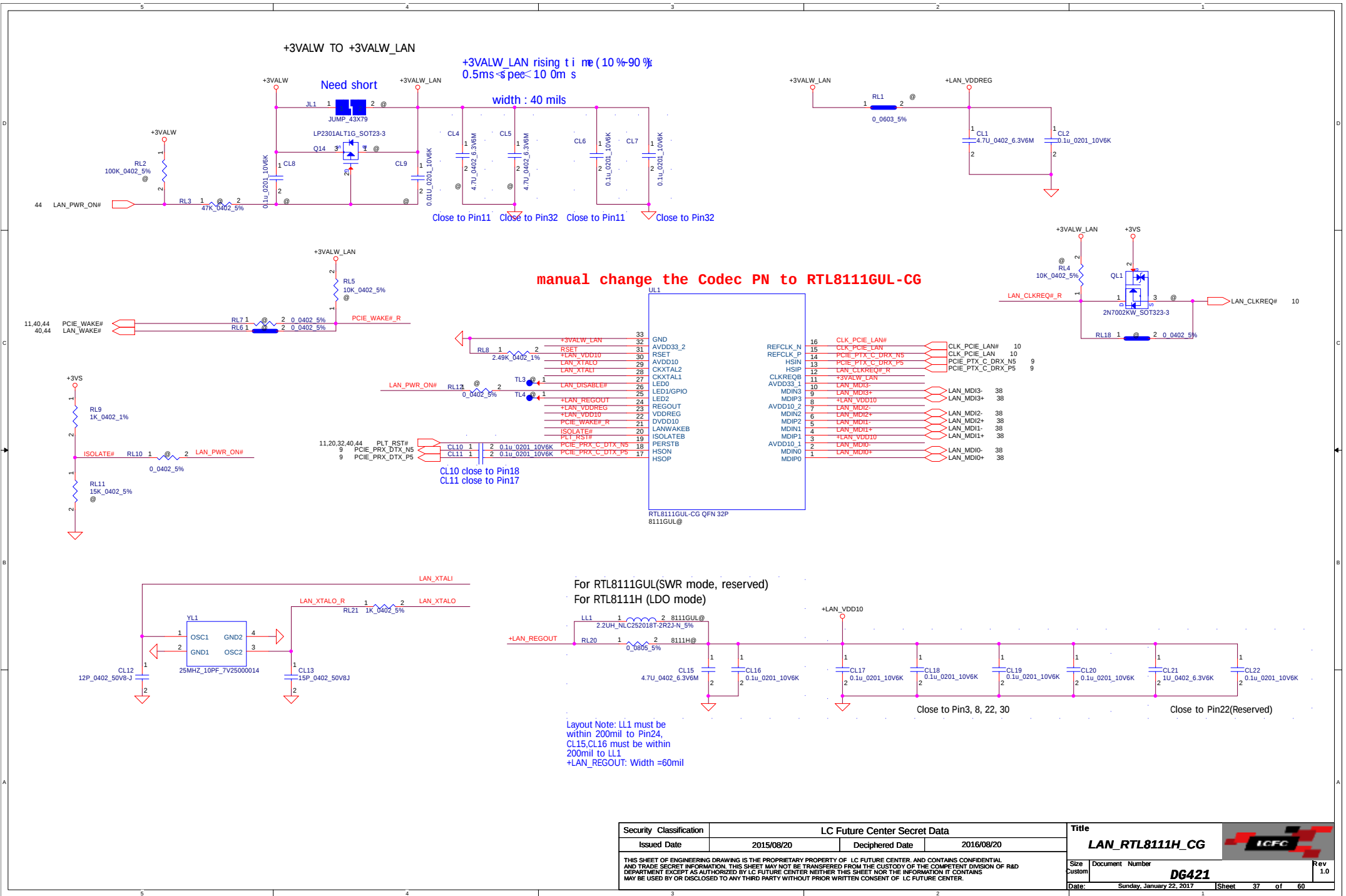
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LCFC					
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Size		Document Number		Rev	
Custom		D6421		1.0	
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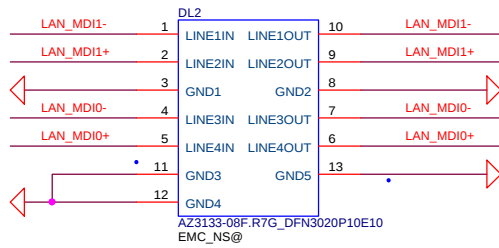
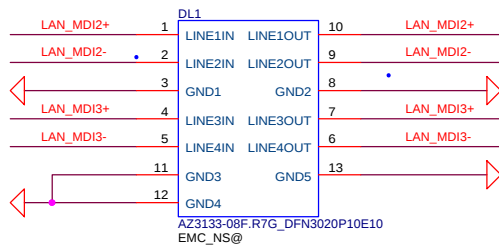
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Security Classification		LC Future Center Secret Data		Title					
Issued Date		2015/08/20	Deciphered Date		2016/08/20		P35-Blank		
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Date:		Sunday, January 22, 2017				Sheet	35	of	60

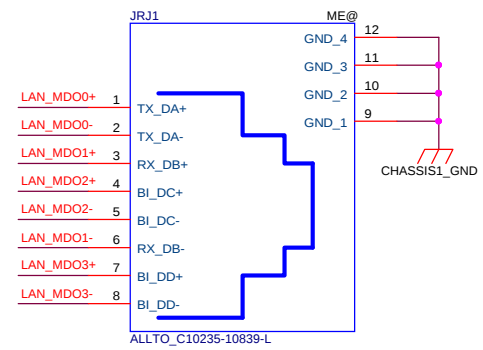
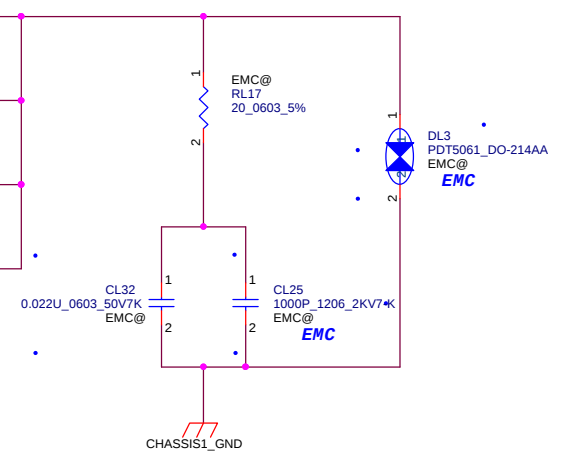
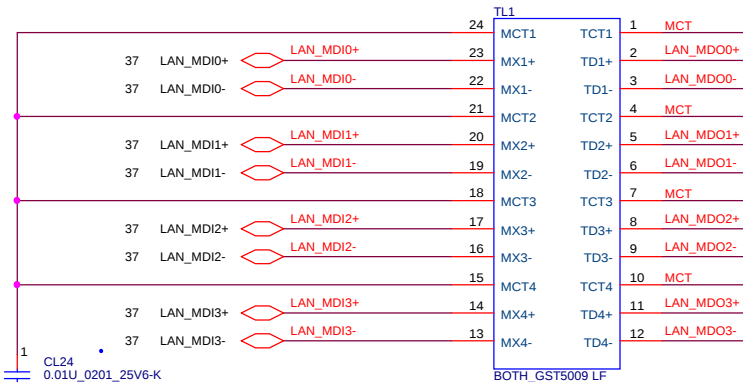
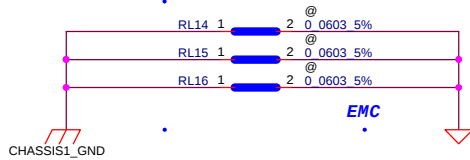
5		4		3		2		1	
D									
C									
B									
A									
				</					



DL1/DL2
1'S PN:SC300003M00



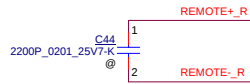
Place Close to TL1



8/16 Update RI45 P/N DC021608091 wei

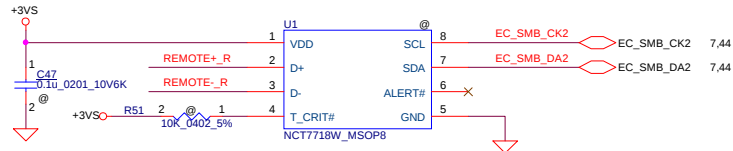
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN Transformer	
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Close to U1

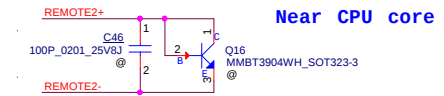


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

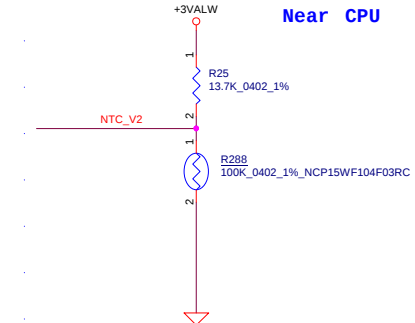
SMSC thermal sensor
placed near DIMM



Address 1001_101xb

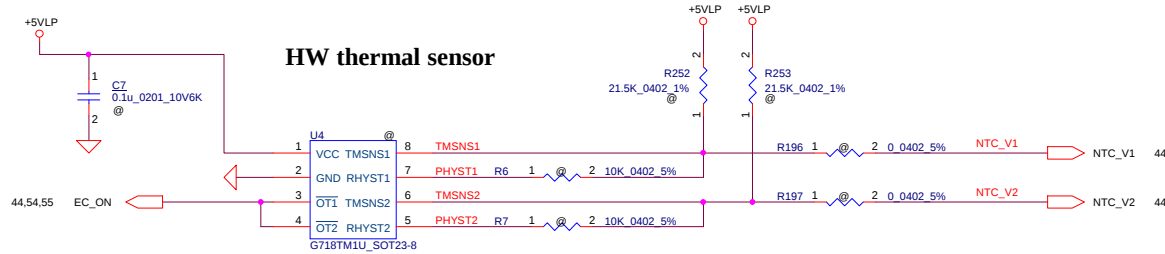


Near CPU



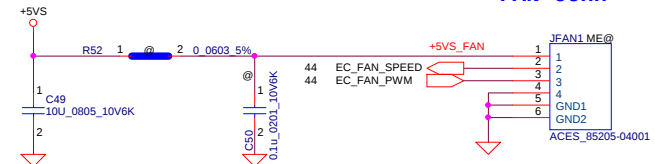
for layout optimized, change the EC_AGND to GND

HW thermal sensor



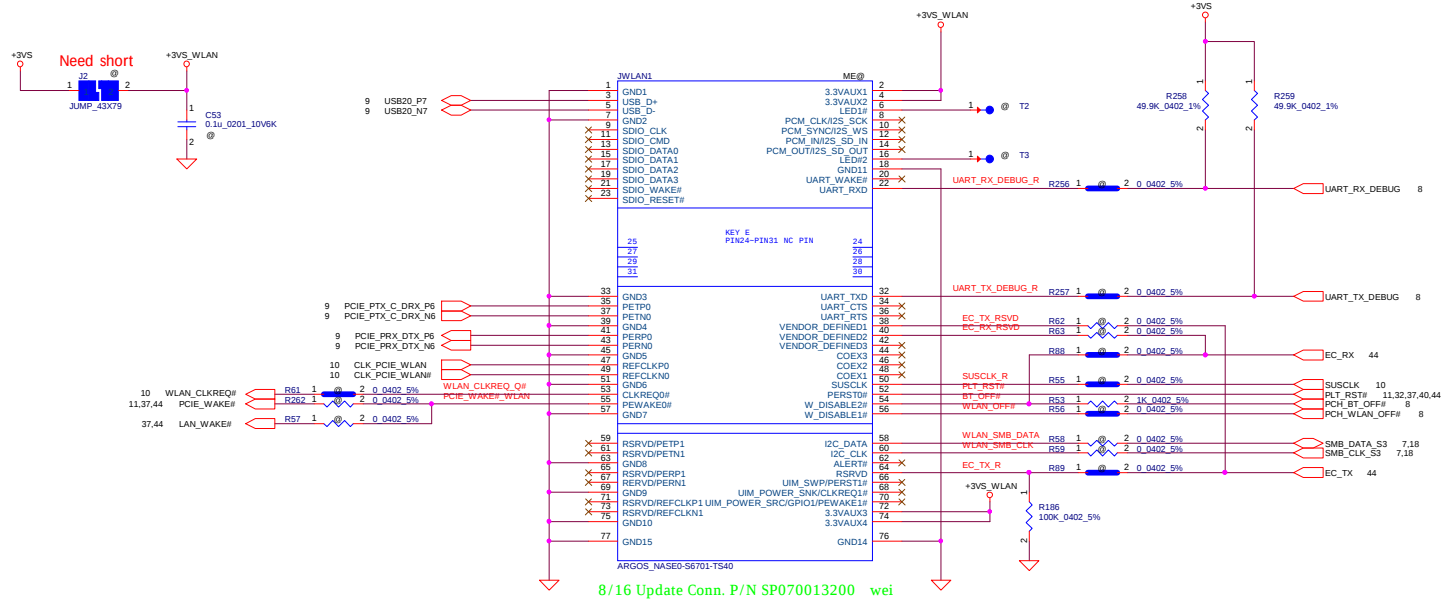
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN Conn

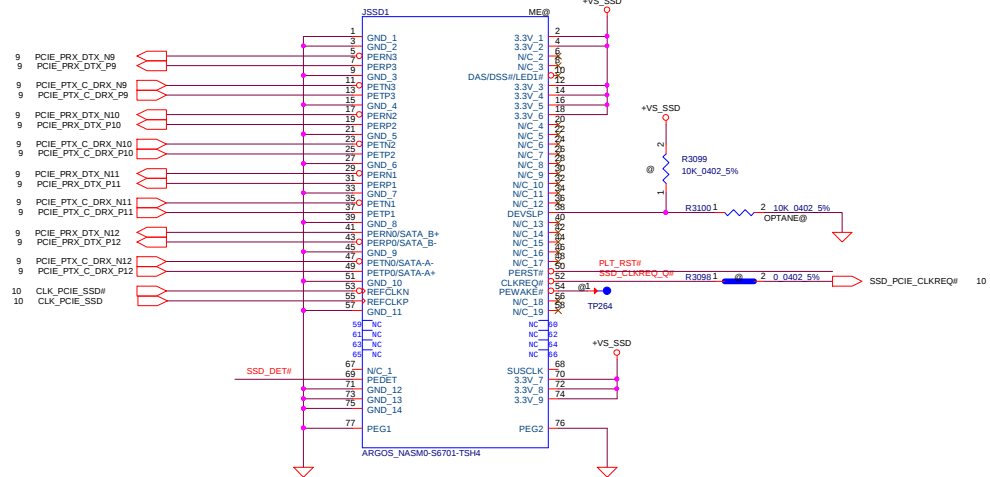
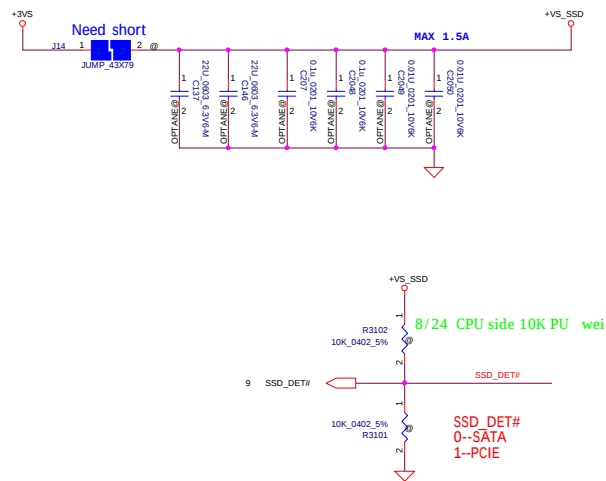


Security Classification	LC Future Center Secret Data			Title	Thermal sensor/FAN Conn		
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document Number	DG421	Rev 1.0
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Mini-Express Card(WLAN/WiMAX)

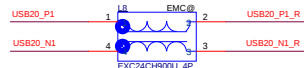
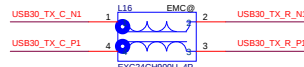
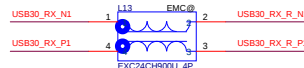
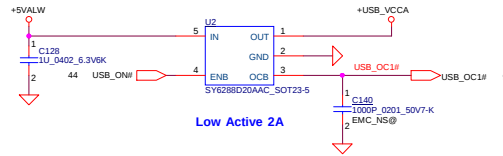


Optane Memory

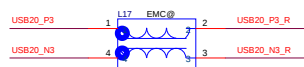
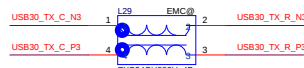
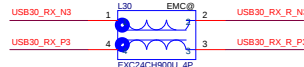


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	NGFF WLAN&SSD	
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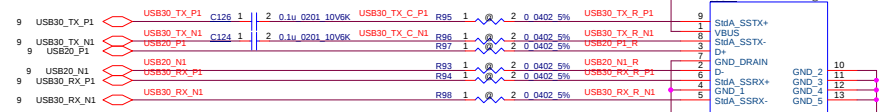
LEFT SIDE USB3.0 PORT x2



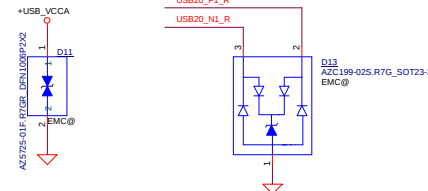
EMC



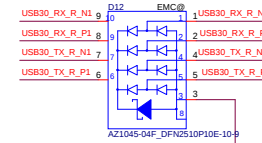
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09/05 Update USBConn. P/N DC021609011

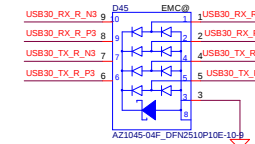
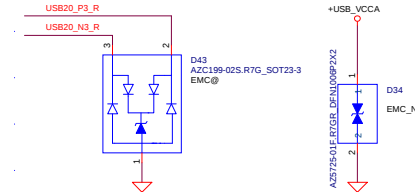


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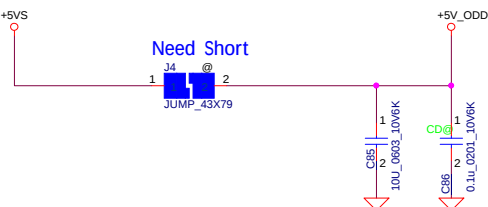
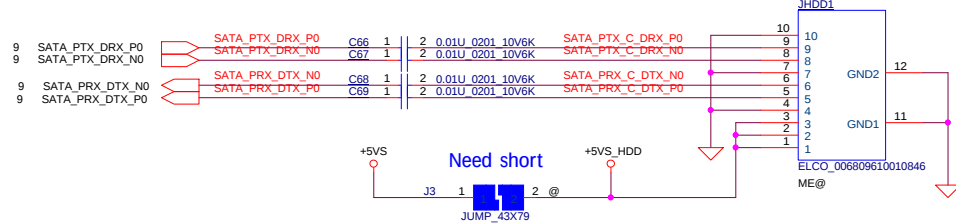
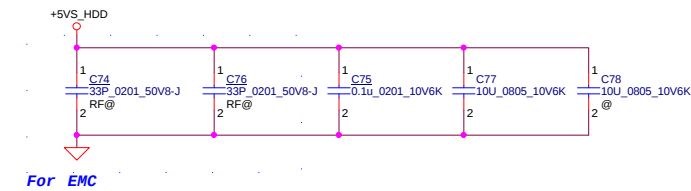
09/05 Update USBConn. P/N DC021609011

FOR ESD Close to Connector

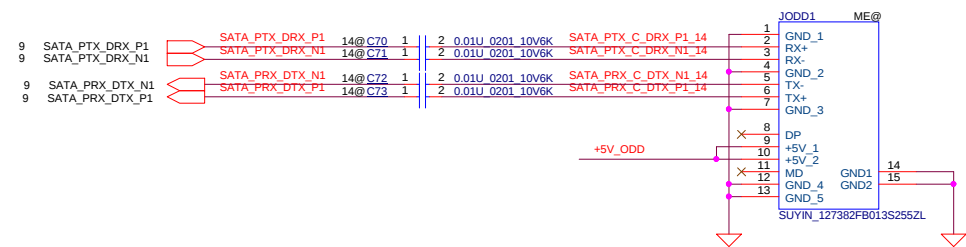


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Issued Date		Deciphered Date		USB3.0 PORT (LEFT)	
2015/08/20		2016/08/20			
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			D6421		
Date	Sunday, January 22, 2017		Sheet	41	of 60

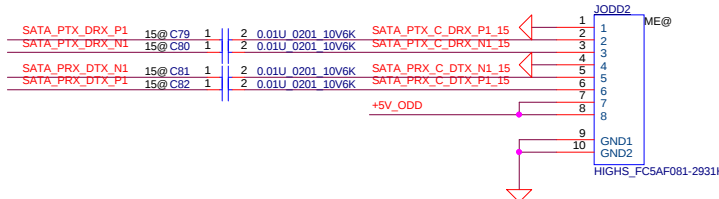
SATA HDD Conn.



FOR 14" SATA ODD Conn.



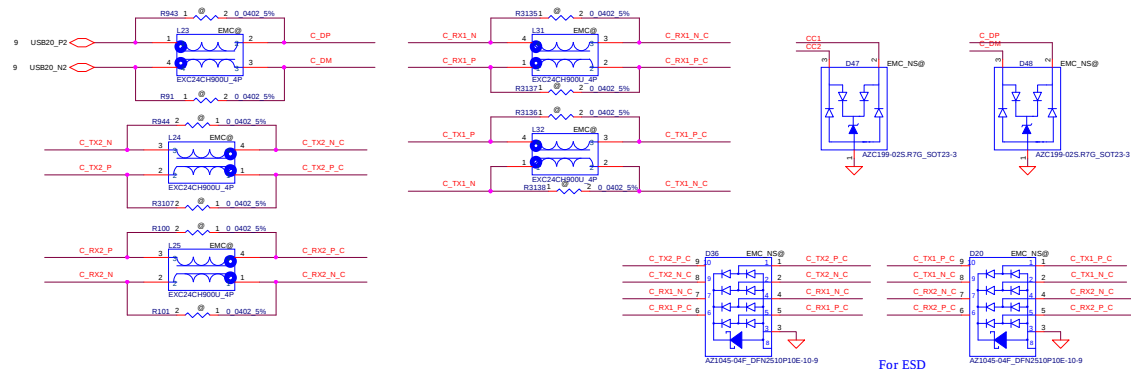
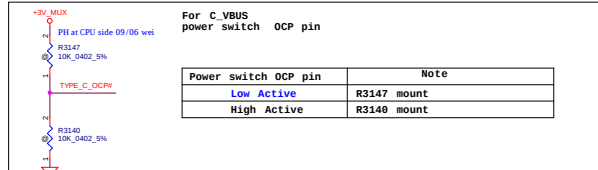
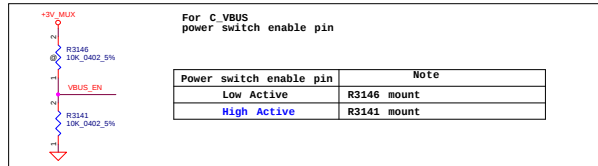
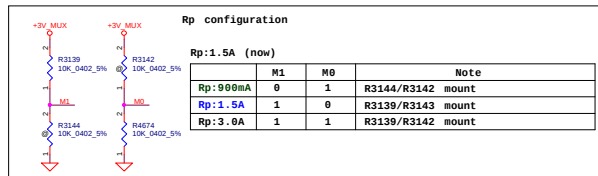
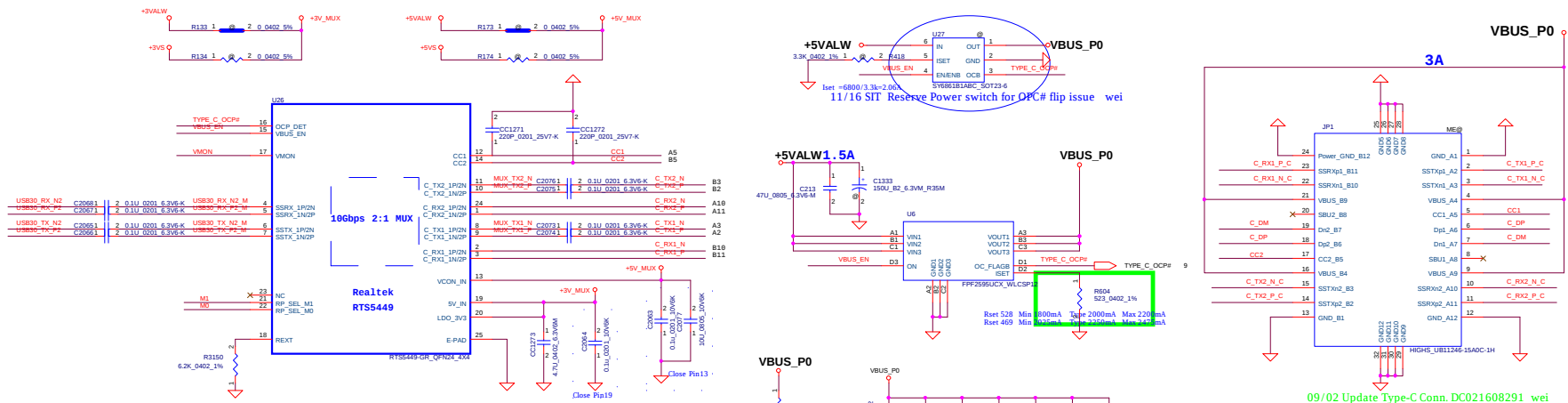
FOR 15" 17" SATA ODD FFC Conn

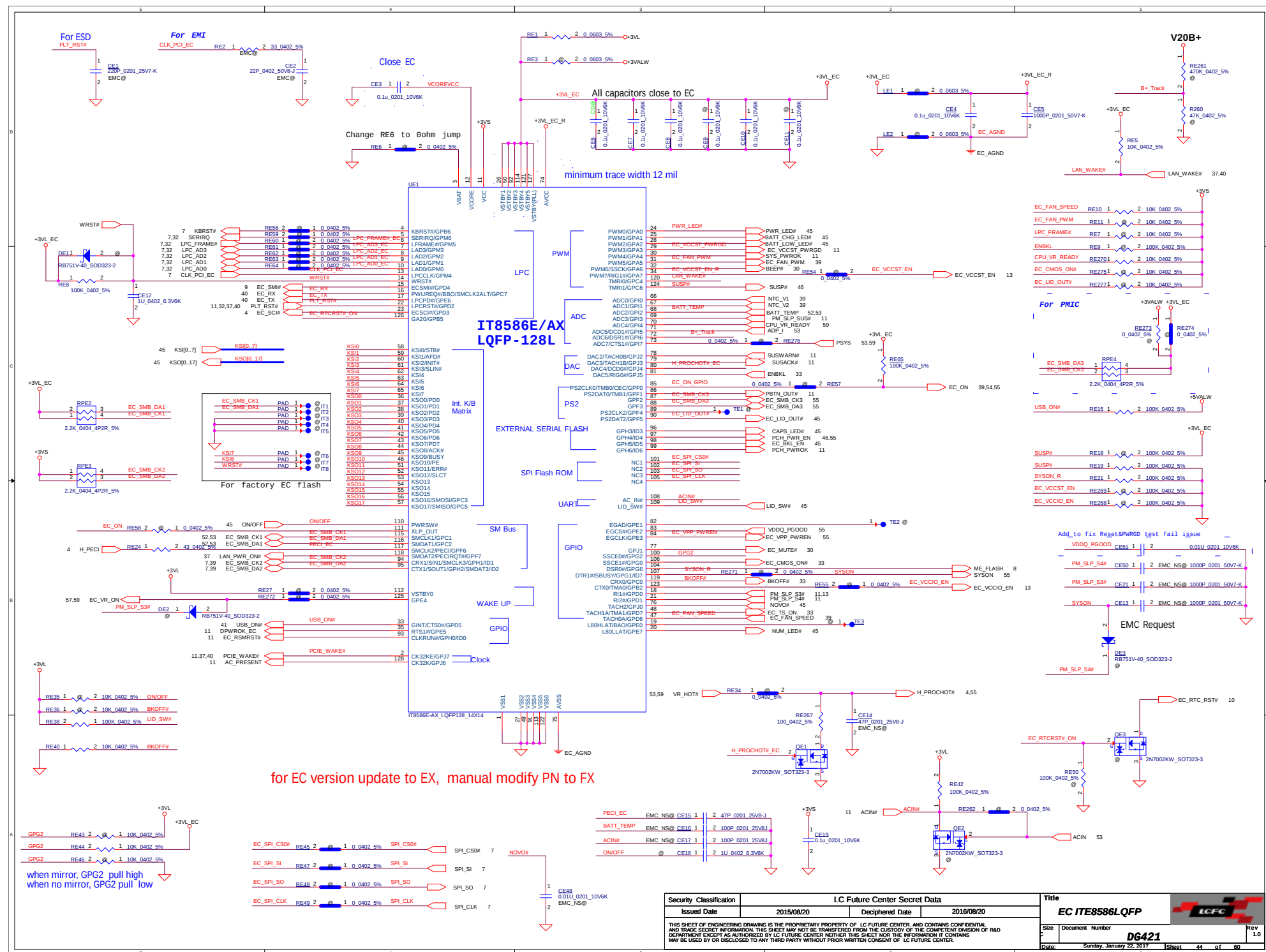


8/16 Update Conn. P/N SP01001YV00 wei

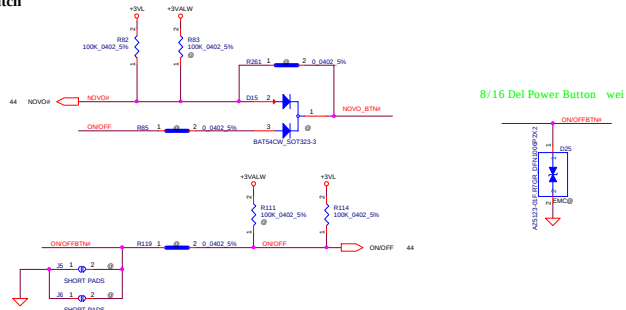
9 USB30_TX_N2 USB30_TX_N2
9 USB30_TX_P2 USB30_TX_P2

9 USB30_RX_N2 USB30_RX_N2
9 USB30_RX_P2 USB30_RX_P2

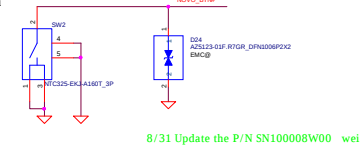




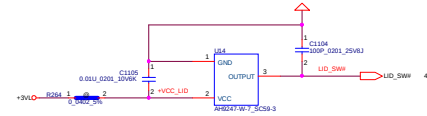
ON/OFF switch



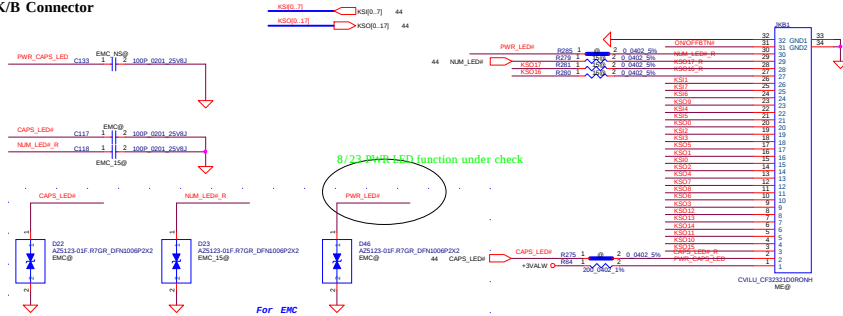
Novo button



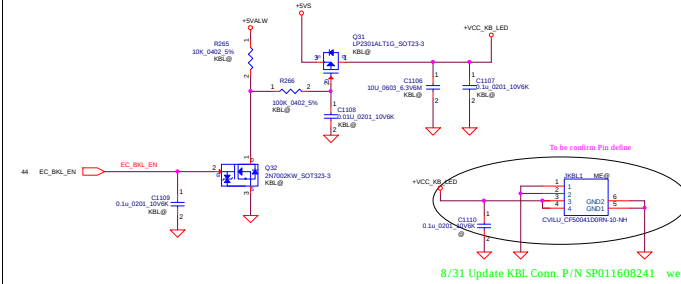
LID switch



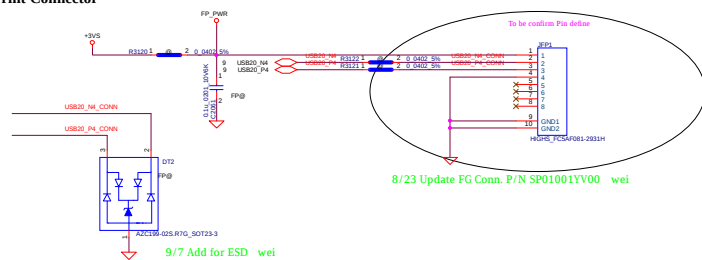
K/B Connector



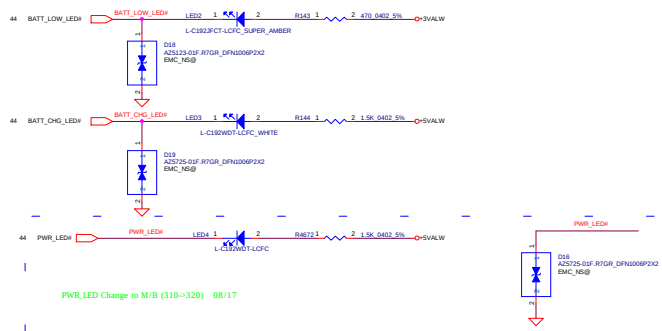
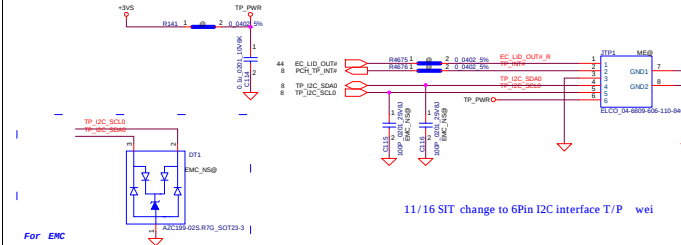
KB Backlight Connector



Finger Print Connector



TP/B Connector



Security Classification				Title	
L.C Future Center Secret Data				KBD/PWR/IO/LED/TP Conn	
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				Date: Sunday, January 22, 2017 10:00 AM	

Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short

Need Short

Change the main source to SA000067600 (GMT) 7/16

ENC

Need short

Id=3.2A

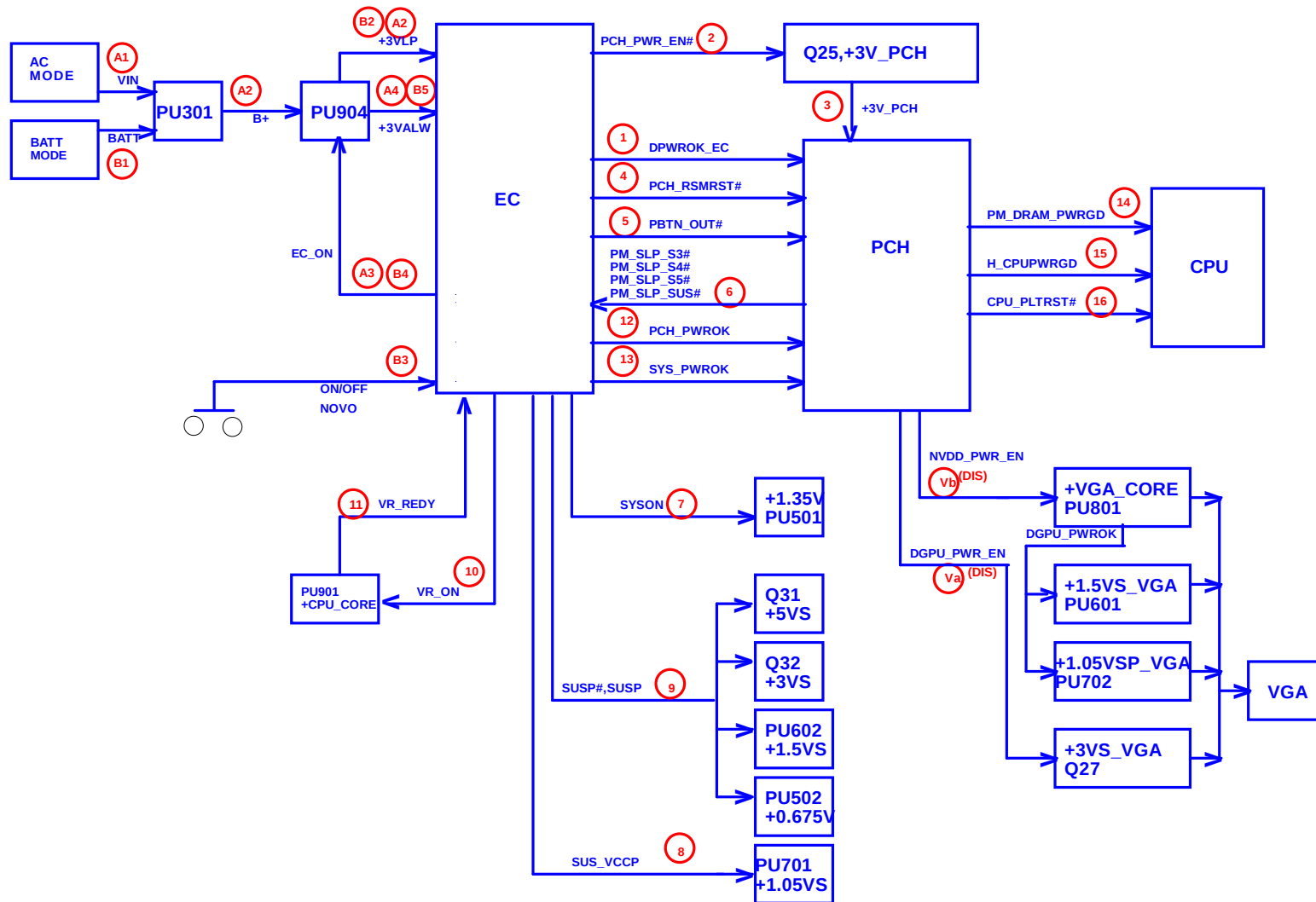
0.6A

8/29 Add +1.8VS Circuit for Audio wei

For DisCharge

08/29: Need double check enable signal and the resistance

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								Date: Sunday, January 22, 2017		Sheet 48 of 60	

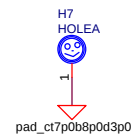
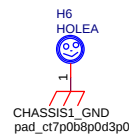
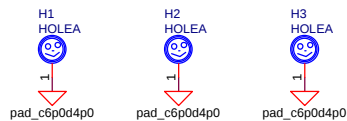
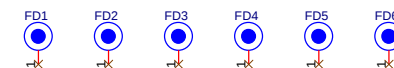
CPU Thermal Holex3

GPU Thermal Holex2

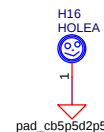
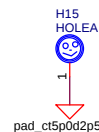
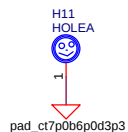
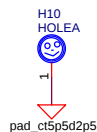
Close to RJ45

Close to Audio jack

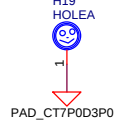
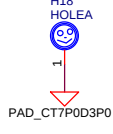
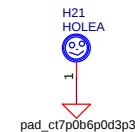
PCB Fedcal Mark PAD



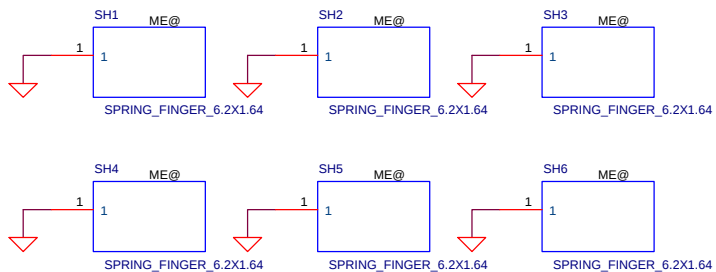
WLAN Standoff



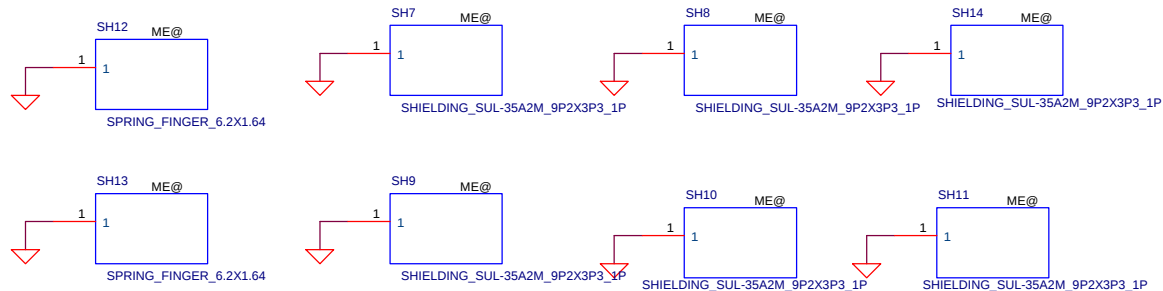
Optane Standoff



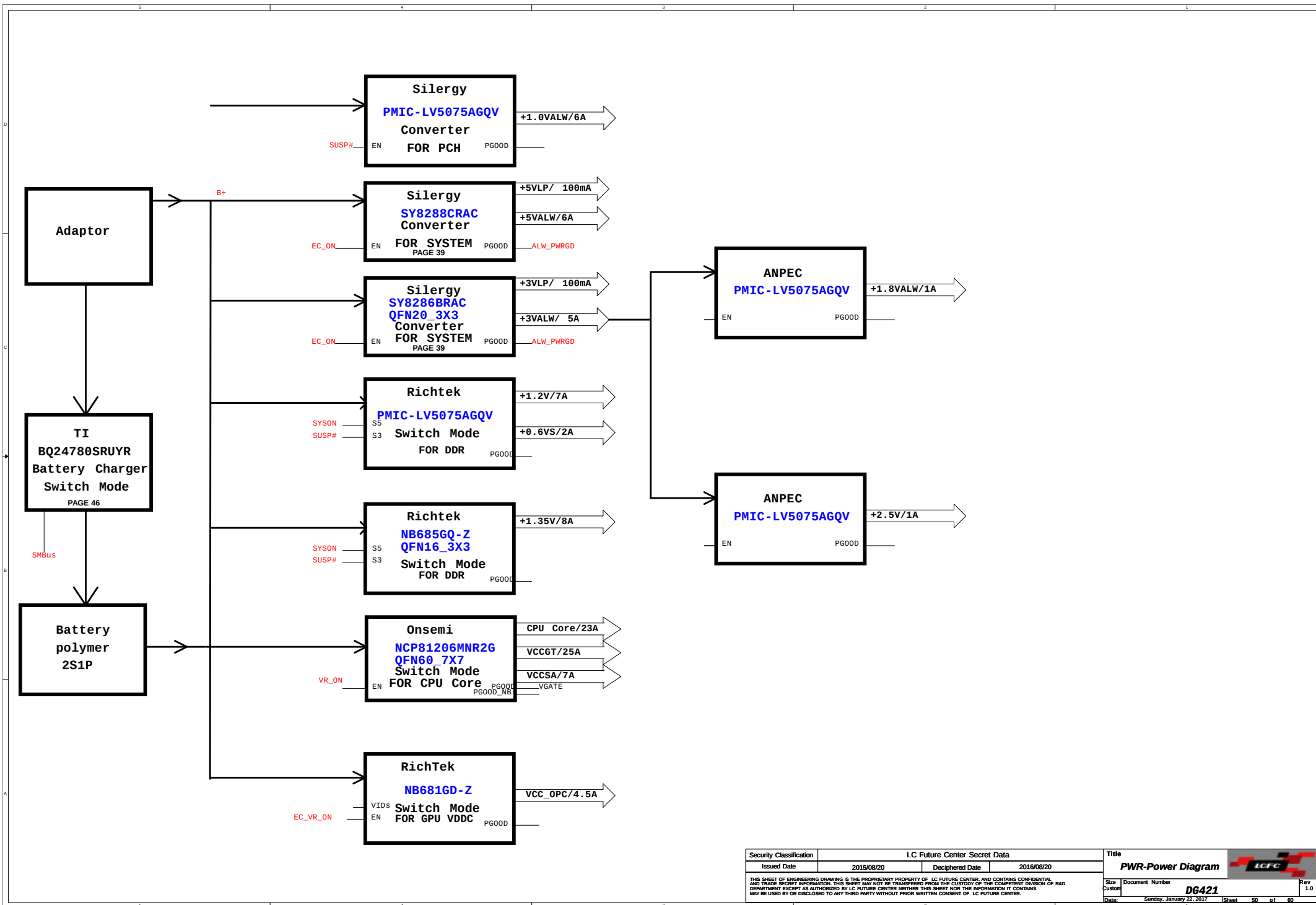
USB3.0 Shielding

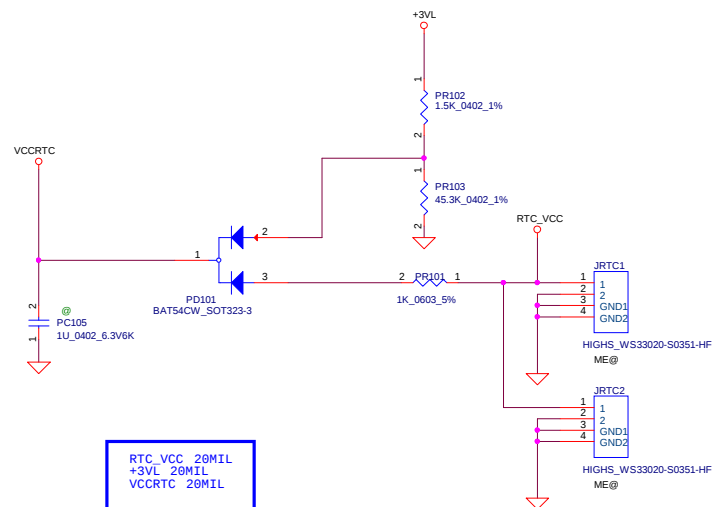


DDR4 Shielding

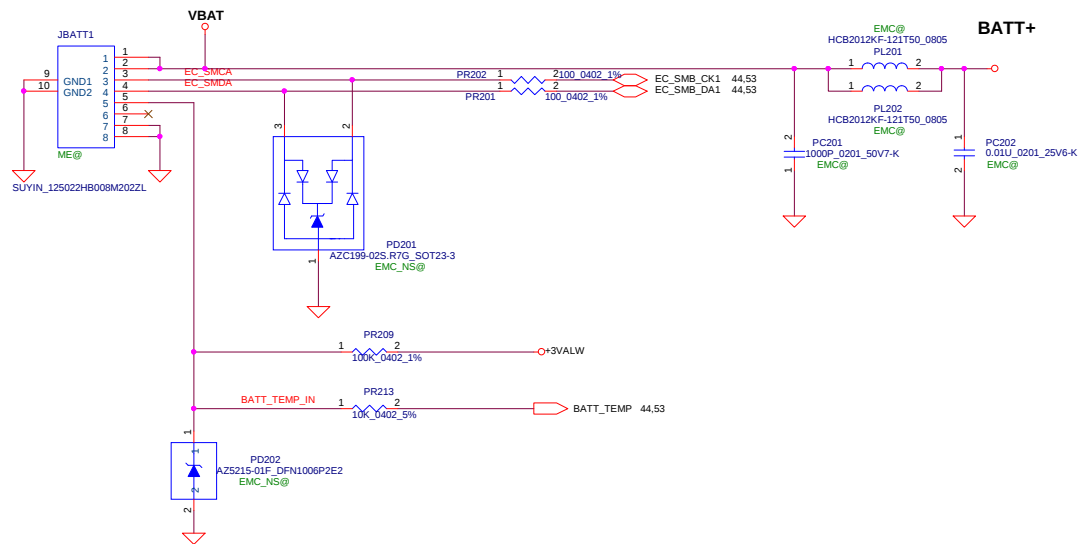


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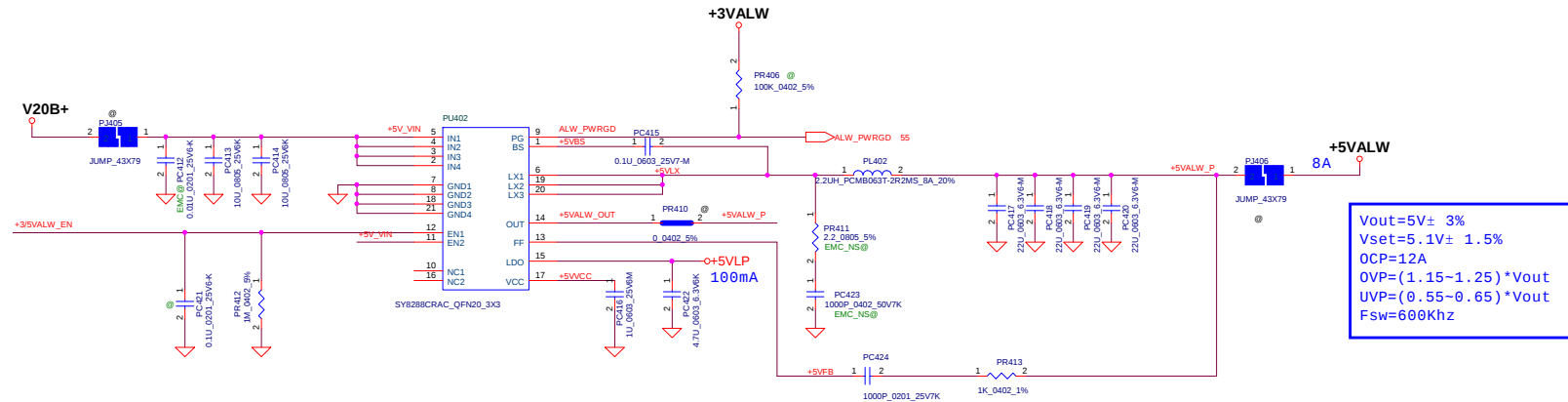
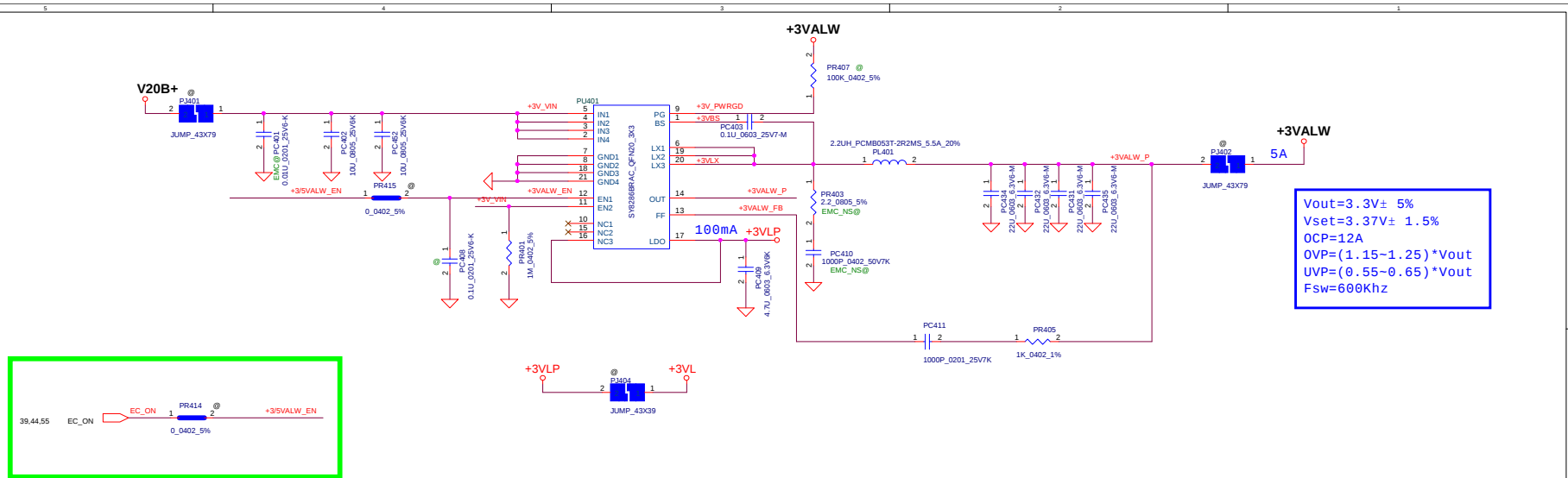


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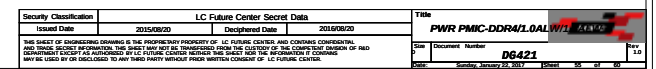


2S1P polymer battery
voltage level: +6V ~
8.4 V

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