LCFC Confidential

Miray-KBL M/B Schematics Document

INTEL KABYLAKE Mobile ULT Platform
INTEL KBL Y-series CPU + LPDDR3 Memory

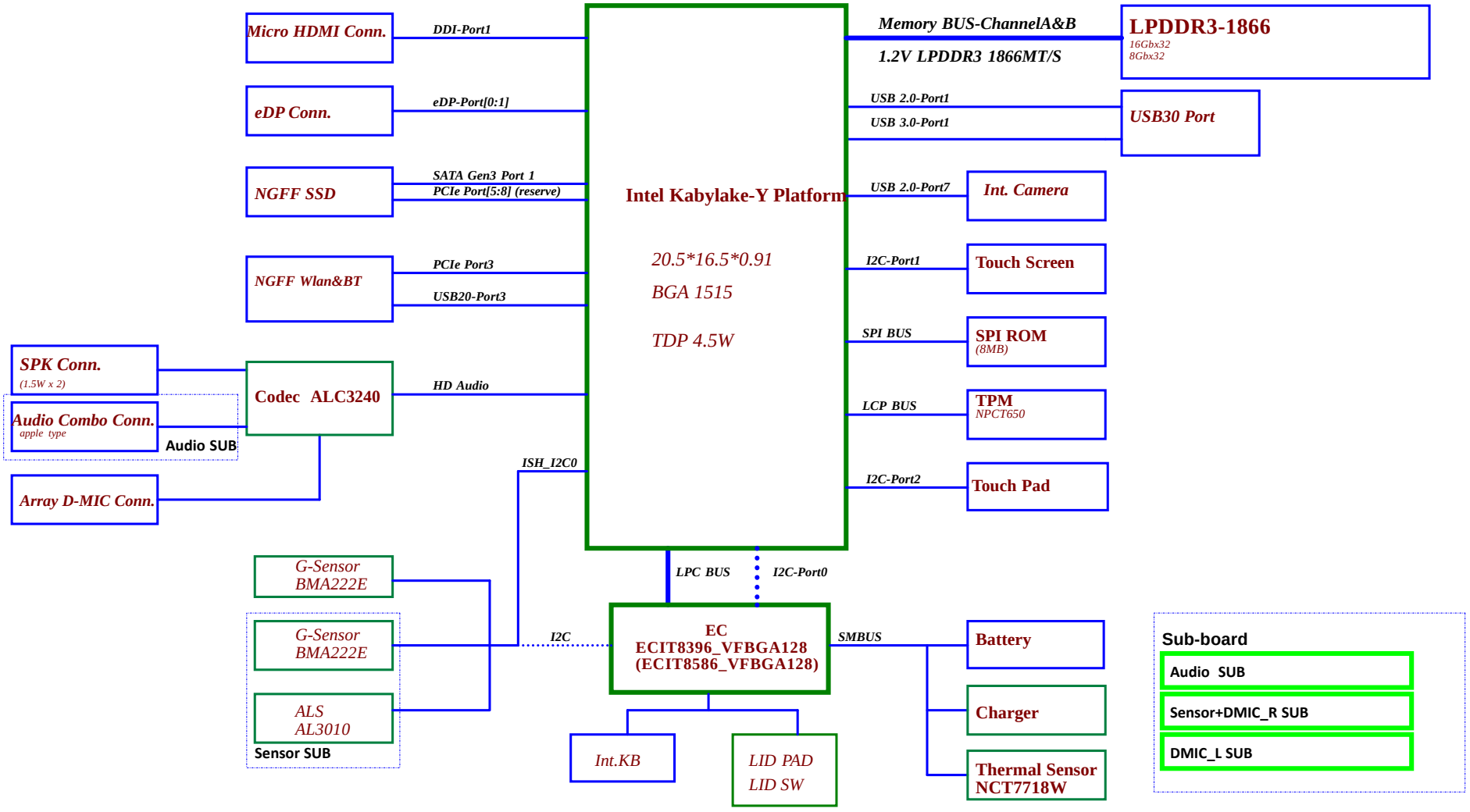
2016-06-21

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: Cover Page		
Size: C	Document Number: Miray-K	Rev: 1.0
Date: Thursday, June 23, 2016	Sheet 1 of 38	

LCFC-Miary Block diagram



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Title: Block Diagram

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 2 of 38

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +1.0VALW +1.8VALW +CPU_VCCPRIM	+3VALW_PCH	+DDR_1.2V +DDR_1.8V	+5VS +3VS +1.8VS +DDR_0.6VS +CPU_CORE +CPU_VCCIO +CPU_VCCGT +CPU_VCCSA
S0	0	0	0	0	0
S3	0	0	0	0	X
DS3	0	0	X	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
DS3 (Suspend to RAM)	LOW	LOW	HIGH	ON	LOW	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	Sensor	ALS	BATT	Thermal Sensor	charger	EC
EC_SMB_CLK1 EC_SMB_DAT1	IT8586 +3VALW_EC	X	X	V	X	V	X
EC_SMB_CLK3 EC_SMB_DAT3	IT8586 +3VS	V +3VS	V +3VS	X	X	X	X
EC_SMB_CLK0 EC_SMB_DAT0	IT8586 +3VS	X	X	X	V +3VS	X	X
EC_SMB_CLK4 EC_SMB_DAT4	PCH +3VS	X	X	X	X	X	V +3VS

SM Bus address

	Device	address
EC1	Battery	0001 011X b
	Charger	
EC3	Sensor	
	ALS	
	Thermal Sensor	1001_100xb
EC0		
PCH EC4	EC	

PCIE PORT LIST

Port	Device
1	
2	
3	WLAN
4	
5 - 8	Reserve PCIE SSD
8	SATA SSD

USB Port Table

	USB20		USB30	
EXHCI/XHCI	1	USB	1	USB
	2		2	
	3	BT	3	
	5		4	
	7	Camera		
	9			

BOM Structure Table

BOM Structure		BOM Structure	
TI@	TI MIPI camera mount	MIRROR@	EC Mirror-code enable
TPM@	TPM module	UNMIRROR@	EC Mirror-code disable
DEBUG@	DEBUG CARD Part	DA8@	PCB
ME@	ME part(connector, hole)	UPI@	UPI MIPI camera mount
RF@	RF request		
EMC@	EMC request		
CD@	COST DOWN Part		
REV@	RESERVER Part		

Board ID Table

Board ID	Description	PCB Revision

BOM Configuration Table

SKU	Description	BOM Config	
SKU1			
SKU2			

X76&VGA Configuration Table

SKU	Description	BOM Config	

PCB And LOGO Config

PCB	ZZZ1 DA8@ PCB 12X NM-B011 REV0 M/B	LOGO
CPU	ZZZ2 G09@ S IC HE8067702739807 QKKR G0 0.9G FCBGA	ZZZ3 HDMI@ HDMI LOGO
VRAM	ZZZ4 MIC8G@ MICRON8G; ZZZ5 MIC4G@ MICRON 4G; ZZZ6 SAM8G@ SAMSUNG 8G; ZZZ7 SAM4G@ SAMSUNG 4G; ZZZ8 HY8G@ HYNIX 8G; ZZZ9 HY4G@ HYNIX 4G	

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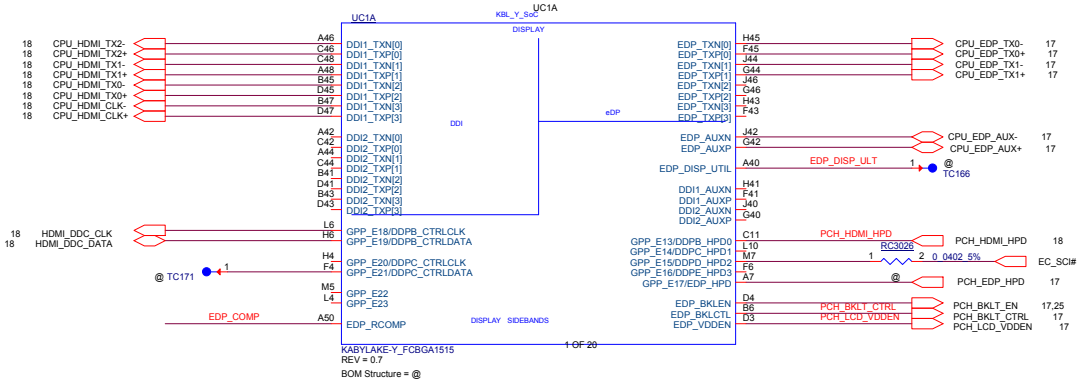
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: Notes List

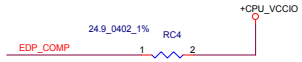
Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 3 of 38



DDP*_CTRLDATA
This signal has a weak internal pull-down.
0 = Port B is not detected.
***1 = Port B is detected.**

pull up at HDMI side.



+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil

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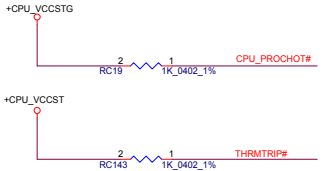
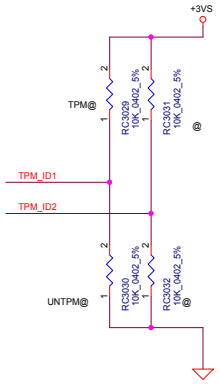
Title: **MCP (DDI,EDP)**

Size	Document Number	Rev
C	Miray-K	1.0
Date: Thursday, June 23, 2016	Sheet 4 of 38	

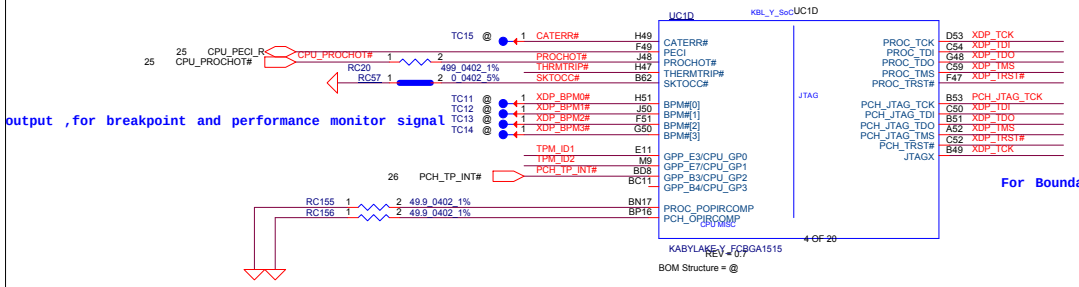


130 degree

TPM_ID1	Description
0	NO physical TPM
1	physical TPM



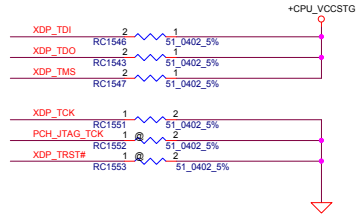
0901 add



output ,for breakpoint and performance monitor signal

For Boundary Scan

Debug Port DG
Merged MCP XDP-SFF-26Pin Connector Pinout



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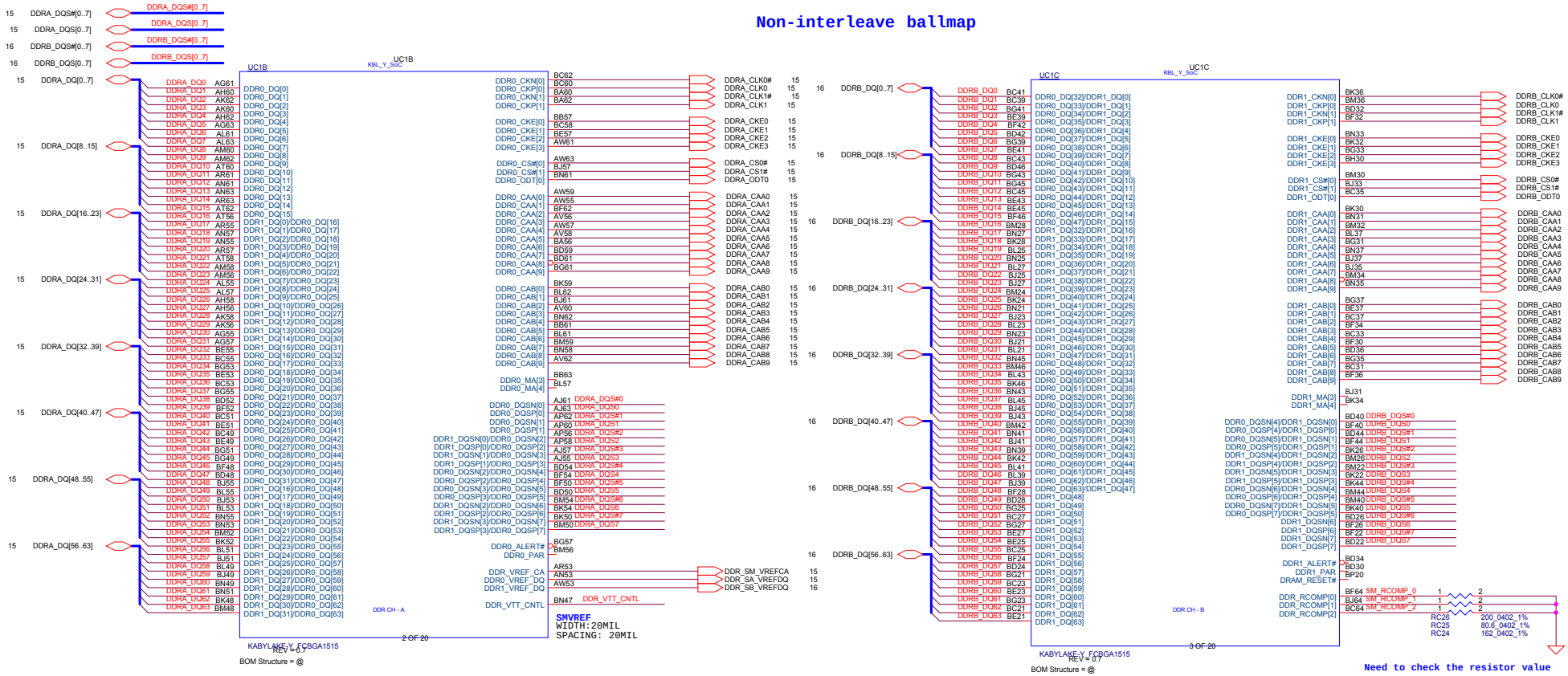
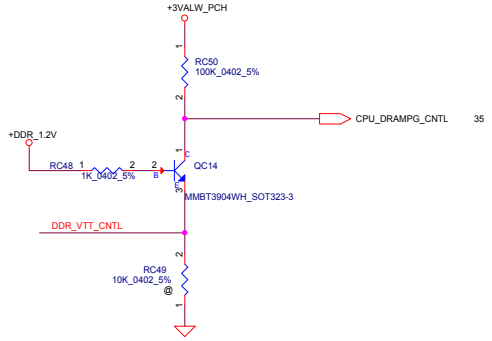
Title: MCP (XDP,JATG)

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 5 of 38

Non-interleave ballmap





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Title: MCP (DDR)

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 6 of 38

+VCCHDA

RC47 1 @ 2 1K_0402_5% HDA_SDOUT

HDA_SDO This signal has a weak internal pull-down.
*** 0 = Enable security measures defined in the Flash Descriptor.**
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

For EMI

PCH_HDA_SDIN0

@ 1 CC7 10P_0402_50V8J 2

The signal has a weak internal pull-down.
0 = Disable " Top Swap" mode. (Default)
1 = Enable " Top Swap" mode

+3VS

2 R684 1 2.2K_0402_5% PCH_BEEP
@

25 PCH_SPI_CS0# PCH_SPI_CS0# RC64 1 2 0_0402_5% SPI_CS0#
25 PCH_SPI_SI PCH_SPI_SI RC52 1 2 15_0402_5% SPI_SI
25 PCH_SPI_SO PCH_SPI_SO RC53 1 2 15_0402_5% SPI_SO
25 PCH_SPI_CLK PCH_SPI_CLK RC65 1 2 15_0402_5% SPI_CLK

+3V_SPI

RC61 1K_0402_5% 1 2
RC60 1K_0402_5% 1 2

SPI_WP# RC54 1 2 15_0402_5% PCH_SPI_WP#
@
SPI_HOLD# RC55 1 2 15_0402_5% PCH_SPI_HOLD#
@

1 R3005 2 @ 100_0402_1%

SPI_HOLD# for SKL ES Sample
1. 1K PD, unmont 1K PU with HOLD functionality disabled
* 2. 100ohm PD, 1K PU, disabled after RSMRST# de-assertion

1 CC1981 2 EMC_NS@ 1000P_0402_50V7K EC_KBRST#
1 CC1982 2 EMC_NS@ 1000P_0402_50V7K PCH_PCI_CLK

+3VALW_PCH +3V_SPI

RC1711 2 0_0402_5%

+3V_SPI

UC3 @

PCH_SPI_CS0# 1 CS# VCC 8
PCH_SPI_SO 2 DO HOLD# 7 PCH_SPI_HOLD#
PCH_SPI_WP# 3 WP# CLK 6 PCH_SPI_CLK
4 GND DI 5 PCH_SPI_SI

W25Q64FVSSIQ_SO8

1 CS28 2 0.1u_0201_10V6K

UC3 and UC4 Colay

+3V_SPI

UC4

PCH_SPI_CS0# 1 /CS VCC 8
PCH_SPI_SO 2 DO(IO1) /HOLD(IO3) 7 PCH_SPI_HOLD#
PCH_SPI_WP# 3 /WP(IO2) CLK 6 PCH_SPI_CLK
4 GND DI(IO0) 5 PCH_SPI_SI
PAD_GND 9

W25Q64FVZPIQ_WSON8_6X5

23 PCH_HDA_SYNC RC43 1 2 33_0402_5% HDA_SYNC
23 PCH_HDA_BCLK RC42 1 2 33_0402_5% HDA_BCLK
HDA_SDOUT
23 PCH_HDA_SDIN0 PCH_HDA_SDIN0
23 PCH_HDA_SDOUT RC45 1 2 33_0402_5% HDA_SDOUT
25 PCH_ME_PROTECT RC46 1 2 0_0402_5%

TC12@ 1

23 PCH_BEEP PCH_BEEP

UC1G KBL_Y_SoC

BJ19	HDA_SYNC/I2S0_SFRM		
BK18	HDA_BLK/I2S0_SCLK		
BK16	HDA_SDO/I2S0_TXD		
BL15	HDA_SDI0/ I2S0_RXD		
BL17	HDA_SDI1/I2S1_RXD		
BL19	HDA_RST# /I2ST_SCLK		
V5	GPD_D23/I2S_MCLK		
BL12	I2S1_SFRM		
BK14	I2S1_TXD		
	AUDIO		
AT13	GPP_F1/I2S2_SFRM		
AT11	GPP_F0/I2S2_SCLK		
AP11	GPP_F2/I2S2_TXD		
AT5	GPP_F3/I2S2_RXD		
V3	GPD_D19/DMIC_CLK0		
V11	GPD_D20/DMIC_DATA0		
U12	GPD_D17/DMIC_CLK1		
U6	GPD_D18/DMIC_DATA1		
AV3	GPP_B14/SPKR		
		AH9	GPP_G0/SD_CMD
		AH11	GPP_G1/SD_DATA0
		AG12	GPP_G2/SD_DATA1
		AF9	GPP_G3/SD_DATA2
		AF11	GPP_G4/SD_DATA3
		AG8	GPP_G5/SD_CD#
	SDIO/SDXC	AG10	GPP_G6/SD_CLK
		AE12	GPP_G7/SD_WP
BL4			GPP_A17/SD_PWR_EN#/ISH_GP7
BN4			GPP_A16/SD_1P8_SEL
BF1			SD_RCOMP
AJ8			GPP_F23

1 @ 1 @ TC82 TC191
SD_RCOMP 2 RC1537 1 200_0402_1%
1 @ TC194

7 OF 20

KABYLAKE-Y_FCBGA1515 REV=0.7

BOM Structure = @

UC1E KBL_Y_SoC

SPI_CLK	AU10	SPI0_CLK	
SPI_SO	AU12	SPI0_MISO	
SPI_SI	AT3	SPI0_MOSI	
SPI_WP#	AV11	SPI0_IO2	SPI - FLASH
SPI_HOLD#	AV13	SPI0_IO3	
SPI_CS0#	AU4	SPI0_CS0#	
	AU6	SPI0_CS1#	
	AU8	SPI0_CS2#	
			SPI - TOUCH
	P9	GPP_D1	
	N8	GPP_D2	
	P3	GPP_D3	
	W12	GPP_D21	
	V7	GPP_D22	
	N6	GPP_D0	
	F12	CL_CLK	C LINK
	D12	CL_DATA	
	B12	CL_RST#	
EC_KBRST#	BL10	GPP_A0/RCIN#	
	BN8	GPP_A6/SERIRQ	
			SMBUS, SMLINK
			LPC
	AC12	GPP_C0/SMBCLK	PCH_SMB_CLK
	W6	GPP_C1/SMBDATA	PCH_SMB_DATA
	W8	GPP_C2/SMBALERT#	SMB_ALERT#
	W4	GPP_C3/SML0CLK	SML0_CLK
	AC10	GPP_C4/SML0DATA	SML0_DATA
	AA6	GPP_C5/SML0ALERT#	SML0_ALERT#
	AA4	GPP_C6/SML1CLK	PCH_SML1_CLK
	W10	GPP_C7/SML1DATA	PCH_SML1_DAT
	BB6	GPP_B23/SML1ALERT#/PCHHOT#	SML1_ALERT#
	BK11		
	BJ8	GPP_A1/LAD0/ESPI_IO0	LPC_AD0 24,25
	BG10	GPP_A2/LAD1/ESPI_IO1	LPC_AD1 24,25
	BP6	GPP_A3/LAD2/ESPI_IO2	LPC_AD2 24,25
	BP7	GPP_A4/LAD3/ESPI_IO3	LPC_AD3 24,25
	BJ6	GPP_A5/LFRAME#/ESPI_CS#	LPC_FRAME# 24,25
		GPP_A14/SUS_STAT#/ ESPI_RESET#	SUS_STAT#
	BJ10	GPP_A9/CLKOUT_LPC0/ESPI_CLK	CLKOUT0
	BF5	GPP_A10/CLKOUT_LPC1	CLK_PCI_TPM_R
	BH11	GPP_A8/CLKRUN#	PM_CLKRUN#

1 @ TC81
RC173 1 2 22_0402_5% PCH_PCI_CLK 25
RC1541 2 1 22_0402_5% CLK_PCI_TPM 24
PM_CLKRUN# 24

5 OF 20

KABYLAKE-Y_FCBGA1515 REV = 0.7

BOM Structure = @

for signal SMB_ALERT#:
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH

SML0_ALERT# 2 @ 1 R687 2.2K_0402_5%
SMB_ALERT# 2 1 R688 2.2K_0402_5%
SML1_ALERT# 1 2 R689 150K_0402_5%

PCH_SMB_CLK 4 RPC686 1
PCH_SMB_DATA 3 2
2.2K_0404_4P2R_5%
@

+3VALW_PCH

SML0_CLK 1 RPC25 8
SML0_DATA 2 7
PCH_SML1_CLK 3 6
PCH_SML1_DAT 4 5
10K_0804_8P4R_5%
@

+3VS

PM_CLKRUN# 1 2 R3024 8.2K_0402_5%

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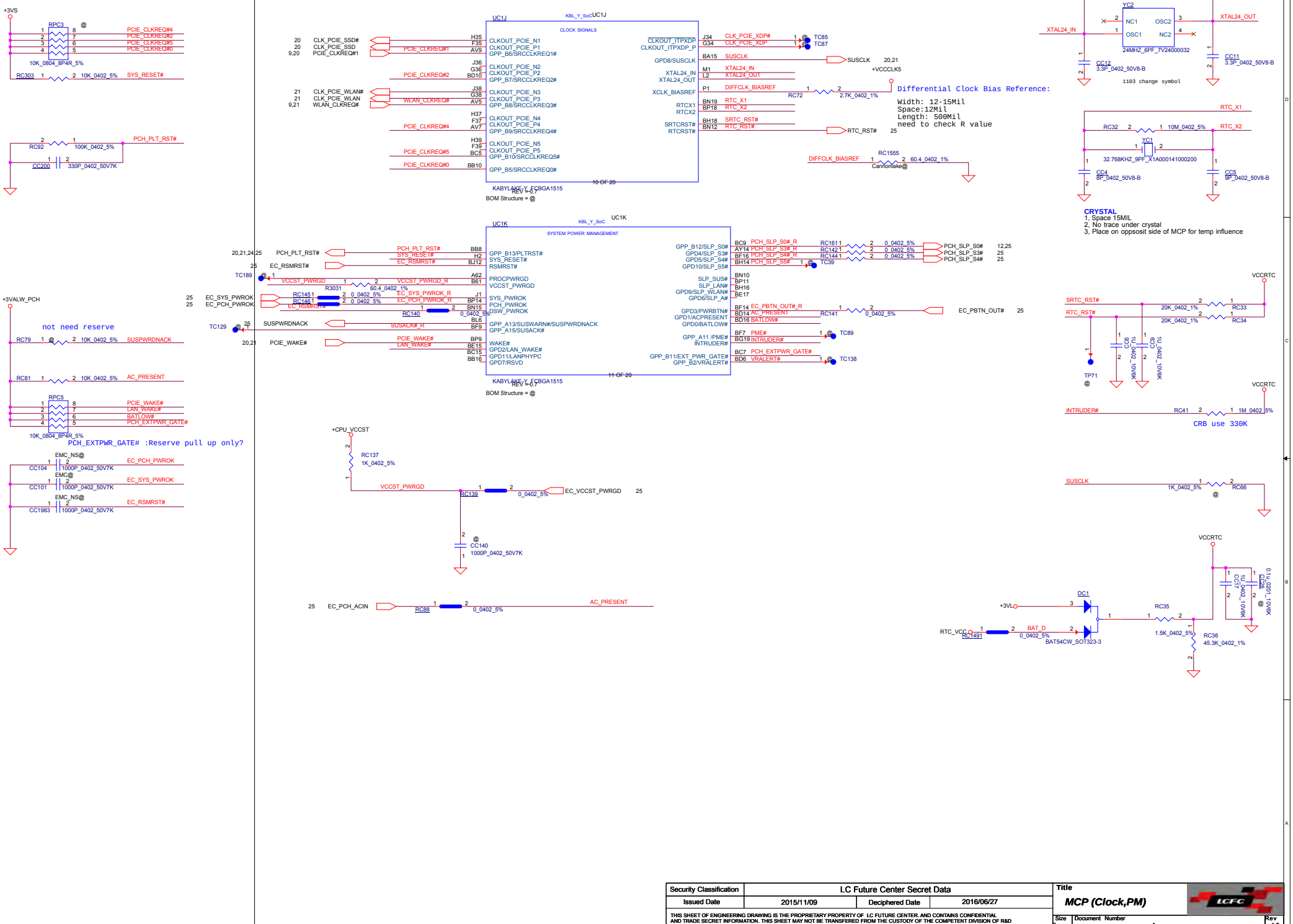
Title	MCP (RTC&AUDIO&SATA&S		
Size C	Document Number Miray-K		Rev 1.0
Date: Thursday, June 23, 2016	Sheet 7	of	38



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Title: **MCP (Clock,PM)**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 8 of 38

The signal has a weak internal pull-down.
0 = Disable " No Reboot" mode. (Default)
1 = Enable " No Reboot" mod

The signal has a weak internal pull-down.
0 = boot from SPI. (Default)
1 = enable boot to LPC,

WLAN

SSD

SSD

Impedance Compensation Inputs

Width 12~15Mil
Space >12Mil
Length 500Mil

USB3.0 stand port

USB3.0 stand port

camera

BT

G Sensor
Light sensor

sensor debug hooks

Sensor

touch panel

touch pad

GPIO Mapping

GroupA/B/C/D/E/G -- Usued for 3.3V power plane
GroupF-Used for 1.8V Power Plane

I2C Mapping

GroupC -- Usued for 3.3V power plane
GroupF-Used for 1.8V Power Plane

BOARD_ID table

BOARD_ID2	BOARD_ID1	BOARD_ID0	DRAM
0	0	0	4G SK HYNIX
0	0	1	4G MICRON
0	1	0	4G SAMSUNG
0	1	1	8G SK HYNIX
1	0	0	8G MICRON
1	0	1	8G SAMSUNG
1	1	0	
1	1	1	

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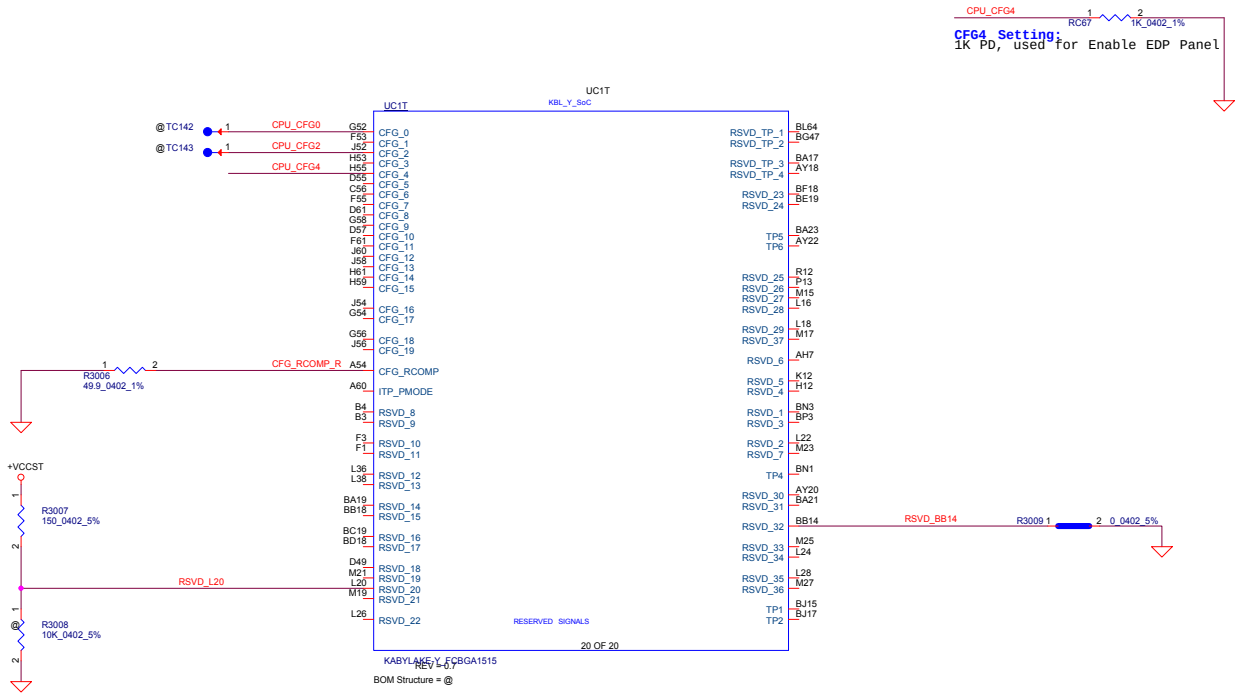
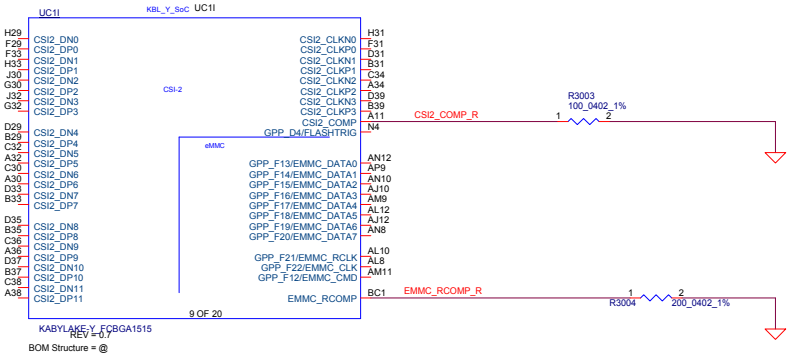
Title: MCP (GPIO,USB,PCIE)

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 9 of 38





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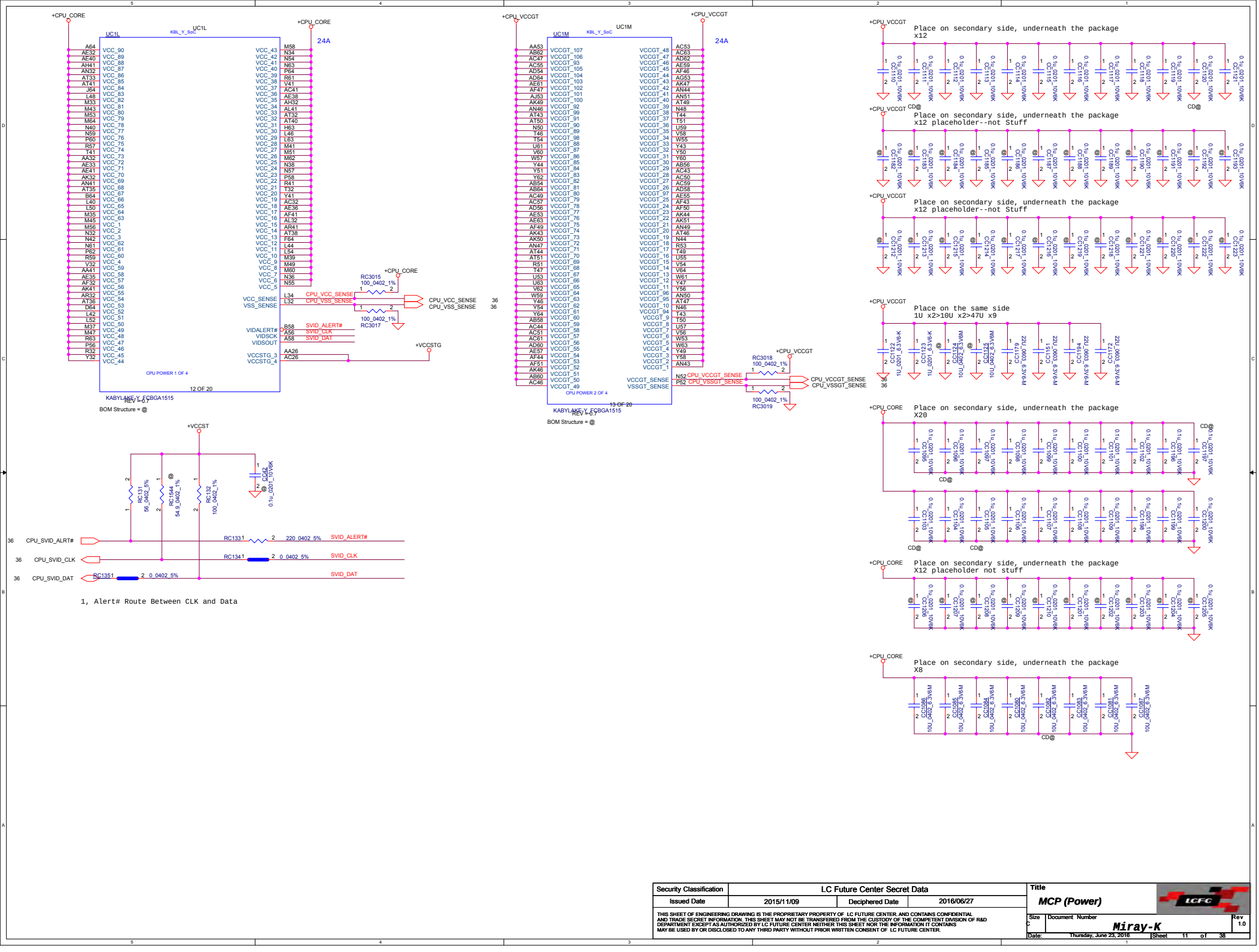
Title		
MCP (OTHER)		
Size: C	Document Number: Miray-K	Rev: 1.0
Date: Thursday, June 23, 2016	Sheet 10 of 38	



1, Alert# Route Between CLK and Data

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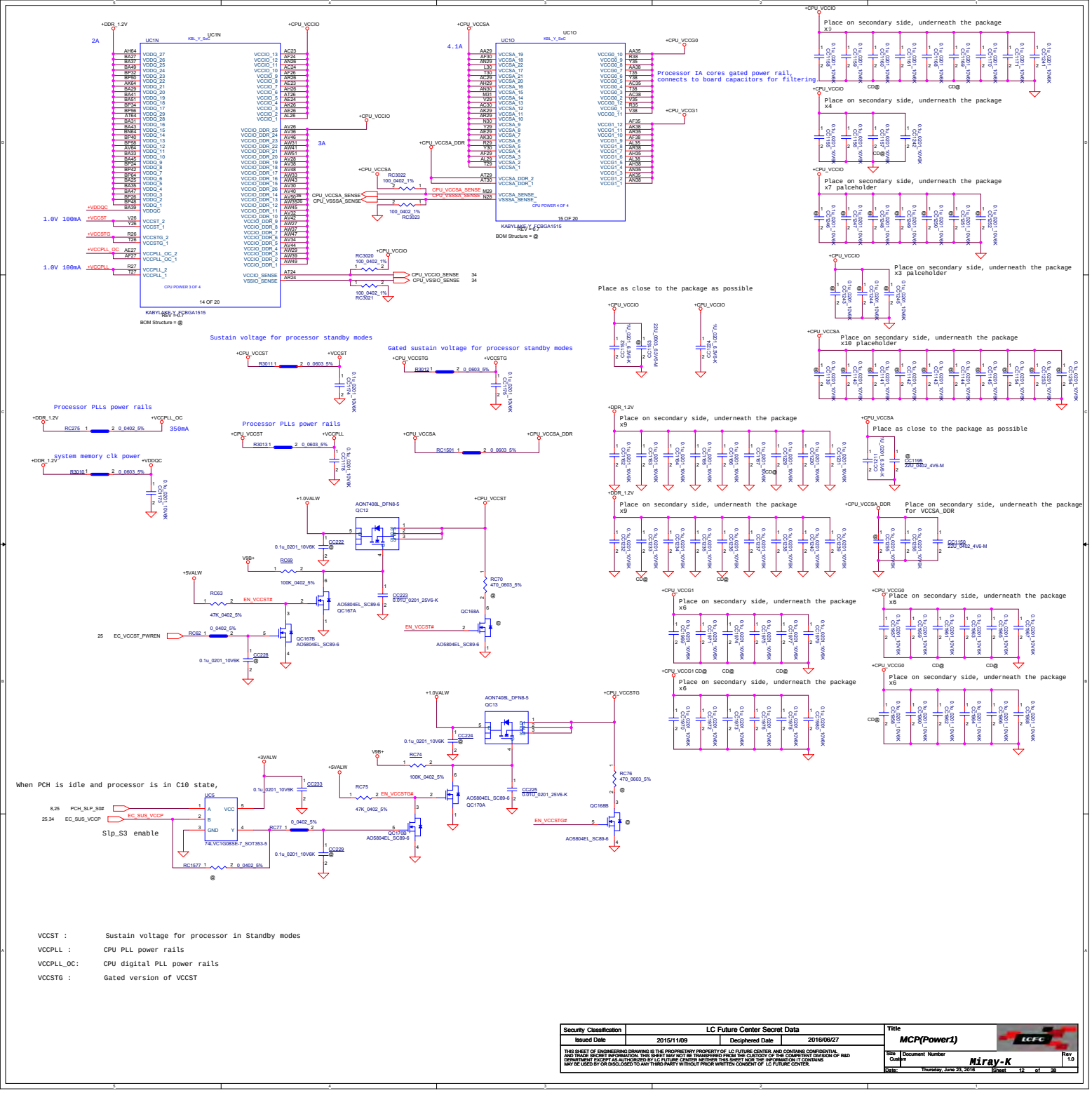
Title: **MCP (Power)**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 11 of 38



VCCST : Sustain voltage for processor in Standby modes

VCCPLL : CPU PLL power rails

VCCPLL_OC: CPU digital PLL power rails

VCCSTG : Gated version of VCCST

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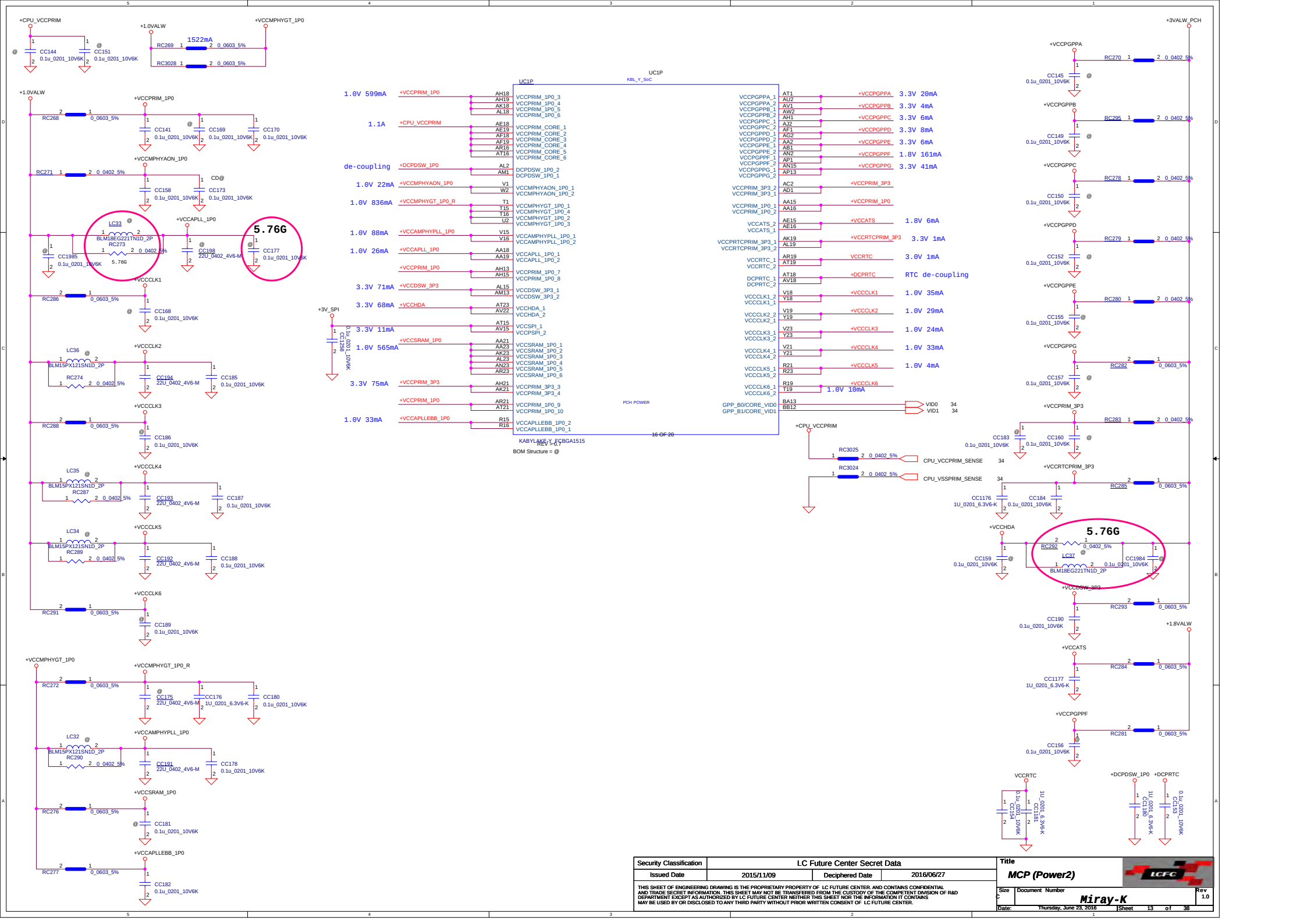
Title: MCP(Power1)

Size: Custom | Document Number: Miray-K | Rev: 1.0

Date: Thursday, June 23, 2016 | Sheet 12 of 38



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Issued Date	2015/11/09	Deciphered Date	2016/06/27

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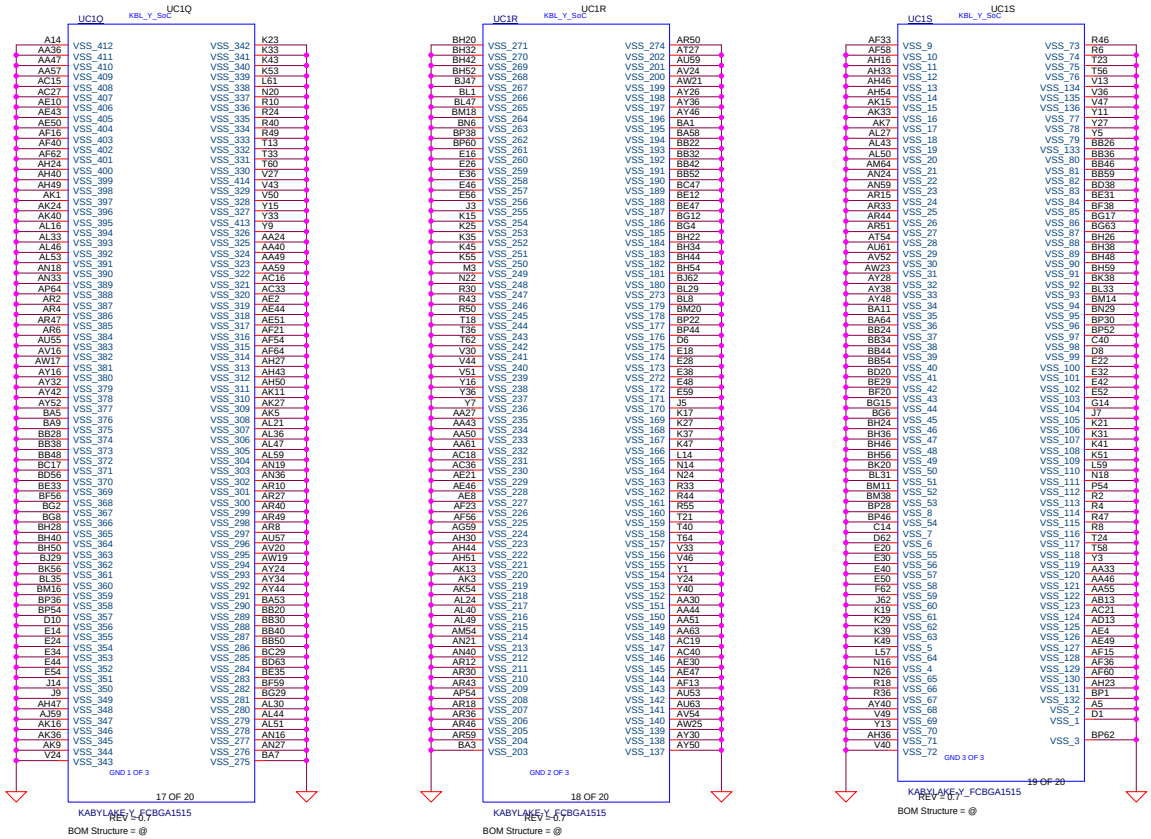
Title: **MCP (Power2)**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 13 of 38

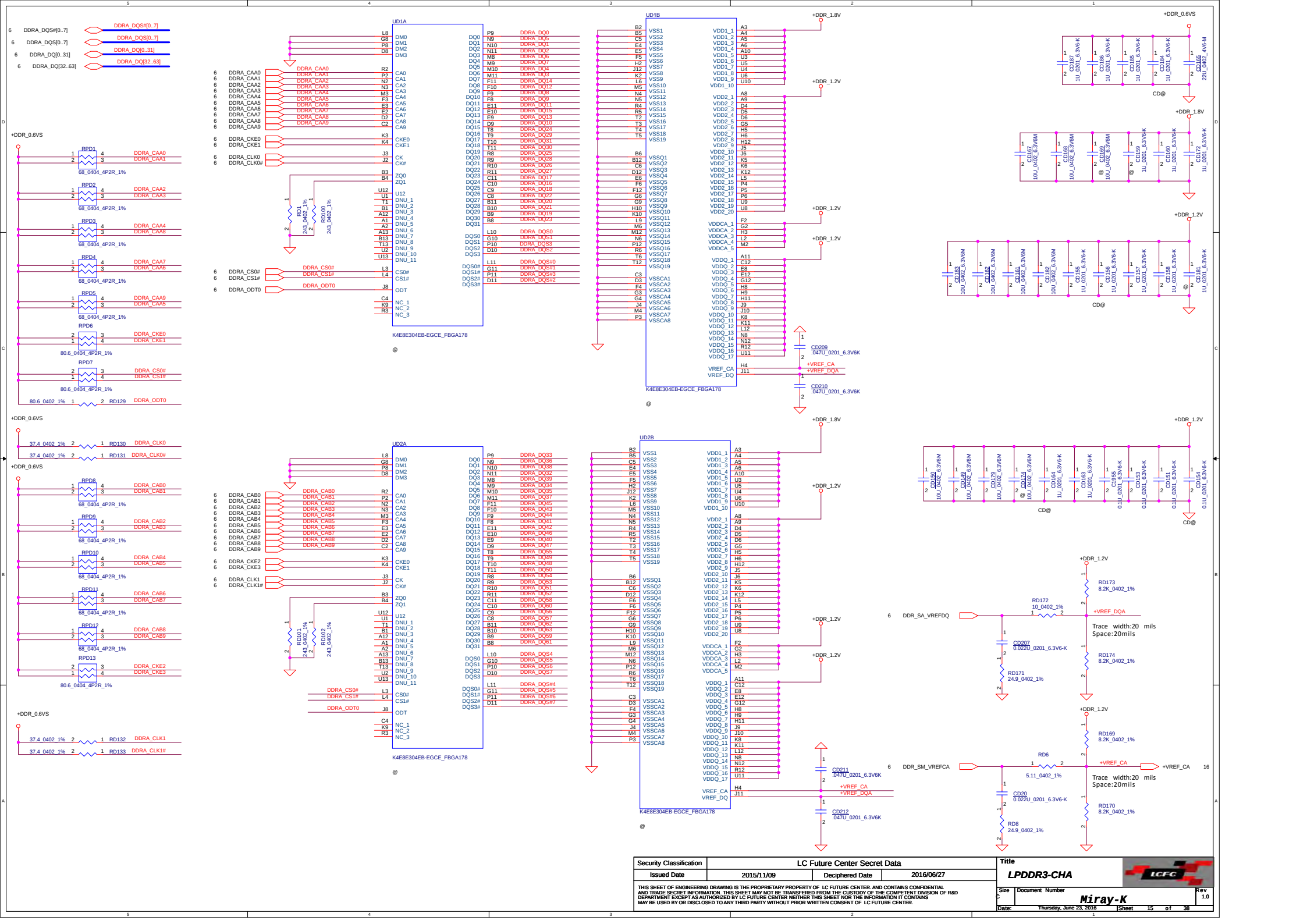


Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: MCP (VSS)

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 14 of 38



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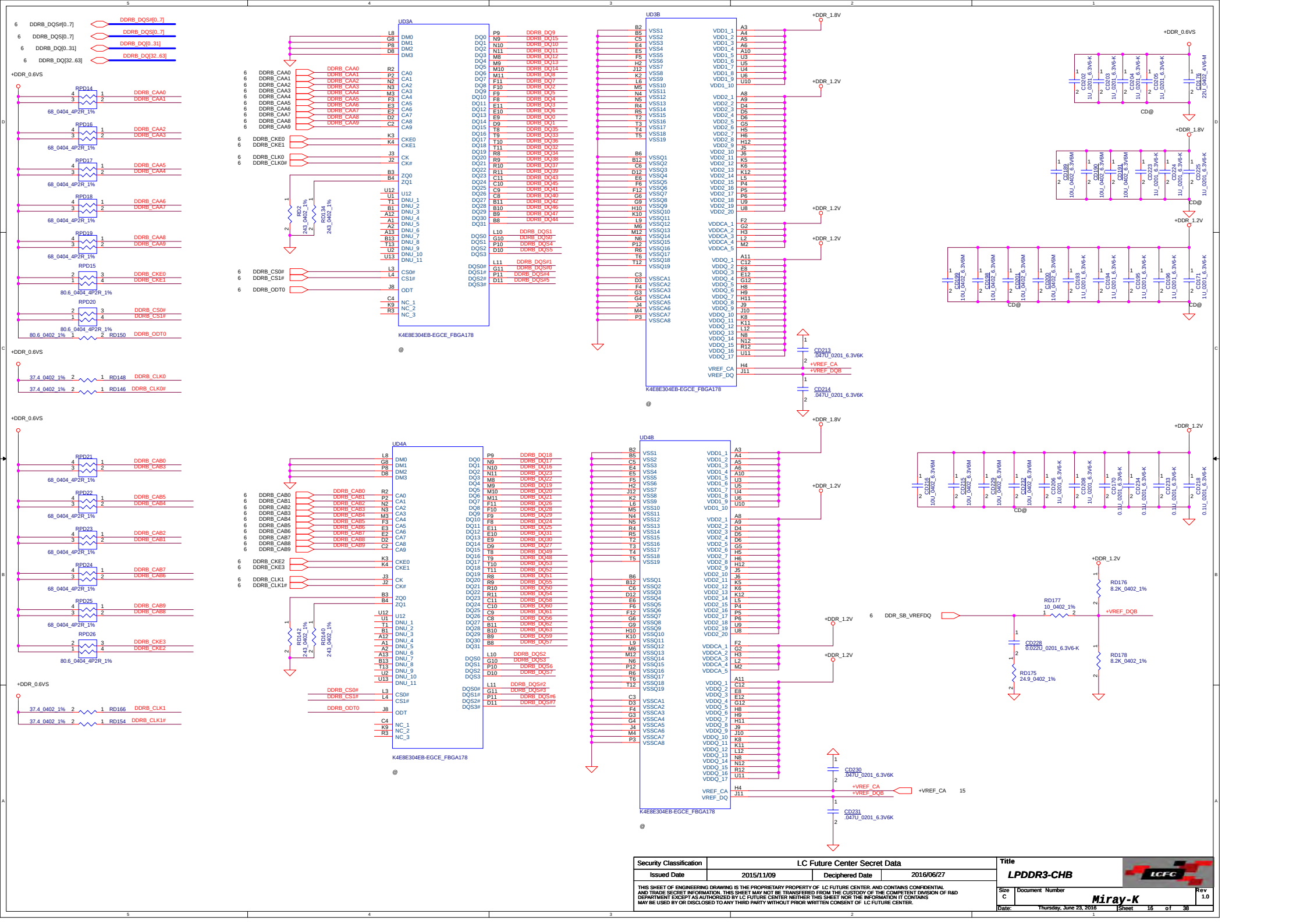
Title: **LPDDR3-CHA**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 15 of 38



Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

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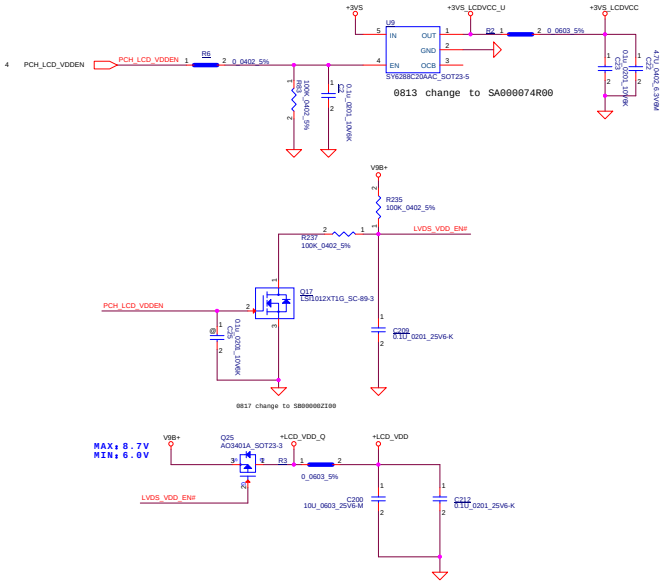
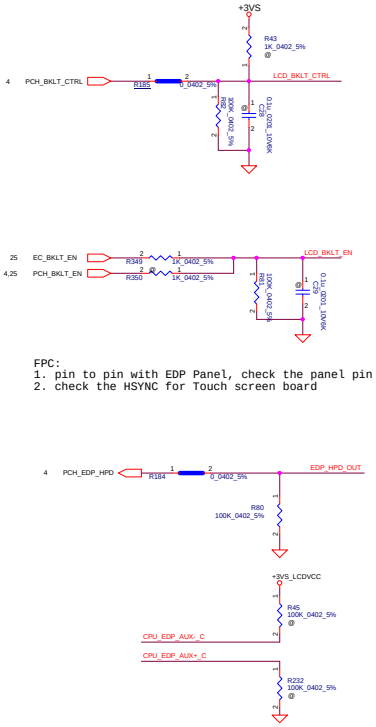
Title: **LPDDR3-CHB**

Size	Document Number	Rev
C	Miray-K	1.0

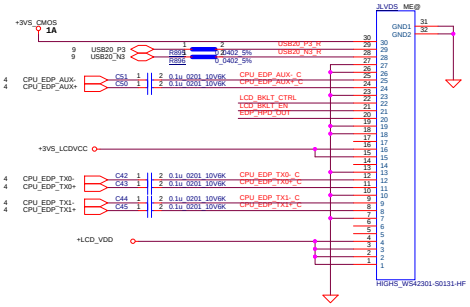
Date: Thursday, June 23, 2016 Sheet 16 of 38

EDP Panel



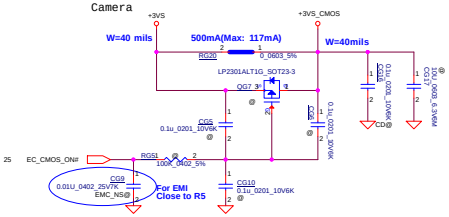


FPC:
1. pin to pin with EDP Panel, check the panel pin definition
2. check the HSYNC for Touch screen board



1106 symbol update

Camera



NOTE

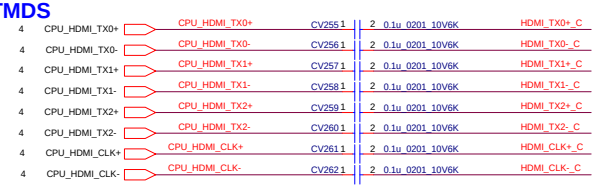
1. AC 19V/DC 8.2V
2. AO5800E for VDS concern
3. R235, R237 for VGS concern
4. C200 for voltage concern

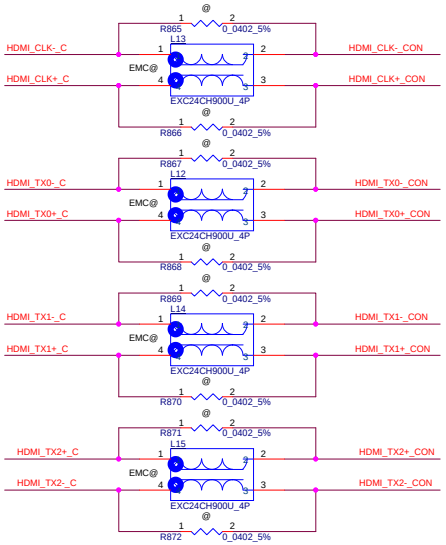
Reserve for other function

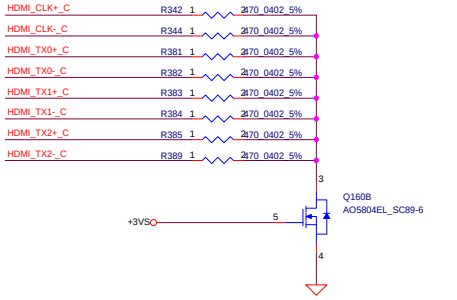
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title	LCD		
Size	Document Number		Rev
Custom	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet 17 of 38	

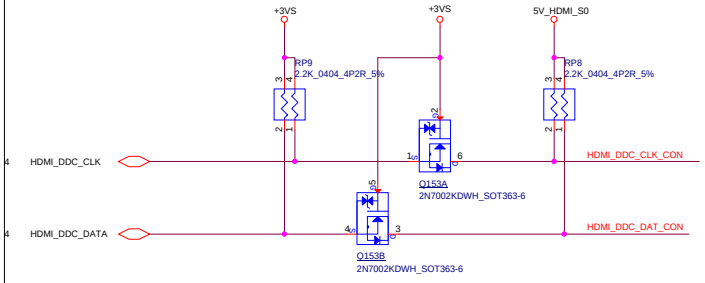
TMDS



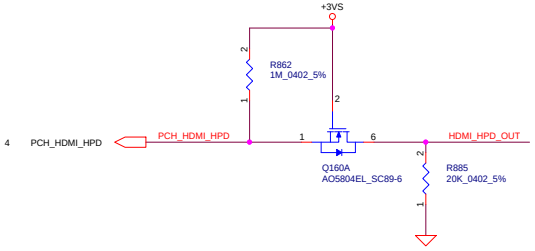




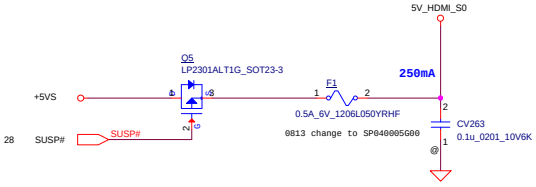
DDC



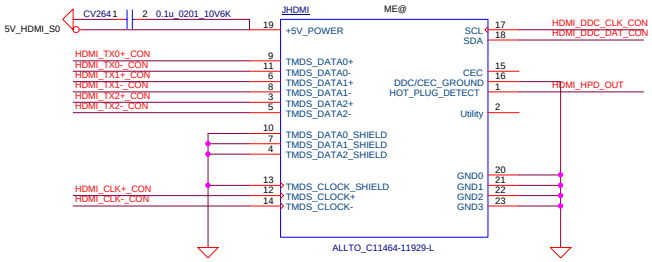
H-PLUG



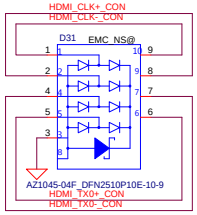
CONN

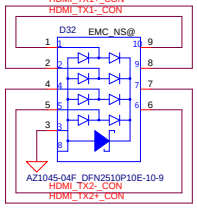


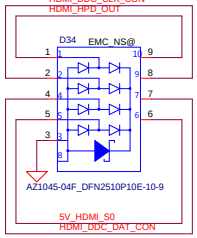
HDMI Type D



0906 change new sysmbol



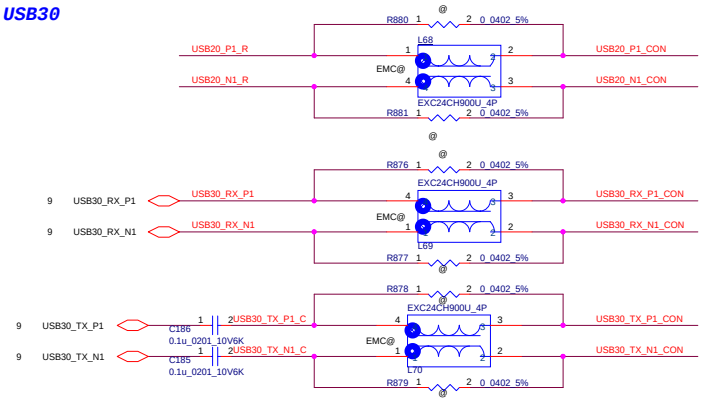


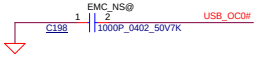


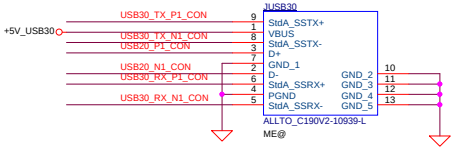
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title	HDMI		
Size	Document Number		Rev
C	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet	18 of 38

USB30

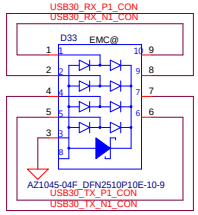


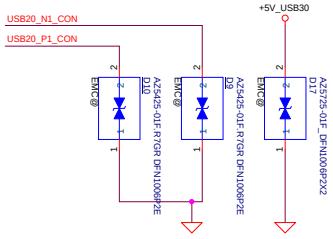




1105 change new sysmbol

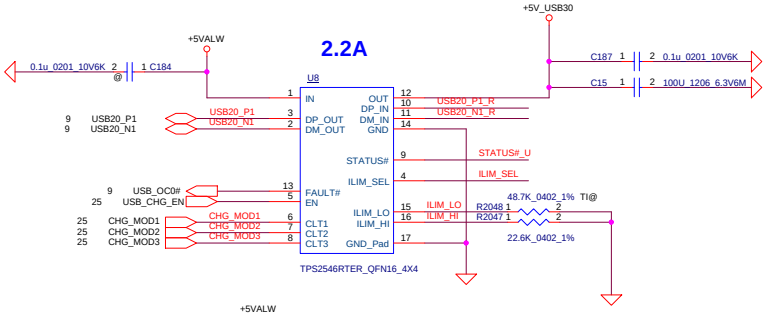
USB type A

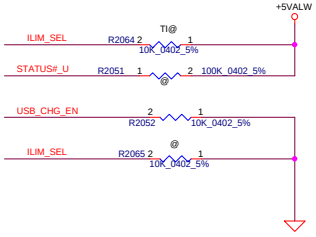




2016/04/20:USB 2.0 port TVS ref location
D9 & D10 change to SC40000651O:
SC400006510 S DIO_ESD AZ5425-01F.R7GR DFN1006P2E
2016/05/10:USB 3.0 port TVS ref location
D17 change to SC400008K00
S DIO_ESD AZ5725-01F.R7GR DFN1006P2X

USB charger



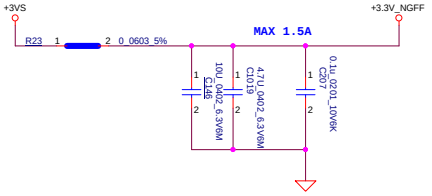


	pin number	6	7	8	4
	pin name	Ctl1	Ctl2	Ctl3	ILM_SEL
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

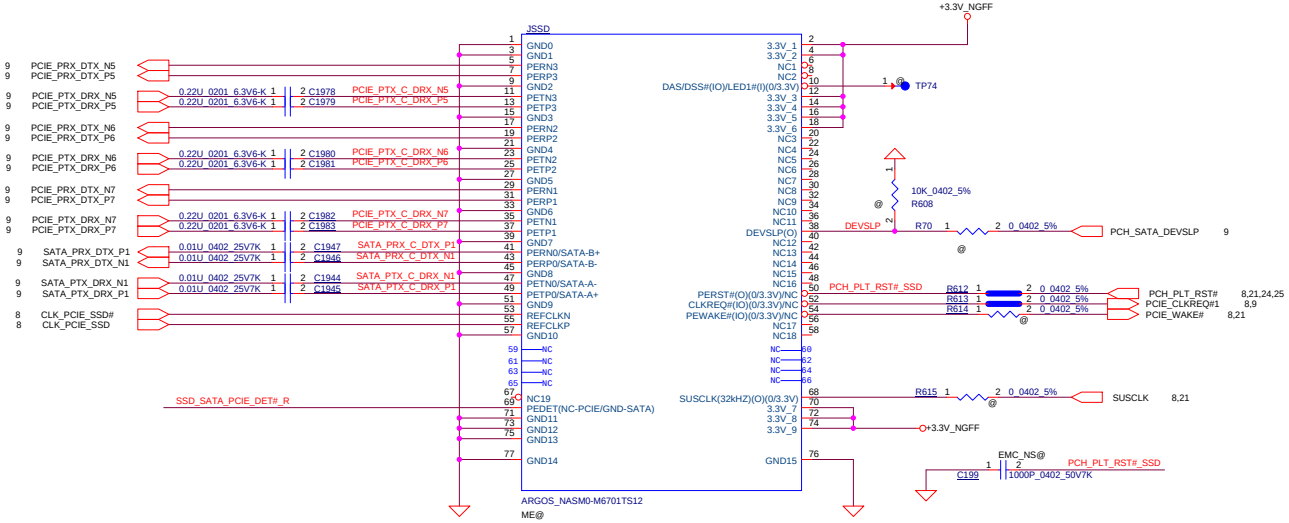
Title	SSD&USB30 Type C		
Size C	Document Number	Miray-K	Rev 1.0
Date:	Thursday, June 23, 2016	Sheet	19 of 38

SSD

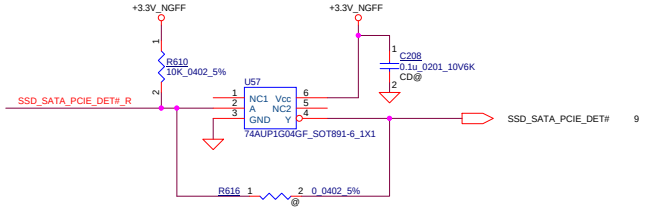


SSD	C1978	C1979	C1980	C1981	C1982	C1983	C1947	C1946	C1944	C1945
PCIE	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0ohm SD02800008J	Stuff 0ohm SD02800008J	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800
SATA	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.22uF SE00000X800	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J	Stuff 0.01uF SE075103K8J

Default stuff SATA option
SDV rework to PCIE option and test SATA/PCIE signal and SSD



0827 symbol update



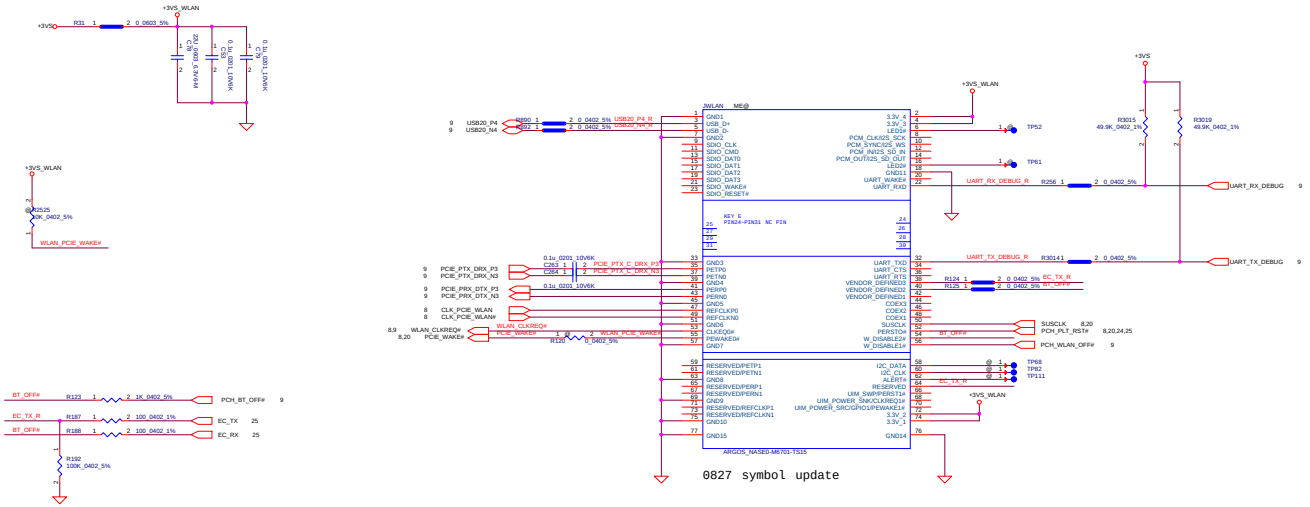
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: **SSD&USB30 Type C**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 20 of 38

Mini Card(WLAN/WiMAX)

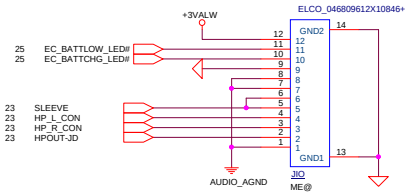


0827 symbol update

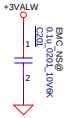
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL	H	L
PCH_BT_ON#	L	H

Security Classification	LC Future Center Secret Data		Title: CONN(WLAN&KB&PWRBTN)
Issued Date	2015/11/09	Deciphered Date	2016/08/27
Size: D	Document Number: Miray-K		Rev: 1.0
Date: Thursday, June 23, 2016	Sheet: 21 of 38		



0111 symbol update

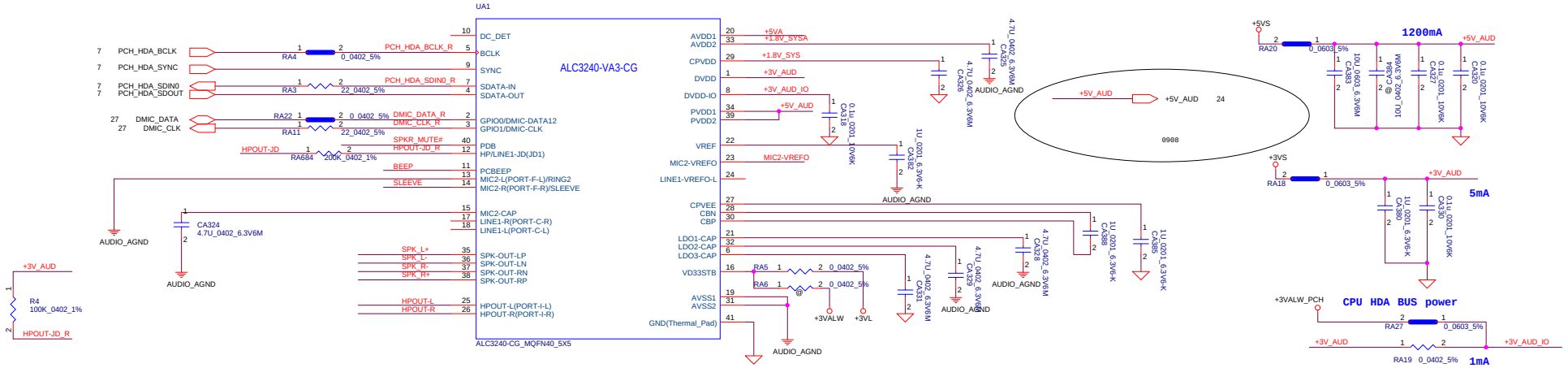


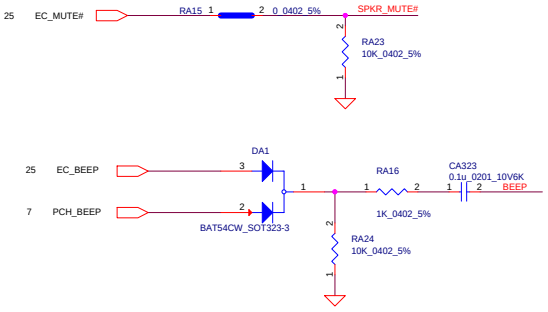
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

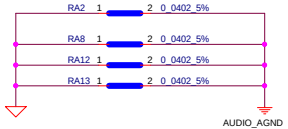
Title: MCU

Size: Custom	Document Number: Miray-K	Rev: 1.0
Date: Thursday, June 23, 2016	Sheet 22 of 38	

CODEC







VD33STB:Power for combo jack depop circuit at system shutdown mode.

AVDD1:Analog power for mixers ,IO ports

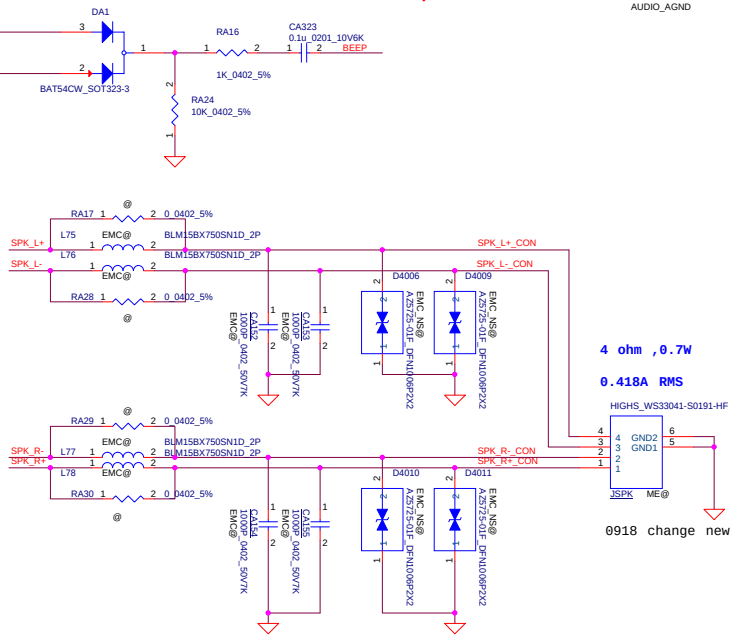
DVDD-IO:Digital power for HDA link

DVDD:Digital power for digital I/0 circuit

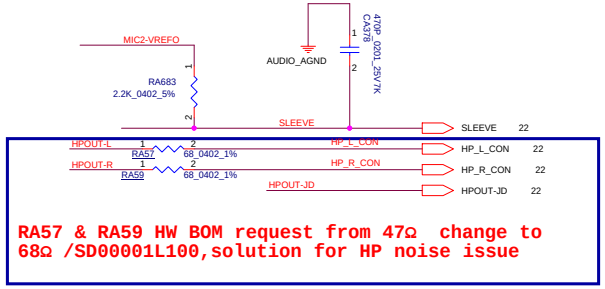
AVDD2:Analog power for DACS ,ADCS

PVDD1,PVDD2:Power supply for full-bridge left and right channel

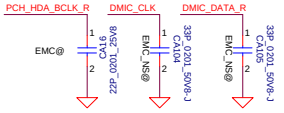
CA381 change to 2.2U_0402_10V



0918 change new sysmbol

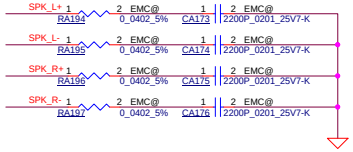


RA57 & RA59 HW BOM request from 47Ω change to 68Ω /SD00001L100,solution for HP noise issue



RA194,RA195,RA196,RA197 will to be changed from 15ohm to 0ohm, for HW SO---->S3 play muisc hang up issue solut i on

Place Close To Codec

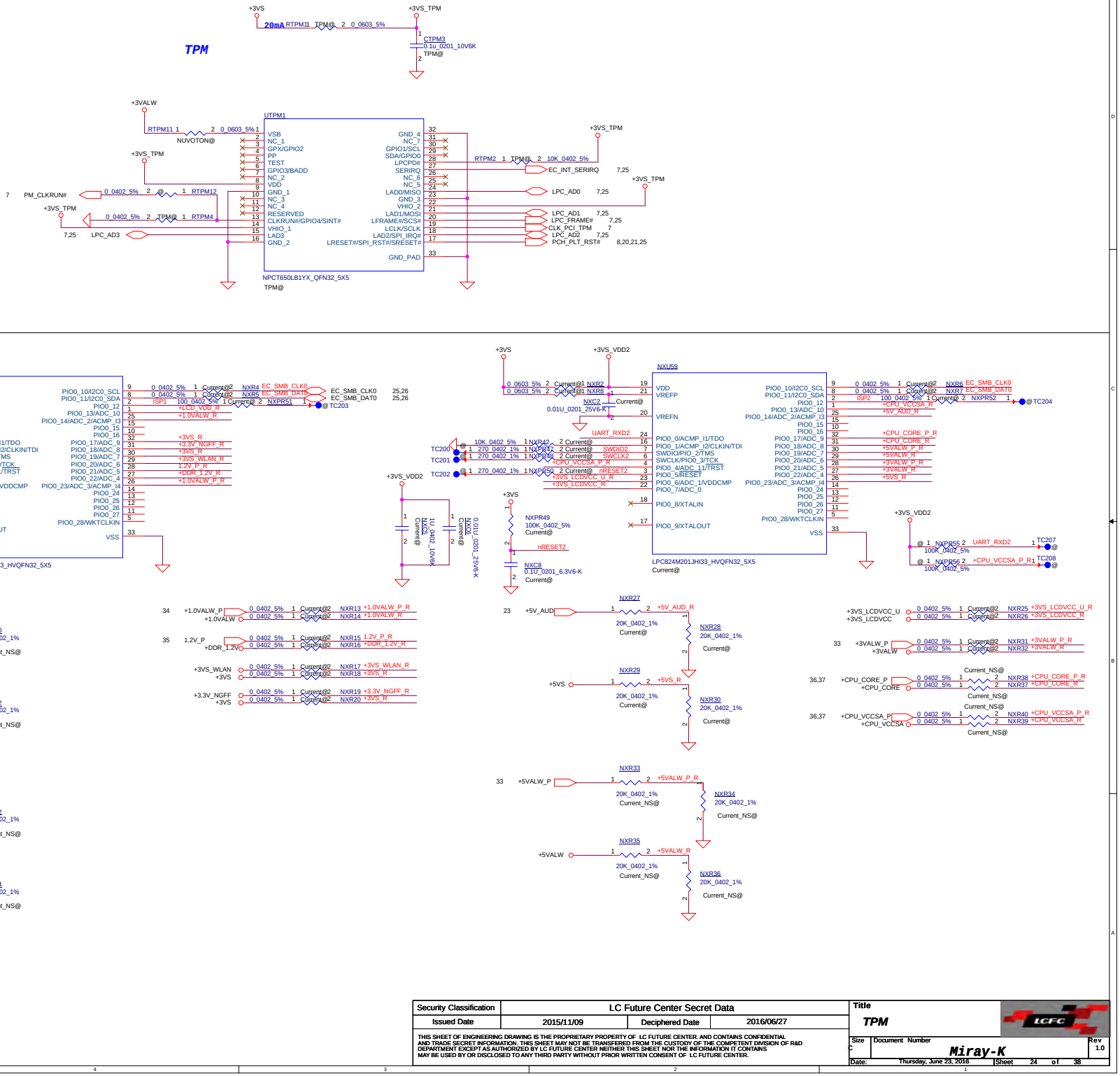


Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title	Size	Document Number	Rev
AUDIO	C	Miray-K	1.0
Date: Thursday, June 23, 2016	Sheet 23 of 38		

	Vendor	PN	Describe
国内	NATIONZ	SA000071N00	S IC Z32H320TC-LPC-T28-233 TSSOP 28P TPM
WW 1.2	Nuvoton	SA00007RJ00	S IC NPCT650LB1WX TSSOP 28P TPM1.2
	Nuvoton	SA00007H110	S IC NPCT650LB1YX QFN 32P DISCRETE TPM
WW 2.0	Nuvoton	SA00007FW00	S IC NPCT650LAAWX TSSOP 28P TPM 2.0

SDV Use WW2.0 Nuvoton
SIV need change to WW1.2 QFN



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Title	TPM		
Size	Document Number		Rev
C	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet	24 of 38

PWR

8396

EC change to 8586 SA00005WC0J
S IC IT8586VG/FX VFBGA128P EMBEDDED CTRL

IT8396

IT8396VG-192-AX_VFBGA128

LPC

PWM

ADC

DAC

PS2

EXTERNAL SERIAL FLASH

SPI Flash ROM

UART

GPIO

Int. K/B Matrix

SM Bus

WAKE UP

Clock

Thermal Sensor

BATT charger

Sensor

EC DSW Signal

For off-line programming the E C code

KSI-6 (pin-H13 --> I2C_DATA)
KSI-7 (pin-G9 --> I2C_CLK)
SMDAT6/GPF3(pin-B16)
SMCLK8/GPF2(pin-A10)

0817 change to SB00000ZI00

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Issued Date	2015/11/09	Deciphered Date	2016/06/27

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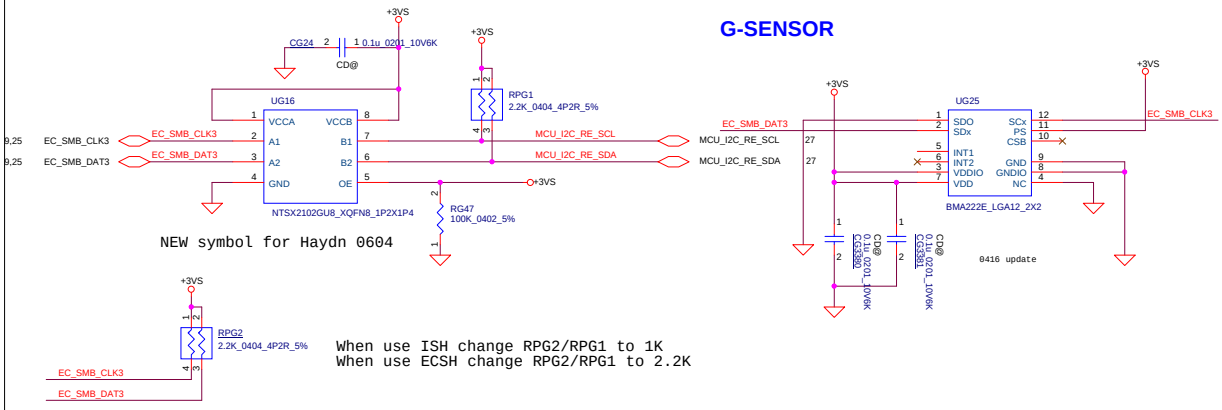
Title: ECIT8396

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, June 23, 2016 | Sheet 25 of 38

Miray-K

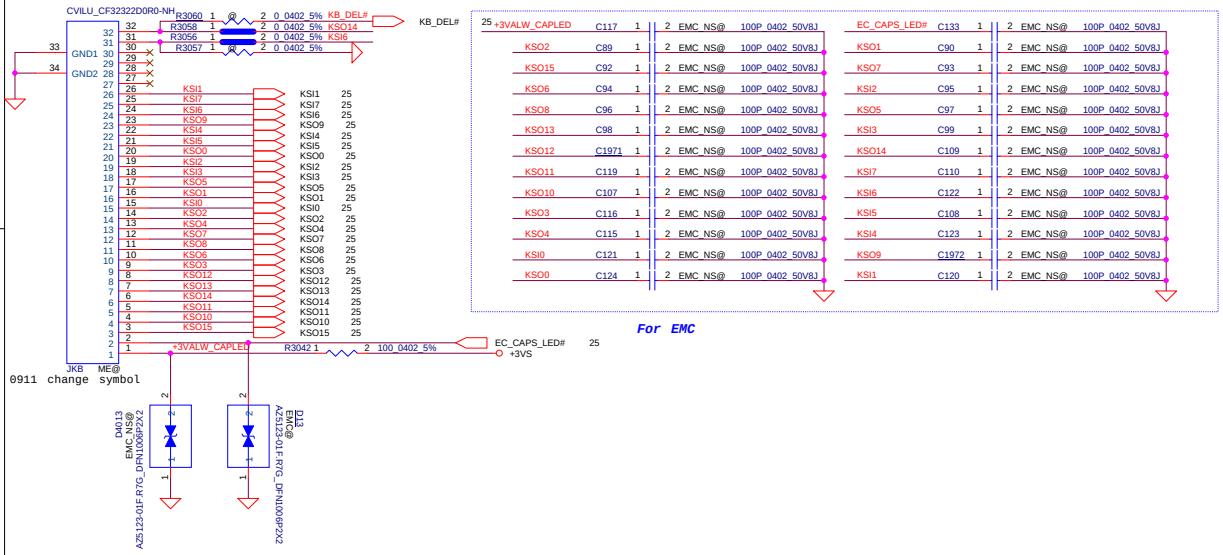
G-SENSOR



NEW symbol for Haydn 0604

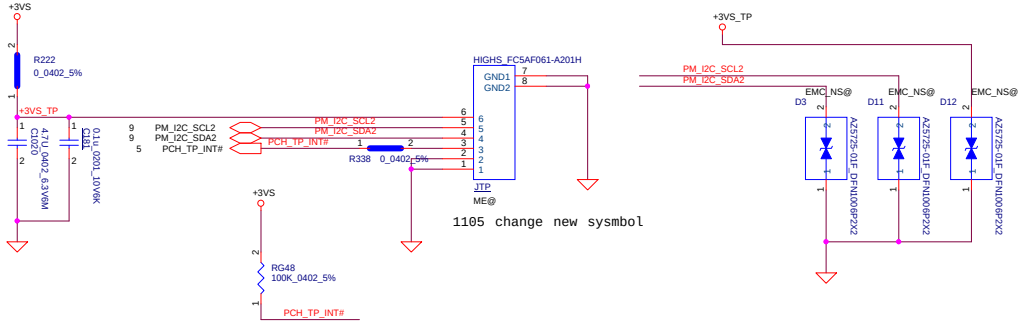
When use ISH change RPG2/RPG1 to 1K
When use ECSH change RPG2/RPG1 to 2.2K

Keyboard Connector



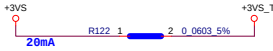
0911 change symbol

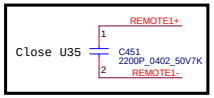
Touch Pad Connector



1105 change new sysmbol

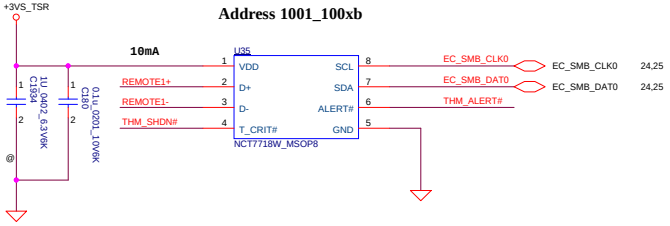
THM Sensor

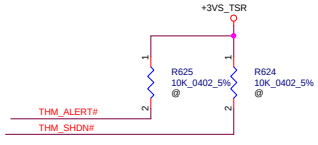


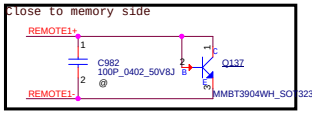


Nuvoton thermal sensor

Address 1001_100xb







REMOTE1+/-:
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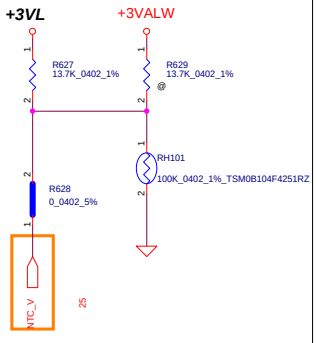
Trace length:<8"



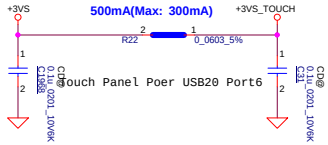
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

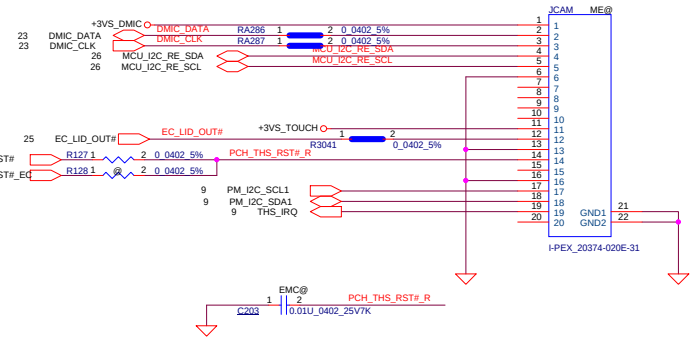
Title: CONN(THM&FAN&RTN&SPK)

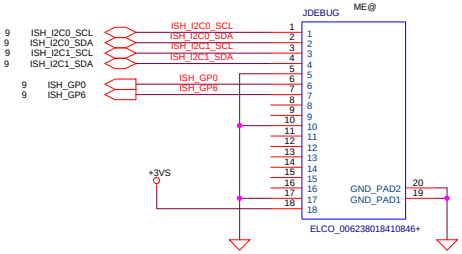
Size	Document Number	Rev
C	Miray-K	1.0

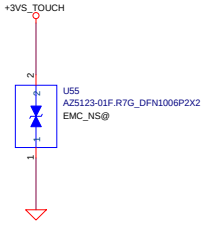
Date: Thursday, June 23, 2016 Sheet 26 of 38

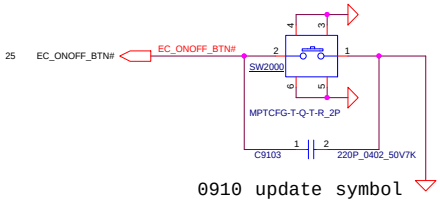
Touch



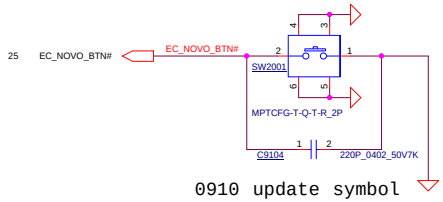






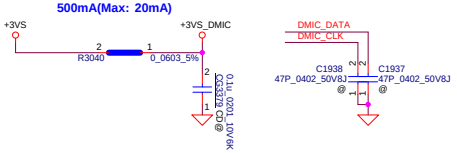


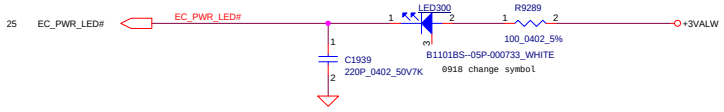
0910 update symbol

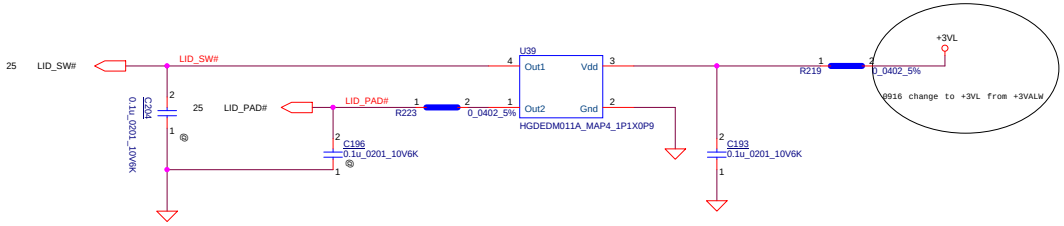


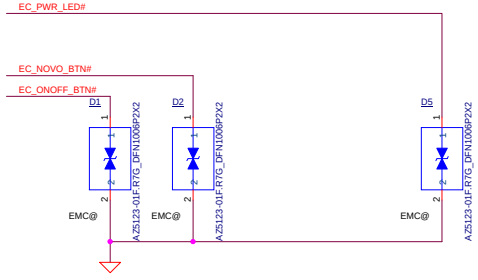
0910 update symbol

DMIC



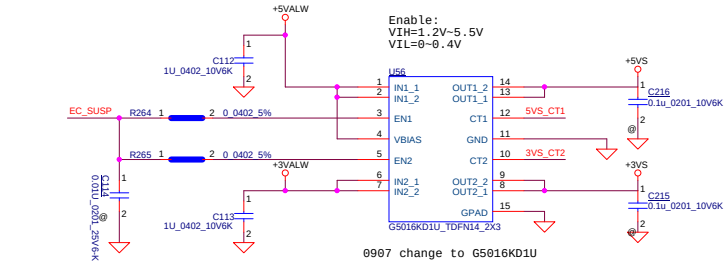


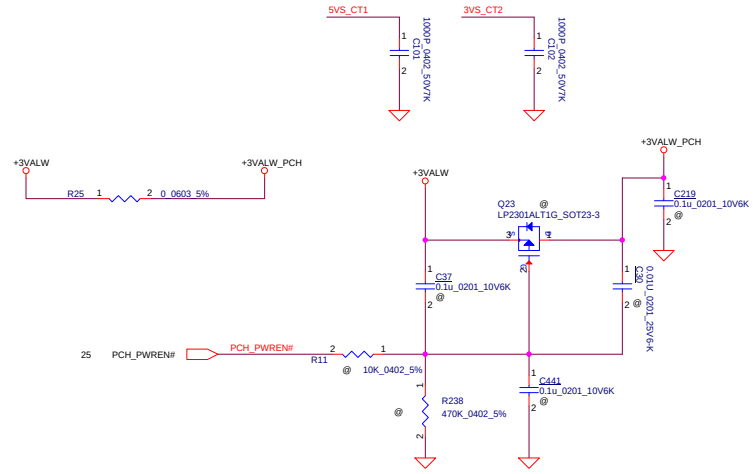


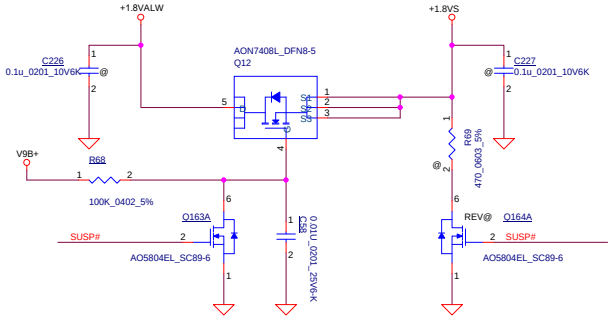


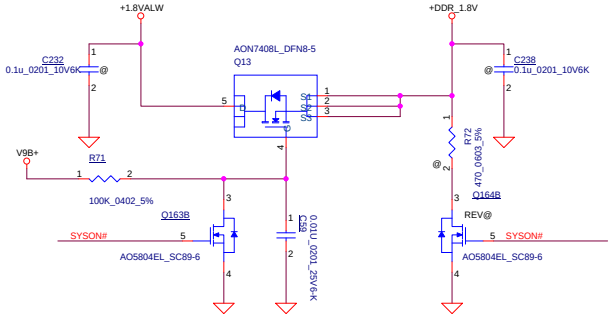
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

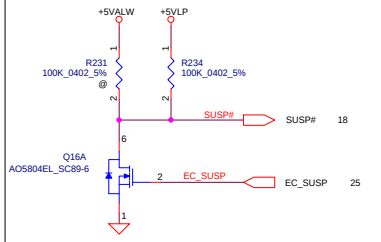
Title	Screw and Hole		
Size	Document Number		Rev
C	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet	27 of 38

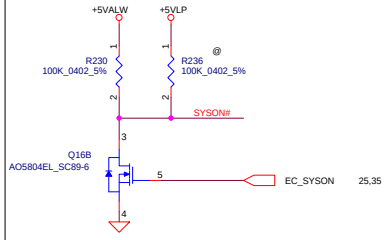


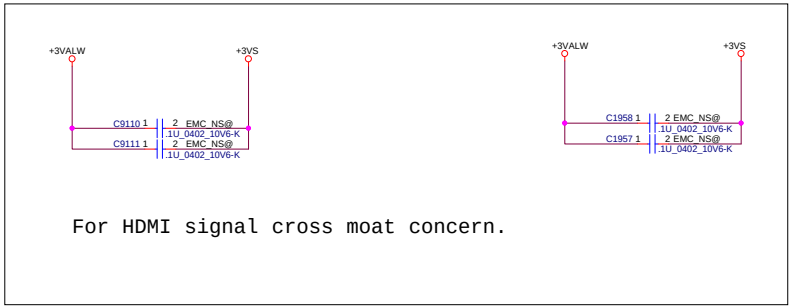


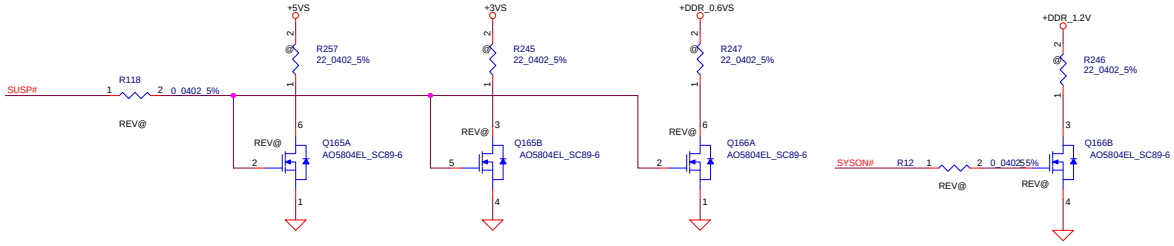












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Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: **POWER SWITCH**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 | Sheet 28 of 38

PAD_C7P0

PAD_C6P0D2P3

PAD_CT5P0D1P5

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title	Screw and Hole		
Size	Document Number		Rev
A		Mray-K	1.0
Date:	Thursday, March 24, 2016	Sheet	45 of 45

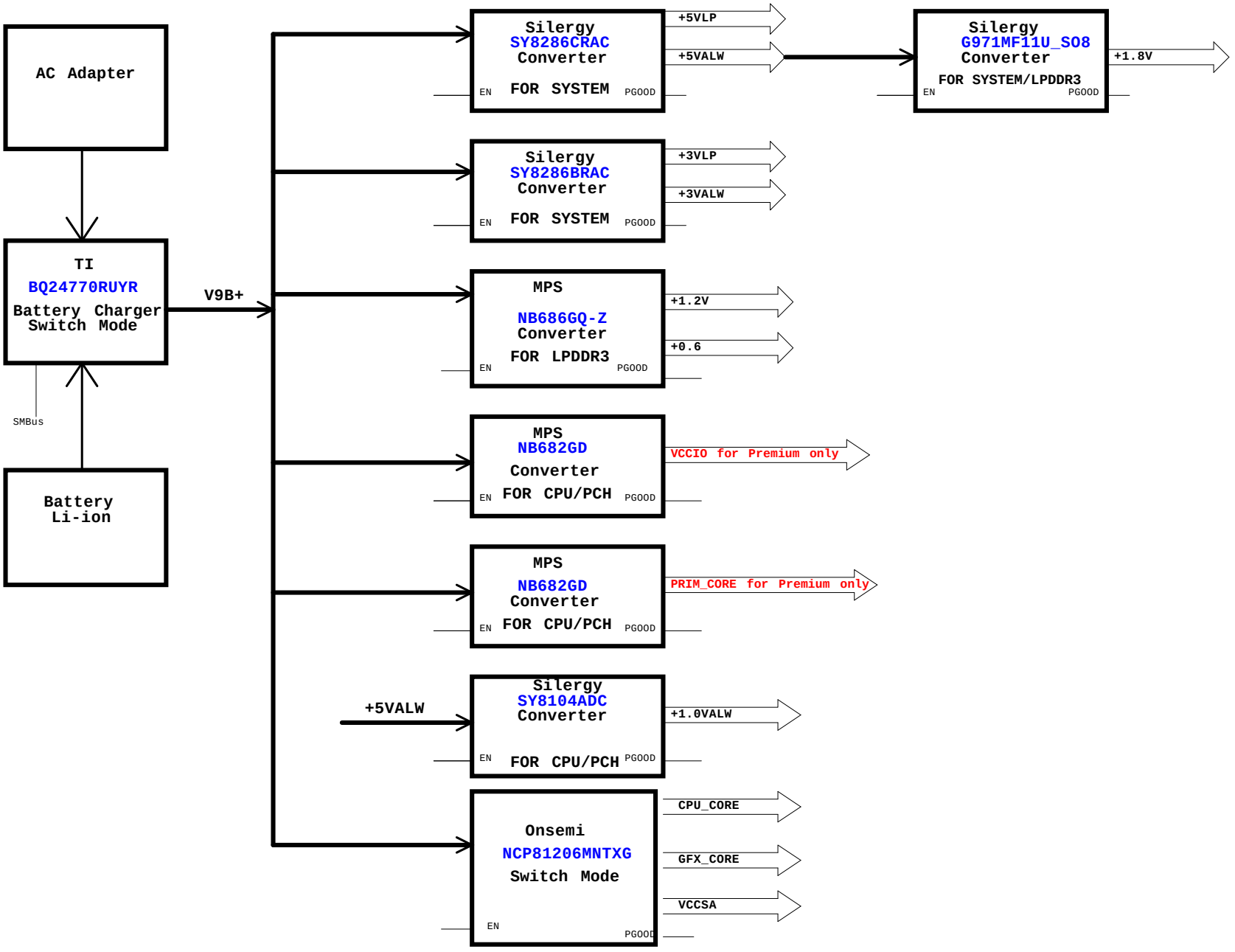
8.31
Follow DXF update Hole

Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: *HW_Change_List*

Size	Document Number	Rev
C	*Miray-K*	1.0

Date: Thursday, June 23, 2016 Sheet 30 of 38



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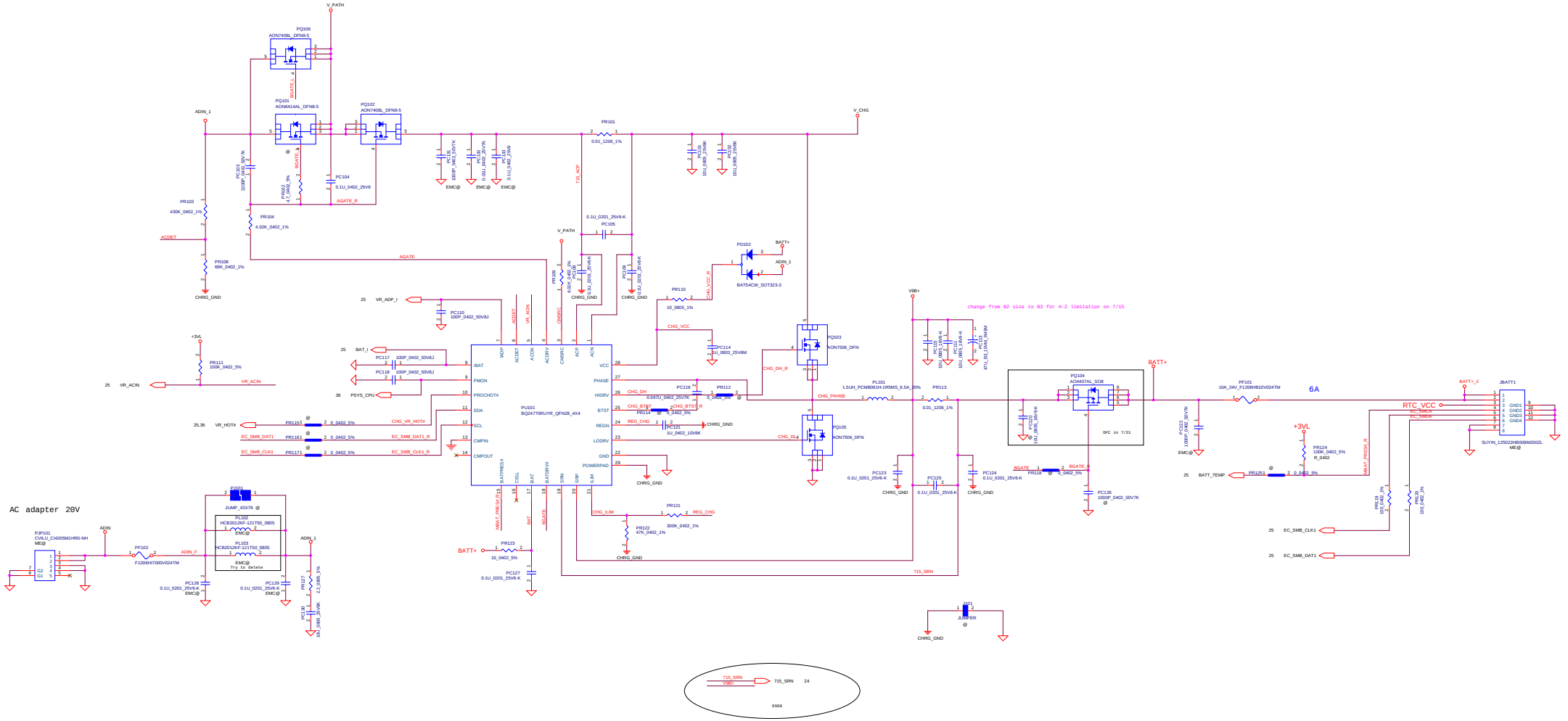
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title	NVDC Charger		
Size	Document Number		Rev
C	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet	31 of 38



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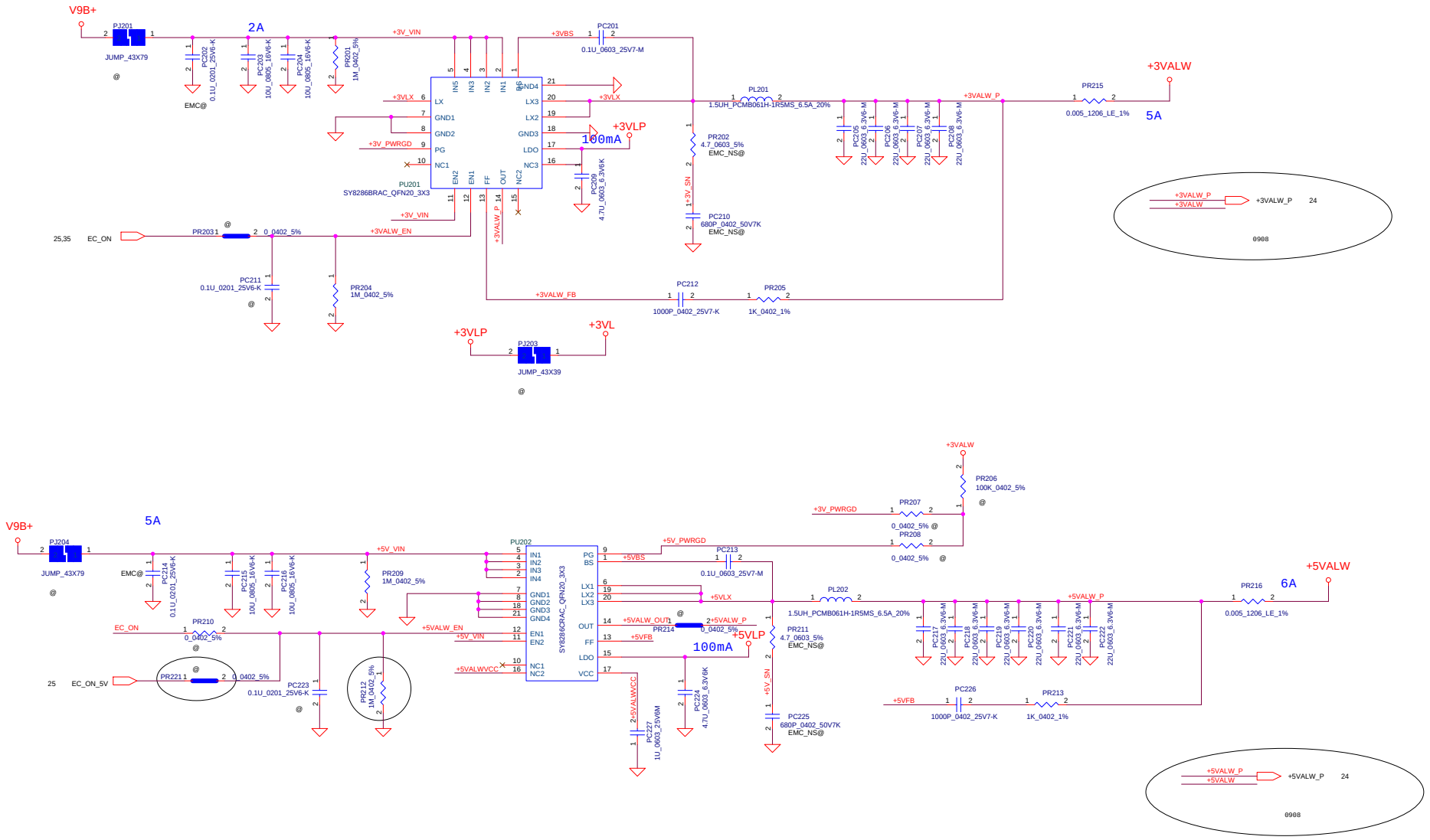
Title	PWR_NVDC Charger		
Size	Document Number		Rev
D	Miray-K		1.0
Date:	Thursday, June 23, 2016	Sheet	32 of 38



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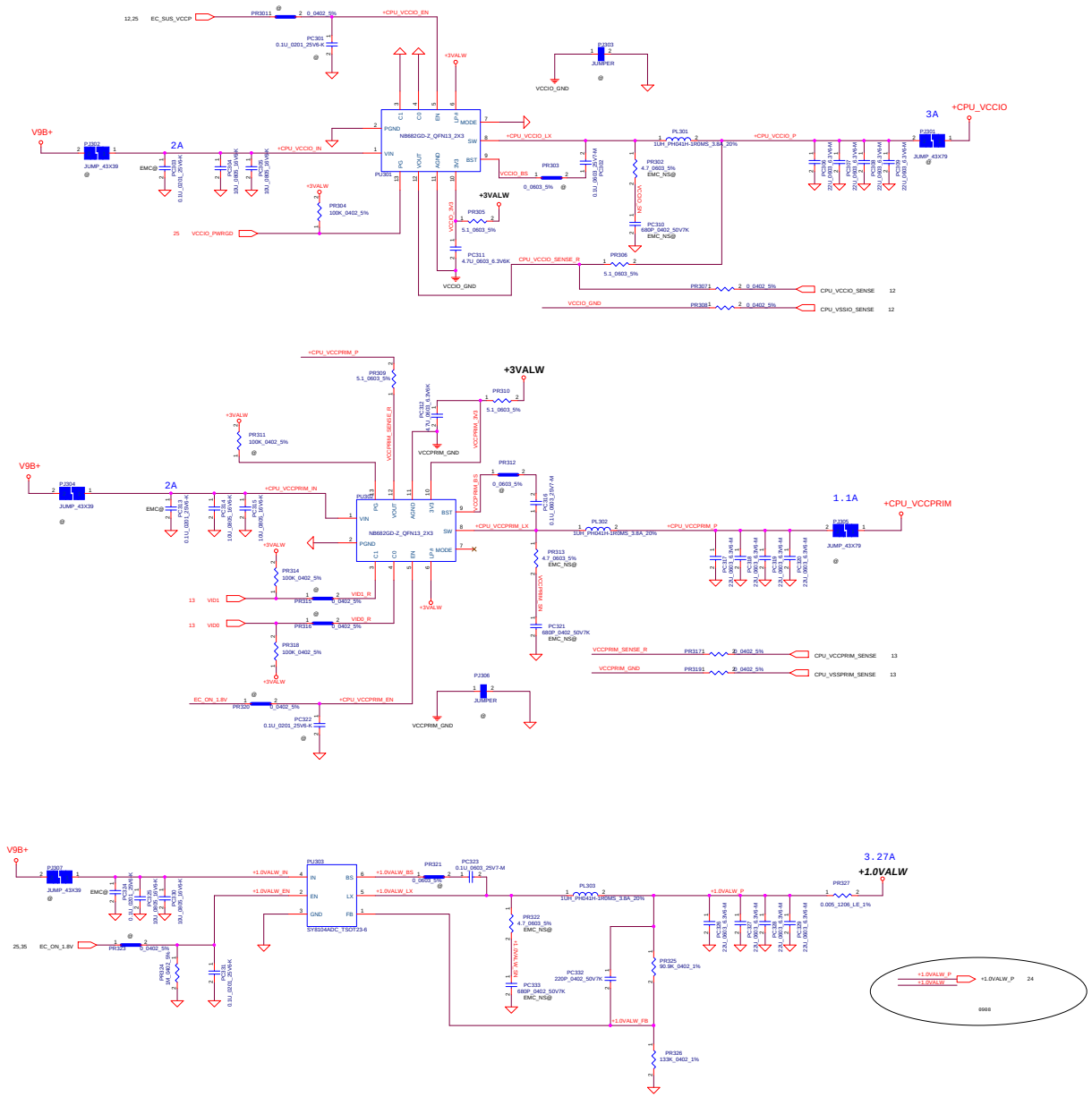
Title: **3VALWP/5VALWP**

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 33 of 38



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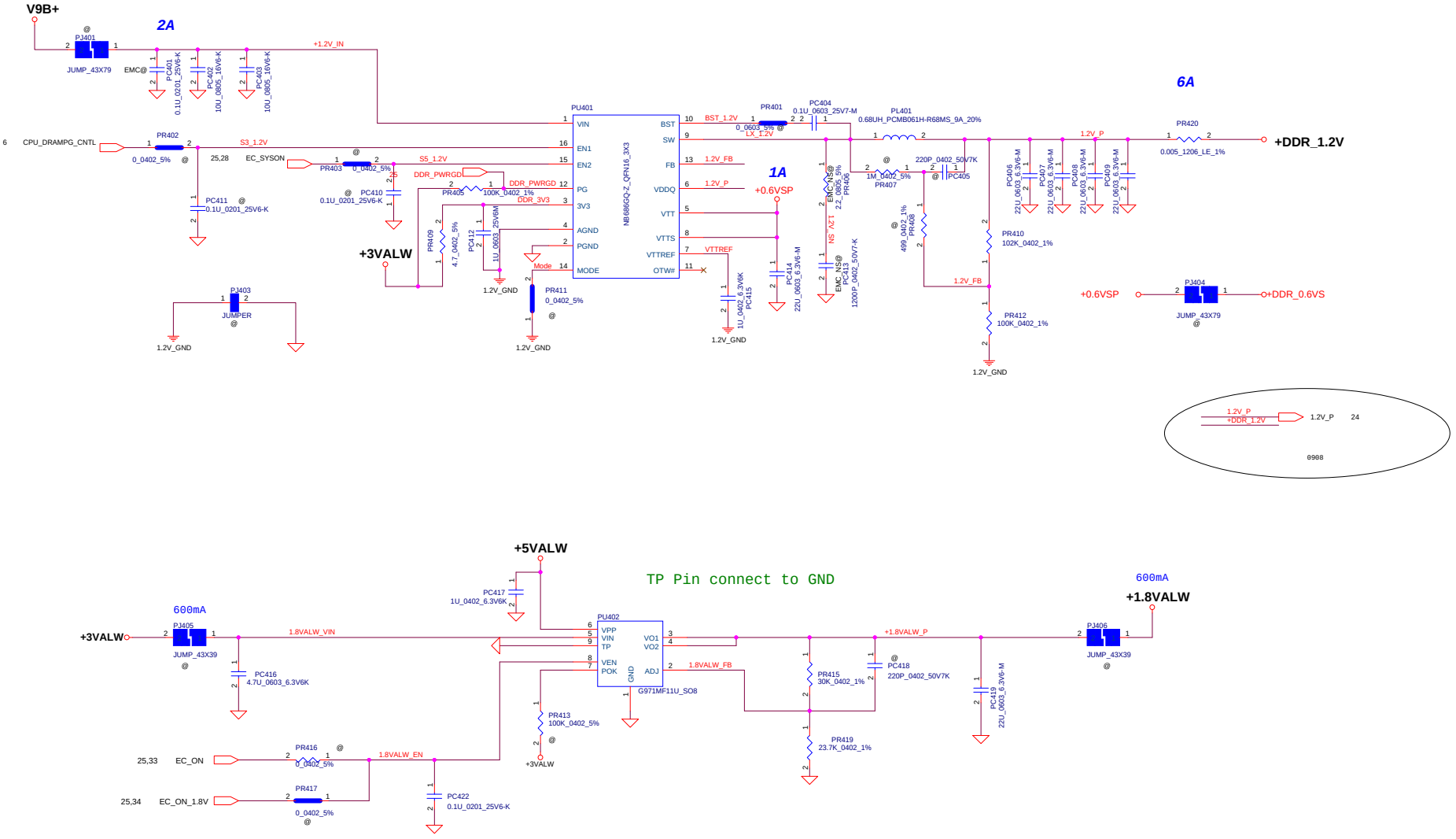
Title: 1.35VS/+0.675VS

Size	Document Number	Rev
D	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 34 of 38



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Issued Date	2015/11/09	Deciphered Date	2016/06/27

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Size	Document Number		Rev
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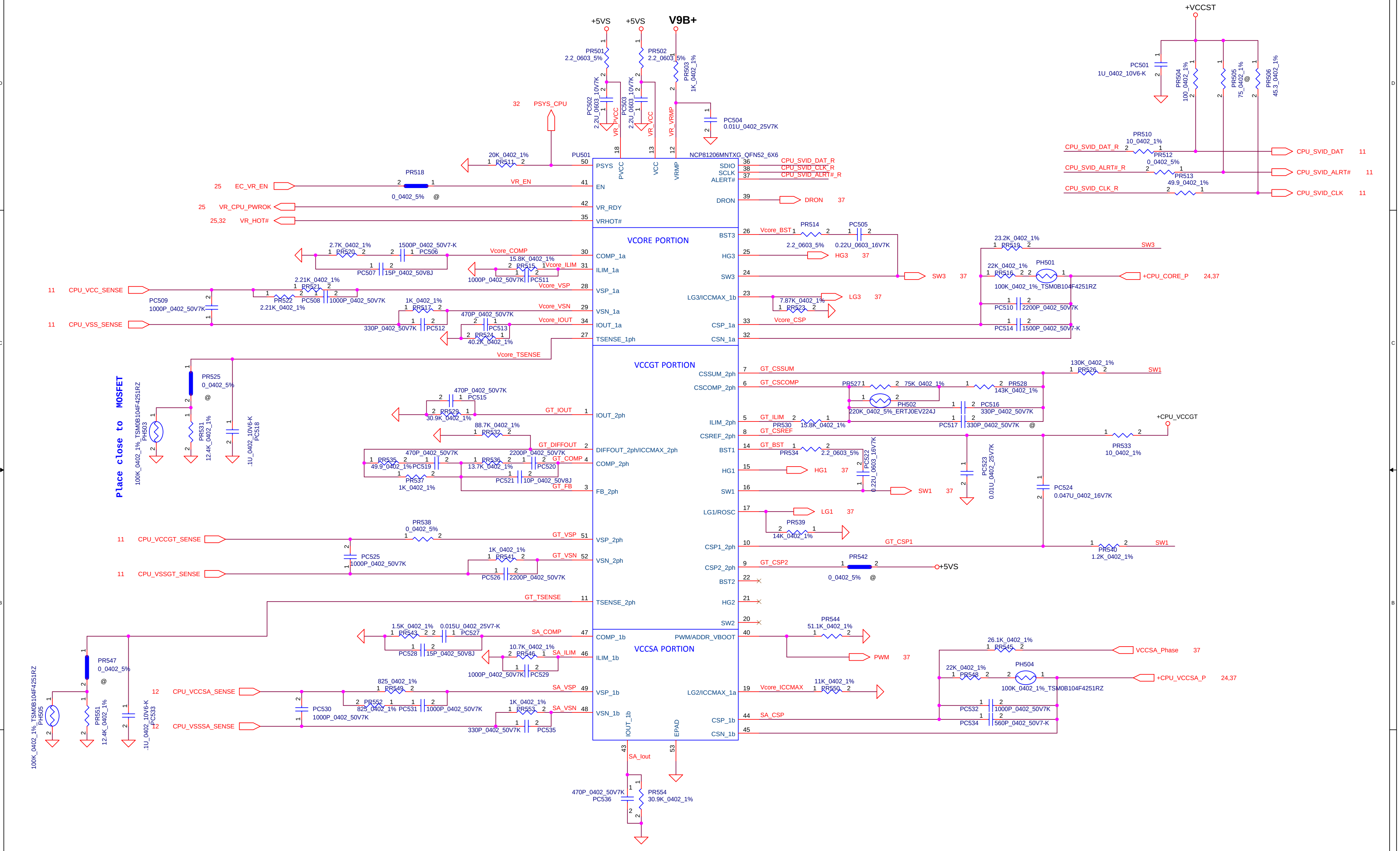
Date:	Thursday, June 23, 2016	Sheet	35 of 38



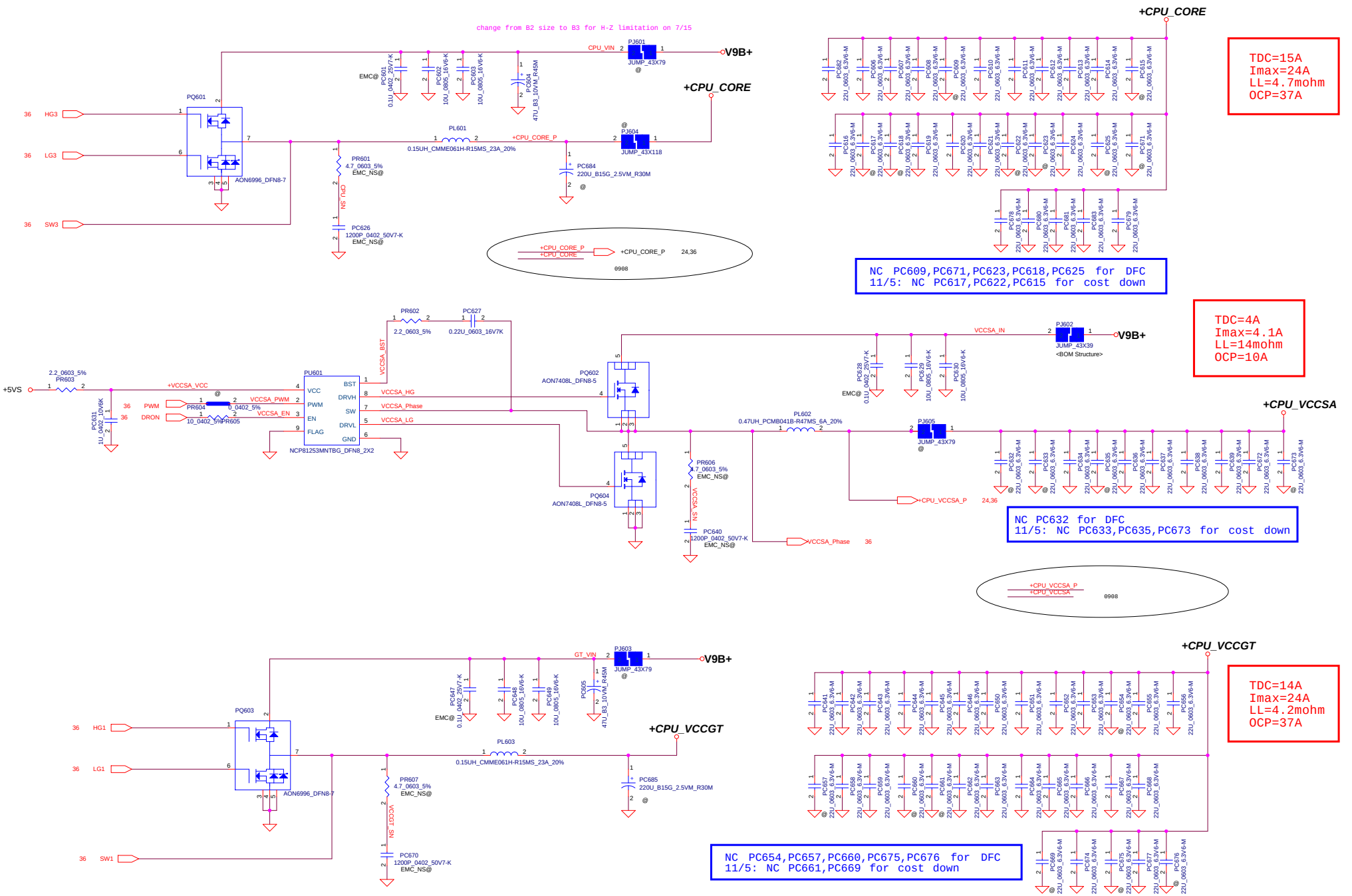
Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: PWR_CPU_CORE

Size: C | Document Number: Miray-K | Rev: 1.0

Date: Thursday, June 23, 2016 |

change from B2 size to B3 for H-Z limitation on 7/15



Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title: PWR_CPU_Core

Size	Document Number	Rev
C	Miray-K	1.0

Date: Thursday, June 23, 2016 Sheet 37 of 38

Security Classification	LC Future Center Secret Data		
Issued Date	2015/11/09	Deciphered Date	2016/06/27

Title

IMVP8

Size	Document Number	Rev
C	***Miray-K***	1.0

Date: Thursday, June 23, 2016 Sheet 38 of 38