Compal Confidentia

Model Name : ELZE1

File Name : LA-G611P

Compal Confidential

WOS M/B Schematics Document

Qualcomm SDM850 with LPDDR4

Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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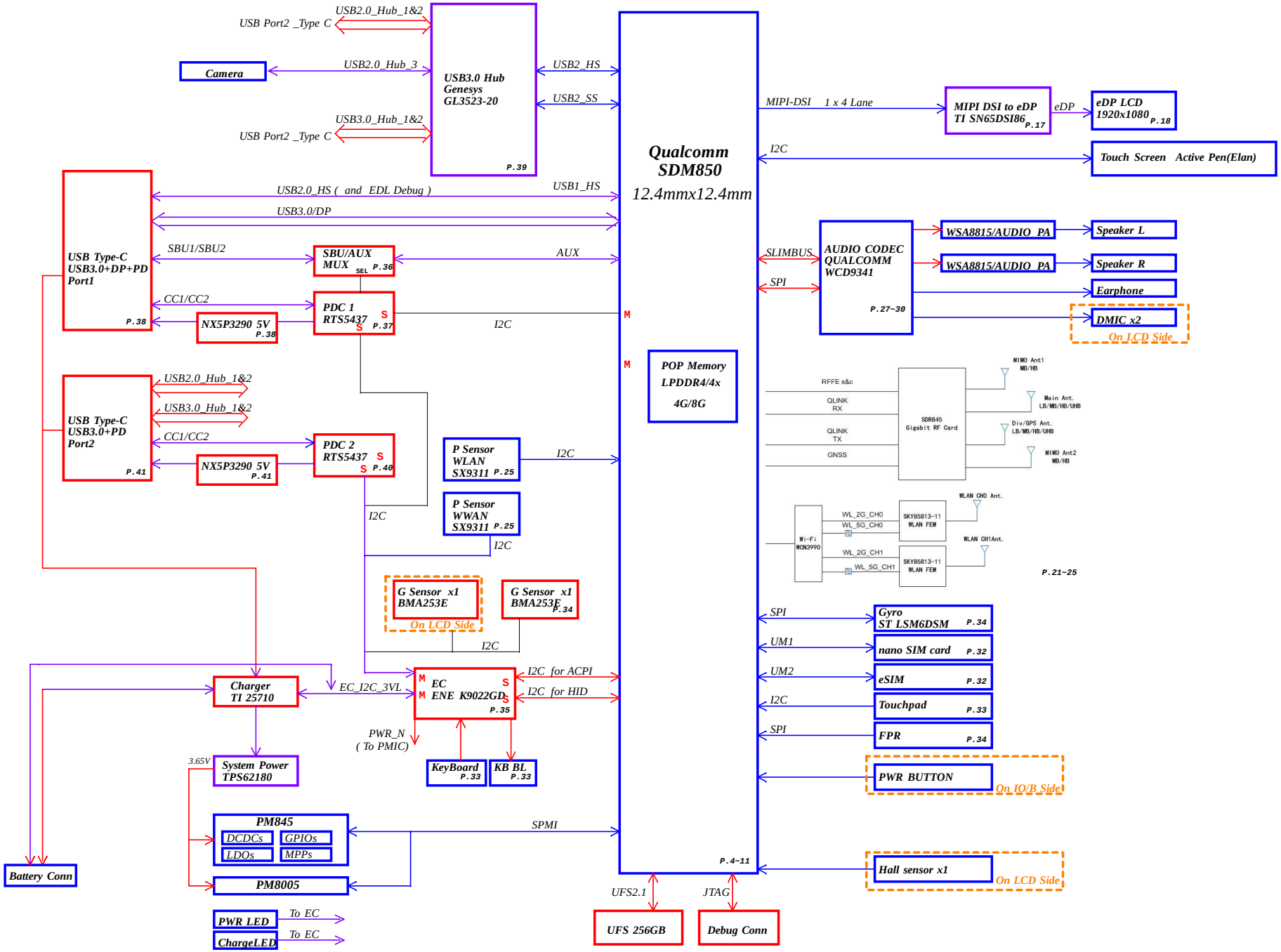
Title: Cover Page			
Size: Custom	Document Number: LA-G611P		Rev: 1.0
Date: Wednesday, August 01, 2018	Sheet 1 of 57		

YOGA WoS Qualcomm SDM850(Compal) Block Diagram



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Title: Block Diagram

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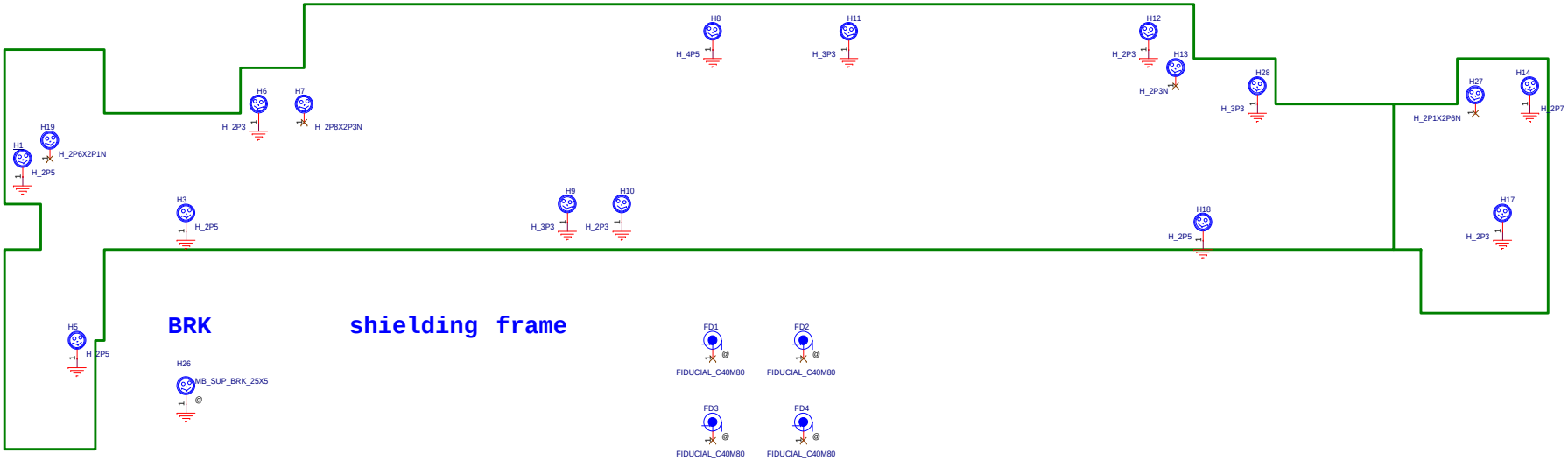

BRK

shielding frame

CPU (U1)

U1 CPU1@

SA0000BWD00

SDM850-0-AC 2.85G

UFS (U1501)

U1501 U128G@

SA0000BWP10

UFS_128G

Samsung	SA0000BWP10, S IC FL 128G KLUDG4U1EA-B0C1 FBGA 153P C38 !
Hynix	SA0000BWM10, S IC FL 128G H28S8Q302CMR FBGA 153P C38 !
Sandisk	SA0000BZZ10, S IC FL 128G SDINDDH4-128-1001V VFBGA 153P UFS C38 !

POP

POPU1 R4G@

SA0000BC000

RAM_4G

Samsung	SA0000BC010, S IC D4 32G/3733 K3UH5H50MM-AGCJ FBGA 556P C38 !
Hynix	SA0000BWS10, S IC D4 32G/4266 H9HKNNNCRMAVAR-NEN FBGA 556P C38 !
Micron	SA0000C0Q10, S IC D4 512M64 MT53D512M64D4RQ-053 WT:E WFBGA 556P C38 !

PCB

ZZZ

DAZ2CU00100

U1501 U256G@

SA0000BNS10

UFS_256G

Samsung	SA0000BNS10, S IC FL 256G KLUEG8U1EA-B0C1005 FBGA 153P UFS C38 !
Hynix	SA0000BWN10, S IC FL 256G H28S9O302BMR FBGA 153P C38 !
Sandisk	SA0000C0010, S IC FL 256G SDINDDH4-256-1001V VFBGA 153P UFS C38 !

POPU1 R8G@

SA0000BS300

RAM_8G

Samsung	SA0000BS310, S IC D4 64G/3733 K3UH7H70MM-AGCJ FBGA 556P C38 !
Hynix	SA0000BWR10, S IC D4 64G/4266 H9HKNNNFBMMVAR-NEN FBGA 556P C38 !

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Title: **Notes_List**

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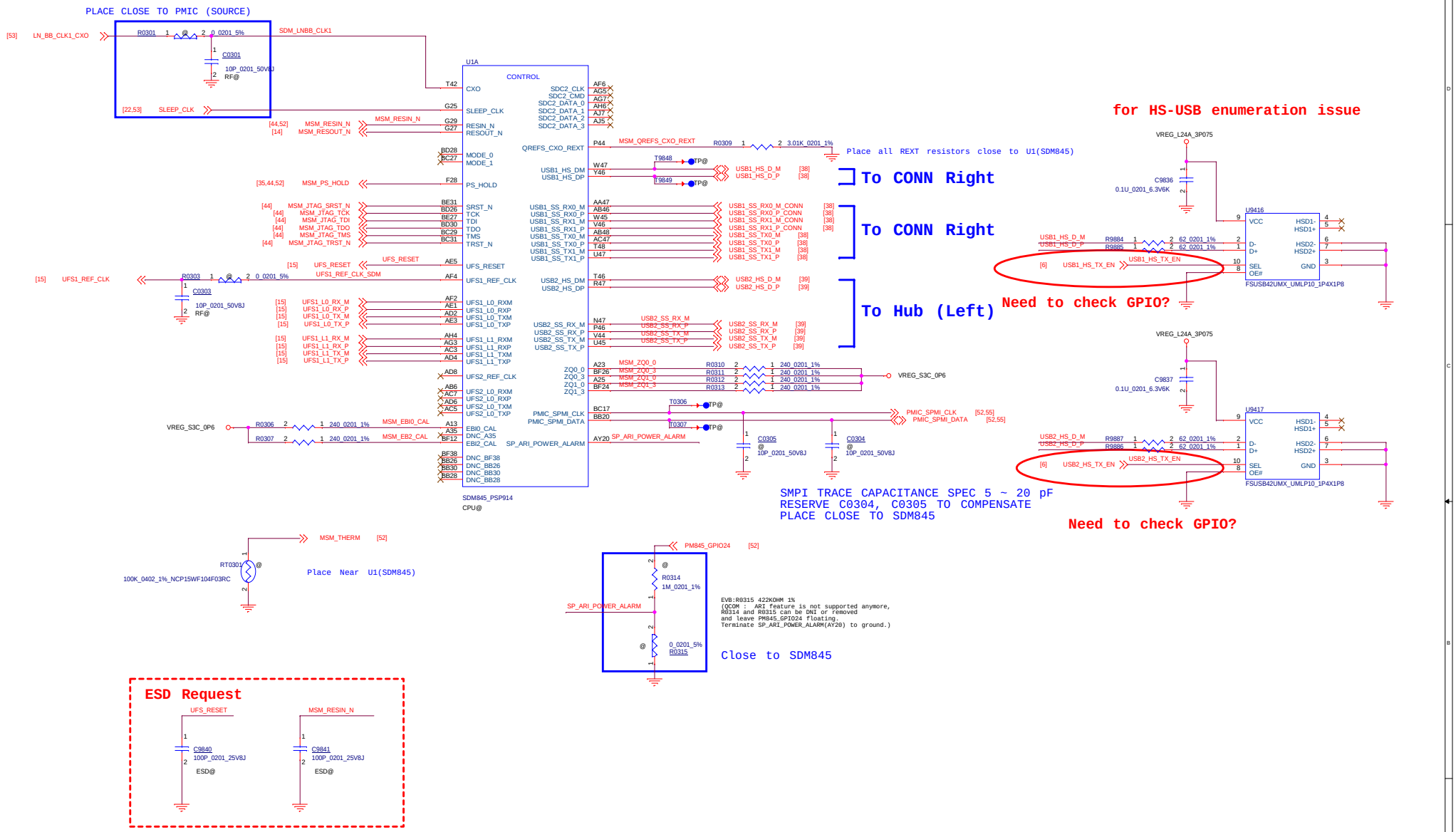

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Title: **SDM845 CONTROL**

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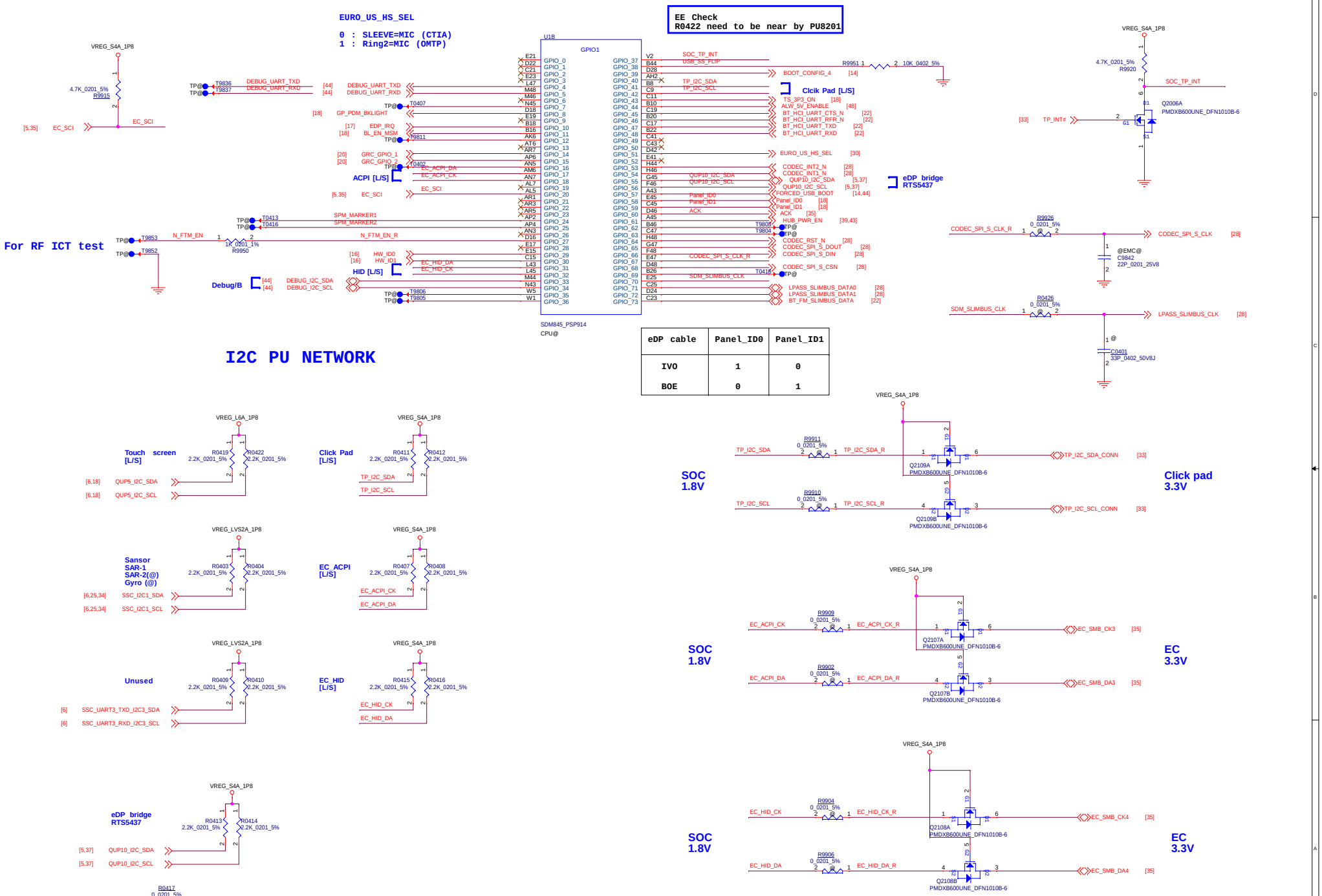

eDP cable	Panel_ID0	Panel_ID1
IVO	1	0
BOE	0	1

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Title: SDM845_GPIO1

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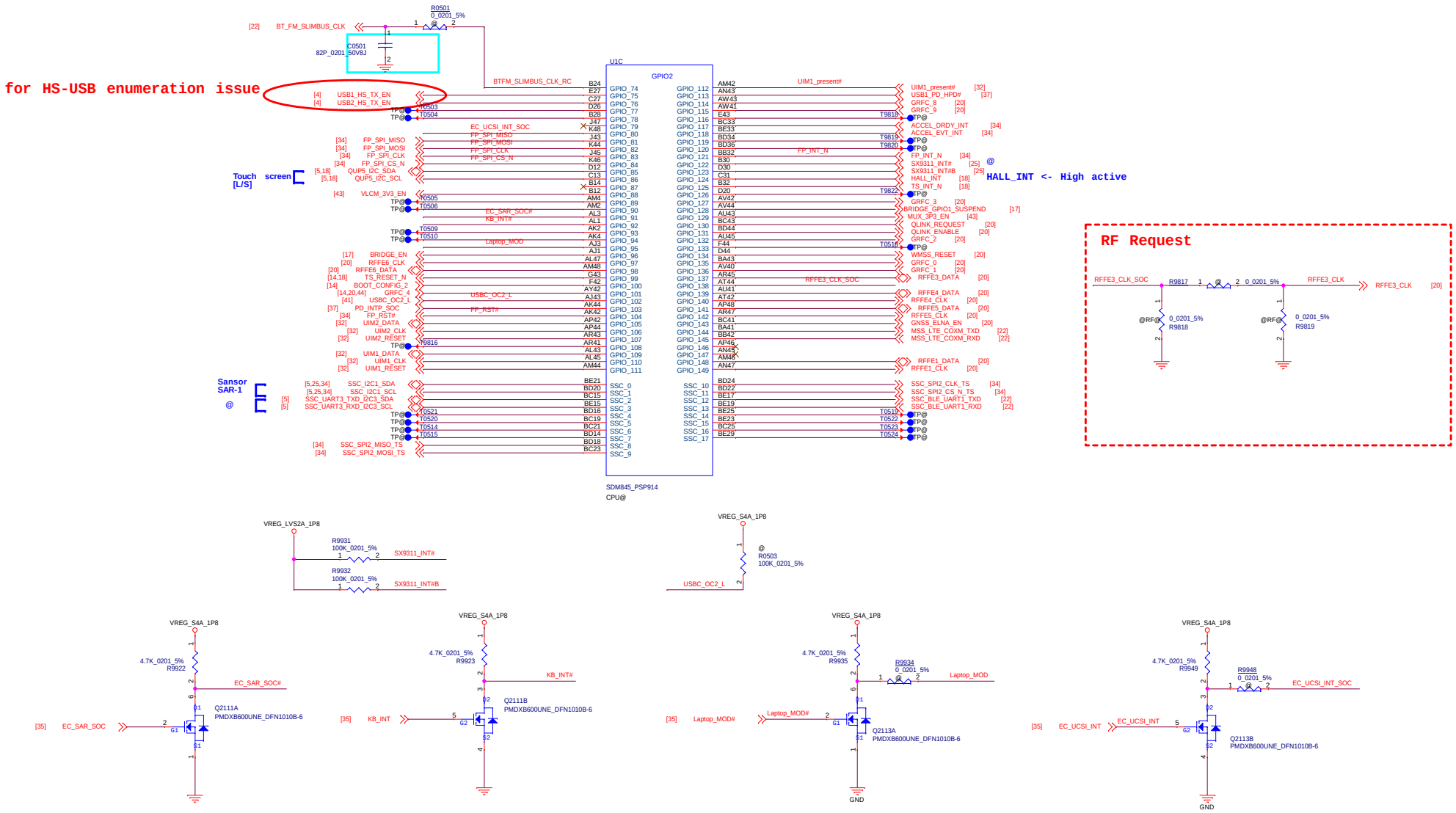

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Compal Electronics, Inc.

Title: **SDM845_GPIO2**

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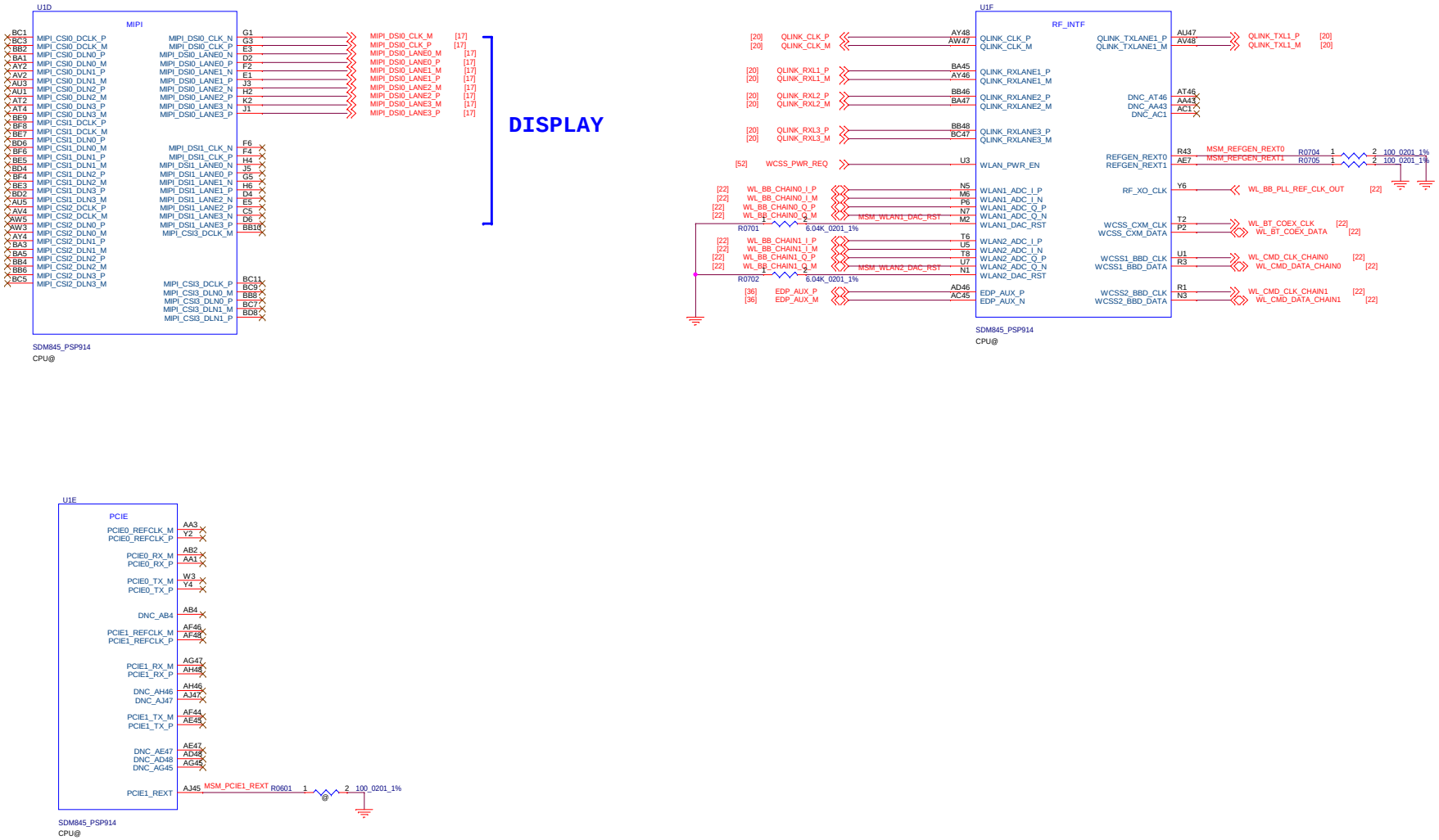

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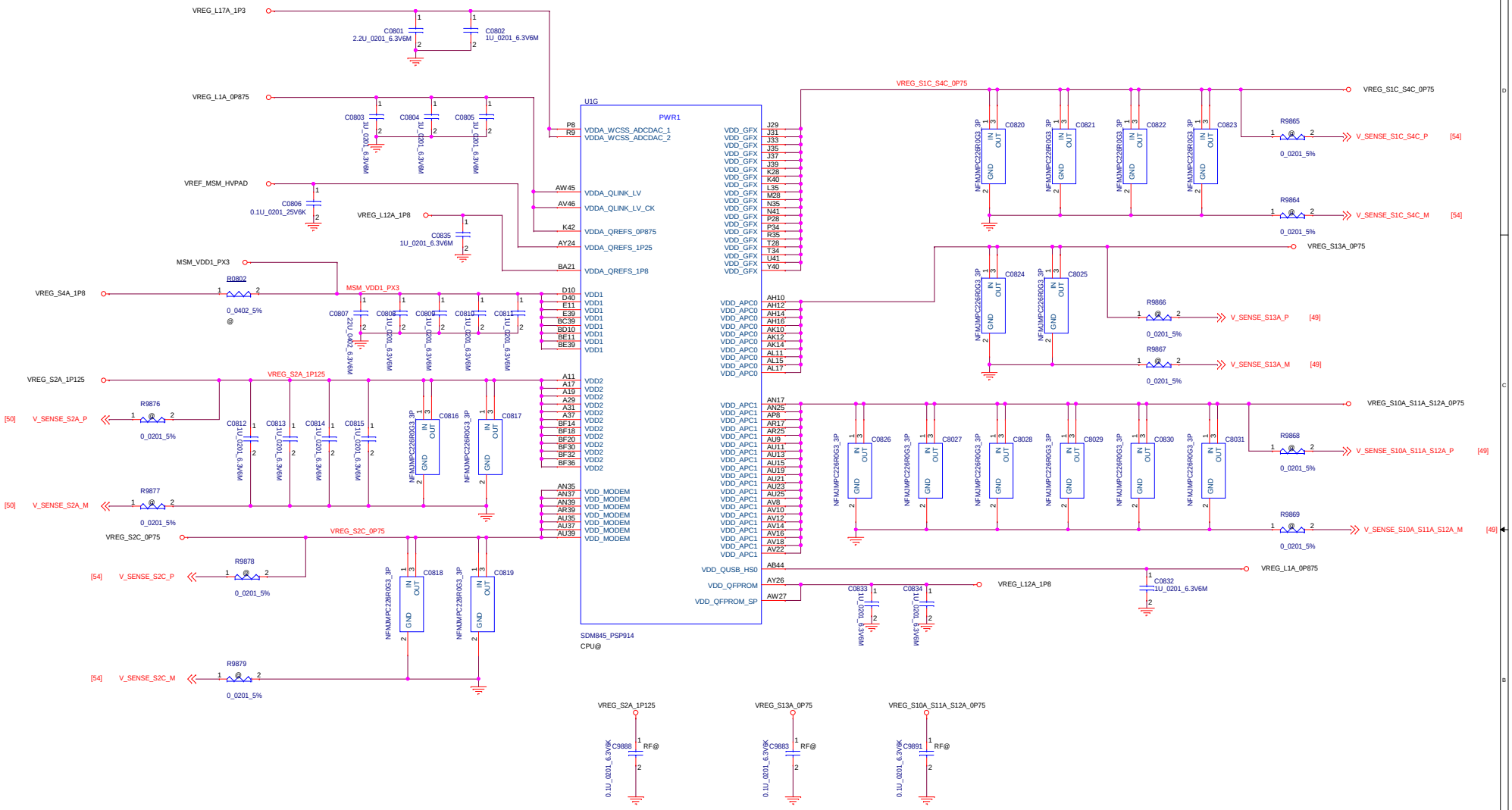

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Title: **SDM845 PWR1**

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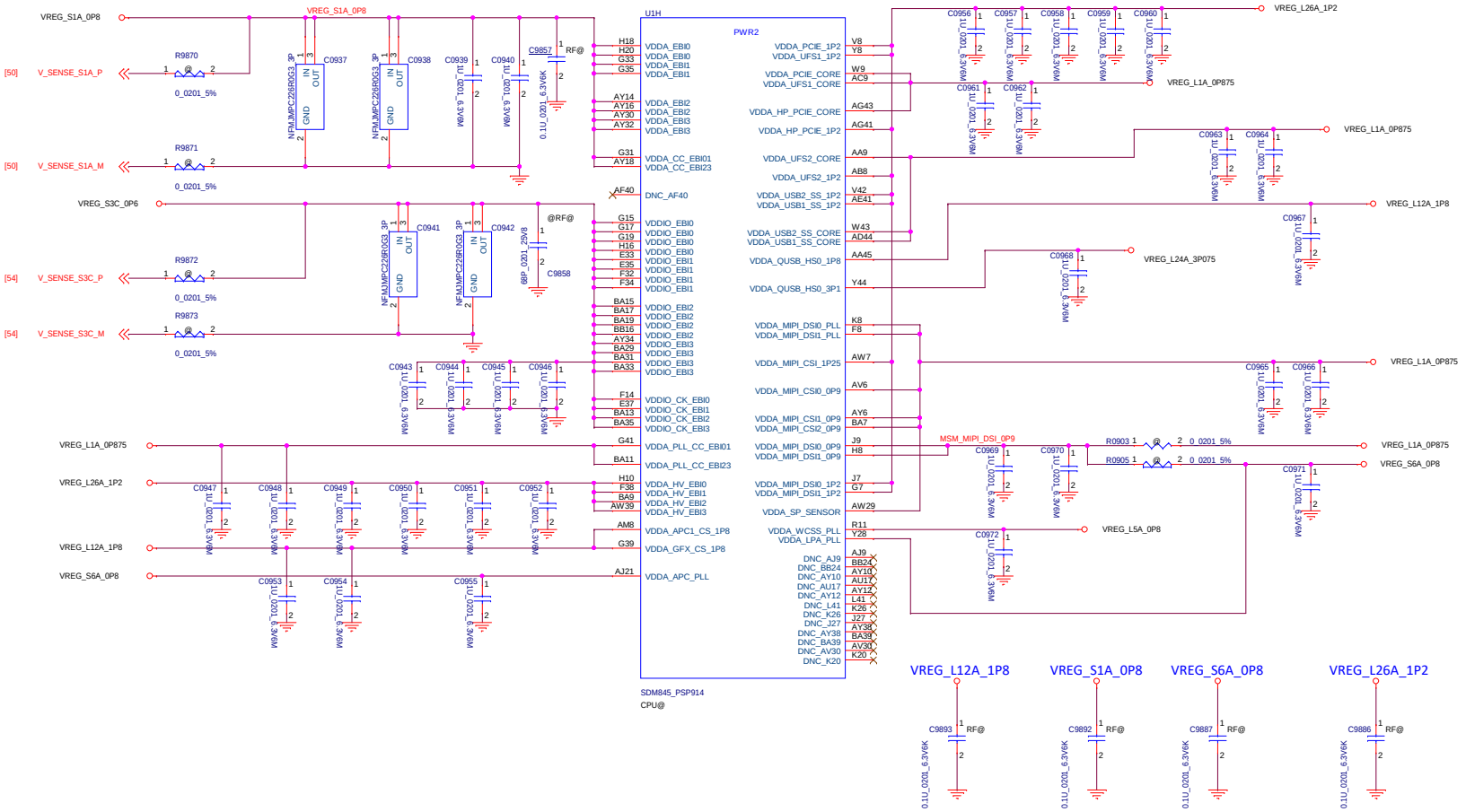

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Title: **SDM845 PWR2**

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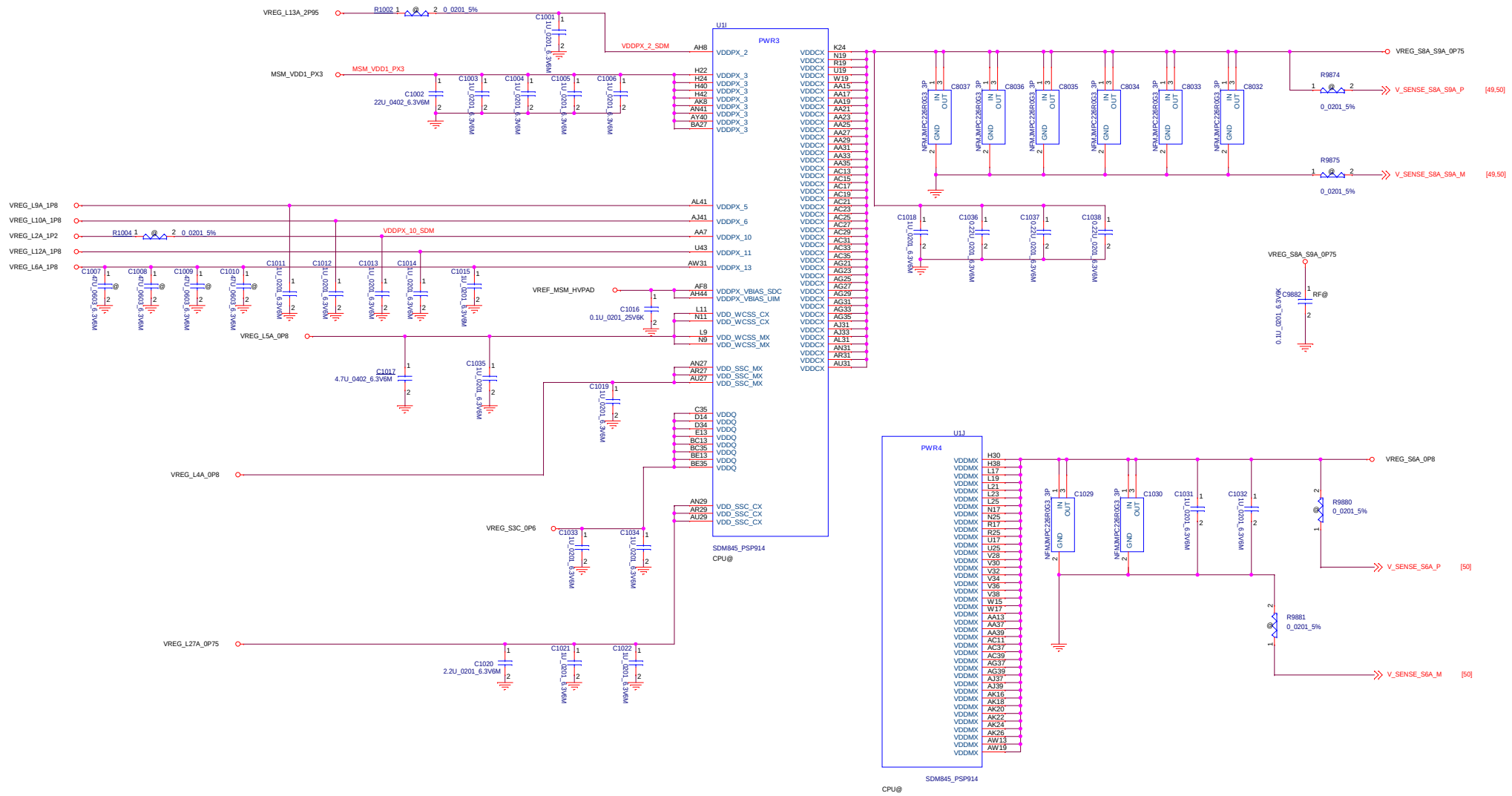

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Title: **SDM845 PWR3**

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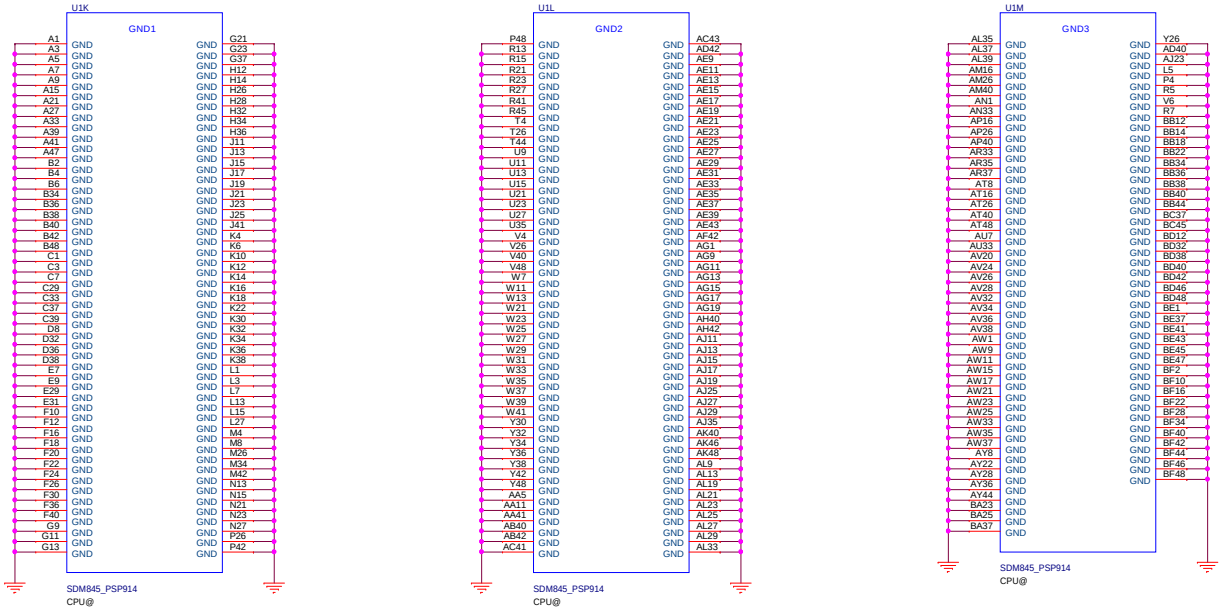

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Title: **SDM845_GND**

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SoC_I2C

Channel	Dev.	Address	Level
GPIO_17/18	EC_ACPI	0x60	3.3(L/S)
GPIO_31/32	EC_HID		3.3(L/S)
GPIO_41/42	Click pad	0X2C (Synaptics) 0X15 (ELAN)	3.3(L/S)
GPIO_85/86	Touch screen	0x10	3.3(L/S)
SSC_0/1	Sar-1_Wlan	0x28	1.8
GPIO_53/54	eDP Bridge	0x2C	1.8
	PDC1_5437	0xBC	3.3(L/S)

EC_I2C

Channel	Dev.	Address	Level
EC_SMB_2	PDC1_5437	0xBC	3.3
	PDC2_5437	0xBE	3.3
	G-Sensor(MB)	0011000b(0x18)	3.3
	G-Sensor(Panel)	0011001b(0x19)	3.3
	Sar-2_LTE	0x28	3.3

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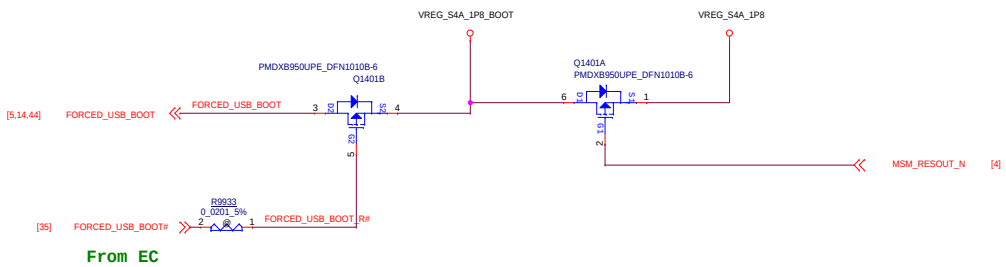
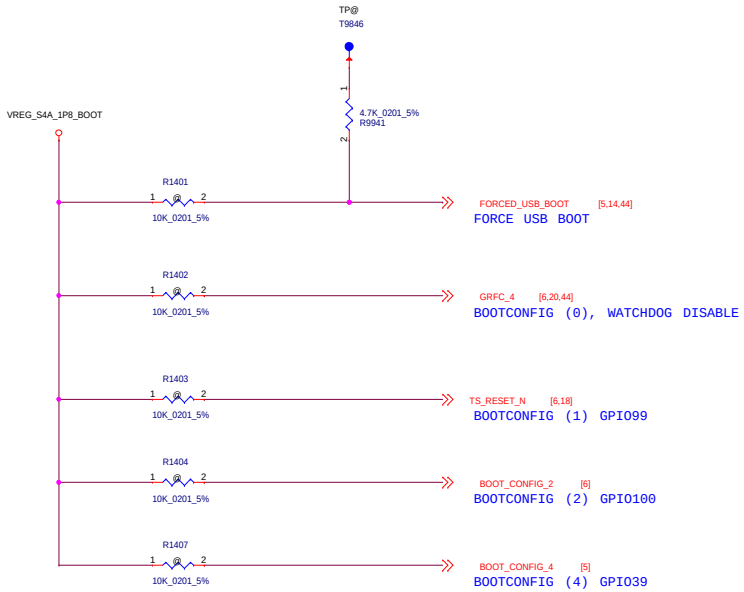


Boot Pin Do not use for PU/PD

Boot configuration #	GPIO #	Function	Bit values
BOOT_CONFIG_0	GPIO_101	WDOG disable	1 – Disables WDOG 0 – Enables WDOG
BOOT_CONFIG_1	GPIO_99	Fast boot bit 0	Selects external boot device.
BOOT_CONFIG_2	GPIO_100	Fast boot bit 1	
BOOT_CONFIG_3	GPIO_133	Fast boot bit 2	
BOOT_CONFIG_4	GPIO_39	Fast boot bit 3	
BOOT_CONFIG_10	GPIO_148	Use serial number	0 – Serial number is not used for authentication. 1 – All segments of serial number used for authentication.
BOOT_CONFIG_11	GPIO_146	MSA PK hash in fuse	0 – Hash of MSA root is in the apps boot ROM. 1 – Hash of MSA root is in the OEM PK hash.
BOOT_CONFIG_12	GPIO_141	MSA authentication enable	0 – Disables MSA authentication. 1 – Enables MSA authentication.
BOOT_CONFIG_13	GPIO_136	Apps PK hash in fuse	0 – Hash of apps root is in the apps boot ROM. 1 – Hash of apps root is in the OEM PK hash.
BOOT_CONFIG_14	GPIO_132	Apps authentication enable	0 – Disables apps authentication. 1 – Enables apps authentication.
BOOT_CONFIG_15	GPIO_116	Force MSA authentication enable	0 – Disables force MSA authentication. 1 – Enables force MSA authentication.
FORCE_USB_BOOT	GPIO_57	Force USB download	0 – Releases USB download mode. 1 – Enables USB download mode.



	GPIO				
FAST_BOOT	39	133	100	99	Boot device/comments
Default 0000	0	0	0	0	UFS (1)
					Then SD card on SDC2 (2)
					Then SS/HS/FS USB on USB 3.1 (3)
0001	0	0	0	1	SD card on SDC2 (1)
					Then UFS (2)
					Then SS/HS/FS USB on USB 3.1 (3)
0010	0	0	1	0	SD card on SDC2 (1)
					Then SS/HS/FS USB on USB 3.1 (2)
0011	0	0	1	1	SS/HS/FS USB on USB 3.1 (1)
0100	0	1	0	0	Quad SPI (1)
					Then SS/HS/FS USB on USB 3.1 (2)
0101	0	1	0	1	Single SPI (1)
					Then SS/HS/FS USB on USB 3.1 (2)

QUALCOMM
2017-04-27 20:43:32 PDT
raymond_lai@asus.com

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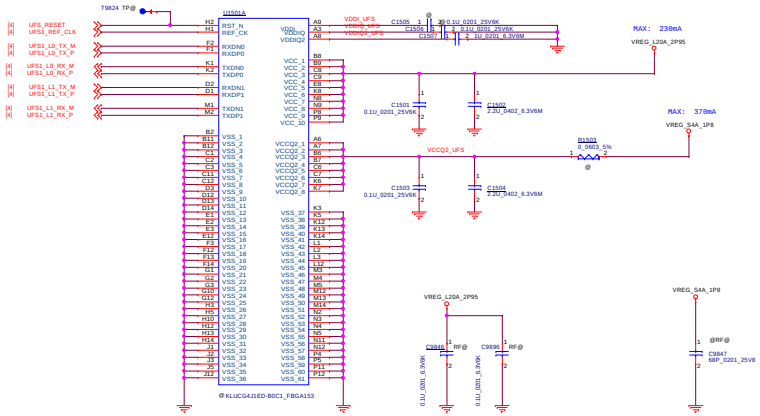
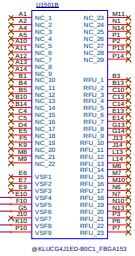
UFS MEMORY (SR)



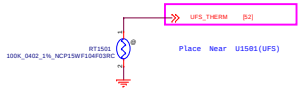


TEST POINTS FOR VENDOR DEBUG

TOSHIBA: VSF4, VSF8

HYNIX: VSF4, VSF6, VSF8, VSF9

SAMSUNG: VSF4, VSF5, VSF8



[Table 7] Power mode and MIPI UniPro and M-PHY power state

UFS power mode	UniPro Power Mode	M-PHY Power Mode	VCC Power	Description
ACTIVE	FAST_STATE	HS-BURST	On	-
IDLE	SLEEP_STATE	STALL	On	-
IDLE2[1)]	HIBERNATE_STATE	Hibern8	On	See the Chapter 2.4.1
SLEEP	HIBERNATE_STATE	Hibern8	Off	-
POWER DOWN	OFF_STATE	UNPOWERED	Off	-

NOTE :
1) Samsung specific power mode for saving the IDLE power. Host shall issue 'enter hibern8' for this power mode.

[Table 3] Supply voltage for operating

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Supply Voltage	VCCQ2	1.7	1.8	1.95	V

[Table 17] Power Consumption

Power	Density	NAND Type	HS Gear3 x 1Lane		HS Gear3 x 2Lane		Unit
			VCCQ2(1.8V)	VCC(3.3V)	VCCQ2(1.8V)	VCC(3.3V)	
Active	64 GB	128Gb MLC x 4	320	230	370	230	mA
IDLE2			450	70	450	70	uA
Sleep				0[1)]		0[1)]	uA

[Table 2] 153 FBGA Ball Information

Name	Type	Description
VCC	Supply	Supply voltage for the memory devices
VCCQ2	Supply	Supply voltage used typically for the PHY interface and the memory controller and any other internal low voltage block
VDDiQ	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator typically related to the memory controller
VDDiQ2	Input	Input terminal to provide bypass capacitor for VCCQ2 internal regulator, typically related to memory IF
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator
VSS	Supply	Ground
RST_n	Input	Input hardware reset signal. This is an active low signal
REF_CLK	Input	Input reference clock. When not active, this signal shall be pull-down or driven low by the host SoC.
RXDP0 / RXDP1	Input	Downstream data lane(1st and 2nd lane) : differential input signals into UFS device from the host
RXDN0 / RXDN1		
TXDP0 / TXDP1	Output	Upstream data lane(1st and 2nd lane) : differential output signals from the UFS device to the host
TXDN0 / TXDN1		
NC	-	Not Connected. NC pins can be connected to ground or left floating
RFU	-	Reserved for Future Use. RFU pins must be left floating.
VSFn	-	Vendor Specific Function. VSFn(n=1-9) pins must be left floating. Each vendor is able to use these pins during manufacturing

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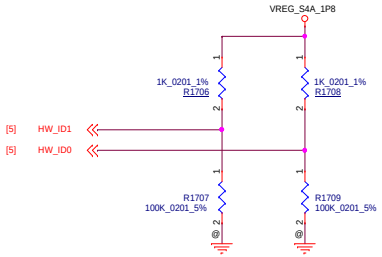

PCB ID (1,0)

PCB Ver.	Value	Phase
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0.2	01	FVT
0.3	10	SIT
1.0	11	SVT

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Title: **PCB ID & BUTTON**

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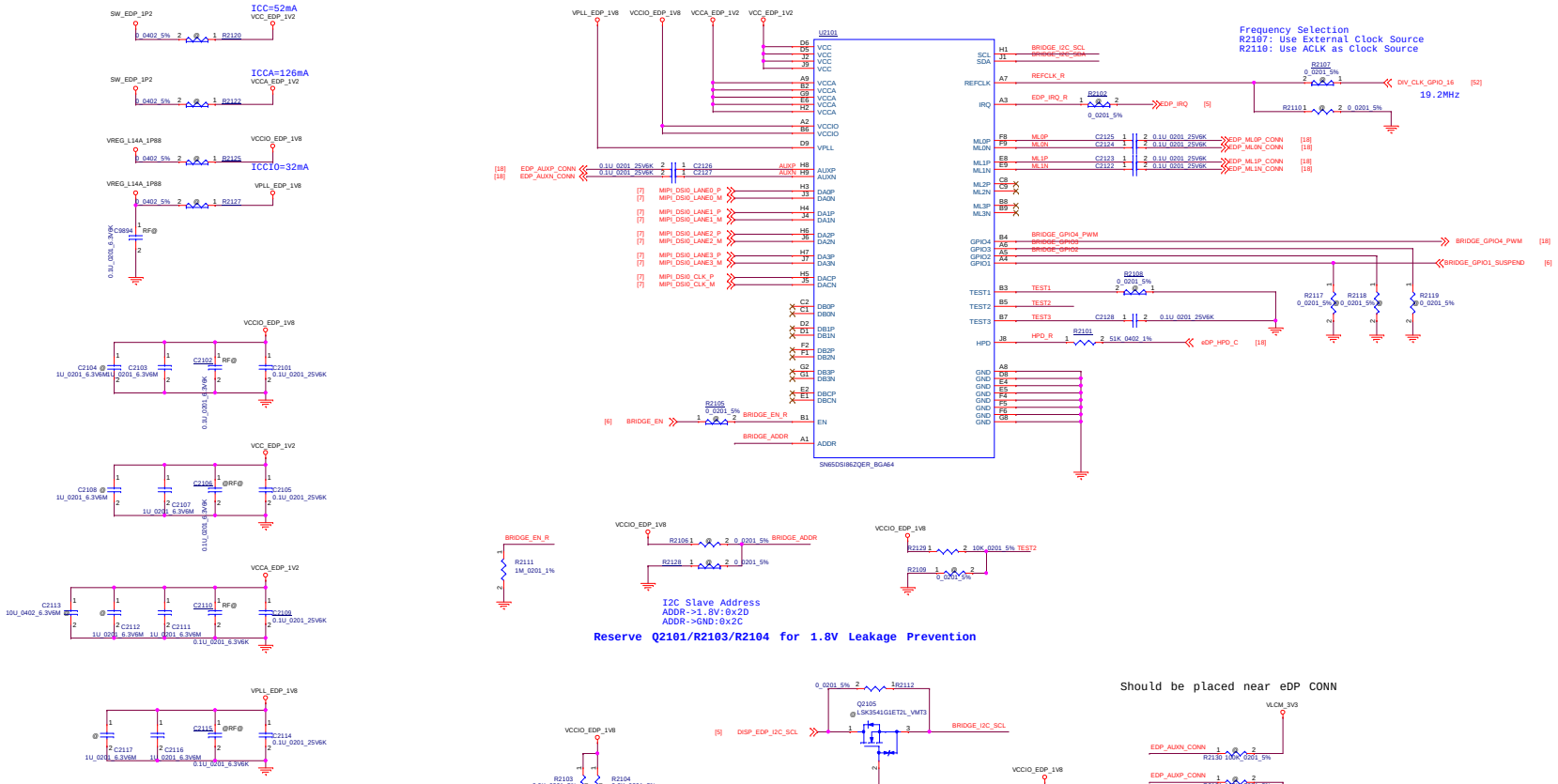
Date: Wednesday, August 01, 2018 | Sheet 16 of 57



TI_SN65DSI86 POR (Use REFCLK as Clock Source)

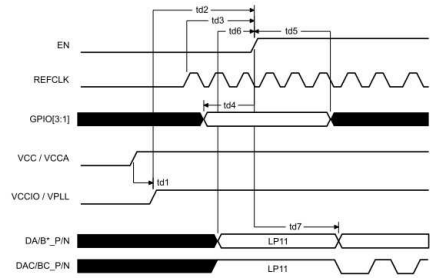


Figure 1. Power-Up Timing Definitions for DPPLL_CLK_SRC = REFCLK

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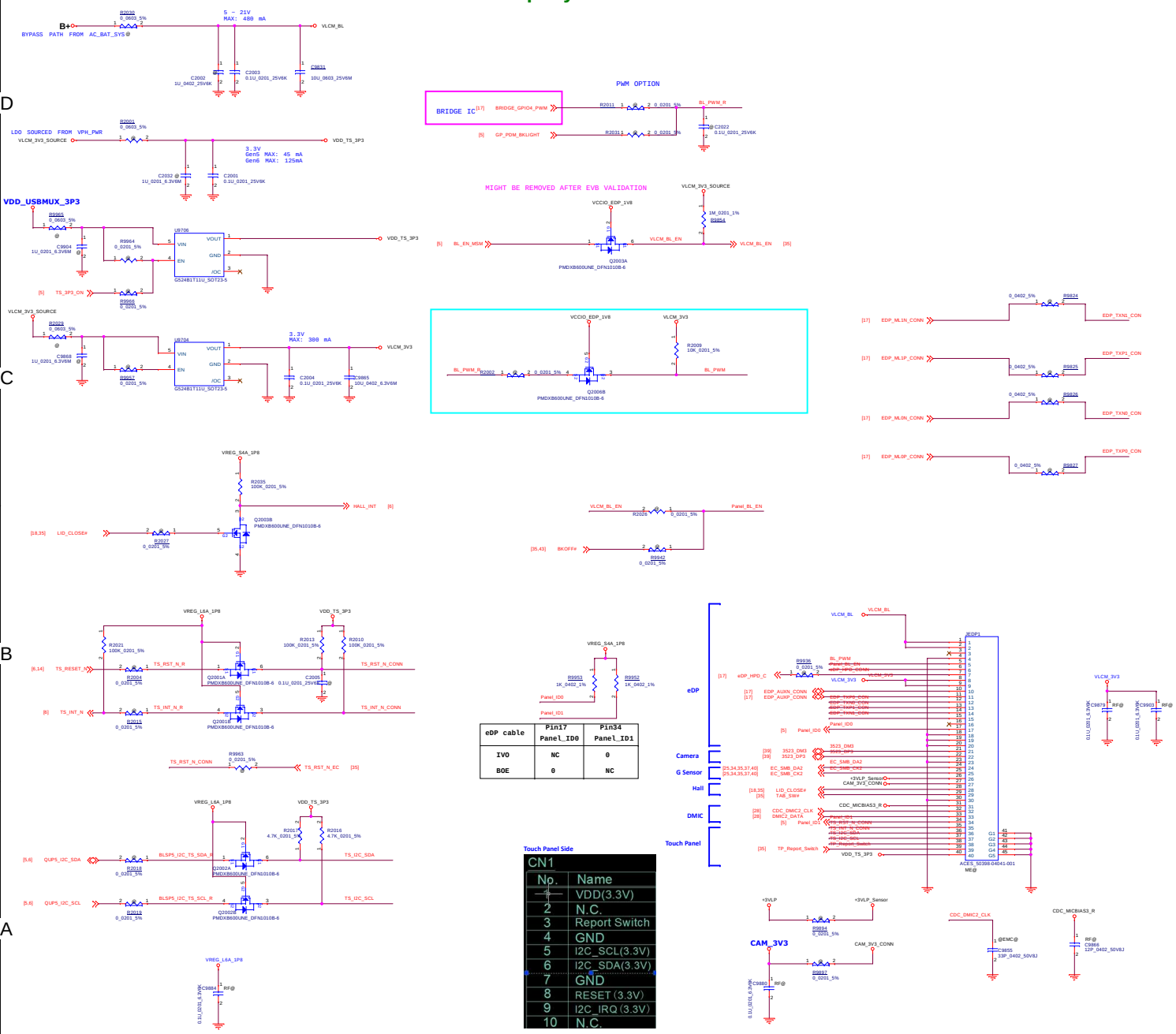
Display



eDP cable	Pin17 Panel_ID0	Pin34 Panel_ID1
IVO	NC	0
BOE	0	NC

Touch Panel Side

CN1	
No.	Name
1	VDD(3.3V)
2	N.C.
3	Report Switch
4	GND
5	I2C_SCL(3.3V)
6	I2C_SDA(3.3V)
7	GND
8	RESET (3.3V)
9	I2C_IRQ (3.3V)
10	N.C.

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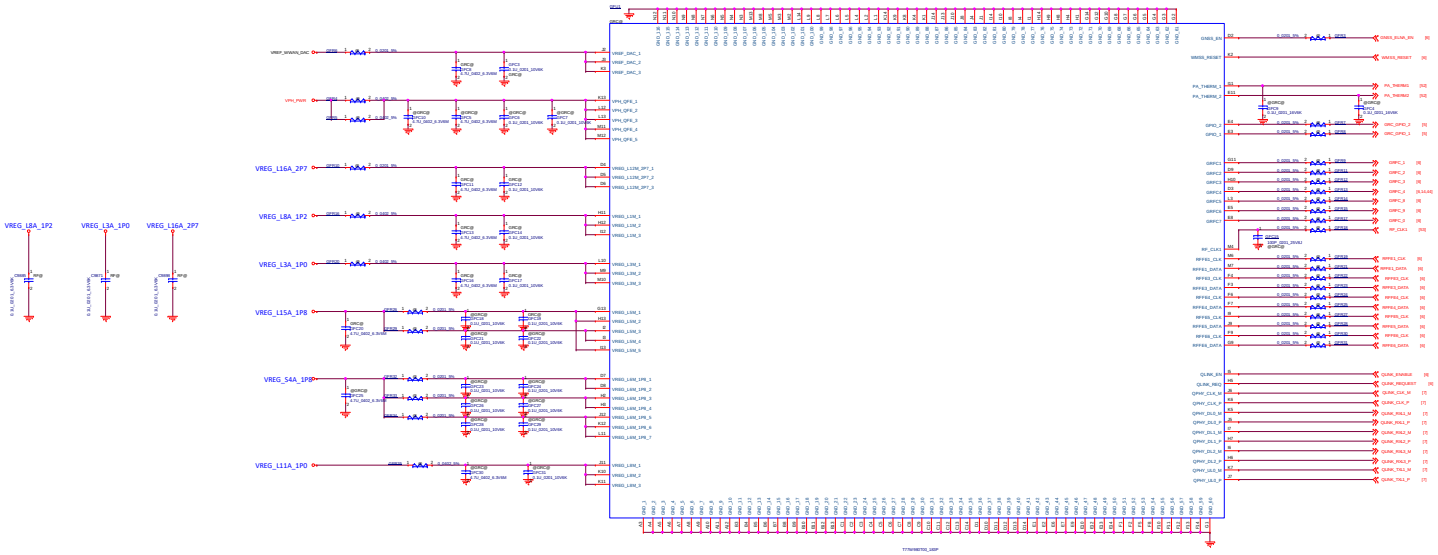

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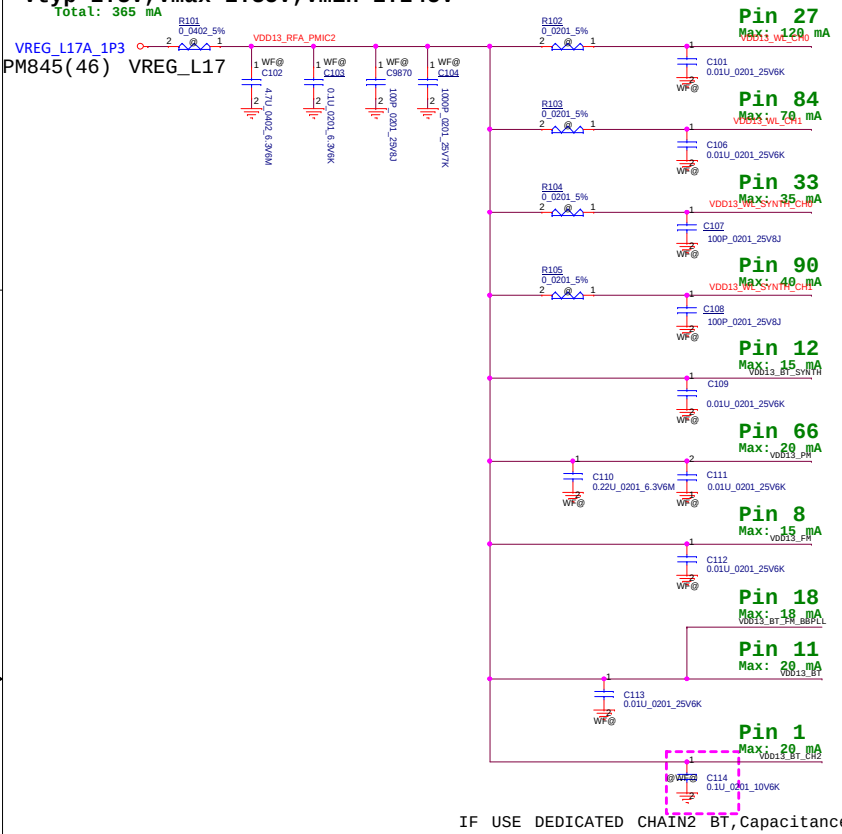
01_POWER_GROUND

WCN3990 POWER/GROUND

Vtyp=1.3V,Vmax=1.35V,Vmin=1.245V
Total: 365 mA

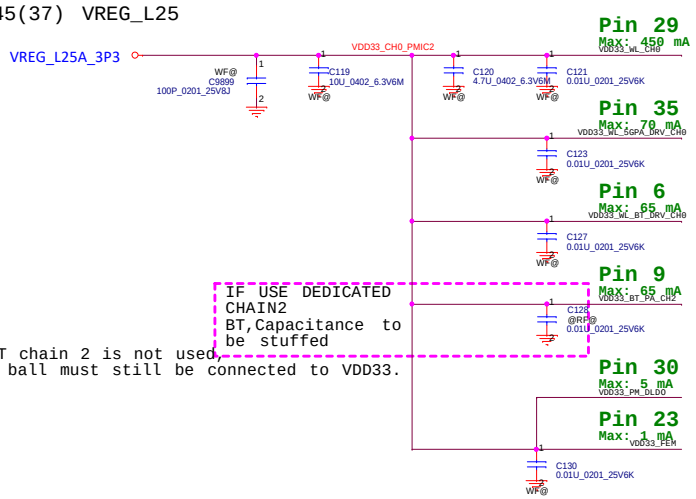
VREG_L17A_1P3
PM845(46) VREG_L17



IF USE DEDICATED CHAIN2 BT,Capacitance to be stuffed

Vtyp=3.3V,Vmax=3.4V,Vmin=3.2V
Total: 656 mA

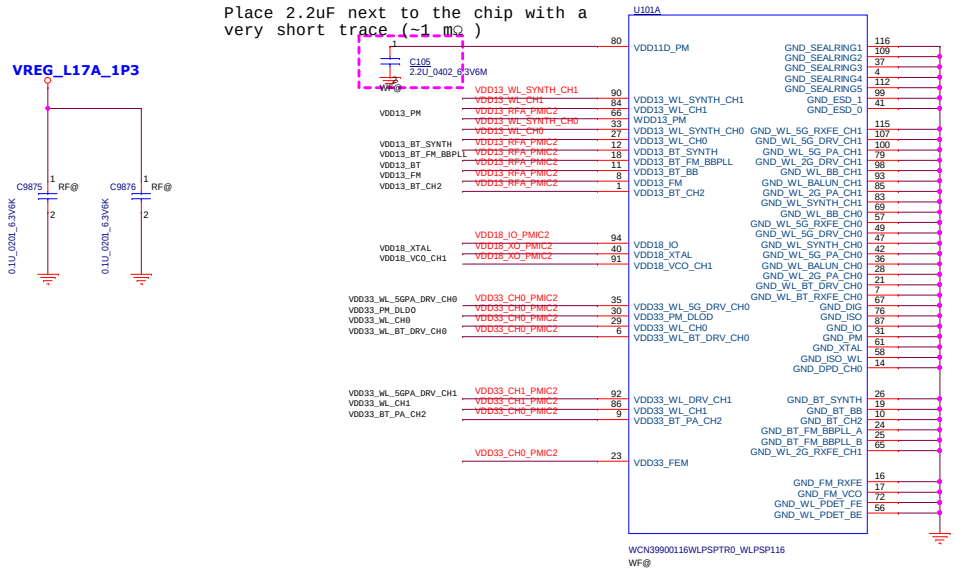
PM845(37) VREG_L25



IF USE DEDICATED CHAIN2 BT,Capacitance to be stuffed

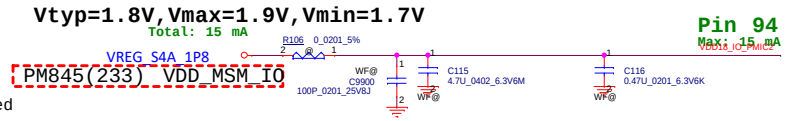
If BT chain 2 is not used, this ball must still be connected to VDD33.

Place 2.2uF next to the chip with a very short trace (~1 mm)



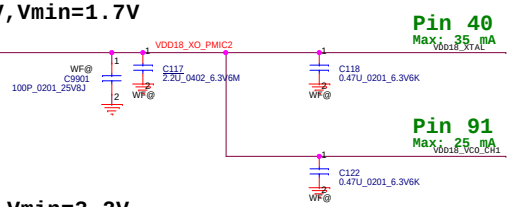
Vtyp=1.8V,Vmax=1.9V,Vmin=1.7V
Total: 15 mA

VREG_S4A_1P8
PM845(233) VDD_MSM_IO



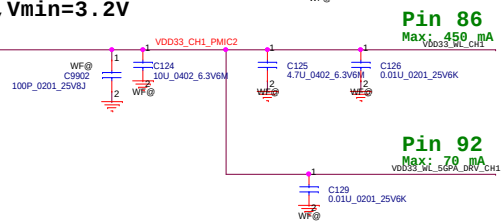
Vtyp=1.8V,Vmax=1.9V,Vmin=1.7V
Total: 60 mA

VREG_L7A_1P8
PM845(51) VREG_L7



Vtyp=3.3V,Vmax=3.4V,Vmin=3.2V
Total: 520 mA

VREG_L23A_3P3
PM845(61) VREG_L23



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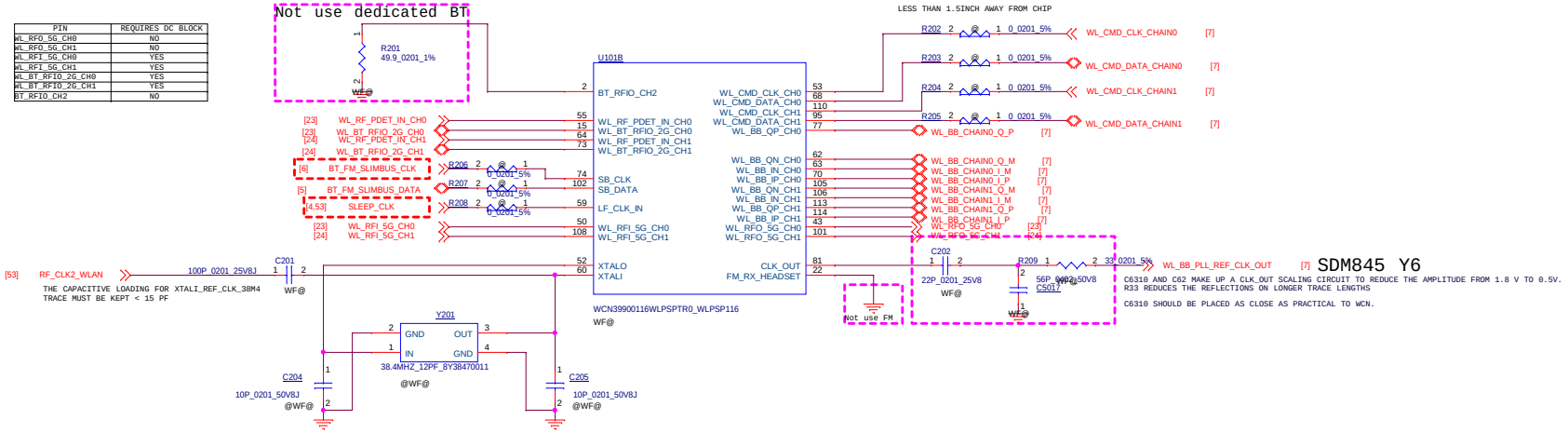
02_RF_INTERFACES

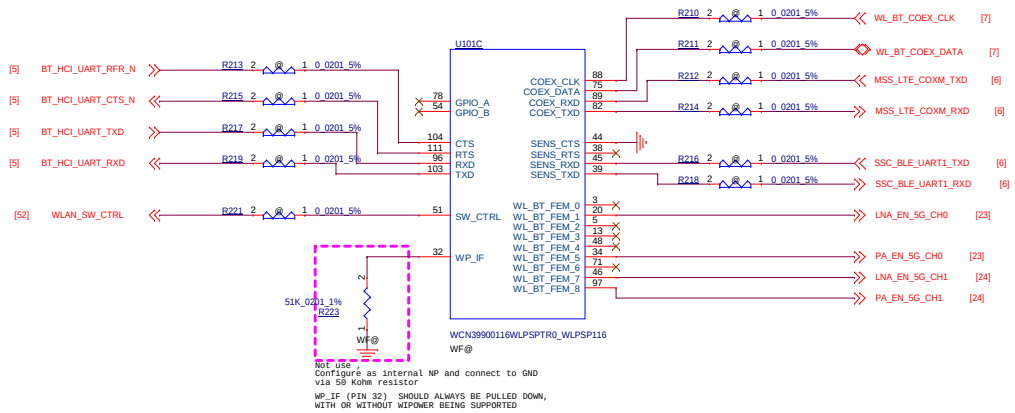
WCN3990 RF/CONTROL

PIN	REQUIRES DC BLOCK
WL_RFO_5G_CH0	NO
WL_RFO_5G_CH1	NO
WL_RFI_5G_CH0	YES
WL_RFI_5G_CH1	YES
WL_BT_RFIO_2G_CH0	YES
WL_BT_RFIO_2G_CH1	YES
BT_RFIO_CH2	NO



NOTE: CRYSTAL BACKUP STUFF OPTION CAN BE USED FOR IMPROVING EVM PERFORMANCE IN DESIGNS THAT HAVE PMIC/CLOCK LAYOUT ISSUES.IF USING XTAL OPTION INSERT Y1, C27, C19, AND DNI C40

WCN3990 RF/IO



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Title: RF_INTERFACES

Size: C | Document Number: LA-G611P | Rev: 1.0

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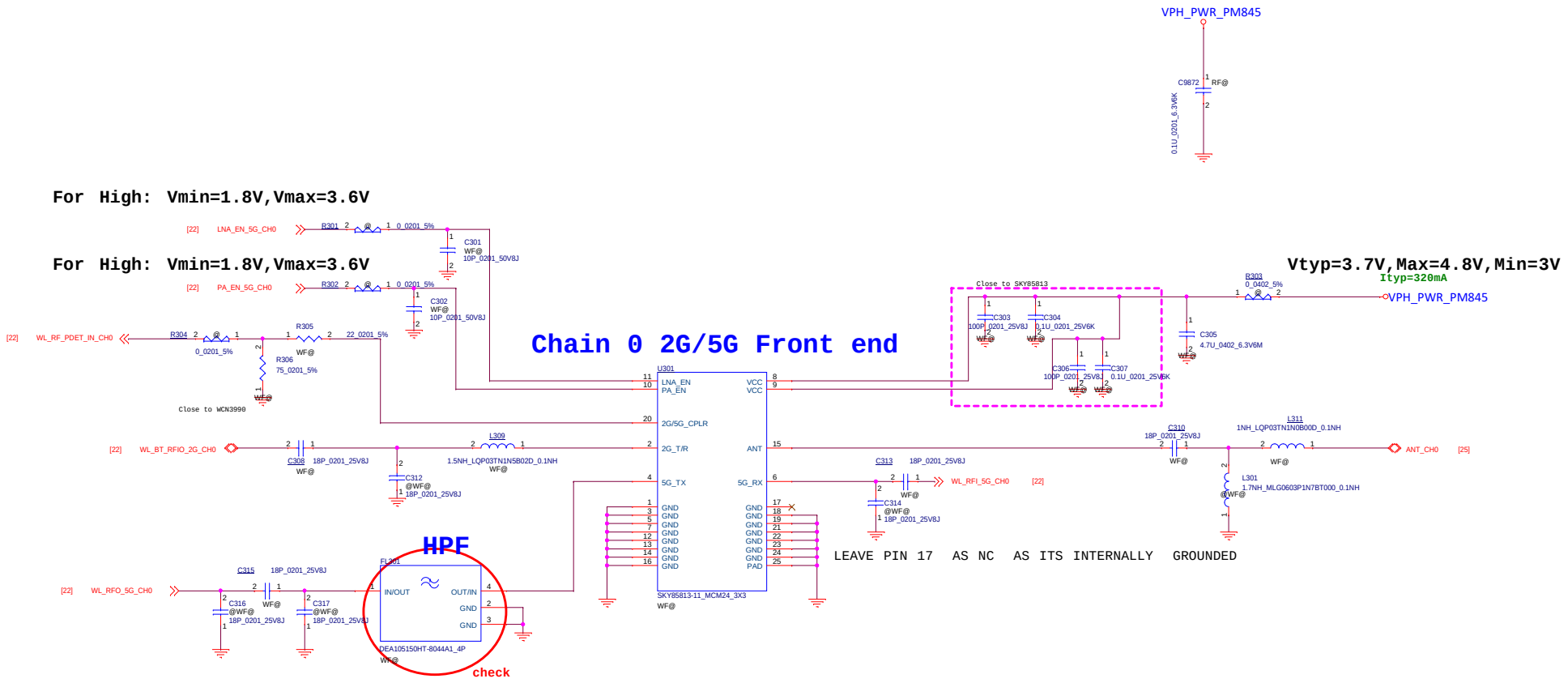
03_RFFE_CHAIN0_2G_IPA_5G_FEM_NON_ANTENNA SHARING



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				Date: Wednesday, August 01, 2018; Sheet 23 of 57

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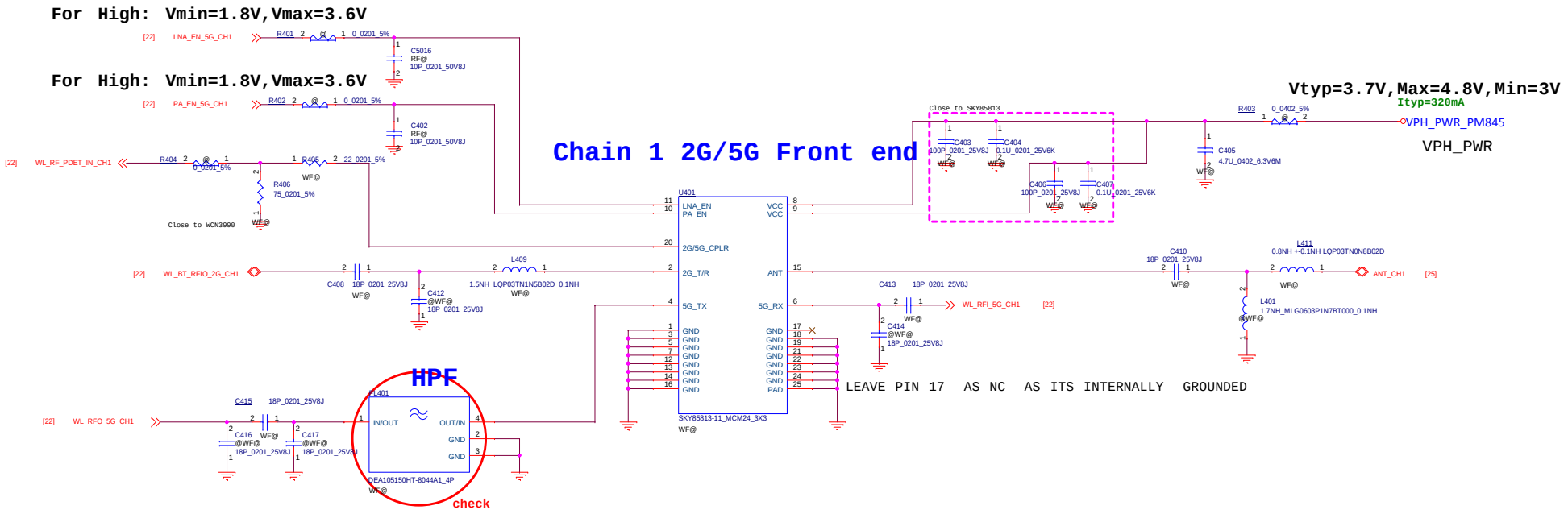
04_RFFE_CHAIN1_2G_IPA_5G_FEM_NON_ANTENNA SHARING



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Title: RFFEM_CHAIN1

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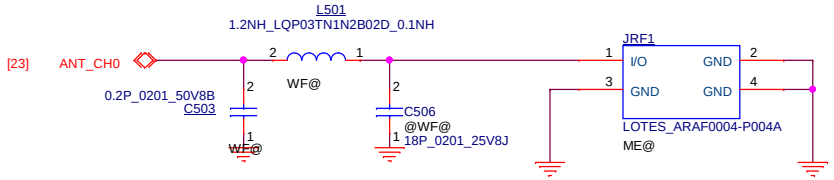
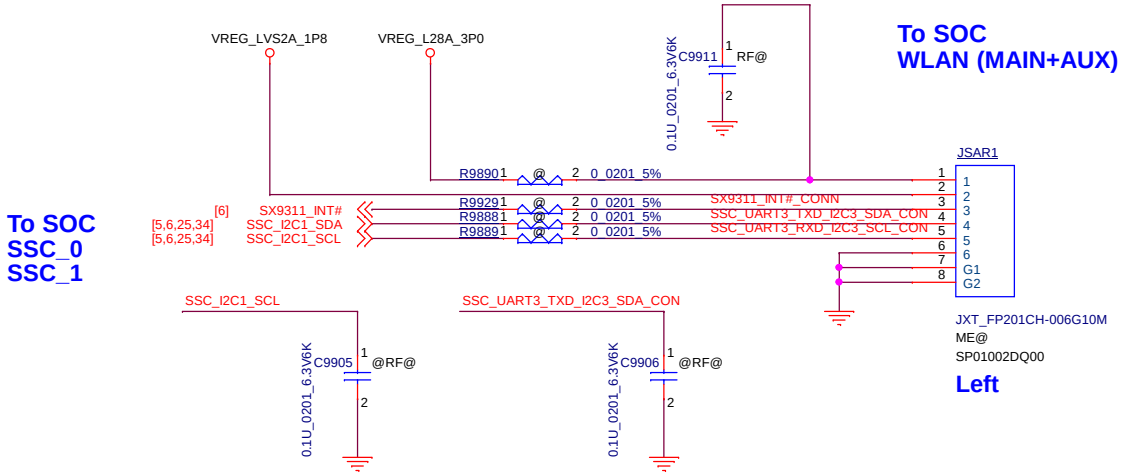
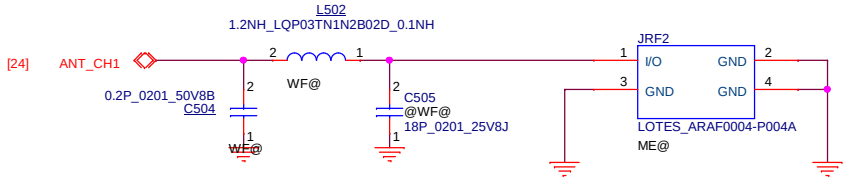
05_ANT_PORT

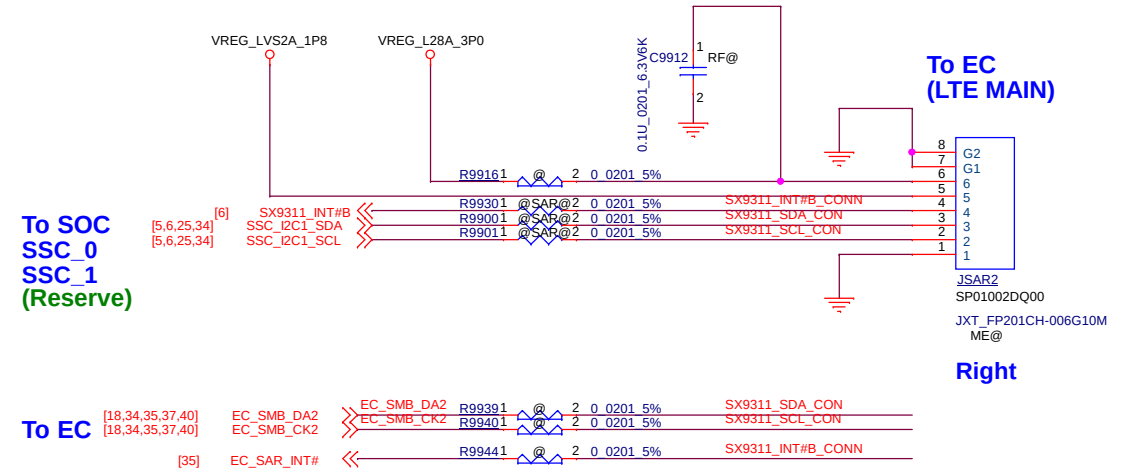
Chain 0 RF Connector

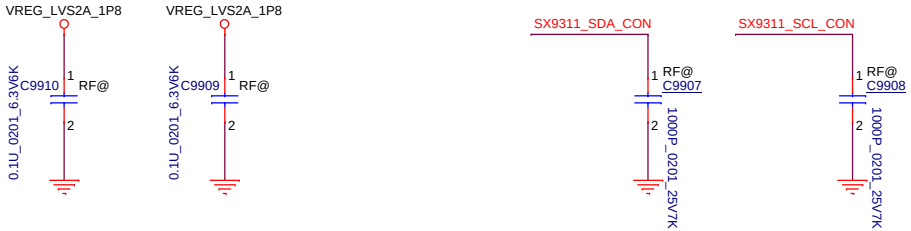




Chain 1 RF Connector







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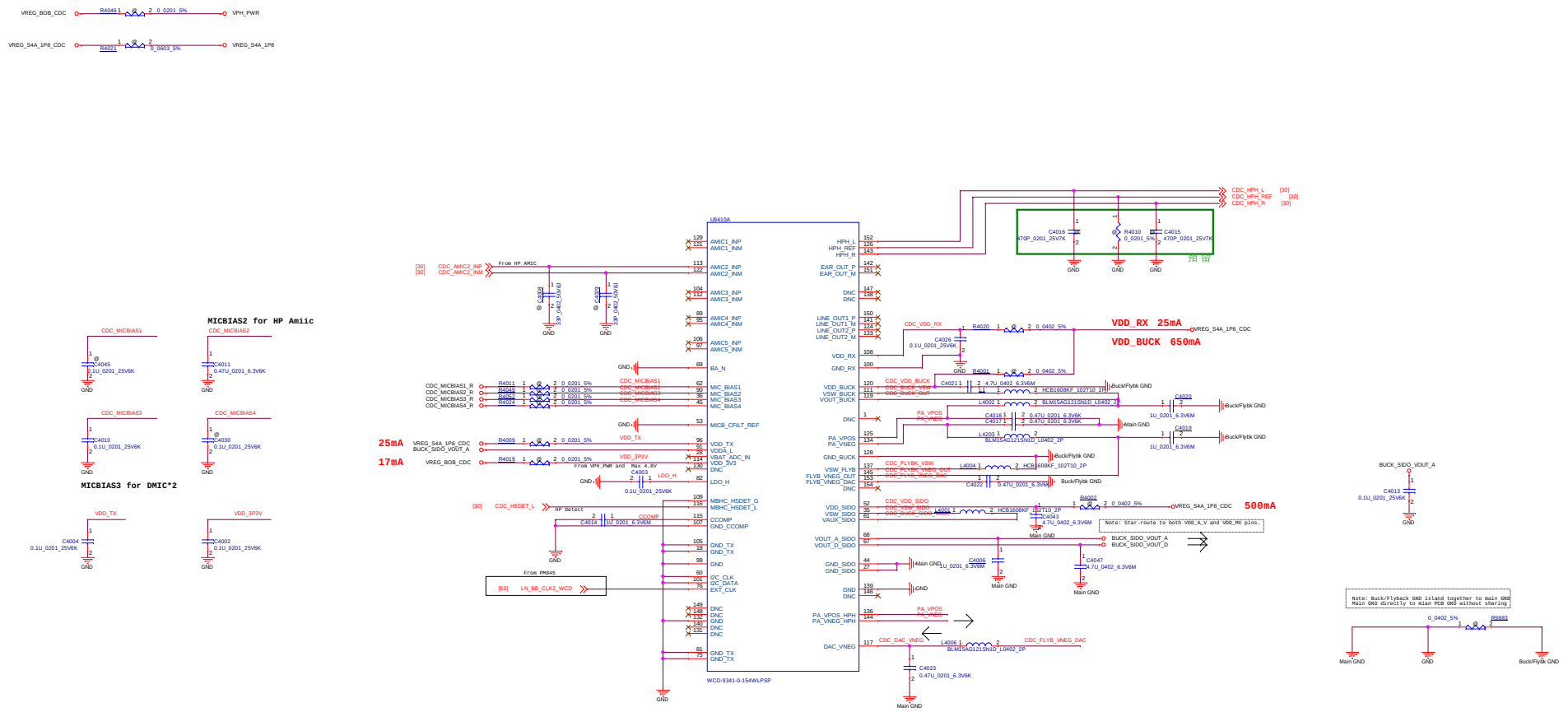

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Title: **WCD9341**

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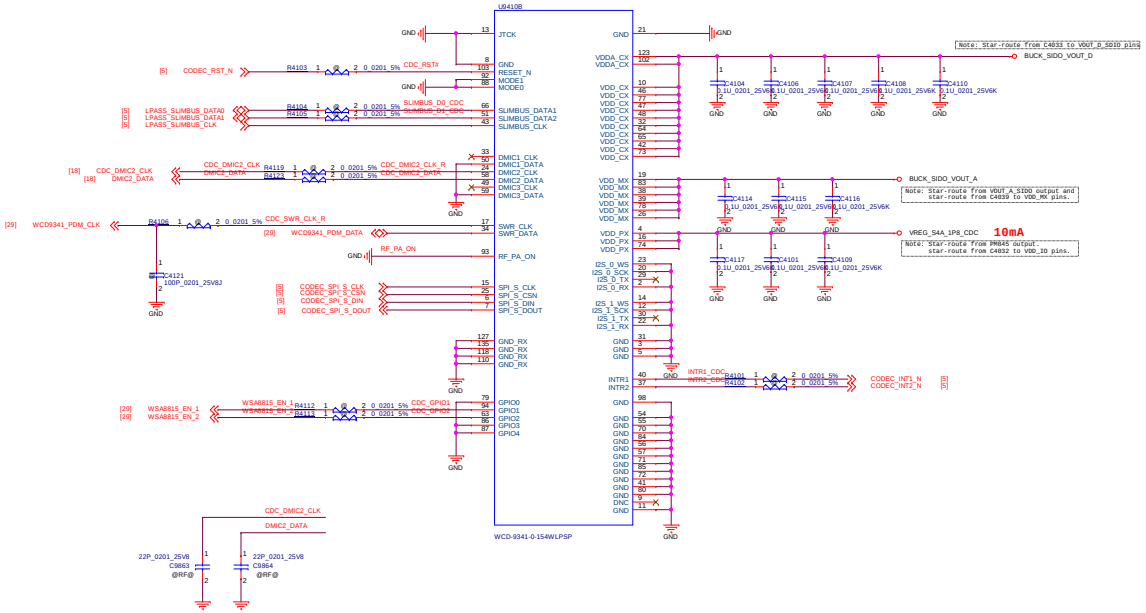

MIC Select	Assert data on	latch data on
High	Rising clock edge	Falling clock edge
Low	Falling clock edge	Rising clock edge

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Issued Date	2018/01/30	Deciphered Date	2018/10/30

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Title: WCD9341

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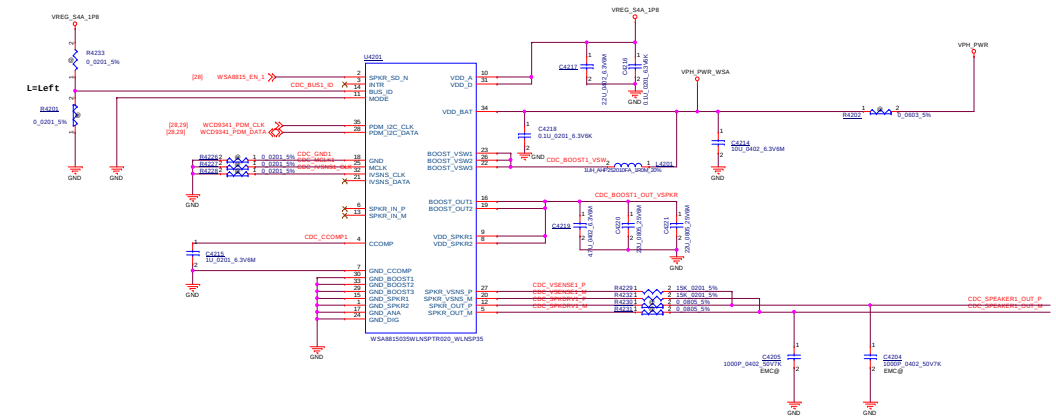
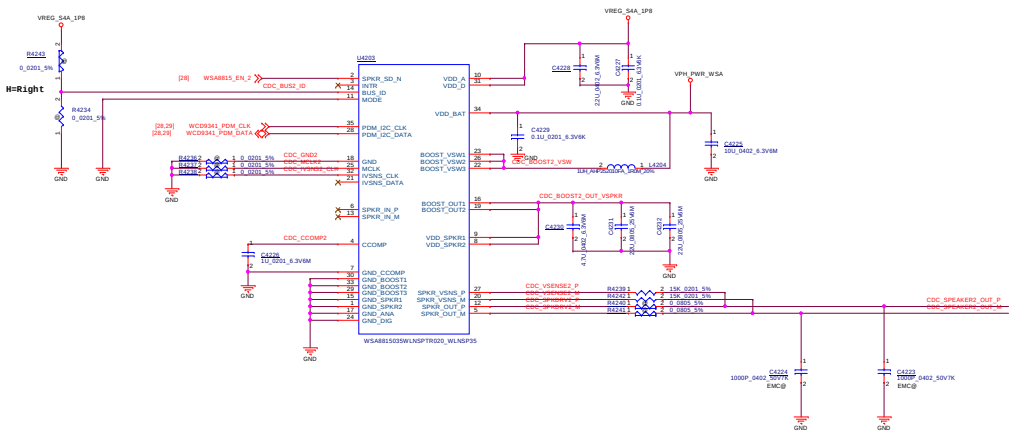
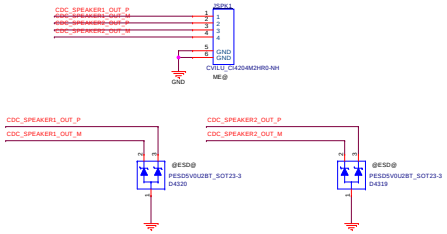
WSA8815 Digital interface AMP x 2







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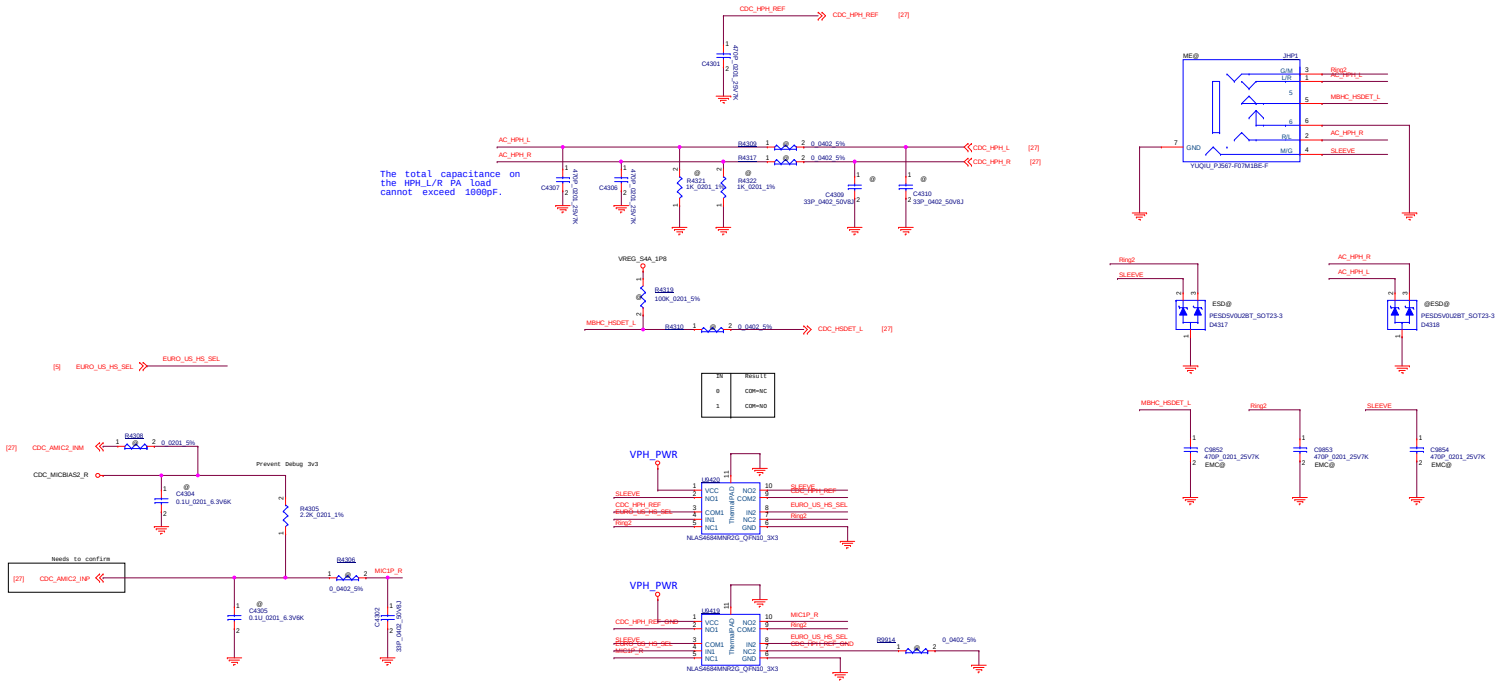
			Date: Wednesday, August 01, 2018 / Sheet 29 of 57



EURO_US_HS_SEL

0 : SLEEVE=MIC (CTIA)
1 : Ring2=MIC (OMTP)

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Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: AUDIO JACK
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				Date: Wednesday, August 01, 2018; Sheet 30 of 57

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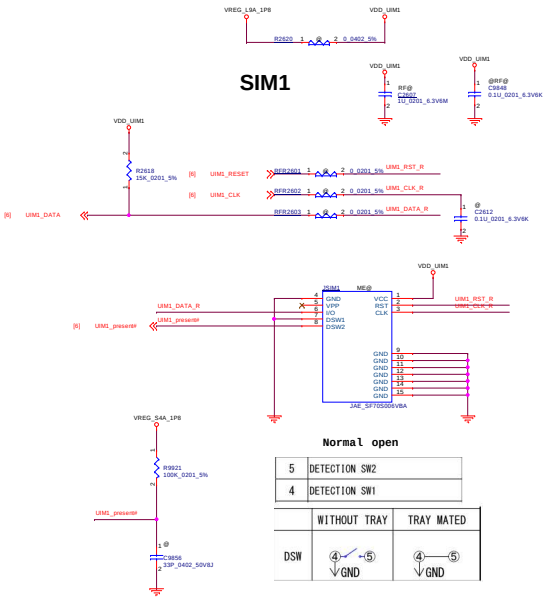
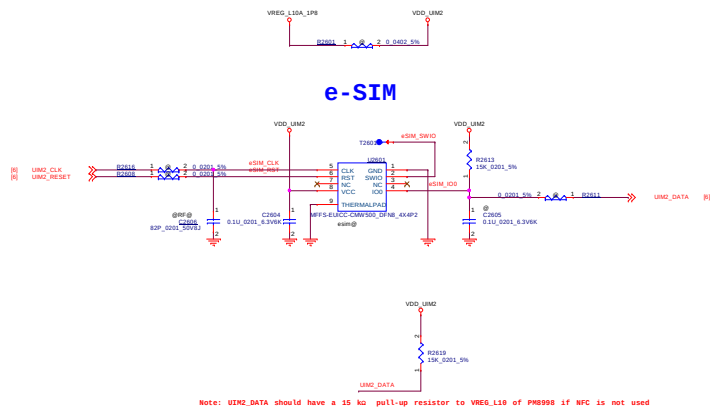


Normal open

5	DETECTION SW2
4	DETECTION SW1

	WITHOUT TRAY	TRAY MATED
DSW	④ ⑤ GND	④ ⑤ GND



Note: UIM2_DATA should have a 15 kΩ pull-up resistor to VREG_L10 of PM8998 if NFC is not used

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Issued Date	2018/01/30	Deciphered Date	2018/10/30

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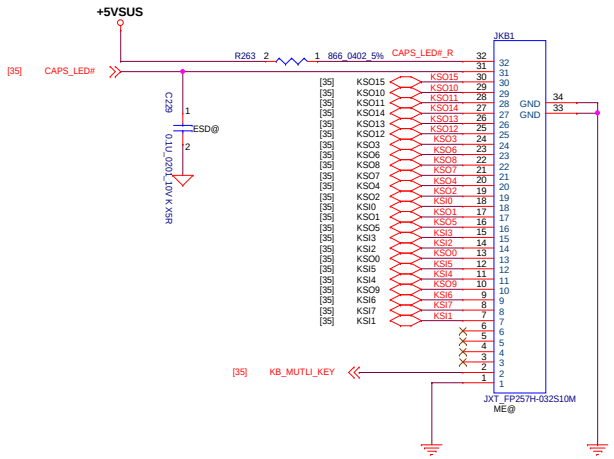
Title: e-SIM/Nano SIM

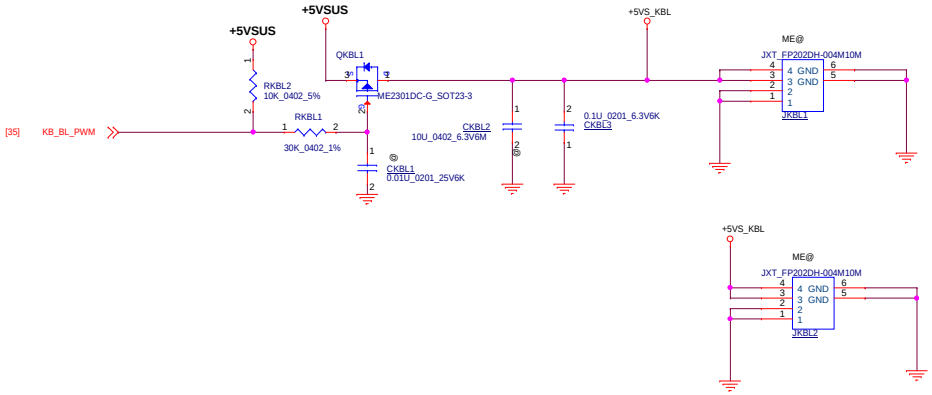
Size: D | Document Number: LA-G611P | Rev: 1.0

Date: Wednesday, August 15, 2018 | Sheet 32 of 57

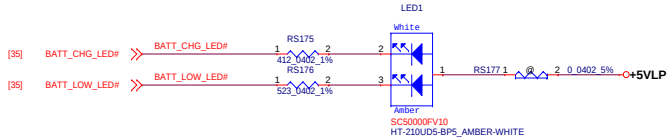
Keyboard



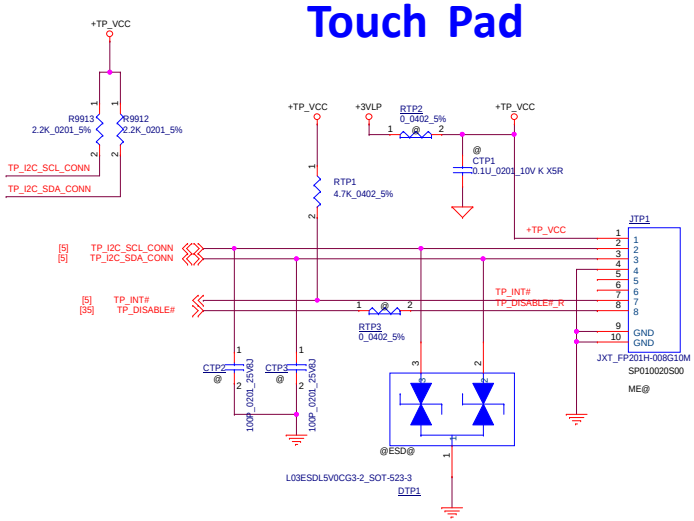
Keyboard Backlight



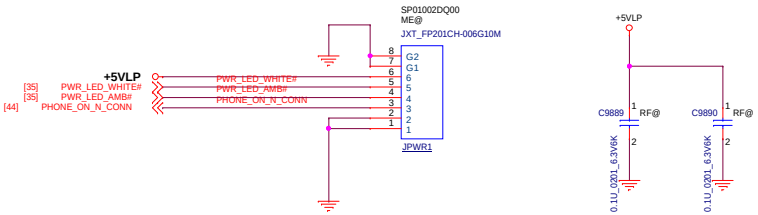
BATT LED

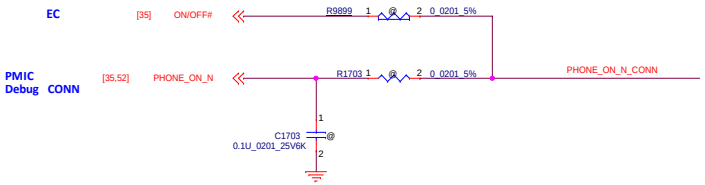


Touch Pad



PWR/B





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Issued Date	2018/01/30	Deciphered Date	2018/10/30

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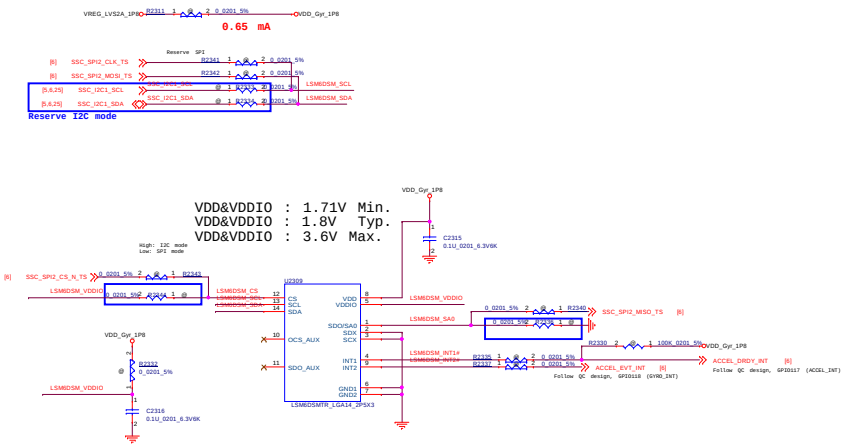
Compal Electronics, Inc.

Title: **KB/TP/KBL/LED/PWRB**

Size: C | Document Number: **LA-G611P** | Rev: 1.0

Date: Monday, August 13, 2018 | Sheet 33 of 57

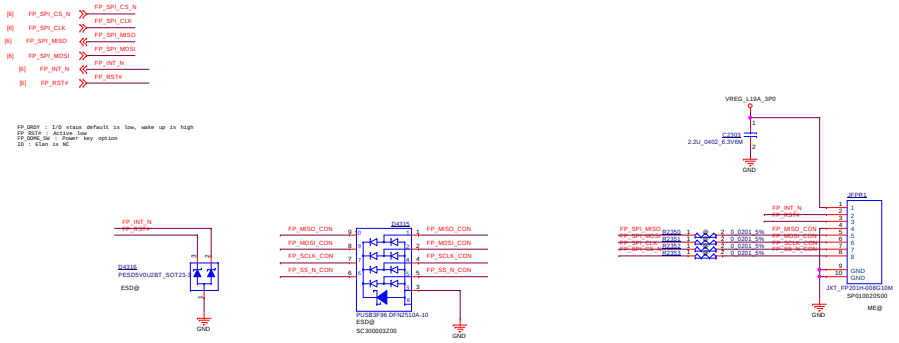
Gyroscope and Accelerometer
ST LSM6DSM



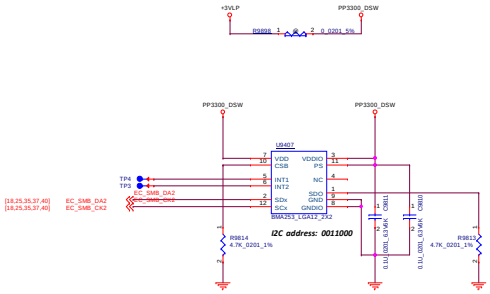
SA0 Low : I2C Address 1101010 (0x6A)
SA0 High : I2C Address 1101011 (0x6B)

If the SA0 is connect to ground, the LSb value is 0(1101010). else if SA0 is high then LSb is 1(1101011)

Finger Print



G-SENSOR



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Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: Sensor/FPR
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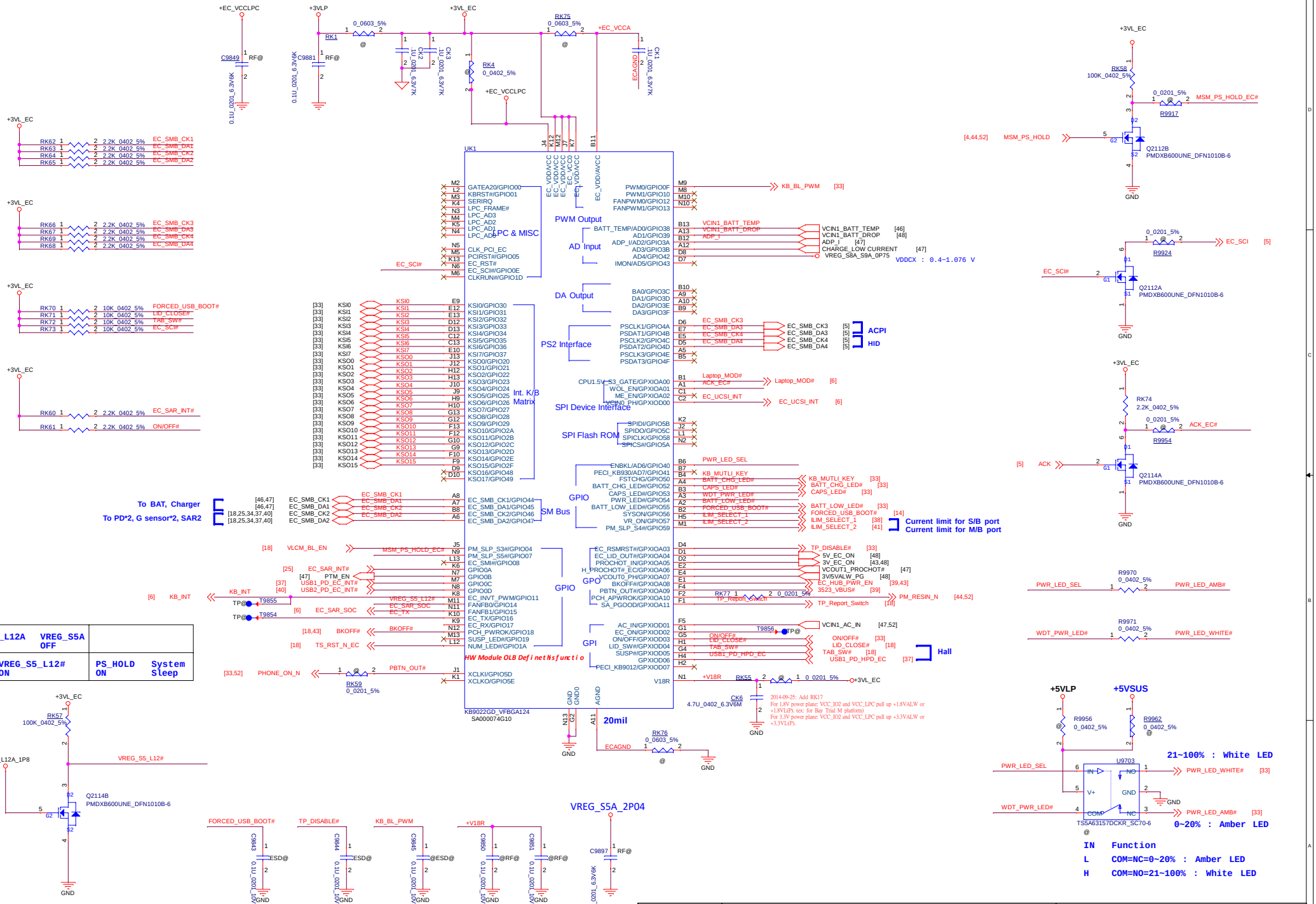
				Date: Wednesday, August 01, 2018; Sheet 34 of 57



Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

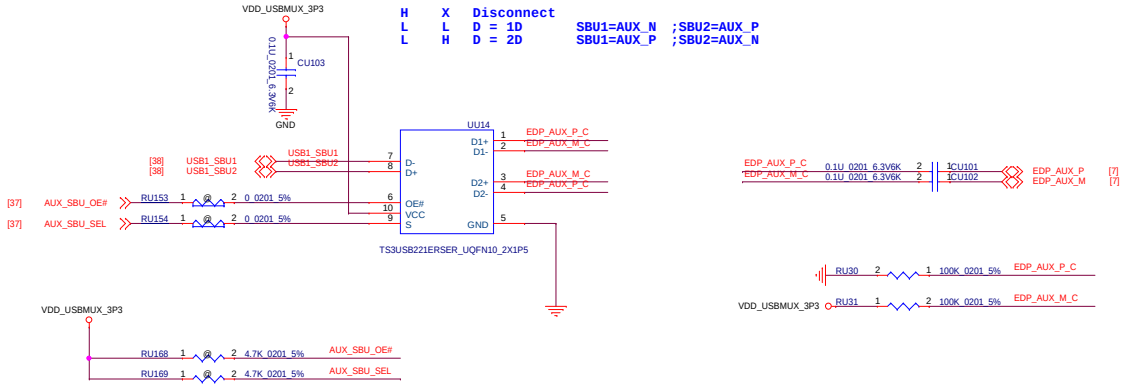
Title: **EC ENE-KB9022GD**

Size: Custom | Document Number: **LA-G611P** | Rev: 1.0

Date: Wednesday, August 15, 2018 | Sheet 35 of 57

AUX/SBU for port 1

OE#	S	Function	
H	X	Disconnect	
L	L	D = 1D	SBU1=AUX_N ;SBU2=AUX_P
L	H	D = 2D	SBU1=AUX_P ;SBU2=AUX_N



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Issued Date	2018/01/30	Deciphered Date	2018/10/30

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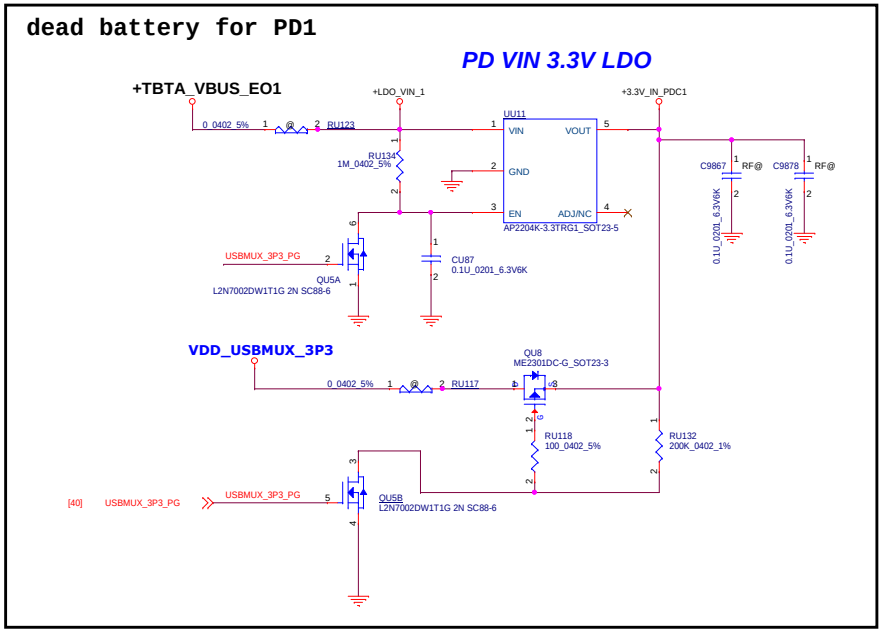
Compal Electronics, Inc.

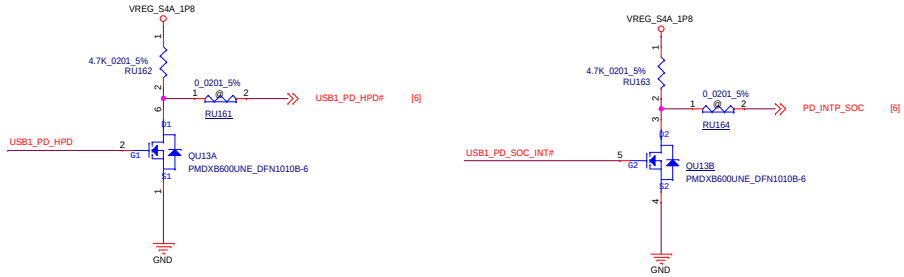
Title: **TypeC_AUX/SBU_Port1**

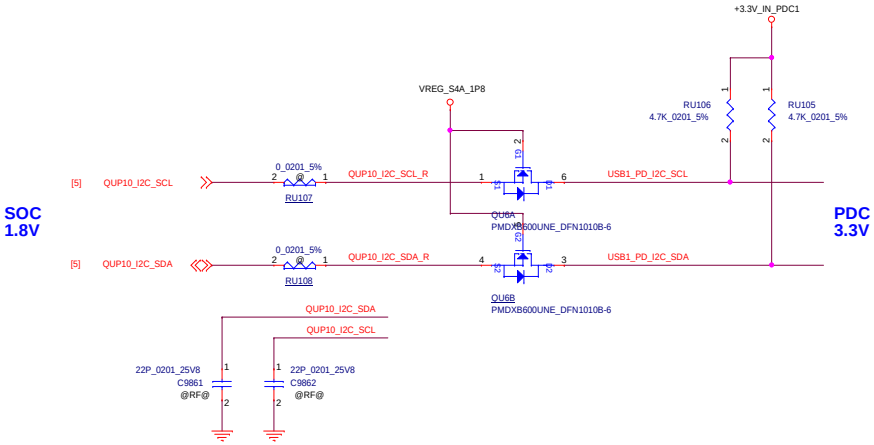
Size: C | Document Number: **LA-G611P** | Rev: 1.0

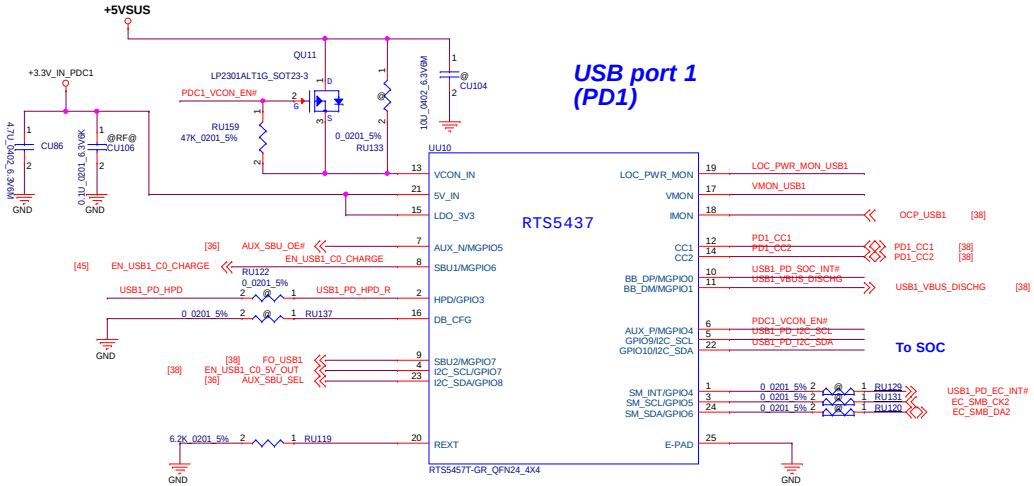
Date: Wednesday, August 01, 2018 | Sheet 36 of 57

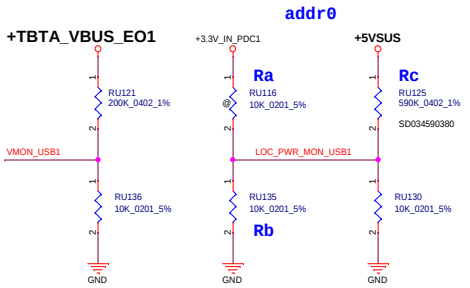
Type C port 1



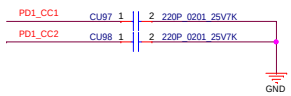


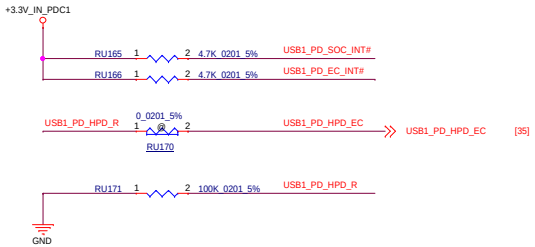


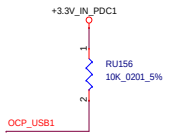




DB_CFG
Dead battery function Cfig. pin.
Tie to GND to disable dead battery ' Rd'
Floating to enable dead battery ' Rd'







If local power voltage is less than or equal to 6V, use the resistor value in the table below.

Slave Addr	Ra 1%	Rb 1%	Rc 1%
addr0	NC	10K	590K
addr1	54.9K	12.1K	
addr2	27.4K	15.8K	
addr3	18.2K	22.1K	

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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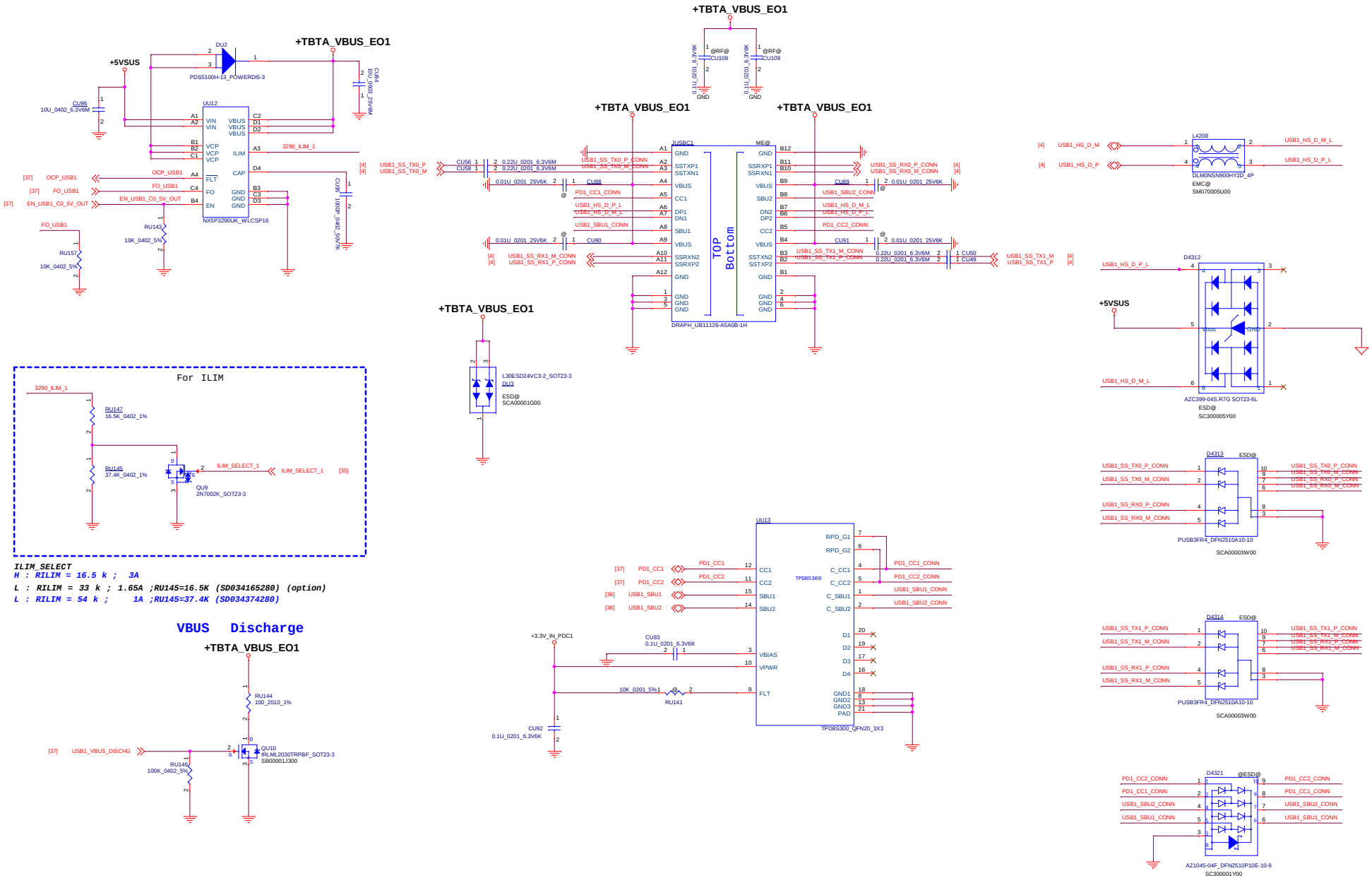
Compal Electronics, Inc.

Title: PDC_RTS5457T_Port1

Size: C | Document Number: LA-G611P | Rev: 1.0

Date: Monday, August 13, 2018 | Sheet 37 of 57

Type C port 1



ILIM_SELECT

H : RILIM = 16.5 k ; 3A

L : RILIM = 33 k ; 1.65A ;RU145=16.5K (SD034165280) (option)

L : RILIM = 54 k ; 1A ;RU145=37.4K (SD034374280)

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Issued Date	2018/01/30	Deciphered Date 2018/10/30	Title: TypeC CONN_Port1
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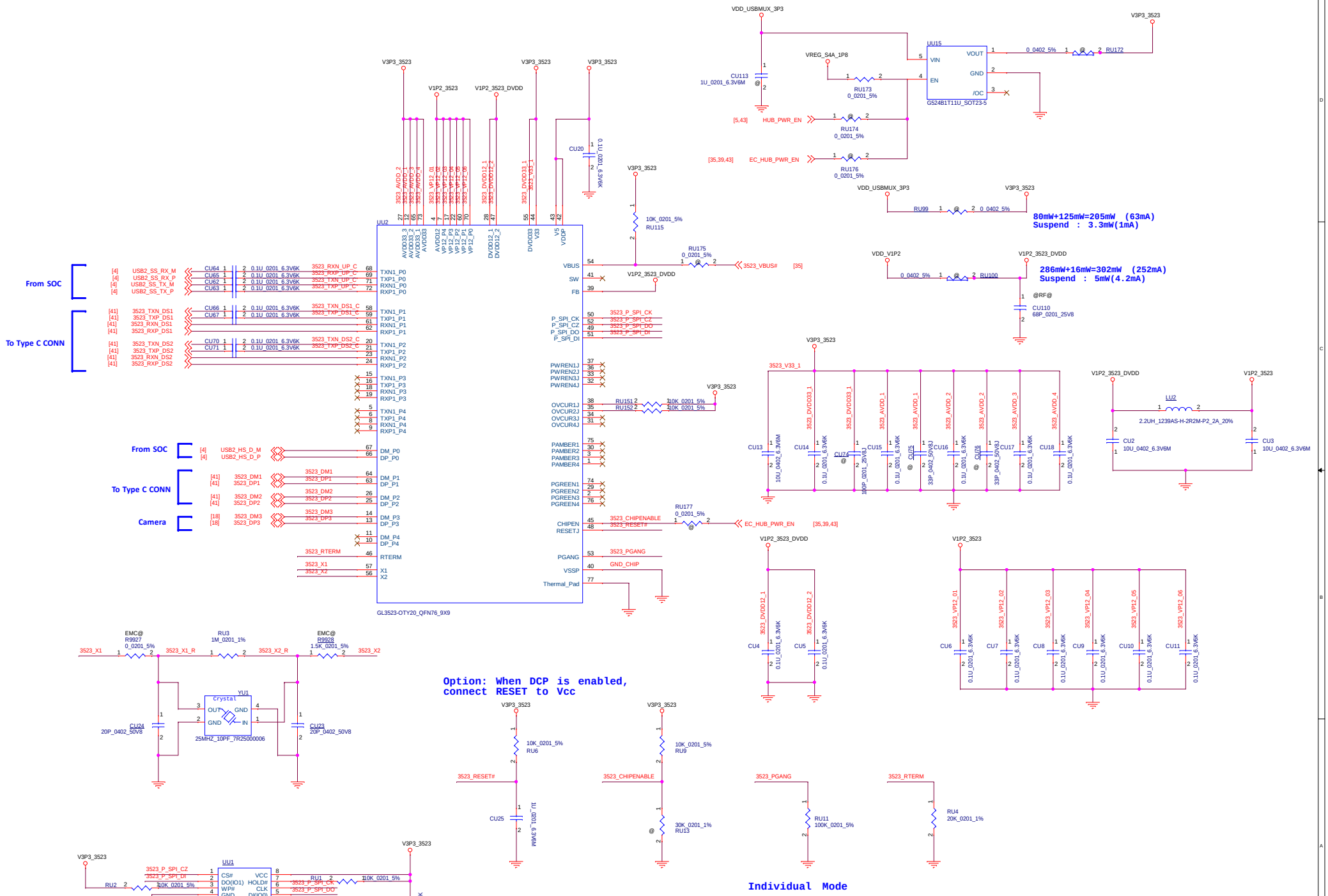
			Date: Monday, August 06, 2018; Sheet 38 of 57

USB 3.0 HUB



Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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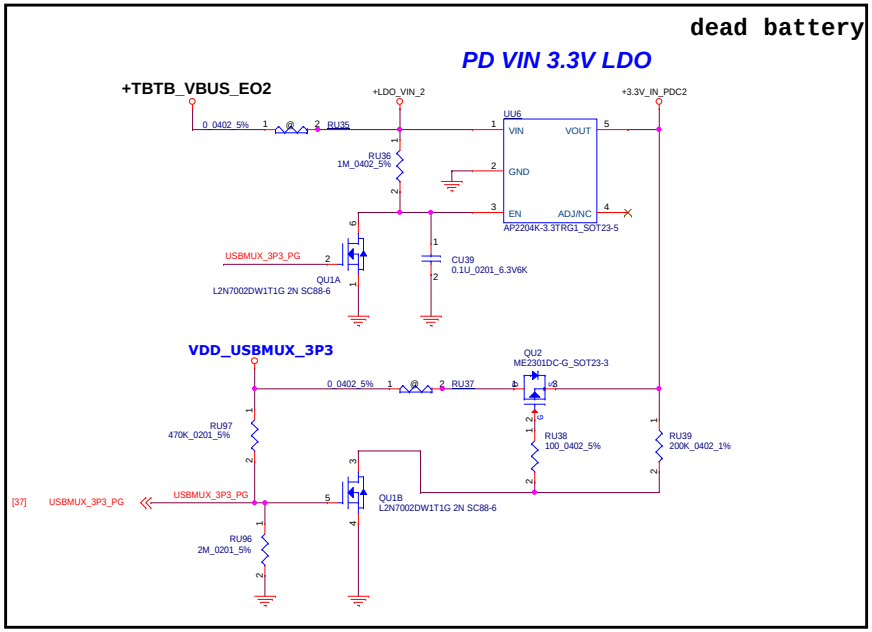
Compal Electronics, Inc.

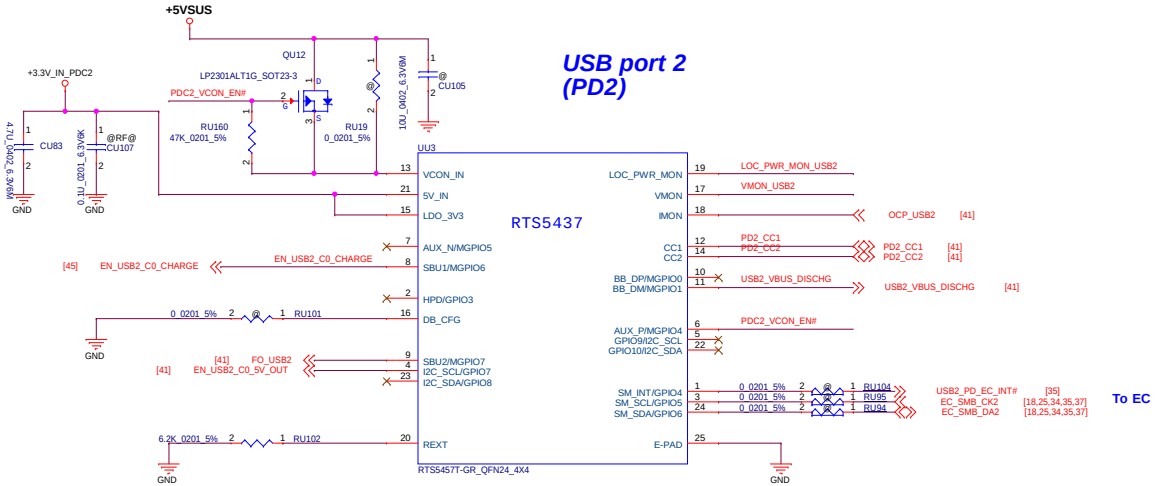
Title: **USB3 HUB**

Size: C | Document Number: **LA-G611P** | Rev: 1.0

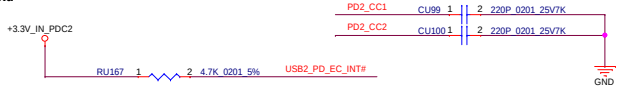
Date: Wednesday, August 01, 2018 | Sheet 39 of 57

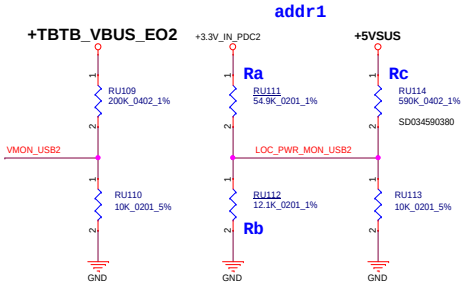
Type C port 2

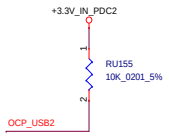




DB_CFG
Dead battery function Cfig. pin.
Tie to GND to disable dead battery ' Rd'
Floating to enable dead battery ' Rd'







If local power voltage is less than or equal to 6V, use the resistor value in the table below.

Slave Addr	Ra 1%	Rb 1%	Rc 1%
addr0	NC	10K	590K
addr1	54.9K	12.1K	
addr2	27.4K	15.8K	
addr3	18.2K	22.1K	

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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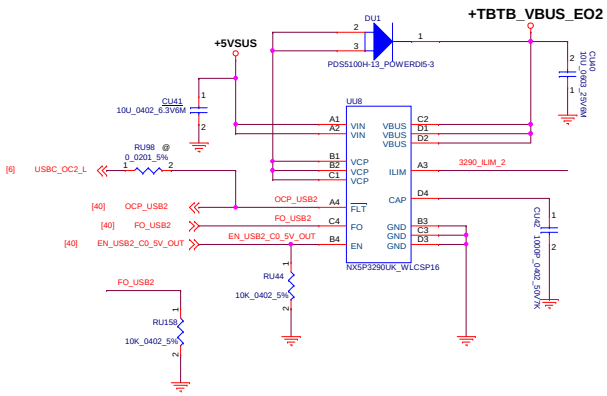
Compal Electronics, Inc.

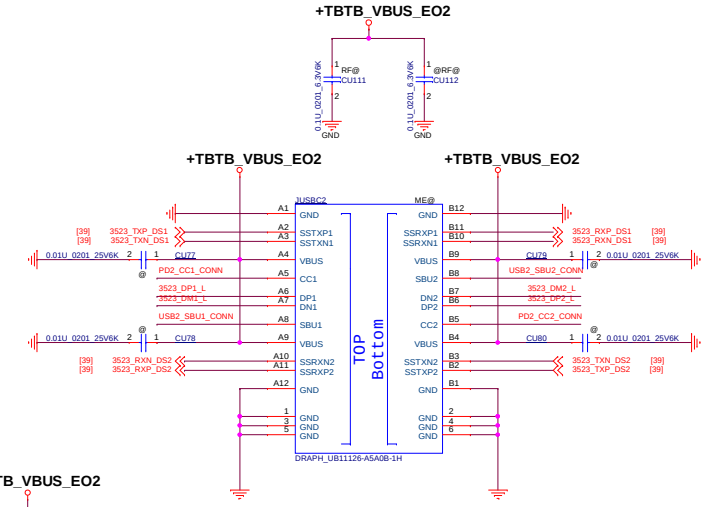
Title: PDC_RTS5457T_Port2

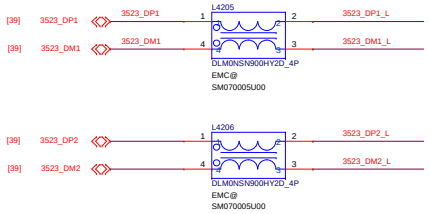
Size: C | Document Number: LA-G611P | Rev: 1.0

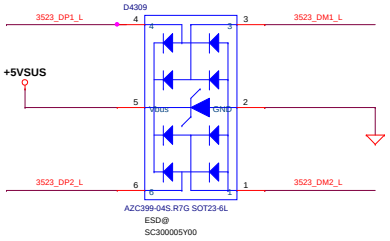
Date: Monday, August 13, 2018 | Sheet 40 of 57

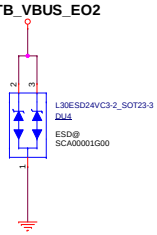
Type C port 2

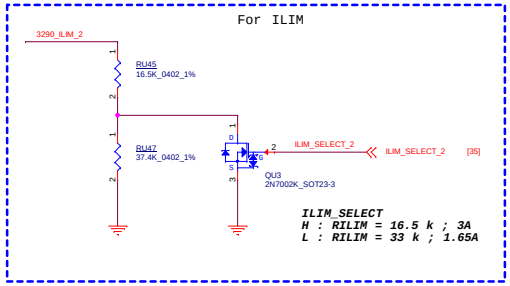


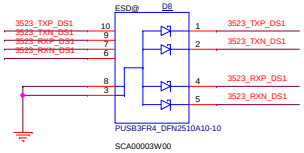


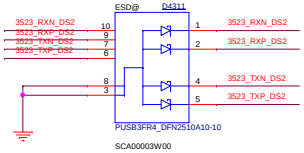






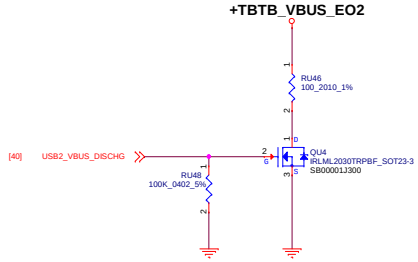


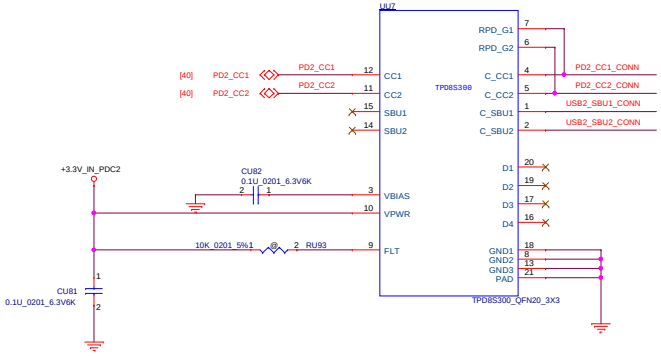




ILIM_SELECT
H : RILIM = 16.5 k ; 3A
L : RILIM = 33 k ; 1.65A ;RU47=16.5K (SD034165280) (option)
L : RILIM = 54 k ; 1A ;RU47=37.4K (SD034374280)

VBUS Discharge





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Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: TypeC CONN_Port2
				Size: Custom; Document Number: LA-G611P; Rev: 1.0
				Date: Wednesday, August 01, 2018; Sheet 41 of 57

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Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

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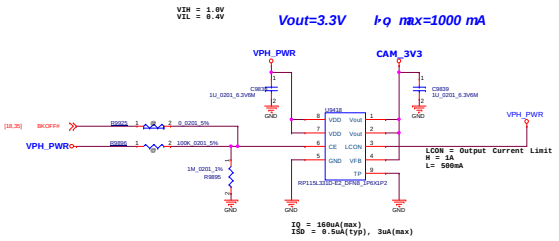
Size	Document Number	Rev
C	LA-G611P	1.0

Date: Wednesday, August 01, 2018 | Sheet 42 of 57

3V3_Camera



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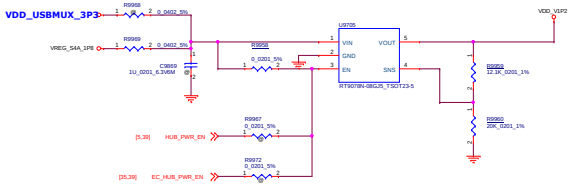

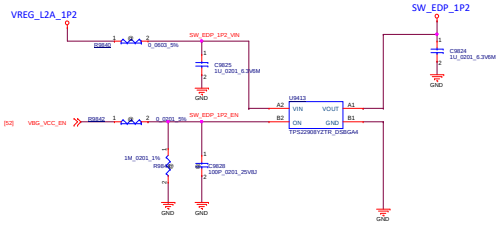

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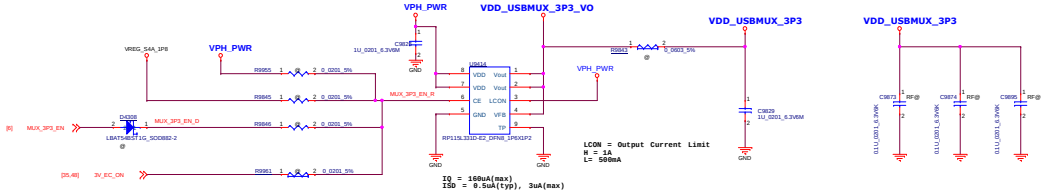

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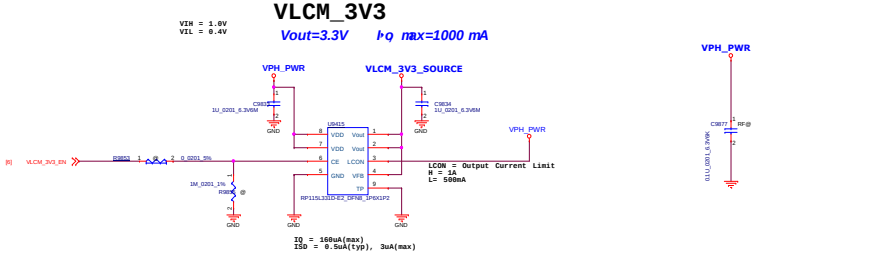

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: LDO
				Size: A1 / Document Number: LA-G611P / Rev: 1.0
				Date: Tuesday, August 14, 2018 / Sheet 43 of 57

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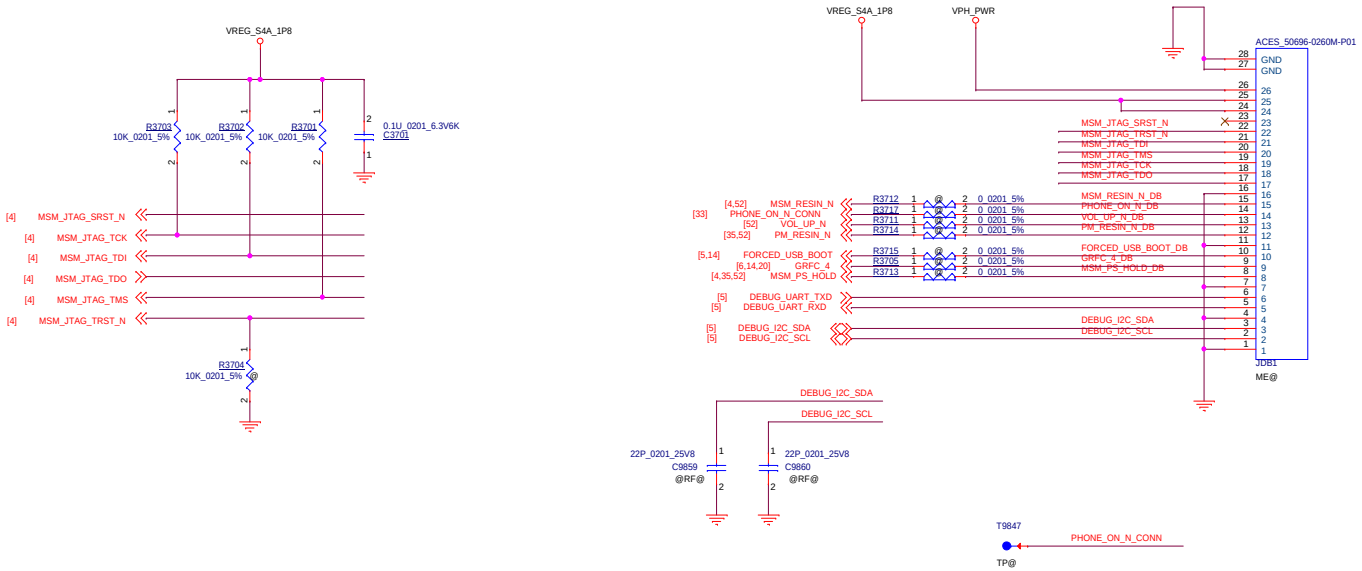
DEBUG CONNECTOR



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: DB CONN
				Size: C; Document Number: LA-G611P; Rev: 1.0
				Date: Wednesday, August 01, 2018; Sheet 44 of 57

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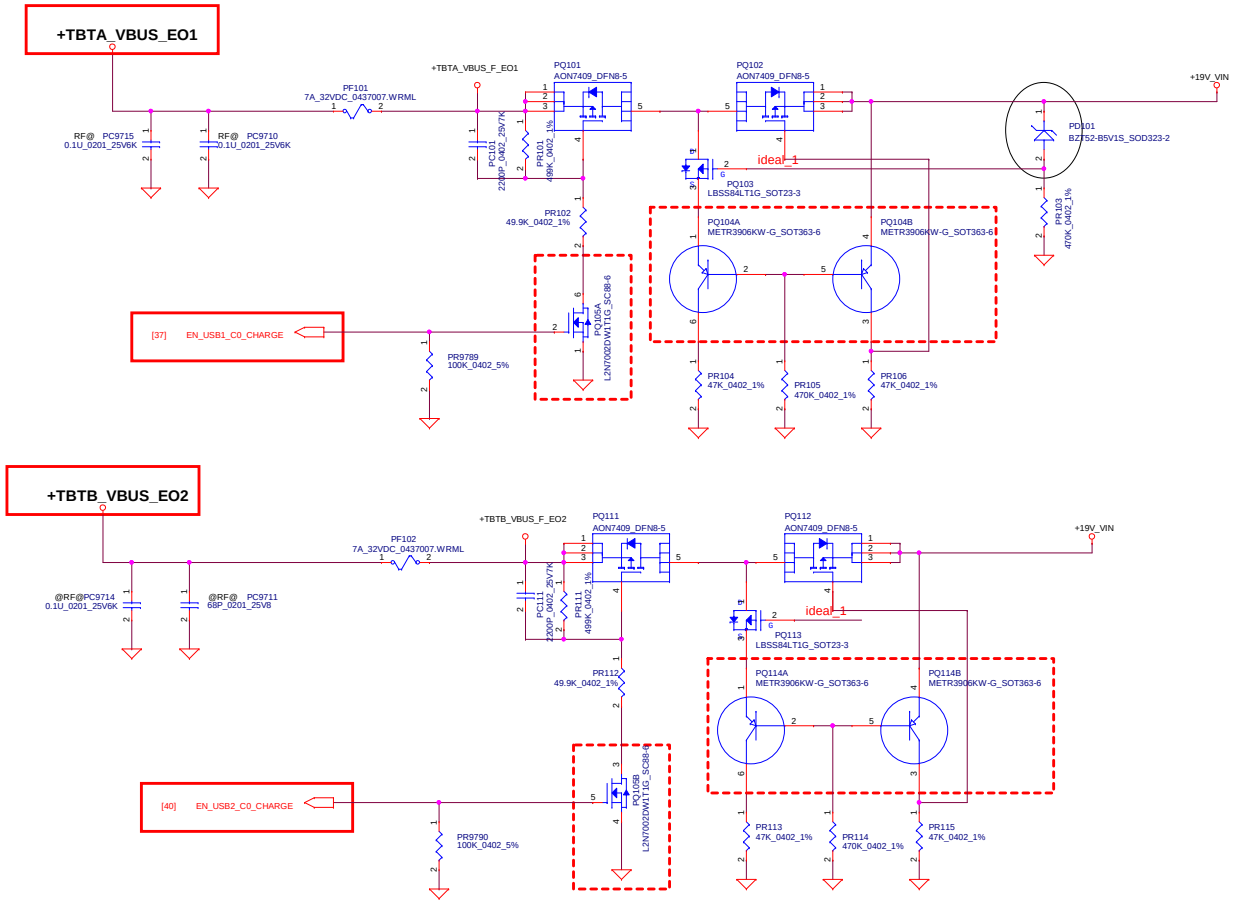

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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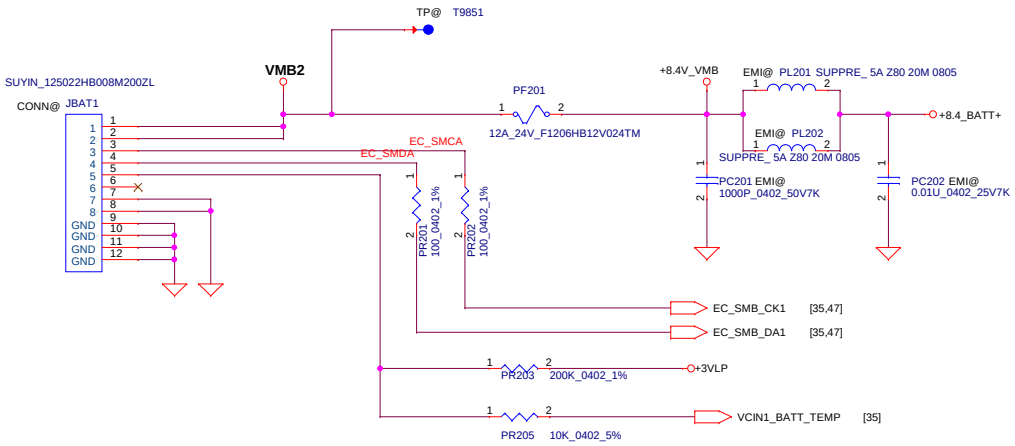
Compal Electronics, Inc.

Title: **TYPE-C IN**

Size: Custom | Document Number: **LA-G611P** | Rev: 1.0

Date: Wednesday, August 01, 2018 | Sheet 45 of 57



Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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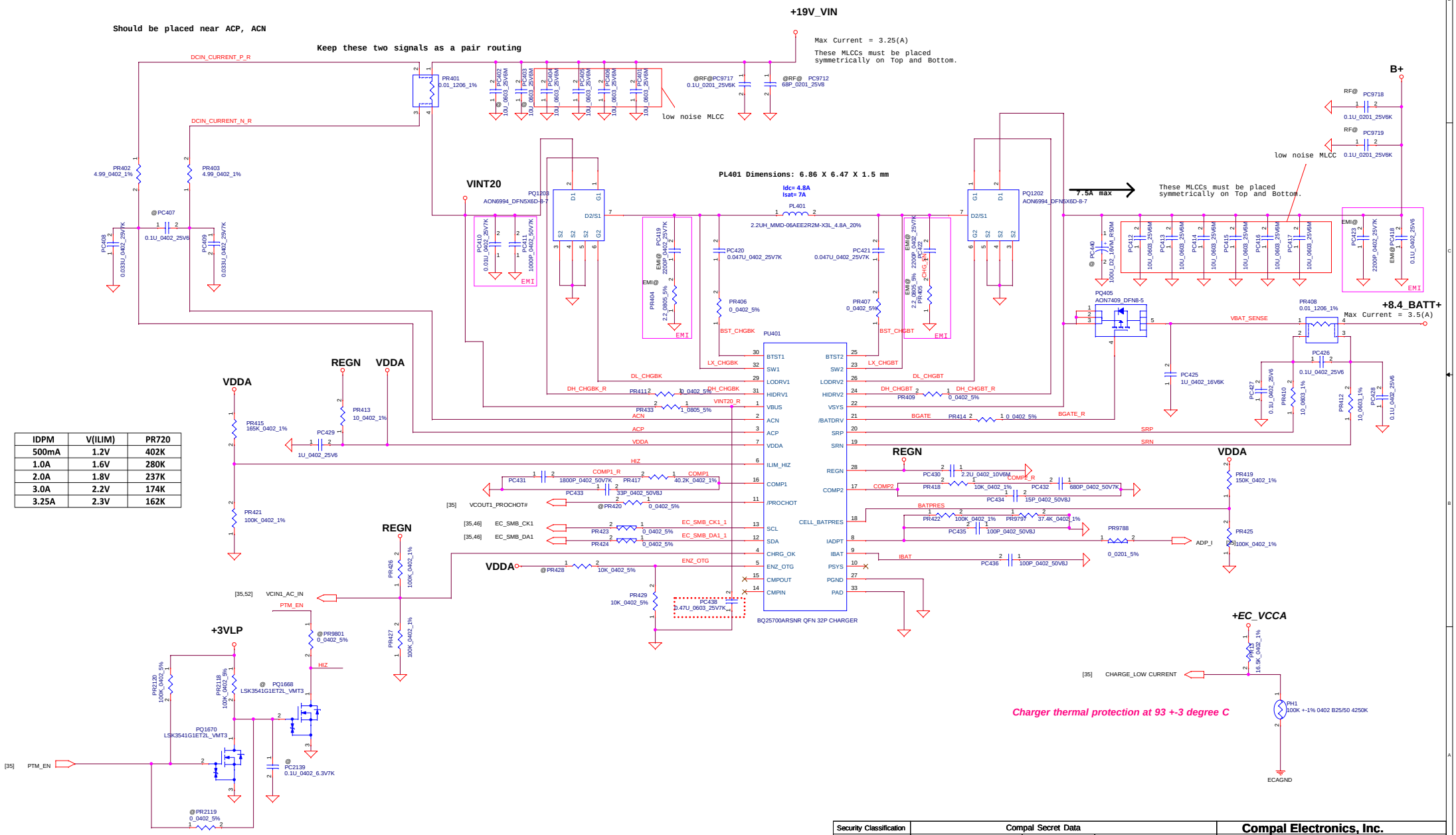
Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size: Custom | Document Number: **LA-G611P** | Rev: 1.0

Date: Wednesday, August 01, 2018 | Sheet 46 of 57



IDPM	V(ILIM)	PR720
500mA	1.2V	402K
1.0A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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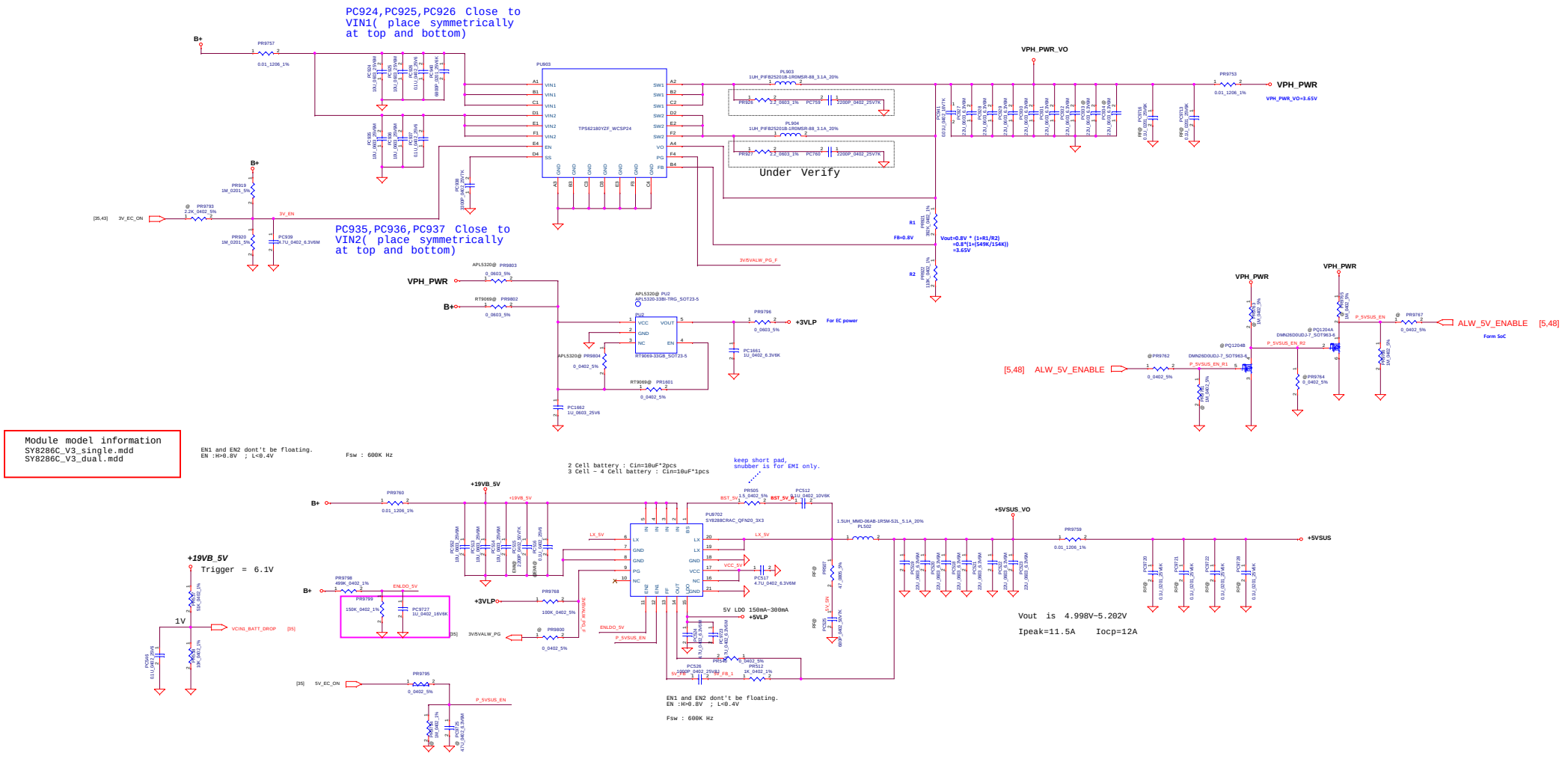
Compal Electronics, Inc.

Title: BATTERY CHARGER(BQ25700)

Size: Custom | Document Number: LA-G611P | Rev: 1.0

Date: Wednesday, August 01, 2018 | Sheet 47 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: +3VALW/+5VALW
Size: D	Document Number: LA-G611P			Rev: 1.0
Date: Wednesday, August 01, 2018	Sheet 48 of 57			

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84_PMIC_PM845_BUCK1

PM845 Regulator

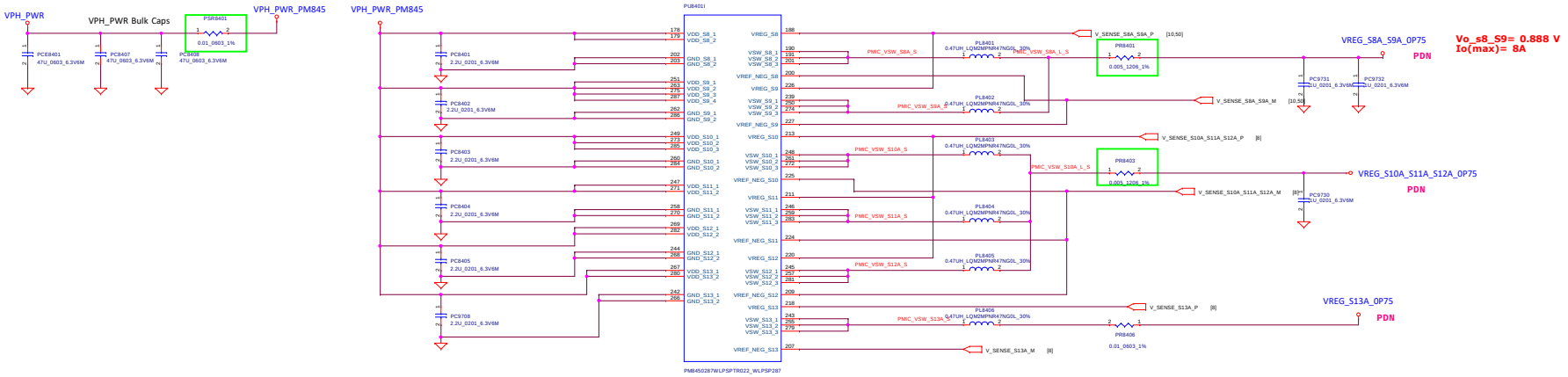
Regulator	I_rated(mA)	Voltage(V)
S1	2000	0.8
S2	2500	1.128
S3	2500	1.352
S4	2850	1.8
S5	1100	2.04
S6	4000	0.8
S7	3600	1.028
S8	4000	0.752
S9	4000	0.752
S10	4000	0.756
S11	4000	0.752
S12	4000	0.752
S13	4000	0.752

PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
L16	300	2.704
L17	600	1.304
L18	50	2.704
L19	600	3.008
L20	800	2.96
L21	800	2.96
L22	150	2.864
L23	600	3.312
L24	150	3.088
L25	600	3.312
L26	600	1.2
L27	600	0.752
L28	150	3.008
L29(VREF_SP)	50	1.904
LVS1	300	1.8
LVS2	100	1.8

PM8005 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	4000	0.752
S2	3000	0.752
S3	2000	0.6
S4	4000	0.752



Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

Title: PMIC PM845 Buck1

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85_PMIC_PM845_BUCK2

PM845 Regulator

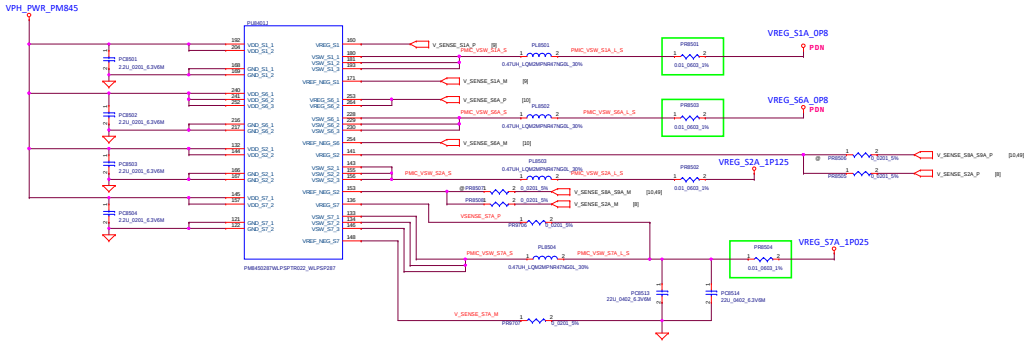
Regulator	I_rated(mA)	Voltage(V)
S1	2000	0.8
S2	2500	1.128
S3	2500	1.352
S4	2850	1.8
S5	1100	2.04
S6	4000	0.8
S7	3600	1.028
S8	4000	0.752
S9	4000	0.752
S10	4000	0.756
S11	4000	0.752
S12	4000	0.752
S13	4000	0.752

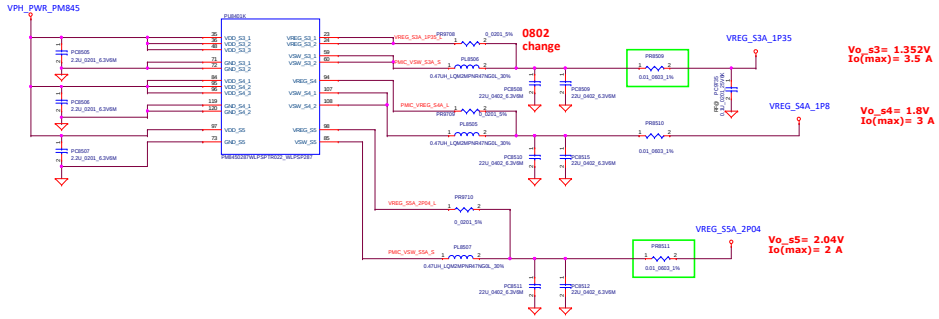
PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
L16	300	2.704
L17	600	1.304
L18	50	2.704
L19	600	3.008
L20	800	2.96
L21	800	2.96
L22	150	2.864
L23	600	3.312
L24	150	3.088
L25	600	3.312
L26	600	1.2
L27	600	0.752
L28	150	3.008
L29(VREF_SP)	50	1.904
LVS1	300	1.8
LVS2	100	1.8

PM8005 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	4000	0.752
S2	3000	0.752
S3	2000	0.6
S4	4000	0.752





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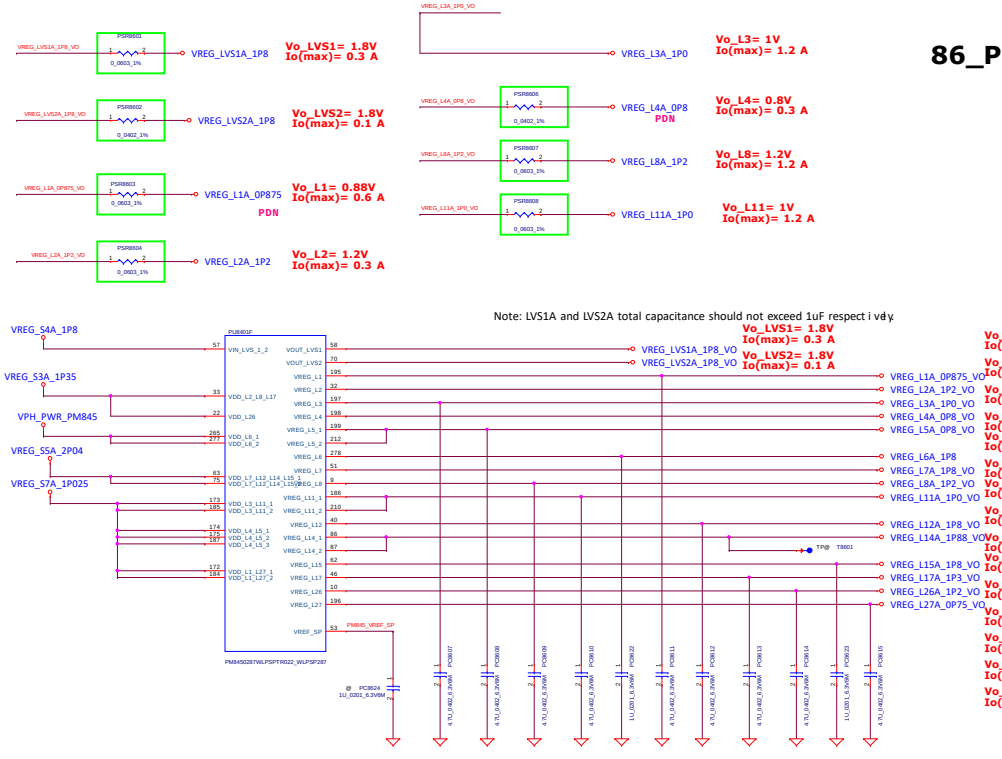
Compal Electronics, Inc.

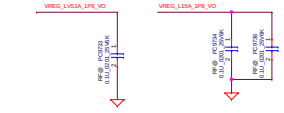
Title: PMIC_PM845_Buck2

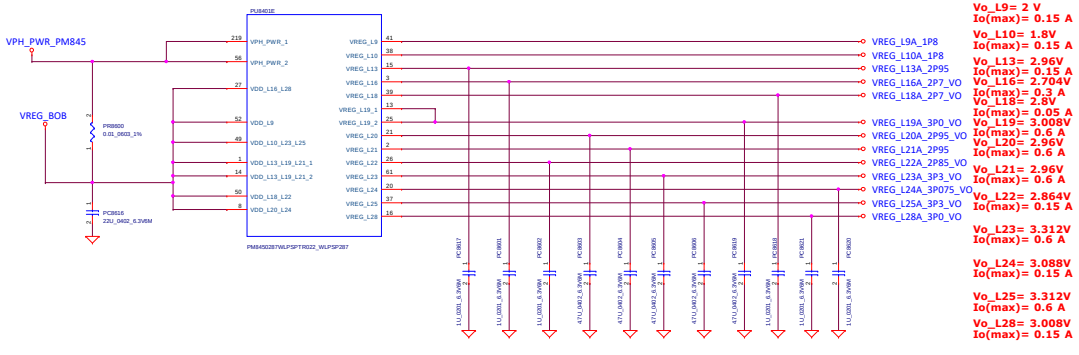
Size: | Document Number: LA-G611P | Rev: 1.0

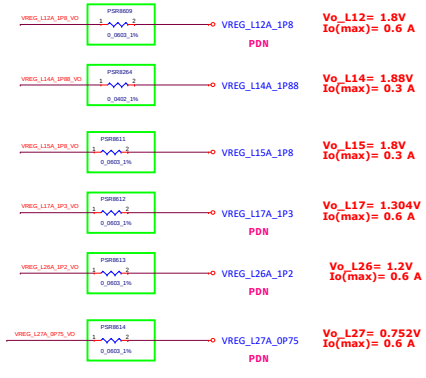
Date: Wednesday, August 01, 2018 | Sheet 55 of 57

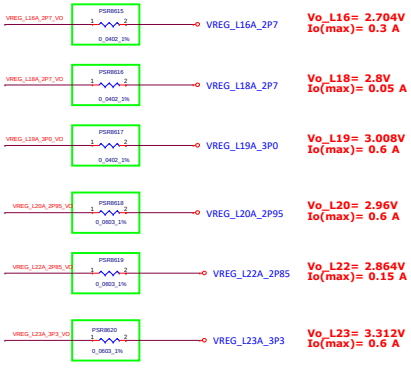
86_PMIC_PM845_LDO

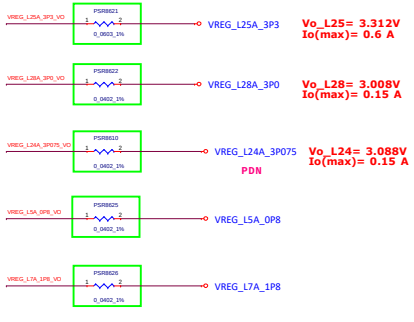












PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	2000	0.8
S2	2500	1.128
S3	2500	1.352
S4	2850	1.8
S5	1100	2.04
S6	4000	0.8
S7	3600	1.028
S8	4000	0.752
S9	4000	0.752
S10	4000	0.756
S11	4000	0.752
S12	4000	0.752
S13	4000	0.752

PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
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L18	50	2.704
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L21	800	2.96
L22	150	2.864
L23	600	3.312
L24	150	3.088
L25	600	3.312
L26	600	1.2
L27	600	0.752
L28	150	3.008
L29(VREF_SP)	50	1.904
LVS1	300	1.8
LVS2	100	1.8

PM8005 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	4000	0.752
S2	3000	0.752
S3	2000	0.6
S4	4000	0.752

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: PMIC_PM845_LDO
Size: A1	Document Number: LA-G611P			Rev: 1.0
Date: Wednesday, August 01, 2018	Sheet 51 of 57			

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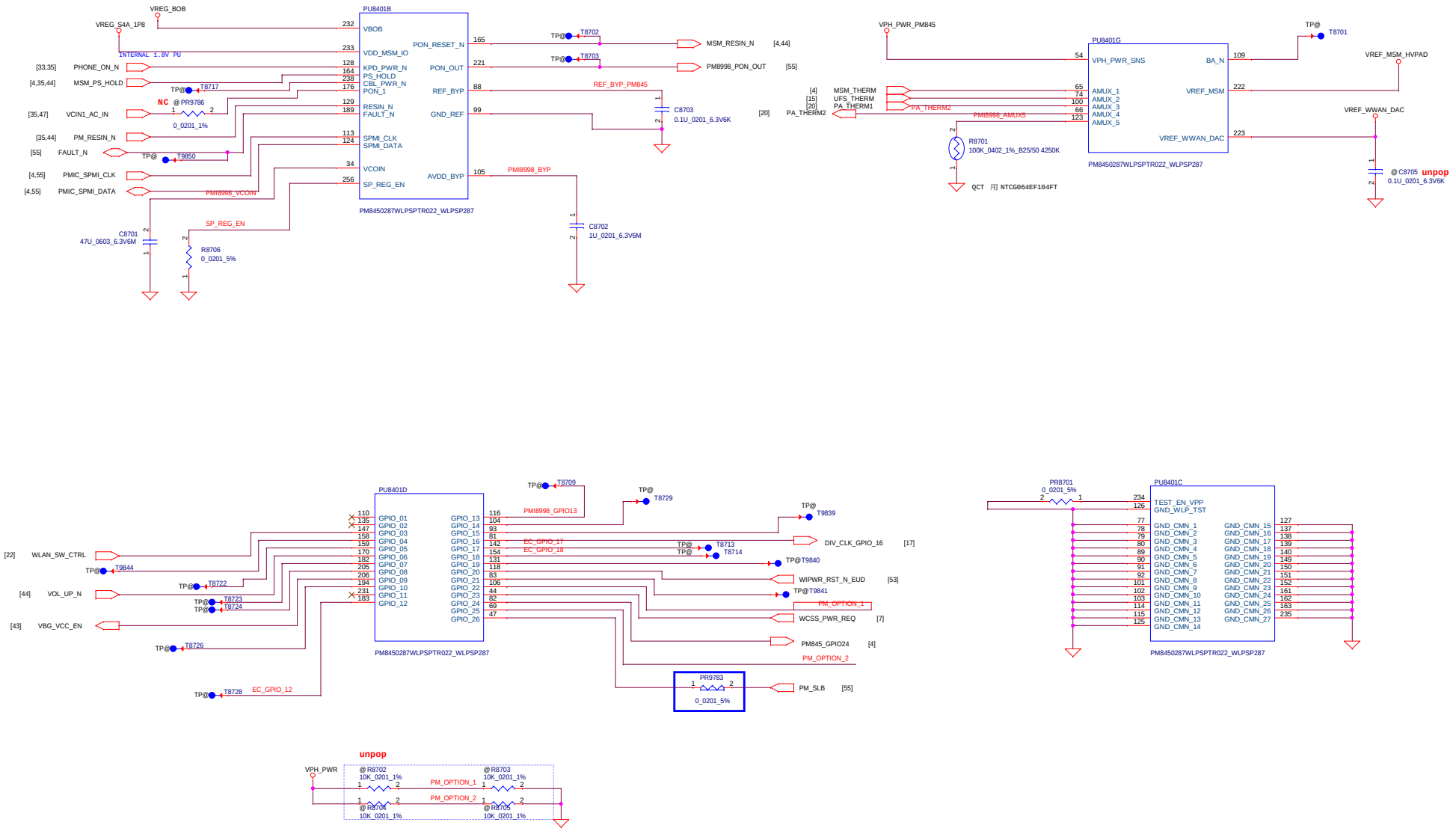

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Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: PWR_PMIC_PM845 CTL & GPIO
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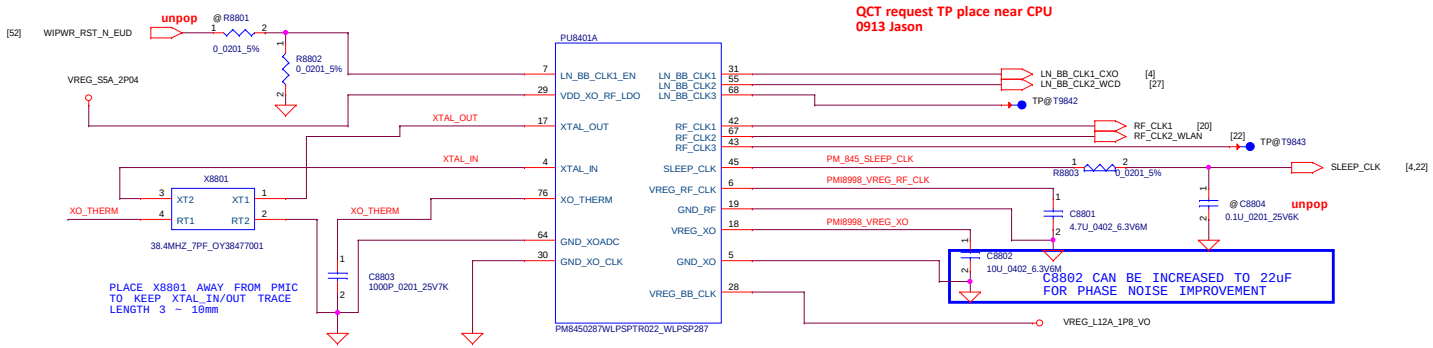
				Date: Wednesday, August 01, 2018 / Sheet 52 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: PWR PMIC PM845 CLKS
				Size: C; Document Number: LA-G611P; Rev: 1.0
				Date: Wednesday, August 01, 2018; Sheet 53 of 57

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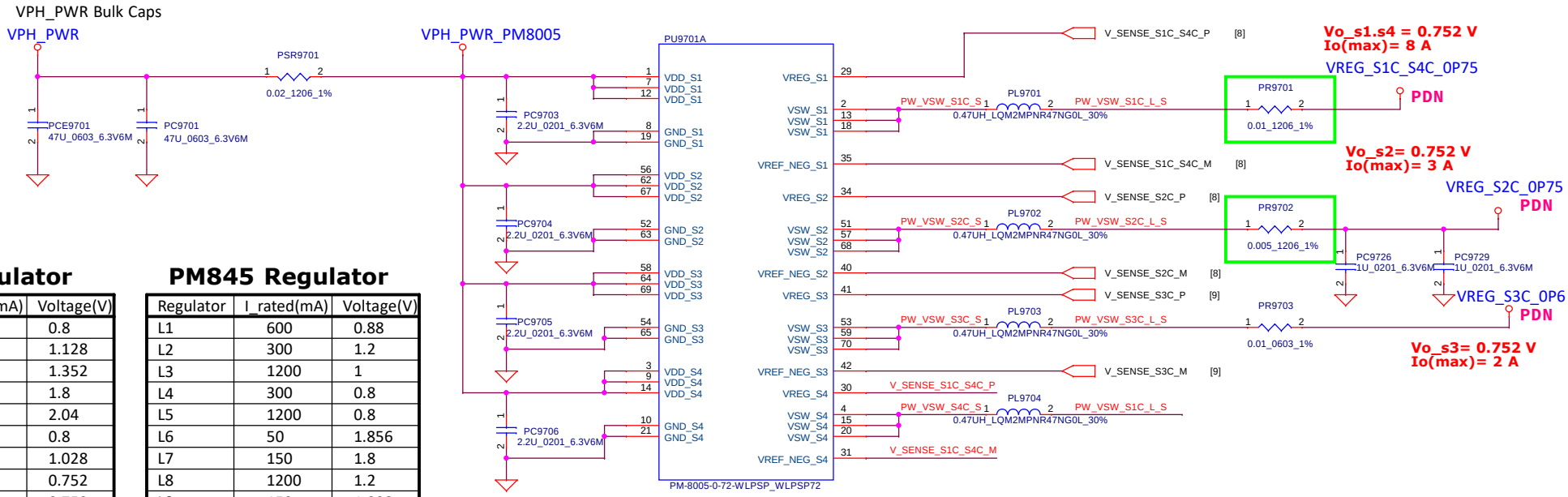
97_PMIC_PM8005_BUCK



PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	2000	0.8
S2	2500	1.128
S3	2500	1.352
S4	2850	1.8
S5	1100	2.04
S6	4000	0.8
S7	3600	1.028
S8	4000	0.752
S9	4000	0.752
S10	4000	0.756
S11	4000	0.752
S12	4000	0.752
S13	4000	0.752

PM8005 Regulator

Regulator	I_rated(mA)	Voltage(V)
S1	4000	0.752
S2	3000	0.752
S3	2000	0.6
S4	4000	0.752

PM845 Regulator

Regulator	I_rated(mA)	Voltage(V)
L1	600	0.88
L2	300	1.2
L3	1200	1
L4	300	0.8
L5	1200	0.8
L6	50	1.856
L7	150	1.8
L8	1200	1.2
L9	150	1.808
L10	150	1.8
L11	1200	1
L12	300	1.8
L13	150	2.96
L14	300	1.8
L15	300	1.8
L16	300	2.704
L17	600	1.304
L18	50	2.704
L19	600	3.008
L20	800	2.96
L21	800	2.96
L22	150	2.864
L23	600	3.312
L24	150	3.088
L25	600	3.312
L26	600	1.2
L27	600	0.752
L28	150	3.008
L29(VREF_SP)	50	1.904
LVS1	300	1.8
LVS2	100	1.8

Security Classification	Compal Secret Data		
Issued Date	2018/01/30	Deciphered Date	2018/10/30

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Title: **PWR_PM8005_BUCK**

Size: A3 | Document Number: **LA-G611P** | Rev: 1.0

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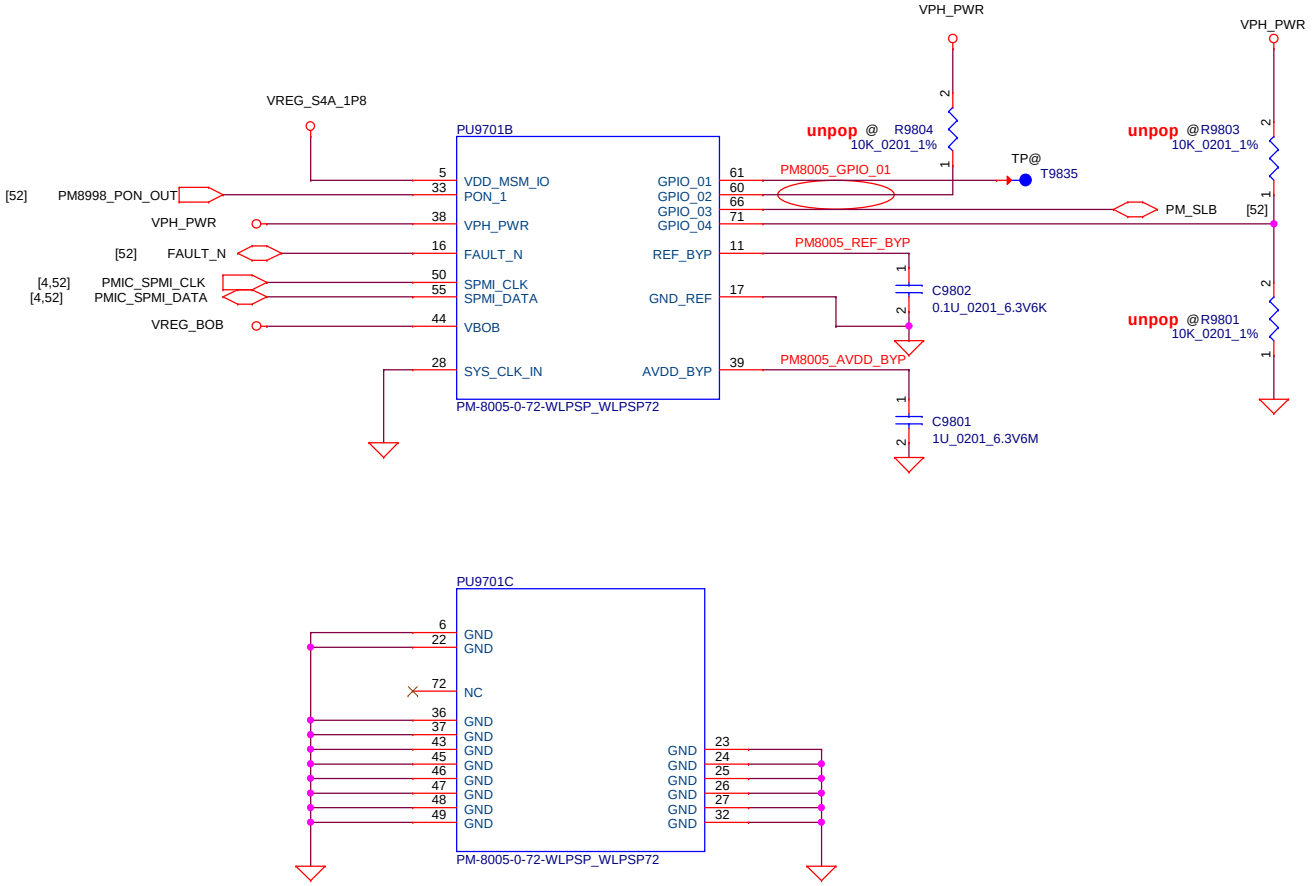

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Issued Date	2018/01/30	Deciphered Date	2018/10/30	Title: PWR_PM8005 Control
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For energy star	47	Add PC2139, PQ1668, PQ1670, PR2118, PR2119, PR2120 for charger PTM (Pass Through Mode)	20180423	SDV
2	For ME height restrict area	47	PC438 change to 0.68u_0603_25V size	20180423	SDV
3					
4					
5					
6					
7					
8					

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Title: PIR

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