# SP9 BLOCK DIAGRAM

01

**PCB STACK UP**

Discrete 8L

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND2
LAYER 8 : Bottom

BATTERY SELECTOR PAGE 46
SYSTEM CHARGER(BQ24704) PAGE 46
SYSTEM POWER RT8206B PAGE 39
DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 44
VCCP +1.5V AND GMCH 1.05V(ISL62872) PAGE 40
VDDCI RT8209A PAGE 42
VGACORE ISL6264 PAGE 43
CPU CORE NCP6131S52MNR2G
CPU CORE NCP5911 PAGE 47\48

**intel**
Intel Sandy
4 Core
rPGA 988
(37.5mm X 37.5mm)
CPU 45Watt
35Watt
DDR SYSTEM MEMORY
PCI-E X16
FDI
DMI
P3~P6

10.8GT/s → Embedded DisplayPort P26

DDR III
SO-DIMM 0
SO-DIMM 1
P12, 13
Dual Channel
1066/1333 MHz

VRAM GDDR5*8
32*32\64*16\128*16
P20~P23

PCIE 5GT/s → ATI GPU
Granville-LP
(16 x 64Mb\128Mb x 8pcs)
P14~P19
X'TAL 27.0MHz

EXT_CRT / INT_CRT → CRT Switchable P24 → CRT P27
EXT_LVDS / INT_LVDS → LVDS Switchable P24 → LVDS P24
EXT_DisplayPort / INT_DisplayPort → DP\eDP Switch PS8321 P26 → DP\eDP Port P26
EXT_HDMI / INT_HDMI → HDMI Switch PI3HDMI201 P28 → HDMI P28

FDI interface 2.7GT/s
X4 DMI interface 5GT/s

HDD (SATA) P33 — SATA0
HDD (SATA) P33 — SATA1
ODD (SATA) P33 — SATA4
eSATA/USB Port x 1 P33 — USB1/ SATA5

**intel**
<PCH>
FDI
DMI
SATA Gen3
SATA Gen2
SATA Gen2
USB
HDA
SPI
LPC
iGFX Interfaces
RTC
P9
PCI-E
Platform Controller Hub
mBGA 989
(25mm X 25mm)
P8~P11

INT_CRT
INT_LVDS
INT_DisplayPort
INT_HDMI

X'TAL 32.768KHz

PCI-Express Gen2 5GT/s
PCIE3 → NEC USB3.0 DB P38 → USB2/3 Combo X1
PCIE2 → Realtek Giga-LAN RTL8111E P32 (X'TAL 25MHz)
PCIE1 → Mini-card (Wireless LAN Shirley Peak 802.11a/b/g/n) P37

USB 2.0
USB Port*2 USB8&9 P34
Bluetooth USB13 P34
Webcam w/ Mic USB4 P34
CardReader RTS5159 USB12 P34

Azalia
Audio Codec IDT92HD80 P29
Amplifier TPA6130A2 P29
Amplifier TPA3111D1 P30
Combo Jack (Headphone/MIC) P30
Line out (Headphone) P30
Int Speaker P27
Sub-Woofer P29

Dual SPI ROM 4MB x1 (Basic ME+Braidwood) P7
EC KB3926 D2 P36 (X'TAL 32.768KHz)
SPI ROM P36
Touch Pad P34
Keyboard P35
SYSTEM/GPU FAN P37
Accelerometer LIS3LV02DL P30

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 1A |

N85/RD2

Date: Tuesday, August 10, 2010 Sheet 1 of 49

# Sandy Bridge Processor (DMI,PEG,FDI)

# Sandy Bridge Processor (CLK,MISC,JTAG)

02

U39A

DMI

Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

U39B

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Close to EC

8/10 SI Modify

CPU RESET#

SM_DRAMPWROK Processor Input.

7/27 SI Modify

3/26 DB del for DG update.

5/4 DB add.

4/20 DB add.

3/26 DB for H/W modify.

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils.

CPU XDP

DDR3 DRAM RESET

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

## FDI disable (DIS only stuff)

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

## PEG x16 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

## Embedded Display PLL Clock

| | Ra | Rb | Rc |
|---|---|---|---|
| DIS | NC | Stuff | Stuff |
| SG/UMA | Stuff | NC | NC |

## DP & PEG Compensation\ Hot-plug

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up (CPU)

| | | |
|---|---|---|
| H_PROCHOT# | R186 | 62_4 |
| XDP_TDO | R591 | 51_4 |
| XDP_TMS | R589 | 51_4 |
| XDP_TDI_R | R200 | 51_4 |
| XDP_PREQ# | R203 | *51_4 |
| XDP_TCLK | R592 | 51_4 |
| XDP_TRST# | R587 | 51_4 |

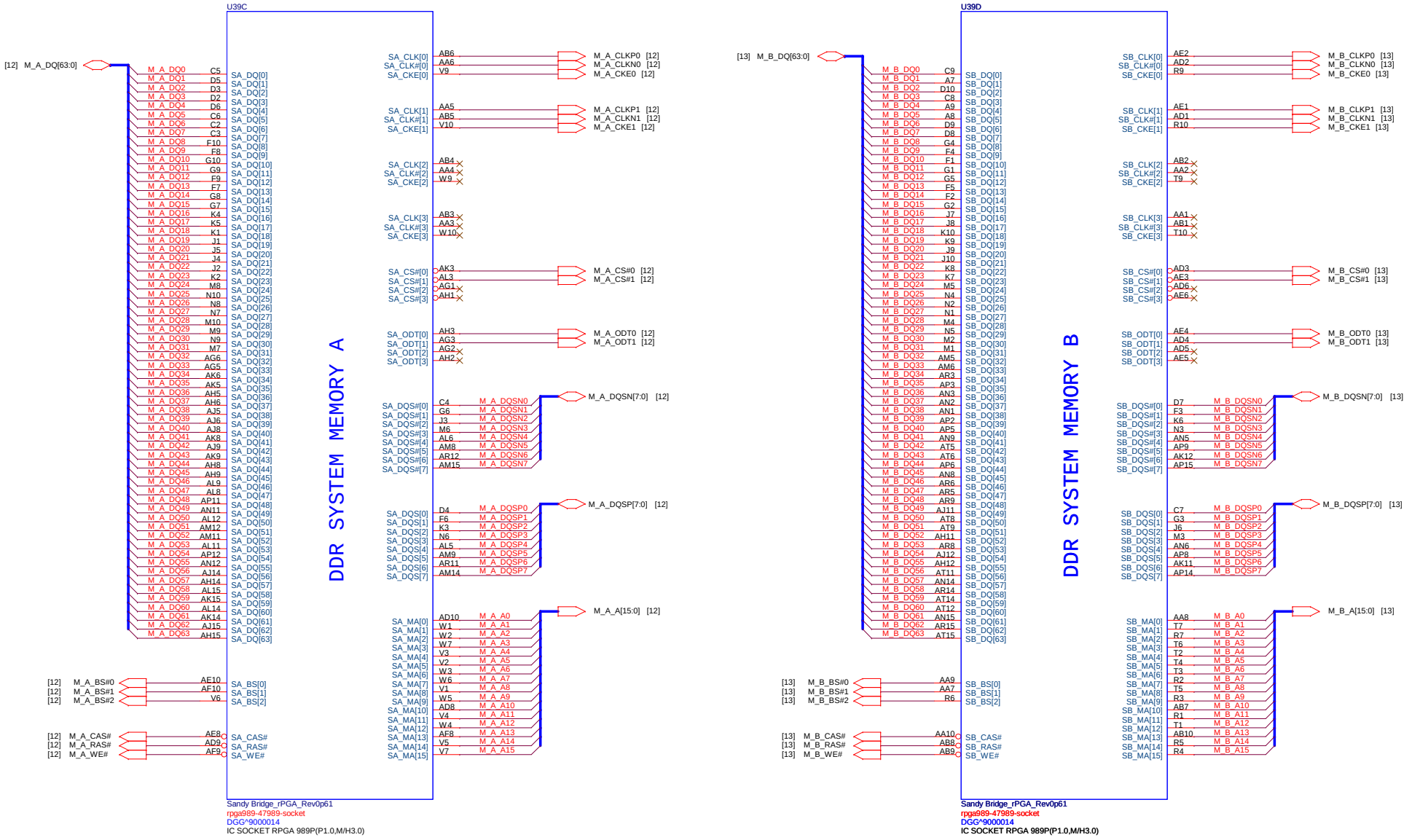
**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 1/4 (PCIE&DMI&FDI) | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 2 of 49 | |

NB5/RD2

# Sandy Bridge Processor (DDR3)






**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 2/4 (DDR3 I/F) | 1A |

N85/RD2

Date: Tuesday, August 10, 2010 | Sheet 3 of 49

# Sandy Bridge Processor (POWER)

# Sandy Bridge Processor (GRAPHIC POWER)

04

U39F

SNB: 55A

+VCC_CORE

C685 22U/6.3VS_8 C701 22U/6.3VS_8 C691 22U/6.3VS_8
C754 22U/6.3VS_8 C747 22U/6.3VS_8 C722 22U/6.3VS_8
C697 22U/6.3VS_8 C692 22U/6.3VS_8 C159 22U/6.3VS_8
C184 22U/6.3VS_8 C117 22U/6.3VS_8 C676 22U/6.3VS_8
C79 22U/6.3VS_8 C709 22U/6.3VS_8 C96 22U/6.3VS_8
C715 *22U/6.3VS_8 C138 *22U/6.3VS_8 C174 *22U/6.3VS_8
C147 22U/6.3VS_8 C22 22U/6.3VS_8 C694 22U/6.3VS_8
C729 22U/6.3VS_8 C767 22U/6.3VS_8 C33 22U/6.3VS_8
C28 *22U/6.3VS_8 C27 22U/6.3VS_8 C24 22U/6.3VS_8
C772 *22U/6.3VS_8 C693 *22U/6.3VS_8 C742 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C23 22U/6.3VS_8 C21 22U/6.3VS_8 C652 22U/6.3VS_8
C157 22U/6.3VS_8 C93 22U/6.3VS_8 C182 22U/6.3VS_8
C26 22U/6.3VS_8 C133 22U/6.3VS_8 C684 *22U/6.3VS_8
C696 *22U/6.3VS_8 C110 *22U/6.3VS_8 C29 *22U/6.3VS_8
C663 *22U/6.3VS_8 C34 *22U/6.3VS_8 C172 *22U/6.3VS_8
C70 *22U/6.3VS_8 C668 *22U/6.3VS_8 C145 *22U/6.3VS_8
C675 *22U/6.3VS_8 C666 *22U/6.3VS_8 C61 *22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT_40 R67 *0_4/S

+1.05V_VTT

VIDALERT# VIDSCLK VIDSOUT

AJ29 H_CPU_SVIDALRT#
AJ30 VR_SVID_CLK
AJ28 VR_SVID_DATA

3/26 DB Modify.

VCC_SENSE VSS_SENSE

AJ35 AJ34

R118 100_4 +VCC_CORE
VCC_SENSE [47]
VSS_SENSE [47]
R117 100_4

VCCIO_SENSE VSSIO_SENSE

B10 A10

VCCP_SENSE [41]
VSSP_SENSE
TP46

Trace Route to Power IC area.

+VCC_CORE [47,48]
+VCC_GFX [47,48]
+VCCSA [40]
+1.05V_VTT [2,10,36,41,47]
+1.5V_CPU [2,37,45]
+1.5V_CPU [2,37,45]
+1.5VSUS [2,10,12,13,40,44]

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

U39G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX

SNB: 21.5A

C140 22U/6.3V_8 C158 22U/6.3V_8
C176 22U/6.3V_8 C185 22U/6.3V_8
C173 22U/6.3V_8 C137 22U/6.3V_8
C183 22U/6.3V_8 C146 22U/6.3V_8
C148 22U/6.3V_8 C303 22U/6.3V_8
C160 22U/6.3V_8 C116 22U/6.3V_8

Ra R584 *0_4

| | DIS | SG/UMA |
|---|---|---|
| Ra | Stuff | NC |

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

+1.8V

SNB: 1.5A

C606 10U/6.3V_8 C612 1U/6.3V_4 C613 1U/6.3V_4 + C608 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge. 6/7 stuff

3/26 DB change 10U FP to 0805.

VCCPLL1 VCCPLL2 VCCPLL3

B6 A6 A2

1.8V RAIL

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SENSE LINES

VAXG_SENSE VSSAXG_SENSE

AK35 AK34

3/26 DB Modify.

R171 100_4 +VCC_GFX
VCC_AXG_SENSE [47]
VSS_AXG_SENSE [47]
R176 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R586 *0_8 DDR_VTTREF [12,13,44]
R585 100K_4
Q43 2N7002
MAIND MAIND [45]

DDR3 -1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15

AE7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

SNB: 5A +1.5V_CPU

C99 10U/6.3V_8 C141 10U/6.3V_8 C179 10U/6.3V_8 C170 10U/6.3V_8
C169 10U/6.3V_8 C168 10U/6.3V_8 C95 330U/2V_7343 5/9 stuff

330uF x1, 10uF_8 x6 Socket BOT edge.
3/26 DB change 10U FP to 0805.

SA RAIL

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8

M27 M26 L26 J26 J25 J24 H26 H25

SNB: 6A +VCCSA

C76 10U/6.3V_8 C611 10U/6.3V_8 C77 10U/6.3V_8 C610 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.
3/26 DB change 10U FP to 0805.

MISC

VCCSA_SENSE H23

R506 0_4 VCCUSA_SENSE [40]

H_FC_C22 R505 10K_4

FC_C22 C22
VCCSA_VID1 C24

VCCSA_SEL [40]

R499 10K_4

5/11 add 10K by power

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

R150 *54.9/F_4 +1.05V_VTT

VR_SVID_CLK VR_SVID_CLK [47]

3/26 DB Modify.

SVID DATA

6/7 no stuff

+1.05V_VTT +1.05V_VTT

Place PU resistor close to CPU

R147 130/F_4

R141 *130/F_4

Place PU resistor close to VR

VR_SVID_DATA VR_SVID_DATA [47]

3/26 DB Modify.

SVID ALERT

Place PU resistor close to CPU

+1.05V_VTT R157 75_4

H_CPU_SVIDALRT# R164 43_4 VR_SVID_ALERT# [47]

3/26 DB Modify.

+1.5VSUS

JP1 *SOLDERJUMPER-2

+1.5V_CPU

Q3 AON7410

R137 220_8

MAIND

C161 *470P/50V_4

Q5 2N7002

MAIN_ONG [2,45]

SNB: 5A +1.5VSUS

C102 0.1U/10V_4
C113 0.1U/10V_4
C122 0.1U/10V_4
C131 0.1U/10V_4

3/26 DB add for Intel. Placement close to CPU.

CPU VDDQ

PROJECT : SP9 (Huron River)

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 3/4 (POWER) | 1A |

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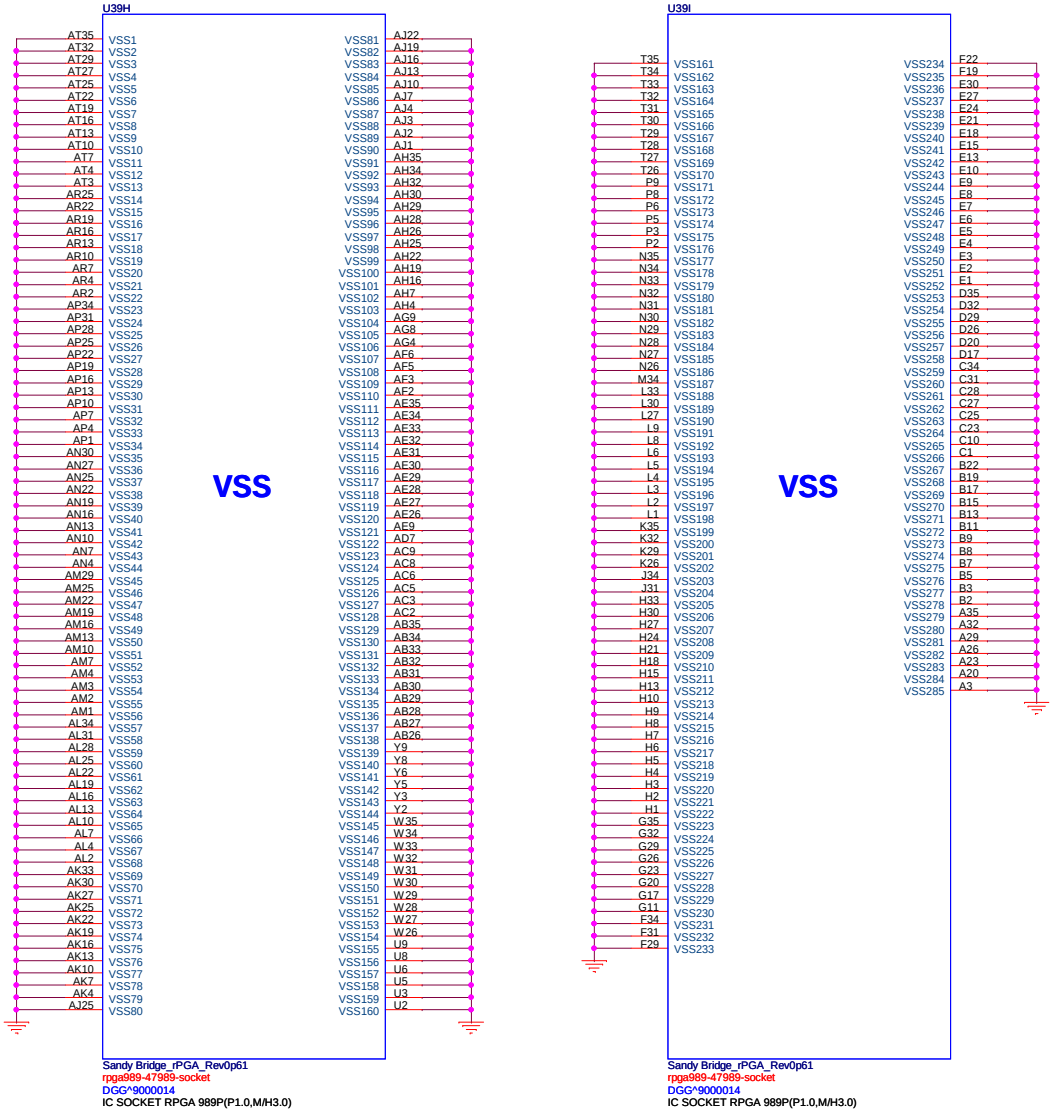
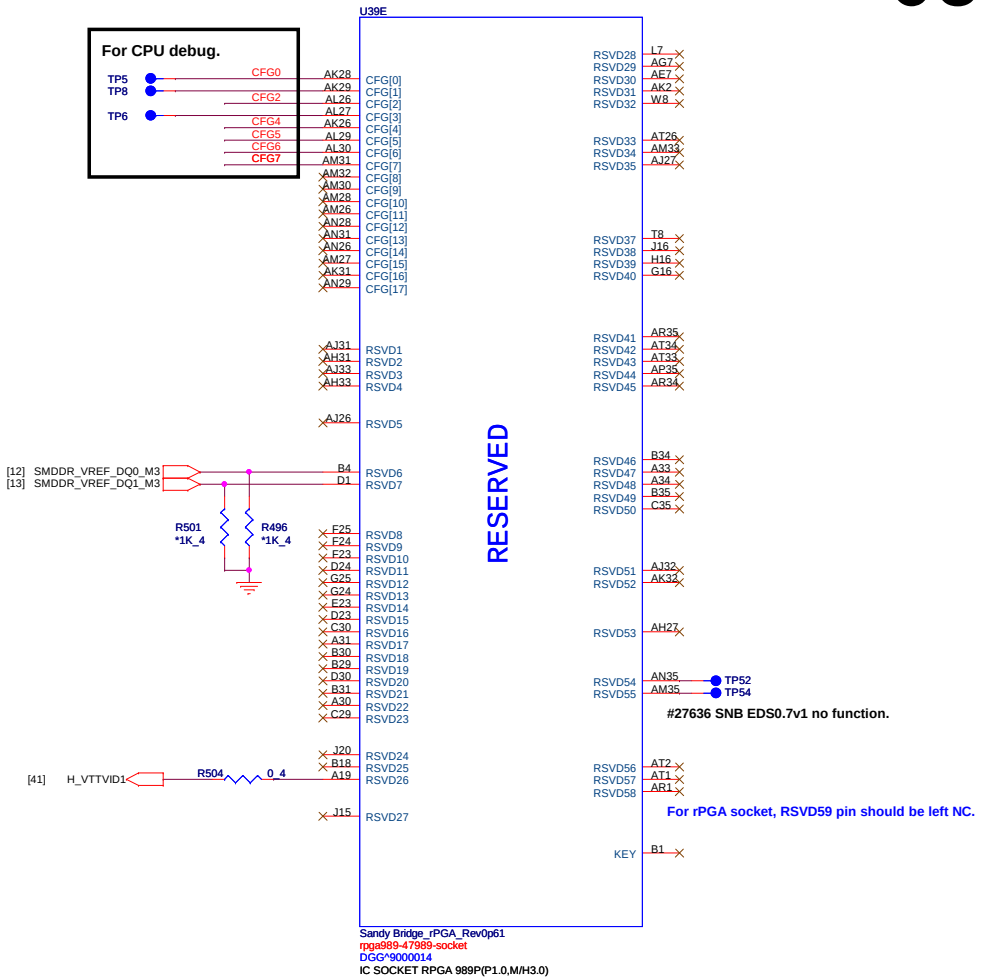
N85/RD2

# Sandy Bridge Processor (GND)




# Sandy Bridge Processor (RESERVED, CFG)

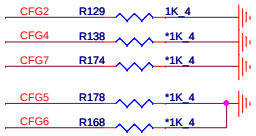
05




## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |




**CFG[6:5] (PCIE Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 4/4 (GND) | 1A |

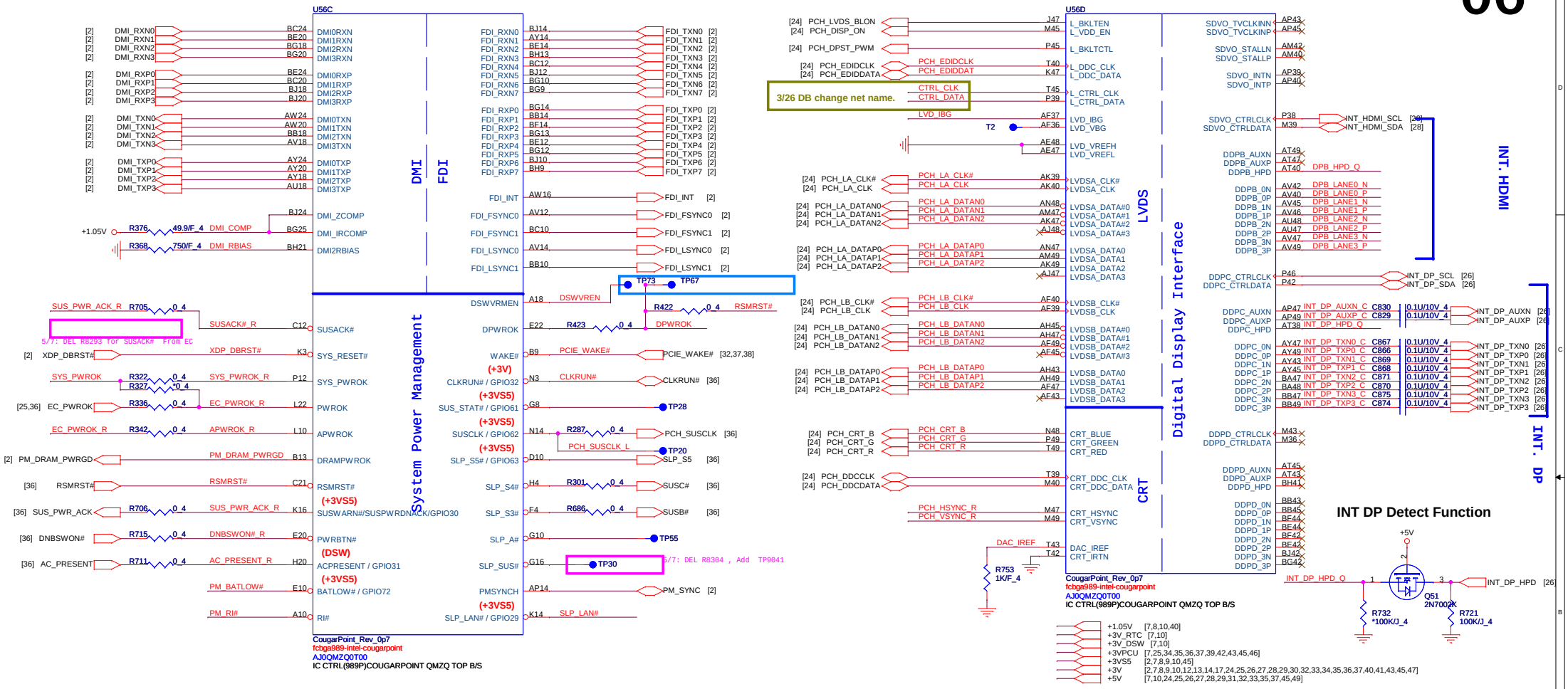
N85/RD2

Date: Tuesday, August 10, 2010 Sheet 5 of 49

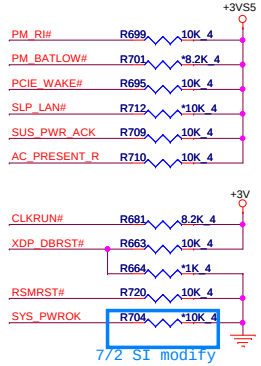
# Cougar Point (DMI,FDI,PM)

# Cougar Point (LVDS,DDI)

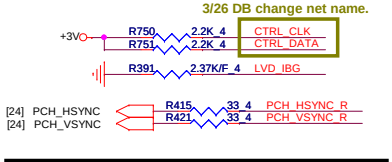
06




## PCH Pull-high/low(CLG)

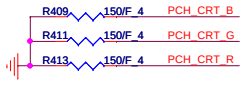



## INT LVDS & CRT disable (DIS only remove)

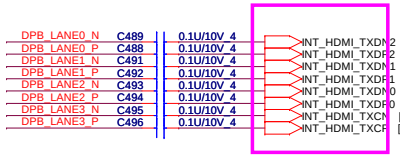



**PD Res place close to PCH**

**PCH to Res routeing 37.5ohm Impedance.**
**Res to connector filter routeing 50ohm Impedance.**

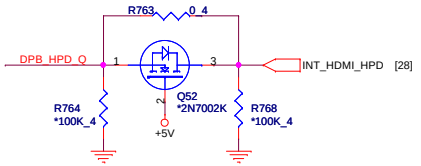



## INT HDMI disable (DIS only remove)

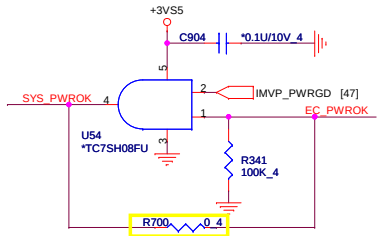


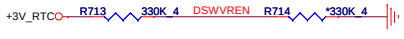

### INT HDMI Detect Function

5/11: swap 0 and 2



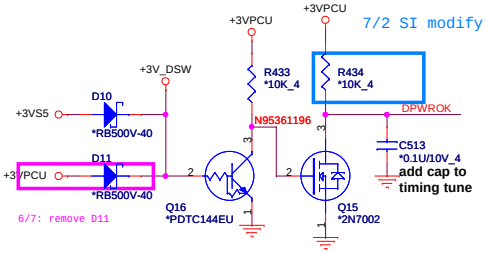

## System PWR_OK(CLG)




| On Die DSW VR Enable |
|---|
| High = Enable (Default)<br>Low = Disable |

## DPWROK FOR DSW





PROJECT : SP9 (Huron River)
Quanta Computer Inc.
N85/RD2
Size Custom
Document Number PCH 1/6 (DMI/FDI/VIDEO)
Rev 1A
Date: Tuesday, August 10, 2010
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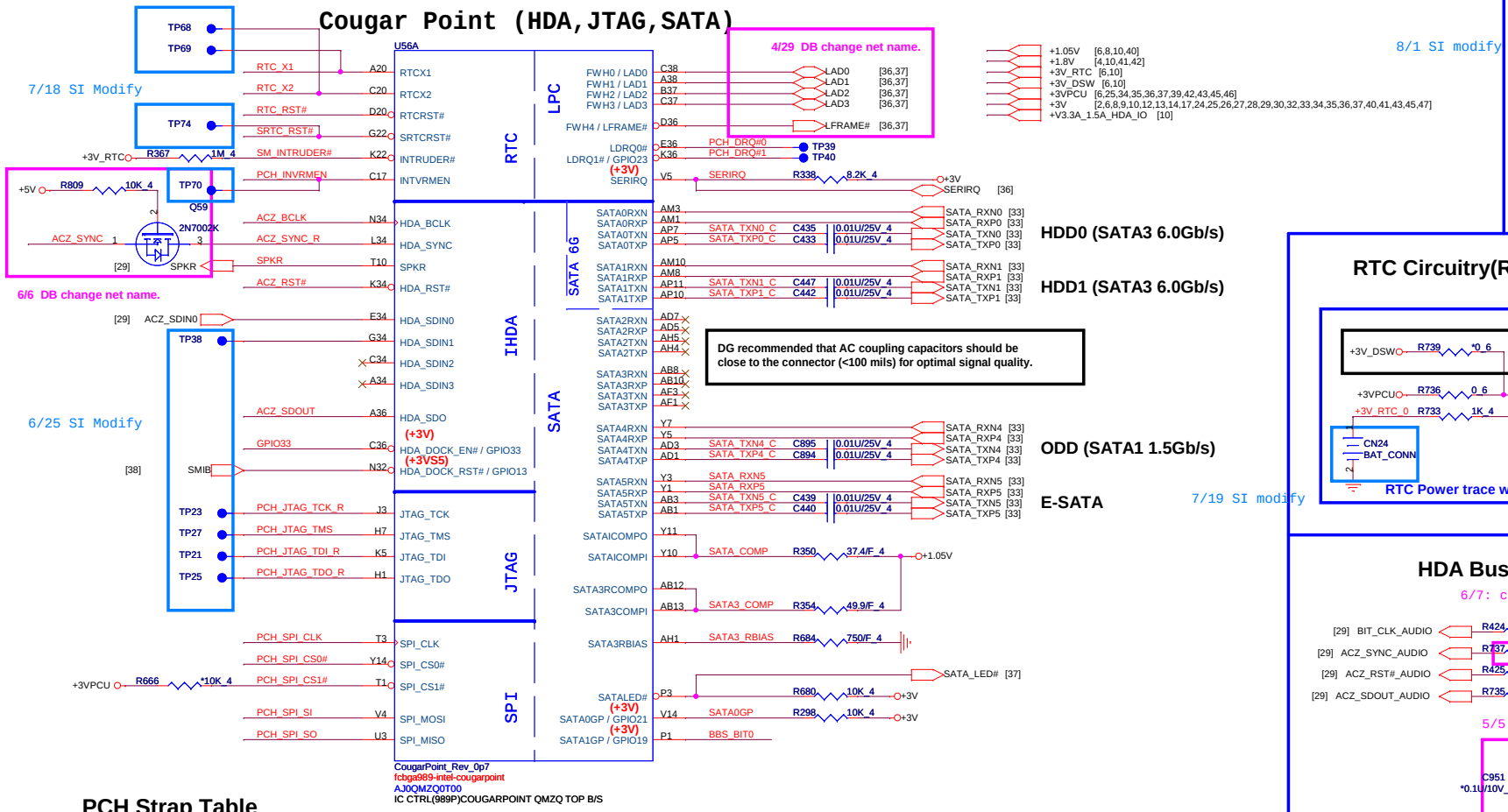
# Cougar Point (HDA,JTAG,SATA)






4/29 DB change net name.

+1.05V [6,8,10,40]
+1.8V [4,10,41,42]
+3V_RTC [6,10]
+3V_DSW [6,10]
+3VPCU [6,25,34,35,36,37,39,42,43,45,46]
+3V [2,6,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+V3.3A_1.5A_HDA_IO [10]

8/1 SI modify

7/18 SI Modify

6/6 DB change net name.

6/25 SI Modify

HDD0 (SATA3 6.0Gb/s)

HDD1 (SATA3 6.0Gb/s)

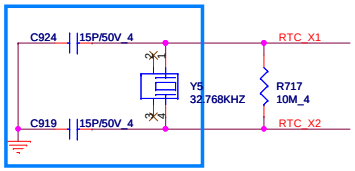
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

ODD (SATA1 1.5Gb/s)

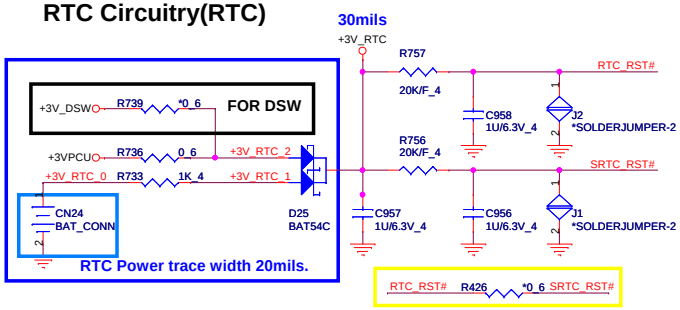
E-SATA

7/19 SI modify

## RTC Clock 32.768KHz




## RTC Circuitry(RTC)

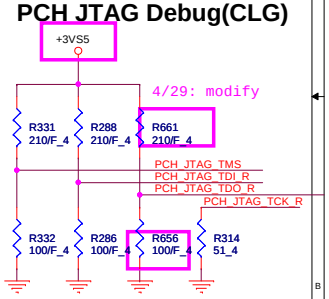



## HDA Bus(CLG)

6/7: change back to 33

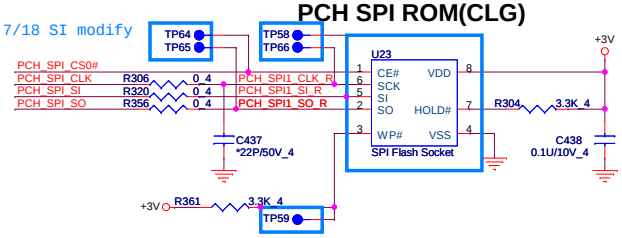



## PCH JTAG Debug(CLG)




## PCH SPI ROM(CLG)

7/18 SI modify




| Vender | Size | P/N |
|---|---|---|
| EON | 4MB | AKE39FN0Q00 (EN25F32-100HIP) |
| Winbond | 4MB | AKE391P0N00 (W25Q32BVSSIG) |
| Socket | | DG008000031 |

## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | Circuit |
|---|---|---|---|---|
| SPKR (Different from Calpella) | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | SPKR R660 *1K_4 +3V |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R749 *1K_4, R746 10K_4, +3V, PCI_GNT3# [8]<br>Bios request, for can't boot Capella 4/23. |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | PCH_INVRMEN R716 330K_4 +3V_RTC |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | GPIO33 R727 1K_4 GPIO33_E [36] |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# 1, GNT0# 1 → SPI<br>GNT1# 0, GNT0# 0 → LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1# |
| GPIO19 (Different from Calpella) | Boot BIOS Selection 0 [bit-0] | PWROK | | R667 *1K_4, R752 *1K_4, BBS_BIT0, BBS_BIT1 [8] |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | +1.8V R691 *1K_4 NV_ALE [8] |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 20kohm<br>4/30 reserve. | +1.8V R678 2.2K_4, R694 4.7K_4, NV_CLE [8], H_SNB_IVB# [2]<br>N.A at CPT EDS 0.7 |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V | +3VS5 R734 1K_4 ACZ_SYNC_R<br>5/4 add |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | ACZ_SDOUT R738 *1K_4 +V3.3A_1.5A_HDA_IO |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down (weak pull-up 20K) | R703 *1K_4 ICC_EN# [9]<br>4/29 reserve. |
| GPIO28 (Different from Calpella) | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | R693 *1K_4 PLL_ODVR_EN [9] |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | PCH_SPI_SI R308 1K_4 +3V |

N85/RD2

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 2/6 (SATA/HDA/SPI) | 1A |

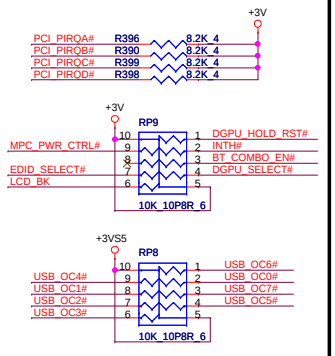
Date: Tuesday, August 10, 2010 Sheet 7 of 49

# Cougar Point-M (PCI,USB,NVRAM)

# Cougar Point-M (PCI-E,SMBUS,CLK)

08

## PCI/USBOC# Pull-up(CLG)




| MPC Switch Control | |
|---|---|
| MPC_PWR_CTRL# | Low = MPC ON<br>High = MPC OFF (Default) |

MPC_PWR_CTRL# R769 *1K_4

## U56E

BG26 BJ26 BH25 BJ16 BG16 AH38 AH37 AK43 AK45 C18 N30 H3 AH12 AM4 AM5 Y13 K24 L24 AB46 AB45 — TP1–TP20

B21 M20 AY16 BG46 — TP21–TP24

BE28 BC30 BE32 BJ32 BC28 BE30 BE32 BG32 AV26 BB26 AU28 AY30 AU26 AY26 AV28 AW30 — TP25–TP40

### RSVD

### NVRAM

NV_CE#0 AY7
NV_CE#1 AV7
NV_CE#2 AU3
NV_CE#3 BG4
NV_DQS0 AT10
NV_DQS1 BC8
NV_DQ0 / NV_IO0 AU2
NV_DQ1 / NV_IO1 AT4
NV_DQ2 / NV_IO2 AT3
NV_DQ3 / NV_IO3 AT1
NV_DQ4 / NV_IO4 AY3
NV_DQ5 / NV_IO5 AT5
NV_DQ6 / NV_IO6 AV3
NV_DQ7 / NV_IO7 AV1
NV_DQ8 / NV_IO8 BB1
NV_DQ9 / NV_IO9 BA3
NV_DQ10 / NV_IO10 BB5
NV_DQ11 / NV_IO11 BB3
NV_DQ12 / NV_IO12 BB7
NV_DQ13 / NV_IO13 BE8
NV_DQ14 / NV_IO14 BD4
NV_DQ15 / NV_IO15 BF6
NV_ALE AV5 — NV_ALE
NV_CLE AY1 — NV_CLE
NV_RCOMP AV10
NV_RB# AT8
NV_RE#_WRB0 AY5
NV_RE#_WRB1 BA2
NV_WE#_CK0 AT12
NV_WE#_CK1 BF3

### PCI

PIRQA# K40
PIRQB# K38
PIRQC# H38
PIRQD# G38
REQ1# / GPIO50 C46 (+3V)
REQ2# / GPIO52 C44 (+3V)
REQ3# / GPIO54 E40 (+3V)
GNT1# / GPIO51 D47 (+3V)
GNT2# / GPIO53 E42 (+3V)
GNT3# / GPIO55 F46 (+3V)
PIRQE# / GPIO2 G42 (+3V)
PIRQF# / GPIO3 G40 (+3V)
PIRQG# / GPIO4 C42 (+3V)
PIRQH# / GPIO5 D44 (+3V)
PME# K10
PLTRST# C6

### USB

USBP0N C24
USBP0P A24
USBP1N C25
USBP1P B25
USBP2N C26
USBP2P A26
USBP3N K28
USBP3P H28
USBP4N E28
USBP4P D28
USBP5N C28
USBP5P A28
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
USBP8N L30
USBP8P K30
USBP9N G30
USBP9P E30
USBP10N C30
USBP10P A30
USBP11N L32
USBP11P K32
USBP12N G32
USBP12P E32
USBP12N C32
USBP12P A32
USBP13N A32
USBP13P
USBRBIAS# C33 — USB_BIAS — R718 22.6/F_4
USBRBIAS B33

USBP0- [33] — USBP0+ [33] — [E-SATA]
TP34 — TP35 — [Fingerprint]
USBP4- [34] — USBP4+ [34] — [Webcam]
USBP5- [38] — USBP5+ [38] — [USB 3.0 Co-layout]
USBP8- [34] — USBP8+ [34] — [Right USB #1]
USBP9- [34] — USBP9+ [34] — [Right USB #2]
USBP10- [37] — USBP10+ [37] — [WLAN]
TP37 — TP36 — [Card Reaer]
USBP12- [34] — USBP12+ [34] — [Blue Tooth LCD]
USBP13- [34] — USBP13+ [34]

### USB 3.0

(+3VS5) OC0# / GPIO59 A14 — USB_OC0# — USB_OC0# [38]
(+3VS5) OC1# / GPIO40 K20 — USB_OC1#
(+3VS5) OC2# / GPIO41 B17 — USB_OC2#
(+3VS5) OC3# / GPIO42 C16 — USB_OC3#
(+3VS5) OC4# / GPIO43 L16 — USB_OC4#
(+3VS5) OC5# / GPIO9 A16 — USB_OC5#
(+3VS5) OC6# / GPIO10 D14 — USB_OC6#
(+3VS5) OC7# / GPIO14 C14 — USB_OC7#

[38] CLK_USB3.0_GEN2# — RP4 0_4P2R_4 — CLK_USB3.0_GEN2N# AB42
[38] CLK_USB3.0_GEN2 — CLK_USB3.0_GEN2P AB40
[38] PCIE_CLK_REQB# — R305 0_4 — CLK_PEGB_REQ# E6

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

## WLAN / LAN / [USB3.0]

[37] PCIE_RXN1 — C477 0.1U/10V_4 — PCIE_TXN1_C — C481 0.1U/10V_4 — PCIE_TXP1_C
[37] PCIE_RXP1
[37] PCIE_TXN1
[37] PCIE_TXP1

[32] PCIE_RXN2_LAN — C485 0.1U/10V_4 — PCIE_TXN2_LAN_C — C486 0.1U/10V_4 — PCIE_TXP2_LAN_C
[32] PCIE_RXP2_LAN
[32] PCIE_TXN2_LAN
[32] PCIE_TXP2_LAN

[38] PCIE_RXN1_USB3.0
[38] PCIE_RXP1_USB3.0
[38] PCIE_TXN1_USB3.0
[38] PCIE_TXP1_USB3.0
C484 .1U/10V_4 — PCIE_TXN3_C
C487 .1U/10V_4 — PCIE_TXP3_C

## SMB_PCH_DAT / SMB_PCH_CLK

+3V — C974 *0.1U/10V_4 — Q54 *2N7002E — Q56 *2N7002E — AMP_SDA [30]
+3V — C965 *0.1U/10V_4
+3V — C973 *0.1U/10V_4 — Q53 *2N7002E — Q57 *2N7002E — AMP_SCL [30]

SMB_RUN_DAT — R431 0_4 — AMP_SDA
SMB_RUN_CLK — R432 0_4 — AMP_SCL

Reserve for Amp I2C 5/4.
6/7 modified

## U56B

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

### PCI-E*

### SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 — SMBALERT#
SMBCLK H14 — SMB_PCH_CLK
SMBDATA C9 — SMB_PCH_DAT
(+3VS5) SMLOALERT# / GPIO60 A12 — DRAMRST_CNTRL_PCH — DRAMRST_CNTRL_PCH [2]
SMLOCLK C8 — SMB_ME0_CLK
SMLODATA G12 — SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 — SML1ALERT#_R — TP33
(+3VS5) SML1CLK / GPIO58 E14 — SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 — SMB_ME1_DAT

### Controller Link

CL_CLK1 M7 — CL_CLK_R — TP22
CL_DATA1 T11 — CL_DAT_R — TP24
CL_RST1# P10 — CL_RST#_R — TP26

### CLOCKS

(+3VS5) PEG_A_CLKRQ# / GPIO47 M10 — CLK_PEGA_REQ#
CLKOUT_PEG_A_N AB37 — CLK_PCH_PEGAN
CLKOUT_PEG_A_P AB38 — CLK_PCH_PEGAP
CLKOUT_DMI_N AV22 — CLK_CPU_BCLKN [2]
CLKOUT_DMI_P AU22 — CLK_CPU_BCLKP [2]
CLKOUT_DP_N AM12 — CLK_DPLL_SSCLKN [2]
CLKOUT_DP_P AM13 — CLK_DPLL_SSCLKP [2]
CLKIN_DMI_N BF18 — CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P BE18 — CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N BJ30 — CLK_BUF_BCLK_N
CLKIN_GND1_P BG30 — CLK_BUF_BCLK_P
CLKOUT_DOT_96N G24 — CLK_BUF_DREFCLK#
CLKOUT_DOT_96P E24 — CLK_BUF_DREFCLK
CLKIN_SATA_N AK7 — CLK_BUF_DREFSSCLK#
CLKIN_SATA_P AK5 — CLK_BUF_DREFSSCLK
REFCLK14IN K45 — CLK_PCH_14M
CLKIN_PCILOOPBACK H45 — CLK_PCI_FB

CLKOUT_PCIE0N Y40
CLKOUT_PCIE0P Y39
PCIECLKRQ0# / GPIO73
CLK_PCIE_REQ0# J2
CLKOUT_PCIE1N AB49
CLKOUT_PCIE1P AB47
PCIECLKRQ1# / GPIO18
CLK_PCIE_REQ1# M1
CLKOUT_PCIE2N AA48
CLKOUT_PCIE2P AA47
PCIECLKRQ2# / GPIO20
CLK_PCIE_REQ2# V10
CLKOUT_PCIE3N Y37
CLKOUT_PCIE3P Y36
PCIECLKRQ3# / GPIO25
CLK_PCIE_REQ3# A8
CLKOUT_PCIE4N Y43
CLKOUT_PCIE4P Y45
PCIECLKRQ4# / GPIO26
CLK_PCIE_REQ4# L12
CLKOUT_PCIE5N V45
CLKOUT_PCIE5P V46
PCIECLKRQ5# / GPIO44
CLKOUT_PEG_B_N AB42
CLKOUT_PEG_B_P AB40
PEG_B_CLKRQ# / GPIO56
CLKOUT_PCIE6N V40
CLKOUT_PCIE6P V42
PCIECLKRQ6# / GPIO45
CLKOUT_PCIE7N V38
CLKOUT_PCIE7P V37
PCIECLKRQ7# / GPIO46
CLKOUT_ITPXDP_N AK14
CLKOUT_ITPXDP_P AK13
CLK_PCH_ITPN
CLK_PCH_ITPP

### FLEX CLOCKS

(+3V) CLKOUTFLEX0 / GPIO64 L43 — CLK_FLEX0 — TP42
(+3V) CLKOUTFLEX1 / GPIO65 L47 — CLK_FLEX1 — R412 22_4 — CLK_48M_CR [38]
(+3V) CLKOUTFLEX2 / GPIO66 L47 — CLK_FLEX2 — TP57
(+3V) CLKOUTFLEX3 / GPIO67 L49 — CLK_FLEX3 — R416 *22_4 — PCH_CLK27M_1

Remove Ra, Rb for UMA & SG.
27MHz support DIS only.

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

## +3V / DGPU_PWROK

C502 1U/10V_4 — DGPU_PWROK [9,36,42,43,44]
U27 — 7/18 : Modify PN
PCH_CLK_27M — PCH_CLK_27M [17] — *74LVC1G126
R808 *0_4

Bios swap GPIO 4/28. — TP29
Bios swap GPIO 4/23. — [9] BOARD_ID0 — RP4 0_4P2R_4
[9] BOARD_ID1
[9] BOARD_ID2

## 3/26 DB del external clock generator.

4/19 change FB to small size

TP71 — C953 27P/50V_4 — Y6 25MHZ — C952 27P/50V_4 — TP72
R744 1M_4
XTAL25_IN V47 — XTAL25_OUT V49
XCLK_RCOMP Y47 — R741 90.9/F_4 — +1.05V

5/13: modify CLK_48M to CLK_FLEX1

## PLTRST#(CLG)

+3VS5 — C431 *0.1U/10V_4 — U22 *TC7SH08FU — R283 100K_4 — R292 0_4
PCI_PLTRST# — PLTRST# — 4/29 modify — PLTRST# [2,32,35,36,37,38]

## PEG Clock detect (SG only)

DGPU_PWROK [9,36,42,43,44]
Q14 *2N7002 — CLK_PEGA_REQ# — 5/7: modify

## SMBus/Pull-up(CLG)

4/20 modify

[13,26,30,36] MBCLK2 — Q49 2N7002K — SMB_ME1_CLK — R702 2.2K_4 — R708 2.2K_4 — +3VS5
[13,26,30,36] MBDATA2 — Q50 2N7002K — SMB_ME1_DAT

SMB_PCH_DAT — Q13 2N7002K — R290 4.7K_4 — SMB_RUN_DAT [12,13]
SMB_PCH_CLK — Q12 2N7002K — R289 4.7K_4 — SMB_RUN_CLK [12,13]

## CLK_REQ/Strap Pin(CLG)

CLK_PCIE_REQ1# R329 10K_4
CLK_PCIE_REQ2# R315 10K_4
CLK_PCIE_REQ0# R689 10K_4
CLK_PCIE_REQ3# R692 10K_4
CLK_PCIE_REQ4# R323 10K_4
CLK_PEGB_REQ# R310 10K_4
CLK_PEGA_REQ# Ra R325 *10K_4
CLK_PEGA_REQ# Rb R311 10K_4
SG : Rb ; UMA : Ra
CLK_BUF_BCLK_N R382 10K_4
CLK_BUF_BCLK_P R381 10K_4
CLK_BUF_PCIE_3GPLL# R362 10K_4
CLK_BUF_PCIE_3GPLL R357 10K_4
CLK_BUF_DREFCLK# R377 10K_4
CLK_BUF_DREFCLK R379 10K_4
CLK_BUF_DREFSSCLK# R334 10K_4
CLK_BUF_DREFSSCLK R335 10K_4
CLK_PCH_14M R407 10K_4
CLOCK TERMINATION for FCIM

## PCIE Clock

3/26 DB change Part reference.

WLAN: [37] CLK_PCIE_WLANN / [37] CLK_PCIE_WLANP — RP1 0_4P2R_4 — CLK_PCH_SRC0N / CLK_PCH_SRC0P
[37] PCIE_CLKREQ_WLAN# — R674 0_4 — CLK_PCIE_REQ0#
LAN: [32] CLK_PCIE_LANN / [32] CLK_PCIE_LANP — RP3 0_4P2R_4 — CLK_PCH_SRC2N / CLK_PCH_SRC2P
[32] PCIE_CLKREQ_LAN# — R679 0_4 — CLK_PCIE_REQ1#
GPU: [14] CLK_PCIE_VGA# / [14] CLK_PCIE_VGA — RP2 0_4P2R_4 — CLK_PCH_PEGAN / CLK_PCH_PEGAP

+3VS5 +3V [2,6,7,9,10,45] [2,6,7,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

## SMBus/Pull-up(CLG)

+3VS5
R330 1K_4 DRAMRST_CNTRL_PCH
R337 10K_4 SMBALERT#
R347 2.2K_4 SMB_PCH_CLK
R343 2.2K_4 SMB_PCH_DAT
R677 2.2K_4 SMB_ME0_CLK
R349 2.2K_4 SMB_ME0_DAT
R364 10K_4 SML1ALERT#_R

NB5/RD2

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 3/6 (PCIE/USB/CLK) | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 8 of 49 | |

# Cougar Point (GPIO,VSS_NCTF,RSVD)



Bios swap GPIO 4/28.

Add R9048 4/28.

Add TP 8204 5/14.

Bios swap GPIO 4/28.

U56F

GPIO

CPU/MISC

NCTF

DG rev0.9 suggest to TS_VSS connect to GND 4/23.

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

+3VS5 [2,6,7,8,10,45]
+3V [2,6,7,8,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

## Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

## MFG-TEST

## SGPIO

Bios swap GPIO 4/28.

## GPIO Pull-up/Pull-down(CLG)

5/4 modify

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY: High = Disable (Default); Low = Enable

SV_SET_UP: High = Strong (Default)

TEST DETECT: Low = Default

DMI TERMINATION VOLTAGE OVERRIDE: Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE: LOW - Tx, Rx terminated to same voltage

| Model | BOARD_ID5 | BOARD_ID4 | BOARD_ID3 | BOARD_ID2 | BOARD_ID1 | BOARD_ID0 |
|---|---|---|---|---|---|---|
| SP9 2D | 0 | 0 | 0 | 0 | 0 | 0 |
| SP9 3D | 0 | 0 | 0 | 0 | 0 | 1 |

8/2 SI Modify

4/29 modify

## GFX Present

| | SG | UMA |
|---|---|---|
| Stuff | Ra | Rb |
| NC | Rb | Ra |

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 4/6 (GPIO/MISC) | 1A |

N85/RD2

Date: Tuesday, August 10, 2010 Sheet 9 of 49

# Cougar Point-M (POWER)

# COUGAR POINT (POWER)

7/29 SI Modify for CRT noise

10

U56J

U56G

8/8 SI Modify

7/18 SI Modify

1.01A (60mils)

1.3 A (60mils)

2.925 A (140mils)

3mA (10mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

1.01A (60mils)

160mA (20mils)

65mA (10mils)

8mA (10mils)

55mA (10mils)

95mA (10mils)

10mA (10mils)

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

160mA (15mils)

(Mobile 1.5V)

65mA (10mils)

8mA (10mils)

20mA (10mils)

20mA (10mils)

20mA (10mils)

1mA (10mils)

1mA (10mils)

60mA (10mils)

SG & UMA : Ra
DIS : Rb

42mA (10mils)

190 mA (15mils)

20mA (10mils)

V5REF= 1mA

VCC5REFSUS=1mA

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMZQ TOP B/S

+1.05V [6,7,8,40]
+1.05V_VTT [2,4,36,41,47]
+1.5VSUS [2,4,12,13,40,44]
+1.8V [4,7,41,42]

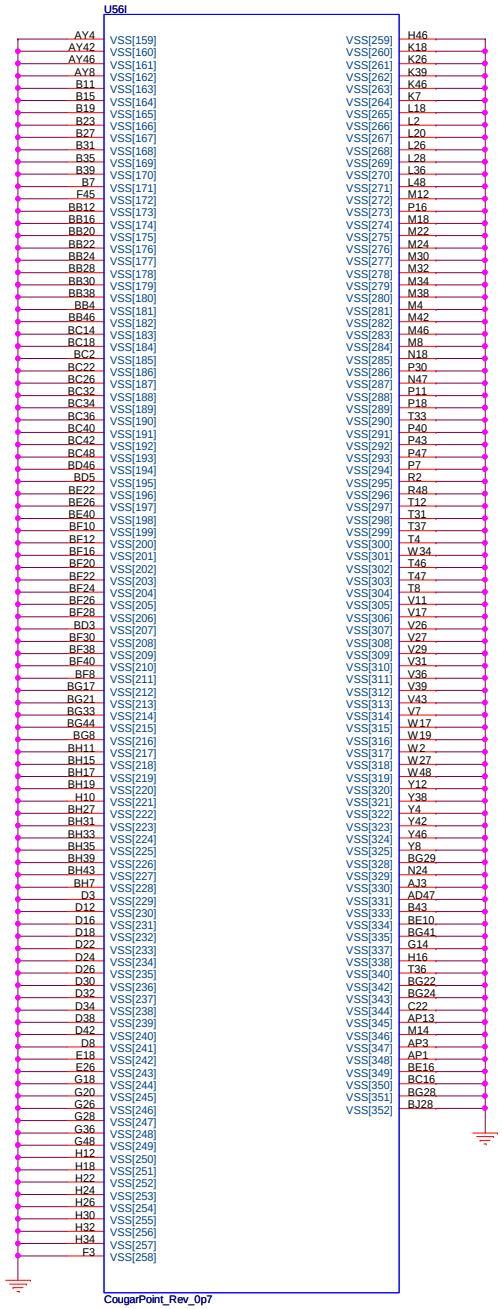
+3V_RTC [6,7]
+3V_DSW [6,7]
+3VS5 [2,6,7,8,9,45]
+3V [2,6,7,8,9,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5VS5 [25,45]
+5V [6,7,24,25,26,27,28,29,31,32,33,35,37,45,49]

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

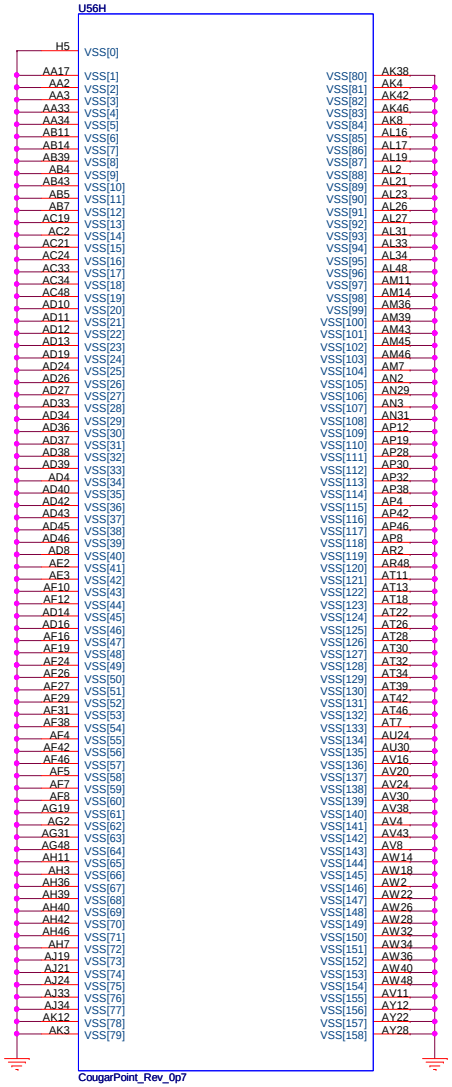
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 5/6 (POWER) | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 10 of 49 | |

N85/RD2

## IBEX PEAK-M (GND)




## IBEX PEAK-M (GND)

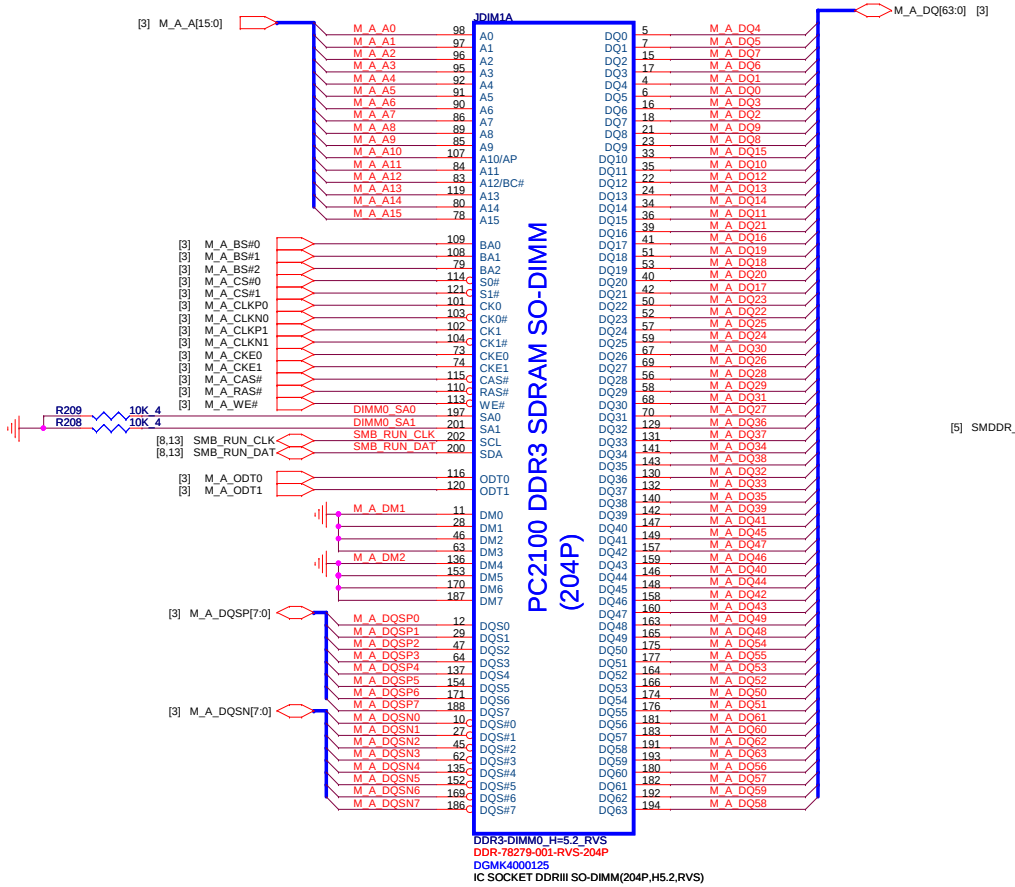


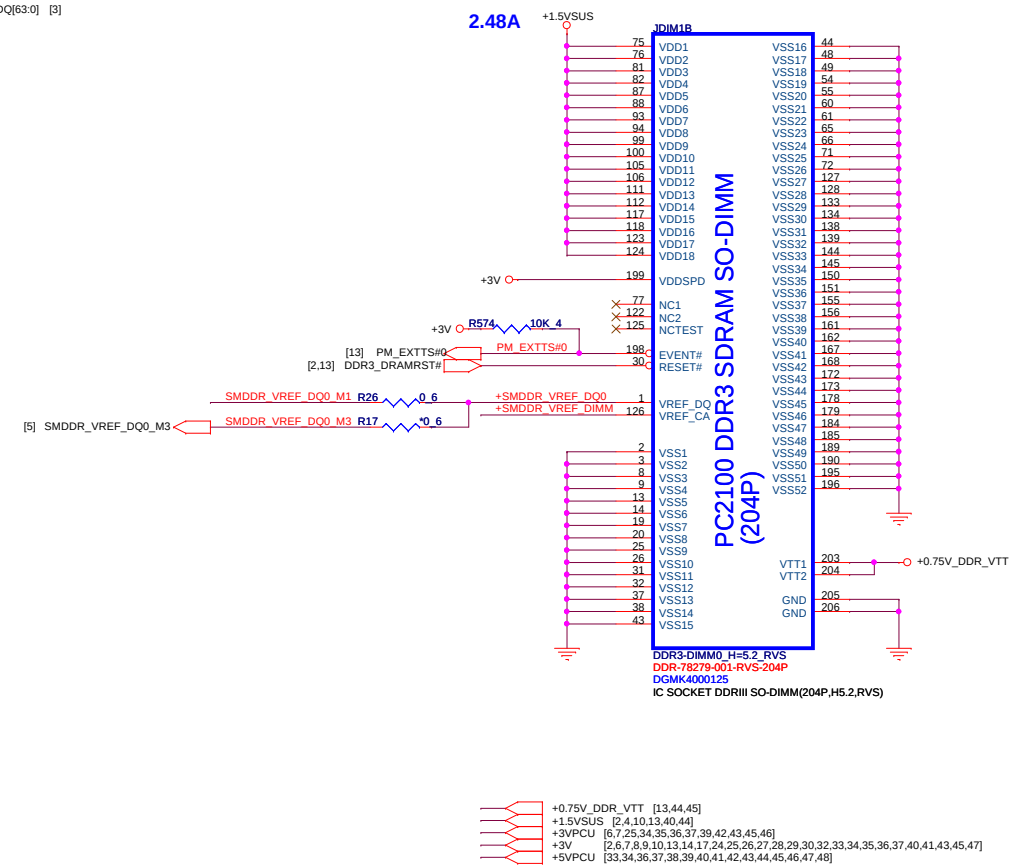

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 6/6 (GND) | 1A |

NB5/RD2

Date: Tuesday, August 10, 2010 Sheet 11 of 49

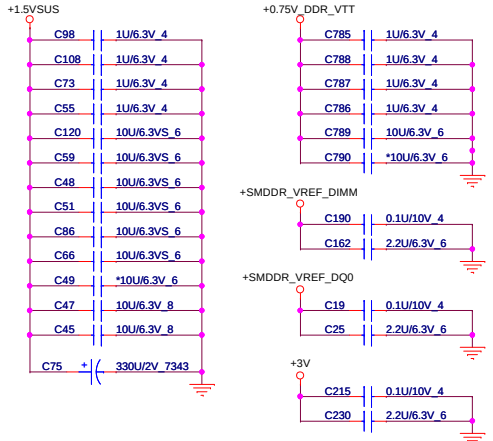


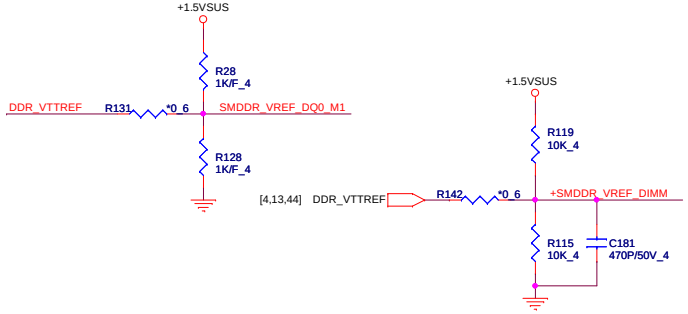

## VREF DQ0 M2 Solution

7/18 : Del M2 solution

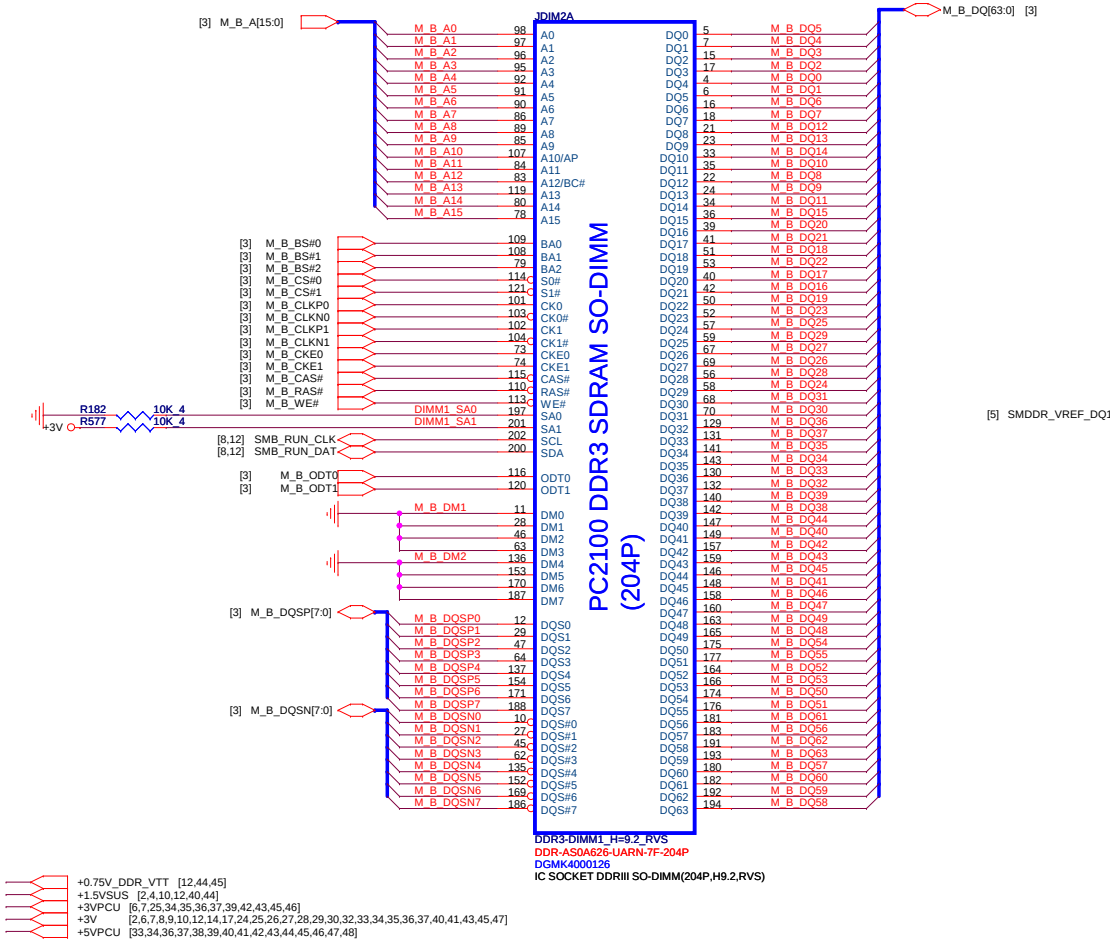
## Place these Caps near So-Dimm0.

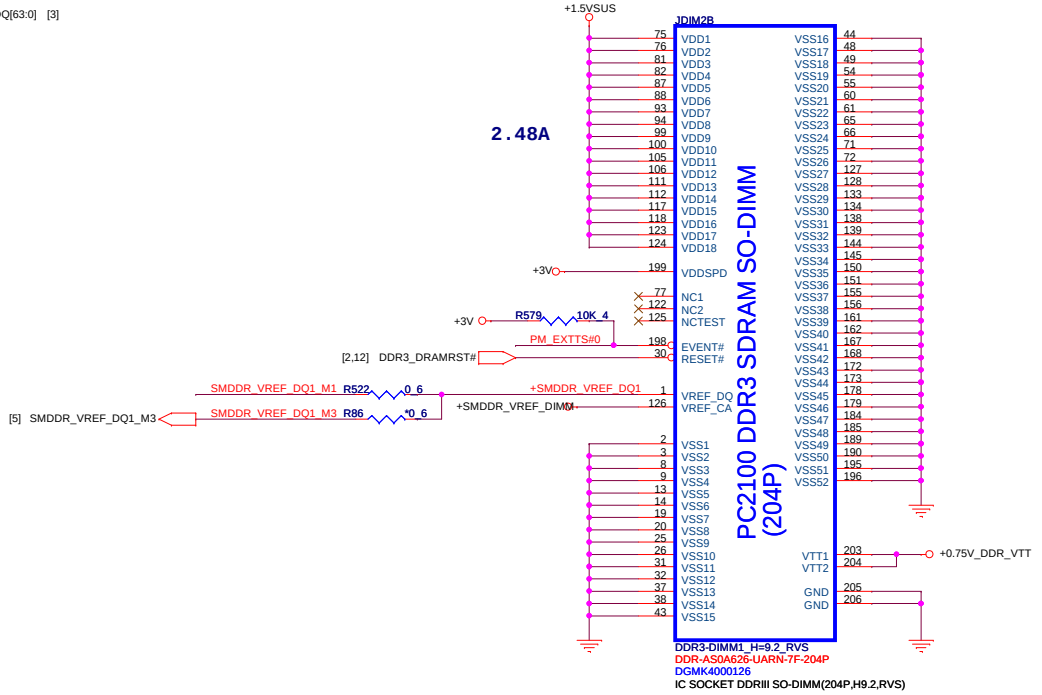



## VREF DQ0 M1 Solution

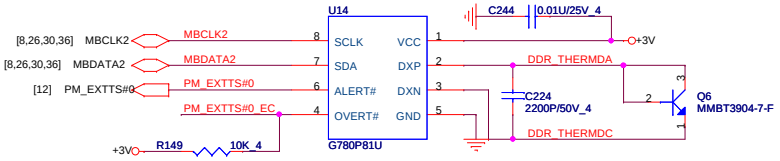



| | | |
|---|---|---|
| N85/RD2 | **PROJECT : SP9 (Huron River)** Quanta Computer Inc. | |
| Size: Custom | Document Number: DDR3 DIMM0-RVS (5.2H) | Rev: 1A |
| Date: Tuesday, August 10, 2010 | Sheet 12 of 49 | |



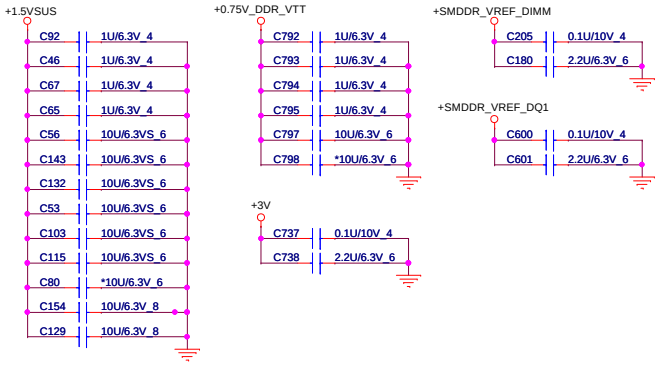

## DDR3 Thermal Sensor



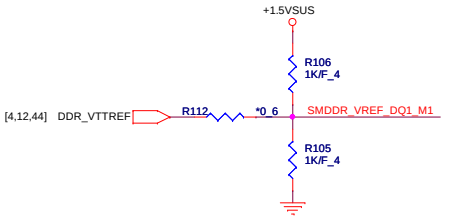

## VREF DQ1 M2 Solution

7/18 : Del M2 solution

## Place these Caps near So-Dimm1.



## VREF DQ1 M1 Solution



| | |
|---|---|
| PROJECT : SP9 (Huron River) | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: DDR3 DIMM1-RVS (9.2H) |
| Rev: 1A | |
| N85/RD2 | Date: Tuesday, August 10, 2010 |
| Sheet 13 of 49 | |

[16,18,44] +1.0V_VGA
[4,7,10,41,42] +1.8V
[2,6,7,8,9,10,12,13,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] +3V

U41A

PCI EXPRESS INTERFACE

| | | | | | | |
|---|---|---|---|---|---|---|
| [2] PEG_TX15 | PEG_TX15 AA38 | PCIE_RX0P | PCIE_TX0P | Y33 | C_PEG_RXP15 C239 .1U/10V_4 | PEG_RX15 [2] |
| [2] PEG_TX#15 | PEG_TX#15 Y37 | PCIE_RX0N | PCIE_TX0N | Y32 | C_PEG_RXN15 C228 .1U/10V_4 | PEG_RX#15 [2] |
| [2] PEG_TX14 | PEG_TX14 Y35 | PCIE_RX1P | PCIE_TX1P | W33 | C_PEG_RXP14 C254 .1U/10V_4 | PEG_RX14 [2] |
| [2] PEG_TX#14 | PEG_TX#14 W36 | PCIE_RX1N | PCIE_TX1N | W32 | C_PEG_RXN14 C257 .1U/10V_4 | PEG_RX#14 [2] |
| [2] PEG_TX13 | PEG_TX13 W38 | PCIE_RX2P | PCIE_TX2P | U33 | C_PEG_RXP13 C259 .1U/10V_4 | PEG_RX13 [2] |
| [2] PEG_TX#13 | PEG_TX#13 V37 | PCIE_RX2N | PCIE_TX2N | U32 | C_PEG_RXN13 C265 .1U/10V_4 | PEG_RX#13 [2] |
| [2] PEG_TX12 | PEG_TX12 V35 | PCIE_RX3P | PCIE_TX3P | U30 | C_PEG_RXP12 C253 .1U/10V_4 | PEG_RX12 [2] |
| [2] PEG_TX#12 | PEG_TX#12 U36 | PCIE_RX3N | PCIE_TX3N | U29 | C_PEG_RXN12 C245 .1U/10V_4 | PEG_RX#12 [2] |
| [2] PEG_TX11 | PEG_TX11 U38 | PCIE_RX4P | PCIE_TX4P | T33 | C_PEG_RXP11 C271 .1U/10V_4 | PEG_RX11 [2] |
| [2] PEG_TX#11 | PEG_TX#11 T37 | PCIE_RX4N | PCIE_TX4N | T32 | C_PEG_RXN11 C281 .1U/10V_4 | PEG_RX#11 [2] |
| [2] PEG_TX10 | PEG_TX10 T35 | PCIE_RX5P | PCIE_TX5P | T30 | C_PEG_RXP10 C266 .1U/10V_4 | PEG_RX10 [2] |
| [2] PEG_TX#10 | PEG_TX#10 R36 | PCIE_RX5N | PCIE_TX5N | T29 | C_PEG_RXN10 C270 .1U/10V_4 | PEG_RX#10 [2] |
| [2] PEG_TX9 | PEG_TX9 R38 | PCIE_RX6P | PCIE_TX6P | P33 | C_PEG_RXP9 C285 .1U/10V_4 | PEG_RX9 [2] |
| [2] PEG_TX#9 | PEG_TX#9 P37 | PCIE_RX6N | PCIE_TX6N | P32 | C_PEG_RXN9 C289 .1U/10V_4 | PEG_RX#9 [2] |
| [2] PEG_TX8 | PEG_TX8 P35 | PCIE_RX7P | PCIE_TX7P | P30 | C_PEG_RXP8 C286 .1U/10V_4 | PEG_RX8 [2] |
| [2] PEG_TX#8 | PEG_TX#8 N36 | PCIE_RX7N | PCIE_TX7N | P29 | C_PEG_RXN8 C298 .1U/10V_4 | PEG_RX#8 [2] |
| [2] PEG_TX7 | PEG_TX7 N38 | PCIE_RX8P | PCIE_TX8P | N33 | C_PEG_RXP7 C308 0.1U/10V_4 | PEG_RX7 [2] |
| [2] PEG_TX#7 | PEG_TX#7 M37 | PCIE_RX8N | PCIE_TX8N | N32 | C_PEG_RXN7 C307 0.1U/10V_4 | PEG_RX#7 [2] |
| [2] PEG_TX6 | PEG_TX6 M35 | PCIE_RX9P | PCIE_TX9P | N30 | C_PEG_RXP6 C300 0.1U/10V_4 | PEG_RX6 [2] |
| [2] PEG_TX#6 | PEG_TX#6 L36 | PCIE_RX9N | PCIE_TX9N | N29 | C_PEG_RXN6 C306 0.1U/10V_4 | PEG_RX#6 [2] |
| [2] PEG_TX5 | PEG_TX5 L38 | PCIE_RX10P | PCIE_TX10P | L33 | C_PEG_RXP5 C309 0.1U/10V_4 | PEG_RX5 [2] |
| [2] PEG_TX#5 | PEG_TX#5 K37 | PCIE_RX10N | PCIE_TX10N | L32 | C_PEG_RXN5 C314 0.1U/10V_4 | PEG_RX#5 [2] |
| [2] PEG_TX4 | PEG_TX4 K35 | PCIE_RX11P | PCIE_TX11P | L30 | C_PEG_RXP4 C312 0.1U/10V_4 | PEG_RX4 [2] |
| [2] PEG_TX#4 | PEG_TX#4 J36 | PCIE_RX11N | PCIE_TX11N | L29 | C_PEG_RXN4 C315 0.1U/10V_4 | PEG_RX#4 [2] |
| [2] PEG_TX3 | PEG_TX3 J38 | PCIE_RX12P | PCIE_TX12P | K33 | C_PEG_RXP3 C320 0.1U/10V_4 | PEG_RX3 [2] |
| [2] PEG_TX#3 | PEG_TX#3 H37 | PCIE_RX12N | PCIE_TX12N | K32 | C_PEG_RXN3 C321 0.1U/10V_4 | PEG_RX#3 [2] |
| [2] PEG_TX2 | PEG_TX2 H35 | PCIE_RX13P | PCIE_TX13P | J33 | C_PEG_RXP2 C322 0.1U/10V_4 | PEG_RX2 [2] |
| [2] PEG_TX#2 | PEG_TX#2 G36 | PCIE_RX13N | PCIE_TX13N | J32 | C_PEG_RXN2 C323 0.1U/10V_4 | PEG_RX#2 [2] |
| [2] PEG_TX1 | PEG_TX1 G38 | PCIE_RX14P | PCIE_TX14P | K30 | C_PEG_RXP1 C325 0.1U/10V_4 | PEG_RX1 [2] |
| [2] PEG_TX#1 | PEG_TX#1 F37 | PCIE_RX14N | PCIE_TX14N | K29 | C_PEG_RXN1 C324 0.1U/10V_4 | PEG_RX#1 [2] |
| [2] PEG_TX0 | PEG_TX0 E35 | PCIE_RX15P | PCIE_TX15P | H33 | C_PEG_RXP0 C318 0.1U/10V_4 | PEG_RX0 [2] |
| [2] PEG_TX#0 | PEG_TX#0 E37 | PCIE_RX15N | PCIE_TX15N | H32 | C_PEG_RXN0 C319 0.1U/10V_4 | PEG_RX#0 [2] |

CLOCK

[8] CLK_PCIE_VGA — CLK_PCIE_VGA AB35 — PCIE_REFCLKP
[8] CLK_PCIE_VGA# — CLK_PCIE_VGA# AA36 — PCIE_REFCLKN

AJ21 NC#1
AK21 NC#2
PWRGOOD_BUF — AH16 PWRGOOD

[35] PEGX_RST# — AA30 PERSTB

CALIBRATION

PCIE_CALRP — Y30 — R173 1.27K/F_4
PCIE_CALRN — Y29 — R172 2K/F_4 — +1.0V_VGA

Broadway

for DB2

U41H

| DP C/D POWER | | DP A/B POWER | |
|---|---|---|---|
| +1.8V_DPC_VDD18 | AP20, AP21 | DPA_VDD18#1, DPA_VDD18#2 | AN24, AP24 — +1.8V_DPA_VDD18 |
| +1.0V_DPC_VDD10 | AP13, AT13 | DPA_VDD10#1, DPA_VDD10#2 | AP31, AP32 — +1.0V_DPA_VDD10 |
| | AN17, AP16, AP17, AW14, AW16 | DPA_VSSR#1–#5 | AN27, AP27, AP28, AW24, AW26 |
| +1.8V_DPC_VDD18 | AP22, AP23 | DPB_VDD18#1, DPB_VDD18#2 | AP25, AP26 — +1.8V_DPA_VDD18 |
| +1.0V_DPC_VDD10 | AP14, AP15 | DPB_VDD10#1, DPB_VDD10#2 | AN33, AP33 |
| | AN19, AP18, AP19, AW20, AW22 | DPD_VSSR#1–#5 | DPB_VSSR#1–#5: AN29, AP29, AP30, AW30, AW32 |
| R45 150/F_4 DPCD_CALR | AW18 DPCD_CALR | | DPAB_CALR AW28 — DPAB_CALR R539 150/F_4 |
| **DP E/F POWER** | | **DP PLL POWER** | |
| +1.8V_DPE_VDD18 | AH34, AJ34 | DPA_PVDD, DPA_PVSS | AU28, AV27 — +1.8V_VGA |
| +1.0V_DPE_VDD10 | AL33, AM33 | DPB_PVDD, DPB_PVSS | AV29, AR28 |
| | AN34, AP39, AR39, AU37 | DPC_PVDD, DPC_PVSS | AU18, AV17 |
| +1.8V_DPE_VDD18 | AF34, AG34 | DPD_PVDD, DPD_PVSS | AV19, AR18 |
| +1.0V_DPE_VDD10 | AK33, AK34 | DPE_PVDD, DPE_PVSS | AM37, AN38 |
| | AF39, AH39, AK39, AL34, AM34 | DPF_PVDD, DPF_PVSS | AL38, AM35 |
| R545 150/F_4 DPEF_CALR | AM39 DPEF_CALR | | |

Broadway

( DPA/B_VDD10 : 1.0V@115mA+115mA) — +1.0V_VGA
HCB1608KF-181T15_6 L13
C119 10U/6.3V_8, C135 1U/6.3V_4, C136 .1U/10V_4

AMD 0821

(DPB_PVDD : 1.8V@20mA) — +1.8V_VGA
+1.8V_DPB_PVDD — HCB1608KF-181T15_6 L50
C653 10U/6.3V_8, C658 1U/6.3V_4, C659 .1U/10V_4

(DPC_PVDD:1.8V@20mA) — +1.8V_VGA
+1.8V_DPC_PVDD — HCB1608KF-181T15_6 L44
C625 10U/6.3V_8, C637 .1U/10V_4, C632 1U/6.3V_4

(DPD_PVDD:1.8V@20mA) — +1.8V_VGA
+1.8V_DPD_PVDD — HCB1608KF-181T15_6 L47
C648 10U/6.3V_8, C660 .1U/10V_4, C655 1U/6.3V_4

(DPE/F_PVDD1.8V@20mA+20mA) — +1.8V_VGA
+1.8V_DPE_PVDD — HCB1608KF-181T15_6 L51
C670 10U/6.3V_8, C671 .1U/10V_4, C672 .1U/10V_4

for AMD comment add for SI

(DPE/F_VDD18 : 1.8V@200mA+200mA) — +1.8V_VGA
+1.8V_DPE_VDD18 — HCB1608KF-181T15_6 L17
C165 10U/6.3V_8, C166 1U/6.3V_4, C167 .1U/10V_4

(DPE/F_VDD10 : 1.0V@115mA+115mA) — +1.0V_VGA
+1.0V_DPE_VDD10 — HCB1608KF-181T15_6 L12
C123 10U/6.3V_8, C126 1U/6.3V_4, C127 .1U/10V_4

(DPA/B_VDD18 : 1.8V@300mA+220mA) — +1.8V_VGA
+1.8V_DPA_VDD18 — HCB1608KF-181T15_6 L46
C636 10U/6.3V_8, C644 1U/6.3V_4, C647 .1U/10V_4

(DPC/D_VDD10 : 1.0V@115mA+115mA) — +1.0V_VGA
+1.0V_DPC_VDD10 — HCB1608KF-181T15_6 L9
C107 10U/6.3V_8, C661 1U/6.3V_4, C656 .1U/10V_4

( DPC/D_VDD18 : 1.8V@300mA+220mA) — +1.8V_VGA
+1.8V_DPC_VDD18 — HCB1608KF-181T15_6 L11
C643 10U/6.3V_8, C635 1U/6.3V_4, C634 .1U/10V_4

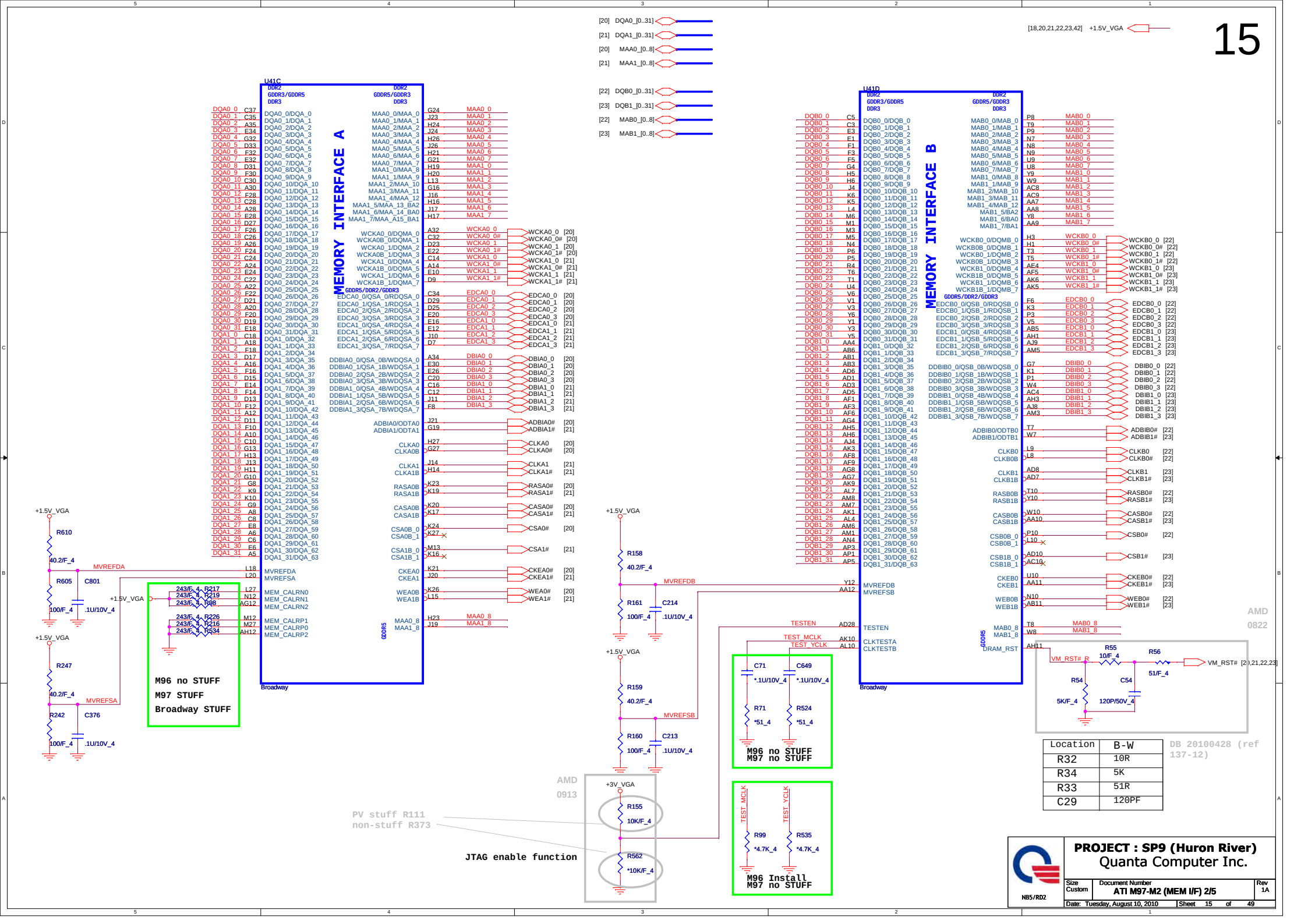
+3V
[36,39,40,41,44,49] HWPG
U4 *MC74VHC1G08DFT2G
R52 4 *10K_4
PWRGOOD_BUF
R53 10K_4

For future ASIC, if PWRGOOD_BUF is not requred it should be pulled to ground.

NB5/RD2

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ATI M97-M2 (PCIE I/F) 1/5 | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 14 of 49 | |



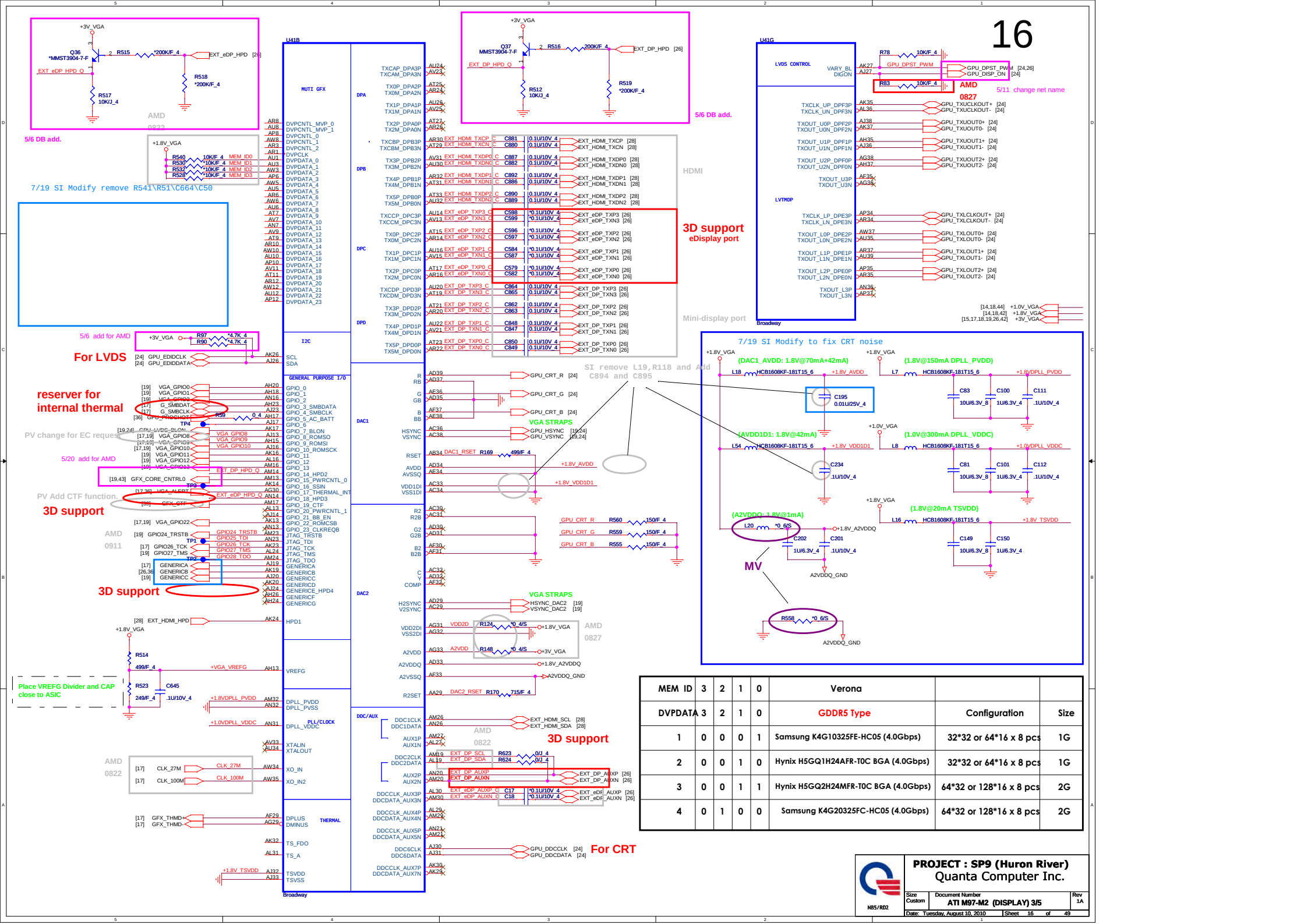

| Location | B-W |
|---|---|
| R32 | 10R |
| R34 | 5K |
| R33 | 51R |
| C29 | 120PF |

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ATI M97-M2 (MEM I/F) 2/5 | 1A |

Date: Tuesday, August 10, 2010 Sheet 15 of 49

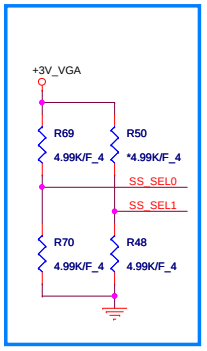
N85/RD2




| MEM ID | 3 | 2 | 1 | 0 | Verona | | |
|---|---|---|---|---|---|---|---|
| DVPDATA | 3 | 2 | 1 | 0 | GDDR5 Type | Configuration | Size |
| 1 | 0 | 0 | 0 | 1 | Samsung K4G10325FE-HC05 (4.0Gbps) | 32*32 or 64*16 x 8 pcs | 1G |
| 2 | 0 | 0 | 1 | 0 | Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps) | 32*32 or 64*16 x 8 pcs | 1G |
| 3 | 0 | 0 | 1 | 1 | Hynix H5GQ2H24MFR-T0C BGA (4.0Gbps) | 64*32 or 128*16 x 8 pcs | 2G |
| 4 | 0 | 1 | 0 | 0 | Samsung K4G20325FC-HC05 (4.0Gbps) | 64*32 or 128*16 x 8 pcs | 2G |

PROJECT : SP9 (Huron River)
Quanta Computer Inc.
NB5/RD2
Size: Custom | Document Number: ATI M97-M2 (DISPLAY) 3/5 | Rev: 1A
Date: Tuesday, August 10, 2010 | Sheet 16 of 49

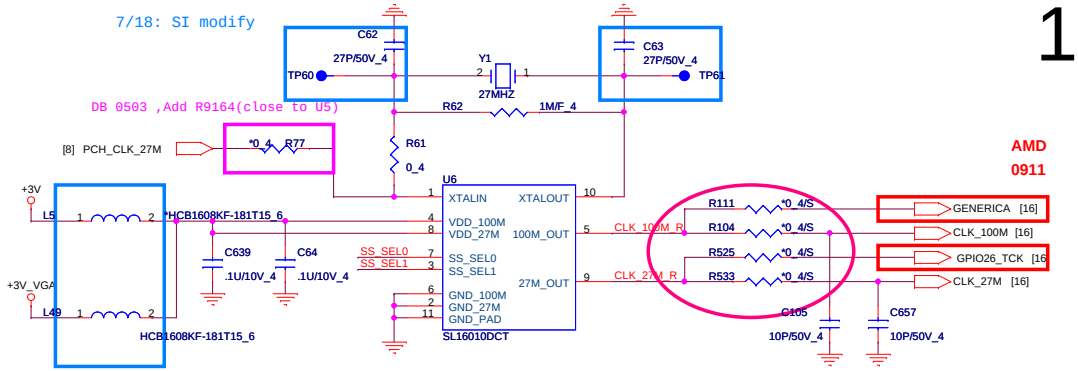
## 27MHz + 100Mhz OSC Option




7/18: SI modify

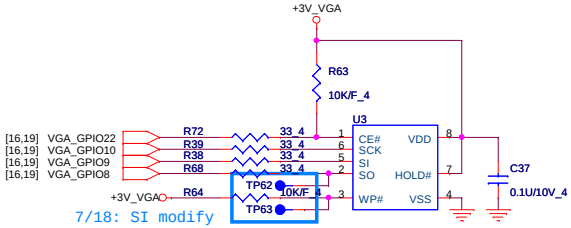
7/18: SI modify

DB 0503 ,Add R9164(close to U5)




AMD
0911

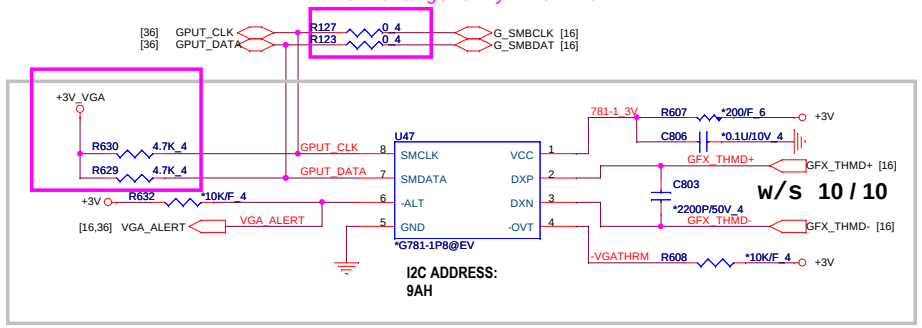
## Ext EEPROM




7/18: SI modify

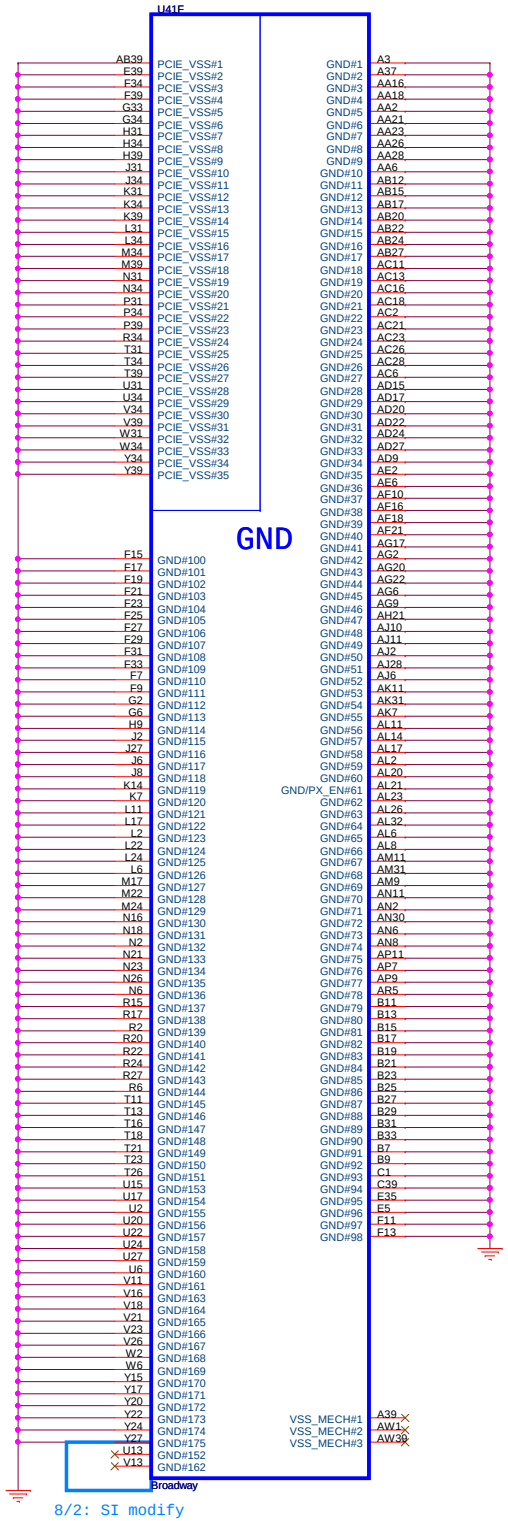
## Thermal Sensor

4/19: change only from VGA

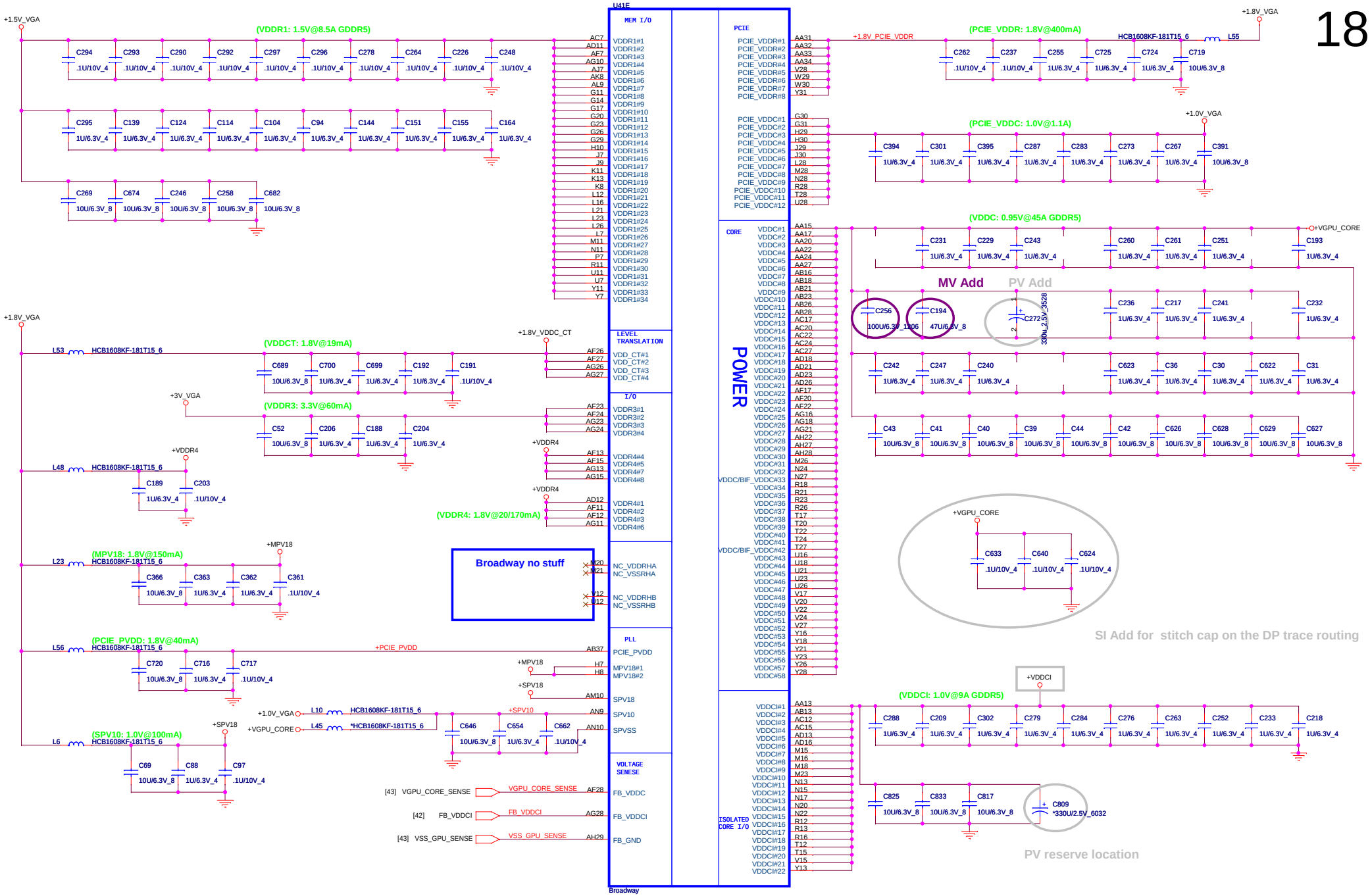



[2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] +3V

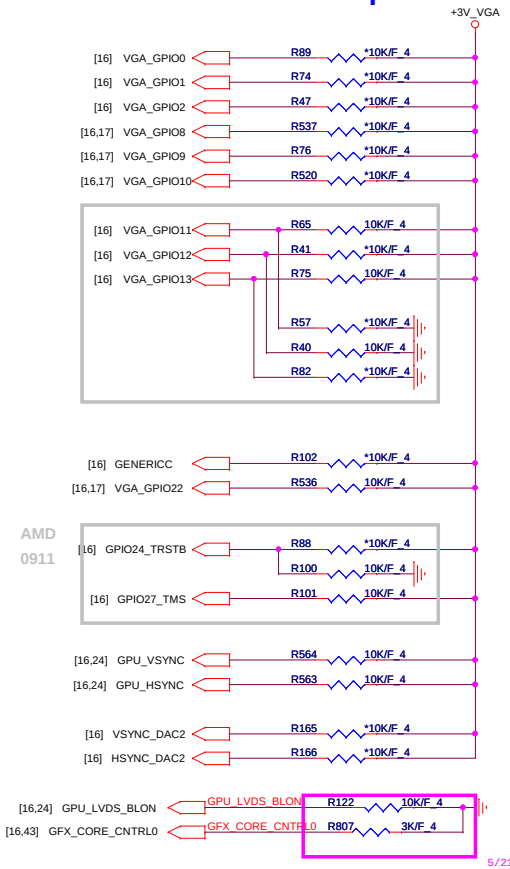
[15,16,18,19,26,42] +3V_VGA




8/2: SI modify


U41E
MEM I/O
PCIE
POWER
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
Broadway
(VDDR1: 1.5V@8.5A GDDR5)
(VDDCT: 1.8V@19mA)
(VDDR3: 3.3V@60mA)
(VDDR4: 1.8V@20/170mA)
(MPV18: 1.8V@150mA)
(PCIE_PVDD: 1.8V@40mA)
(SPV10: 1.0V@100mA)
(PCIE_VDDR: 1.8V@400mA)
(PCIE_VDDC: 1.0V@1.1A)
(VDDC: 0.95V@45A GDDR5)
(VDDCI: 1.0V@9A GDDR5)
Broadway no stuff
MV Add
PV Add
SI Add for stitch cap on the DP trace routing
PV reserve location
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
ATI M97-M2 (POWER) 5/5
NB5/RD2
Size Custom
Rev 1A
Date: Tuesday, August 10, 2010
Sheet 18 of 49

# Straps




Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

5/21 add pu down by AMD request.

**Table 3-34 ROM Configurations**

| Manufacturer | Part Number | Size | CONFIG[2:0] |
|---|---|---|---|
| Atmel | AT25F512 | 512 kbit | 001 |
| | AT25F512A | 512 kbit | 010 |
| | AT25F1024 | 1 Mbit | 011 |
| | AT25F1024A | 1 Mbit | 011 |
| | AT25F2048 | 2 Mbit | 011 |
| | AT25F4096 | 4 Mbit | 011 |
| ST Microelectronics | M25P05A | 512 kbit | 100 |
| | M25P10A | 1 Mbit | 101 |
| | M25P20 | 2 Mbit | 101 |
| | M25P40 | 4 Mbit | 101 |
| | M25P80 | 8 Mbit | 101 |
| Silicon Storage Technology | SST25VF512 | 512 kbit | 010 |
| | SST25VF010 | 1 Mbit | 011 |
| | SST25VF020 | 2 Mbit | 011 |
| | SST25VF040 | 4 Mbit | 011 |
| Winbond Electronics Corporation | W45B512 | 512 kbit | 110 |
| | W45B012 | 1 Mbit | 111 |
| YMC | Y25LF05 | 512 kbit | 010 |
| | SA25C020 | 2 Mbit | 011 |
| PMC | Pm25LV512 | 512 kbit | 100 |
| | Pm25LV010 | 1 Mbit | 101 |

**Default**

| Strap Name | Pin Straps | Description | Default Value |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | GPIO[1:0]:Recommend to pulling up for PICE setting.<br>GPIO_0:PCIE full TX output swing | |
| TX_DEEMPH_EN | GPIO1 | GPIO_1:PCIE Transmitter DE-EMPHASIS enabled | |
| BIF_GEN2_EN | GPIO2 | GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support.<br>(0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s) | |
| STRAP_BIF_CLK_PM_EN | GPIO8 | | |
| CONFIG[3]<br>CONFIG[2]<br>CONFIG[1]<br>CONFIG[0] | GPIO9<br>GPIO13<br>GPIO12<br>GPIO11 | | |
| BIOS_ROM_EN | GPIO22 | BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type.<br>(See table as below) | |
| AUDIO[0] | VSYNC | | |
| AUD(1) | HSYNC | | |
| VSYNC_DAC2 | V2SYNC | | |
| HSYNC_DAC2 | H2SYNC | | |
| | GENERICC | | |

# 1GB GDDR5 : CHANNEL A-0 (64M x 16)



[15] DQA0_[31..0]
[15] MAA0_[8..0]

MF=1 Mirror

U48

U19

170-BALL SDRAM GDDR5

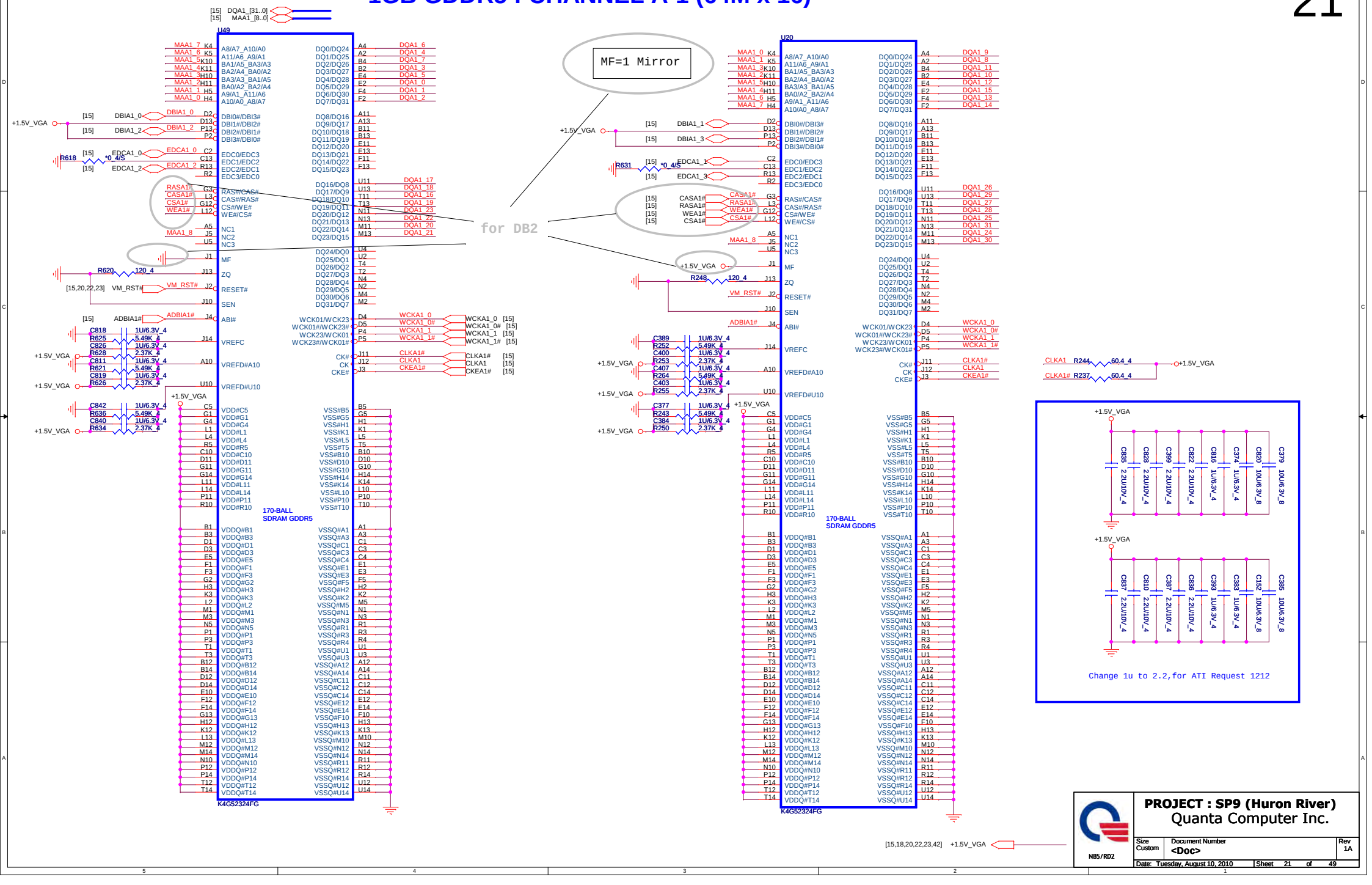
K4G52324FG

Change 1u to 2.2,for ATI Request 1212

[15,18,21,22,23,42] +1.5V_VGA

# 1GB GDDR5 : CHANNEL A-1 (64M x 16)





# 1GB GDDR5 : CHANNEL B-0 (64M x 16)



[15] DQB0_[0..31]
[15] MAB0_[0..8]

MF=1 Mirror

U16

U42

170-BALL SDRAM GDDR5

K4G52324FG

Change 1u to 2.2,for ATI Request 1212

[15,18,20,21,23,42] +1.5V_VGA

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

NB5/RD2

Size: Custom | Document Number: <Doc> | Rev: 1A

Date: Tuesday, August 10, 2010 | Sheet 22 of 49

# 1GB GDDR5 : CHANNEL B-1 (64M x 16)



[15] DQB1_[0..31]
[15] MAB1_[0..8]

MF=1 Mirror

for DB2

U40

U9

170-BALL SDRAM GDDR5

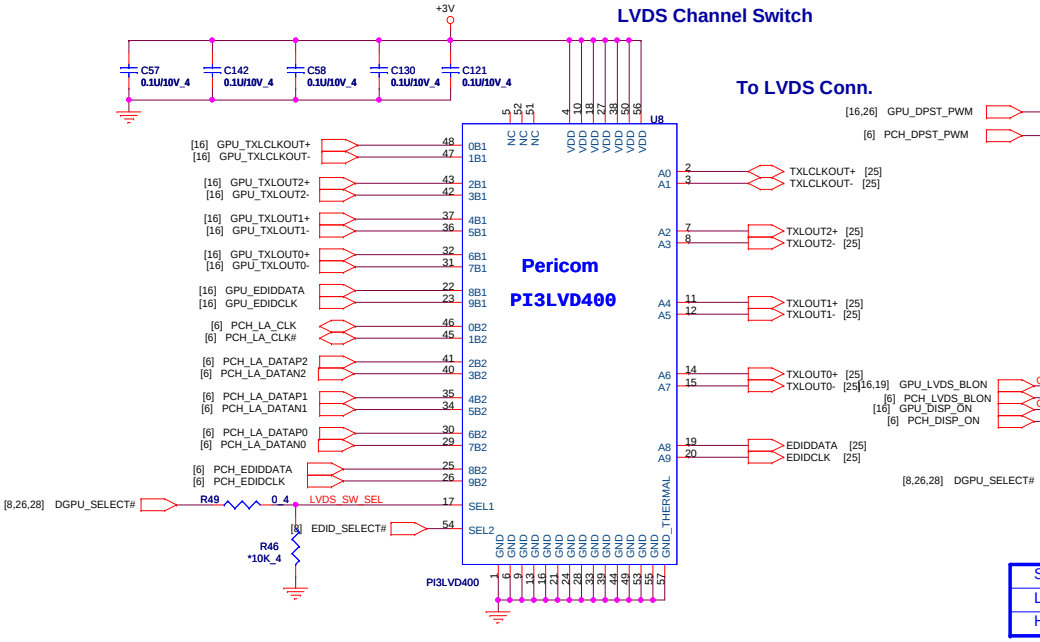
K4G52324FG

Change 1u to 2.2,for ATI Request 1212

[15,18,20,21,22,42] +1.5V_VGA

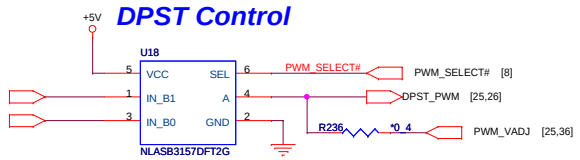
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
N85/RD2
Size Custom
Document Number <Doc>
Rev 1A
Date: Tuesday, August 10, 2010
Sheet 23 of 49

## LVDS Channel Switch

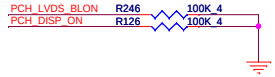



| SEL | FUNCTION |
|---|---|
| LOW | DGPU (AN to B1) |
| HIGH | IGPU (AN to B2) |

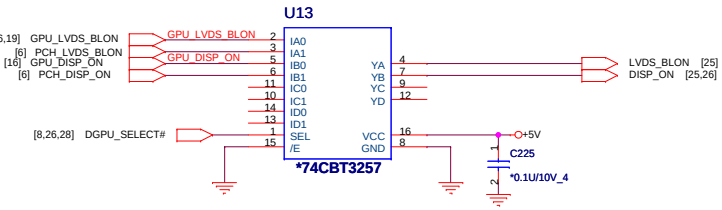
## DPST Control




| SEL | FUNCTION(COM) |
|---|---|
| LOW | IN_B0 to A |
| HIGH | IN_B1 to A |

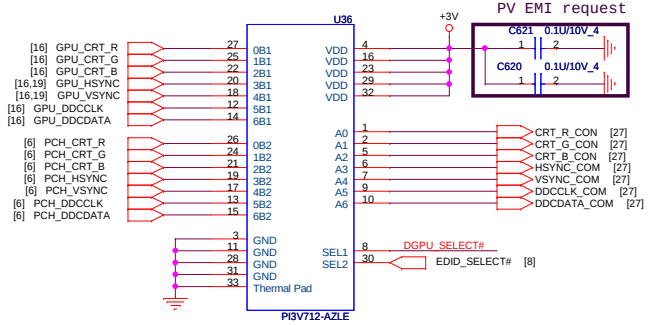



## LCD BLON/ DISP control

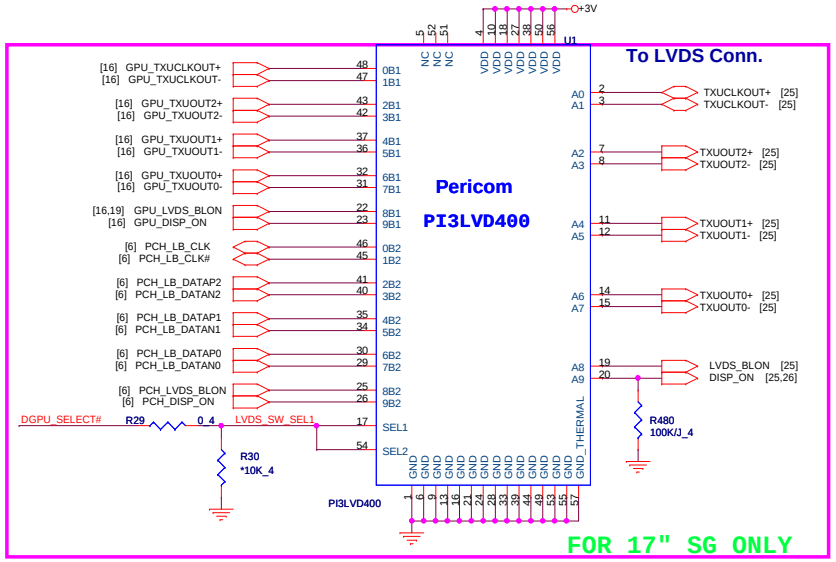


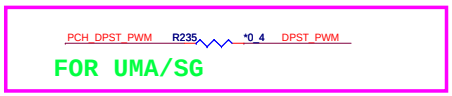

| SEL | FUNCTION(COM) |
|---|---|
| LOW | IN_B1 to A |
| HIGH | IN_B2 to A |

## VGA SWITCH




| SEL | FUNCTION(COM) |
|---|---|
| LOW | nB1 to An |
| HIGH | nB2 to An |




| | | |
|---|---|---|
| +3V | [2,6,7,8,9,10,12,13,14,17,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47] |
| +5V | [6,7,10,25,26,27,28,29,31,32,33,35,37,45,49] |
| +1.8V | [4,7,10,41,42] |

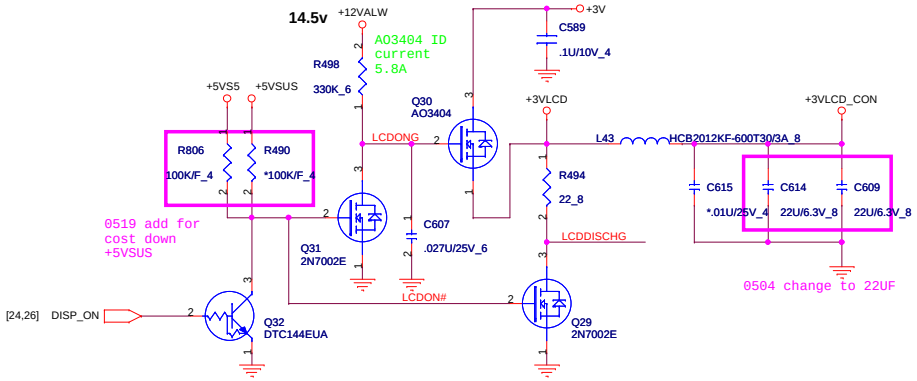
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

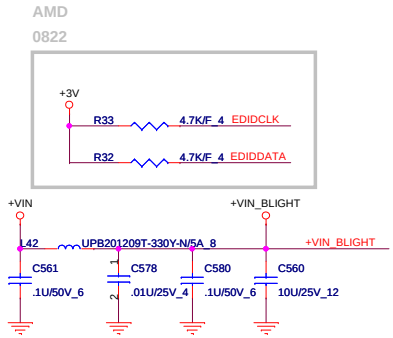
| Size | Document Number | Rev |
|---|---|---|
| Custom | SWITCHABLE | 1A |

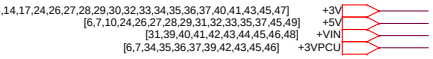
NB5/RD2

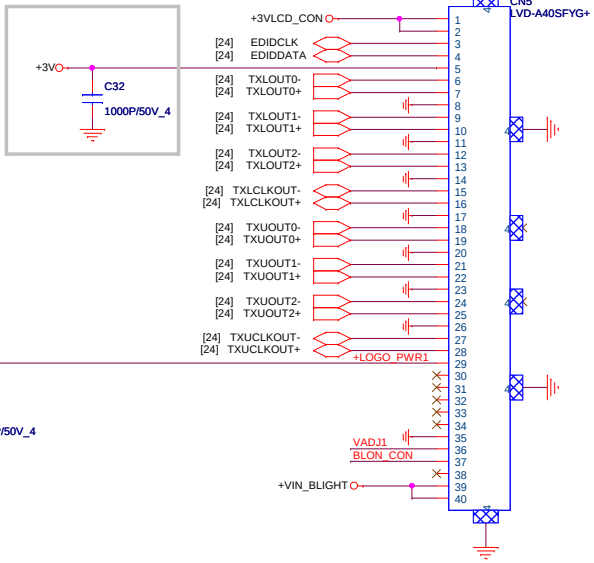
Date: Tuesday, August 10, 2010 Sheet 24 of 49

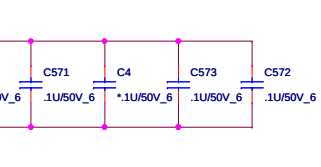
# LCD

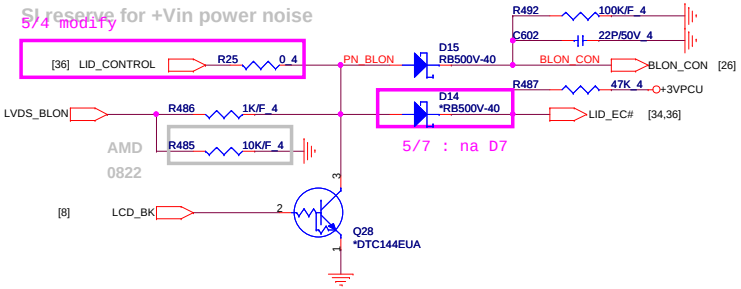


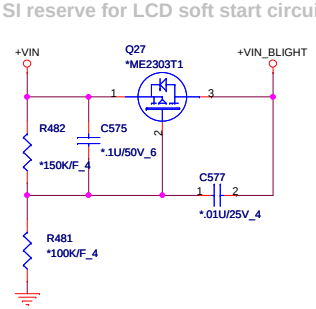



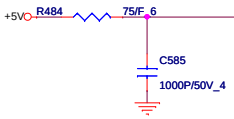



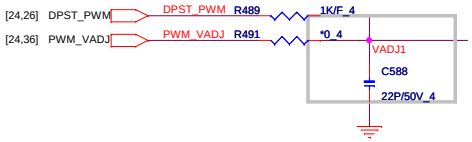



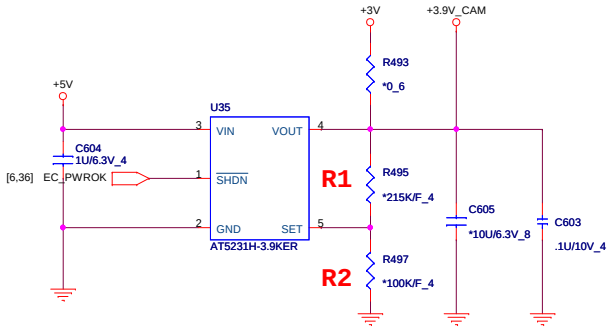



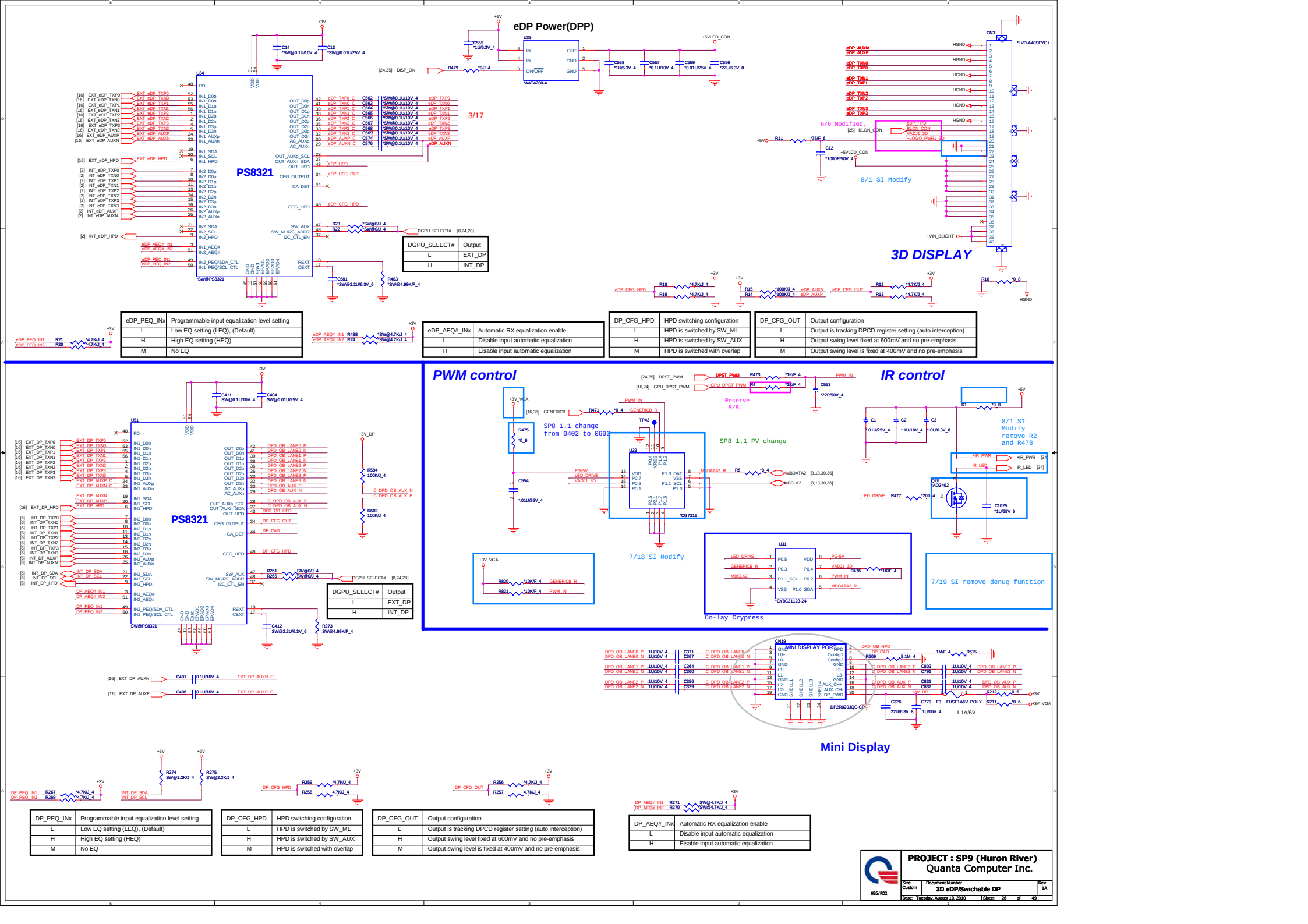




**Vout=1.25(1+R1/R2)**

| | | |
|---|---|---|
| PROJECT : SP9 (Huron River) | | |
| Quanta Computer Inc. | | |
| N85/RD2 | Size: Custom; Document Number: LCD CONN/LID function | Rev: 1A |
| | Date: Tuesday, August 10, 2010 | Sheet 25 of 49 |




| eDP_PEQ_INx | Programmable input equalization level setting |
|---|---|
| L | Low EQ setting (LEQ), (Default) |
| H | High EQ setting (HEQ) |
| M | No EQ |

| eDP_AEQ#_INx | Automatic RX equalization enable |
|---|---|
| L | Disable input automatic equalization |
| H | Eisable input automatic equalization |

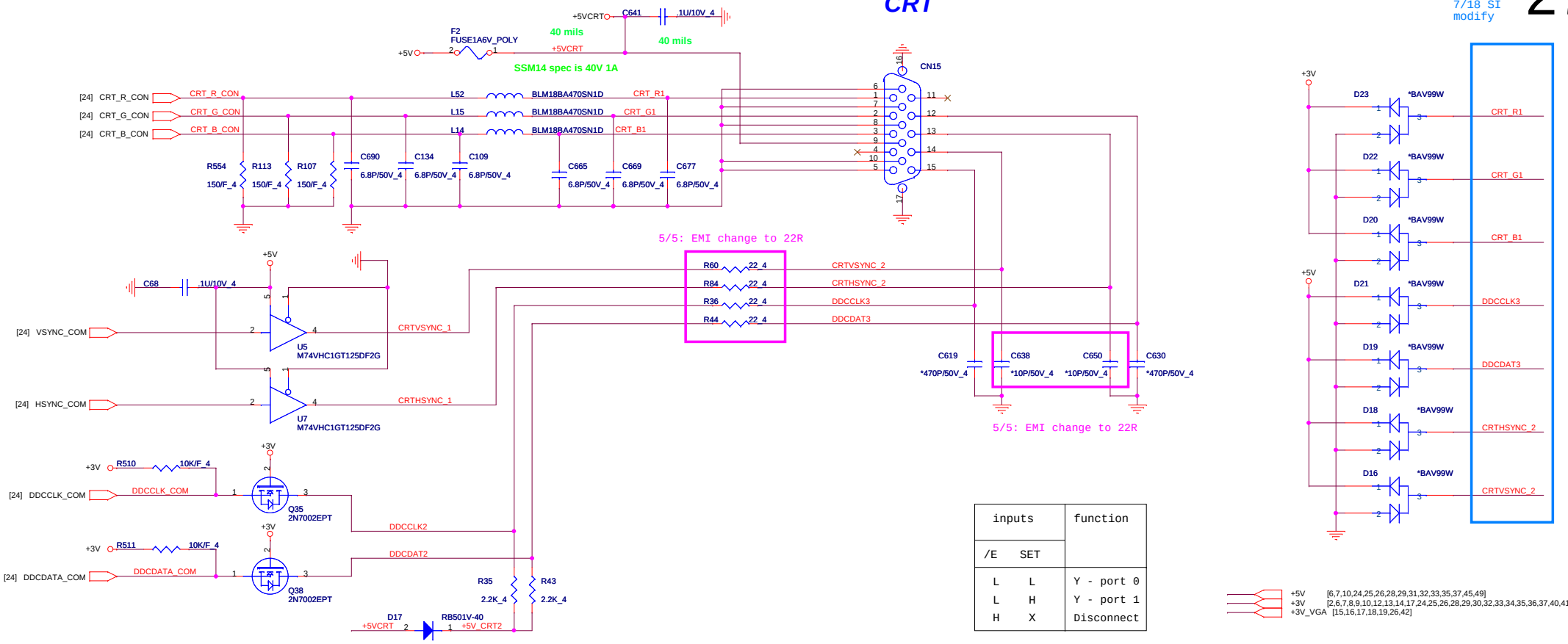
| DP_CFG_HPD | HPD switching configuration |
|---|---|
| L | HPD is switched by SW_ML |
| H | HPD is switched by SW_AUX |
| M | HPD is switched with overlap |

| DP_CFG_OUT | Output configuration |
|---|---|
| L | Output is tracking DPCD register setting (auto interception) |
| H | Output swing level fixed at 600mV and no pre-emphasis |
| M | Output swing level is fixed at 400mV and no pre-emphasis |

| DGPU_SELECT# | Output |
|---|---|
| L | EXT_DP |
| H | INT_DP |

# CRT

7/18 SI modify



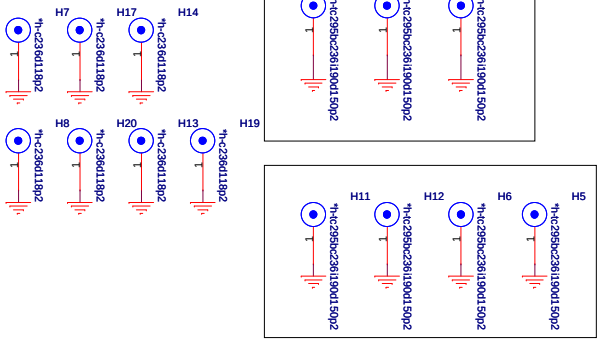

| inputs | | function |
|---|---|---|
| /E | SET | |
| L | L | Y - port 0 |
| L | H | Y - port 1 |
| H | X | Disconnect |




+5V [6,7,10,24,25,26,28,29,31,32,33,35,37,45,49]
+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+3V_VGA [15,16,17,18,19,26,42]

# HOLDs

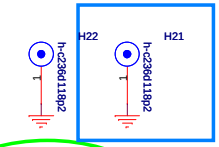
for GPU



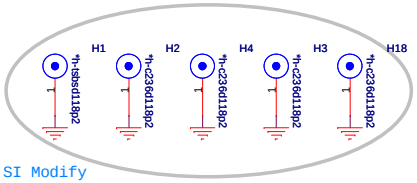

for CPU

Modify H5\H6,H11\H12\H13\H16\H17,H15 at 0506

SI ME change Footprint

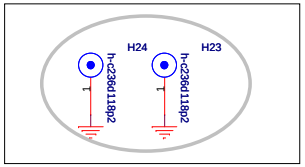


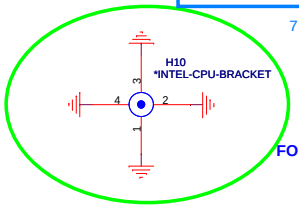

SI for ME change footprint




7/18 SI Modify

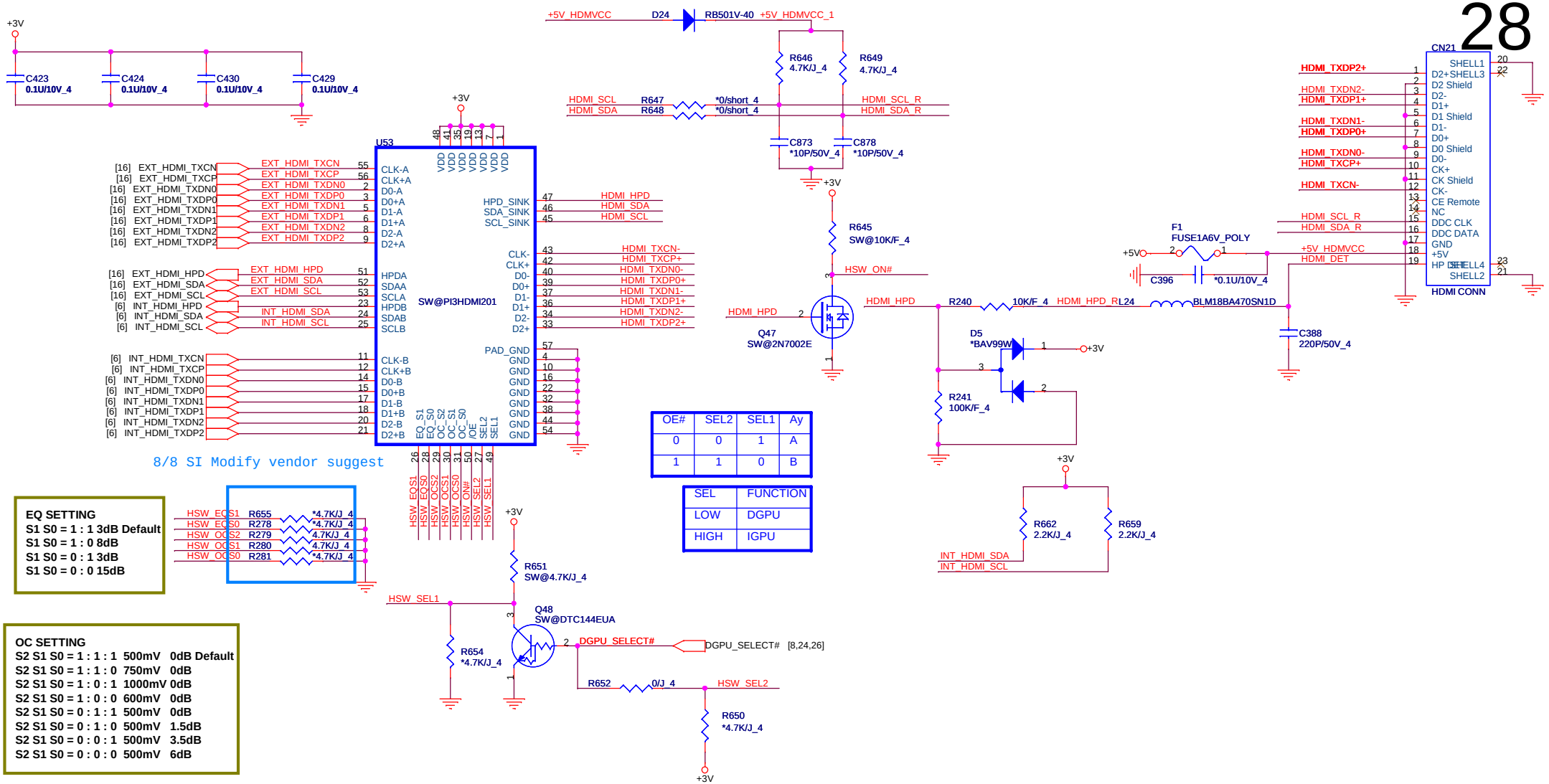
SI add for PCH hole




FOR LAYOUT

| | | |
|---|---|---|
| N85/RD2 | PROJECT : SP9 (Huron River) Quanta Computer Inc. | |
| Size Custom | Document Number CRT/HDMI Conn | Rev 1A |
| Date: Tuesday, August 10, 2010 | Sheet 27 of 49 | |




| | |
|---|---|
| PROJECT : SP9 (Huron River) | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: SG HDMI Conn |
| Rev: 1A | |
| NB5/RD2 | |
| Date: Tuesday, August 10, 2010 | Sheet 28 of 49 |

[2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,30,32,33,34,35,36,37,40,41,43,45,47] +3V
[30,31] +5V_AVDD
[6,7,10,24,25,26,27,28,31,32,33,35,37,45,49] +5V

Close to CODEC

SI change footprint from 0603 to 0805 for IDT comfirm

Close to CODEC

+5V_AVDD
+5V
L41 *BLM18PG181SN1D(180,1.5A)_6
C546 10U/6.3V_6S
C545 1U/6.3V_4
C1011 1U/10V_4
AGND
C542 1U/6.3V_4
C538 1U/10V_4
C543 10U/6.3V_6S
AGND

PV non-Stuff

+3V
C535 1U/6.3V_4
C533 1U/10V_4
+3V_DVDD_CORE
C524 10U/6.3V_6S
+3V
C531 .1U/10V_4

U30

1 DVDD_CORE
9 DVDD
3 DVDD_IO
6 HDA_BITCLK
8 HDA_SDI
5 HDA_SDO
10 HDA_SYNC
11 HDA_RST#
2 DMIC_CLK/GPIO1
4 DMIC0/GPIO2
DMIC1/GPIO0/SPDIF_OUT_1
48 SPDIF_OUT_0
47 EAPD
35 CAP-
36 CAP+
7 DVSS
33 AVSS
30 AVSS
26 AVSS
42 PVSS
49 DAP
92HD80Bx

27 AVDD
38 AVDD
>40mils
39 PVDD
45 PVDD
>40mils
13 SENSE_A
14 SENSE_B
SENSE_A [30]
28 MIC_L
29 MIC_R
23 VREFOUT
C551 2.2U/25V_8
C1015 2.2U/25V_8
EXT_MIC [30]
VREFOUT_A [30]
31 HPOUT_L
32 HPOUT_R
HPOUT_L [30]
HPOUT_R [30]
19 PORT_C_L
20 PORT_C_R
24 VREFOUT_C
40 L_SPK+
41 L_SPK-
43 R_SPK-
44 R_SPK+
15 PORT_E_L
16 PORT_E_R
17 PORT_F_L
18 PORT_F_R
12 PC_BEEP
25 MONO_OUT
22 CAP2
21 VREFFILT
34 V-
37 VREG

[HDA Bus]

[7] BIT_CLK_AUDIO R448 *0_4/S HD_BCLK
[7] ACZ_SDIN0 R449 33_4 HD_SDIN0
[7] ACZ_SDOUT_AUDIO R447 *0_4/S HD_SDOUT
C526 10P/50V_4
[7] ACZ_SYNC_AUDIO R450 *0_4/S HD_SYNC
C532 10P/50V_4
[7] ACZ_RST#_AUDIO

[Combo MIC]
[Combo HP & Salve HP]

[Digital MIC]

[34] DIGITAL_CLK
[34] DIGITAL_D1
C518 10P/50V_4 R445 100/F_4 DMIC_CLK_R
C534 10P/50V_4
DMIC0
IDT_GPIO0

[Internal Speaker]

PV Change from +5V to +5V_ADD

0901

[36] VOLMUTE#
+3V R453 10K/F_4
D12 RB500V-40
[31] ADC_EAPD#
ADC_EAPD#

Close to CODEC

CAP-
C549 4.7U/6.3V_6
CAP+

BIT_CLK_AUDIO
ACZ_SDIN0
C520 *27P/50V_4
C521 27P/50V_4
FOR EMI

AGND

SPDIF_OUT_0
SPKR_PORT_D_L+
SPKR_PORT_D_L-
SPKR_PORT_D_R-
SPKR_PORT_D_R+
AMP_BEEP
BASS_OUT
BASS_OUT [31]
ADC_CAP2
ADC_VREFFILT
ADC_V-
ADC_VREG

C992 .1U/10V_4
AMP_BEEP_L
R790 47K_4
AMP_BEEP_R2
C988 .1U/10V_4
R793 10K/F_4
C998 .1U/10V_4
AGND

+5V_AVDD
6/17
R797 10K/F_4
2N7002E Q58
SPKR [7]
AGND

SENSE_A R456 2.49K/F_4 +5V_AVDD
C539 1000P/50V_4 AGND
SENSE_B R459 100K/F_4 +5V_AVDD
C540 *1000P/50V_4 AGND

C548 4.7U/6.3V_6
C550 10U/6.3V_6S
C541 10U/6.3V_6S
C544 1U/6.3V_4
AGND AGND AGND AGND

Close to CODEC

## INT. SPEAKER

L_SPK+ L40 BK1608LL121_6 L_SPK+_R
L_SPK- L38 BK1608LL121_6 L_SPK-_R
R_SPK- L37 BK1608LL121_6 R_SPK-_R
R_SPK+ L35 BK1608LL121_6 R_SPK+_R
CN10
INT SPEAKER CONN
C990 1000P/50V_4
C994 1000P/50V_4
C996 1000P/50V_4
C1003 1000P/50V_4
AGND

## MUTE_LED

Low -->MUTE
High-->un-Mute

+3V
R462 *100K/F_4
[35] MUTE_LED#
+3V R458 10K/F_4
VOLMUTE#
IDT_GPIO0
D13 BAT54A
MUTE_LED_R
Q23 2N7002E

C948 *1000P/50V_4
C547 *1000P/50V_4
C501 *.1U/10V_4
C993 *.1U/10V_4
C960 *10P/50V_4
C972 *10P/50V_4
C509 *1000P/50V_4
C1013 *1000P/50V_4
C966 *.1U/10V_4
C511 *.1U/10V_4
C975 *10P/50V_4
C503 *10P/50V_4
AGND

R759 *0_6/S
R795 *0_6/S
R789 *0_6/S
AGND

| | | | |
|---|---|---|---|
| | PROJECT : SP9 (Huron River) Quanta Computer Inc. | | |
| N85/RD2 | Size: Custom | Document Number: Azalia 92HD80 | Rev: 1A |
| | Date: Tuesday, August 10, 2010 | Sheet 29 of 49 | |

SI change to TPA6130A2 and modify sense circuit

+5V_AVDD
C516 1U/10V_X5R_6
C510 1U/10V_X5R_6
C508 1U/10V_X5R_8
AGND
U29
TPA6130A2
[29] HPOUT_L
HPOUT
R444 *0_6/S
C976 1U/10V_X5R_6
[29] HPOUT_R
R443 *0_6/S
C977 1U/10V_X5R_6
LEFTINML-
LEFTINP+
RIGHTINP+
RIGHTINM-
LINEOUT_L
LINEOUT_R
C507 1U/10V_X5R_6
R435 2K/F_4
C515 0.1U/10V_4
AMP_SDA
AMP_SCL
TPA6130A2

+3V +5V_AVDD
R755 0_4
R754 *0_4
R762 *2K/F_4
R758 *2K/F_4
Reserve for Amp I2C 5/4.
PV Stuff
[8] AMP_SDA
[8] AMP_SCL

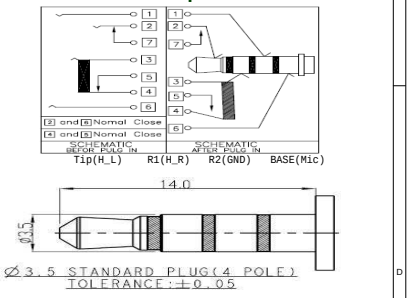
Line out
AGND SHIELD
LINEOUT_L R452 16.1/F_4
LINEOUT_R R451 16.1/F_4
HPOUT_L1 L36 BK1608HM241
HPOUT_R1 L34 BK1608HM241
HPOUT_L2
HPOUT_R2
C536 1000P/50V_4
C527 1000P/50V_4
C537 0.1U/10V_4
C525 0.1U/10V_4
SENSE_PHONE
CN27
HP-JACK-GREEN
Normal Close

SENSE_A [29]
R438 20K/F_4
R442 10K/F_4
SENSE_PHONE
Q20 DMN601K-7
R437 10K/F_4
Q18 DMN601K-7
JACK_SN#
Q55 DMN601K-7
R454 20K/F_4
HEADSET_DETECT
Q22 DMN601K-7
R455 39.2K/F_4
R446 10K/F_4
Q21 DMN601K-7
C528 220P/50V_4

[29] VREFOUT_A
C505 1U/6.3V_4
R429 2.2K_4
R428 47K_4
C504 1U/6.3V_4
L30 BK1608HM241
C499 10U/6.3V_8
D9 BAT54C T/R
R427 10K/F_4
U28 LMV331M5X
R773 560K/F_4
R436 47K_4
Combo Jack
PV change net name 1211
LINEOUT_L R441 16.1/F_4
LINEOUT_R R430 16.1/F_4
HPOUT_L1_C L33 BK1608HM241
HPOUT_R1_C L31 BK1608HM241
HPOUT_L2_C
HPOUT_R2_C
CN26
AUDIO JACK CONN
Normally close
[29] EXT_ MIC
EXT_ MIC L32 BK1608HM241
EXT_ MIC_L2
C519 220P/50V_4
C506 220P/50V_4
C517 .01U/16V_4
C500 .01U/16V_4
C512 220P/50V_4

SI change to with ESD function

SI change footprint and pin out




## Accelerometer Sensor

+3V
U45
*HP302DLTR8
C776 *10U/6.3V_8
C769 .1U/10V_4
C768 .1U/10V_4
[8] [36] INTH# G_INT2#
[8,13,26,36] MBDATA2
[8,13,26,36] MBCLK2
R593 *10K/F_4
Vdd_IO
VDD
Reserved
INT1
INT2
SDO
SDA/SDI/SDO
SCL/SPC
CS
GND

7/18: SI Add

U60
HP3DCTR
R815 0_4
R816 0_4
RESERVED

Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex

NB5/RD2

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | AMP_TPA6047/Accelerometer | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 30 of 49 | |

# SUBWOOFER

PV change R575 from 20K to 10K for HP request

Change 4EQ to 2EQ

SI add LDO for SUBWOOFER power

for PV

Vset=1.242V

DB modified 20100429

MV

7/18 SI Modify

close to Connect

for DB2

MV add R317

## Sub-Woofer power

MV

SI change type

| GAIN1 | GAIN0 | dB |
|---|---|---|
| 0 | 0 | 20 |
| 0 | 1 | 26 |
| 1 | 0 | 32 |
| 1 | 1 | 36 |

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5V_AVDD [29,30]
+VIN [25,39,40,41,42,43,44,45,46,48]

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SUBWOOFER (EQ & AMP.) | 1A |
| Date: Tuesday, August 10, 2010 | Sheet 31 of 49 | |

N85/RD2

4/19 change FB to small size

7/27 SI Modify

5/9 modify

Close to U14 pin 34,35

GND VIA x 9 Pcs

AL08111DB00 RTL8111E-VB-GR

U21 RTL8111E-VB-GR

U50 NS892405

NS892402:GIGABIT DB0AT9LAN05

>60mil >60mil

Power trace Layout 寬度> 60mil

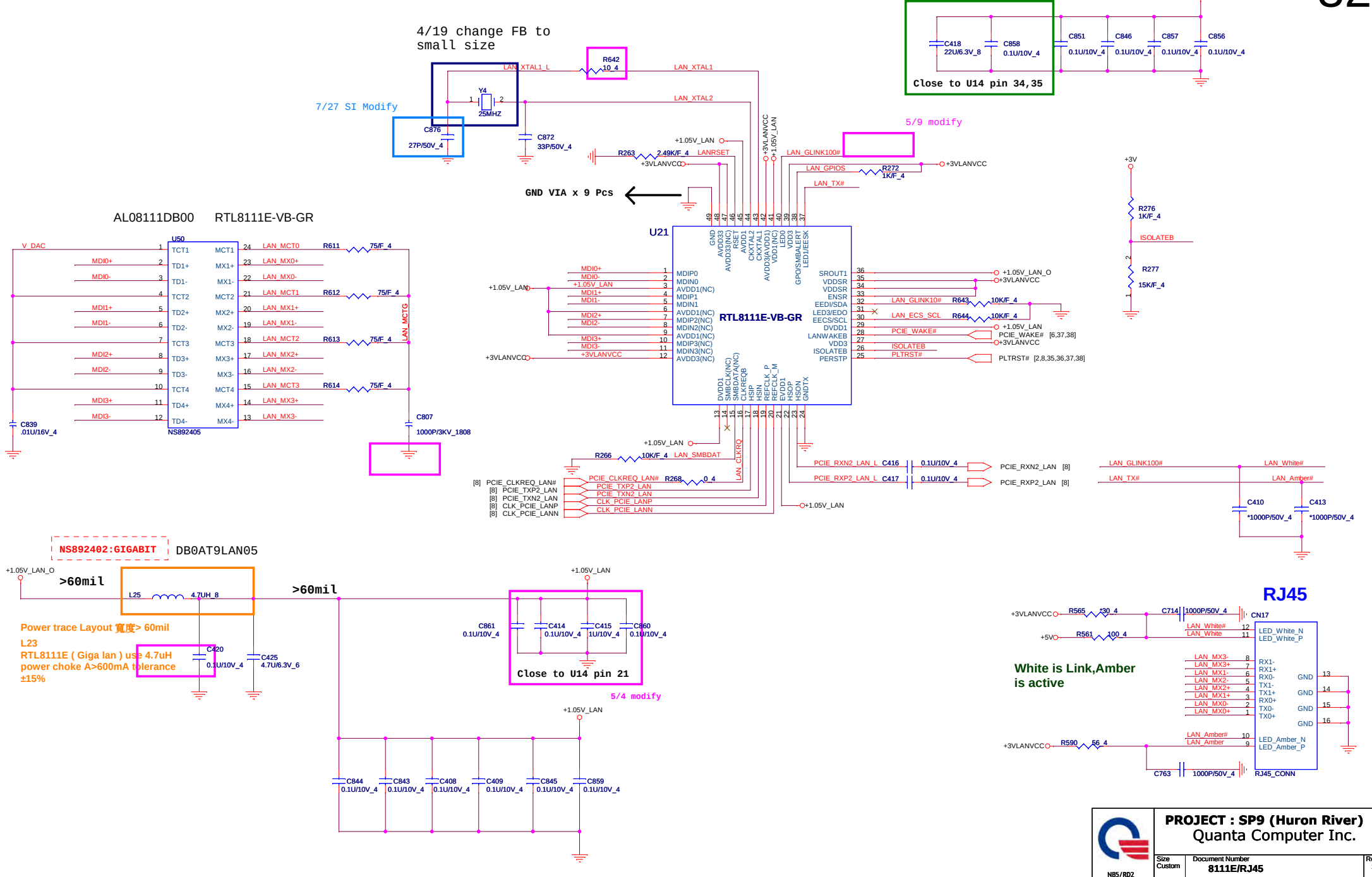
L23
RTL8111E ( Giga lan ) use 4.7uH
power choke A>600mA tolerance ±15%

Close to U14 pin 21

5/4 modify

RJ45

White is Link,Amber is active



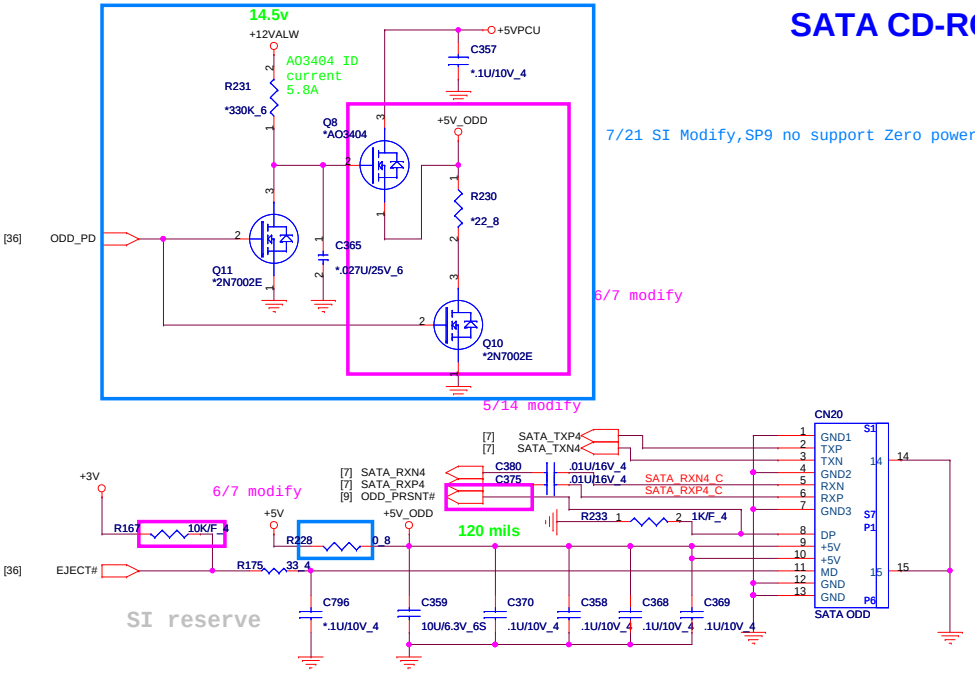

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | 8111E/RJ45 | 1A |

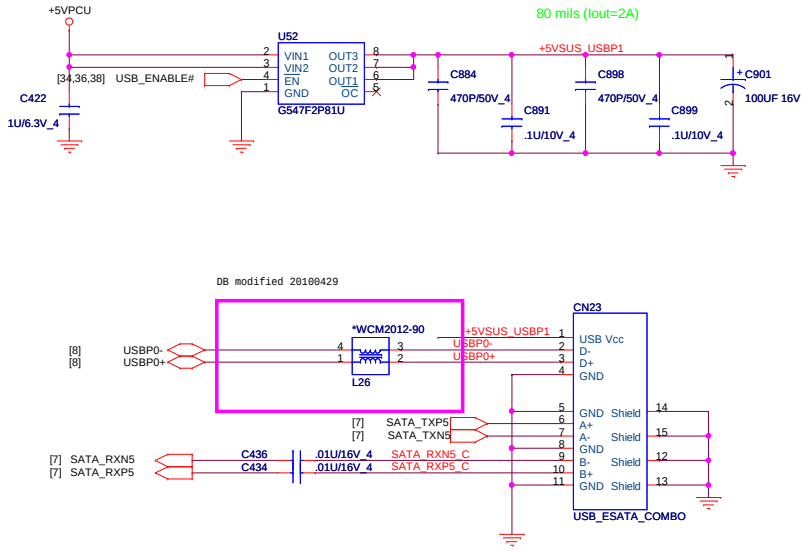
N85/RD2

Date: Tuesday, August 10, 2010 Sheet 32 of 49

## SATA CD-ROM

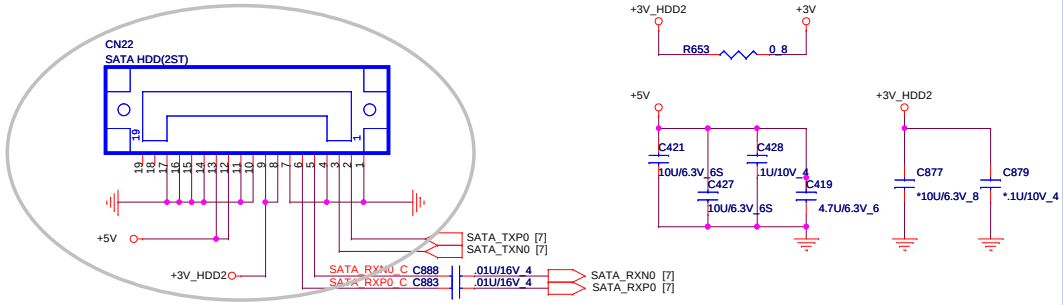



## E-SATA



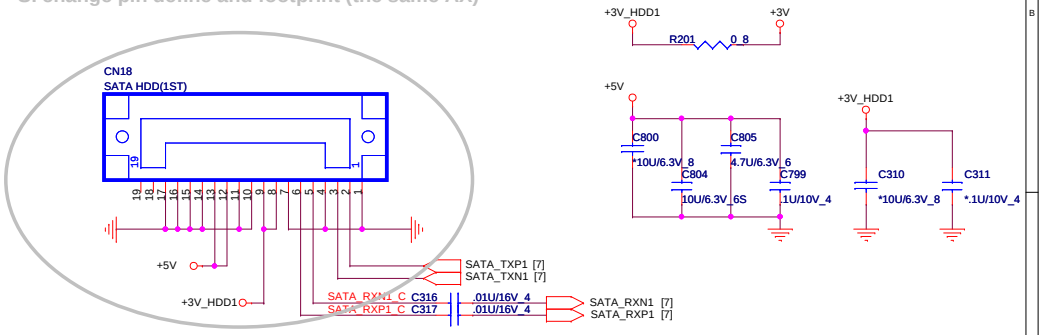

## SATA HDD #1

SI change pin define and footprint (the same AX)



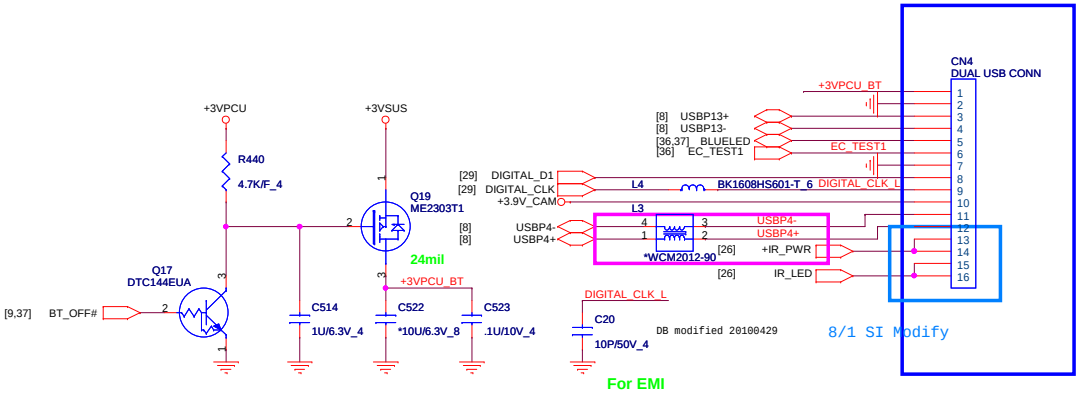

## SATA HDD #2

SI change pin define and footprint (the same AX)

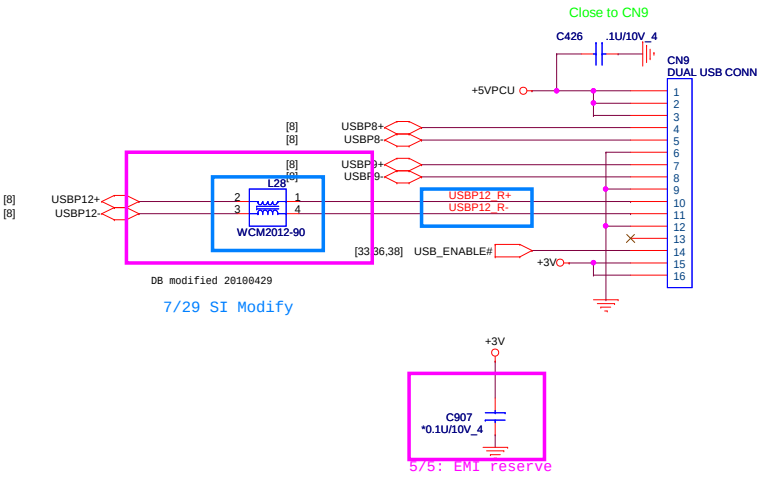



| | | |
|---|---|---|
| N85/RD2 | PROJECT : SP9 (Huron River)<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: ODD/HDD/ONFI | Rev: 1A |
| Date: Tuesday, August 10, 2010 | Sheet 33 of 49 | |

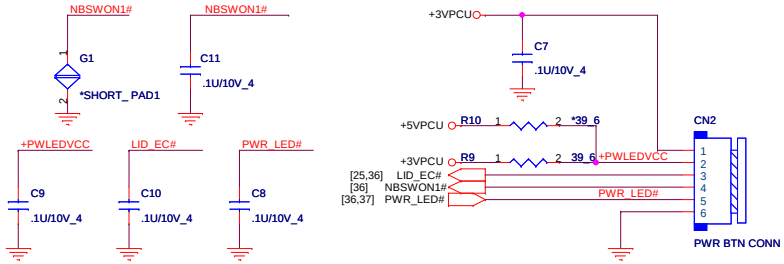
## Bluetooth




## Ext USB & Card Reader

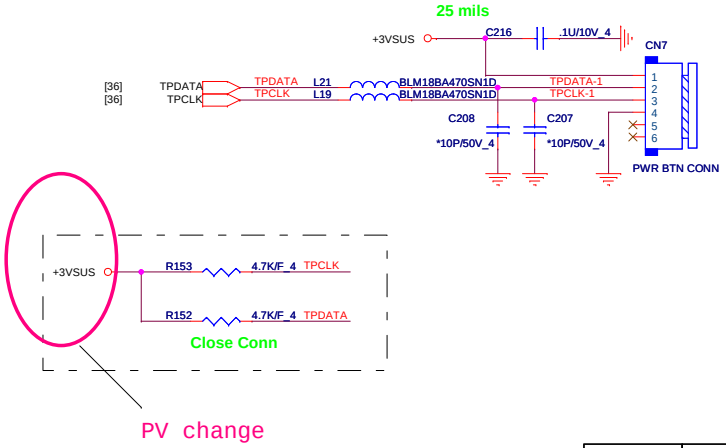



## Power Botton




1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

## Touch Pad Botton




**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | BT/WC/FT/Touchscreen | 1A |
| N85/RD2 | Date: Tuesday, August 10, 2010 | Sheet 34 of 49 |

# Mini Display



[36] MY[0..17] → MY[0..17]
[36] MX[0..7] → MX[0..7]

8/5 SI modify

RP7
MY2 MY4 MY15 MY1 → MY3 MY5 MY6 MY0
+3VPCU
*10P8R-8.2K

RP6
MY12 MY13 MY8 MY7 → MY14 MY9 MY11 MY10
*10P8R-8.2K

R221 *8.25K/F_4 MY16
R220 *8.25K/F_4 MY17

CN8
MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17
WIRELESS_ON_R
WIRELESS_OFF_R
[29] MUTE_LED#
[36] CAPSLED#
R222 200_4
R223 200_4
+3V
KB CONN

+12VALW
R556 100K/F_4
R557 1M_4
Q41 2N7002E
[36] KB_LED_EN
+5V
Q40 AO3404
R553 *0_8
C706 .1U/50V_6
C686 .1U/10V_4
140 mA
+5V_LED_KBLIGHT
CN6
88513-0401-4P-L-smt
DFFC04FR042
KB LIGHT CONN

1. LEDVCC
2. LEDVCC
3. GND
4. GND

6/6 changed FP to 0603
7/18 SI modify

MY5 C346 MY6 C339 MY3 C338 MY7 C341 — 220P/50V_4
MY8 C340 MY9 C352 MY10 C333 MY11 C334 — 220P/50V_4
MY1 C345 MY2 C343 MY4 C342 MY0 C349 — 220P/50V_4
MX4 C351 MX6 C353 MX3 C347 MX2 C348 — 220P/50V_4
MX7 C354 MX0 C344 MX5 C350 MX1 C355 — 220P/50V_4
MY12 C337 MY13 C336 MY14 C335 MY15 C332 MY16 C331 MY17 C330 — 220P/50V_4

## FOR SG ONLY

+3V
U25 MC74VHC1G08DFT2G
C478 0.1U/10V_4
[2,8,32,36,37,38] PLTRST#
[8] DGPU_HOLD_RST#
R392 330_4 DGPU_HIN_RST#
R393 100K_4
PEGX_RST# [14]

## PV Modify
change from non-stuff to stuff

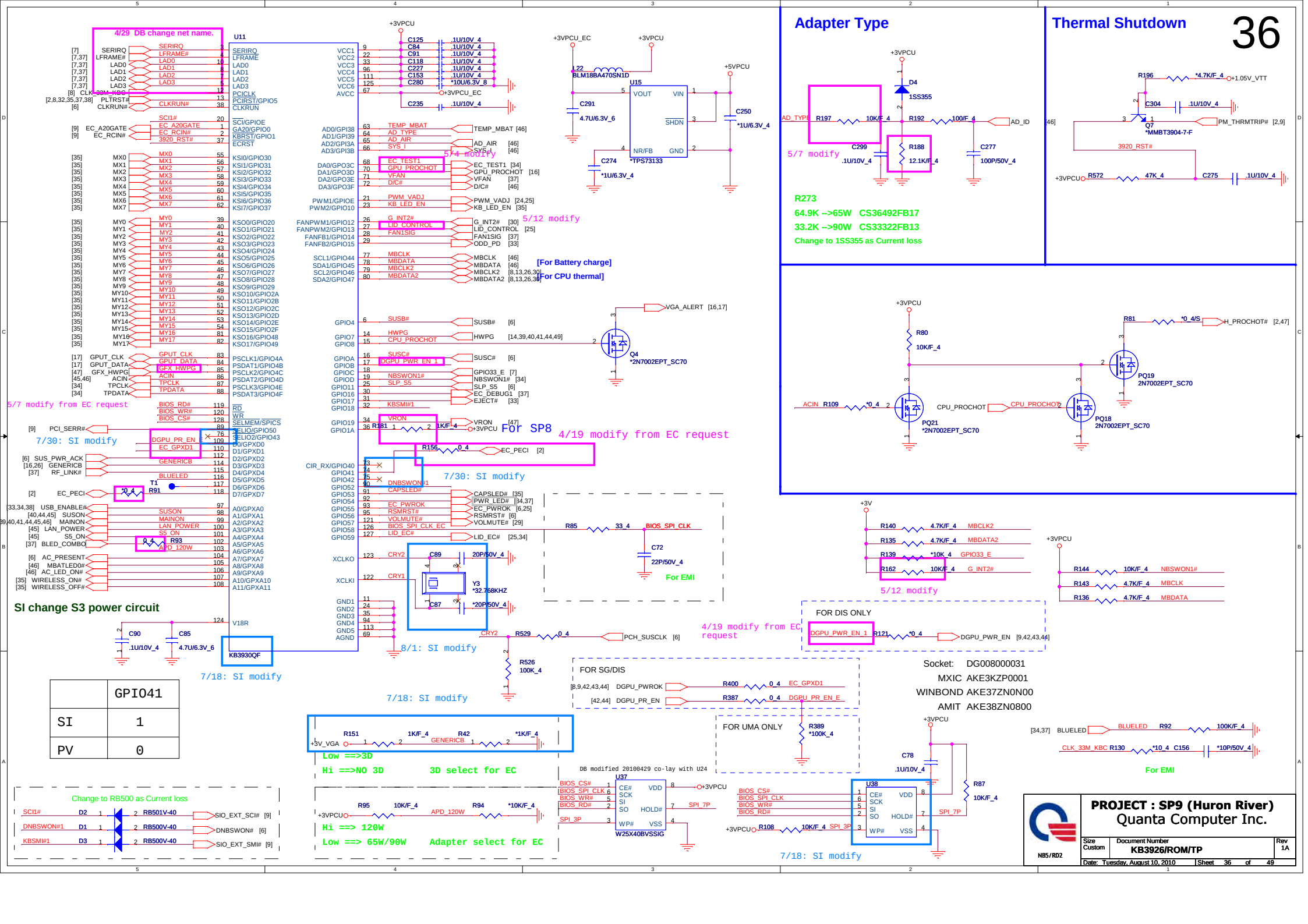
+5V
R616 1K/F_4
R225 *200/F_6
WIRELESS_ON_R
[36] WIRELESS_ON#
Q45 PDTC144EU

+5V
R617 1K/F_4
R224 *200/F_6
WIRELESS_OFF_R
[36] WIRELESS_OFF#
Q46 PDTC144EU

LED1 Wireless Enable White 27
LED2 Wireless Disable Amber 28
LED3 Mute Amber 29
LED4 Caps White 30
VCC 31
VCC 32

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

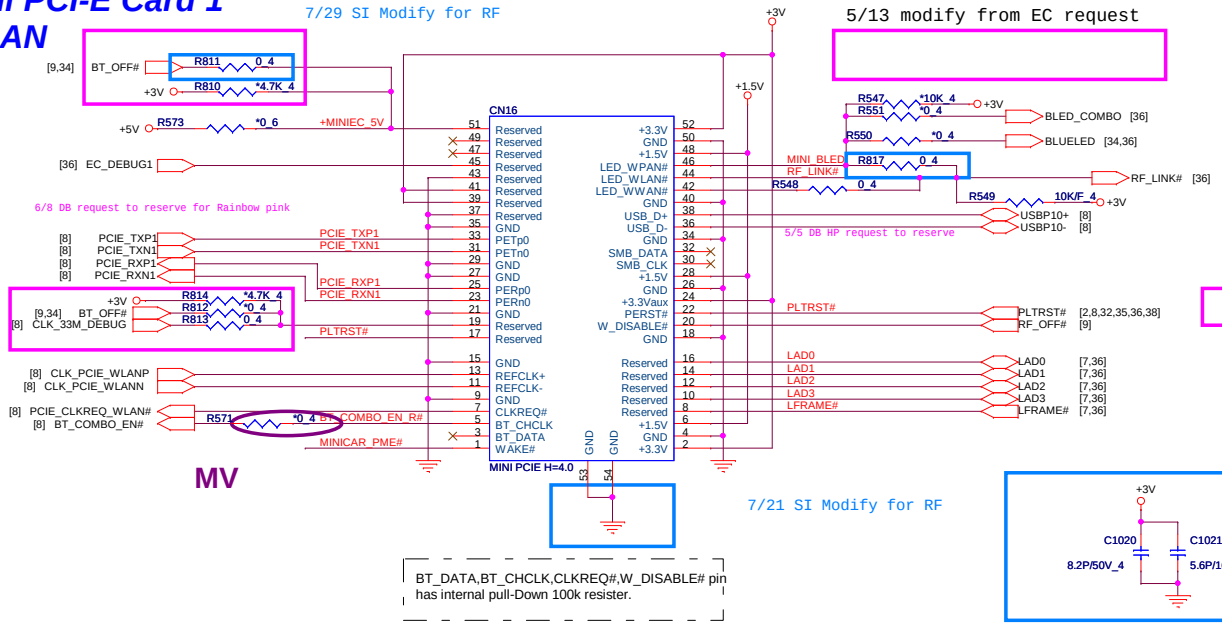
| Size | Document Number | Rev |
|---|---|---|
| Custom | KB/LED/POWER CONN | 1A |
| N85/RD2 | Date: Tuesday, August 10, 2010 | Sheet 35 of 49 |


4/29 DB change net name.
U11
KB3930QF
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLK_33M_KBC
PLTRST#
CLKRUN#
SCI1#
EC_A20GATE
EC_RCIN#
3920_RST#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MY16
MY17
GPUT_CLK
GPUT_DATA
GFX_HWPG
ACIN
TPCLK
TPDATA
BIOS_RD#
BIOS_WR#
BIOS_CS#
PCI_SERR#
DGPU_PR_EN
EC_GPXD1
GENERICB
BLUELED
EC_PECI
SUSON
MAINON
LAN_POWER
S5_ON
APD_120W
AC_PRESENT
MBATLED0#
AC_LED_ON#
WIRELESS_ON#
WIRELESS_OFF#
V18R
7/30: SI modify
7/18: SI modify
SI change S3 power circuit
GPIO41
SI 1
PV 0
Change to RB500 as Current loss
RB501V-40
RB500V-40
SIO_EXT_SCI#
DNBSWON#
SIO_EXT_SMI#
5/7 modify from EC request
5/4 modify
5/12 modify
[For Battery charge]
[For CPU thermal]
For SP8
4/19 modify from EC request
For EMI
8/1: SI modify
4/19 modify from EC request
Low ==>3D
Hi ==>NO 3D
3D select for EC
Hi ==> 120W
Low ==> 65W/90W
Adapter select for EC
DB modified 20100429 co-lay with U24
W25X40BVSSIG
FOR SG/DIS
FOR UMA ONLY
FOR DIS ONLY
Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800
Adapter Type
R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss
5/7 modify
Thermal Shutdown
36
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
N85/RD2
Size Custom
Document Number KB3926/ROM/TP
Rev 1A
Date: Tuesday, August 10, 2010
Sheet 36 of 49

# Mini PCI-E Card 1 WLAN

7/29 SI Modify for RF

5/13 modify from EC request

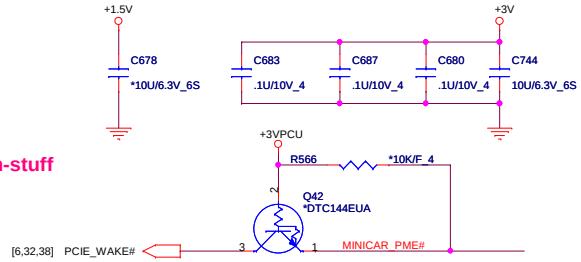


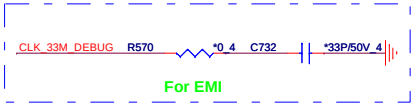

MV

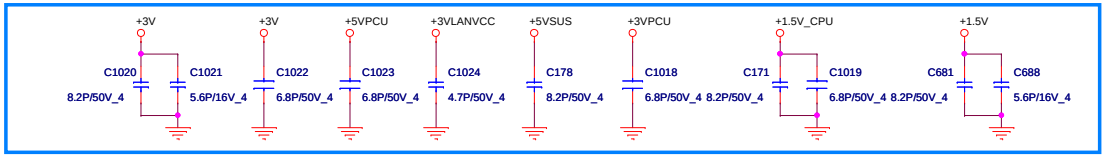
7/21 SI Modify for RF

BT_DATA,BT_CHCLK,CLKREQ#,W_DISABLE# pin has internal pull-Down 100k resister.

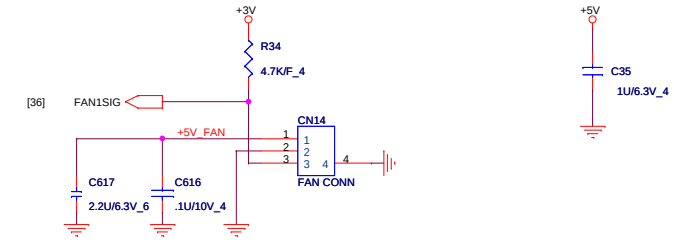
PV non-stuff



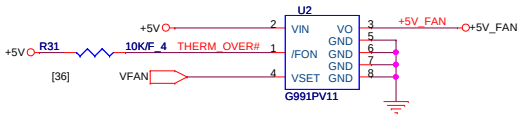



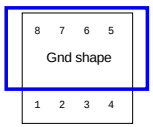

# CPU FAN




FANPWR = 1.6*VSET 30 MIL



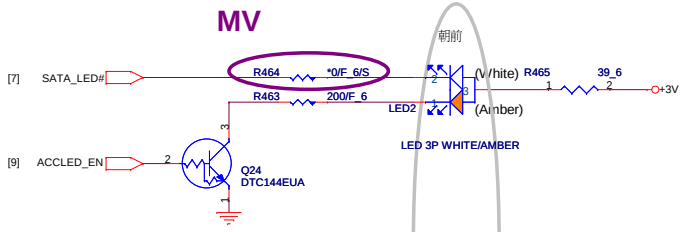

G995 layout notice



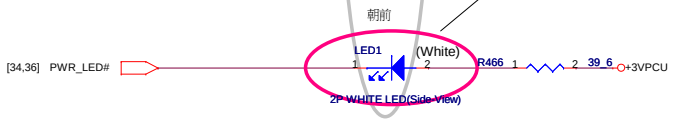

# LED

SI Change Fpptprint

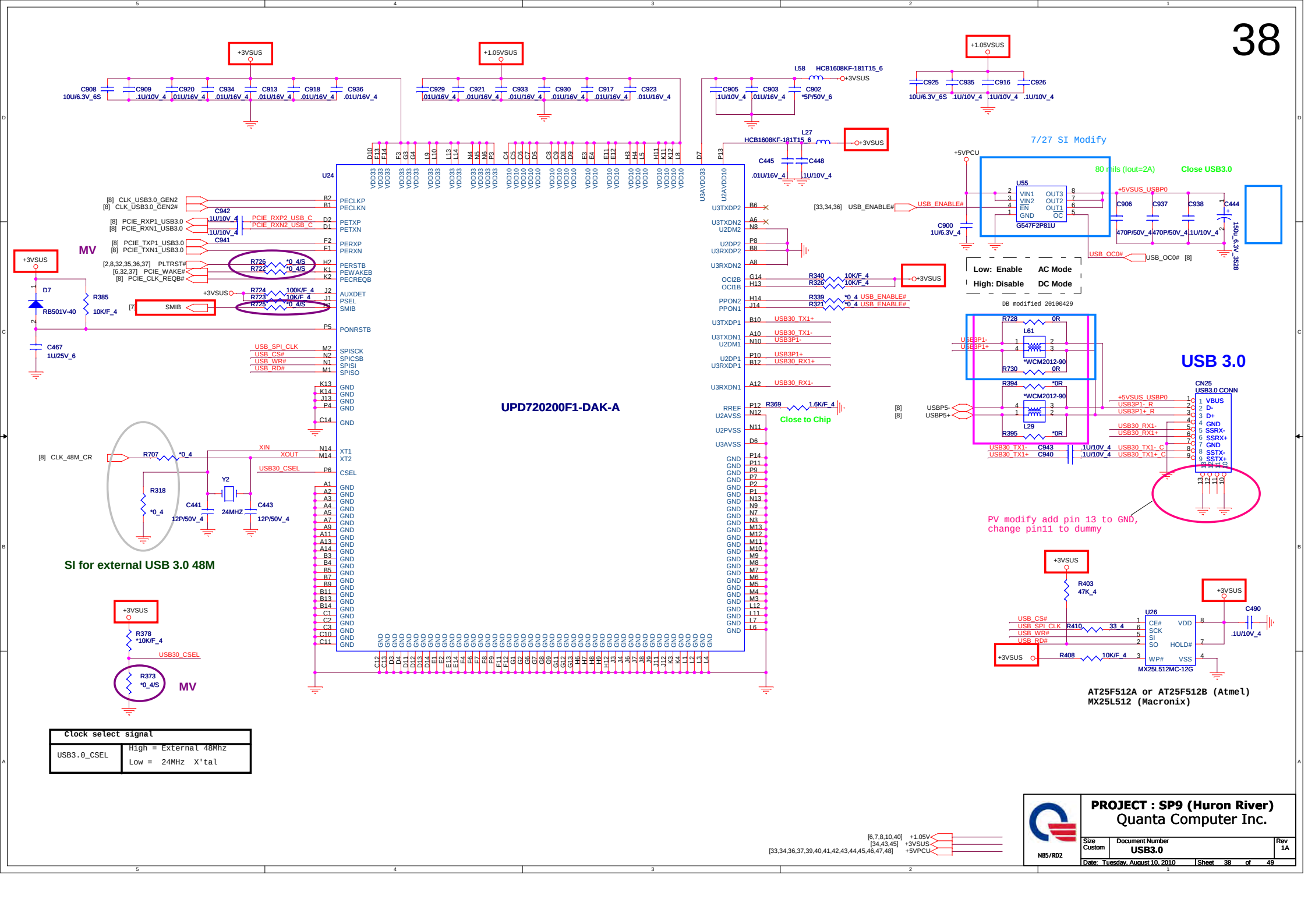
MV




PV Change Fpptprint for solve SMT open issue

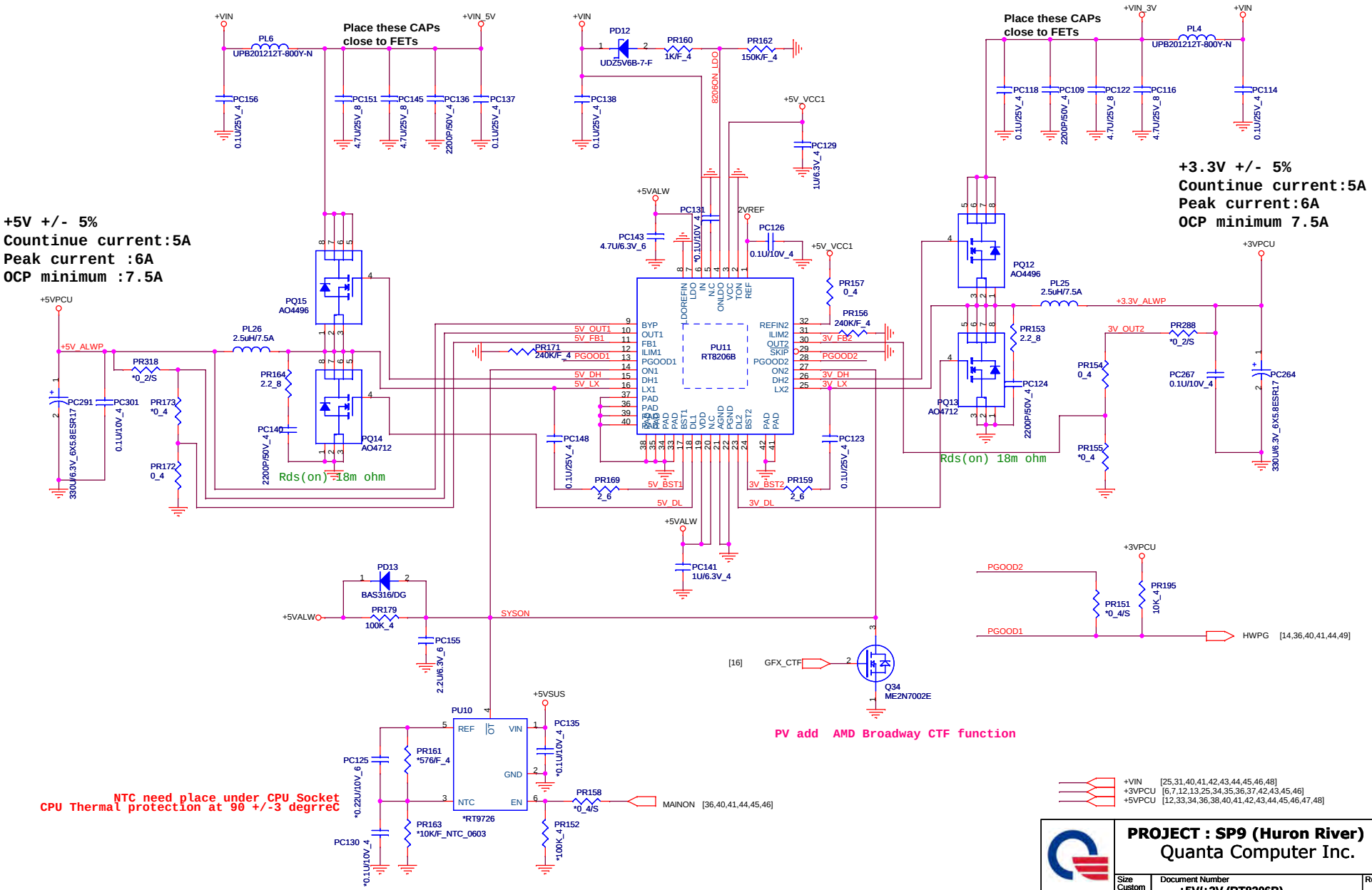


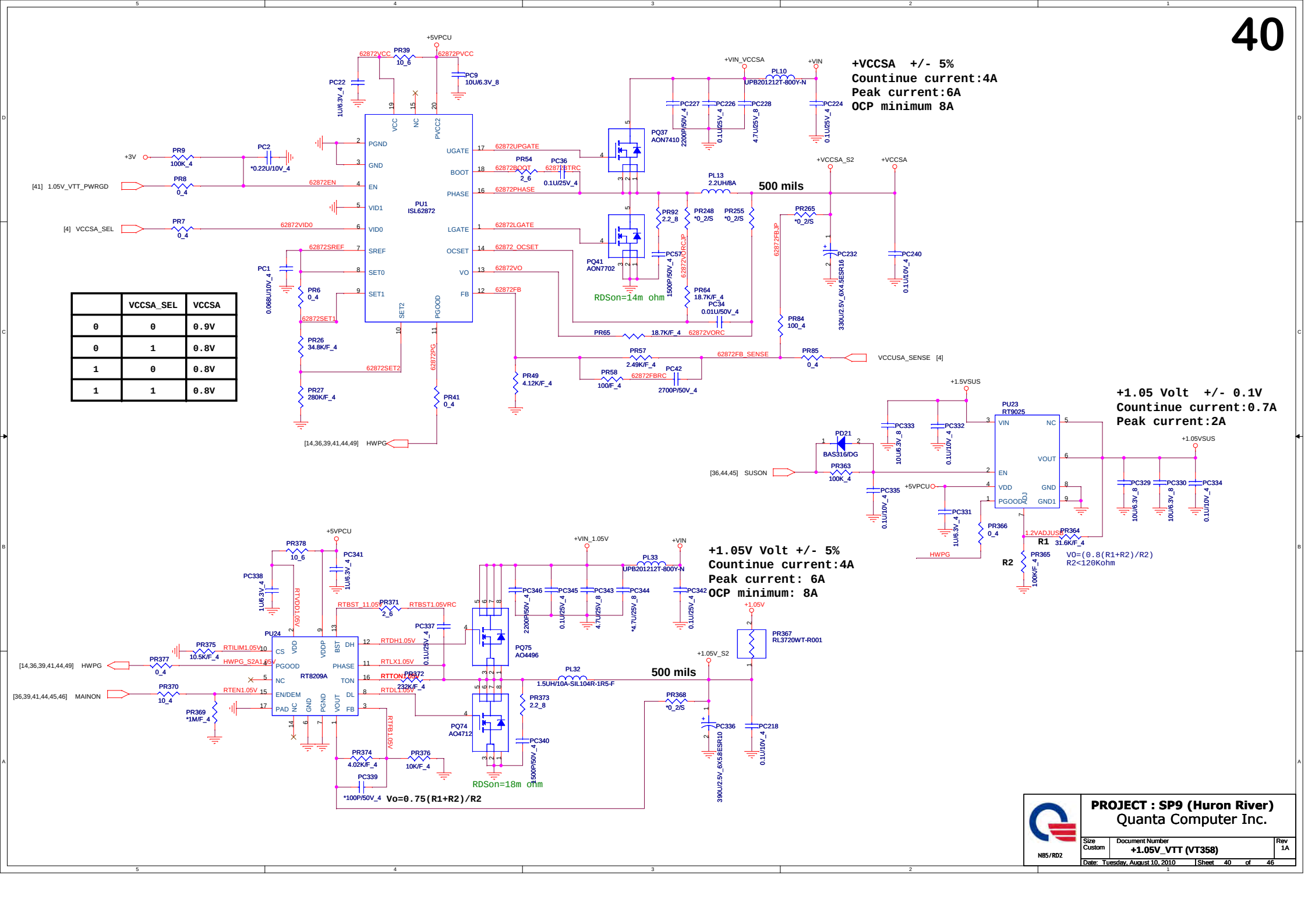

| | | |
|---|---|---|
| N85/RD2 | PROJECT : SP9 (Huron River)<br>Quanta Computer Inc. | |
| Size Custom | Document Number<br>MINI PCIE CONN X2 | Rev 1A |
| Date: Tuesday, August 10, 2010 | Sheet 37 of 49 | |


UPD720200F1-DAK-A
USB 3.0
SI for external USB 3.0 48M
MV
7/27 SI Modify
80 mils (Iout=2A)
Close USB3.0
Close to Chip
Low: Enable AC Mode
High: Disable DC Mode
DB modified 20100429
PV modify add pin 13 to GND,
change pin11 to dummy
AT25F512A or AT25F512B (Atmel)
MX25L512 (Macronix)
Clock select signal
USB3.0_CSEL
High = External 48Mhz
Low = 24MHz X'tal
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
Document Number
USB3.0
Rev 1A
Date: Tuesday, August 10, 2010
Sheet 38 of 49
N85/RD2

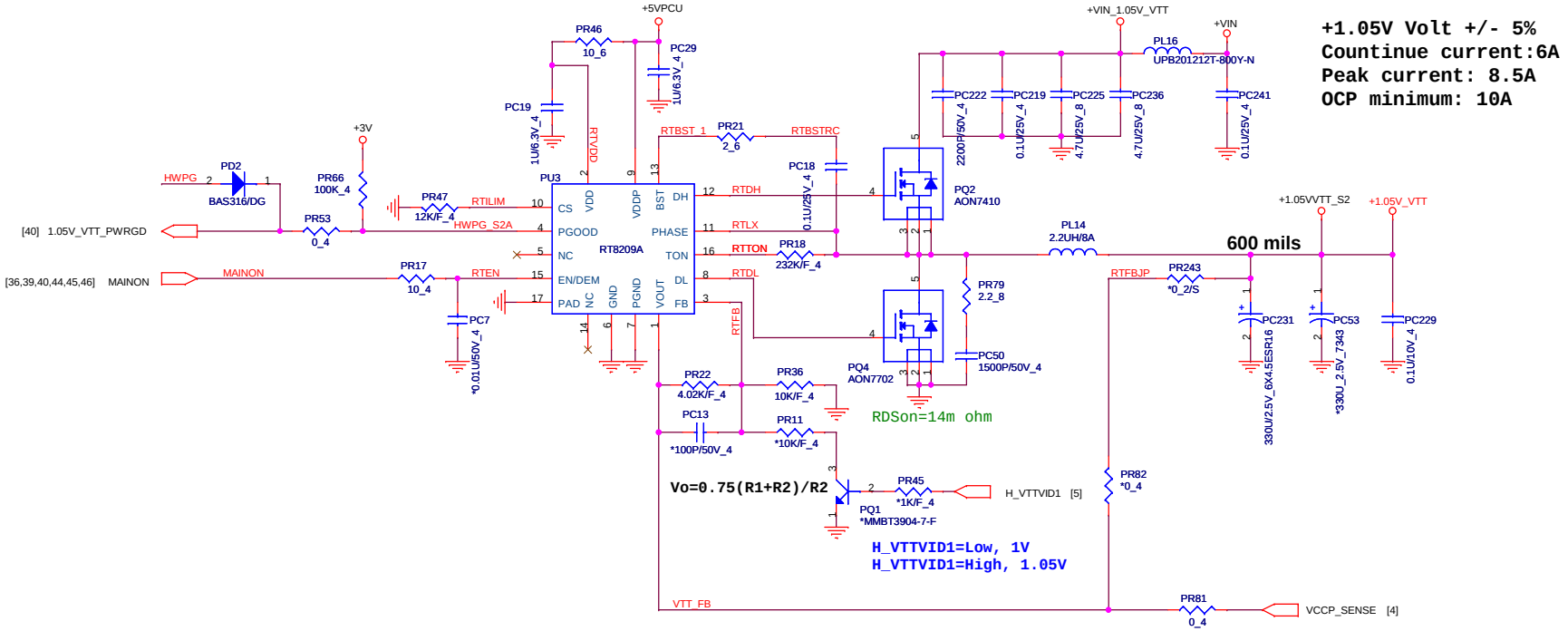
# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

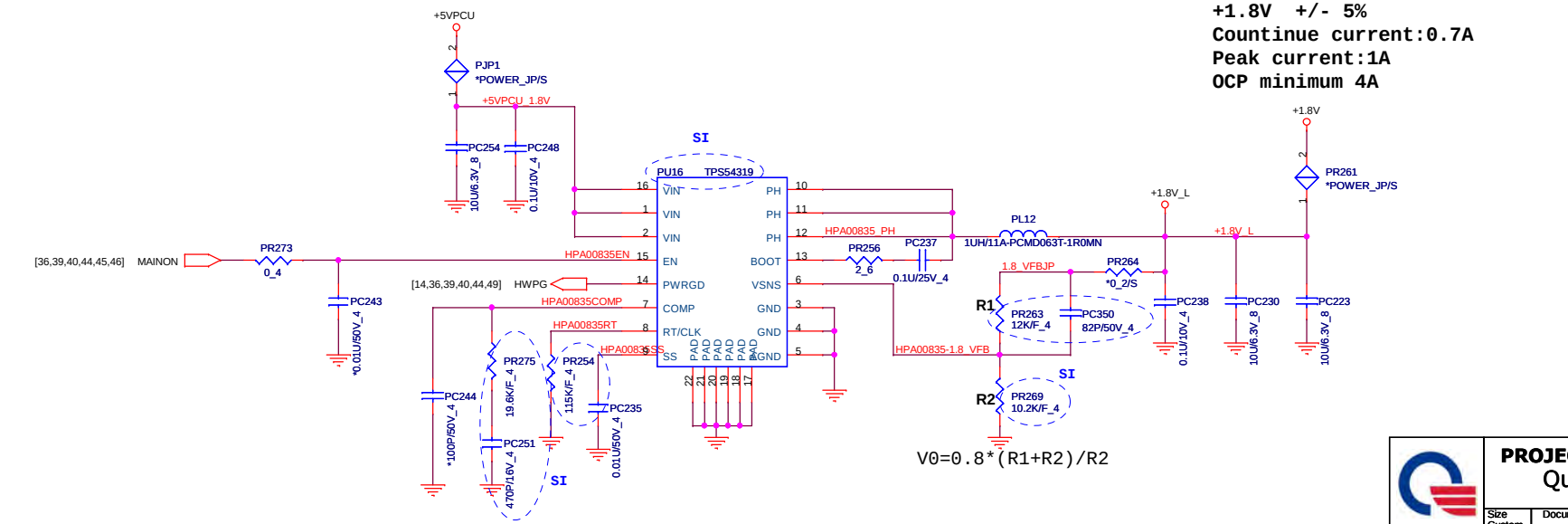




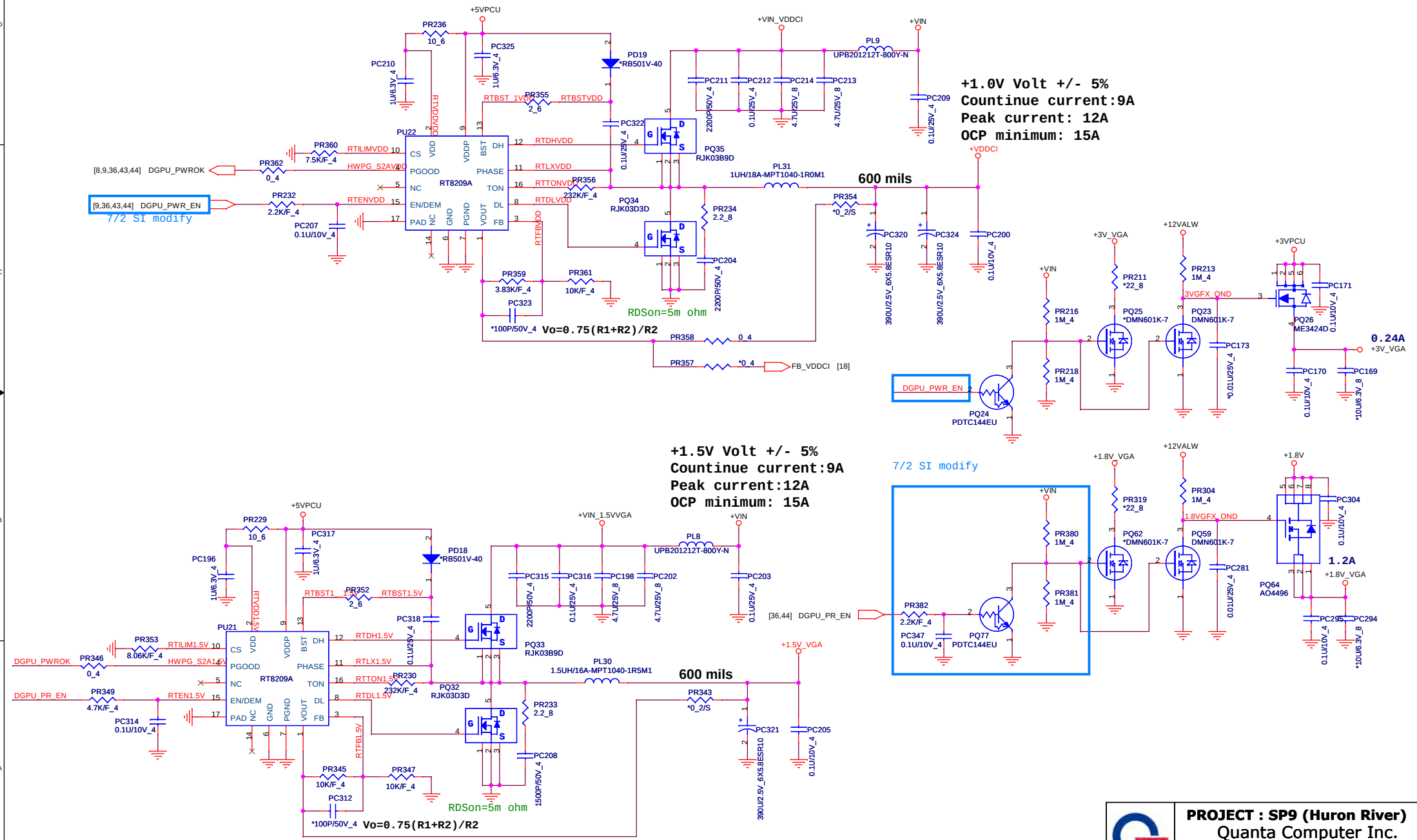



| | VCCSA_SEL | VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.8V |
| 1 | 1 | 0.8V |




| | | | |
|---|---|---|---|
| NB5/RD2 | PROJECT : SP9 (Huron River) Quanta Computer Inc. | | |
| | Size: Custom | Document Number: +1.05V/+1.8V (RT8204C) | Rev: 1A |
| | Date: Tuesday, August 10, 2010 | Sheet 41 of 46 | |


+1.0V Volt +/- 5%
Countinue current:9A
Peak current: 12A
OCP minimum: 15A
600 mils
RDSon=5m ohm
Vo=0.75(R1+R2)/R2
7/2 SI modify
0.24A
+1.5V Volt +/- 5%
Countinue current:9A
Peak current:12A
OCP minimum: 15A
600 mils
RDSon=5m ohm
Vo=0.75(R1+R2)/R2
7/2 SI modify
1.2A
RT8209A
PROJECT : SP9 (Huron River)
Quanta Computer Inc.
VGA Core/+1.8VGFX/1.0VGFX
NB5/RD2
Date: Tuesday, August 10, 2010
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Note: VID[0:5]=011000=0.95V VID[0:5]=011010=0.9V

**Granville LP Setting**

| CTRL0 | Vo |
|---|---|
| 0 | 0.95 |
| 1 | 0.9 |

**+VGACORE +/- 5%**
**Countinue current:27A**
**Peak current:45A**
**OCP minimum 50A**

**Iocset*Roc=Iocp*Rdroop**
**R23=Roc=30A*1m Ohms/10uA ~ 3K**
**Where :**
**Rdroop is AMD spec : -1 m Ohms**
**Iocp is desire over current**
**Iocset is recommendation 10uA from Rbias**

**Close to Phase 1 Inductor**
**Panasonic**
**ERT-J1VR103FA**

7/2 SI modify

Parallel

PU20 ISL6264

PR184 *1K/F_4 PR185 1K/F_4 PR197 1K/F_4 PR181 *1K/F_4 PR175 *1K/F_4 PR165 *1K/F_4
PR183 1K/F_4 PR186 *1K/F_4 PR194 *1K/F_4 PR192 1K/F_4 PR170 *1K/F_4 PR167 1K/F_4
GPU_VID5 GPU_VID4 GPU_VID3 GPU_VID2 GPU_VID1 GPU_VID0
PR379 0_4 PQ76 *ME2303T1 [16,19] GFX_CORE_CNTRL0
PR316 *10K/F_4 PR315 *0_4/S DGPU_PWROK [8,9,36,42,44]
PR168 10_6 PC149 0.1U/25V_4
PR166 10_6 PC142 1U/6.3V_4
PR190 *0_4 PR178 *0_4/S PR174 *0_4/S
PR325 1M/F_4 PR324 147K/F_4 PR182 1K/F_4 PR191 *0_4 PR300 6.8n/25V_4
PR187 0_4 PC348 *0.1U/10V_4 PR180 100K/F_4 PR327 1K/F_4 PR328 255/F_4 PR293 1000P/50V_4
PR331 97.6K/F_4 PC303 470P/50V_4 PC297 220P/50V_4
PR329 6.81K/F_4 PC296 1000P/50V_4
PC292 0.068U/10V_4 PR311 348/F_4 PC290 180P/50V_4 PR310 1K/F_4 PC289 0.22U/6.3V_4
PC299 1000P/50V_4 PC298 1000P/50V_4
PR335 0_4 PR326 0_4 PR334 10_6 PR332 10_6
VGPU_CORE_SENSE [18] VSS_GPU_SENSE [18]
PC279 4.7U/6.3V_6 PC284 0.22U/25V_6 PC278 0.22U/25V_6 PC285 0.22U/25V_6
PR307 2_6 PC280 0.22U/25V_6 PR305 2_6 PR306 2.2_8
PC305 1000P/50V_4 PR333 1.65K/F_4 PC286 0.22U/10V_4 PC287 47n/25V_4 PR308 2.7K/F_4 PR309 11K/F_4 PR303 10K_6 NTC
PR189 10K/F_6 PR196 10K/F_4 PR193 1/F_6 PR177 10K/F_6 PR314 10K/F_6 PR312 10K/F_4 PR320 1/F_6 PR323 10K/F_6
PQ58 RJK03B9D PQ63 RJK03D3D PQ60 RJK03B9D PQ61 RJK03D3D
PC146 PC153 PC152 PC147 PC288 PC127 PC144 PC132 PC128 PC150 PC283
PR330 2.2_8 PC302 1500P/50V_4 PR306 2.2_8 PC282 1500P/50V_4
PR321 *0_4/S PR322 *0_4/S PR313 *0_4/S PR317 *0_4/S
PL5 UPB201212T-800Y-N PL27 0.36uH PL28 0.36uH
PC134 330U_2.5V_7343 PC139 330U_2.5V_7343 PC154 330U_2.5V_7343 PC133 330U_2.5V_7343
+VIN_VGA +VIN +VGPU_CORE +3VPCU +5VPCU +3VSUS +VIN

| | |
|---|---|
| PROJECT : SP9 (Huron River) | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: GPU CORE(ISL6264) |
| Rev: 1A | |
| Date: Tuesday, August 10, 2010 | Sheet 43 of 46 |
| NB5/RD2 | |

**+1.5V +/- 5%**
**Countinue current:6A**
**Peak current:12A**
**OCP minimum 15A**

( VTT/2A )
+0.75V_DDR_VTT
PC104 10U/6.3V_8
PC105 10U/6.3V_8
+1.5VSUS_1
PR144 0_4
PR141 *0_4
DDRMODE
( 3mA )
[4,12,13] DDR_VTTREF
PC120 0.033U/10V_4

PU9
RT8207AGQW
1 VTTGND
2 VTTSNS
3 GND
4 MODE
5 VTTREF
6 COMP
7 NC
8 VDDQSNS
9 VDDQSET
10 S3
11 S5
12 NC
25 GND
24 VTT
23 VLDOIN
22 1116VBST
21 1116DRVH
20 1116LL
19 1116DRVL
18 PGND
17 CS_GND
16 1116CS
15 V5IN
14 V5FILT
13 PGOOD

+1.5VSUS
PC102 *10U/6.3V_8
PR137 2_6
PC108 0.1U/25V_4
1116VDDQSET
PR142 7.5K/F_4
+5VPCU
PC117 1U/6.3V_4
PR146 10_6
PC119 1U/6.3V_4
[36,40,45] SUSON
PR147 619K/F_4
1116TONSET
+VIN
HWPG
HWPG [14,36,39,40,41,49]

+VIN_DDR
+VIN
PL3 UPB201212T-800Y-N
PC88 0.1U/25V_4
PC89 4.7U/25V_8
PC90 4.7U/25V_8
PC87 2200P/50V_4
PC83 0.1U/25V_4

PQ57 RJK03B9D
PQ51 RJK03D3D
PL22 1UH/18A-MPT1040-1R0M1
PR279 2.2_8
PC258 1500P/50V_4
51116FBJP
PR281 *0_2/S
+1.5VSUS_1
+1.5VSUS
PC259 390U/2.5V_6X5.8ESR10
PC256 0.1U/10V_4
PR149 10K/F_4
PR148 10K/F_4

need to stuff for S3 and PR263 change to 100K

[36,39,40,41,45,46] MAINON
PD11 RB501V-40
PR150 100K_4
PC121 0.1U/10V_4

**+1.0V +/- 5%**
**Countinue current:1.7A**
**Peak current:3A**

8/3 SI modify
+1.5VSUS
PC206 10U/6.3V_8
PC199 0.1U/10V_4
PR235 10K/F_4
[9,36] DGPU_PWR_EN
+5VPCU
PC201 0.1U/10V_4
PC197 1U/6.3V_4
[36,42,43] DGPU_PR_EN
[8,9,36,42,43] DGPU_PWROK
PR231 0_4

PU14 RT9025
3 VIN
2 EN
4 VDD
1 PGOOD
5 NC
6 VOUT
8 GND
9 GND1
7 ADJ

+1.0V_VGA
PC194 10U/6.3V_8
PC195 10U/6.3V_8
PC193 0.1U/10V_4
1.2VADJ_1.0V
PR227 26.7K/F_4 /SI
R1
R2
PR228 100K/F_4
VO=(0.8(R1+R2)/R2)
R2<120Kohm

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number DDR3 (RT8207)
Rev 1A
Date: Tuesday, August 10, 2010
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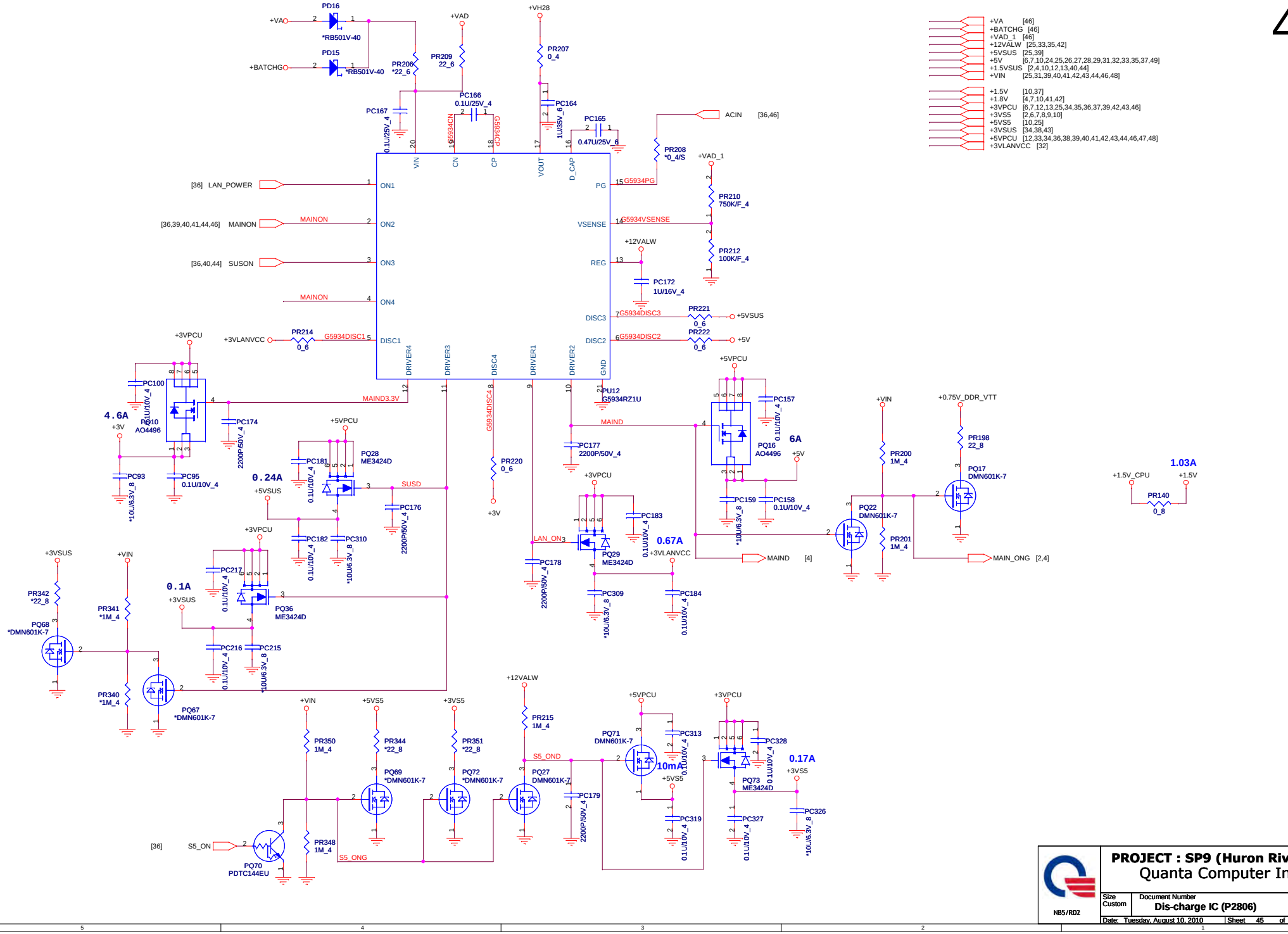



| | |
|---|---|
| PROJECT : SP9 (Huron River) | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: Dis-charge IC (P2806) |
| Rev: 1A | |
| NB5/RD2 | Date: Tuesday, August 10, 2010 |
| Sheet 45 of 46 | |

TOP DC_JACK
65W/90W

7/18: SI modify

For EMI test only no stuff

Do Not add test pad on BATDIS_G signal

CN13 DC-IN CONN

PL20 UPB201212T-800Y-N

PL19 UPB201212T-800Y-N

PC80 0.1U/25V_4

PC85 1000P/50V_4

PC253 0.1U/25V_4

PQ48 FDMC4435BZ

EC1 *10U/25V_8

PD17 P4SMAJ20A

PC265 0.1U/25V_4

PC266 0.1U/50V_6

PQ56 P0603BDG

PC82 0.22U/25V_8

PR267 RC2512-R010

PD20 P4SMA220A

PQ40 P1003EVG

PL15 UPB201212T-800Y-N

PL17 UPB201212T-800Y-N

PC46 0.1U/25V_4

PC245 0.1U/25V_4

CN12

PR63 330_4

PR62 330_4

PR61 10K/F_4

PR60 1K/F_4

200045MR008G10JZR
DFHD08MR095
bat-bp02083-b85b5-9h-8p-l-v

PC33 0.01U/25V_4

PC163 0.01U/25V_4

Place this cap close to EC

PD4 UDZ5V6B-7-F

PD3 UDZ5V6B-7-F

PC24 *100P/50V_4

PC23 *100P/50V_4

PL11 UPB201212T-800Y-N

PC38 0.1U/25V_4

PC52 4.7U/25V_8

PC59 *4.7U/25V_8

PC66 *0.1U/50V_4

PC70 0.1U/25V_4

PR129 100_4

PQ8 DMN601K-7

PR132 100K_4

PR133 100K_4

PR199 *100K_4

PQ20 MMBT3904-7-F

PR130 *0_4/S

PD14 BAS316/DG

PR202 1M_4

PC160 1U/6.3V_4

PR134 220K_4

PR136 220K_4

PQ11 MMDT2907A

PR139 1M_4

PR138 1K_6

PR135 1M_4

PR274 *0_2/S

PR260 *0_2/S

PR42 10/F_4

PR37 10/F_4

PC3 1U/10V_4

PR73 100_4

PC20 2.2U/6.3V_6

PR67 2_6

PC37 0.1U/50V_6

PC39 1U/10V_4

PD6 RB501V-40

PQ38 AON7410

PQ39 AON7702

PL18 PCMC063T-6R8MN

PR242 2.2_8

PC221 1500P/50V_4

PC246 4.7U/25V_8

PC242 4.7U/25V_8

PC255 4.7U/25V_8

PC257 4.7U/25V_8

PC250 4.7U/25V_8

PR250 0.02/F_1206

PR252 *0_2/S

PR246 *0_2/S

PC43 0.1U/25V_4

PD7 RB501V-40

PR93 220K_6

PR1 10/F_4

PR10 10/F_4

PC6 1U/6.3V_4

PC12 0.01U/50V_4

PC4 0.01U/50V_4

PC162 0.01U/50V_4

PR205 10/F_4

PC5 0.47U/10V_4

PR12 0_4

PC30 1U/25V_8

PR74 10_8

PR43 *0_4/S

PR50 *0_4/S

PR28 100K_4

PR29 100K_4

PD1 BAS316/DG

PD5 BAS316/DG

PD8 BAS316/DG

PD9 BAS316/DG

PR33 75K/F_4

PC161 0.1U/10V_4

PR32 12.4K/F_4

Place this cap close to EC

PQ3 IMD2

PU2 OZ8681

PQ7 PDTC144EU

PQ9 PDTC144EU

PC99 1000P/50V_4

PC84 *0.1U/25V_4

PR131 10K_6

PR127 10K_6

PR97 1K_6

PQ5 MMDT2907A

PR98 220K_4

PR96 220K_4

PR99 1M_4

PR117 1M_4

PQ6 PDTC144EU

PR125 0_4

PD10 *BAS316/DG

PC81 *10U/6.3V_8

MV

+VA [45]
+VAD_1 [45]
+VH28 [45]
+BATCHG [45]
+5VPCU [12,33,34,36,38,39,40,41,42,43,44,45,47,48]

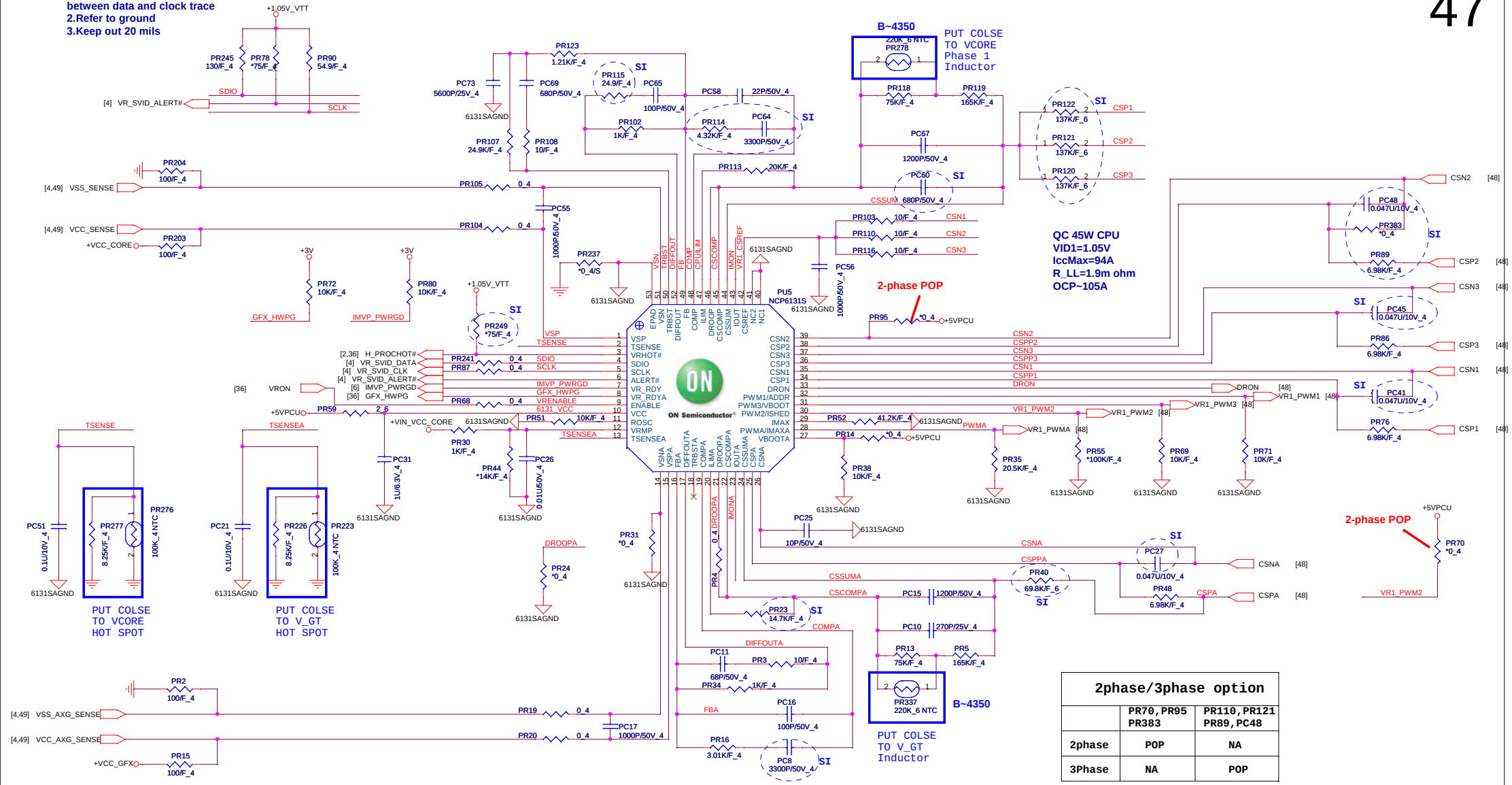
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Charger (BQ24704) | 1A |

N85/RD2

Date: Tuesday, August 10, 2010 Sheet 46 of 46

1.Alert trace routing
between data and clock trace
2.Refer to ground
3.Keep out 20 mils




| 2phase/3phase option | | | |
|---|---|---|---|
| | PR70,PR95 PR383 | PR110,PR121 PR89,PC48 |
| 2phase | POP | NA |
| 3Phase | NA | POP |

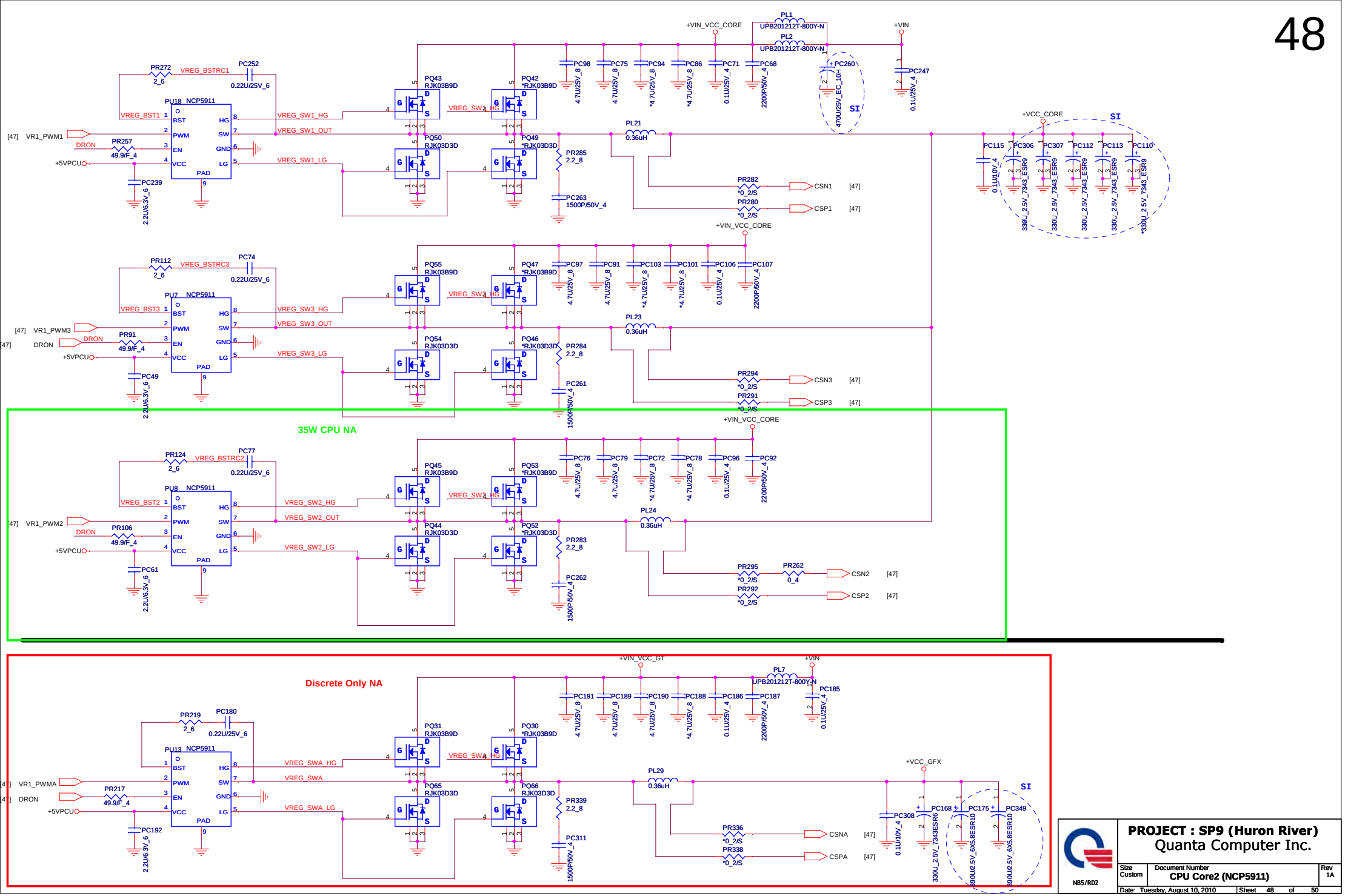
| UMA(Switchable)/Discrete Only option | | | |
|---|---|---|---|
| | PC336,PC340 PC343,PC337 PC342 | PR427,PR433,PR430,PR431,PR423,PR435 PC338,PR424,PR428,PR432,PC339,PC341 PR425,PR426,PR429,PR420,PR422,PR380 PR399,PR421,PC352,PR417,PR418,PC354 PC419 | PR434,PR436 PR378 |
| UMA | POP | POP | NA |
| Discrete | Change to 0 ohm | NA | POP |

**PROJECT : SP9 (Huron River)**
Quanta Computer Inc.

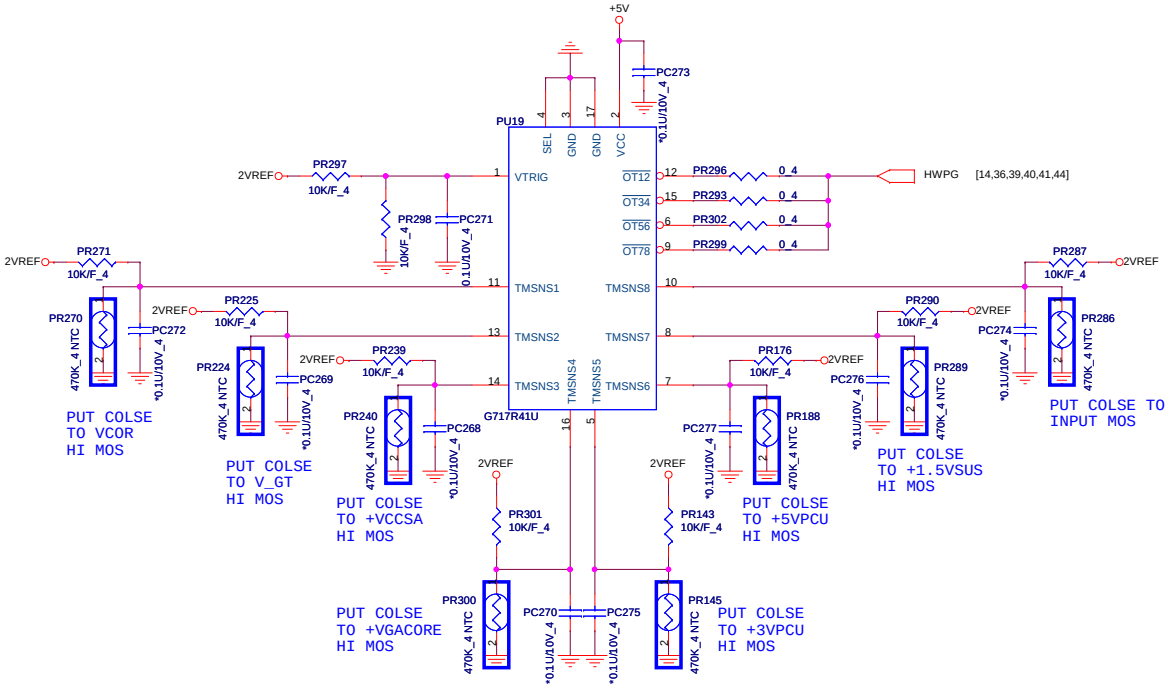
| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU Core1 (NCP6131S) | 1A |

N85/RD2

Date: Tuesday, August 10, 2010 Sheet 47 of 46




| | | | |
|---|---|---|---|
| PROJECT : SP9 (Huron River) Quanta Computer Inc. | | | |
| Size: Custom | Document Number: CPU Core2 (NCP5911) | | Rev: 1A |
| N85/RD2 | Date: Tuesday, August 10, 2010 | Sheet 48 of 50 | |




| Vender | Size | P/N |
|---|---|---|
| EON | 128KB | |
| | 512KB | AKE37ZN0Q01 (EN25F40-100HIP) |
| Winbond | 128KB | AKE35FN0N00 (W25X10BVSNIG) |
| | 512KB | AKE37FN0N01 (W25X40BVSSIG) |
| Socket | | DG008000031 |

| | | |
|---|---|---|
| NB5/RD2 | PROJECT : SP9 (Huron River)<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: IMON | Rev: 1A |
| Date: Tuesday, August 10, 2010 | Sheet 49 of 47 | |