MODEL NAME : *DDP00*
DDB00

PCB NO : *LA-G341P*

BOM P/N :

Dell/Compal Confidential

Schematic Document
Superveloce
(Berlinetta CFL 4-Phase Design)

2018-05-10

Rev: Pilot A00

@ : Nopop Component
XDP@ : Nopop Component
CONN@ : Connector Component
TPM@ : TPM funct i on
EMC@ : Pop of EMI parts
VRAMS@ : Samsung GDDR5
VRAMM@ : Micron GDDR5
G0VRAMH@: Samsung GDDR5 for G0-GPU
NDS@@ : Nopop Component
N18PQ1@ : GPU N18PQ1
N18PQ3@ : GPU N18PQ3
N17PG0@ : GPU N17PG0
N17PG1@ : GPU N17PG1
UMA@ : UMA
DIS@ : DIS
UMAP@ : UMA for Presist i on
UMAX@ : UMA for XPS
3PHASEPCB@ : PCB for 3Phase
4PHASEPCB@ : PCB for 4Phase
3PHASE@ : PCB for 3Phase
4PHASE@ : PCB for 4Phase
VPRO@ : For VPRO SKU
NVPRO@ : For No-VPRO SKU

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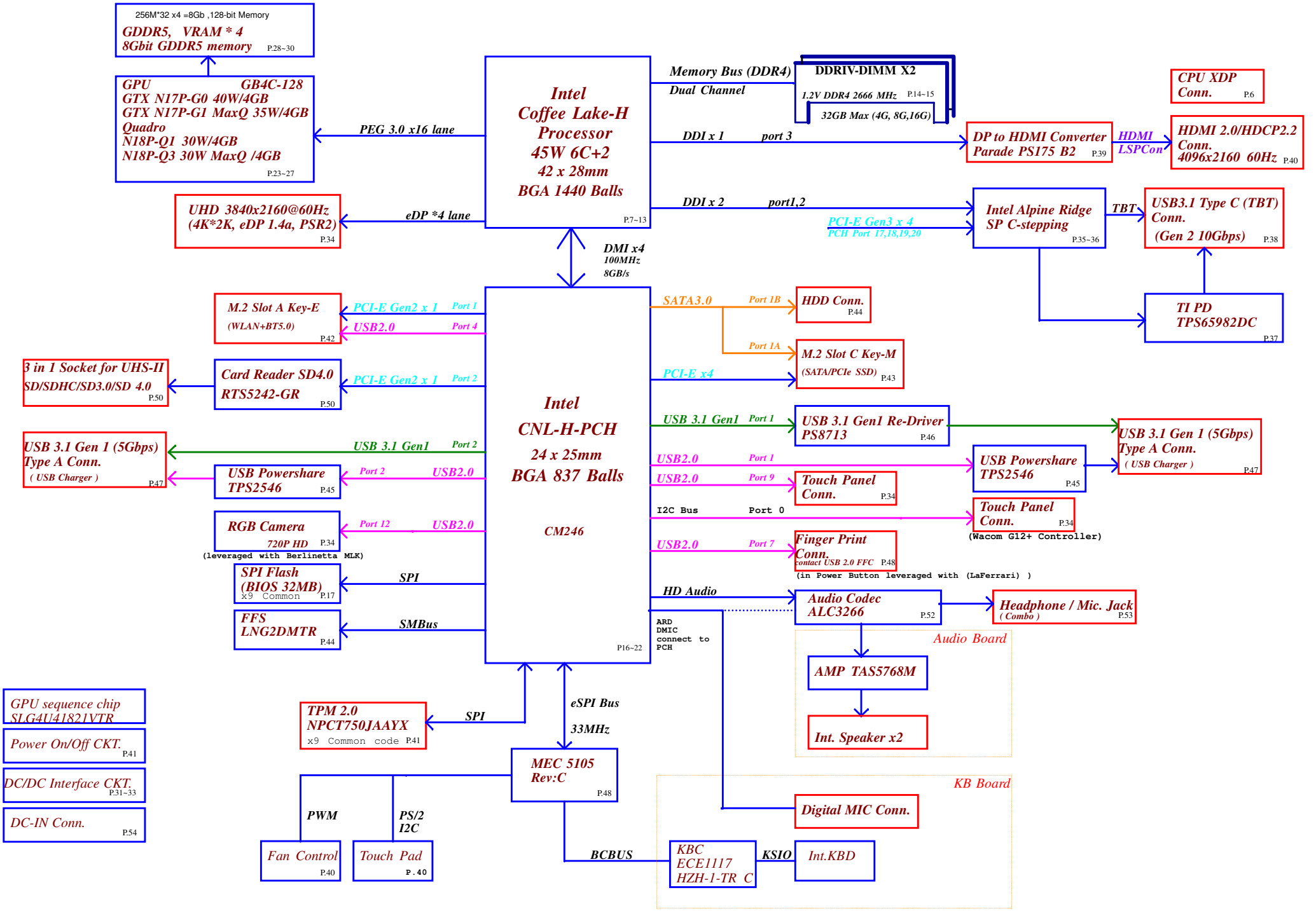
Title: *P01-Cover Page*

Size | Document Number: *LA-G341P* | Rev: 1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 1 of 76



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Issued Date	2017/06/21	Deciphered Date	2027/06/21

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Title: P02-Block Diagram

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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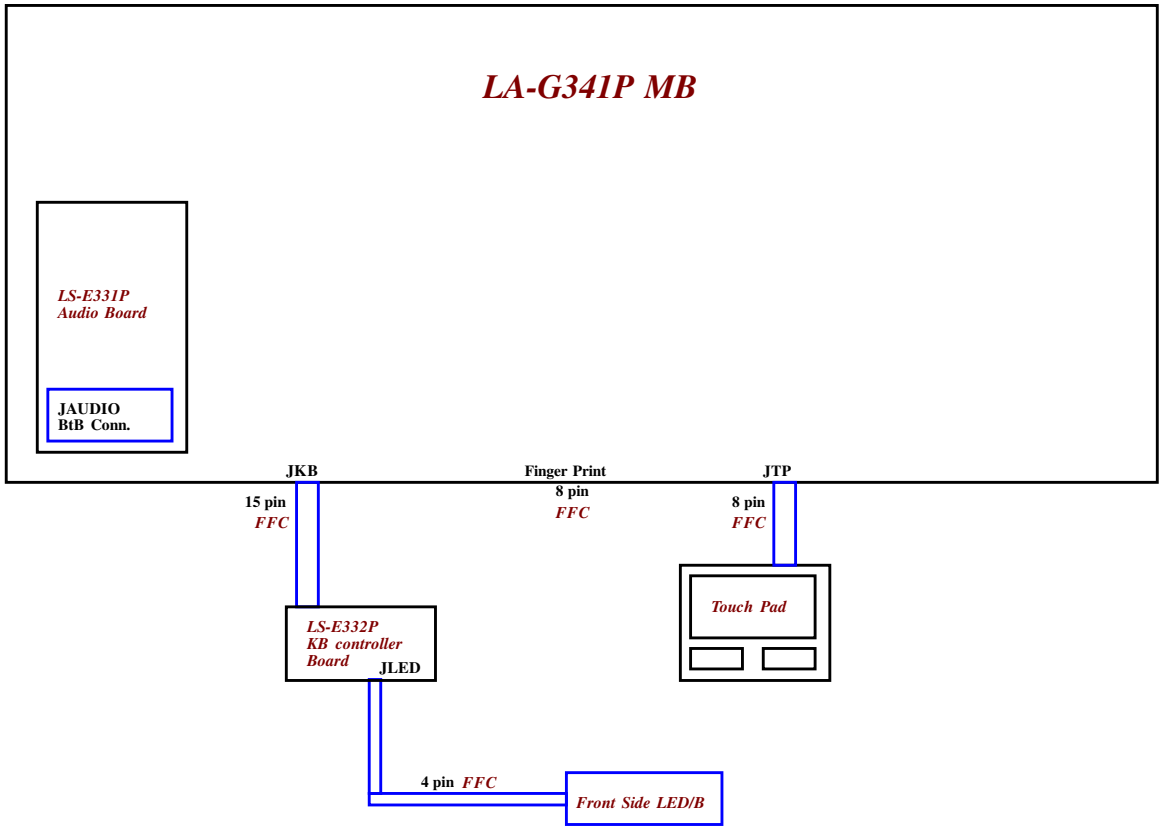
Project Code : DDP00 / DDB00
File Name :



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Title: **P03-Daughter/B block diagram**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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Board ID	Resistor
X00	4.3K
X01	2K
X02	
X03	
A00	1K

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	Touch Screen
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION
Lane 1	NGFF-1 WLAN + BT
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	CARD READER
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	None
Lane 16	None
Lane 17	Alpine Ridge
Lane 18	
Lane 19	
Lane 20	

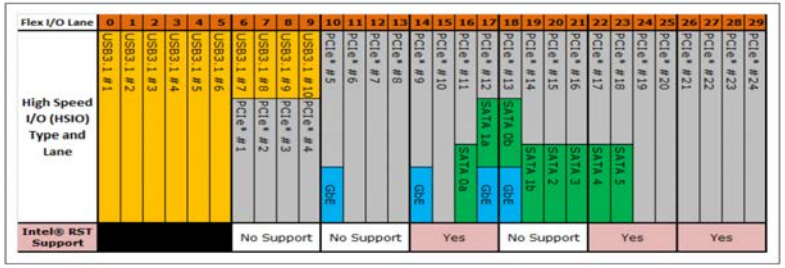
USB3.0	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	N/A
1A	SSD
0B	N/A
1B	N/A
2	HDD
3	N/A
4	N/A
5	N/A

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 Intel® Optane™ Memory Device
– See the " PCI Express* (PCIe*) " chapter for the PCH PCIe* Controllers, configuration, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: P04-Notes List

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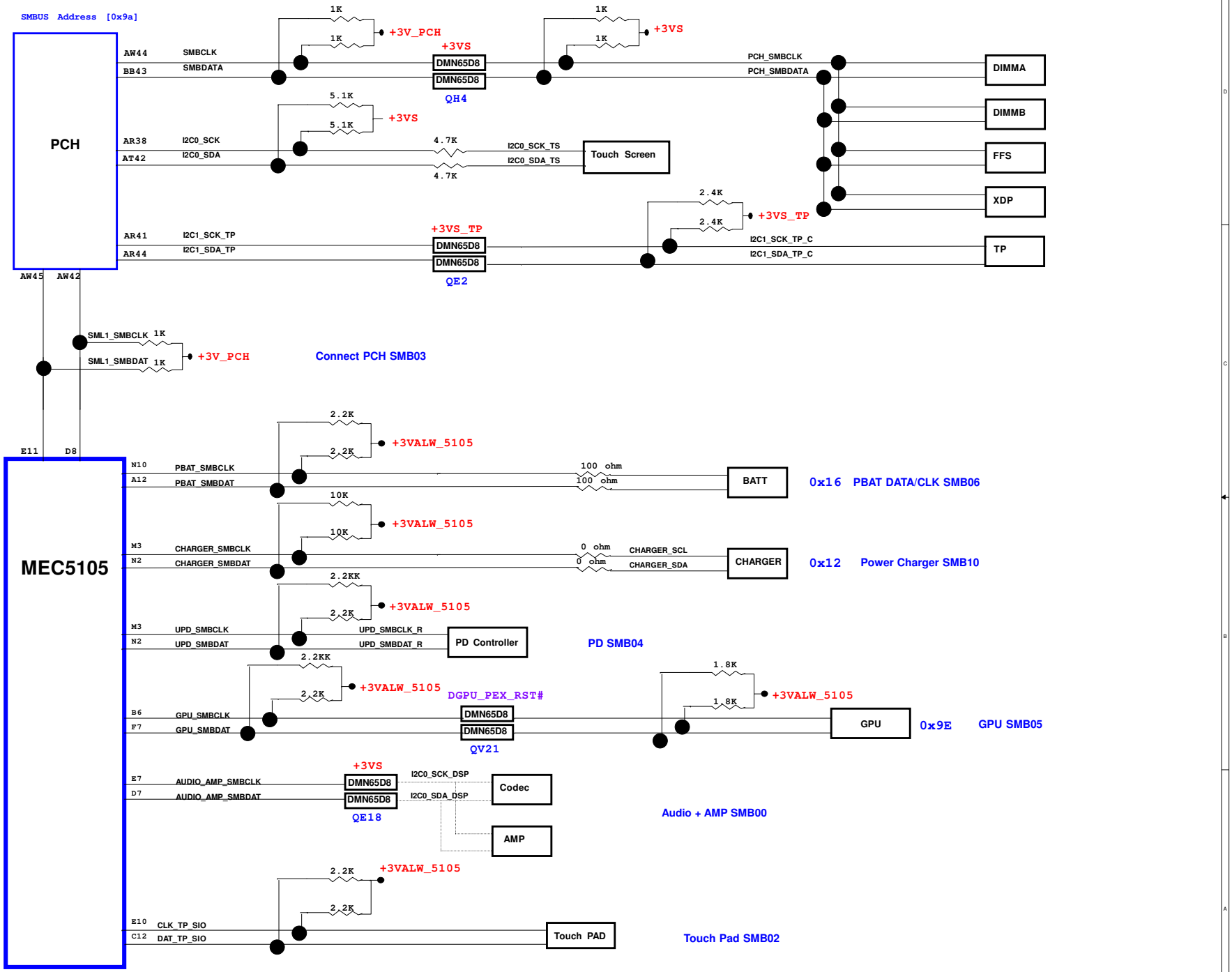

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Title: P05-SMBus block diagram

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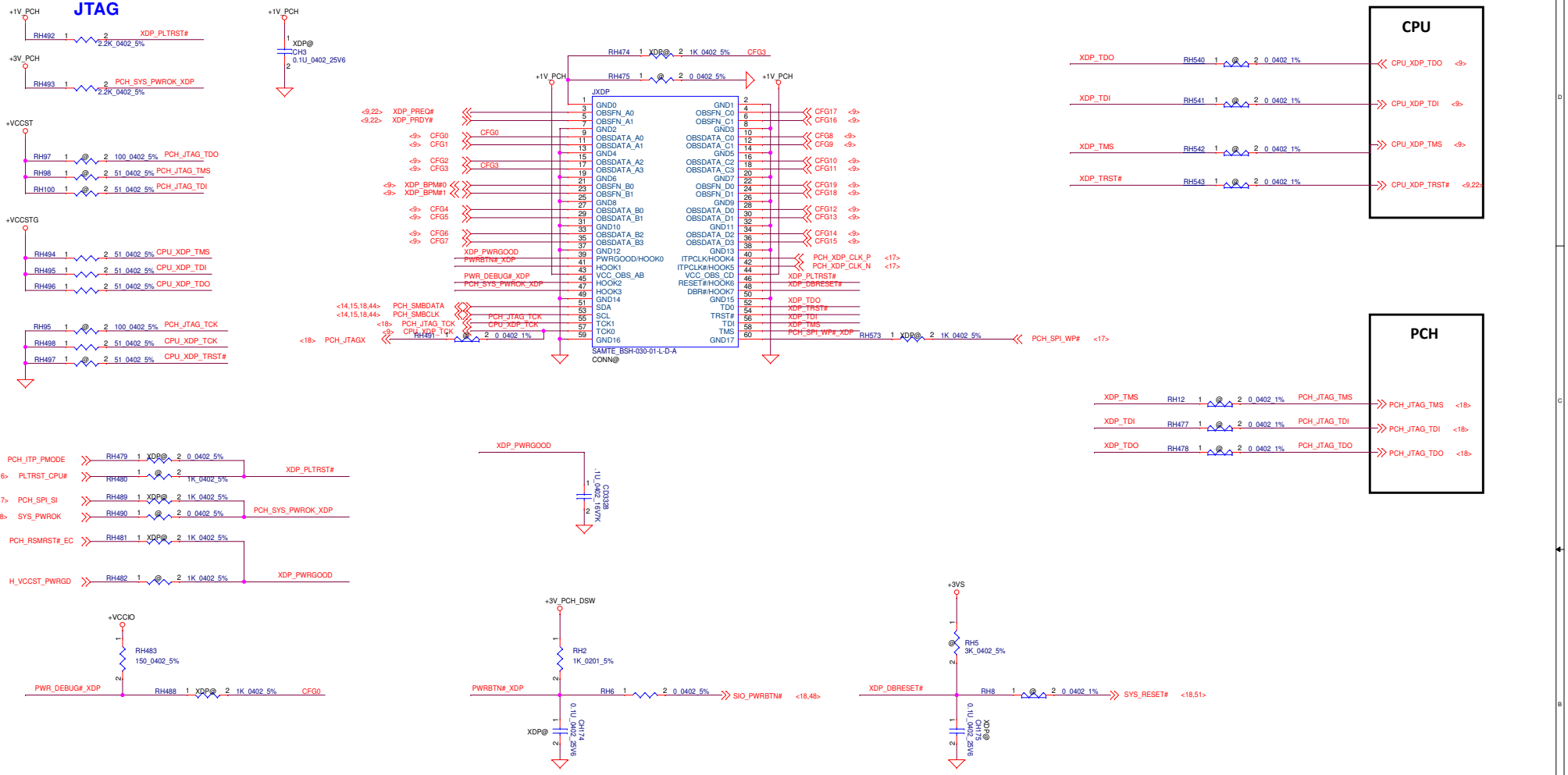

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Title: **P06-XDP CONN**

Size	Document Number	Rev
		1.0(A00)

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Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

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Title: P07-CPU(1/7) DMI,PEG,DDI,EDP

Size	Document Number	Rev
C		1.0(A00)

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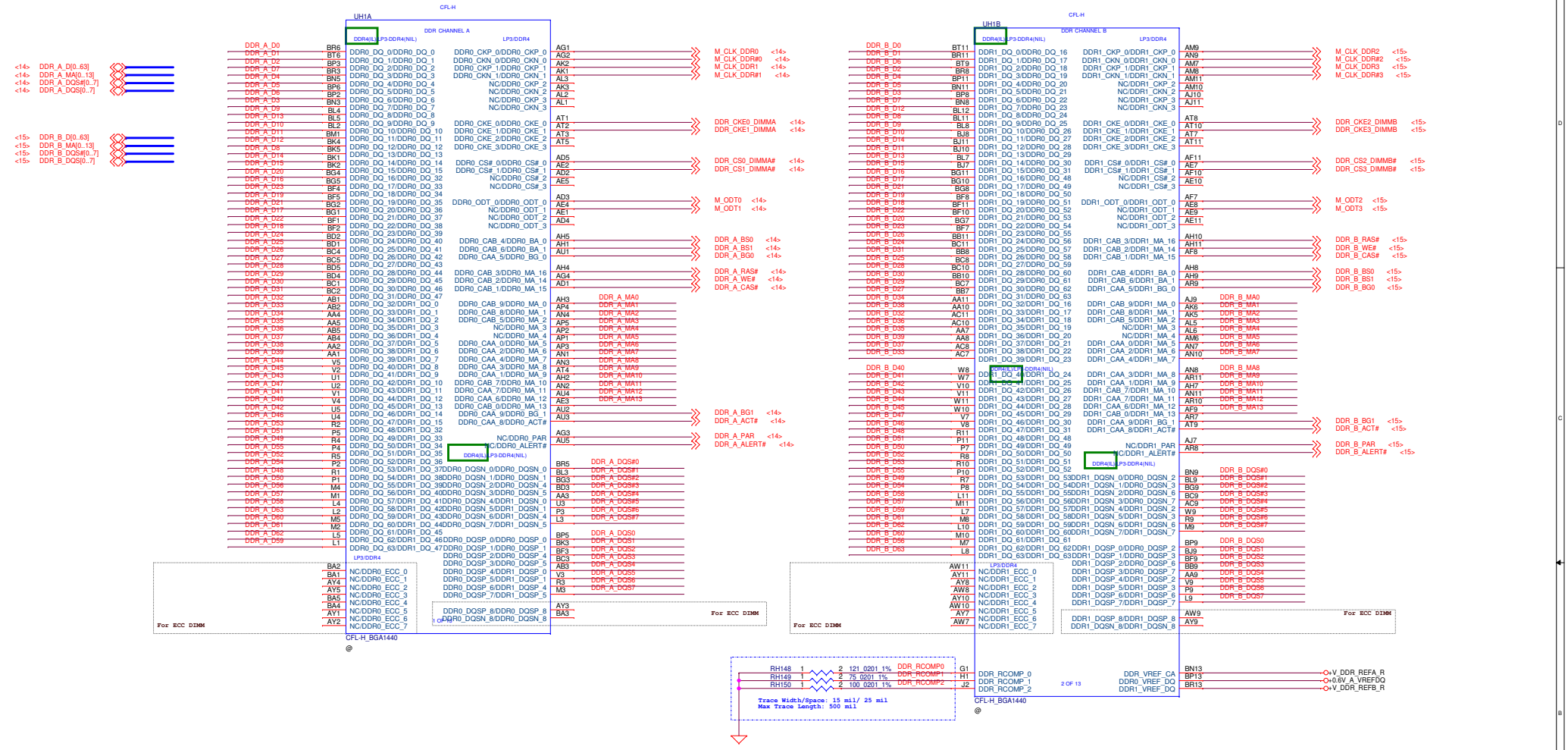
Interleave



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Title: **P08-CPU(2/7) DDR4**

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CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

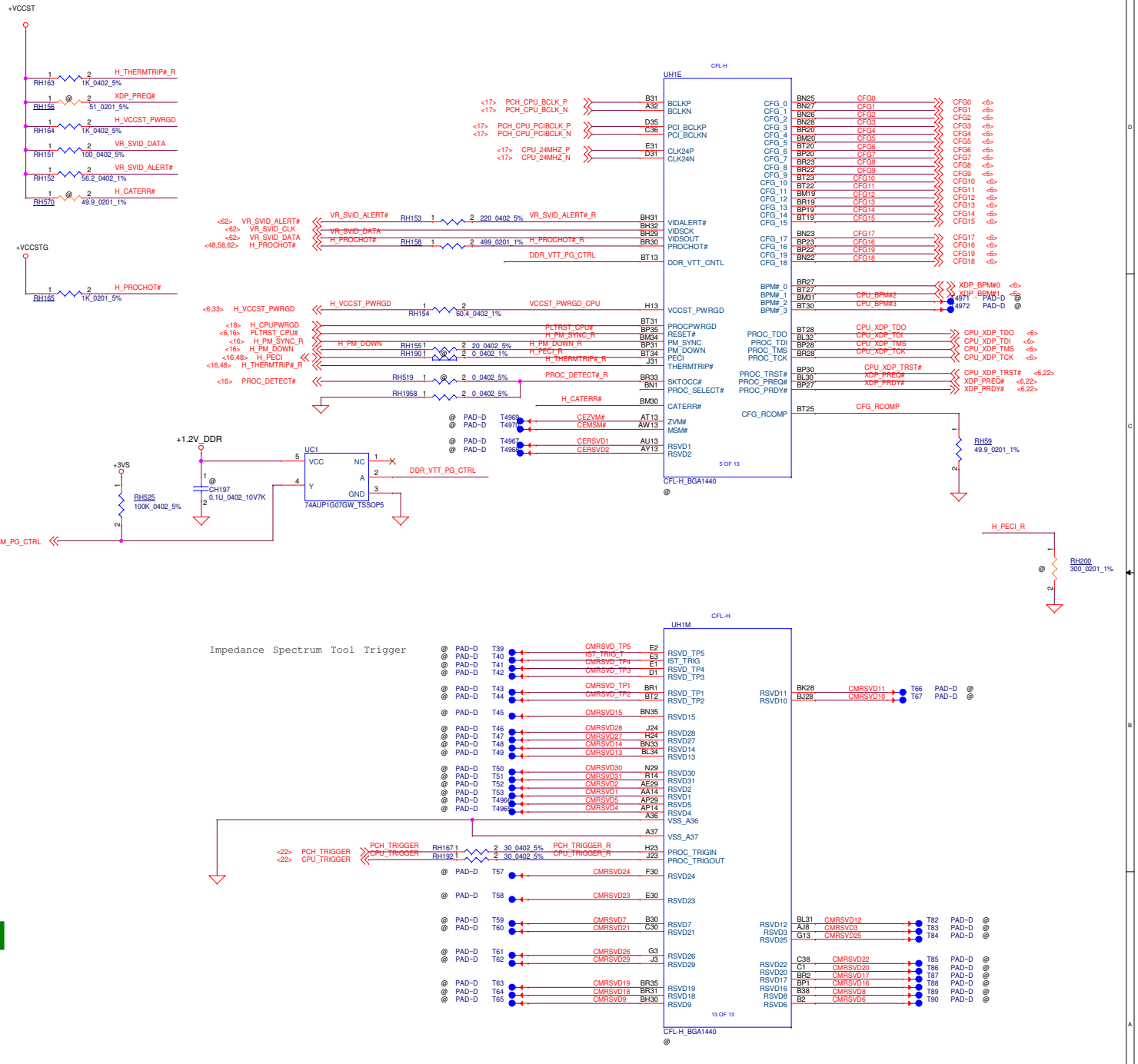
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width 0:1:0	0:1:1	0:1:2	CFG Signals CFG [6]	CFG [5]	CFG [2]	Lanes 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lanes device should use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
4. for reversal lanes, for example:
   When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
5. For Basin Falls platform use 1x8+2x4 Bifurcation



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Title: P09-CPU(3/7) RSVD,CFG,XDP

Size	Document Number	Rev
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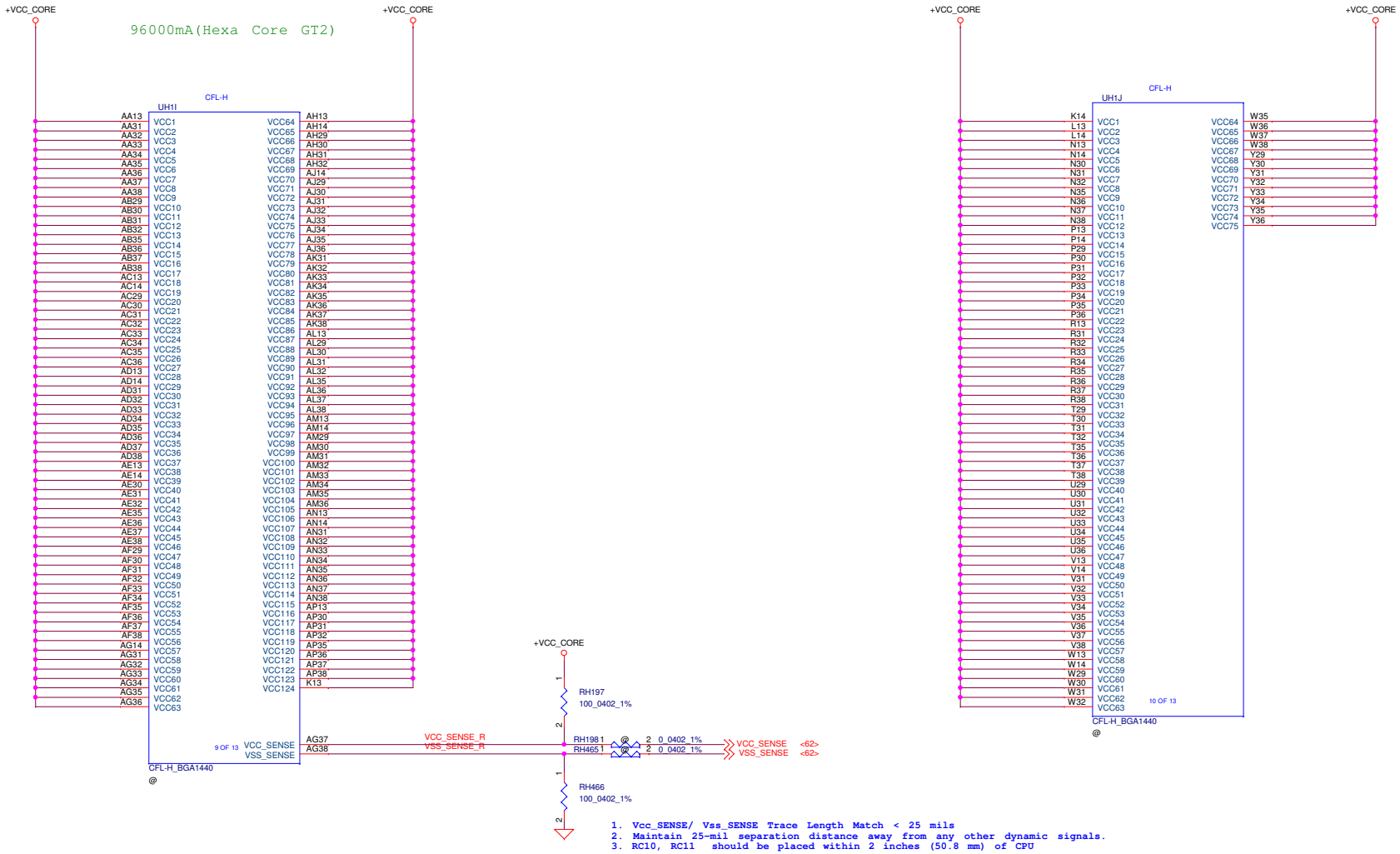

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Title: *P10-CPU(4/7) PWR,VCore,RSVD*

Size	Document Number	Rev
Custom		1.0(A00)

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570805_CFL_EDS_Vol1_Rev0.7
+VCC_SA
Max: 11100mA

+VCCSA

570805_CFL_EDS_Vol1_Rev0.7
+VCC_IO
Max: 6400mA

+VCCIO

570805_CFL_EDS_Vol1_Rev0.7
+1.2V_VDDQ_CPU
Max: 3300mA

VDDQ_DDR

@ PJP1604
PAD-OPEN 3x3m

+1.2V_DDR

571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.05VS_VCCSTG: 1uF * 1

+VCCSTG

1U_0402_6.3V6K CH105
1U_0402_6.3V6K CH106

+VCCST

10U_0402_6.3V6M CH107
10U_0402_6.3V6M CH108
1U_0402_6.3V6K CH109
10U_0402_6.3V6M CH110

Board Edge cap

A00_4P_0524 : Material shortage issue
EE remove 2pcs SE00000Z H00 and power add 5pcs SE00001CA00

+VCCSA

22U_0603_6.3V6M CH134
22U_0603_6.3V6M CH135
47U_0805_4V4M CH136
47U_0805_4V4M CH137

10U_0402_6.3V6M CH111
10U_0402_6.3V6M CH112
10U_0402_6.3V6M CH113
10U_0402_6.3V6M CH114
10U_0402_6.3V6M CH115
10U_0402_6.3V6M CH116
10U_0402_6.3V6M CH117
1U_0201_6.3V6M CH133

CFL-H
UH1L

J30	VCCSA1	VDDQ1	AA6
K29	VCCSA2	VDDQ2	AE12
K30	VCCSA3	VDDQ3	AF5
K31	VCCSA4	VDDQ4	AF6
K32	VCCSA5	VDDQ5	AG5
K33	VCCSA6	VDDQ6	AG9
K34	VCCSA7	VDDQ7	AJ12
K35	VCCSA8	VDDQ8	AL11
L31	VCCSA9	VDDQ9	AP6
L32	VCCSA10	VDDQ10	AP7
L35	VCCSA11	VDDQ11	AR12
L36	VCCSA12	VDDQ12	AR6
L37	VCCSA13	VDDQ13	AT12
L38	VCCSA14	VDDQ14	AW6
M29	VCCSA15	VDDQ15	AY6
M30	VCCSA16	VDDQ16	J5
M31	VCCSA17	VDDQ17	J6
M32	VCCSA18	VDDQ18	K12
M33	VCCSA19	VDDQ19	K6
M34	VCCSA20	VDDQ20	L12
M35	VCCSA21	VDDQ21	L6
M36	VCCSA22	VDDQ22	R6
		VDDQ23	T6
		VDDQ24	W6
		VDDQ25	Y12
AG12	VCCIO1		
G15	VCCIO2		
G17	VCCIO3		
G19	VCCIO4	VCCPLL_OC1	BH13
G21	VCCIO5	VCCPLL_OC2	BJ13
H15	VCCIO6	VCCPLL_OC3	G11
H16	VCCIO7		
H17	VCCIO8	VCCST	H30
H19	VCCIO9		
H20	VCCIO10	VCCSTG2	H29
H21	VCCIO11		G30
H26	VCCIO12	VCCSTG1	
H27	VCCIO13		H28
J15	VCCIO14	VCCPLL1	J28
J16	VCCIO15	VCCPLL2	
J17	VCCIO16		
J19	VCCIO17		M38
J20	VCCIO18	VCCSA_SENSE	M37
J21	VCCIO19	VSSSA_SENSE	
J26	VCCIO20		H14
J27	VCCIO21	VCCIO_SENSE	J14
		12 OF 13 VSSIO_SENSE	

CFL-H_BGA1440
@

570805_CFL_EDS_Vol1_Rev0.7
+1.2V_VCCPLL_OC
Max: 130mA

+1.2V_VCCPLL_OC

RH530 1 @ 2 0_0402_5%

+1.2V_DDR

+VCCST
Max: 60mA

+VCCSTG
Max: 20mA

+VCCST
Max: 150mA

VCCSA_SENSE_R
VSSSA_SENSE_R

RH201 1 2 100_0402_1%
RH202 1 @ 2 0_0402_1%
RH470 1 @ 2 0_0402_1%
RH469 1 2 100_0402_1%

+VCCSA
VCCSA_SENSE <62>
VSSSA_SENSE <62>

VCCIO_SENSE <73>
VSSIO_SENSE <73>

+1.2V_VCCPLL_OC

CH3332 1U_0201_6.3V6M
CH3333 1U_0201_6.3V6M

+VCCST

CH3334 4.7U_0402_6.3V6M

close CPU ball H28,J28

close CPU ball

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC15, RC16 should be placed within 2 inches (50.8 mm) of CPU

Backside cap

+VCCIO

10U_0402_6.3V6M CH126
10U_0402_6.3V6M CH103
10U_0402_6.3V6M CH104

Backside cap

VDDQ_DDR

22U_0603_6.3V6M CH129
22U_0603_6.3V6M CH130
22U_0603_6.3V6M CH131
22U_0603_6.3V6M CH132

VDDQ_DDR

10U_0402_6.3V6M CH118
10U_0402_6.3V6M CH121
10U_0402_6.3V6M CH124
10U_0402_6.3V6M CH120
10U_0402_6.3V6M CH119
10U_0402_6.3V6M CH122
10U_0402_6.3V6M CH123
10U_0402_6.3V6M CH125
10U_0402_6.3V6M CH106
10U_0402_6.3V6M CH127
10U_0402_6.3V6M CH128

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Title: P11-CPU(5/7) PWR,VDDR,VSA,VIO

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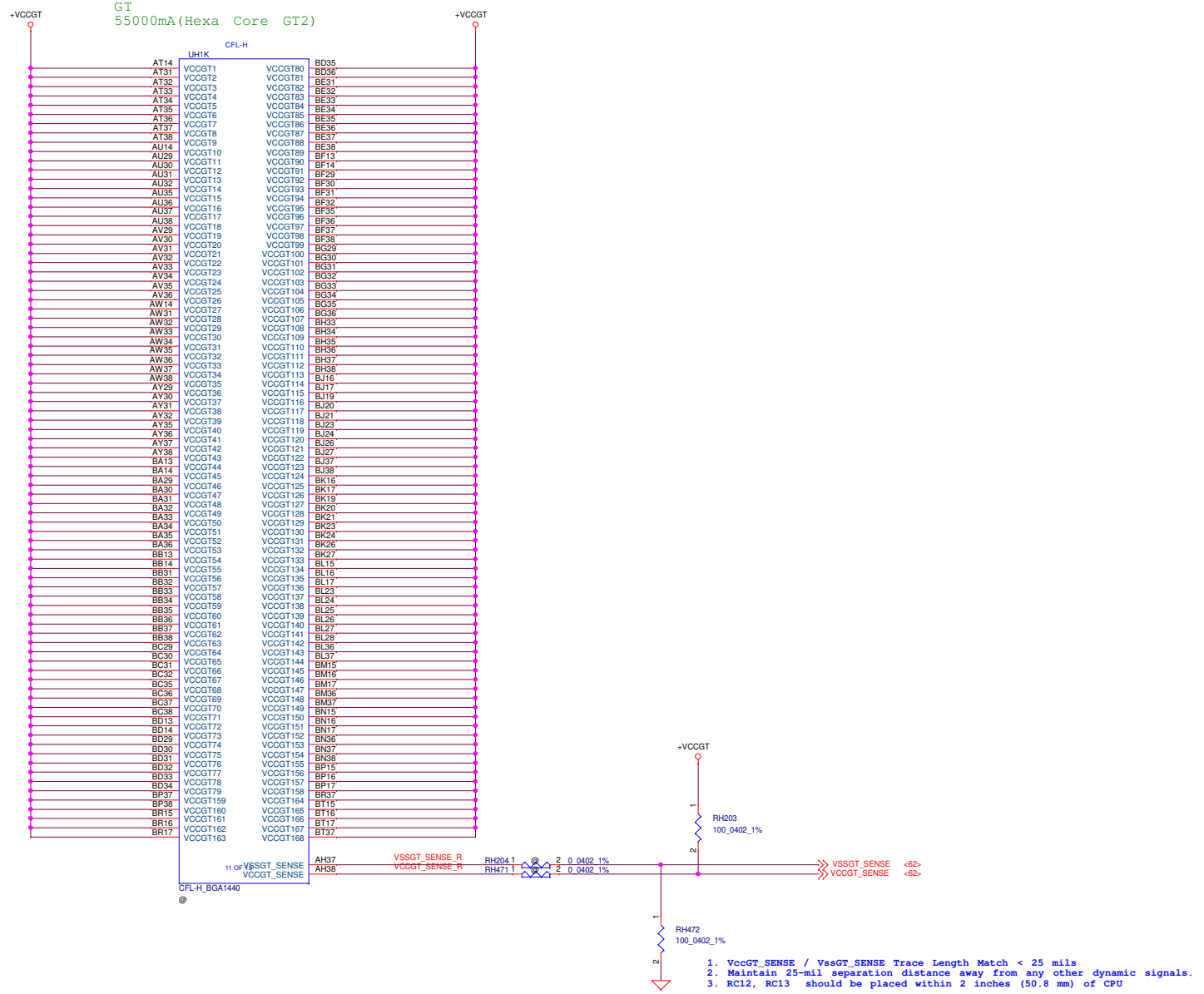

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Title	P12-CPU(6/7) PWR,VGT		
Size Custom	Document Number		Rev 1.0(A00)
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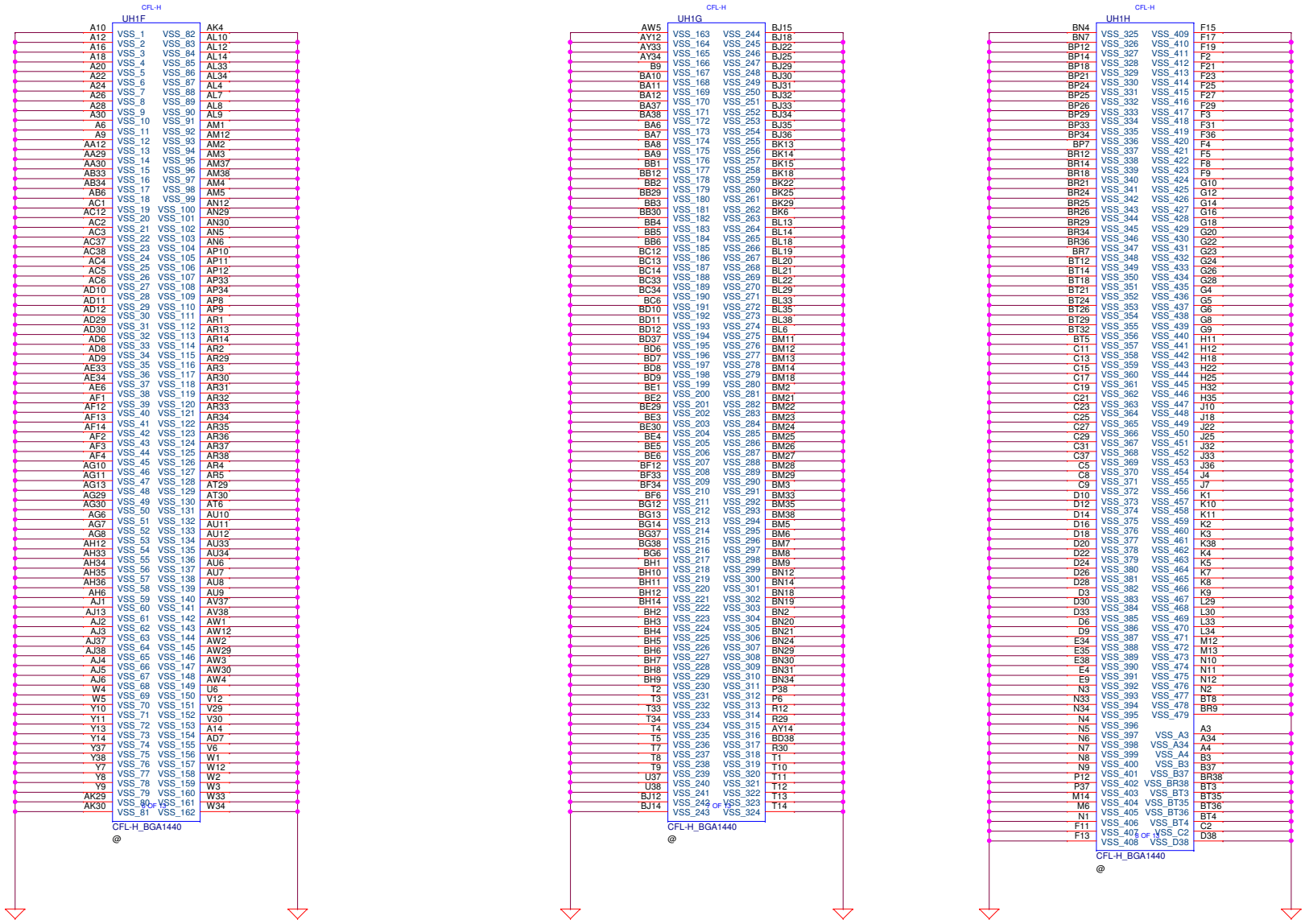

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: P13-CPU(7/7) VSS

Size	Document Number	Rev
Custom		1.0(A00)

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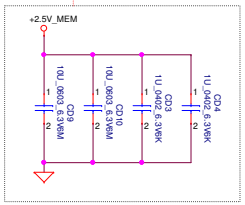
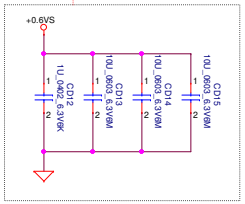
Layout Note:
Place near JDIMM1.257,259

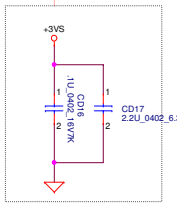
Layout Note:
Place near JDIMM1.258

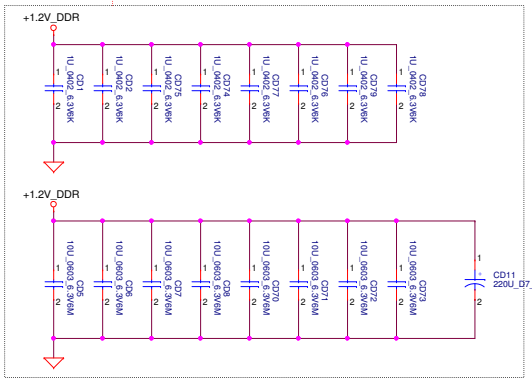
Layout Note:
Place near JDIMM1.255

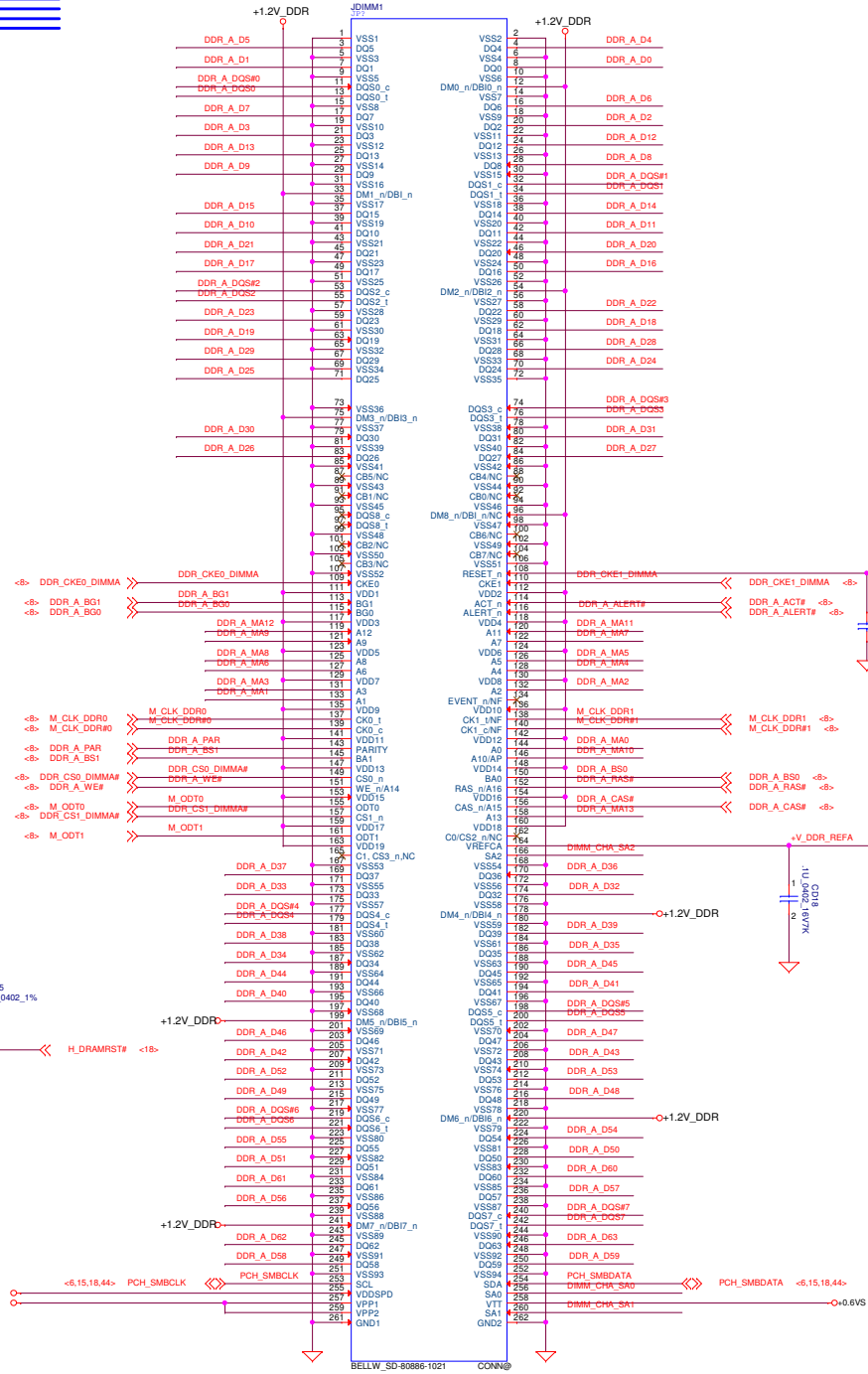
Layout Note:
Place near JDIMM1



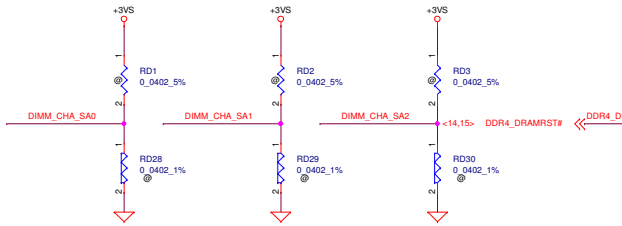




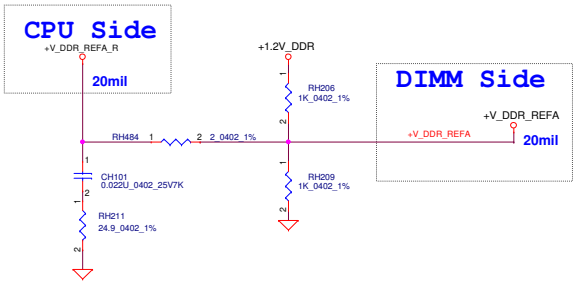




All VREF traces should have 10 mil trace width



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



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Title: P14-DDR4 DIMMA

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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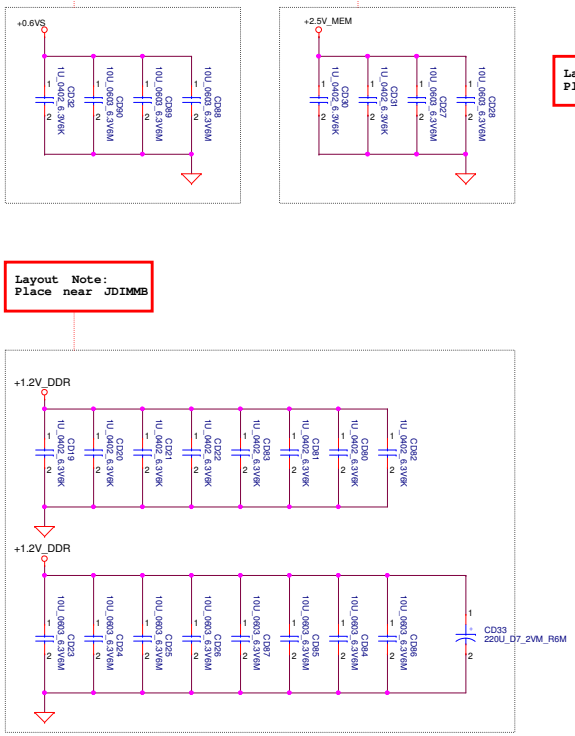
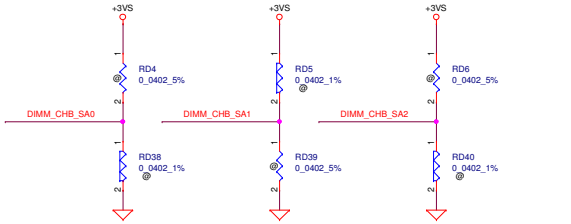
Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM2.257,259

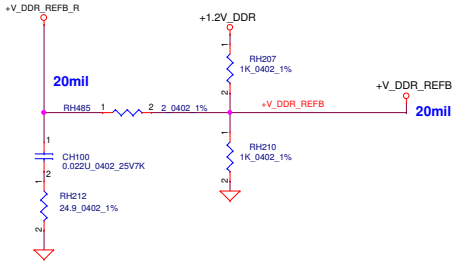
Layout Note:
Place near JDIMM2.255

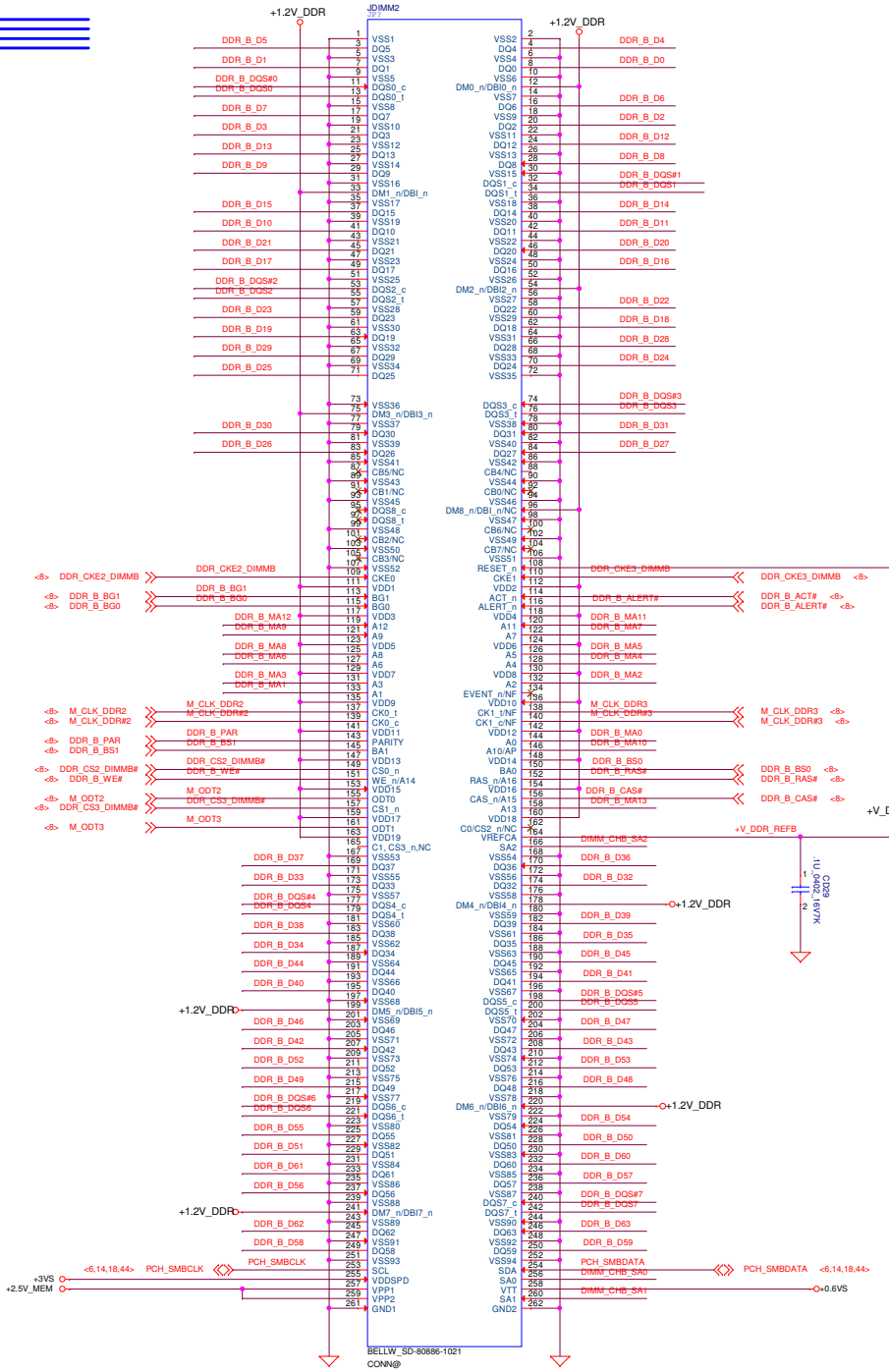
Layout Note:
Place near JDIMMB





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals





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Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P15-DDR4 DIMMB**

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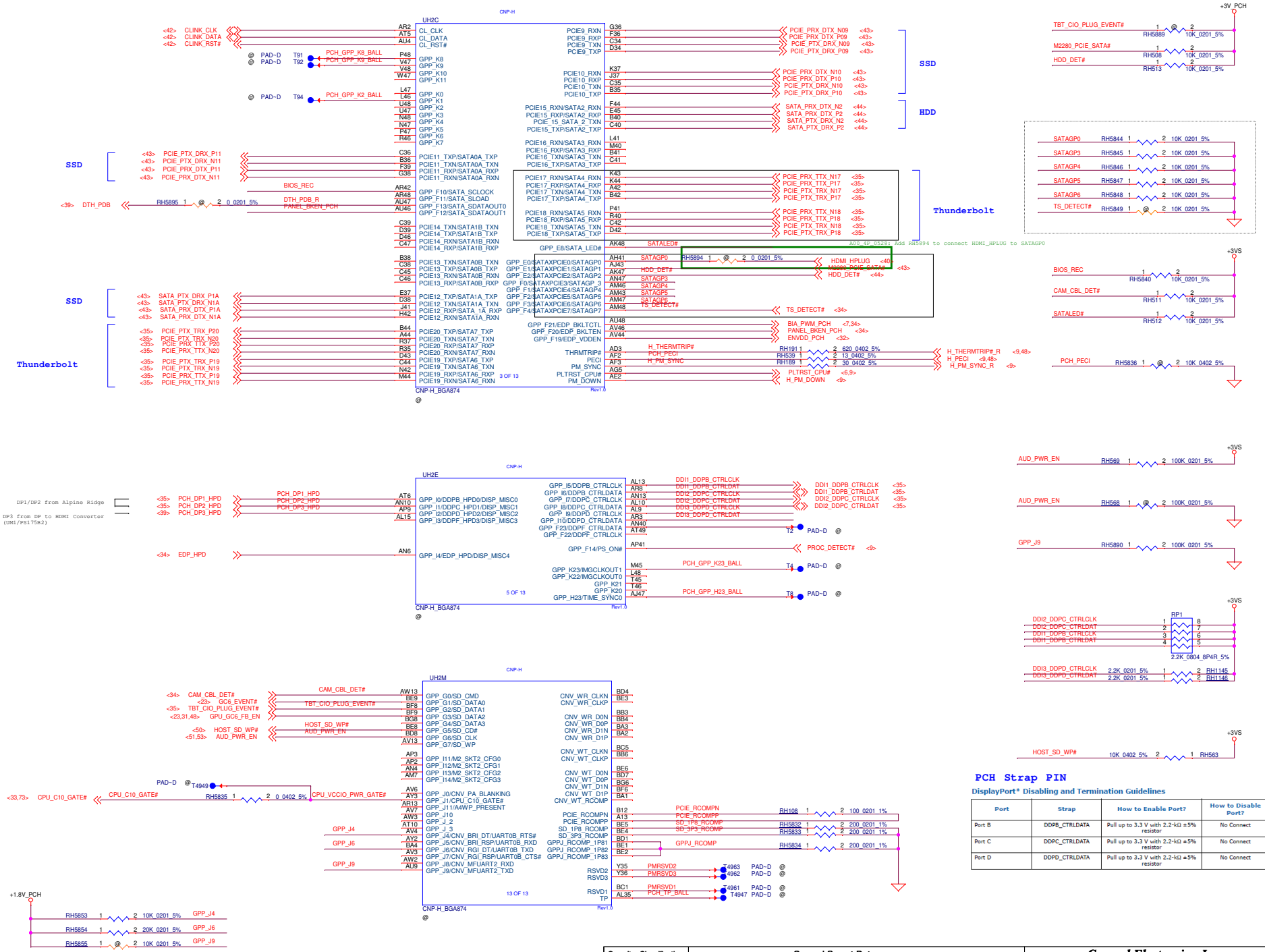

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Issued Date	2017/06/21	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

Title: P16-PCH (1/7) SATA,DDC,PCIE,CNV

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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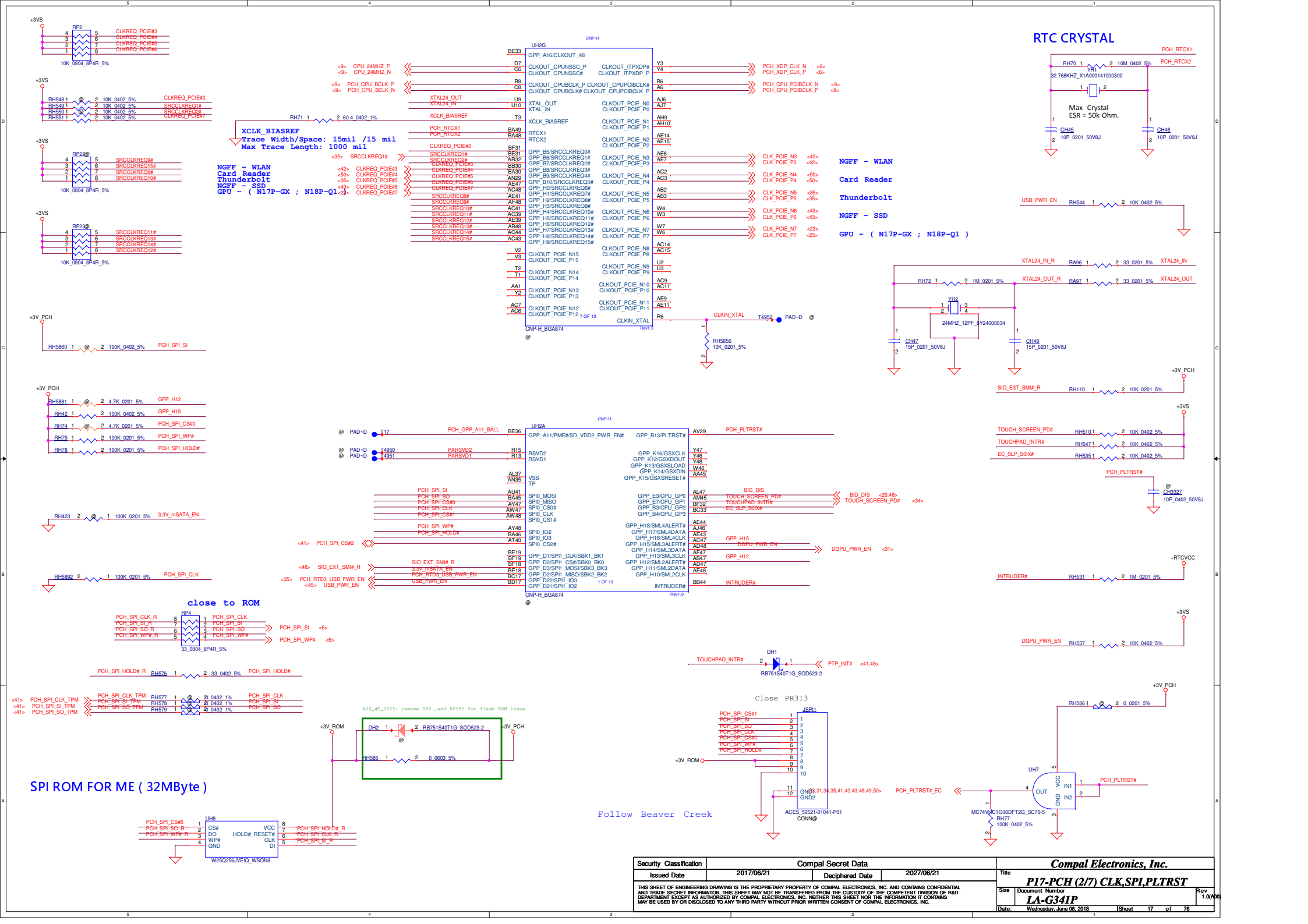

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P17-PCH (2/7) CLK,SPI,PLTRST

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HDA_SDO / I2S0_TXD

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
1=Disable ME Protect (ME can be updated) 0=Enable ME Protect (ME cannot be updated)

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default positi on)

Close to PCH

Close to BOT

PCH to DDR, XDP, FFS

Top Swap Override (internal PD)

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

TLS CONFIDENTIALITY

HIGH	vPRO
LOW(DEFAULT)	non-vPRO

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

PCHHOT# (IntelR DCI-OOB)

HIGH	Enable
LOW(DEFAULT)	Disable

Reserve for EMI

Reserve for RF please close to UH1

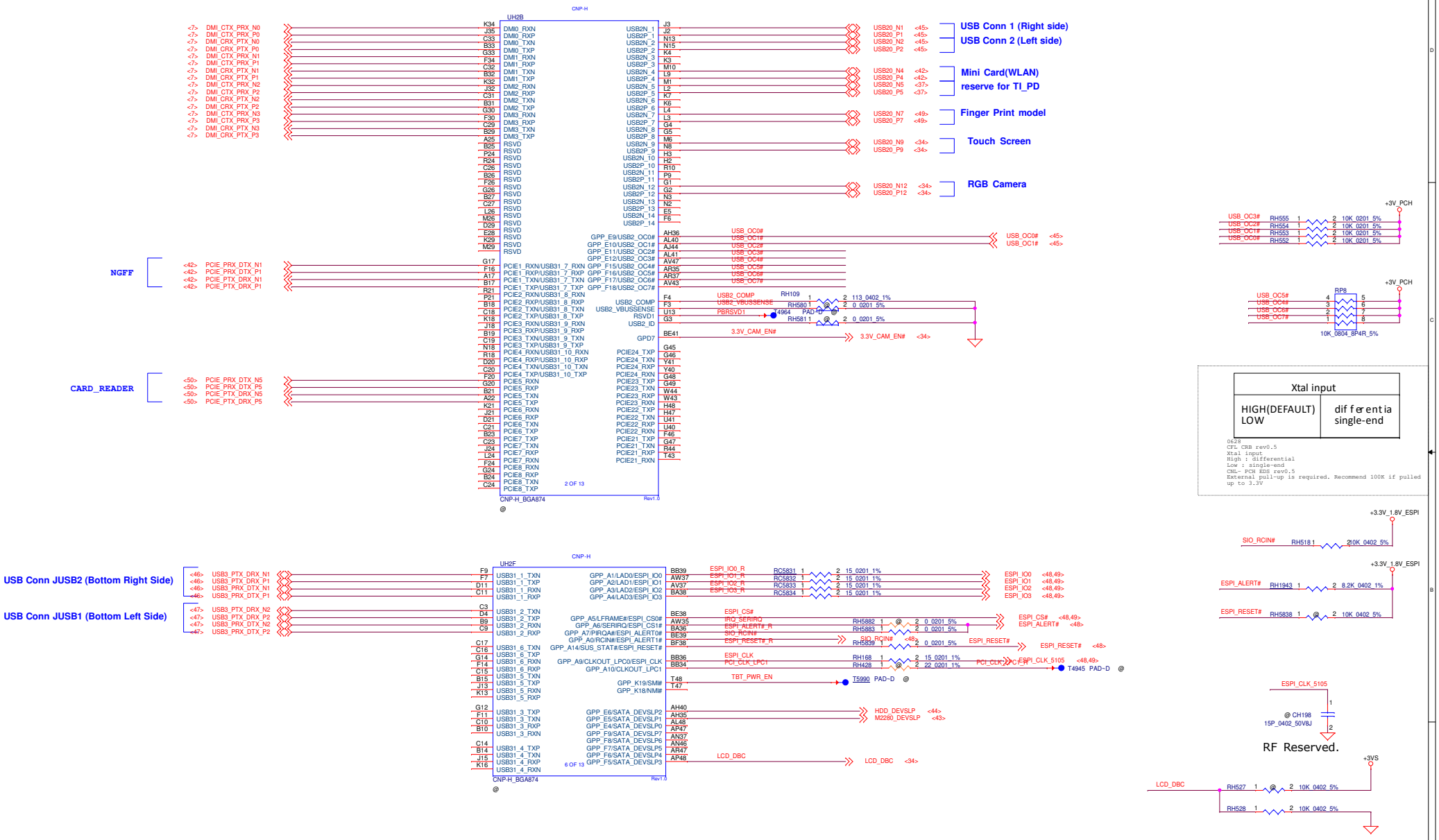
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P18-PCH (3/7) PM,HDA,SMB,JTAG**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 18 of 76



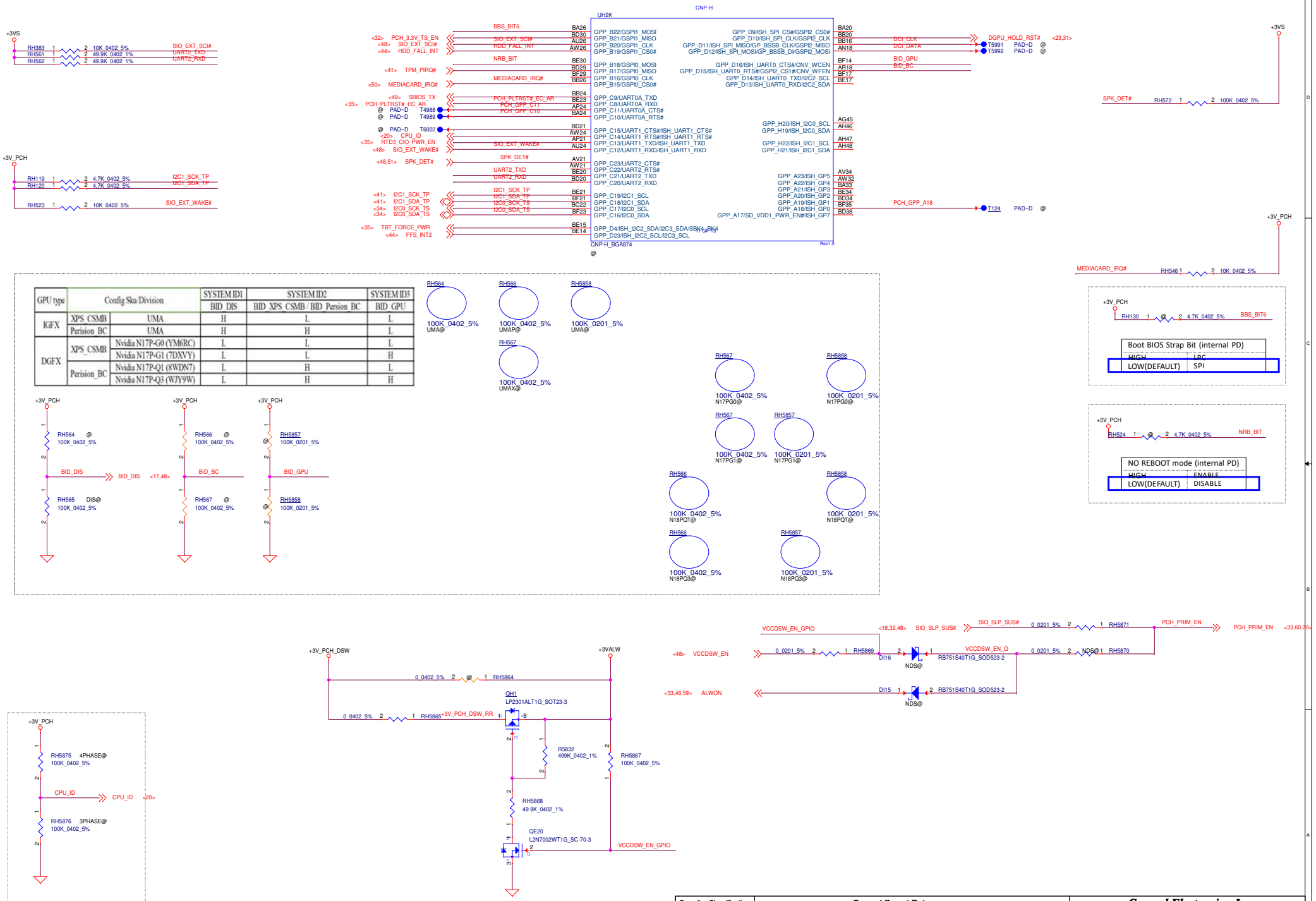
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P19-PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 19 of 76



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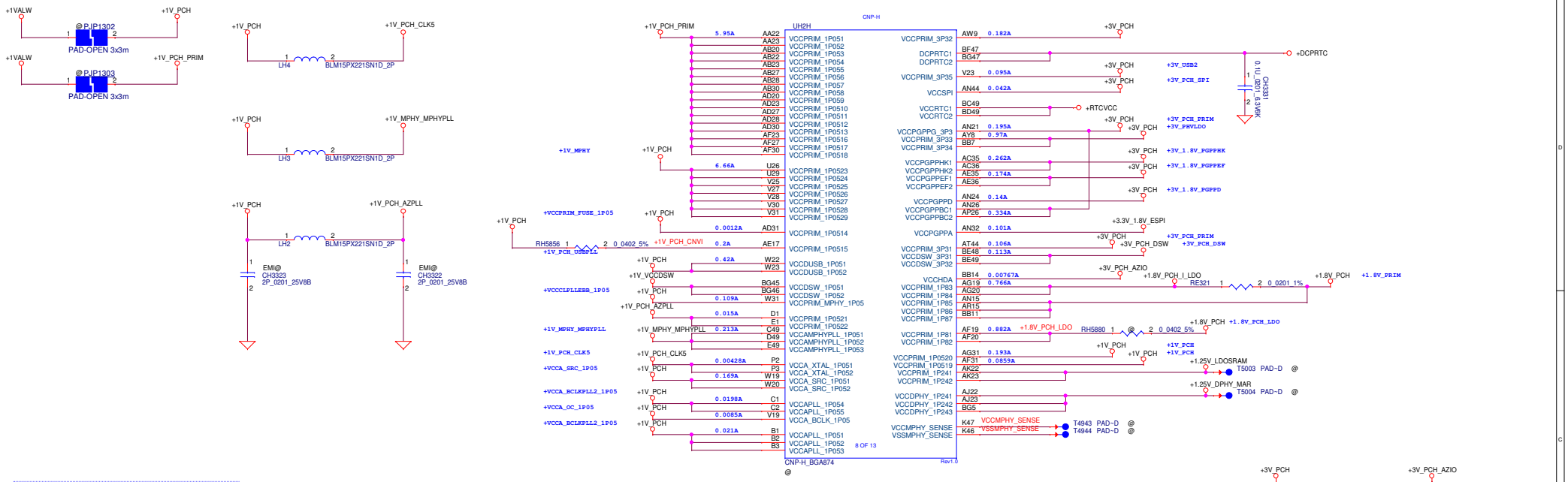
Compal Electronics, Inc.

Title: P20-PCH (5/7) I2C,GPIO

Size | Document Number: LA-G341P | Rev: 1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 20 of 76



+1V_PCH_AZPLL

Close to ball name
D1, E1
CH203 1uF 0402 capacitor

+1V_VCCDSW

Close to ball name
BG45, BG46
1x 1uF 0402

+RTCVCC

Close to ball name
BC49, BD49
1x 0.1uF 0402, 3mm
1x 1uF 0402, 5mm

+1V_PCH

0613
+VCCA_BCLKPLL2_1P05
Intel review
Close to ball name
B1, B2, B3, C1, C2
1uF 0402 capacitor

+1V_PCH_PRIM

0613 intel review
Close to net name
+1V_PCH_PRIM
1uF 0402 capacitor

+3V_PCH_AZIO

0613
Close to ball name
BB14
1uF 0402 capacitor

20170614
+3V_PHVLDO
Intel review
To add 1x 1uF 0603, 3mm
Close to ball name AY8, BB7

20170717 DB review change

+1V_PCH_CLK5

+1V_PCH_CLK5
Close ball name P2 , P3

+3V_1.8V_PGPPEF
Close to ball name
AE35 , AE36
1x 0.1uF 0402 3mm
(placeholder)

+1.8V_PCH

20170614 Intel review
To add 1x 1uF, 0402
on +1.8V_PCH.

+1V_PCH

+1V_MPHY
Close to ball name
U26,U29,V25,
V27,V28,V30,V31
1x 1uF 0402, 3mm
1x 22uF 0805, 5mm

+1V_MPHY_MPHYPLL

20170717 DB review change

20170613
+1V_MPHY_MPHYPLL
Intel review
To change close ball name.
Close to ball name
C49,D49,E49
1x 1uF 0402, 3mm

+1V_PCH_PRIM

Close to ball name
AF31, AG31, AD31, AA22,
AA23, AB20, AB22, AB23,
AB27, AB28, AB30, AD20,
AD23, AD27, AD28, AD30,
AF23, AF27, AF30, AE17, 3mm

20170614
+3V_PCH_DSW
Intel review
To add 1x 0.1uF 0402, 3mm
Close to ball name BE48, BE49

+3V_1.8V_PGPPD
Close to ball name
AN24
1x 0.1uF 0402 3mm
(placeholder)

+1.8V_PCH

+1.8V_PRIM
Close to ball name
AG19, AG20, AR15, AN15, BB11
1x 4.7uF 0603, 3mm
Option 1: Internal LDO
1x 1uF 0402, 3mm
Option 2: External VRM

+3V_PCH

+3V_1.8V_PGPPEF
Close to ball name
AE35, AE36
1x 0.1uF 0402, 3mm
(placeholder)

+3V_1.8V_PGPPHK
Close to ball name
AC35, AC36
1x 0.1uF 0402 3mm
(placeholder)

+1V_PCH

0619
+1V_PCH_USBPLL
EMI require 100nF
Close to W22,W23 for EMI require

+3VS

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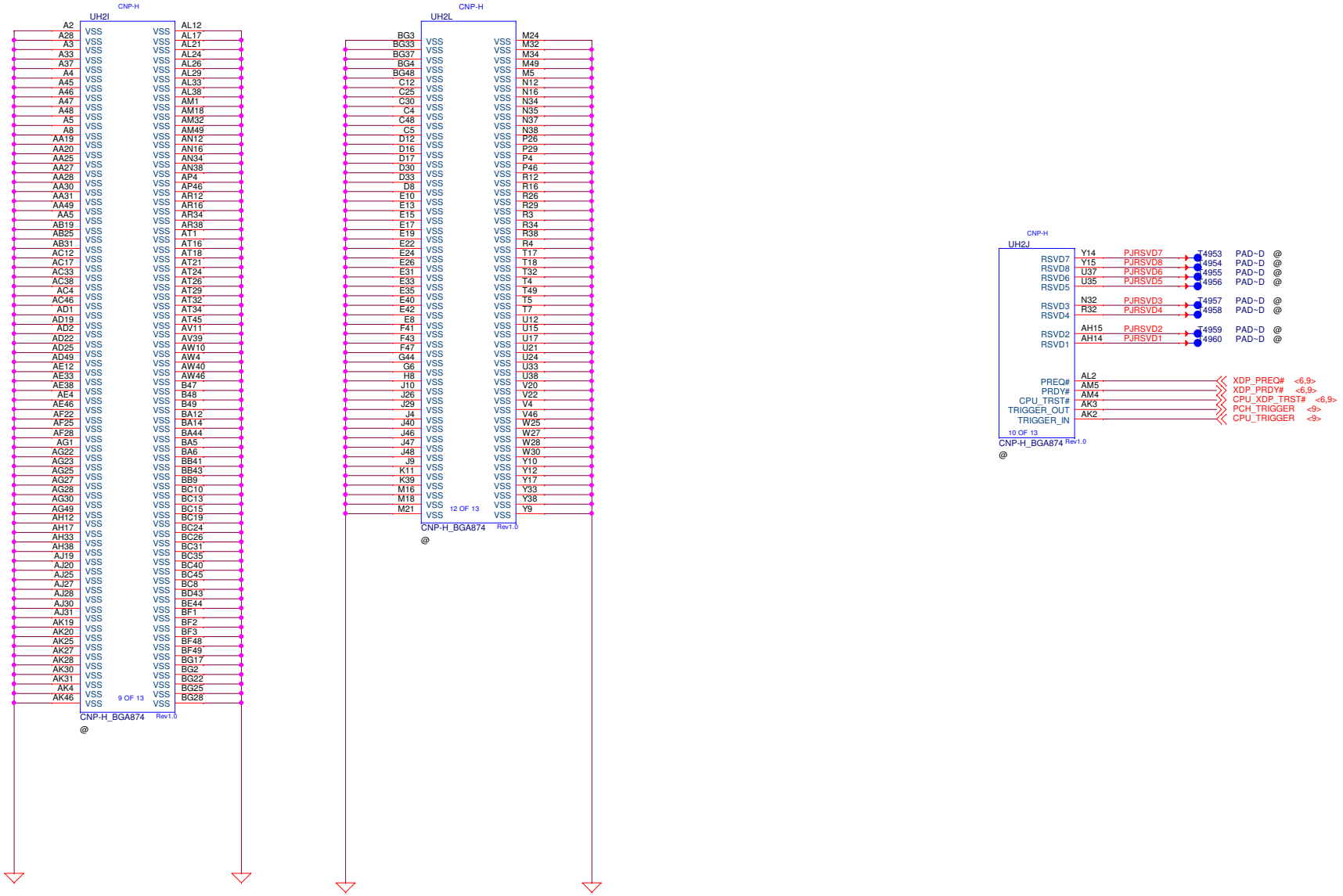
Compal Electronics, Inc.

Title: **P21-PCH (6/7) PWR**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 21 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P22-PCH (7/7) VSS**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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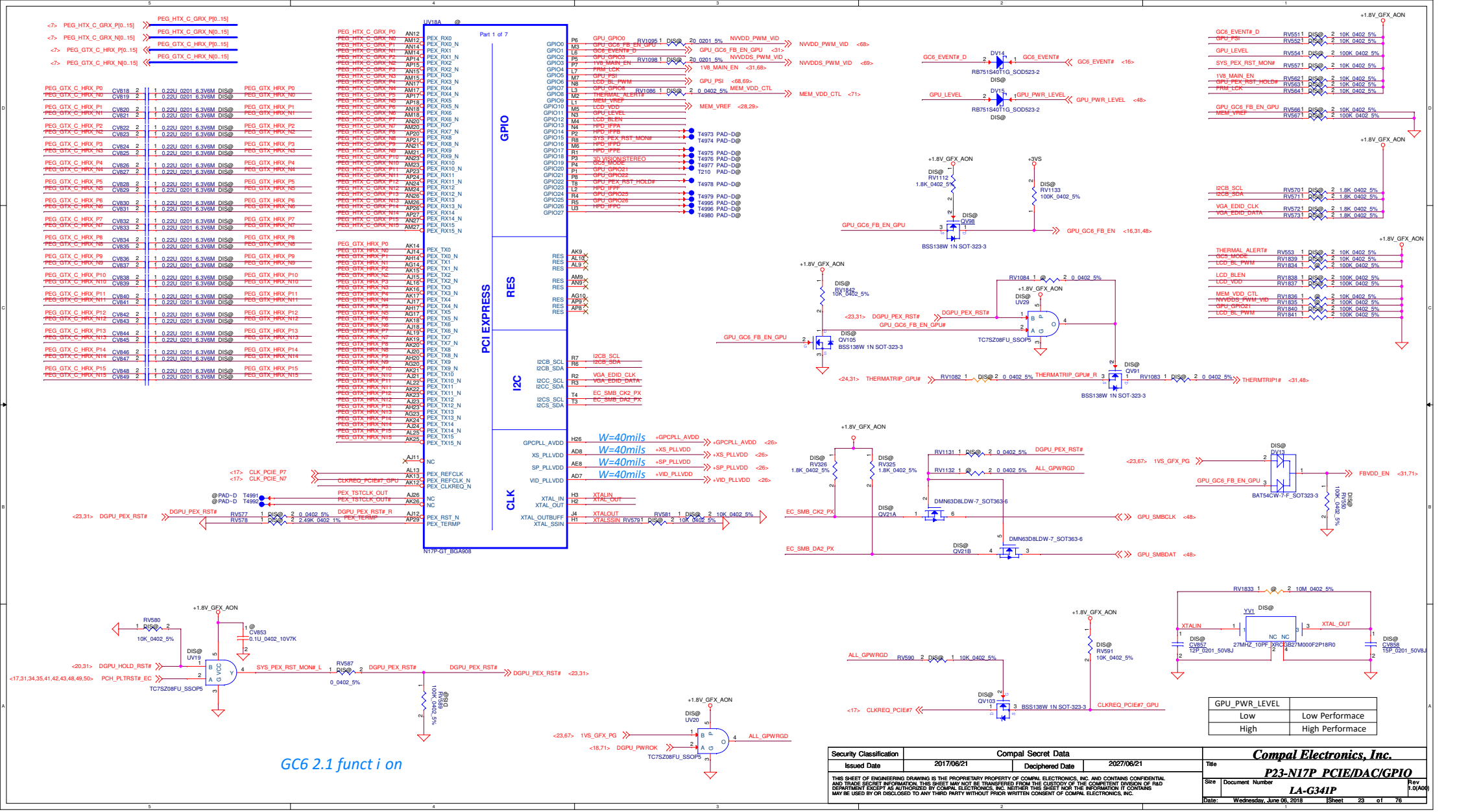
PEG_HTX_C_GRX_P[0..15]
PEG_HTX_C_GRX_N[0..15]
PEG_GTX_C_HRX_P[0..15]
PEG_GTX_C_HRX_N[0..15]
UV18A
Part 1 of 7
PCI EXPRESS
GPIO
RES
I2C
CLK
N17P-GT_BGA908
GPU_GC6_FB_EN_GPU
NVVDD_PWM_VID
NVVDDS_PWM_VID
MEM_VDD_CTL
MEM_VREF
LCD_VDD
LCD_BLEN
HPD_IFPA
HPD_IFPB
SYS_PEX_RST_MON#
HPD_IFPD
HPD_IFPE
3D_VISION/STEREO
GPU_GPIO21
GPU_GPIO22
GPU_PEX_RST_HOLD#
GPU_GPIO25
GPU_GPIO26
HPD_IFPC
I2CB_SCL
I2CB_SDA
VGA_EDID_CLK
VGA_EDID_DATA
EC_SMB_CK2_PX
EC_SMB_DA2_PX
+GPCPLL_AVDD
+XS_PLLVDD
+SP_PLLVDD
+VID_PLLVDD
W=40mils
CLK_PCIE_P7
CLK_PCIE_N7
DGPU_PEX_RST#
DGPU_PEX_RST#_R
PEX_TSTCLK_OUT
PEX_TERMP
GC6 2.1 funct i on
GPU_PWR_LEVEL
Low
Low Performace
High
High Performace
Security Classification
Compal Secret Data
Issued Date
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Compal Electronics, Inc.
P23-N17P PCIE/DAC/GPIO
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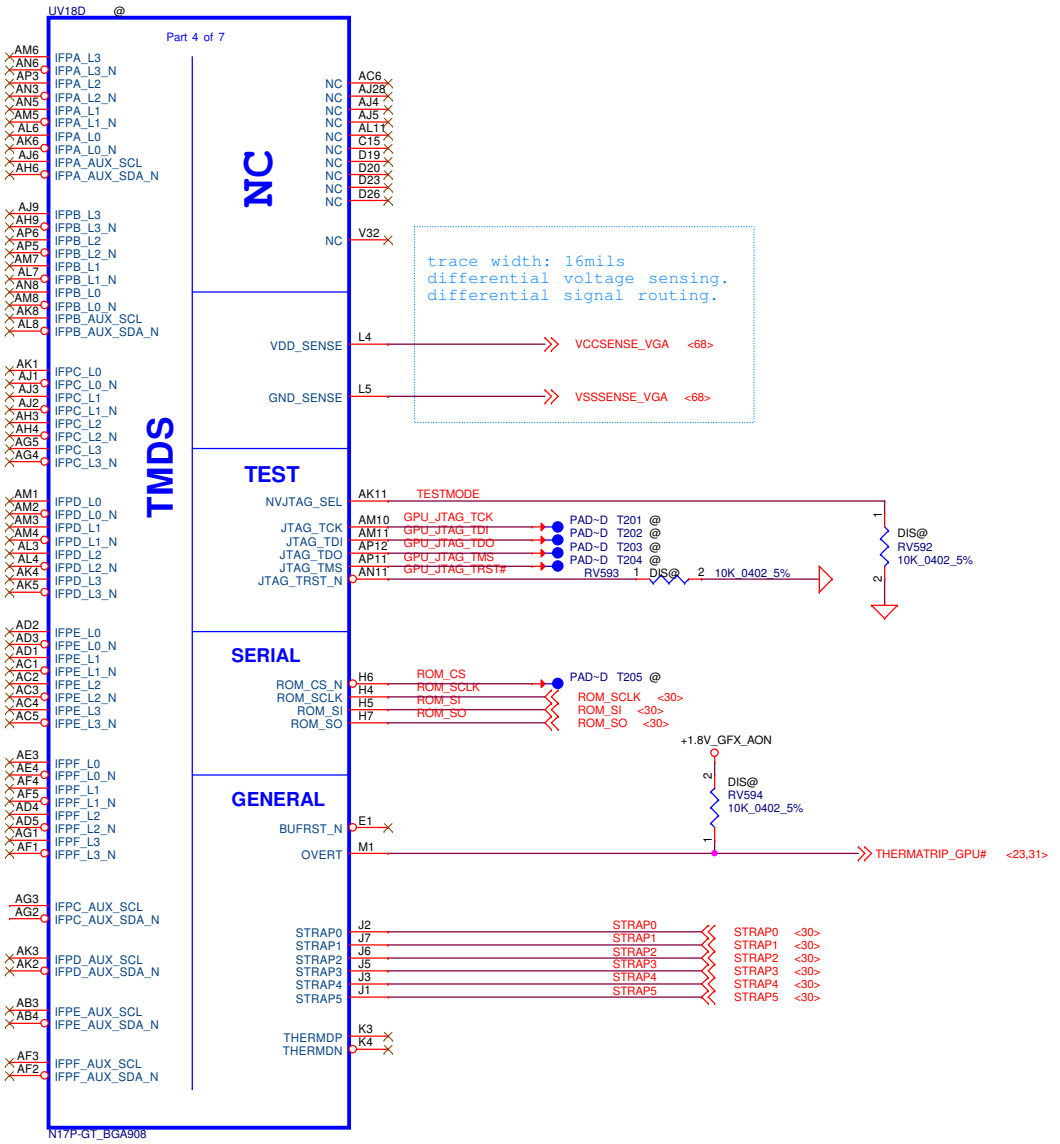

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P24-N17P_eDP/HDMI/mDP**

Size	Document Number	Rev
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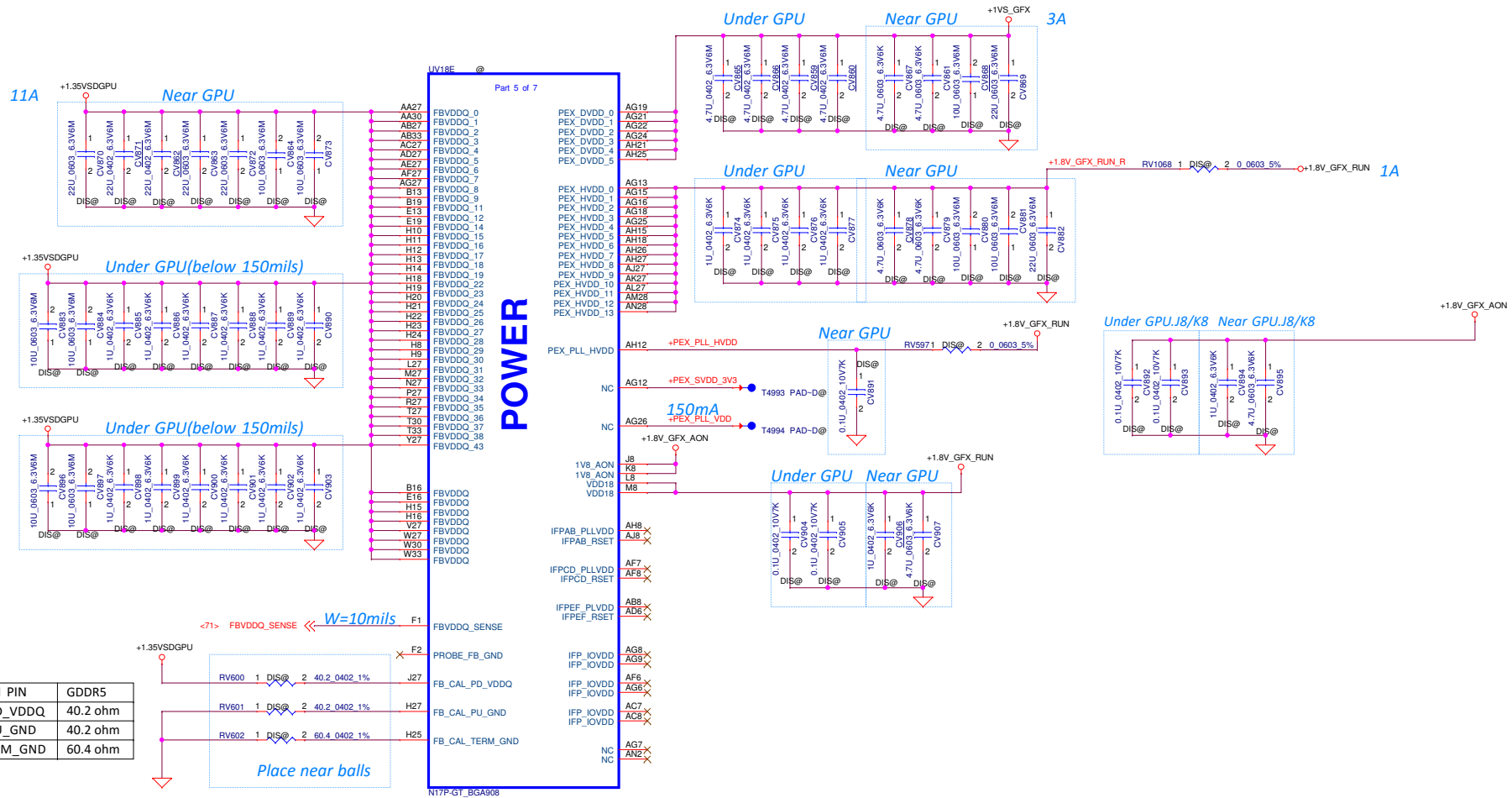
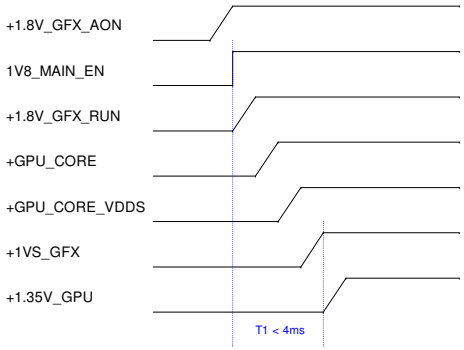


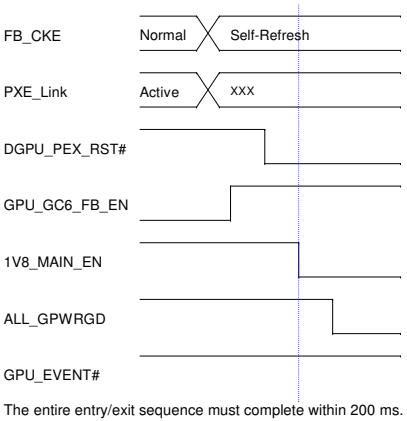
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

GPU Power Up Sequence



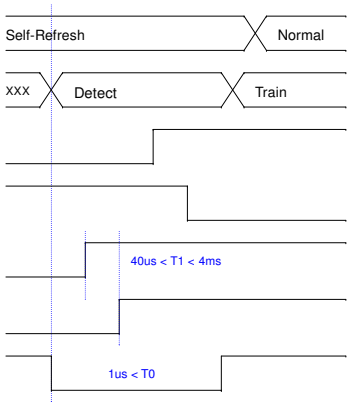
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

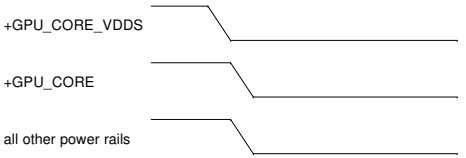


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



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Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title: P25-N17P_Power			
Size	Document Number: LA-G341P		Rev: 1.0(A00)
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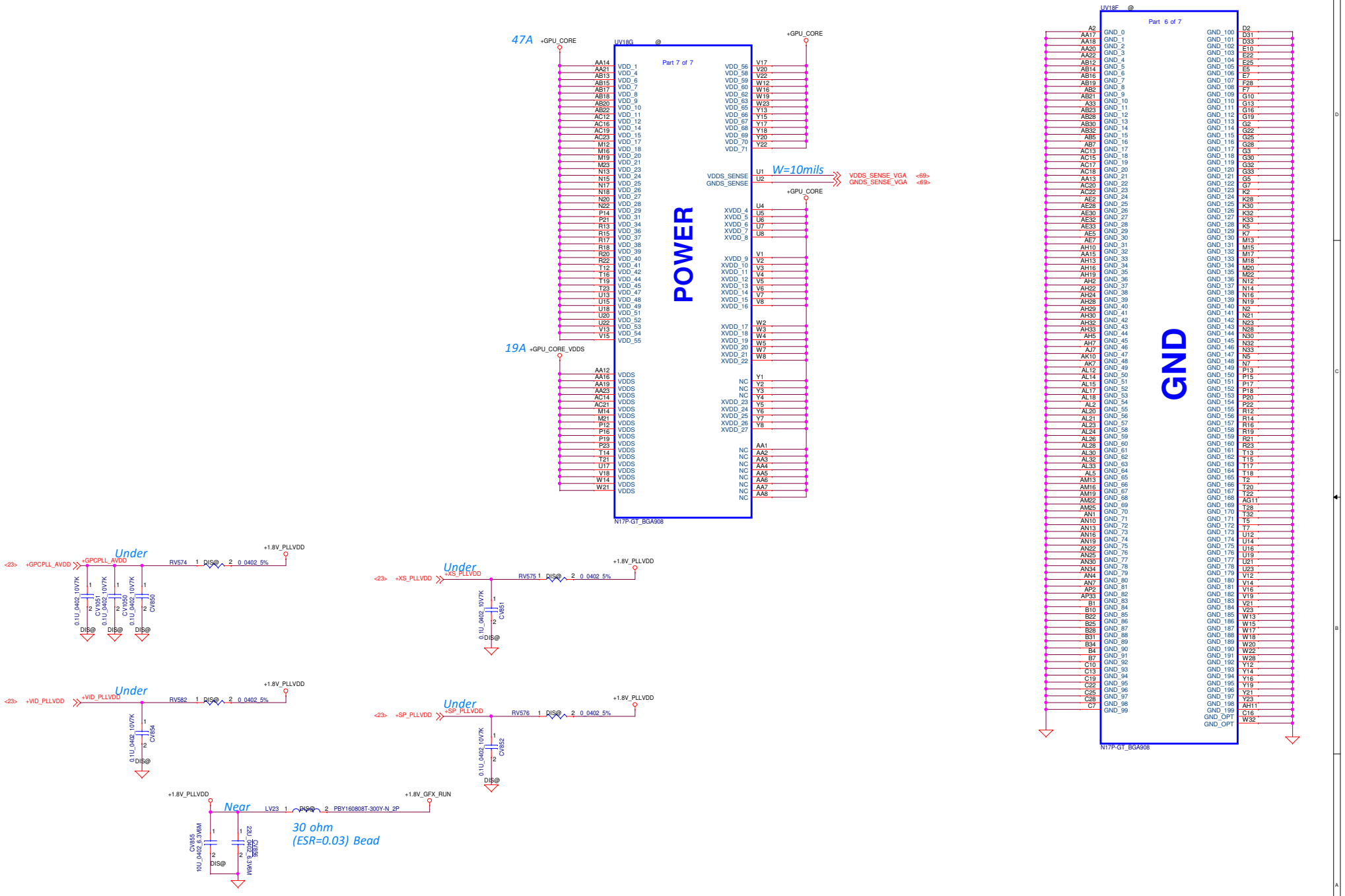

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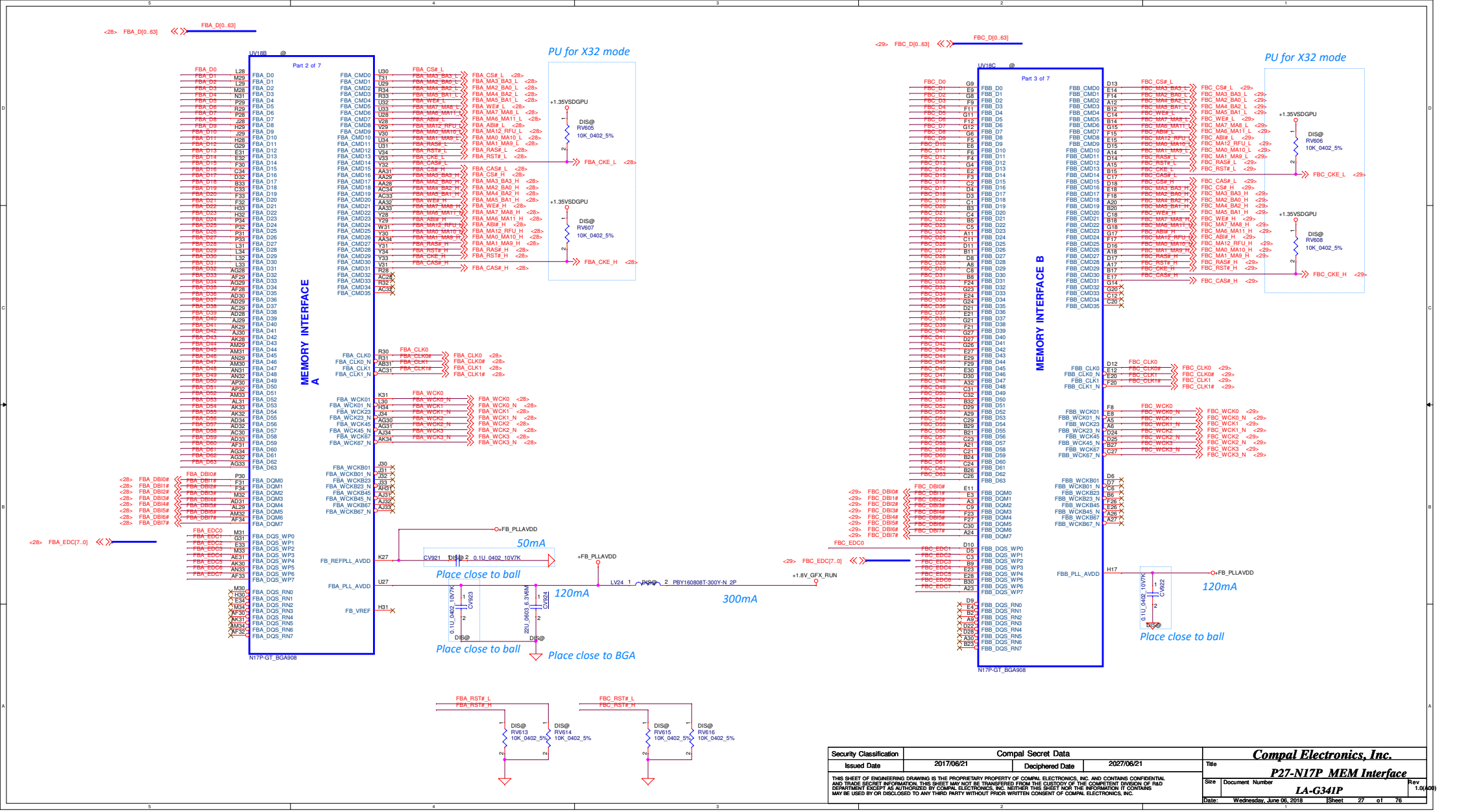
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title	P26-N17P_VGA CORE/GND		
Size	Document Number		Rev
	LA-G341P		1.0(A00)
Date:	Wednesday, June 06, 2018	Sheet	26 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P27-N17P MEM Interface**

Size	Document Number	Rev
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Memory Partition A- Lower 32bit

MF=0

UV23

UV24

MF=1

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

W=16mils

Around DRAM

Close to DRAM

Under DRAM

170-BALL SGRAM GDDR5

K4G80325FB-HC03_FBGA170-D

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P28-N17P GDDR5 A

Size: | Document Number: LA-G341P | Rev: 1.0(A00)

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Memory Partition A- Lower 32bit

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

MF=0

MF=1

UV25

UV26

170-BALL SGRAM GDDR5

K4G80325FB-HC03_FBGA170-D

W=16mils

Around DRAM

Close to DRAM

Under DRAM

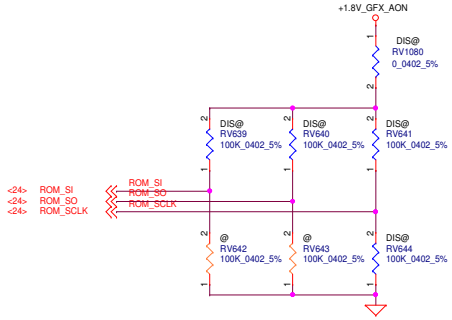
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

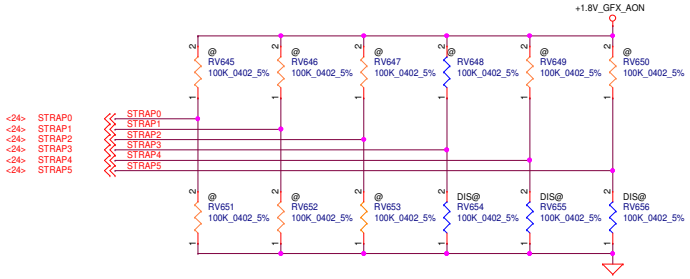
Compal Electronics, Inc.

Title: P29-N17P_GDDR5_B

Size: | Document Number: LA-G341P | Rev: 1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 29 of 76





SMB_ALT_ADDR	State
Low	Single GPU
High	Dual GPU

DEVID_SEL	State
Low	Original Device ID
High	Re-brand Device ID

PCIE_CFG	State
Low	Normal signal swing
High	Reduce the signal amplitude

VGA_DEVICE	State
Low	3D Device
High	VGA Device

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]

Table 4. N17P-Q1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:
1. For N17P-Q1, the maximum allowable memory case temperature is 85 °C.

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Berlinetta MLK			
Straps	(N17P-Q1)		(N17P-G0)
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL.	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0) , DEVIE_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0) , VGA_DEVICE(0)
STRAP5	Unused	"L"	

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Title: P30-N17P_MISC
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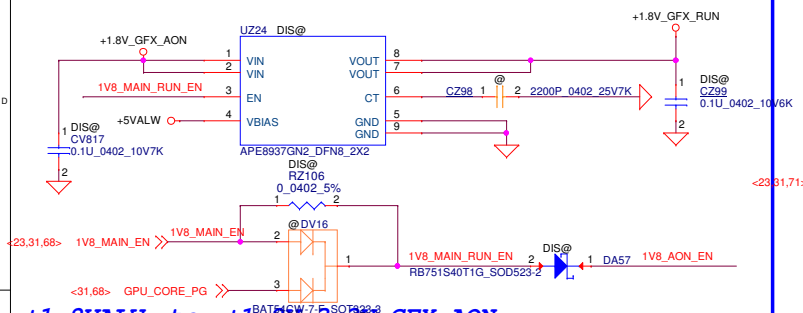
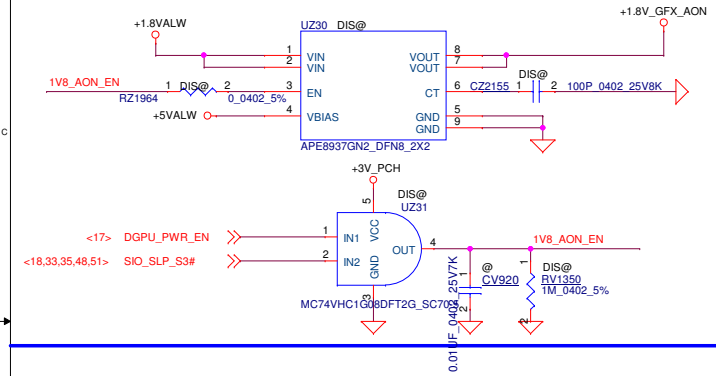
+1.8V_3.3V_GFX_RUN

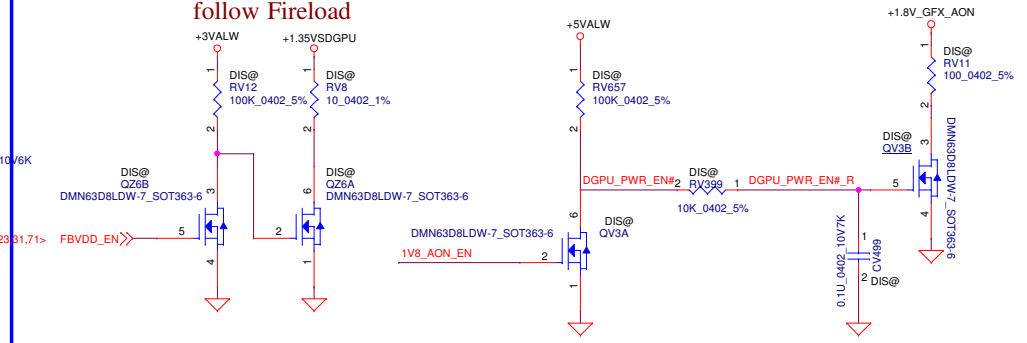


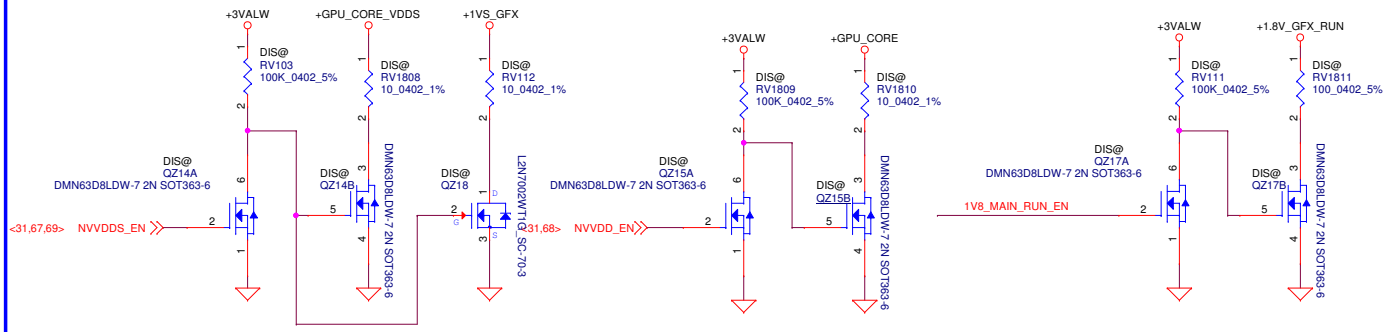
+1.8VALW to +1.8V_3.3V_GFX_AON



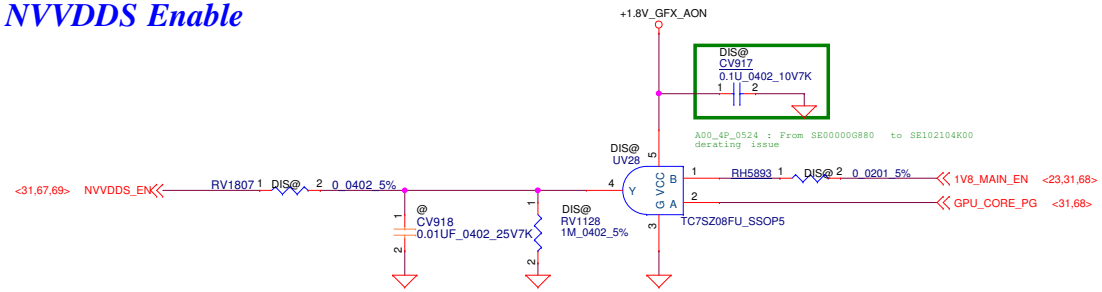
Discharge

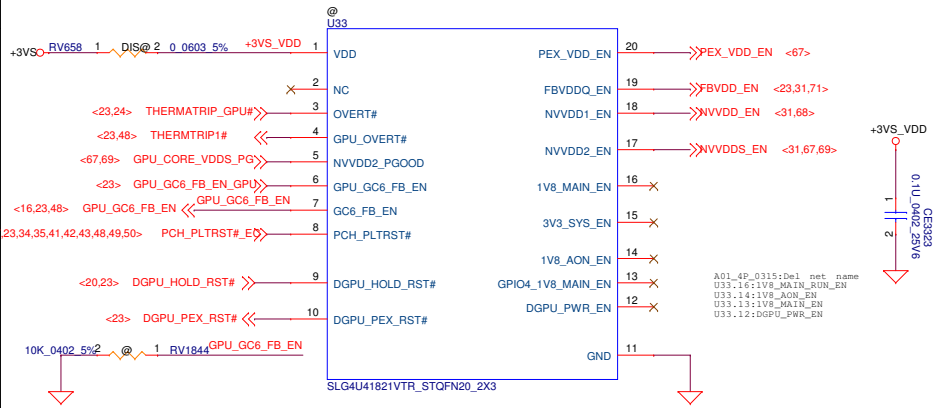
follow Fireload



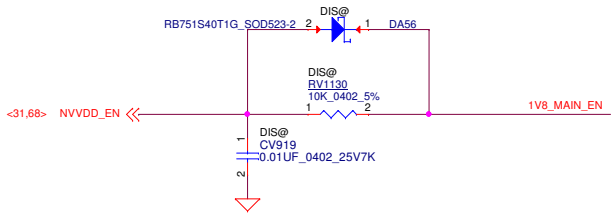


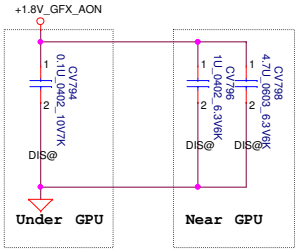
NVVDDS Enable





NVVDD Enable





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P31-DC/DC-VGA**

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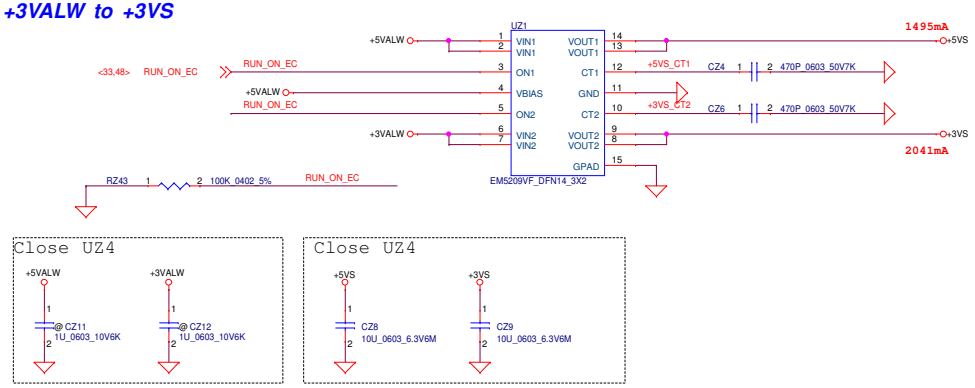
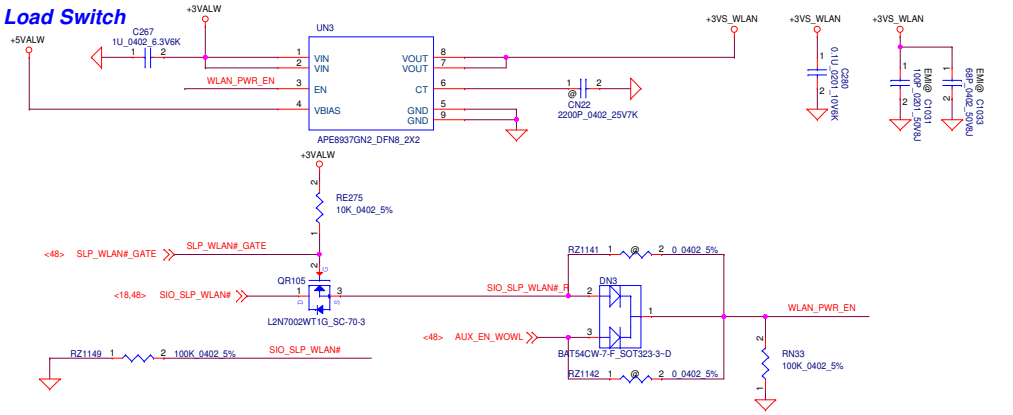
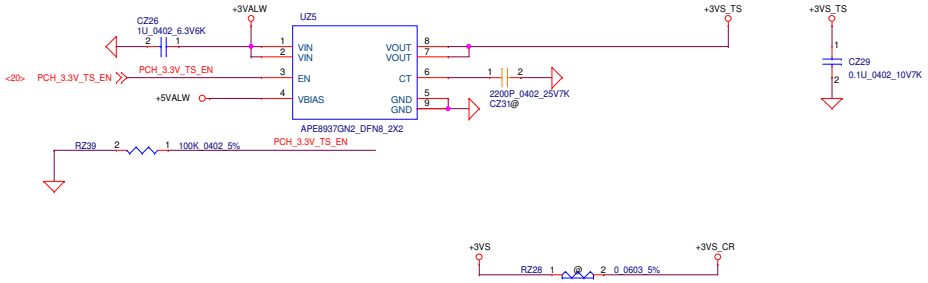
+5VALW to +5VS
+3VALW to +3VS



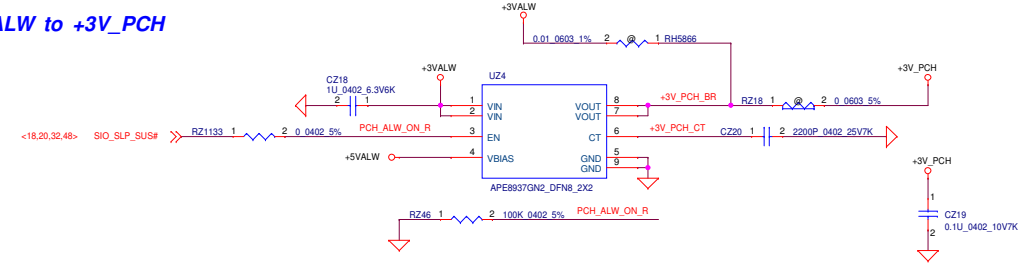
WLAN Load Switch



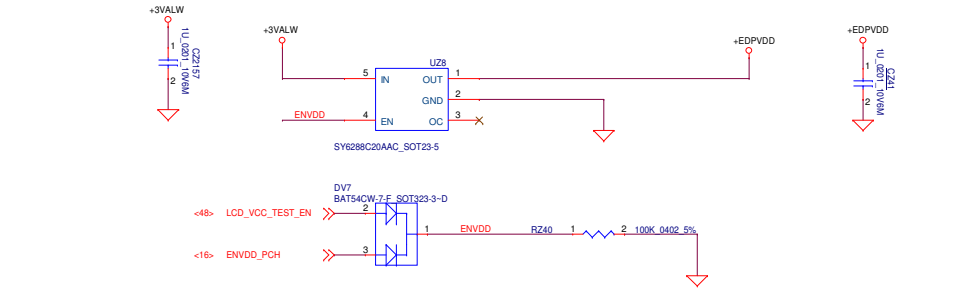
Touch Screen Load Switch & Card Reader



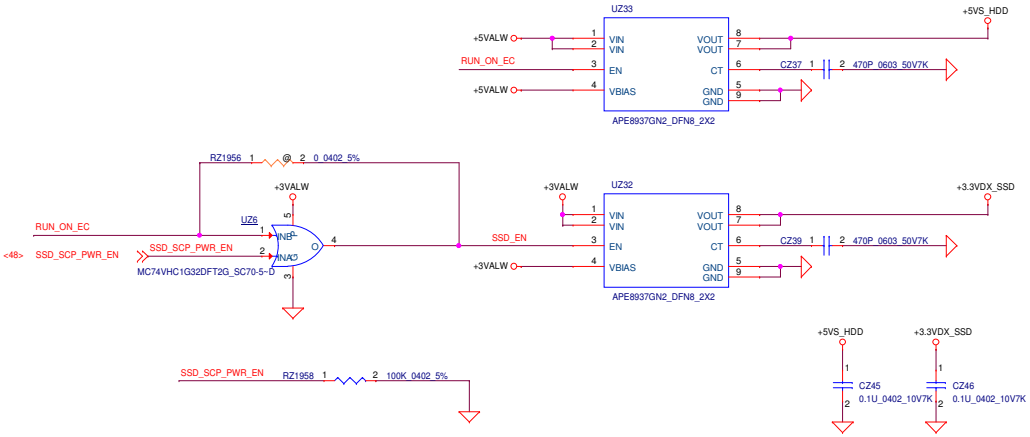
+3VALW to +3V_PCH



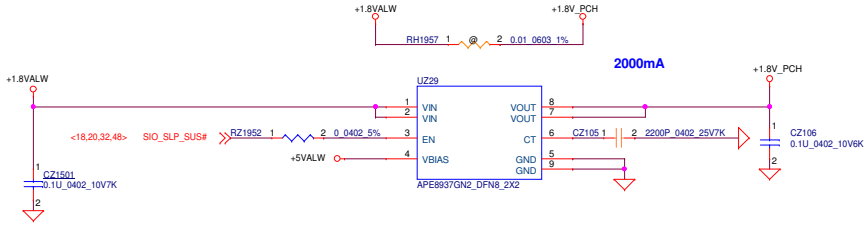
eDP & Camera Load Switch



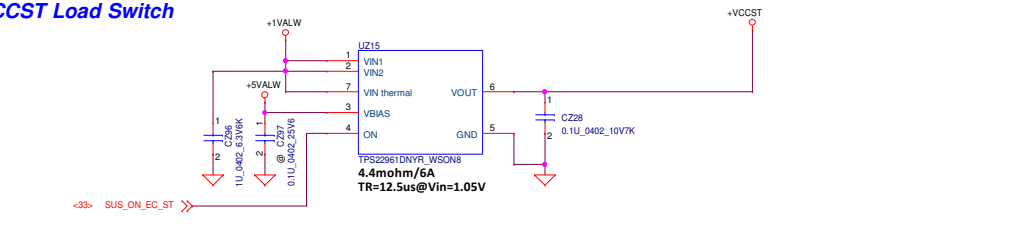
HDD, SSD Load Switch



+1.8VALW to +1.8V_PCH



+VCCST Load Switch



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P32-DC/DC SYSTEM**

Size	Document Number	Rev
	LA-G341P	1.0(A00)

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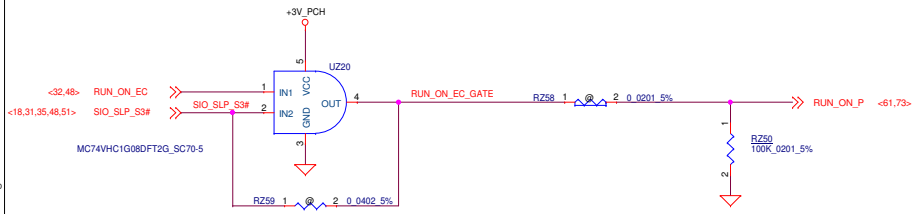
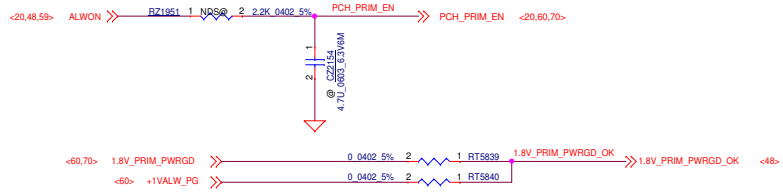
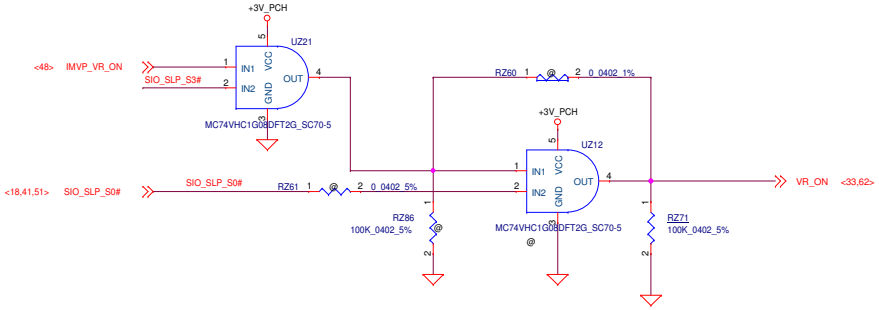
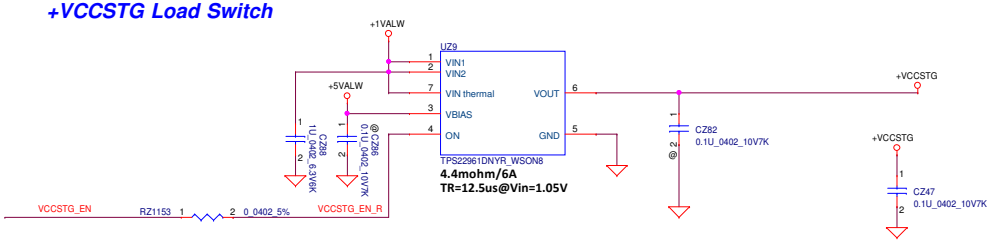
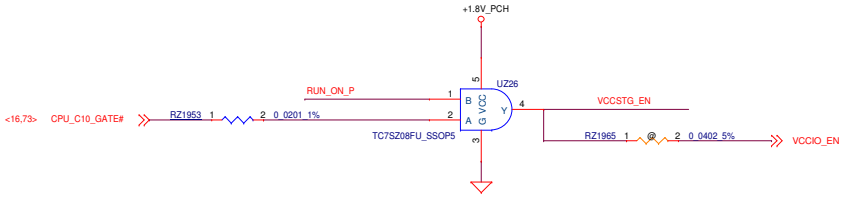


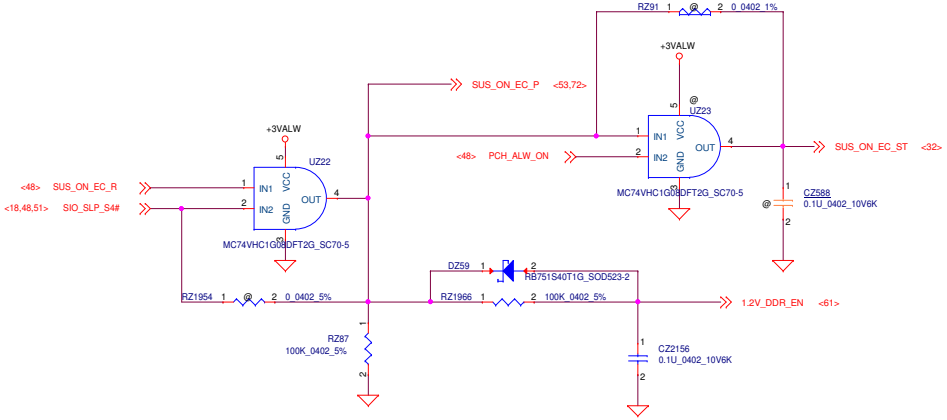




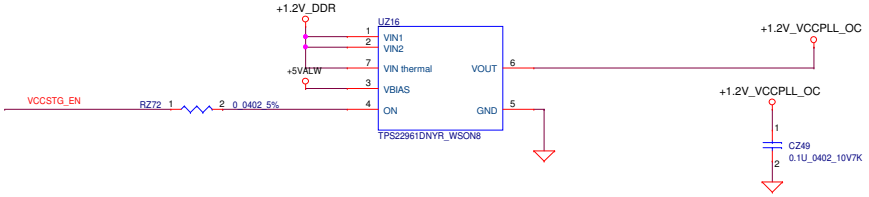
+VCCSTG Load Switch

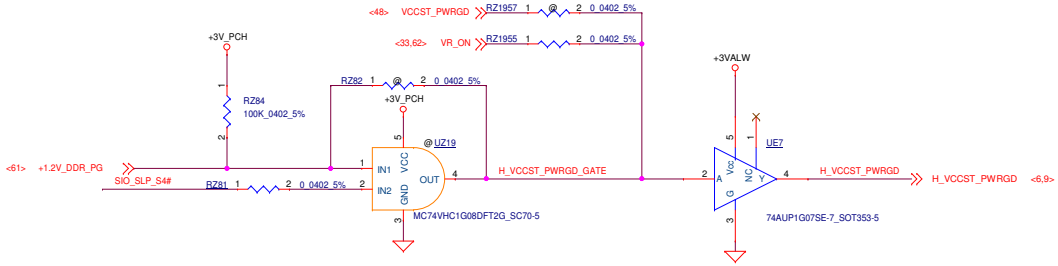






+VCCPLL_OC Load Switch





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P33-DC/DC/S0iX/CS

Size	Document Number	Rev
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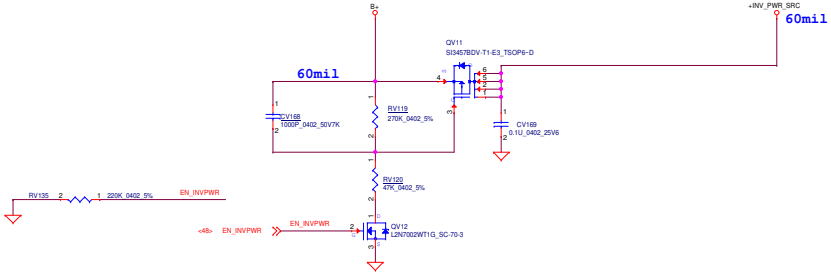
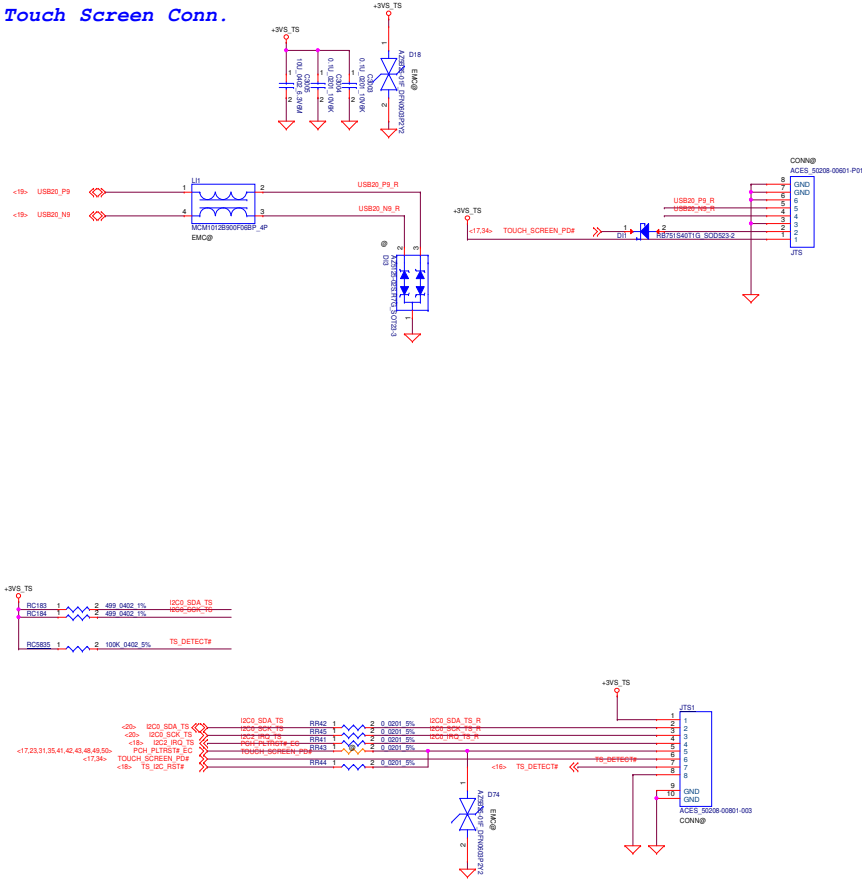
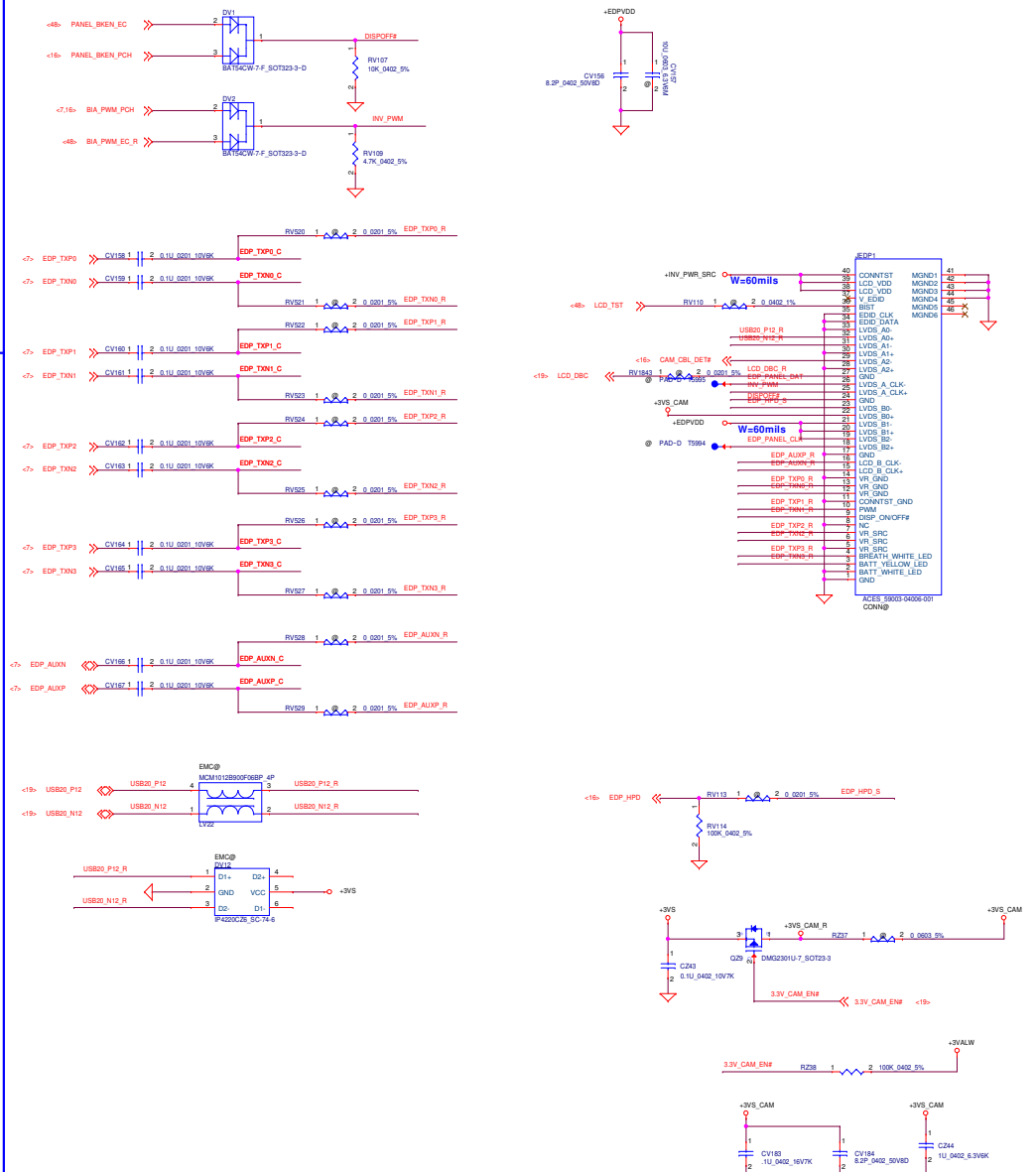
LCD backlight PWR CTRL



Touch Screen Conn.

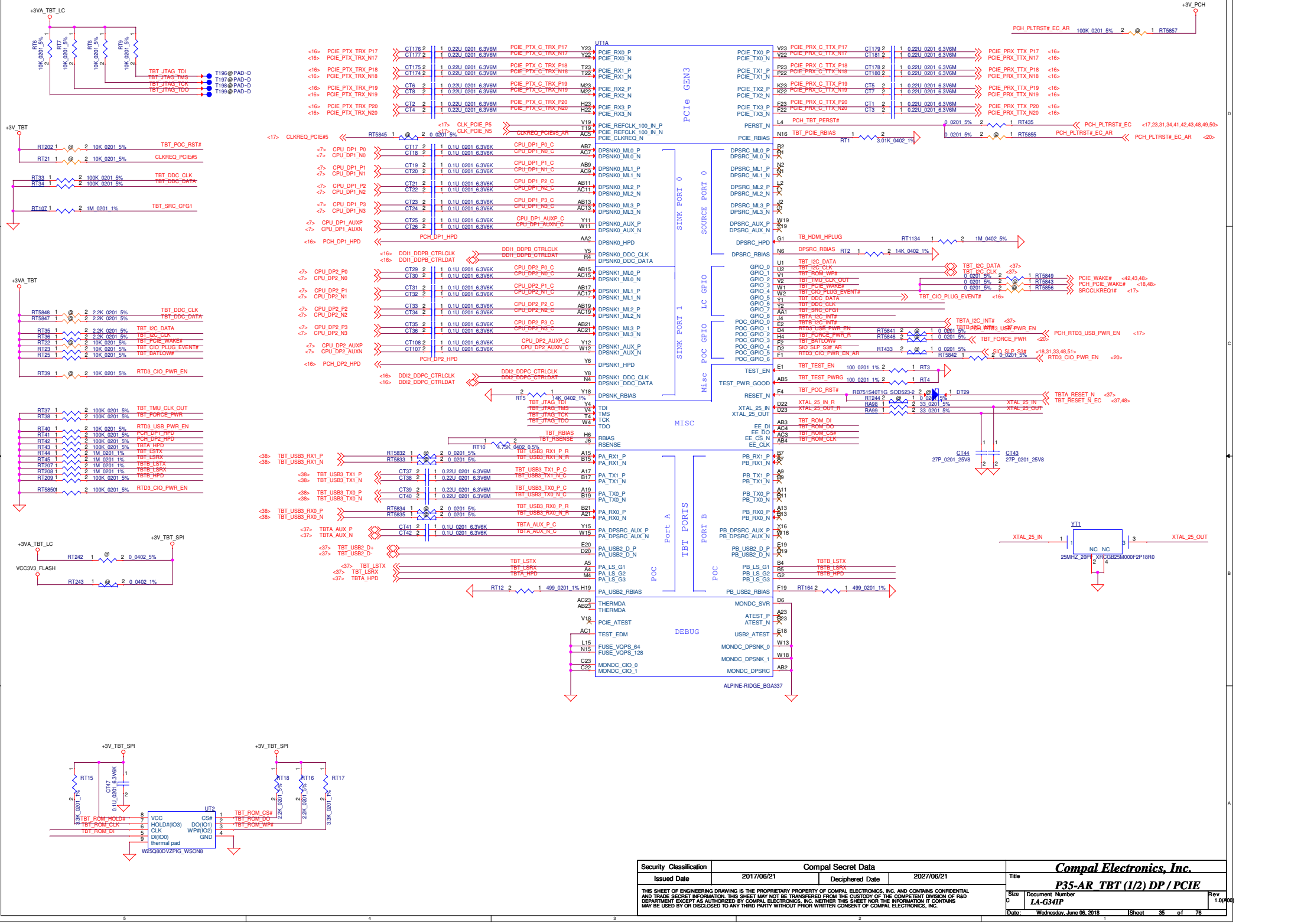


eDP & CCD(RGB) Conn.



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.	
Title	P34-eDP/CCD/TS
Size	Document Number: LA-G341P Rev: 1.0(A00)
Date: Wednesday, June 06, 2018	Sheet 34 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P35-AR_TBT (1/2) DP / PCIE**

Size	Document Number	Rev
C	LA-G341P	1.0(A00)

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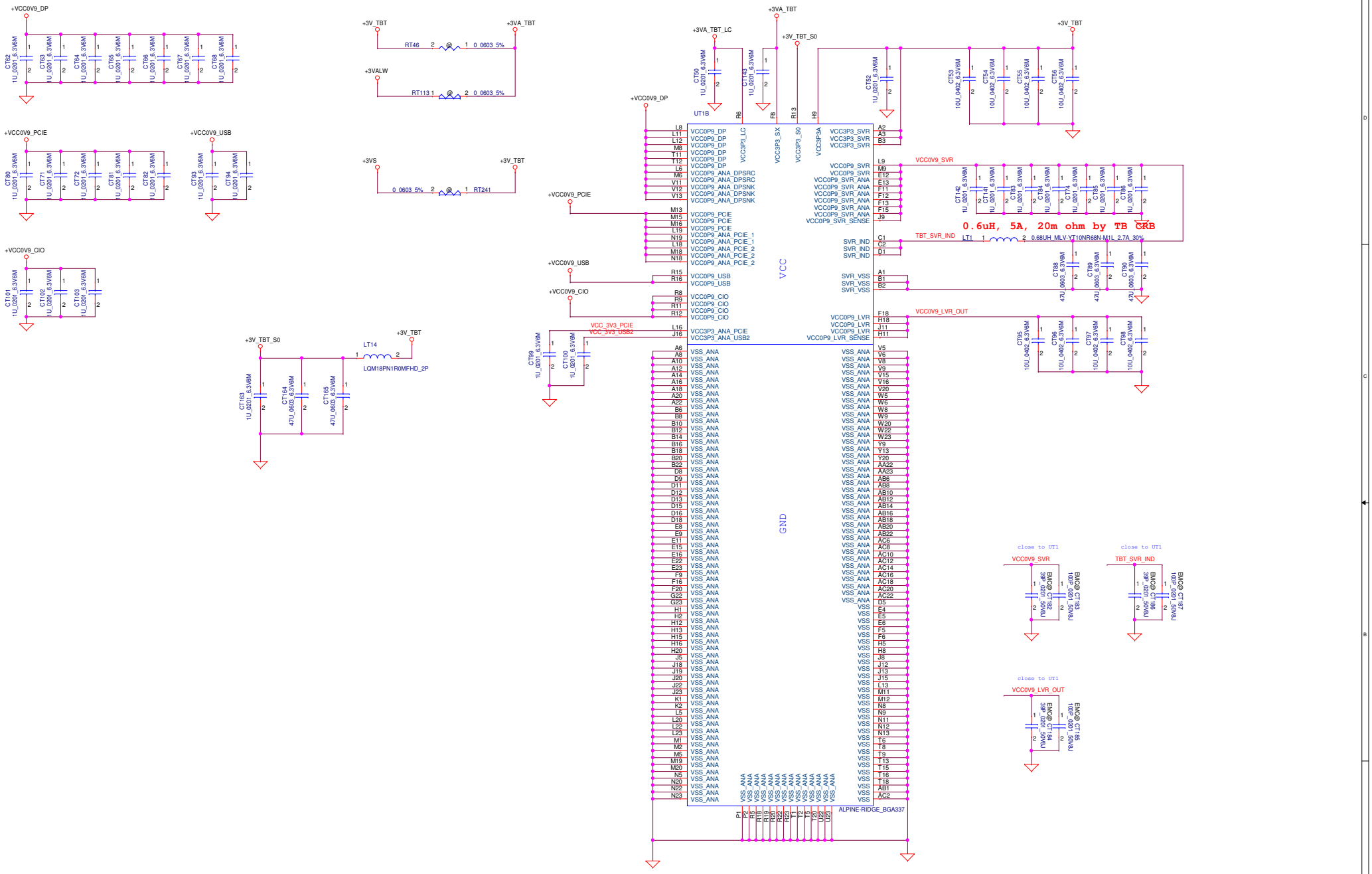

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P36-AR_TBT (2/2) PWR / VSS**

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C	LA-G341P	1.0(A00)

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+5VALW
CT147 22U_0603_6.3V6M
CT148 22U_0603_6.3V6M
CT149 22U_0603_6.3V6M
CT150 22U_0603_6.3V6M
+5VALW
+3VALW
CT188 4.7U_0603_25V6K
CT189 10U_0402_6.3V6M
TBTA_LDO_BMC
VCC3V3_TBT_SX
VCC3V3_FLASH
VCC1V8A_TBTA_LDO
VCC1V8D_TBTA_LDO
CT144 2.2U_0402_6.3V6M
CT145 1U_0201_6.3V6M
CT146 10U_0402_6.3V6M
CT151 2.2U_0402_6.3V6M
CT152 2.2U_0402_6.3V6M
+VBUS_1
CT153 1U_0603_25V6
+3VA_TBT
RT167 10K_0201_5% TBTA_I2C_INT#
RT1145 10K_0201_5% TBTB_I2C_INT#
TBTB_I2C_INT# <35>
VCC3V3_FLASH
RT168 3.3K_0201_1% PD_EE_CS#
RT169 3.3K_0201_1% PD_EE_DO
RT170 3.3K_0201_1% PD_EE_WP#
RT171 3.3K_0201_1% PD_HOLD#
RT432 100K_0201_5% TBTA_AUX_N
RT431 100K_0201_5% TBTA_AUX_P
UT4
PP_HV
RT1092 0_0603_5%
+5VALW
+3VALW
RT1095 0_0402_5%
PD_VDDIO_VIN_3V3
PP_CABLE
VDDIO
VIN_3V3
<35> TBT_I2C_DATA
<35> TBT_I2C_CLK
<35> TBTA_I2C_INT#
RT58361 0_0201_5% TBT_I2C_DATA_R
RT58371 0_0201_5% TBT_I2C_CLK_R
RT58381 0_0201_5% TBTA_I2C_INT#_R
I2C_SDA1
I2C_SCL1
I2C_IRQ1_N
UPD_SMBDAT_R
UPD_SMBCLK_R
I2C_SDA2
I2C_SCL2
I2C_IRQ2_N
<48> UPD1_ALERT#
PD_EE_CLK
PD_EE_DI
PD_EE_DO
PD_EE_CS#
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS_N
<19> USB20_P5
<19> USB20_N5
RT1144 0_0201_5%
RT1143 0_0201_5%
<35> TBT_USB2_D+
<35> TBT_USB2_D-
RT1141 0_0201_5%
RT1142 0_0201_5%
USB20_P5_R
USB20_N5_R
USB_RP_P
USB_RP_N
<35> TBTA_AUX_P
<35> TBTA_AUX_N
AUX_P
AUX_N
@ PAD~D T193
@ PAD~D T194
SWD_CLK
SWD_DATA
RT430 100K_0201_5%
UART_TX
UART_RX
<35> TBT_LSTX
<35> TBT_LSRX
TBT_LSTX
TBT_LSRX
LSTX/R2P
LSRX/P2R
VCC3V3_FLASH
RT226 10K_0201_5%
RT227 10K_0201_5%
PD_DEBUG_CTRL1
PD_DEBUG_CTRL2
DEBUG_CTL1
DEBUG_CTL2
<48> DOCK_TNY_SMB_CLK
<48> DOCK_TNY_SMB_DAT
RT184 20_0201_5%
RT185 20_0201_5%
TBTA_DEBUG1
TBTA_DEBUG2
DEBUG1
DEBUG2
TBT_LSTX
TBT_LSRX
RT233 20_0201_5%
RT232 20_0201_5%
TBTA_DEBUG3_LSTX
TBTA_DEBUG4_LSRX
DEBUG3
DEBUG4
I2C_ADDR
RT187 10K_0201_1%
RT188 10K_0201_1%
@ RT190 0_0402_1%
SN1703018ZQZR_BGA96
TBTA_HRESET
RT429 100K_0201_5%
TBTA_HRESET might be connected to EC or PCH to allow TPS65982 FW load
SENSEP
SENSEN
HV_GATE1
HV_GATE2
VBUS
VOUT_3V3
LDO_3V3
LDO_1V8A
LDO_1V8D
LDO_BMC
T191 PAD~D @
T192 PAD~D @
VCC3V3_TBT_SX
VCC3V3_FLASH
VCC1V8A_TBTA_LDO
VCC1V8D_TBTA_LDO
TBTA_LDO_BMC
CT157 1U_0603_25V6
BAT54HT1G
DT10 AZ4024-02S_SOT23-3~D
EMC@
close to +VBUS_1
C_CC1
C_CC2
CT160 220P_0402_50V7K
CT159 220P_0402_50V7K
TBTA_CC1 <38>
TBTA_CC2 <38>
RPD_G1
RPD_G2
C_USB_TP
C_USB_TN
TBTA_TOP_P <38>
TBTA_TOP_N <38>
0615 CHANGE NET NAME
C_USB_BP
C_USB_BN
TBTA_BOT_P <38>
TBTA_BOT_N <38>
C_SBU1
C_SBU2
TBTA_PD_SBU1
TBTA_PD_SBU2
RT176 0_0201_5%
RT177 0_0201_5%
TBTA_SBU1 <38>
TBTA_SBU2 <38>
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
T185 PAD~D @
RT178 0_0201_5%
RT437 1M_0201_1%
RT5844 0_0201_5%
RT181 0_0201_5%
RT182 0_0201_5%
PD_GPIO2
PD_PGPIO7
TBT_CONFIG
EN_PD_HV_1 <57>
AC1_DISC# <57,58>
TBTA_HPD <35>
PWR_BTN_DOCK1#
MRESET
RESET_N
BUSPOWER_N
R_OSC
SS
PD_PMRESET
RT245 0_0201_5%
RT186 100K_0201_5%
TBT_RESET_N_EC <35,48>
TBTA_RESET_N <35>
RT189 0_0201_5%
VCC3V3_FLASH
RT199 0_0201_5%
PD_SS
CT158 0.22U_0402_10V6K
RT191 15K_0402_0.1%
+3VA_TBT
RT194 100K_0201_5%
PWR_BTN_DOCK1#
RT195 0_0201_5%
PWR_TB_DOCK# <48>
QV89 L2N7002WT1G_SC-70-3
the PD RST will keep low,
it will let PD work abnormal.[Ex. Type-c adapter plug in]
HRESET | D6 | Digital I/O | Hi-Z | Active high hardware reset input. Assertion will cause a reboot sequence. Ground pin when HRESET functionality will not be used.
c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).
LDO_3V3
R1 1%
ADC
CONFIG
R2 1%
If External SPI Connected use "Infinite Retry" Setting by pulling CONFIG (GPIO 8) to LDO_3V3
Figure 78. Factory Configuration Resistor Divider
Table 13. Factory Device Configuration Selection
DIV = R2/(R1+R2) (1)
DIV_min | DIV_max | Factory Device Configuration | Description
0.70 | 1.00 | 7 | Infinite boot retry from Flash to Host I/F cycles.
VCC3V3_FLASH
RT1093 10K_0201_1%
TBT_CONFIG
RT183 100K_0201_1%
VCC3V3_FLASH
MAIN : SA00003K820
2nd : SA00007P810
UT5
PD_HOLD#
PD_EE_CLK
PD_EE_DI
VCC /CS
/HOLD/IO3 DO/IO1
CLK /WP/IO2
DI/IO0 GND
PD_EE_CS#
PD_EE_DO
PD_EE_WP#
W25Q80DVZPIG_WSON8
<48> UPD_SMBDAT
<48> UPD_SMBCLK
RT200 0_0201_5% UPD_SMBDAT_R
RT201 0_0201_5% UPD_SMBCLK_R
Security Classification: Compal Secret Data
Issued Date: 2017/06/21
Deciphered Date: 2027/06/21
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Compal Electronics, Inc.
Title: P37-PD CONTROLLER
Size: Document Number: LA-G341P
Rev: 1.0(A00)
Date: Wednesday, June 06, 2018
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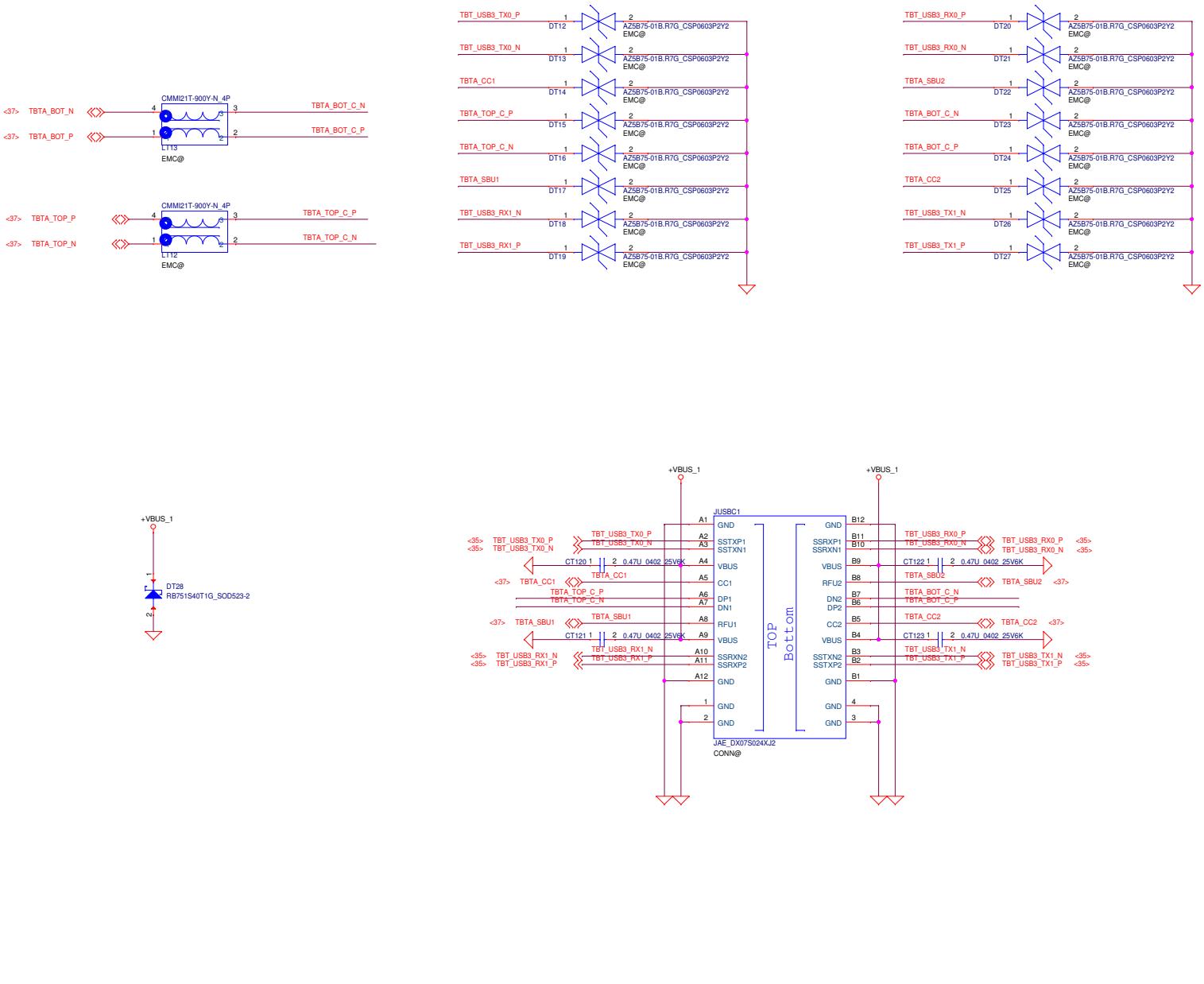

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P38-PD USB TYPE-C CONN.**

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C	LA-G341P	1.0(A00)

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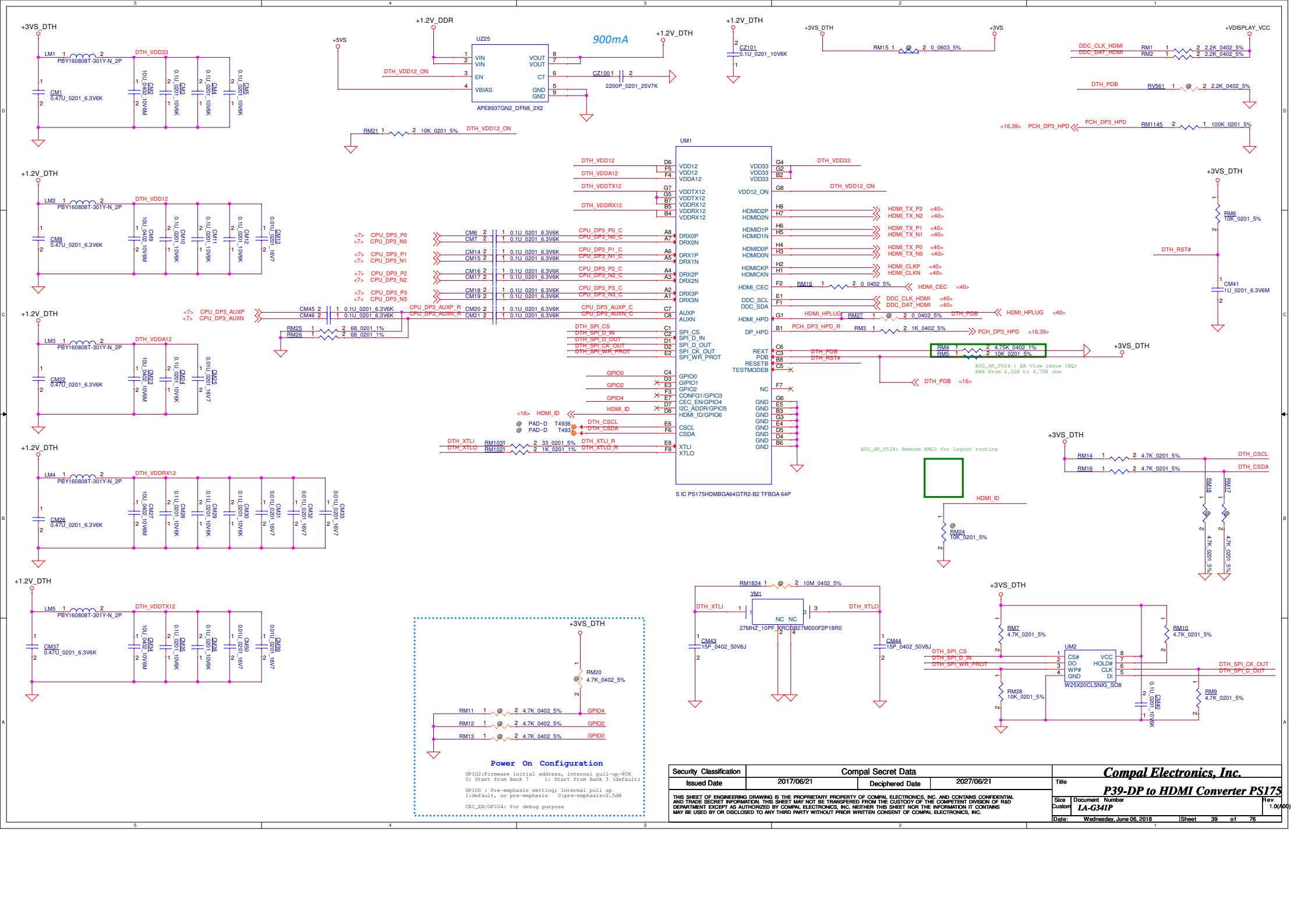
+3VS_DTH
+1.2V_DDR
+5VS
+1.2V_DTH
900mA
UZ25
APE8937GN2_DFN8_2X2
DTH_VDD12_ON
+1.2V_DTH
+3VS_DTH
+3VS
+VDISPLAY_VCC
DDC_CLK_HDMI
DDC_DAT_HDMI
DTH_PDB
PCH_DP3_HPD
UM1
S IC PS175HDMBGA64GTR2-B2 TFBGA 64P
DTH_VDD33
DTH_VDD12_ON
HDMI_TX_P2
HDMI_TX_N2
HDMI_TX_P1
HDMI_TX_N1
HDMI_TX_P0
HDMI_TX_N0
HDMI_CLKP
HDMI_CLKN
HDMI_CEC
DDC_SCL
DDC_SDA
HDMI_HPD
HDMI_HPLUG
DP_HPD
PCH_DP3_HPD_R
REXT
PDB
RESETB
TESTMODE
DTH_RST#
A00_4P_0524 : EA Vlow issue (EQ)
RM4 From 4.22K to 4.75K ohm
A00_4P_0528: Remove RM23 for layout routing
HDMI_ID
DTH_CSCL
DTH_CSDA
DTH_XTLI
DTH_XTLO
27MHZ_10PF_XRCGB27M000F2P18R0
UM2
W25X20CLSNIG_SO8
DTH_SPI_CS
DTH_SPI_D_IN
DTH_SPI_WR_PROT
DTH_SPI_CK_OUT
DTH_SPI_D_OUT
Power On Configuration
GPIO2:Firmware initial address, internal pull-up-80K
0: Start from Bank 7 1: Start from Bank 3 (default)
GPIO0 : Pre-emphasis setting; Internal pull up
1:default, no pre-emphasis 0:pre-emphasis=2.5dB
CEC_EN/GPIO4: For debug purpose
Security Classification
Compal Secret Data
Issued Date
2017/06/21
Deciphered Date
2027/06/21
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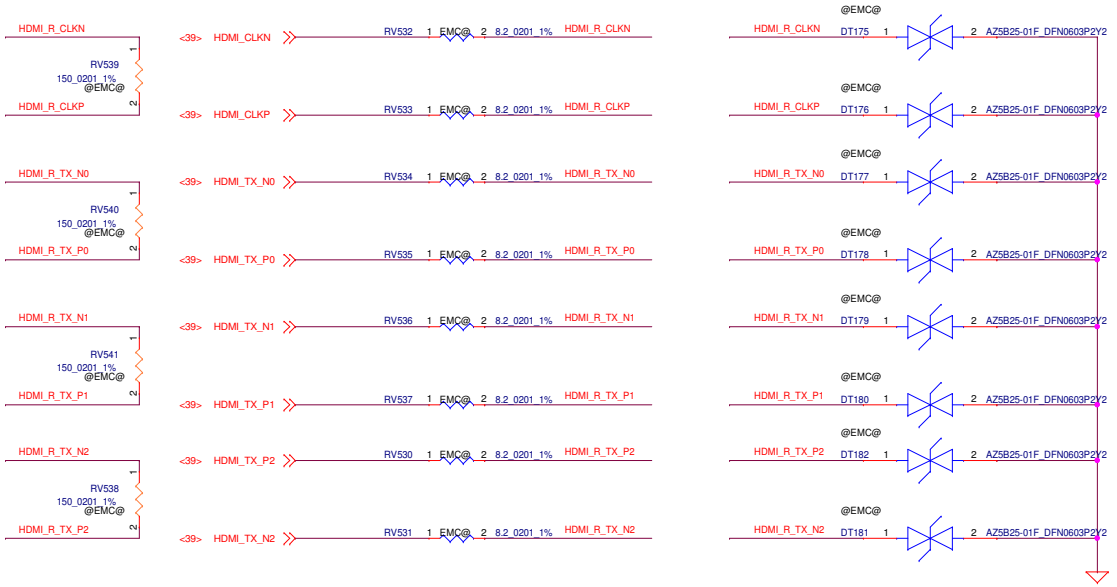
Compal Electronics, Inc.
Title
P39-DP to HDMI Converter PS175
Size
Custom
Document Number
LA-G341P
Rev
1.0(A00)
Date: Wednesday, June 06, 2018
Sheet 39 of 76

HDMI change to CPU to PS185 to CONN

Place between ESD and CM-Choke

Place close to JHDMI1



HDMI DDC

HDMI conn

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

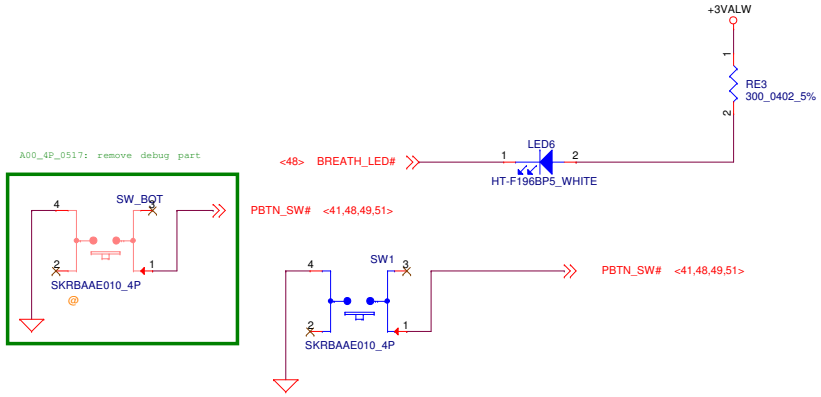
Compal Electronics, Inc.

Title: **P40-HDMI Connector**

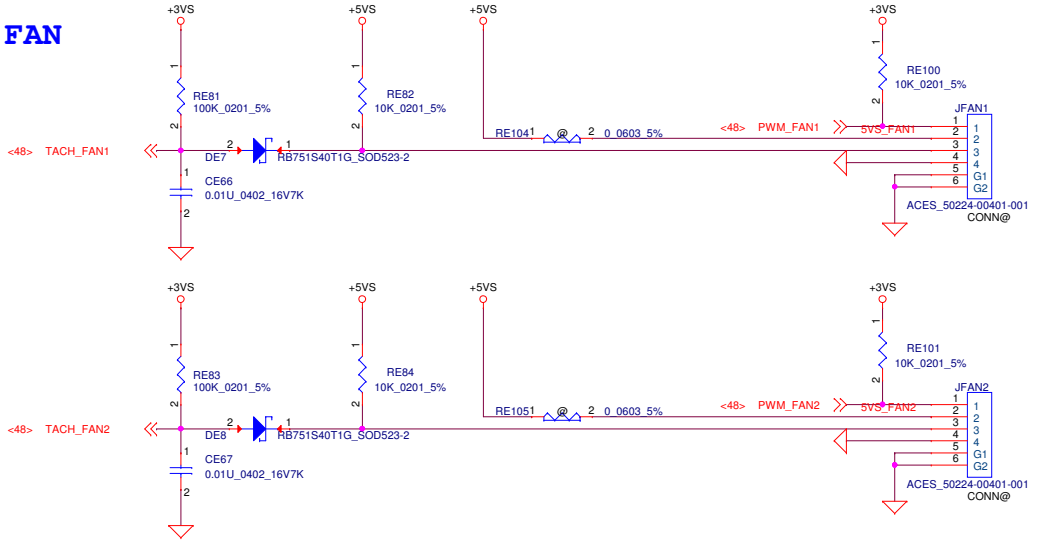
Size	Document Number	Rev
Custom	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 40 of 76

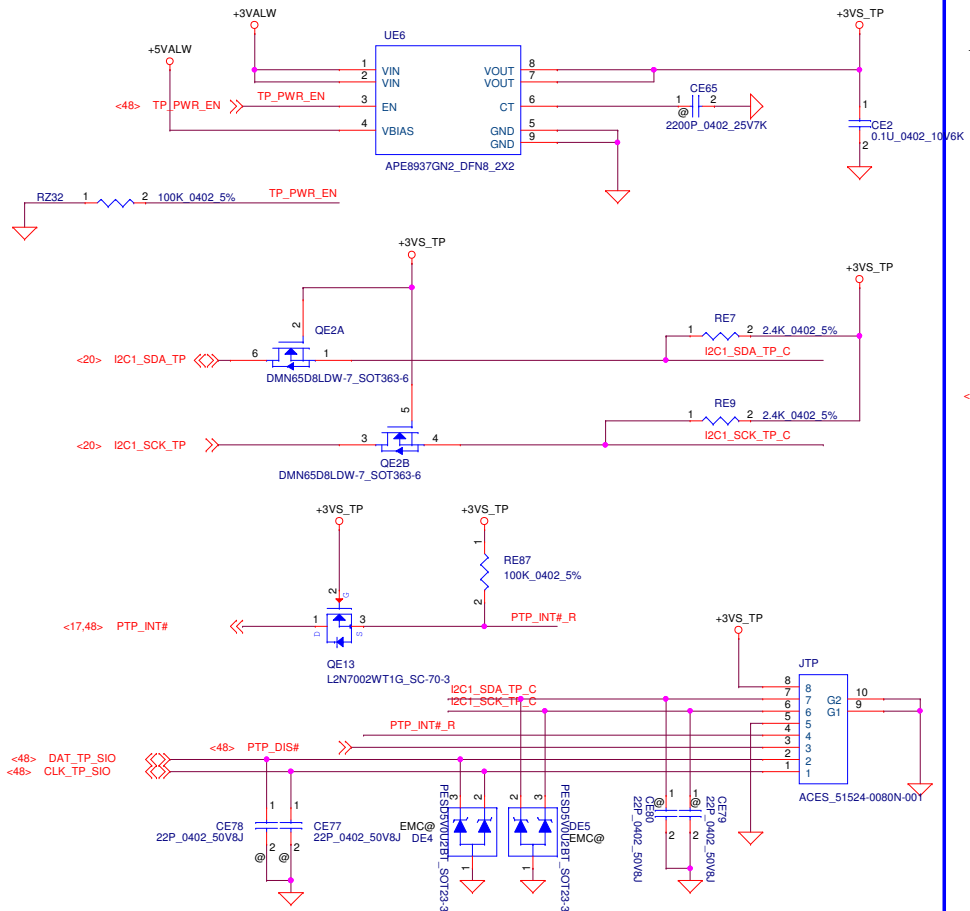
Power Button and LED



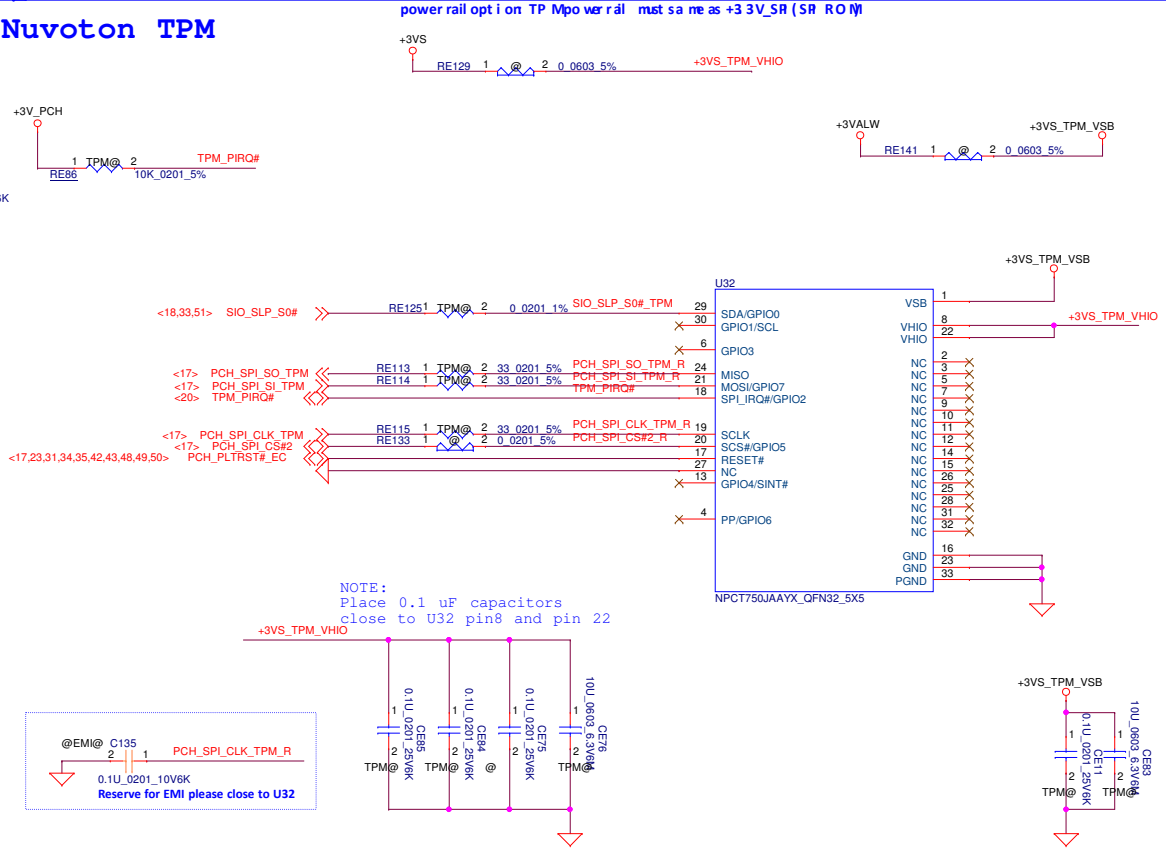
PWM FAN



Touch pad



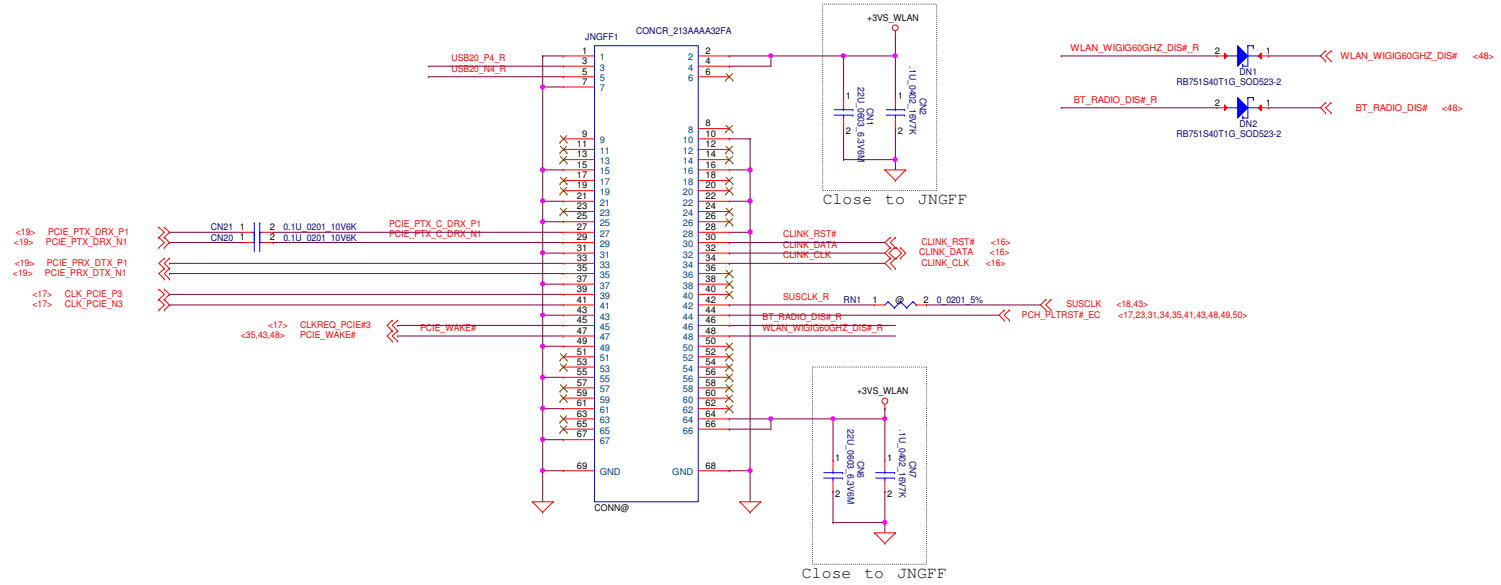
Nuvoton TPM



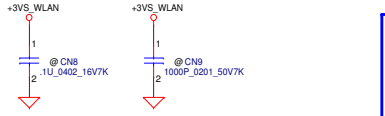
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

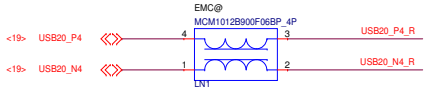
Compal Electronics, Inc.			
Title	P41-FAN/TP/TPM/SW		
Size: Custom	Document Number: LA-G341P		Rev: 1.0(A00)
Date: Wednesday, June 06, 2018	Sheet 41 of 76		

M.2 Slot-A Key-A (WLAN + BT)



Reserve for EMI





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

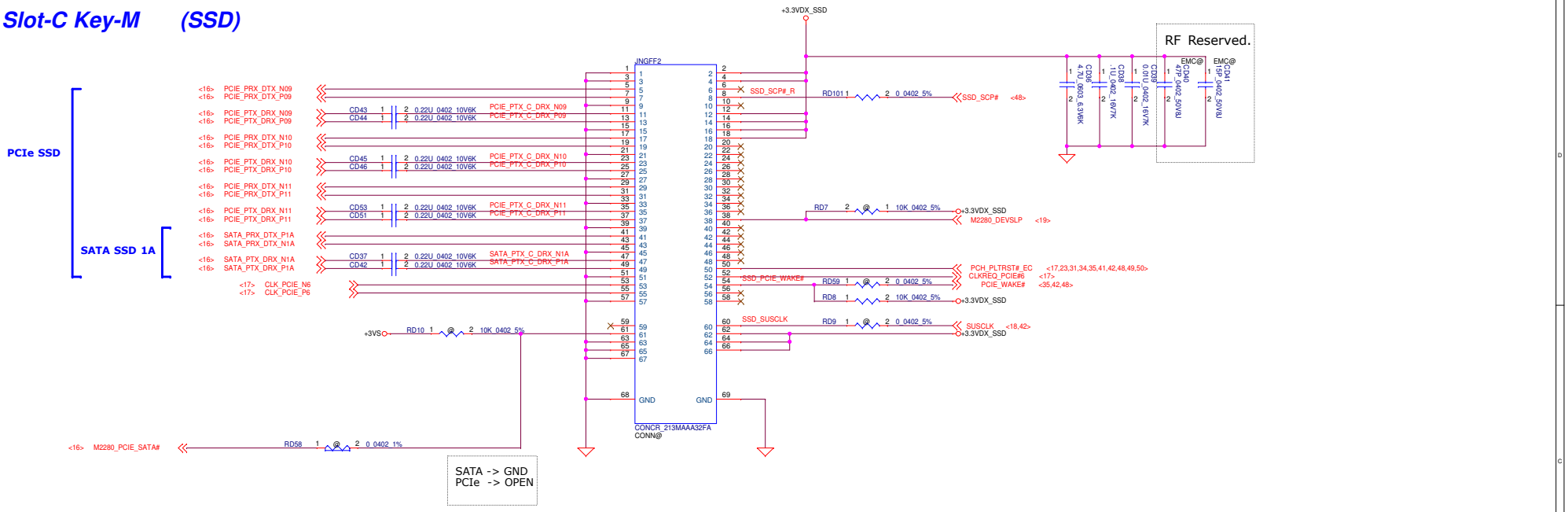
Compal Electronics, Inc.

Title: P42-NGFF-WLAN/BT

Size	Document Number	Rev
C	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 42 of 76

M.2 Slot-C Key-M (SSD)



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P43-NGFF-SSD**

Size	Document Number	Rev
C	LA-G341P	1.0(A00)

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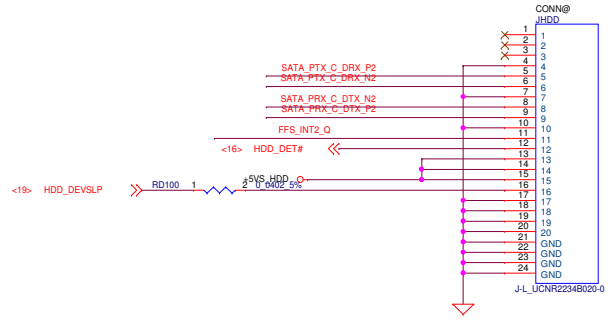
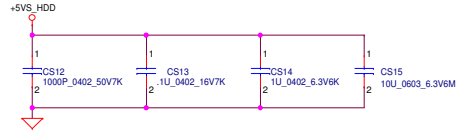
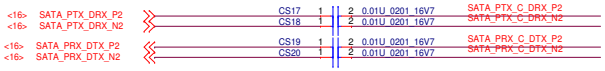
HDD CONN



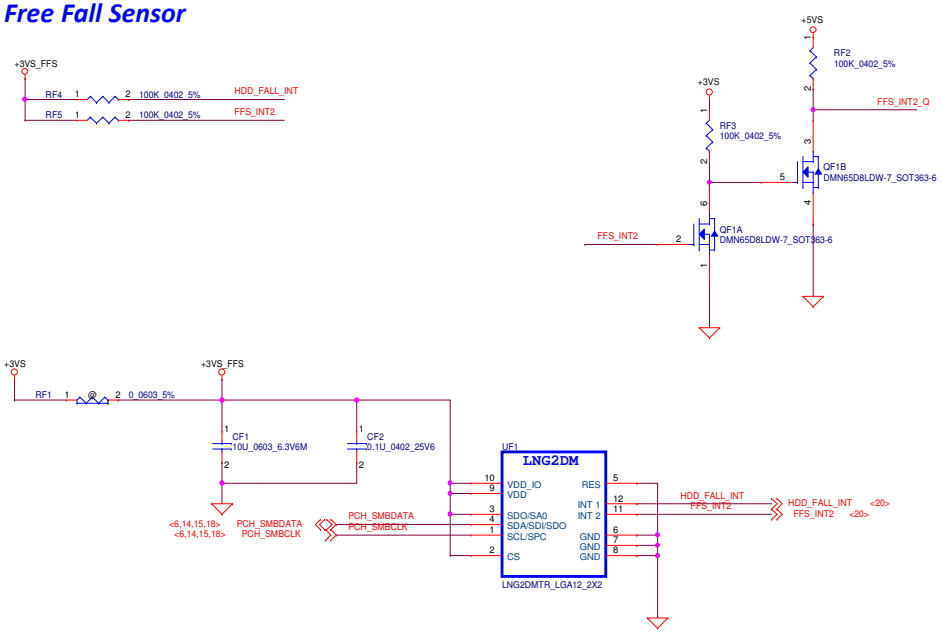
Place near HDD CONN (JHDD1)





BYPASS Circuit

Free Fall Sensor



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P44-HDD / FFS**

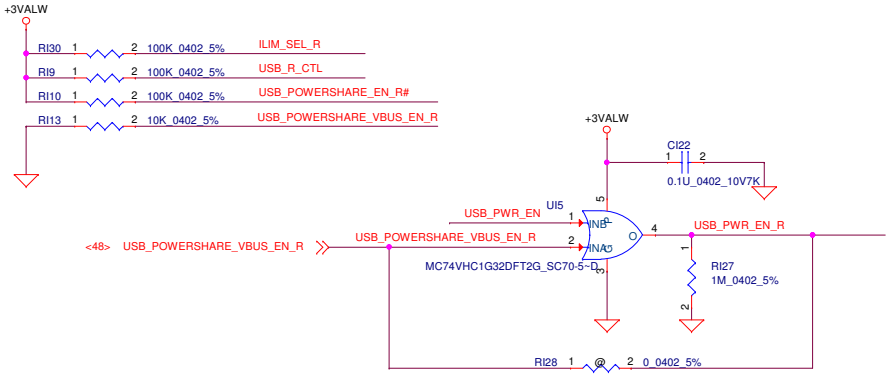
Size	Document Number	Rev
C	LA-G341P	1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 44 of 76

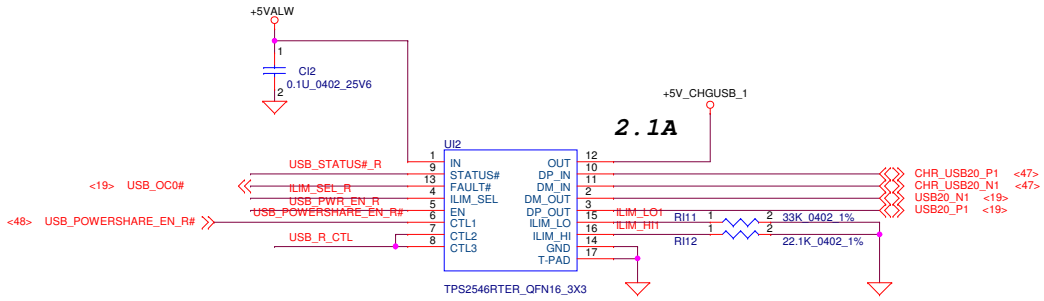
USB Powershare

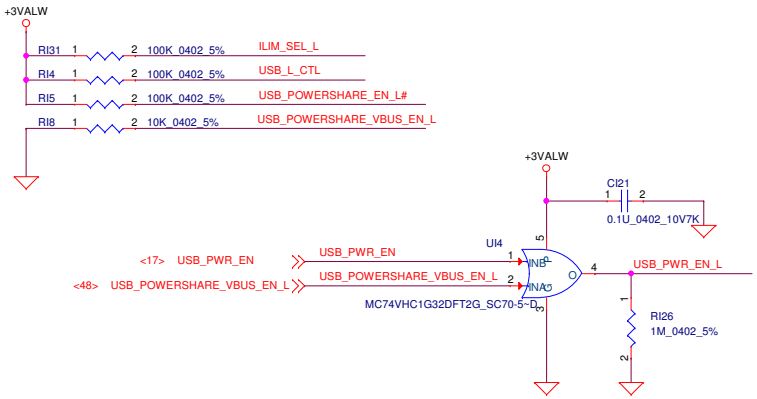
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

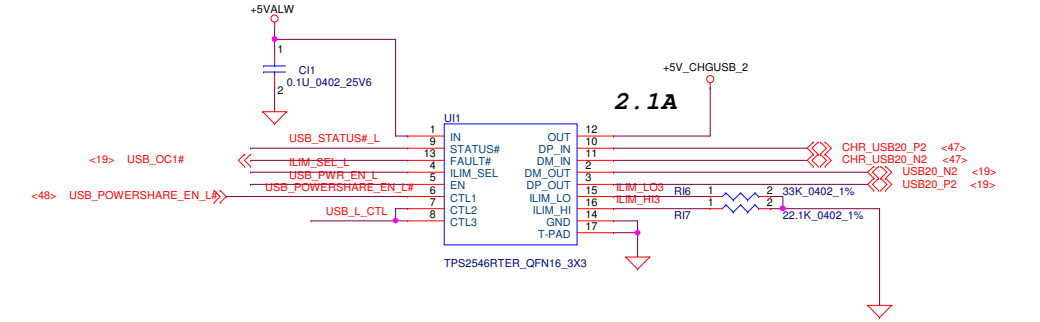


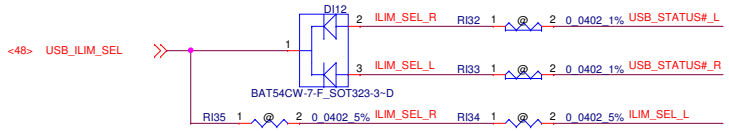
USB3.1 / USB2.0 Port1 (Right Side)





USB3.1 / USB2.0 Port2 (Left Side)





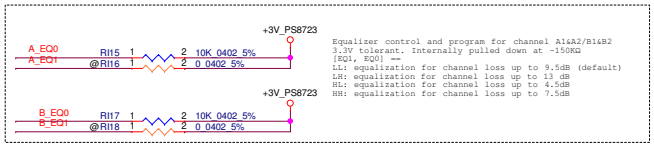
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

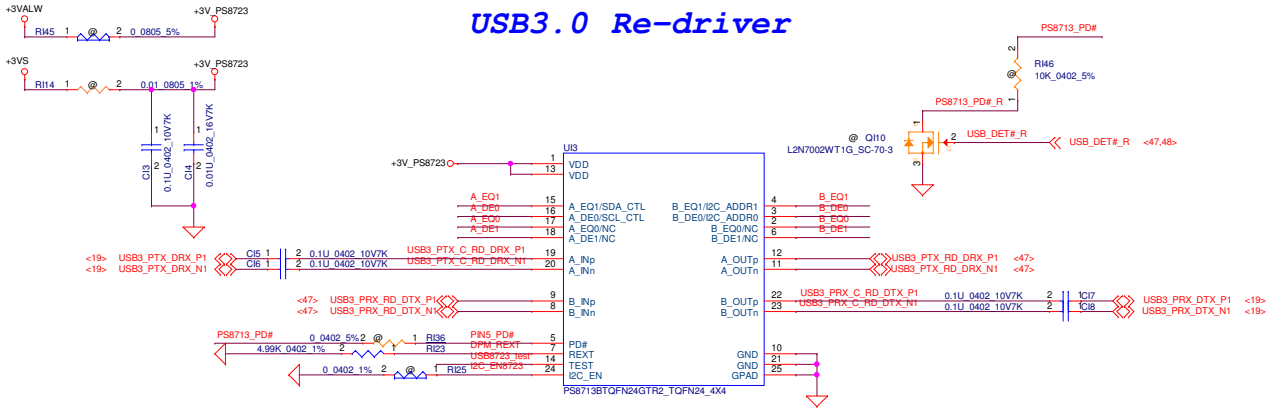
Title: P45-USB Powershare

Size | Document Number: LA-G341P | Rev: 1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 45 of 76



USB3.0 Re-driver



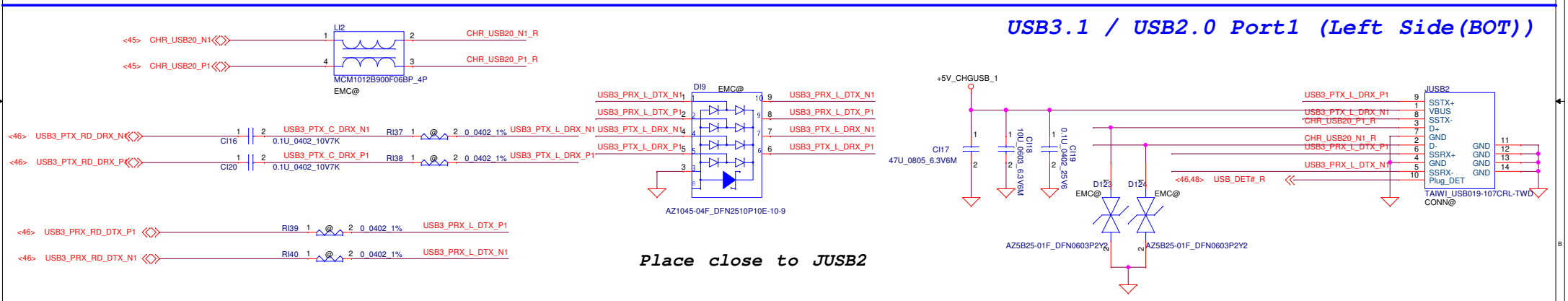
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

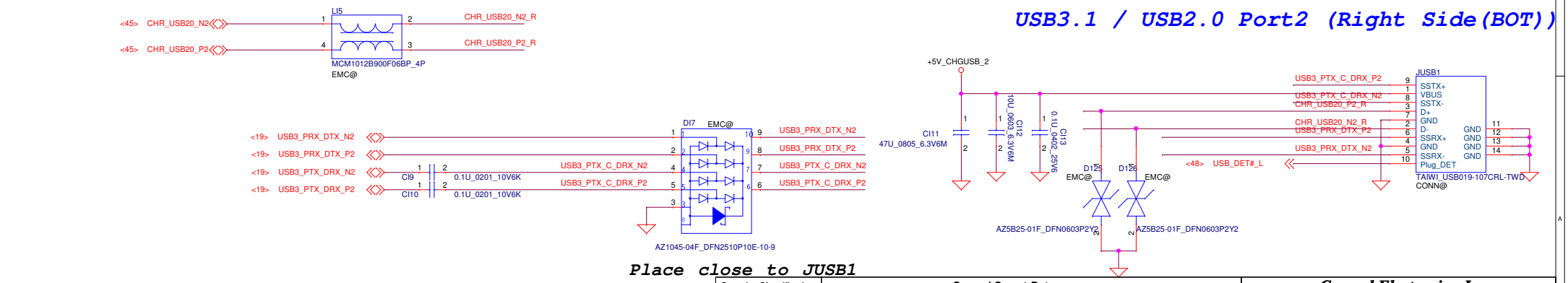
Compal Electronics, Inc.

Title: P46-USB3.1 retimer

Size	Document Number	Rev
Custom		1.0(A00)

Date: Wednesday, June 06, 2018 Sheet 46 of 76





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.	
Title	P47-USB3.1/USB2.0 conn
Size	Document Number: LA-G341P
Rev	1.0(A00)
Date:	Wednesday, June 06, 2018
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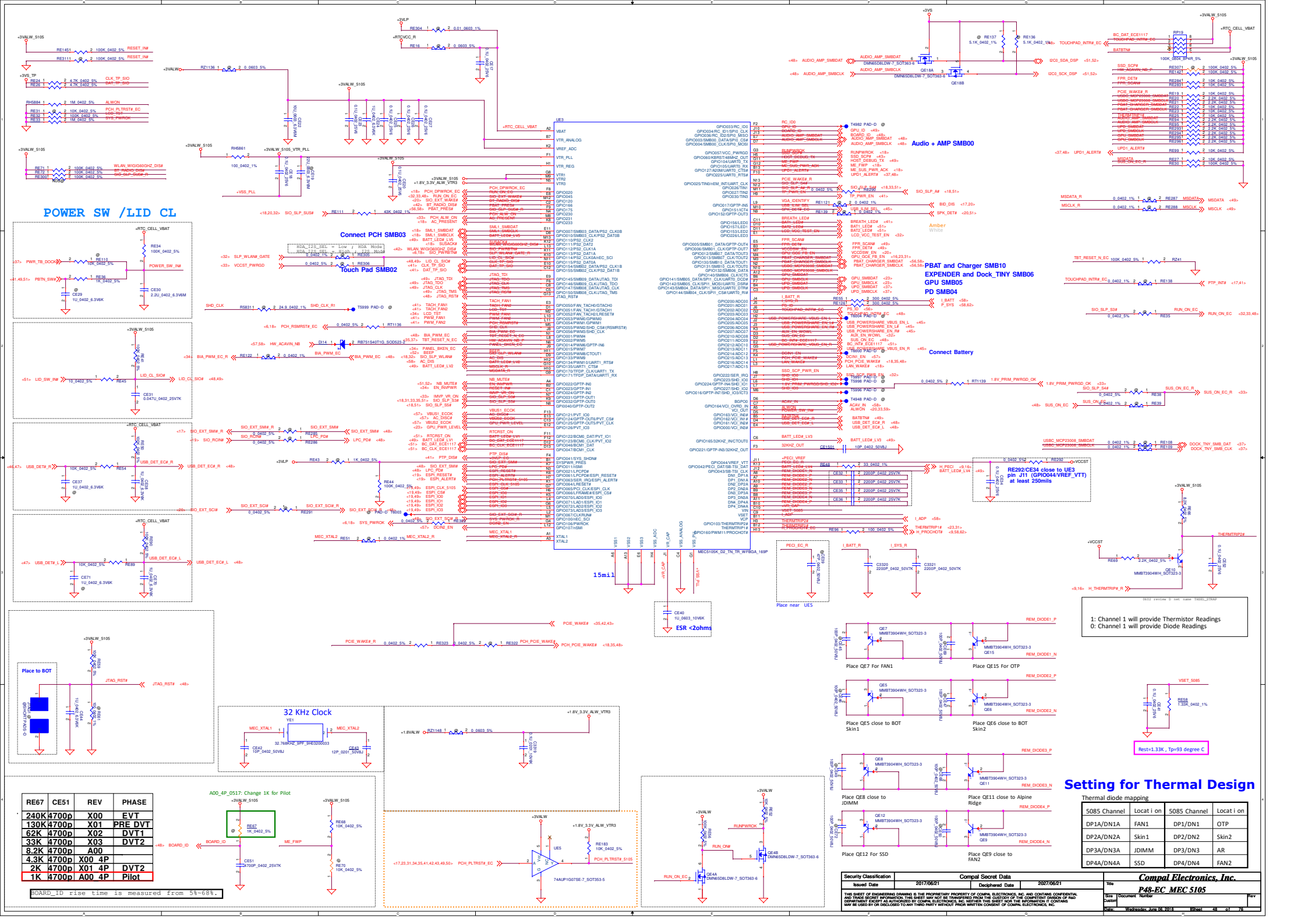

RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	
4.3K	4700p	X00_4P	
2K	4700p	X01_4P	DVT2
1K	4700p	A00_4P	Pilot

Setting for Thermal Design

Thermal diode mapping

5085 Channel	Locat i on	5085 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDIMM	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2

Security Classification	Compal Secret Data	
Issued Date	2017/06/21	Deciphered Date 2027/06/21

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Compal Electronics, Inc.

Title: P48-EC MEC 5105

Size: Custom | Document Number: | Rev:

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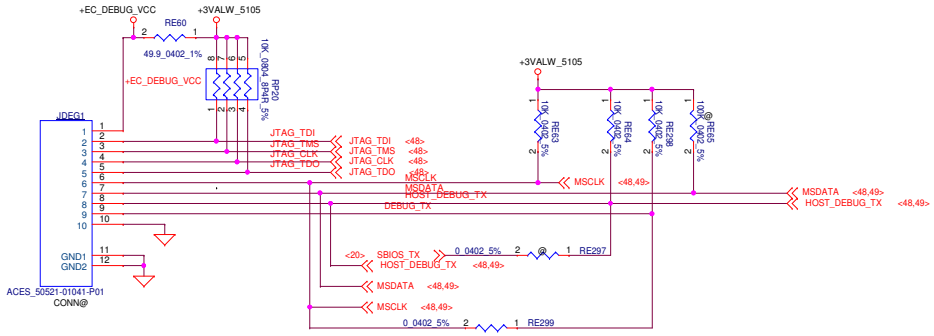
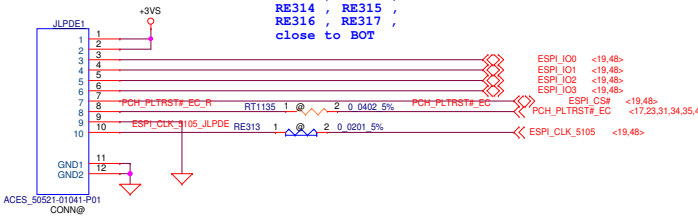
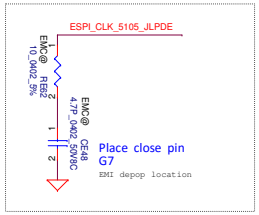
JDEG



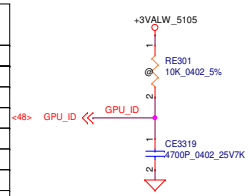
JLPDE

RE312 , RE313 ,
RE314 , RE315 ,
RE316 , RE317 ,
close to BOT

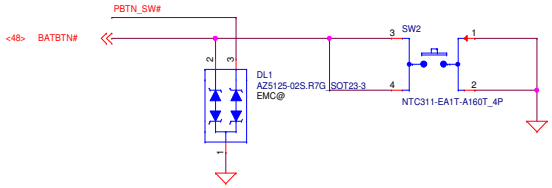




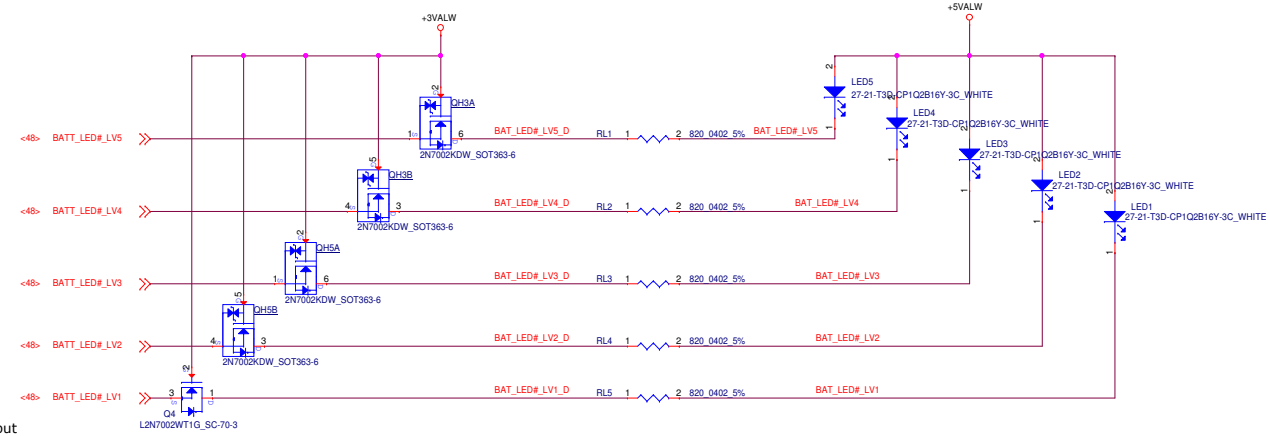
RE301	CE3319	REV
240K	4700p	i3 CPU/UMA
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	



BATT LED Power Button



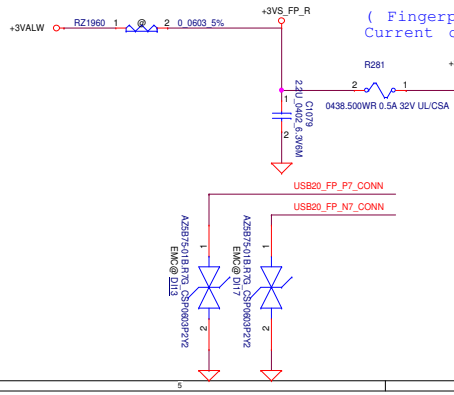
Bat tery Gauge LED

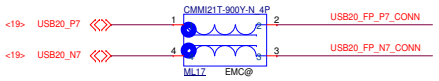


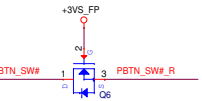
EC GPIO set to OD output

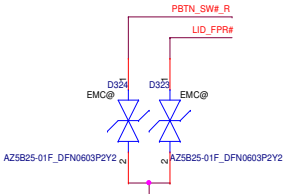
Finger Print circuit

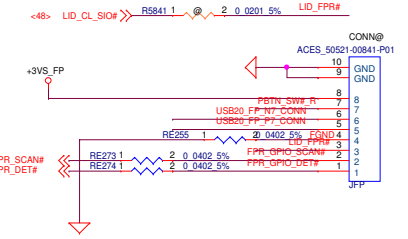
(Fingerprint Reader)
Current capability: 3.3V 150mA











Fingerprint Reader CONN

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P49-BAT LED/BUZZER/FP

Size	Document Number	Rev
C	LA-G341P	1.0(A00)

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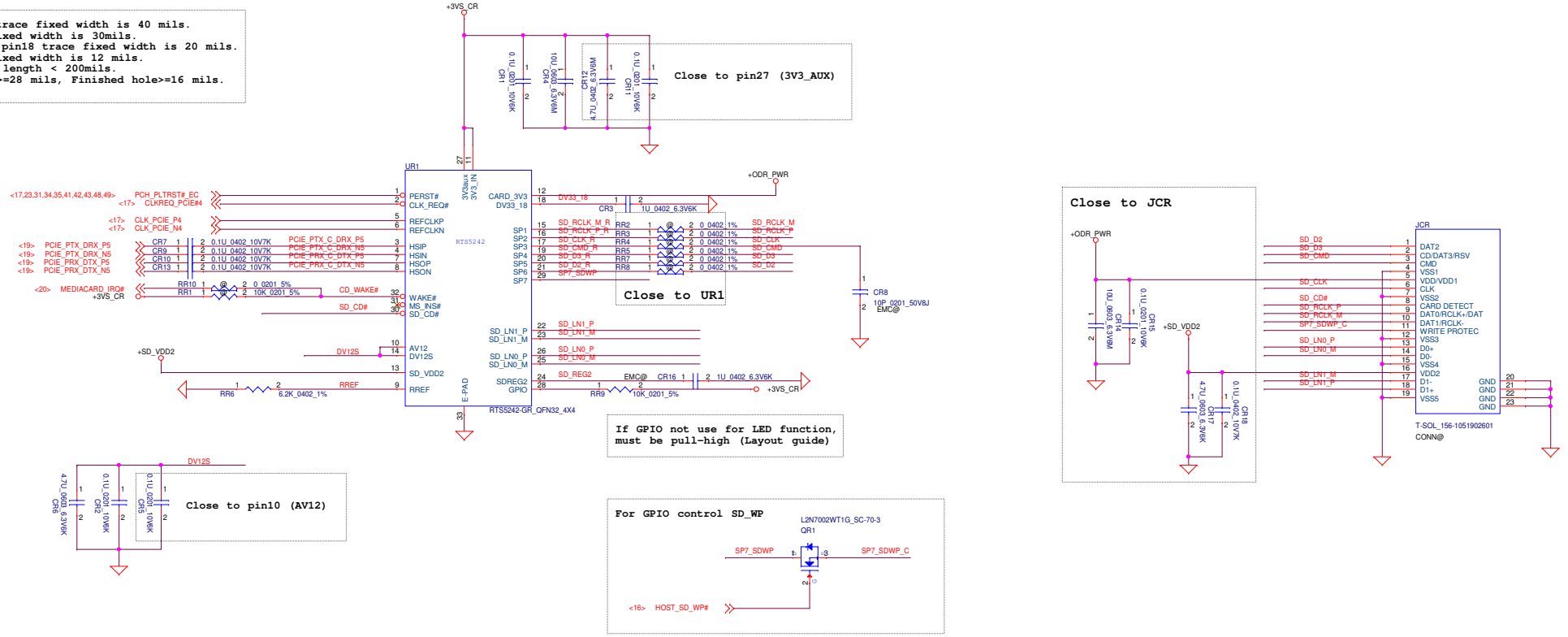
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

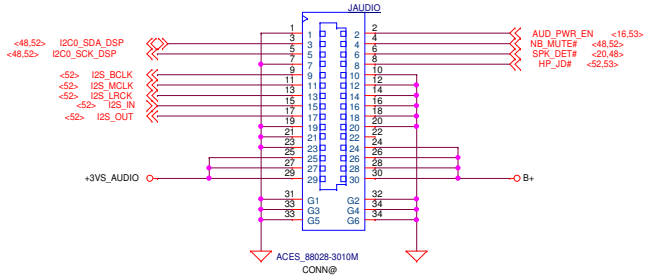
Compal Electronics, Inc.

Title: **P50-Card Reader**

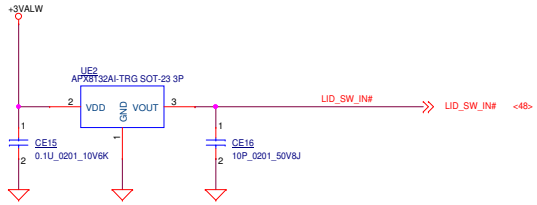
Size	Document Number	Rev
		1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 50 of 76

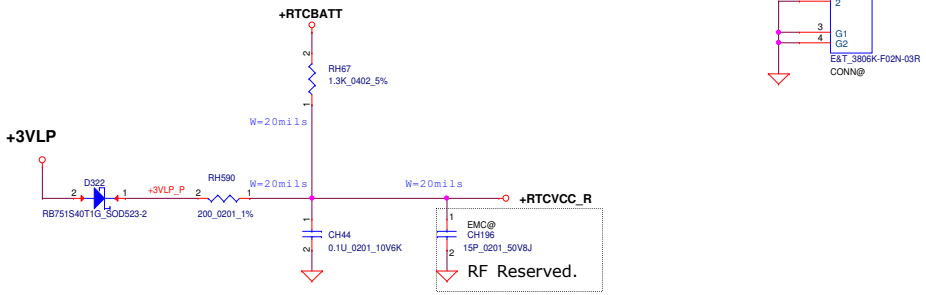
AUDIO Board Conn.



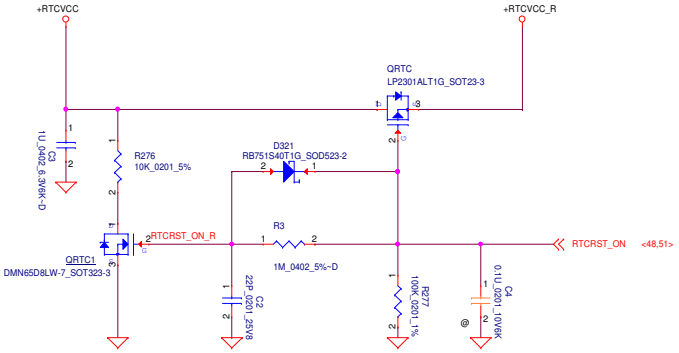
Lid Switch



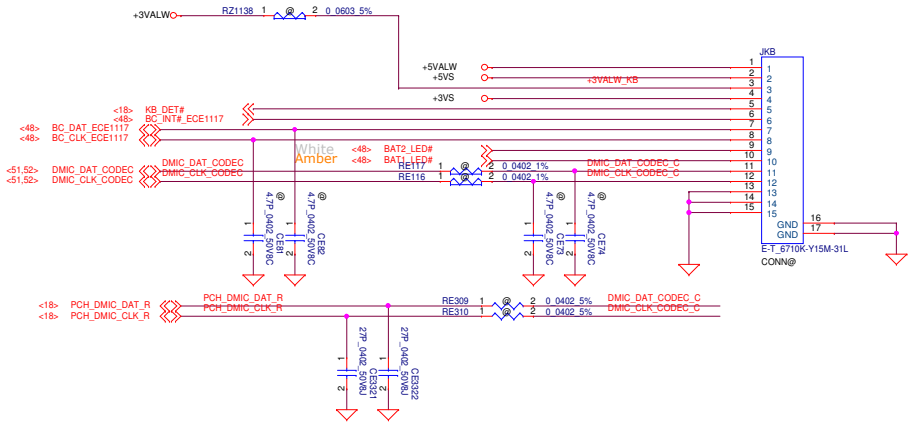
RTC Battery With Charge Function

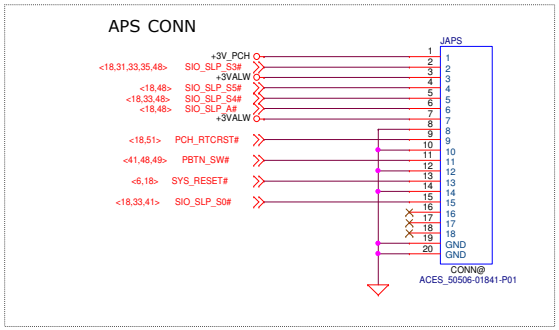


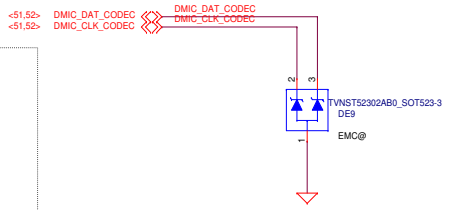
Default: OD EC drives GPIOs to LOW to turn off power to VCCRTC.



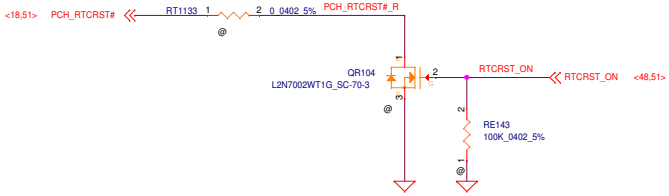
Keyboard Controller board + DMIC







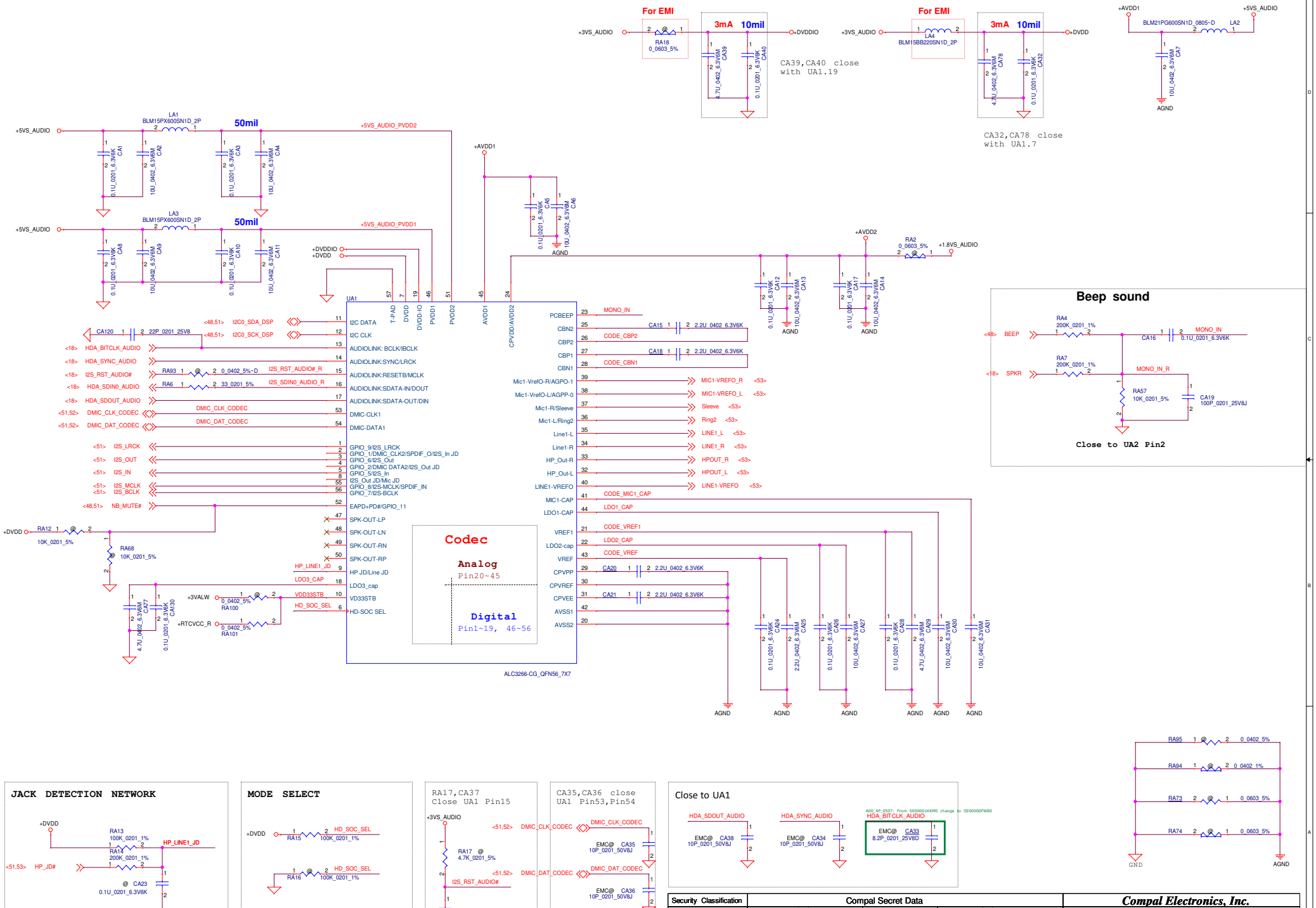
follow Intel Keep old RTC



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title: P51-CONN/Lid/RTC			
Size	Document Number: LA-G341P		Rev: 1.0(A00)
Date: Wednesday, June 06, 2018	Sheet 51 of 76		

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

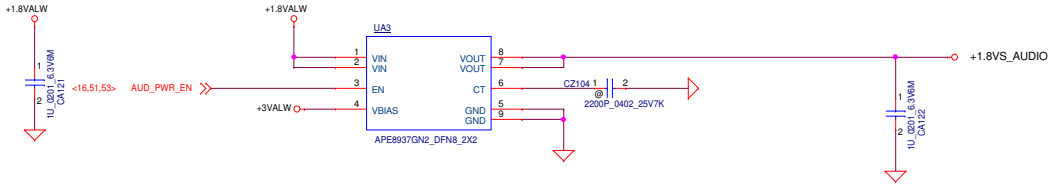
Compal Electronics, Inc.

Title: P52-ALC3266

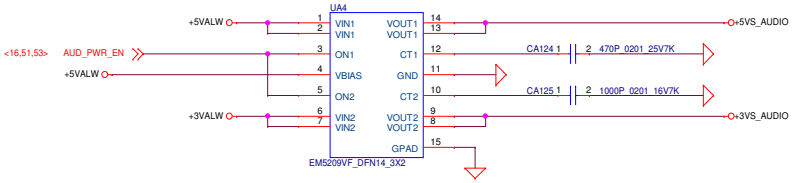
Size | Document Number: LA-G341P | Rev: 1.0(A00)

Date: Wednesday, June 06, 2018 | Sheet 52 of 76

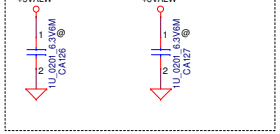
+1.8VALW To +1.8VS_AUDIO



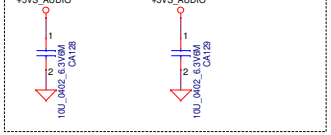
+5VALW and +3VALW To +5VS_AUDIO and +3VS_AUDIO



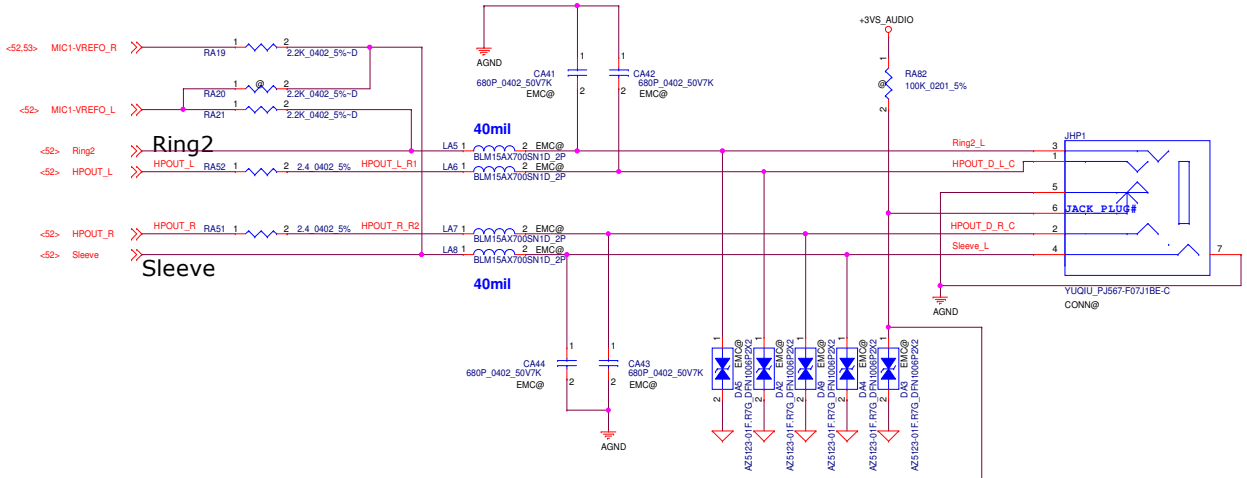
Close UA4



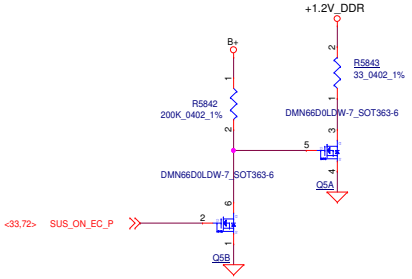
Close UA4

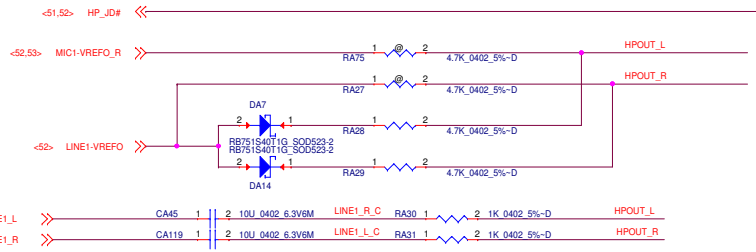


Universal Audio Jack



1.2V DDR dischager





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

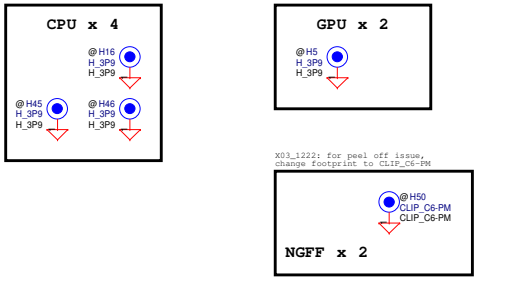
Compal Electronics, Inc.

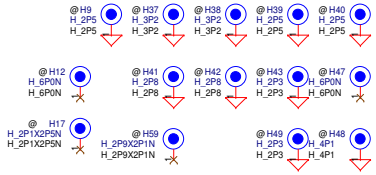
Title: P53-Audio_Jack

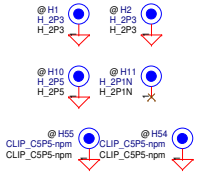
Size	Document Number	Rev
	LA-G341P	1.0(A00)

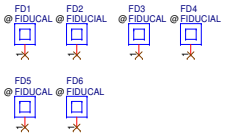
Date: Wednesday, June 06, 2018 | Sheet 53 of 76

Screw Hole









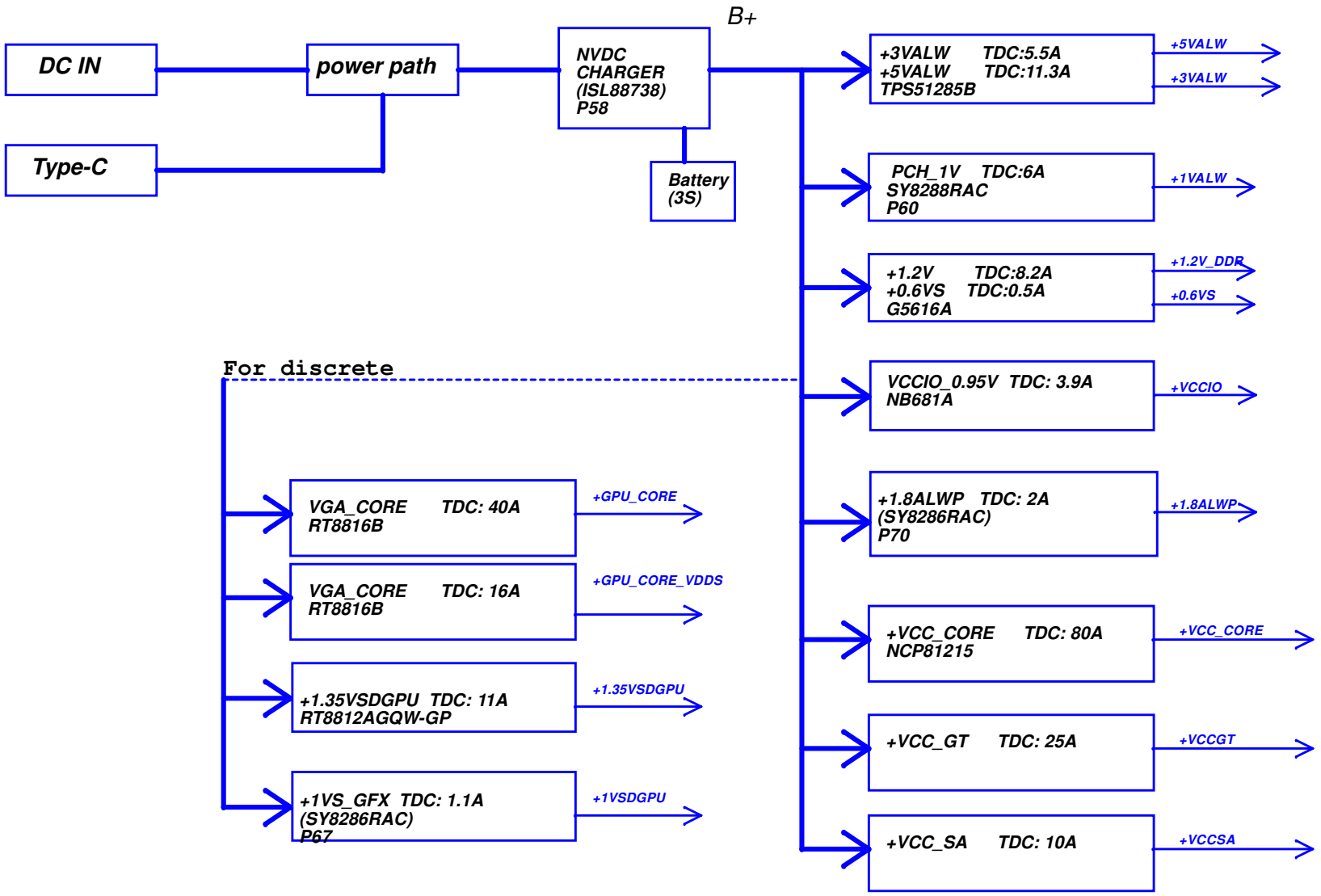
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P54-Screws**

Size	Document Number	Rev
		1.0(A00)

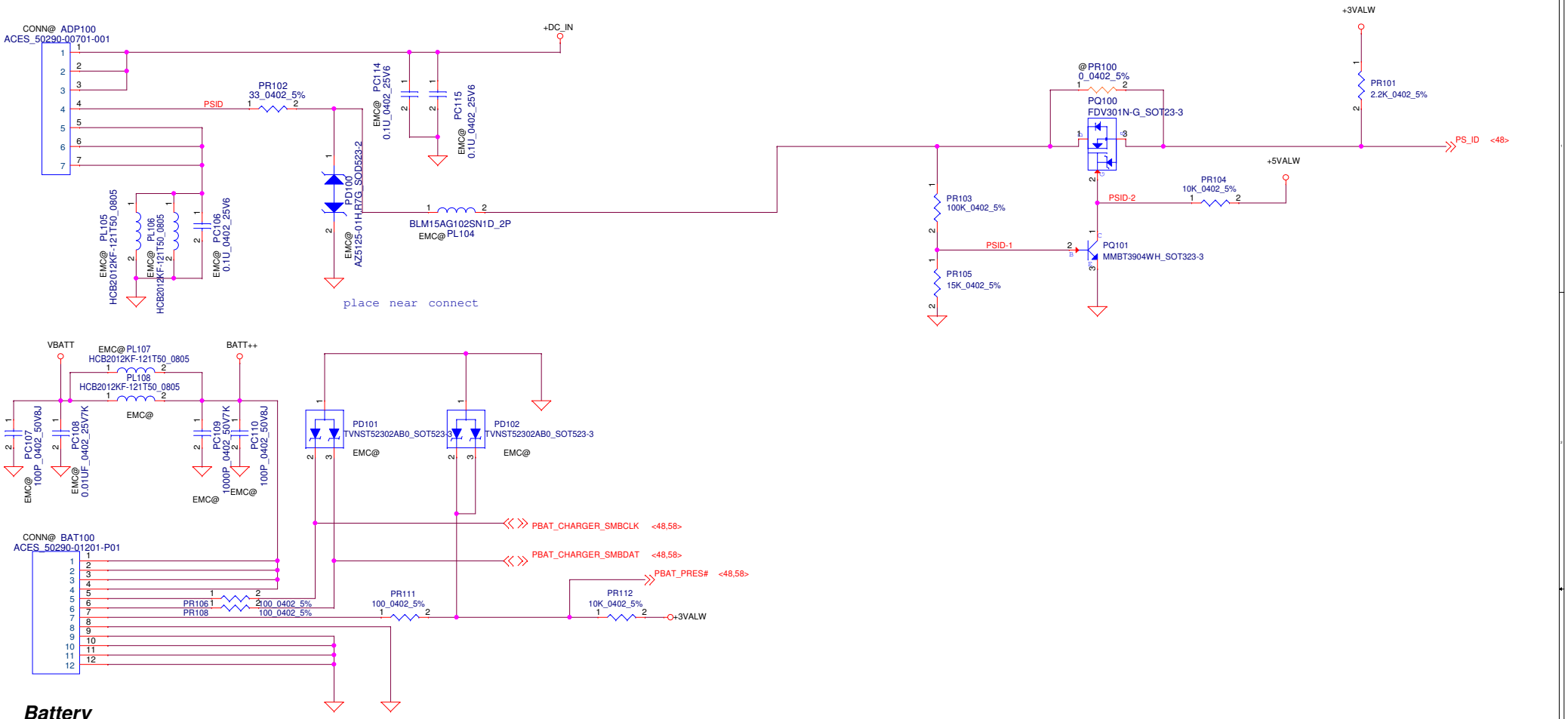
Date: Wednesday, June 06, 2018 | Sheet 54 of 76



@ : Nopop Component
@DIS@ : Nopop Component
DIS@: POP for discrete GPU SKU

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.	
Title	P55-Power Block Diagram
Size	Document Number / Rev 0.1(X00)
Date: Wednesday, June 06, 2018	Sheet 55 of 74



Battery
(3S2P) 97W
(3S1P) 56W

JIMBTY battery connector

SMART
Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Smart Adapter circuit (39.1)

Compal Electronics, Inc.
Title: P56-PWR_DCIN / BATT CONN / OTP
Size: Document Number: LA-F541P
Rev: 0.1(X00)
Date: Wednesday, June 06, 2018
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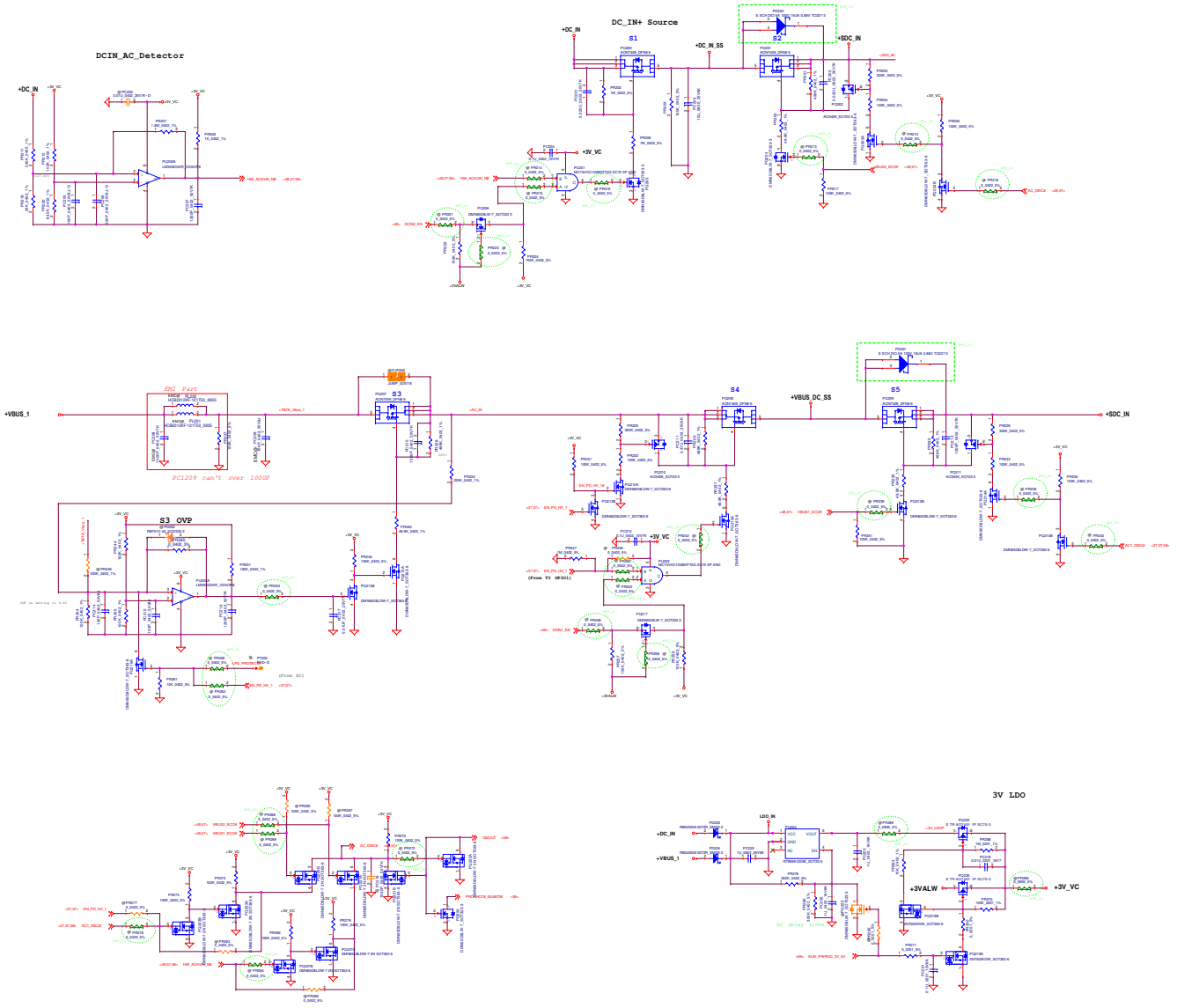
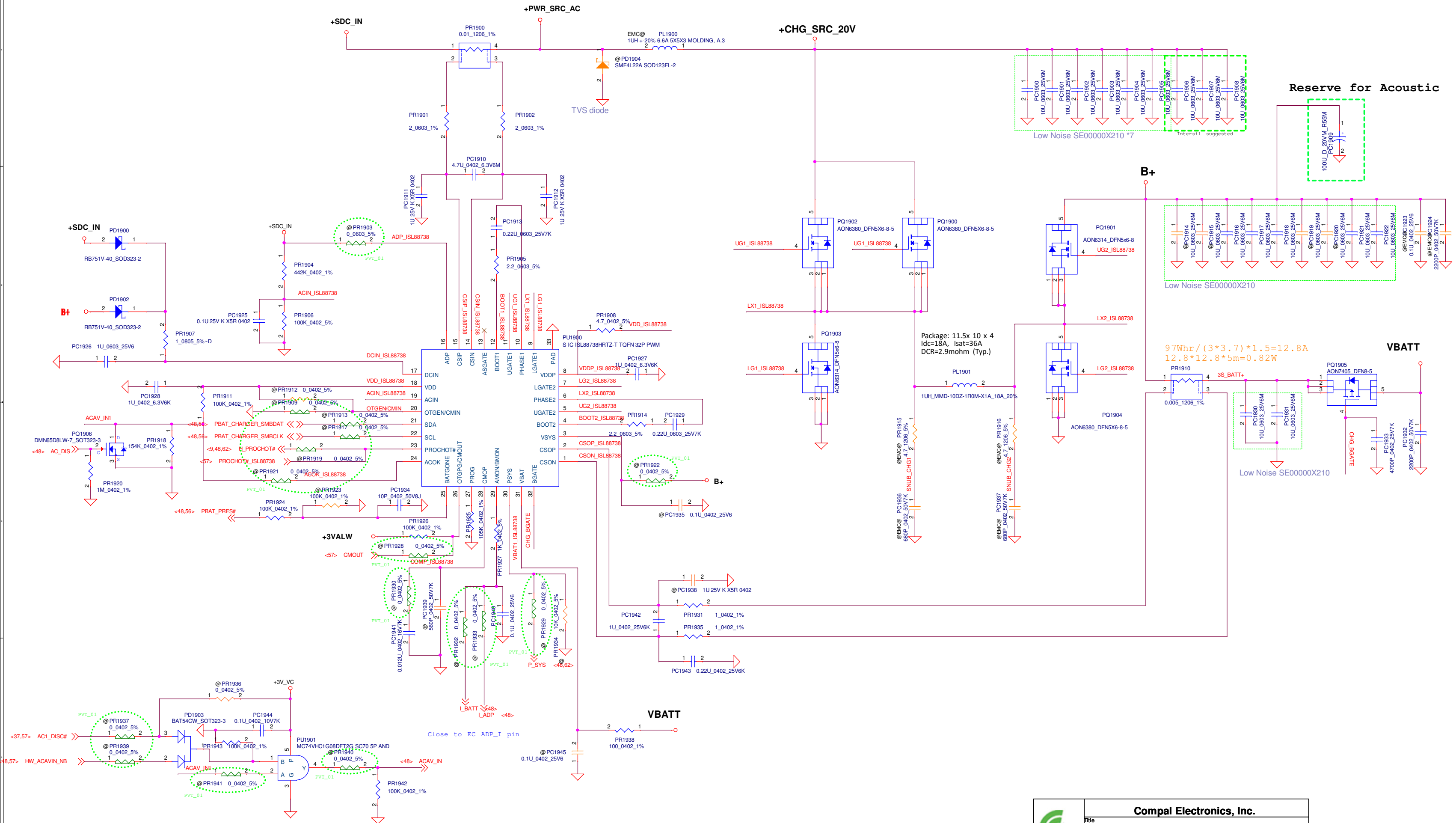
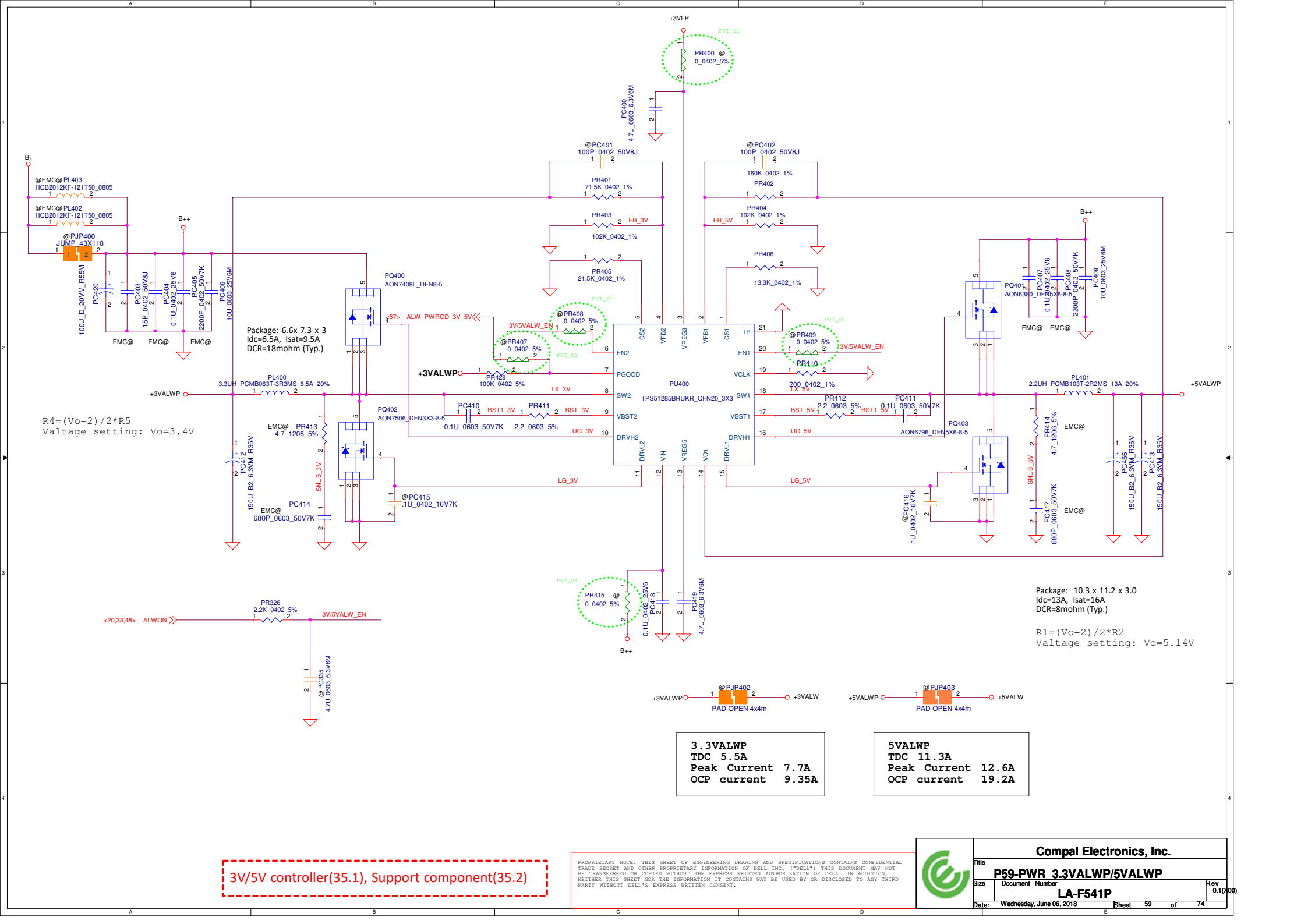


	P57-PWR Switch		
Size	Document Number		Rev
Custom	LA-F561P		0.1(X)
Date:	Wednesday, June 05, 2013	Sheet	47 of 53



Compal Electronics, Inc.		
Title	P58-PWR_CHARGER(ISL88738)	
Size	Document Number: LA-F541P	Rev: 0.1(X00)
Date: Wednesday, June 06, 2018	Sheet 58 of 74	



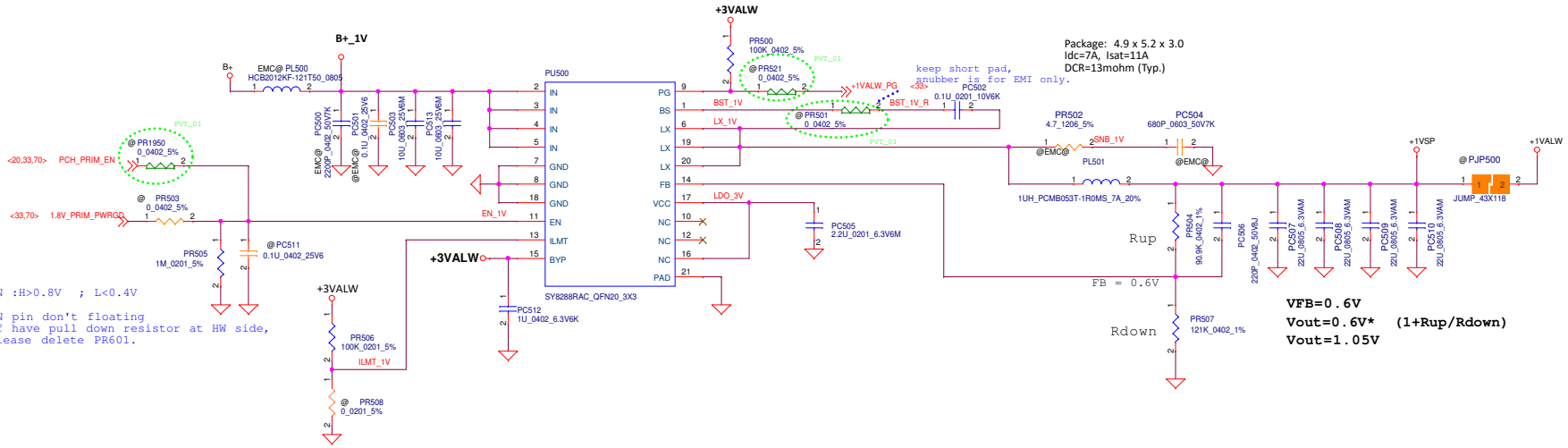
Compal Electronics, Inc.

Title: P59-PWR 3.3VALWP/5VALWP

Size: | Document Number: LA-F541P | Rev: 0.1(X00)

Date: Wednesday, June 06, 2018 | Sheet 59 of 74

+1VSP
TDC 6A
Peak Current 8.2A
OCP current 12A(fix)



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.05V

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

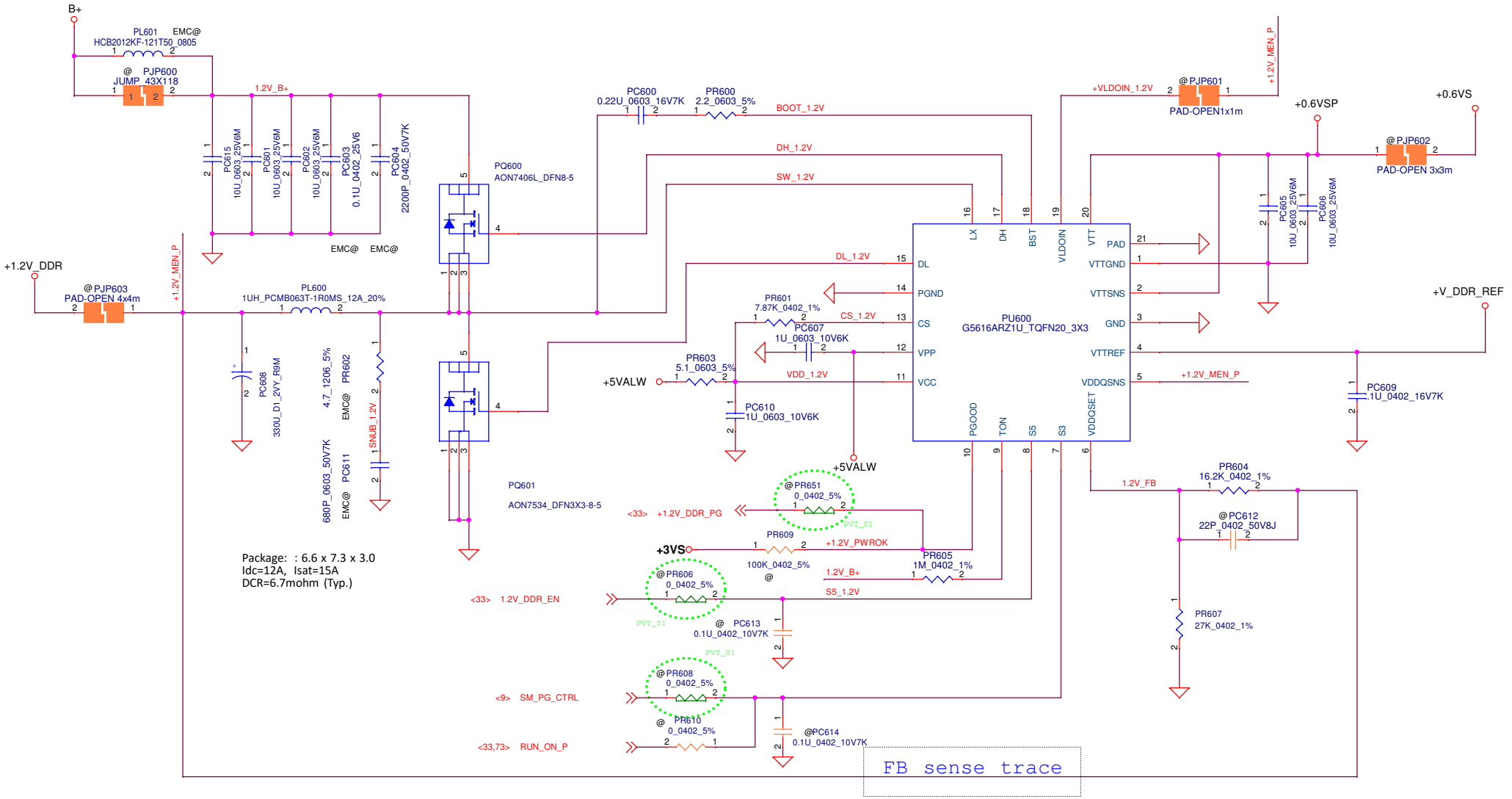
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P60-PWR_PCH_1V(SY8288RAC)**

Size	Document Number	Rev
	LA-F541P	0.1(X00)

Date: Wednesday, June 06, 2018 Sheet 60 of 74



1.2Volt +/- 5%
TDC 8.2A
Peak Current 15.4A
OCP current

0.6Volt +/- 5%
TDC 0.5A
Peak Current 0.7A
OCP Current 0.85A

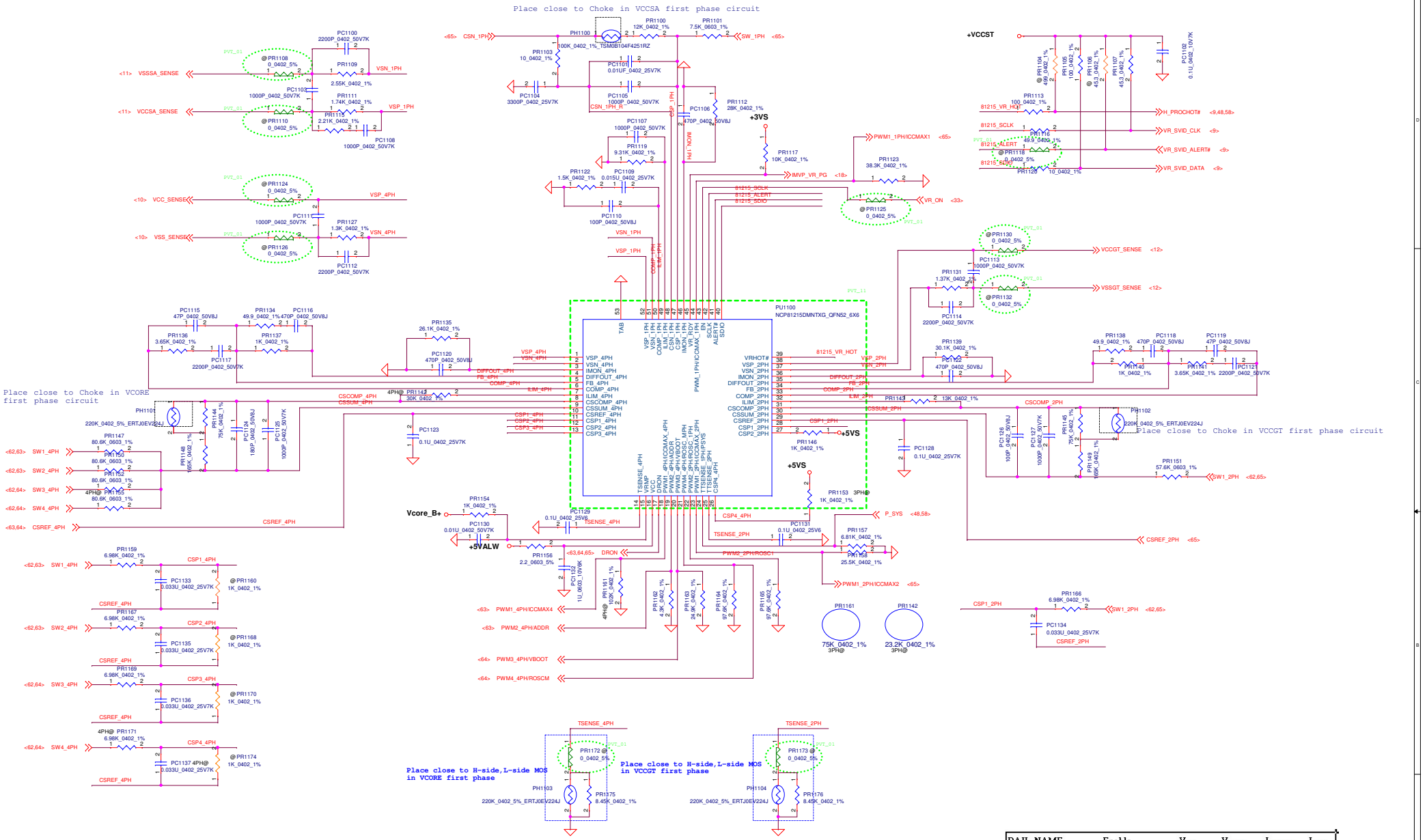
DDR controller(35.3), Support component(35.4)

Compal Electronics, Inc.

Title: P61-PWR_+1.2V_MEN/+0.6V_DDR

Size | Document Number: LA-F541P | Rev: 0.1(X00)

Date: Wednesday, June 06, 2018 | Sheet 61 of 74



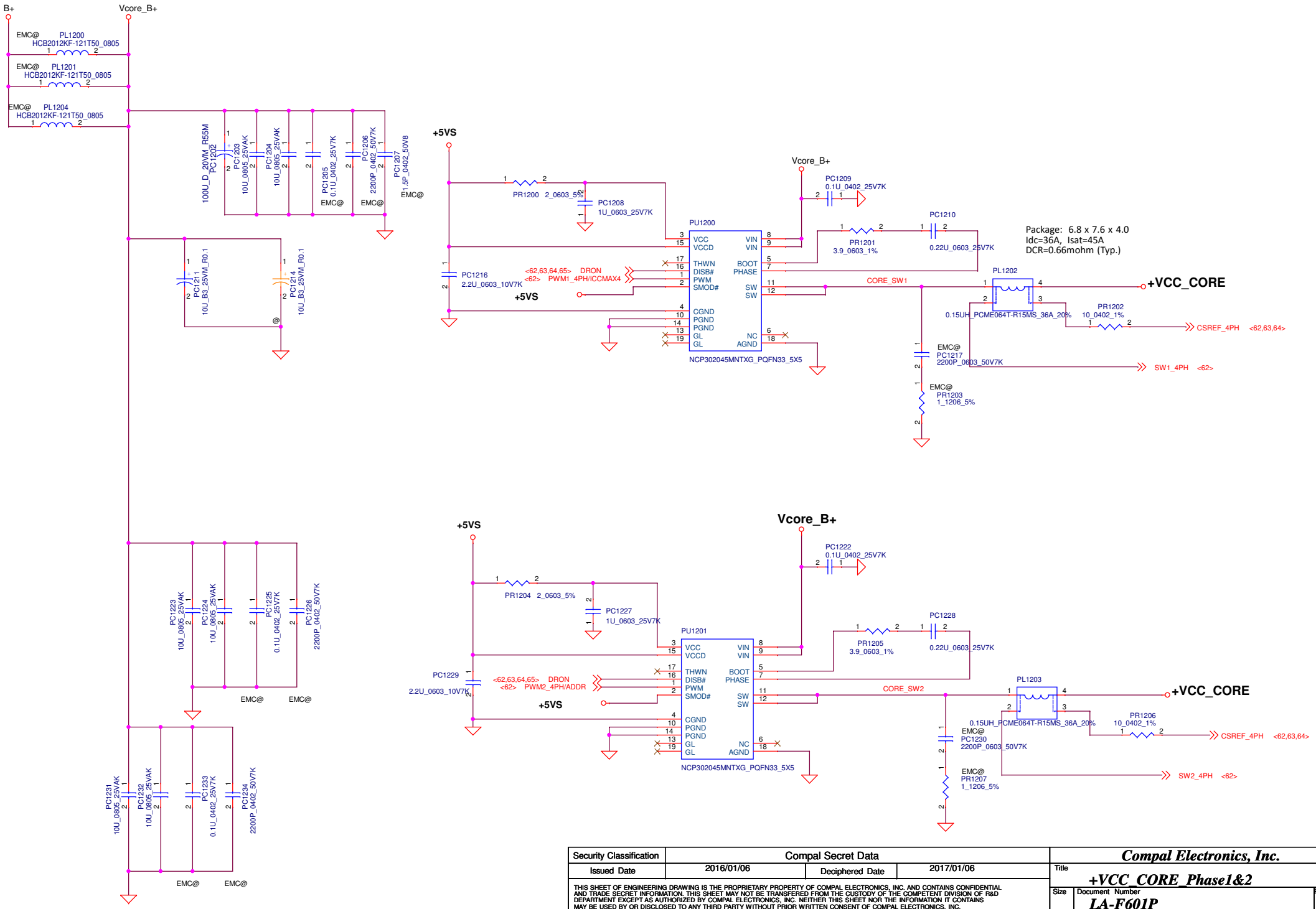
RAIL NAME	Enable	V_{IN}	V_{OUT}	I_{CCMax}	I_{PL2}
Vcc (IMVP8)	VR_EN	VDC	SVID	128.0 A	80.0 A
VccGT (IMVP8)	VR_EN	VDC	SVID	32.0 A	25.0 A
VccSA (IMVP8)	VR_EN	VDC	SVID	11.1 A	10.0 A

Compal Electronics, Inc.

Title: NCP81215

Size: | Document Number: LA-F601P | Rev: 0.0

Date: Wednesday, June 06, 2018 | Sheet 62 of 74



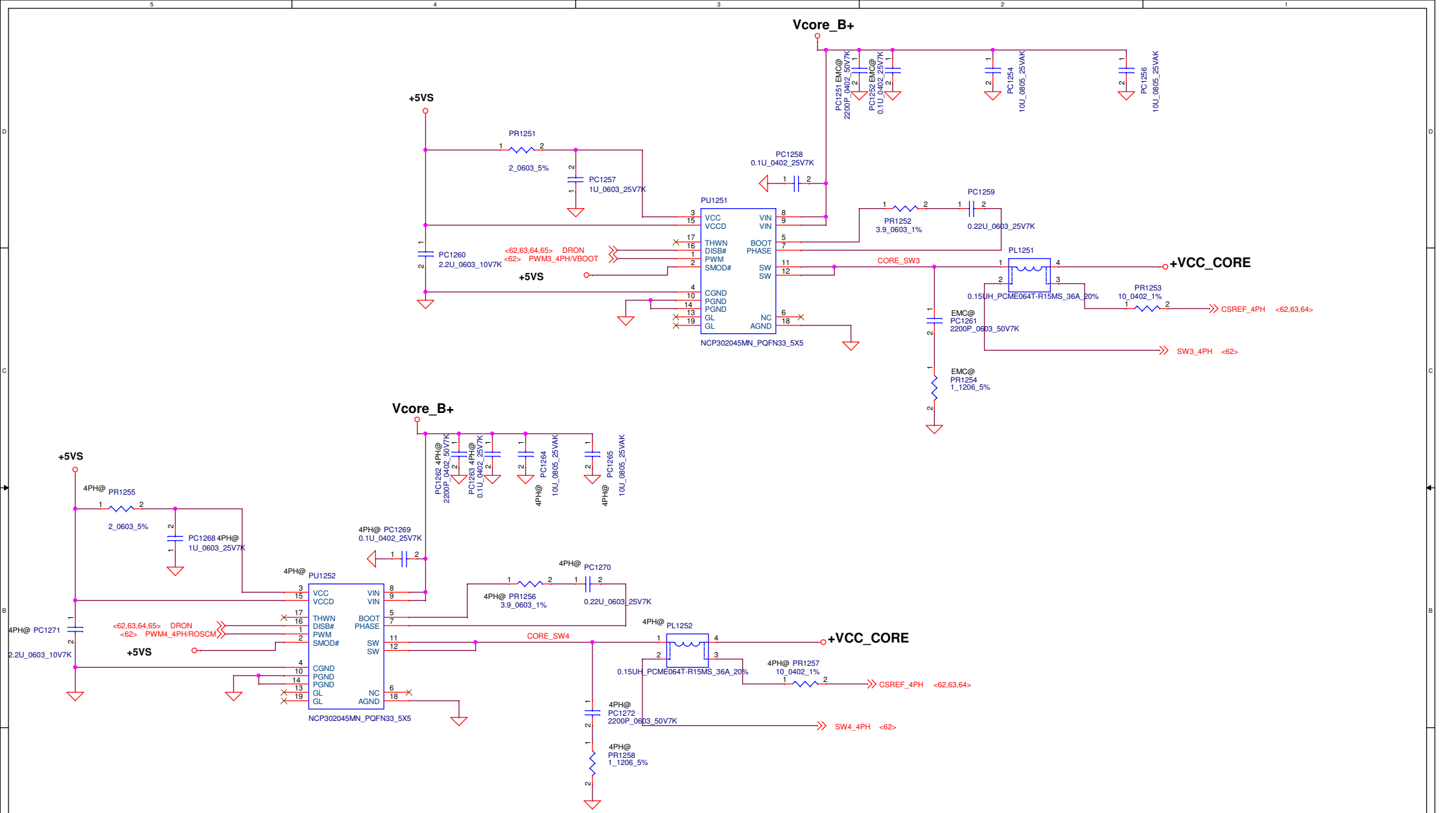
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **+VCC_CORE_Phase1&2**

Size	Document Number	Rev
	LA-F601P	0.0

Date: Wednesday, June 06, 2018 | Sheet 63 of 74



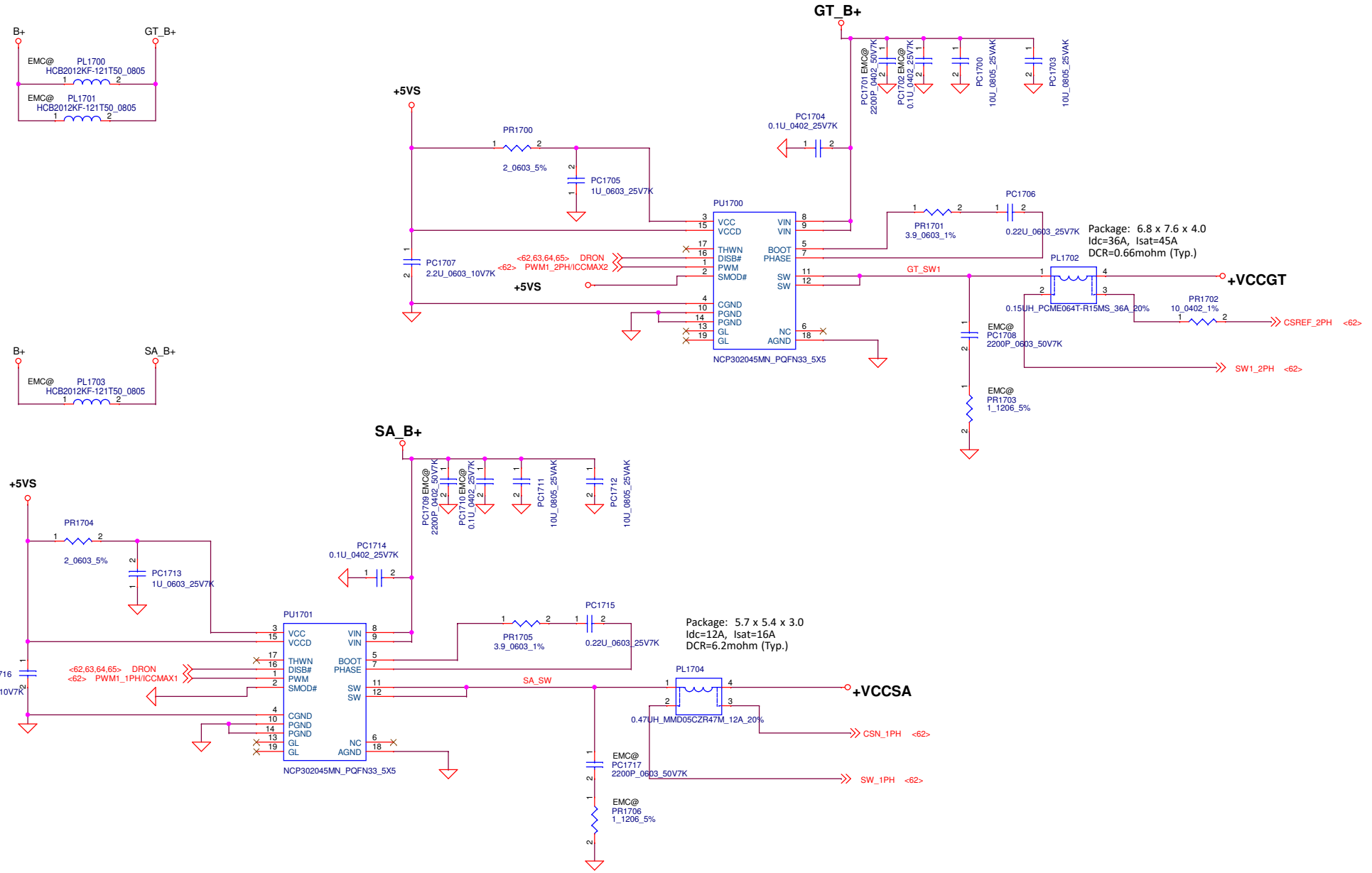
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCC_CORE_Phase3&4

Size | Document Number: LA-F601P | Rev: 0.0

Date: Wednesday, June 06, 2018 | Sheet 64 of 74



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

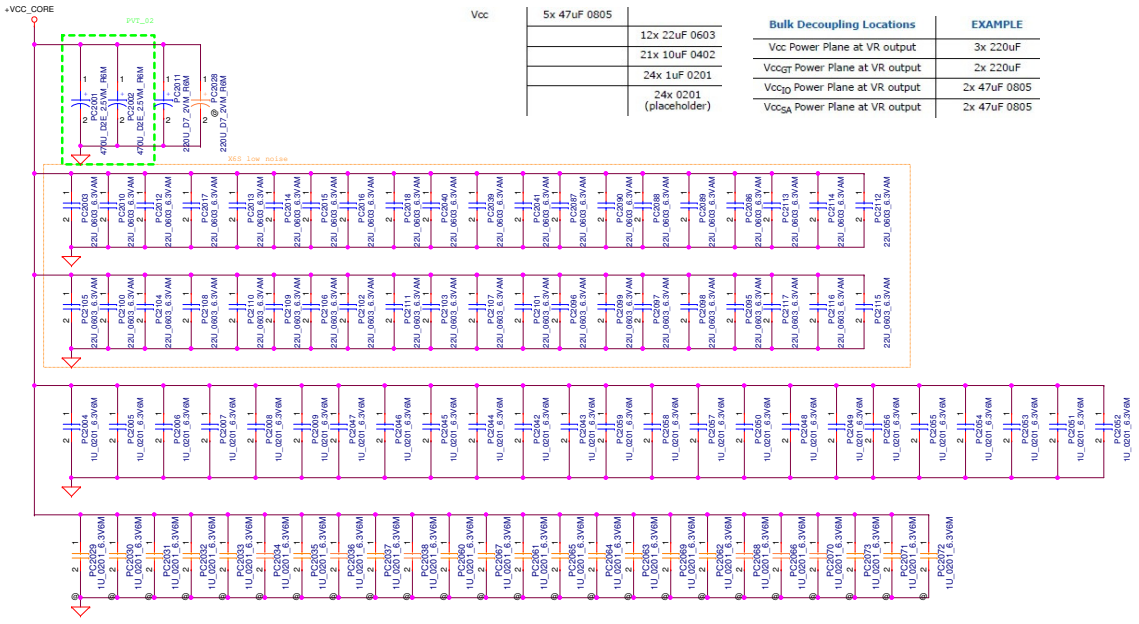
Compal Electronics, Inc.

Title: +VCC_GT/+VCC_SA

Size	Document Number	Rev
	LA-F601P	0.0

Date: Wednesday, June 06, 2018 Sheet 65 of 74

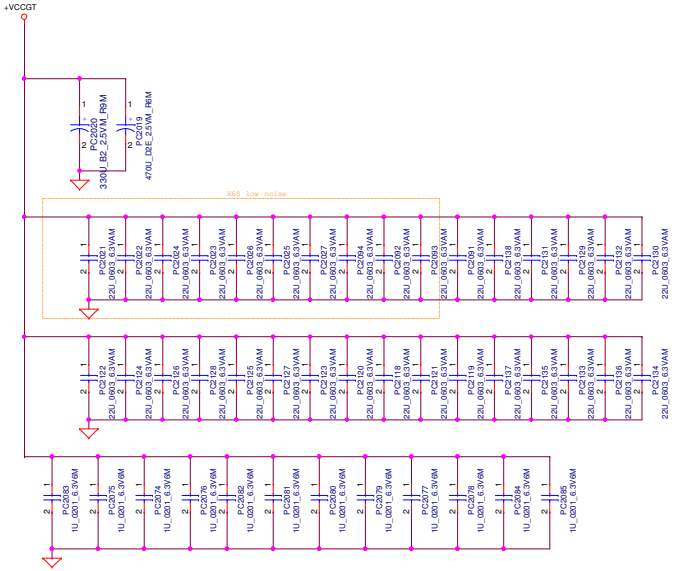
+VCC_CORE
470uF*2
220uF*1
22uF*40
1uF*24



Vcc		
5x 47uF 0805		
	12x 22uF 0603	
	21x 10uF 0402	
	24x 1uF 0201	
	24x 0201 (placeholder)	

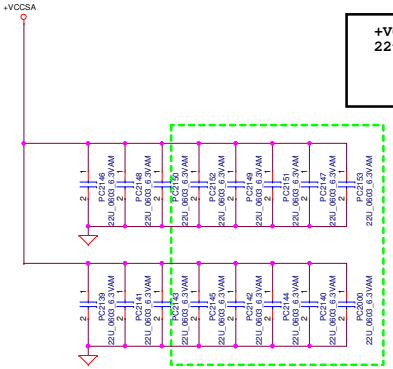
Bulk Decoupling Locations	EXAMPLE
Vcc Power Plane at VR output	3x 220uF
Vcc_{GT} Power Plane at VR output	2x 220uF
Vcc_{IO} Power Plane at VR output	2x 47uF 0805
Vcc_{SA} Power Plane at VR output	2x 47uF 0805

+VCCGT
470uF*2
22uF*32
1uF*12



Vcc_{GT}		
3x 47uF 0805		
7x 22uF 0603		
	10x 10uF 0402	
	12x 1uF 0201	

+VCCSA
22uF*16



Vcc_{SA}		
2x 47uF 0805		
2x 22uF 0805		
	7x 10uF 0402	

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

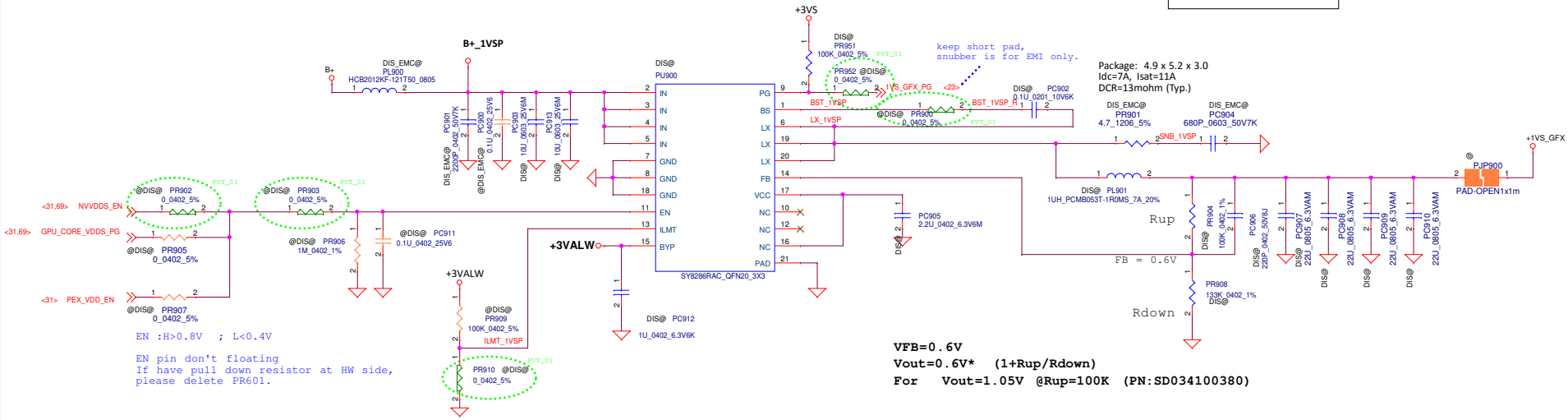
Title: ***P65-PWR_PROCESSOR_DECOUPING***

Size | Document Number: ***LA-F541P*** | Rev: 0.1(000)

Date: Wednesday, June 06, 2018 | Sheet 66 of 74

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

+1.0VSP/1.05VSP
TDC 1.1A
Peak Current 1.1A
OCP current 6A(fix)



VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
For Vout=1.05V @Rup=100K (PN:SD034100380)

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P67-PWR_+1.05VSDGPU(SY8286RAC)**

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

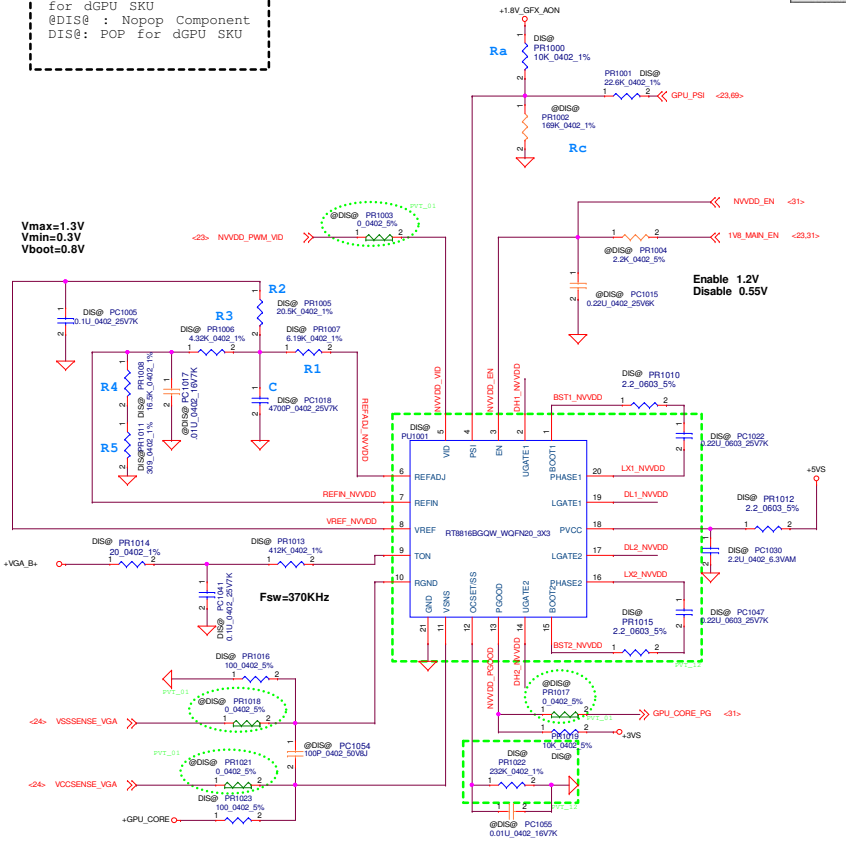
Date: Wednesday, June 06, 2018 | Sheet 67 of 74

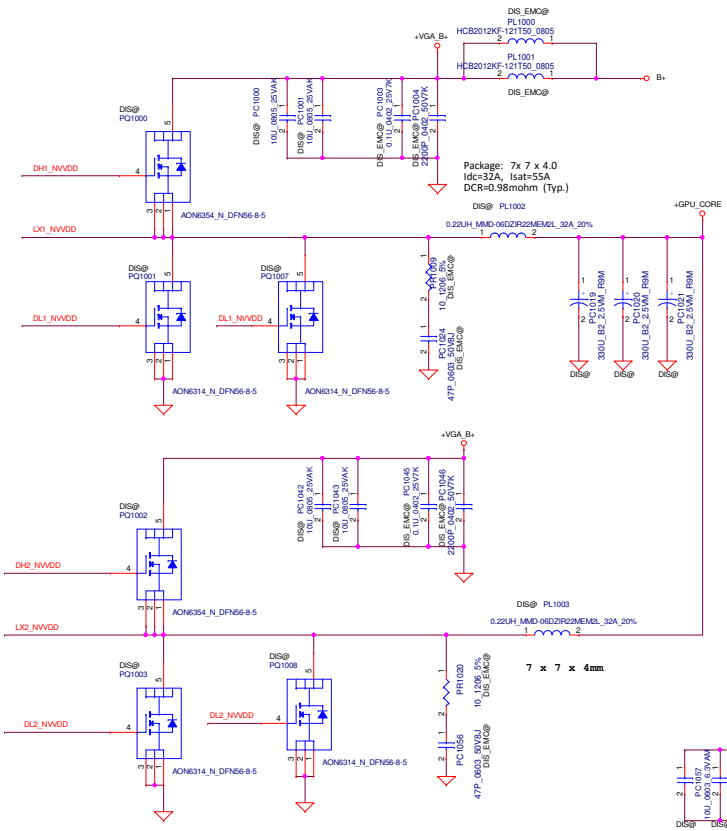
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

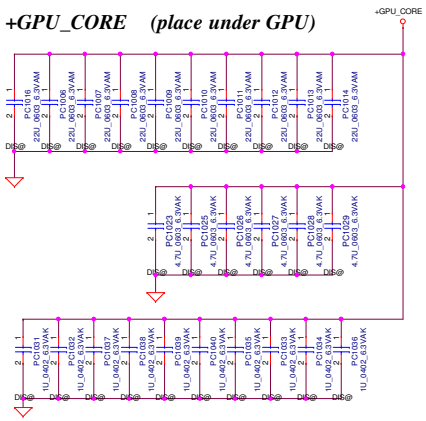
GPU_CORE (0.95V)
TDC 41A
Peak Current 94A
OCP current 100A
DCR 0.98mohm +/- 5%

	MIN	MAX
H/S Rds(on)	4mohm	5.2mohm
L/S Rds(on)	2.8mohm	3.5mohm

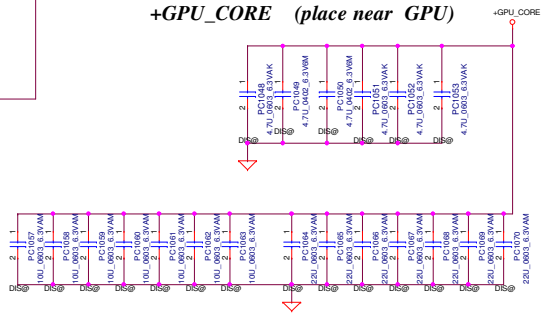




+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



Under:
4.7U_0603_6.3VAK *16
1U_0402_6.3VAK *10

Near:
10U_0805_6.3V6M*7
22U_0805_6.3V6M *7
4.7U_0805_6.3V6K *6
330u*3

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

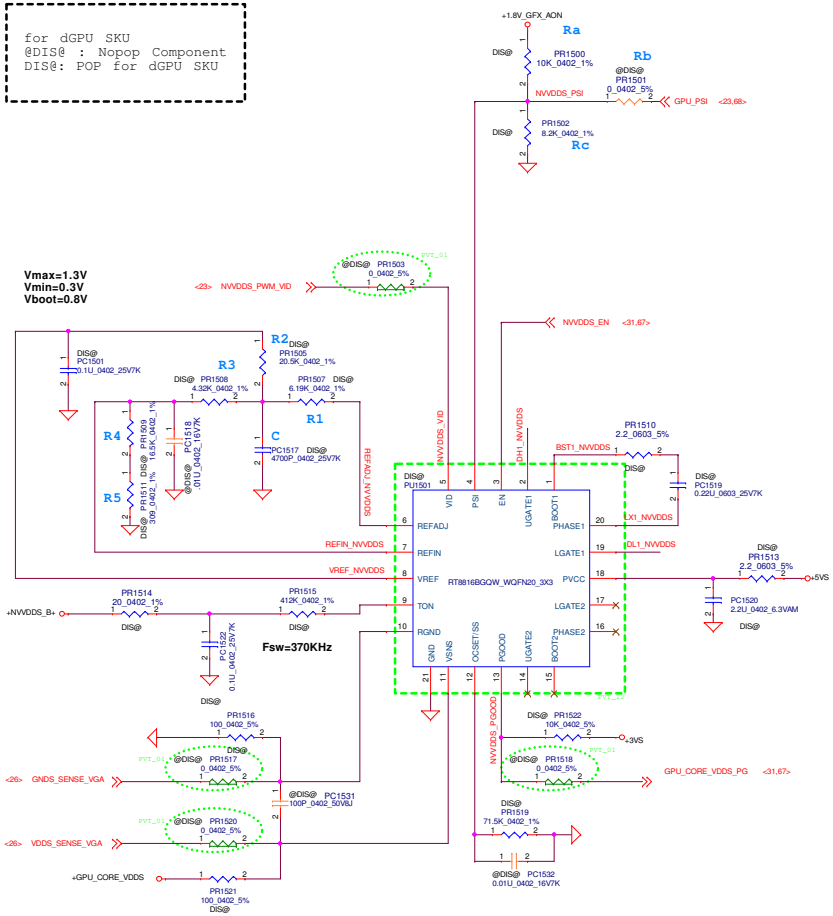
Compal Electronics, Inc.	
Title	P68-PWR-+GPU_CORE
Size	Document Number: LA-F541P
Rev	0.1(X00)
Date:	Wednesday, June 06, 2018
Sheet	68 of 74

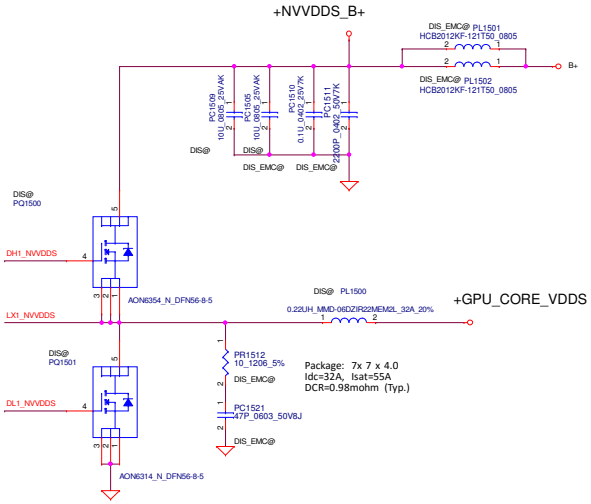
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

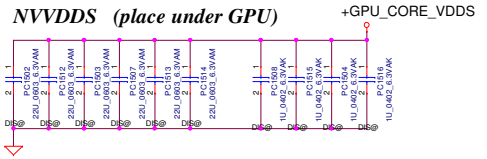
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

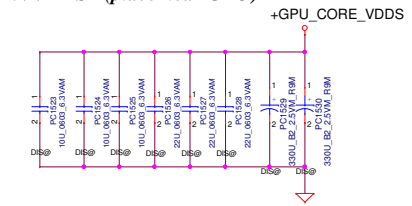
+GPU_CORE_VDDS
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%

	MIN		MAX
H/S Rds(on)	: 3.7mohm	,	4.5mohm
L/S Rds(on)	: 1.5mohm	,	1.9mohm







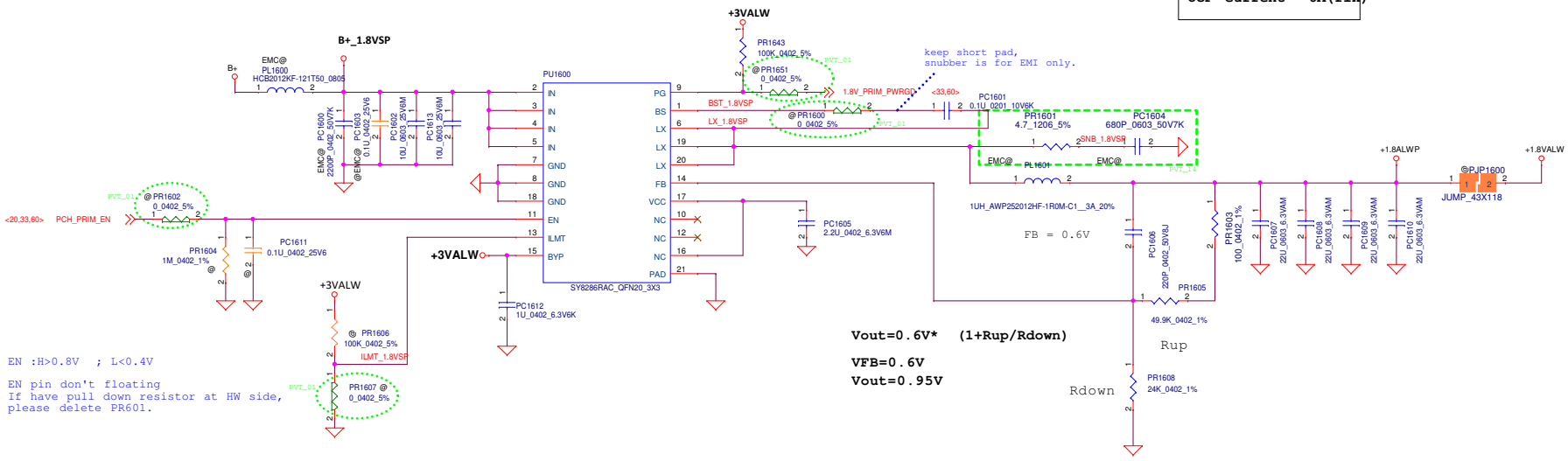


Under:
4.7U_0603_6.3VAK *6
1U_0402_6.3VAK *4

Near:
10U_0603_6.3VAM *3
22U_0603_6.3VAM *3
330u*2

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.	
Title	P69-PWR-+GPU_CORE_VDDS
Size	Document Number: LA-F541P
Rev	0.1(X00)
Date: Wednesday, June 06, 2018	Sheet 69 of 74



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P70-PWR_+1.8ALWP(SY8286RAC)

Size	Document Number	Rev
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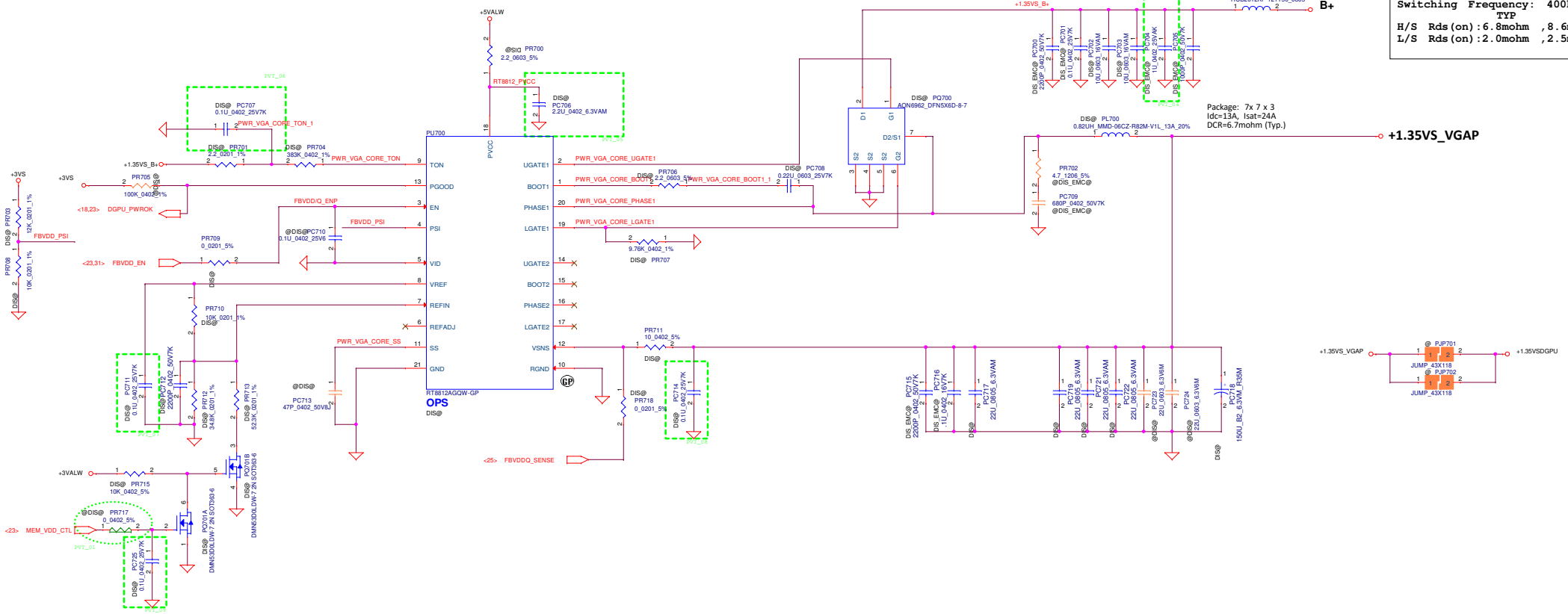
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

1.35VS_VGAP
TDC=11A
Ipeak=20A
OCP=24A
Switching Frequency: 400kHz

	TYP	MAX
H/S Rds(on):	6.8mohm	,8.6mohm
L/S Rds(on):	2.0mohm	,2.5mohm

Package: 7x 7 x 3
Idc=13A, Isat=24A
DCR=6.7mohm (Typ.)



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR +1.35VRAM

Size: | Document Number: LA-E994P | Rev: 0.1(100)

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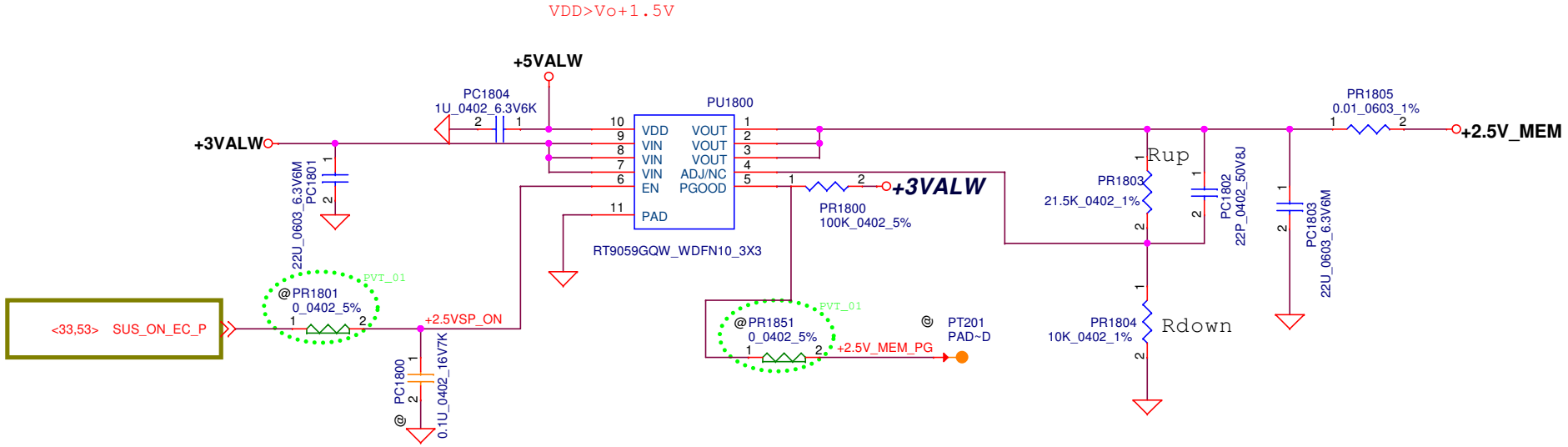
2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.86A
Peak Current 1A
OCP Current 1.46A



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P72-PWR_+2.5V_MEM(RT9059GSP)

Size	Document Number	Rev
	LA-F541P	0.1(X00)

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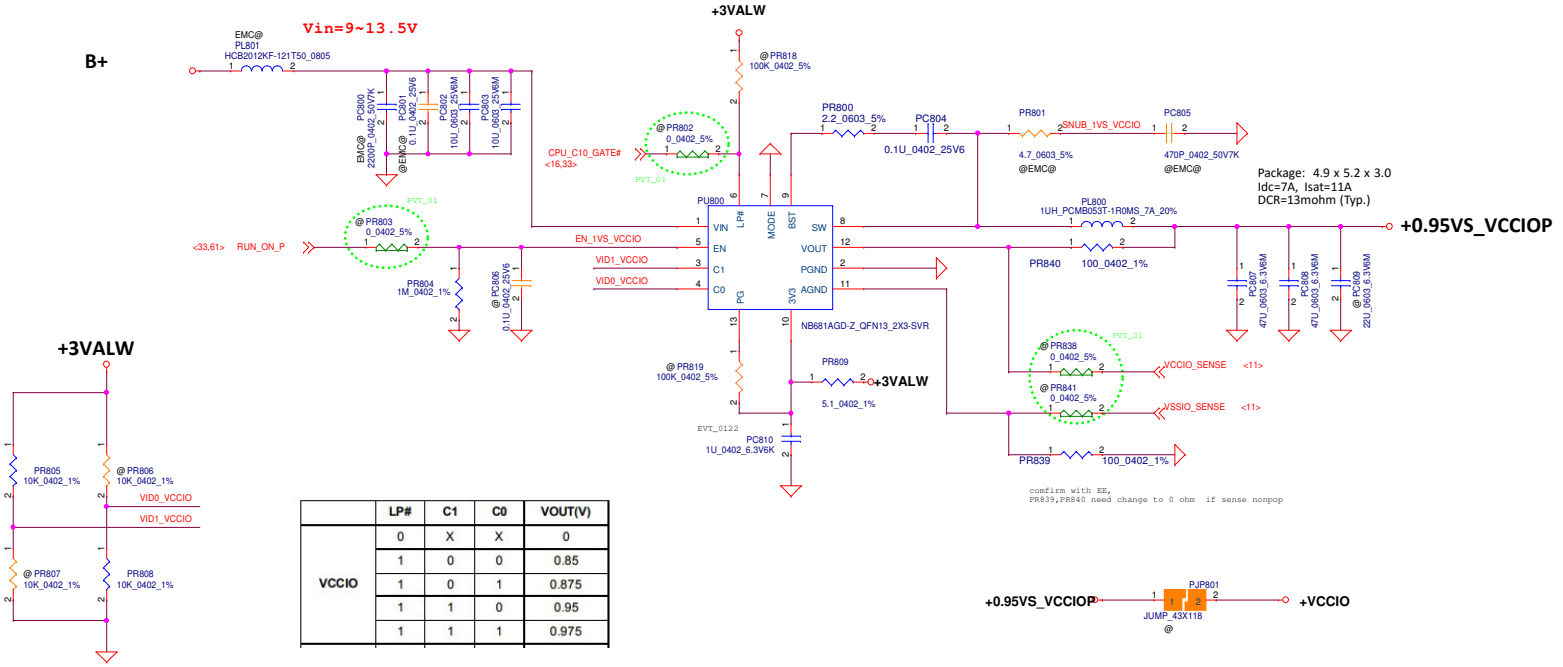
+0.95VS_VCCIOP
TDC 3.9A
Peak Current 5.5 A
OCP Current 6.6 A Fix by IC
TYP MAX



	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Compal Electronics, Inc.
Title: PWR_+1.35VRAM
Size: Document Number: LA-E994P
Rev: 0.1(X00)
Date: Wednesday, June 06, 2018 Sheet 73 of 76

Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
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27				EE			
28				EE			
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30				EE			
31				EE			
32				EE			
33				EE			
34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

Compal Electronics, Inc.		
Title: P74-EE - NOTE2		
Size	Document Number: LA-G341P	Rev: 1.0(A00)
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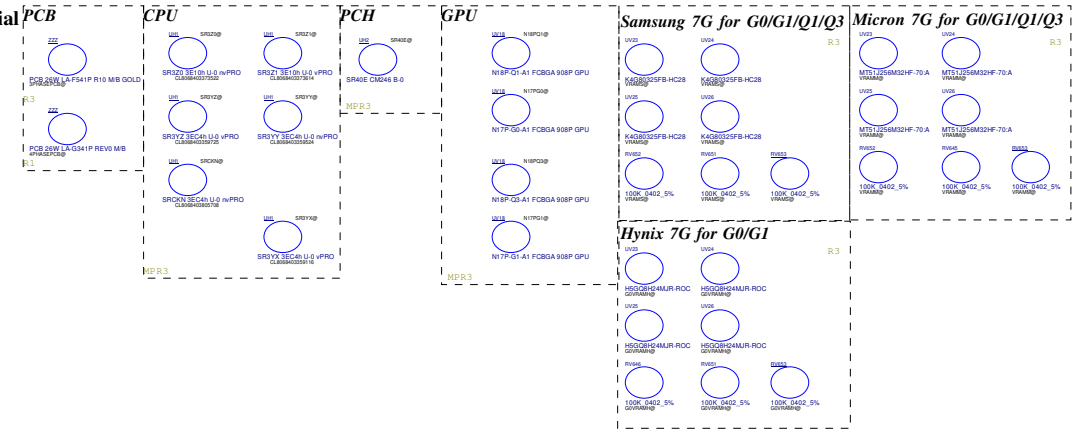
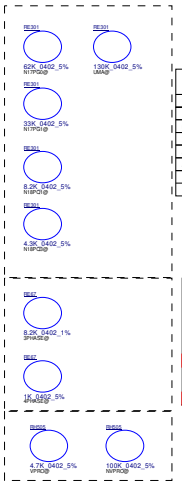
Compal Confidential

Project Code :
File Name :





RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	

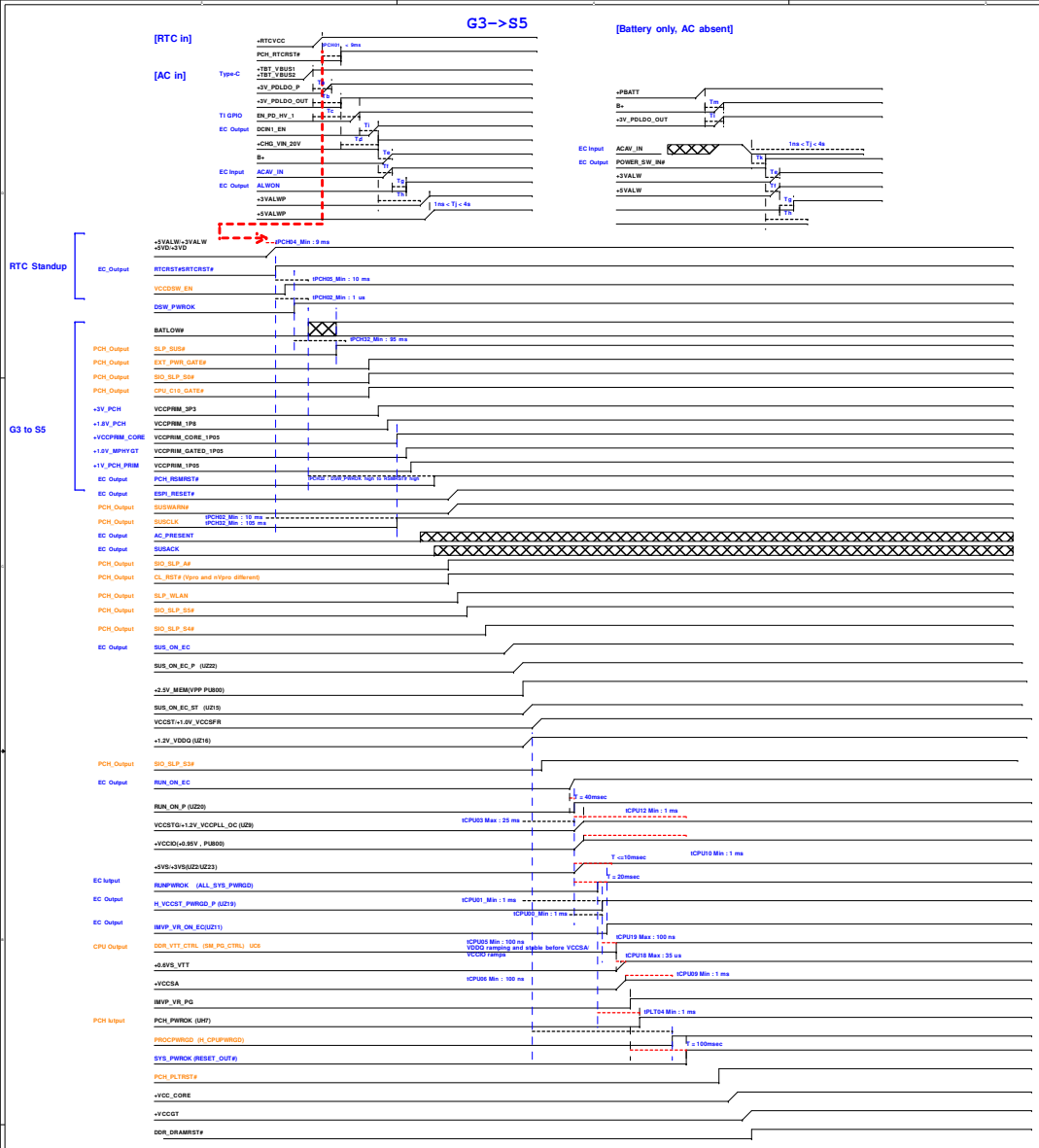
RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	PVT
4.3K	4700p	X00_4P	i9 EVT
2K	4700p	X01_4P	i9 DVT
1K	4700p	A00_4P	i9 PVT

TLS CONFIDENTIALITY
HIGH(4.7k)
LOW(DEFAULT)(100K)
BIOS 20k internal pull-down

DRAM Option	DRAM Config Option (MEM_CONFIG0 / MEM_CONFIG1 / MEM_CONFIG2 / MEM_CONFIG3 / MEM_CONFIG4)	DRAM SDP / DDP Option	R_COMP	X76
SDP MICRON 8G/2400				X7674531L07
SDP HYNIX 8G/2400				X7674531L09
SDP SAMSUNG 8G/2400				X7674531L08
DDP MICRON 16G/2400				X7674531L10
DDP HYNIX 16G/2400				X7674531L15
DDP SAMSUNG 16G/2400				X7674531L11

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: BOM Option			
Size	Document Number: LA-G341P		Rev: 1.0(ANS)
Date: Wednesday, June 06, 2018	Sheet 75 of 76		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/07	Deciphered Date 2018/12/31	Title: Power Up Sequence
			Size: Document Number: Rev: 1.0(0)
			Date: Wednesday, June 06, 2018 Sheet 76 of 76