Daytona ATI Block Diagram

(RoHS)

Project code: 91.4P901.001
PCB P/N : 06201
REVISION : -1

Clock Generator
ICS951413/CY28RS400
3

Mobile CPU
Yonah
4,5

4X DATA
2X ADDRESS
AGTL+
533/667MHz

SMBus
Thermal Sensor & Fan
G792
20

ATI NB RC415ME
AGTL+ P4 CPU I/F
DDR2 I/F
INTEGRATED GRAPHICS
TVOUT/SVIDEO
LVDM(LVDS)
1 X16 PCIE VIDEO/SDVO I/F
1 X4 PCIE SB I/F
6 X1 PCIE GPP I/F
5,6,7,8,9,10

LCD CONN
XGA/SXGA+
14
LVDS

CRT CONN
13
CRT

DDR2 400/533/667 MHz

UNBUFFERED DDR2 SODIMM
11,12

UNBUFFERED DDR2 SODIMM
11,12

PCI-E

GIGA RTL8111B-GR
23

RJ45 CONN
24

PWR SW
TPS2224A
27

CARDBUS
PCI 1520
GHK
25/B/1
26

CARDBUS
TWO SLOT
27

PCI BUS

PCIE
X4

ATI SB460
USB2.0 10 (8)
SATA II (4 PORTS)
AZALIA HD AUDIO
AC97 2.3
ATA 66/100/133
SPI I/F
LPC I/F
ACPI 1.2
INT RTC
HW MONITOR
PCI/PCI BDGE
15,16,17,18,19

Mini-Card
802.11a/b/g/n
25

USB 2.0

USB x 4
22

SATA

HDD
21

SIDE/PATA

Optical
21

RJ11 CONN
24

MODEM
MDC 1.5 Card
22

AZALIA

LPC Bus

LINE IN
MIC IN

Audio CODEC
ALC883
30

PS2
34

KBC
ENE KB3910
32

FlashRom
MX29LV800 2M
35

NS SIO
PC87392
36

TPM1.2
28

SERIAL PORT
29

PRN PORT
29

FDD
21

Touch Pad
33

Int. KB
33

OP AMP
G1432
31

LINE OUT

2CH SPEAKER

SYSTEM DC/DC
MAX8743A

INPUTS	OUTPUTS
DCBATOUT	1D8V_S5 1D2V_S3 +15V

SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC
ISL6262

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

CARD 0D9V (LDO)
TPS51100

INPUTS	OUTPUTS
5V_S5	0D9V_S0

CARD 1D05V (LDO)
APL5912

INPUTS	OUTPUTS
1D2V_S3	1D05V_S0

CPU PLL 1D5V(LDO)
APL5308

INPUTS	OUTPUTS
3D3V_S0	1D5V_S0

PCB LAYER

L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

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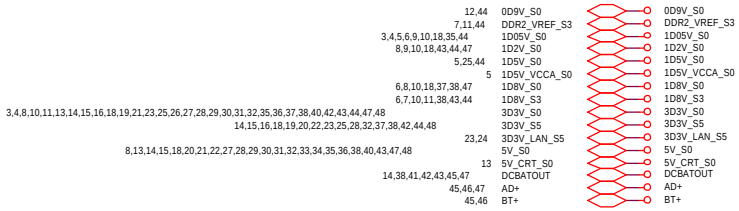
Title: Block Diagram

Size: Custom | Document Number: Daytona | Rev: -1

Date: Thursday, June 15, 2006 | Sheet 1 of 48



PCI RESOURCE TABLE

USB Port	Key West Define
USBP[0]	USB CONN2
USBP[1]	USB CONN3
USBP[2]	Mini card used
USBP[3]	NC
USBP[4]	USB CONN4
USBP[5]	NC
USBP[6]	Finger printer
USBP[7]	USB CONN1

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Cardbus	AD22	INT_E#	REQ0#/GNT0#

Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A2
DDR Module 2	A0
Battery	16
Thermal control	7A

PCIE Port	DK1 ATI Define
PE[0]	NC
PE[1]	NC
PE[2]	Mini Card
PE[3]	LAN

<Core Design>

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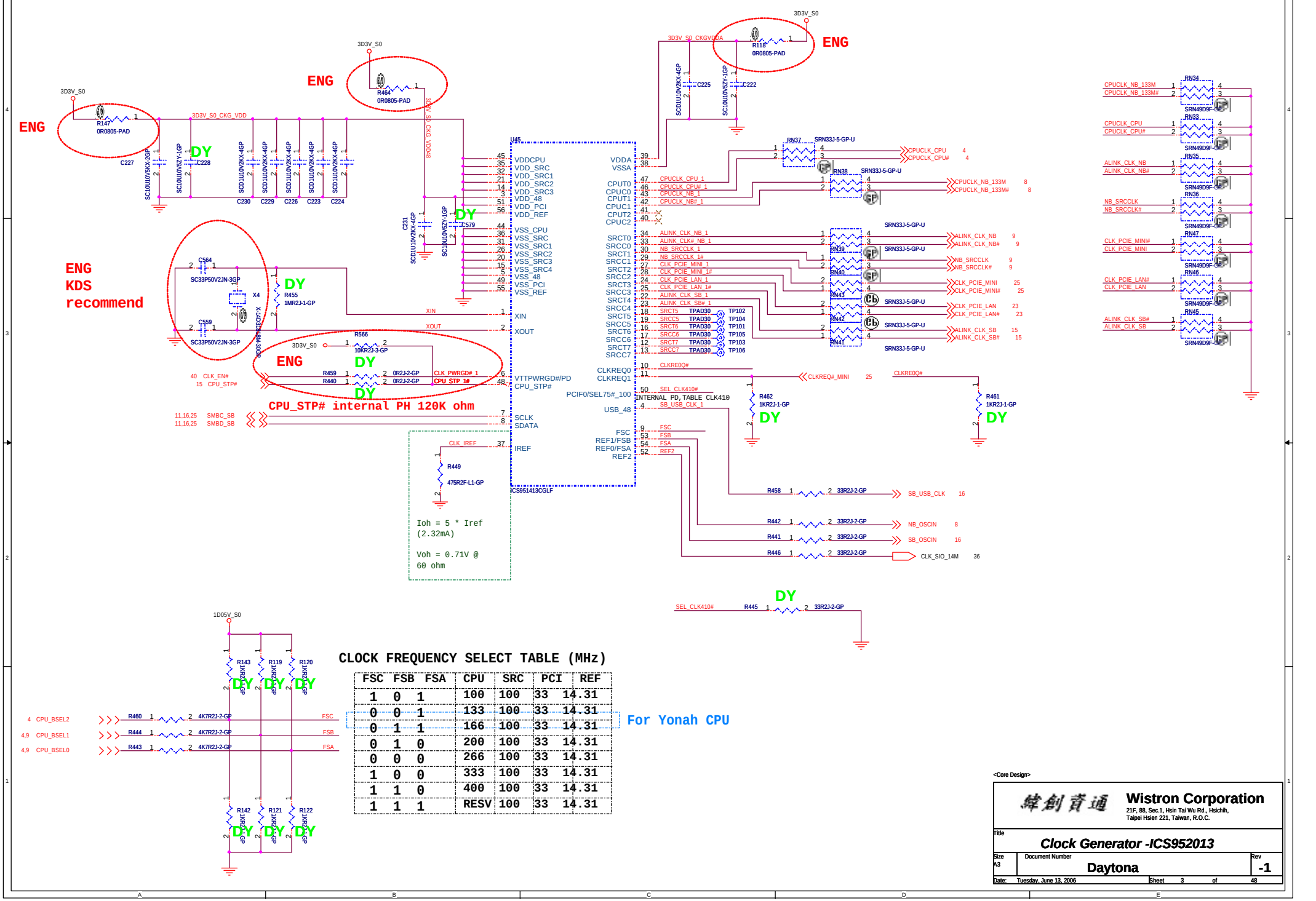
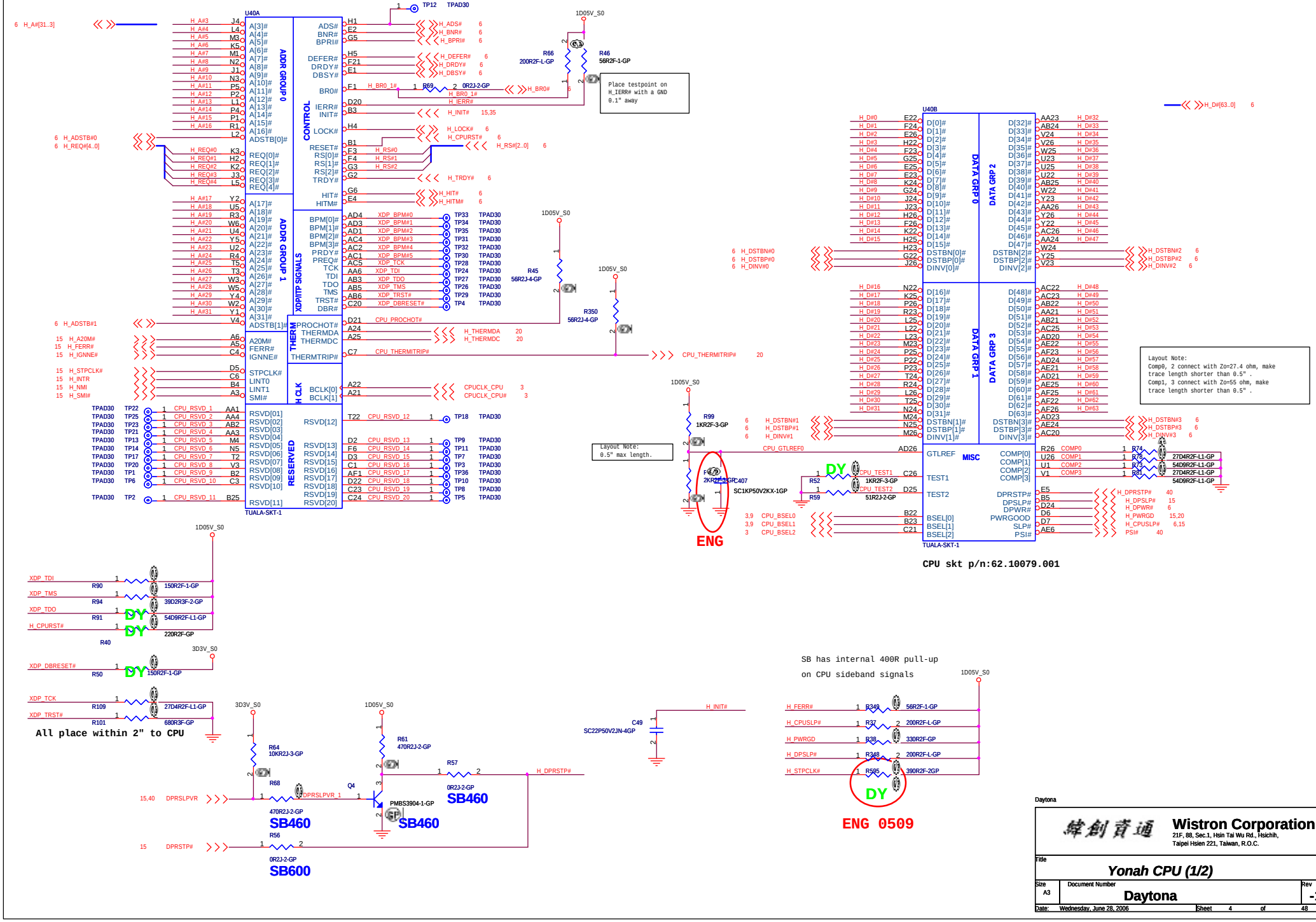
Taipei Hsien 221, Taiwan, R.O.C.

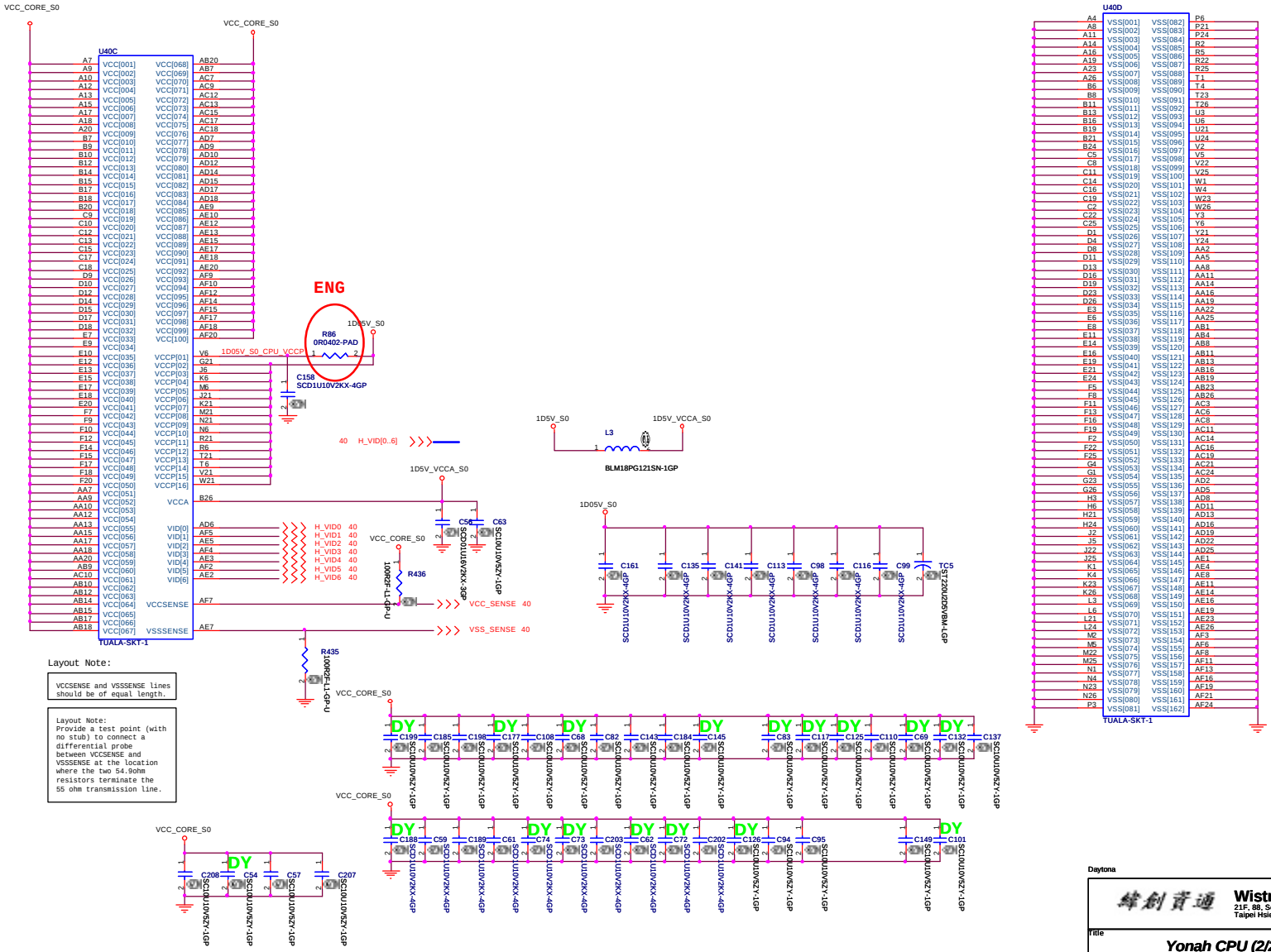
Title: Table of Content / HISTORY

Size: A3 | Document Number: Daytona | Rev: -1

Date: Tuesday, June 13, 2006 | Sheet 2 of 48


ENG
KDS
recommend
CPU_STP# internal PH 120K ohm
Ioh = 5 * Iref
(2.32mA)
Voh = 0.71V @
60 ohm
U45
ICS951413CGLF
CLOCK FREQUENCY SELECT TABLE (MHz)
FSC FSB FSA CPU SRC PCI REF
1 0 1 100 100 33 14.31
0 0 1 133 100 33 14.31
0 1 1 166 100 33 14.31
0 1 0 200 100 33 14.31
0 0 0 266 100 33 14.31
1 0 0 333 100 33 14.31
1 1 0 400 100 33 14.31
1 1 1 RESV 100 33 14.31
For Yonah CPU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Clock Generator -ICS952013
Size A3
Daytona
Rev -1
Date: Tuesday, June 13, 2006
Sheet 3 of 48


U40A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
TUALA-SKT-1
U40B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
TUALA-SKT-1
Place testpoint on H_IERR# with a GND 0.1" away
Layout Note: 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
CPU skt p/n:62.10079.001
SB has internal 400R pull-up on CPU sideband signals
All place within 2" to CPU
ENG
ENG 0509
SB460
SB600
DY
Daytona
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Yonah CPU (1/2)
Daytona
-1
Wednesday, June 28, 2006
4
48


VCC_CORE_S0
U40C
TUALA-SKT-1
ENG
R86
0R0402-PAD
1D05V_S0
1D05V_S0_CPU_VCCP
C158
SCD1U10V2KX-4GP
H_VID[0..6]
1D5V_VCCA_S0
L3
BLM18PG121SN-1GP
R436
VCC_SENSE
VSS_SENSE
R435
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
U40D
TUALA-SKT-1
Daytona
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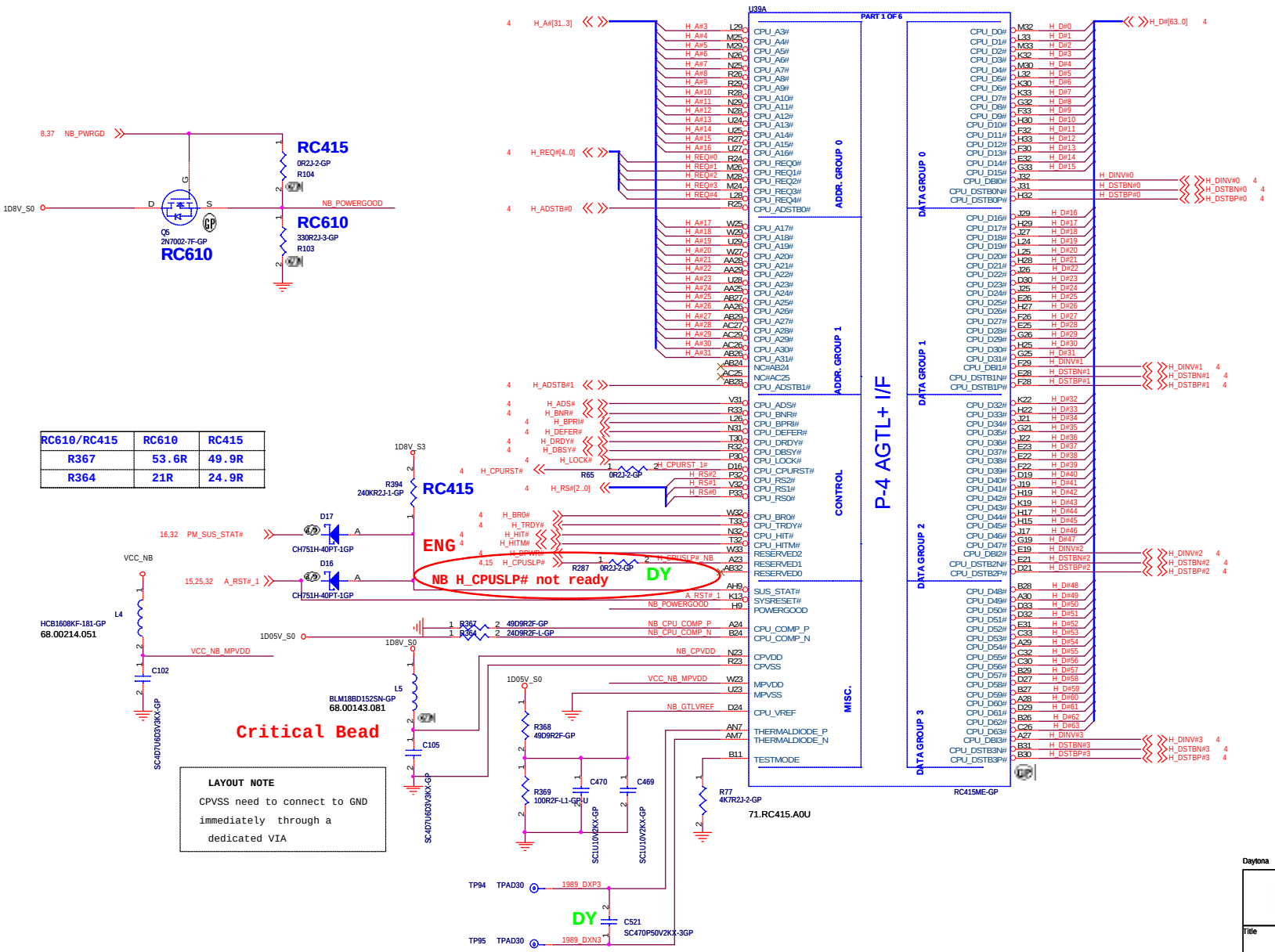
Title
Yonah CPU (2/2)
Size
Custom
Document Number
Daytona
Rev
-1
Date: Tuesday, June 13, 2006
Sheet 5 of 48



Daytona

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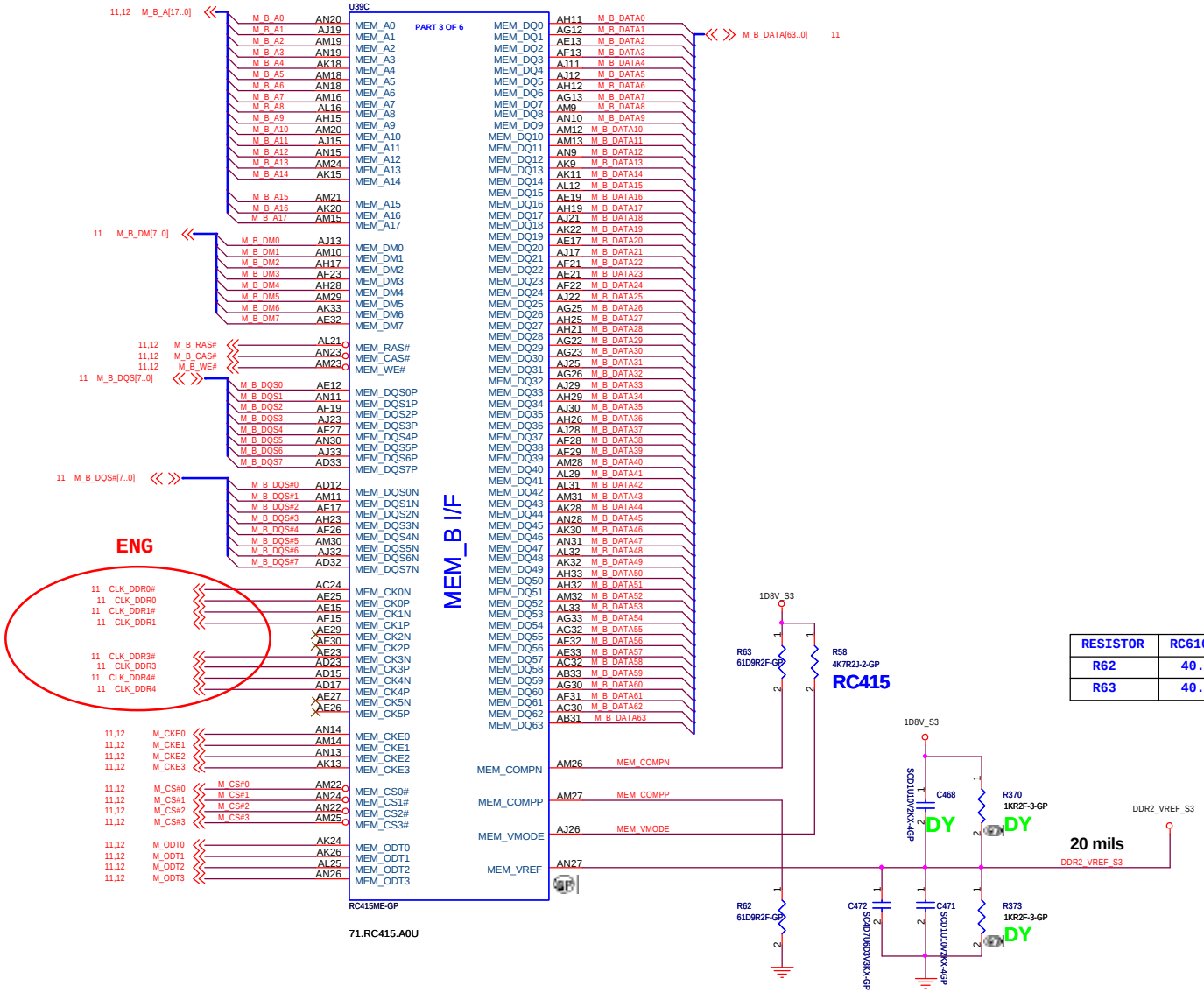
Taipei Hsien 221, Taiwan, R.O.C.

Title: RC415ME (1 of 5) Host I/F

Size	Document Number	Rev
Custom	Daytona	-1

Date: Wednesday, June 28, 2006 Sheet 6 of 48



RESISTOR	RC610	RC415
R62	40.2R	61.9R
R63	40.2R	61.9R

Daytona

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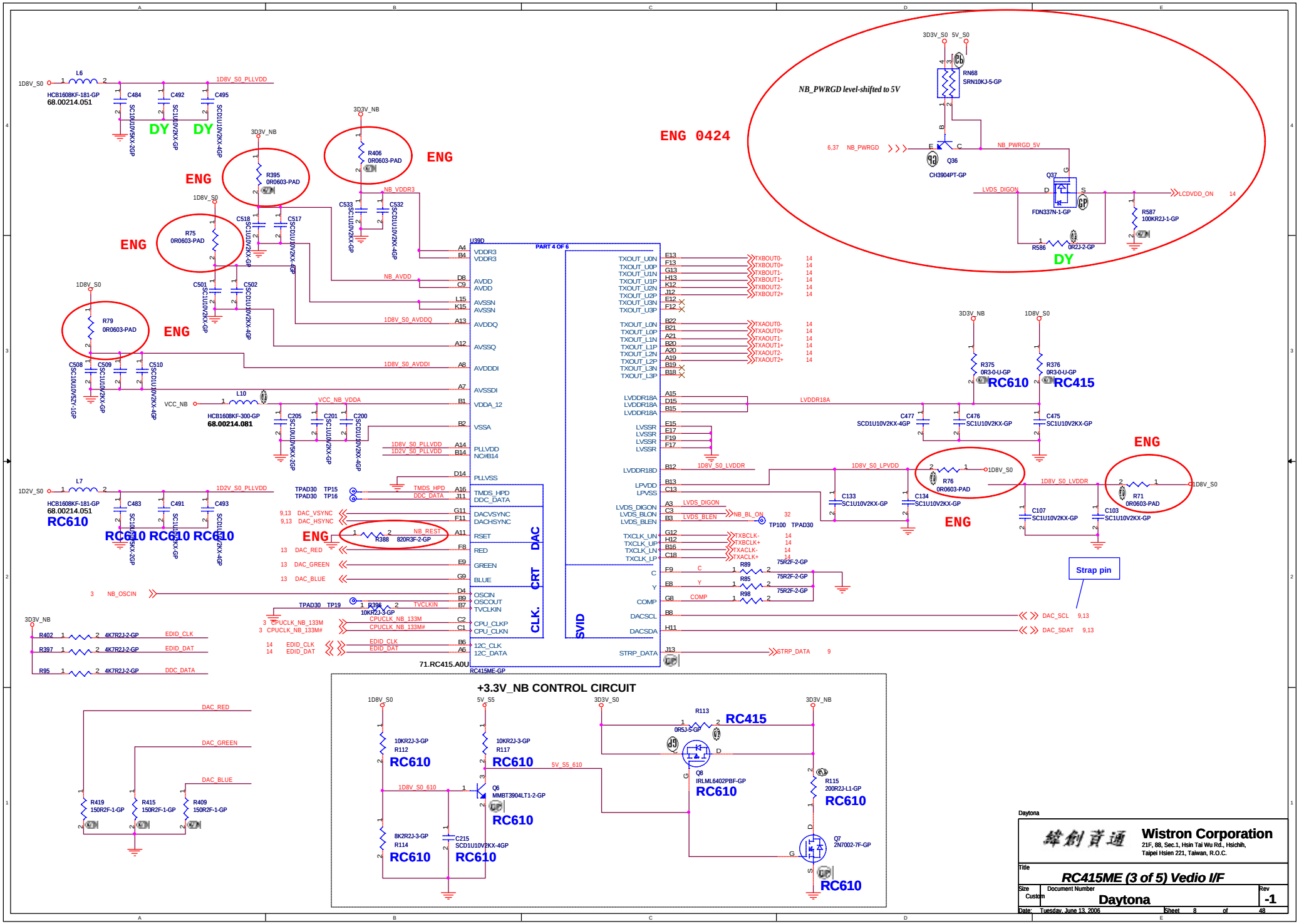
Taipei Hsien 221, Taiwan, R.O.C.

Title: RC415MB (2 of 5) Memory I/F

Size	Document Number	Rev
A3	Daytona	-1

Date: Wednesday, June 28, 2006 Sheet 7 of 48


ENG 0424
NB_PWRGD level-shifted to 5V
+3.3V_NB CONTROL CIRCUIT
Strap pin
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Daytona
RC415ME (3 of 5) Vedio I/F
Size Custom
Document Number Daytona
Rev -1
Date: Tuesday, June 13, 2006
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RC610 STRAPS	RC415 STRAPS
DAC_HSYNC: STRP_INTGFX_DISABLE DEFAULT: 0 0: ENABLE 1: DISABLE	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
DAC_VSYNC: STRAP_MOBILE_GFX DEFAULT: 1 0: DESKTOP GRAPHICS DEVICE 1: MOBILE GRAPHICS DEVICE	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
	BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
STRP_DATA: STRP_MEMSTRAPS DEFAULT: 1 0: SELECT MEMORY CHA A AS DEBUG BUS 1: NORMAL MODE	STRP_DATA:Debug strap DEFAULT: 1 1: E2PROM STRAPING 0: MEMORY CHANNEL STRAPING
DDC_DATA: STRAP_MEMVMODE DEFAULT: 1 0: DDR3 1: DDR2	
	DAC_SCL: CPU VCC DEFAULT:1 1: DESKTOP 0: MOBILE

NB Strap pins

DY

BMREQ# — R106 4K7R2J-2-GP — 3D3V_NB
BMREQ# — R110 4K7R2J-2-GP

3D3V_NB — R408 4K7R2J-2-GP — RC610
3D3V_NB — R430 4K7R2J-2-GP — RC415
1D05V_S0 — R433 4K7R2J-2-GP — RC415

8,13 DAC_HSYNC — R422 4K7R2J-2-GP — DAC_HSYNC_1 — RC415 — Q22 MMBT3904LT1-2-GP — CPU_BSEL1 3,4

3D3V_NB — R416 4K7R2J-2-GP — DY
3D3V_NB — R410 4K7R2J-2-GP — RC610
3D3V_NB — R429 4K7R2J-2-GP — RC415
1D05V_S0 — R431 4K7R2J-2-GP — DY

8,13 DAC_VSYNC — R421 4K7R2J-2-GP — DAC_VSYNC_1 — RC415 — Q23 MMBT3904LT1-2-GP — DY — CPU_BSEL0 3,4

R417 4K7R2J-2-GP — DY

U39B — PART 2 OF 6

PCIE I/F

GFX_RX0P	F4	E5	GFX_TX0P
GFX_RX0N	E2	F5	GFX_TX0N
GFX_RX1P	G4	E4	GFX_TX1P
GFX_RX1N	H5	D3	GFX_TX1N
GFX_RX2P	J5	J6	GFX_TX2P
GFX_RX2N	J4	J7	GFX_TX2N
GFX_RX3P	M6	G2	GFX_TX3P
GFX_RX3N	L6	G1	GFX_TX3N
GFX_RX4P	M8	H2	GFX_TX4P
GFX_RX4N	M9	J1	GFX_TX4N
GFX_RX5P	N9	K2	GFX_TX5P
GFX_RX5N	N8	K1	GFX_TX5N
GFX_RX6P	N5	L2	GFX_TX6P
GFX_RX6N	R5	L1	GFX_TX6N
GFX_RX7P	N6	M2	GFX_TX7P
GFX_RX7N	R6	N1	GFX_TX7N
GFX_RX8P	U9	P2	GFX_TX8P
GFX_RX8N	R9	P1	GFX_TX8N
GFX_RX9P	U5	R2	GFX_TX9P
GFX_RX9N	W5	R1	GFX_TX9N
GFX_RX10P	U6	T2	GFX_TX10P
GFX_RX10N	W6	V1	GFX_TX10N
GFX_RX11P	W8	W2	GFX_TX11P
GFX_RX11N	W9	W1	GFX_TX11N
GFX_RX12P	AA5	Y2	GFX_TX12P
GFX_RX12N	AB5	Y1	GFX_TX12N
GFX_RX13P	AA6	AA2	GFX_TX13P
GFX_RX13N	AB6	AB1	GFX_TX13N
GFX_RX14P	AB8	AC2	GFX_TX14P
GFX_RX14N	AB9	AC1	GFX_TX14N
GFX_RX15P	AC5	AD1	GFX_TX15P
GFX_RX15N	AE5	AD2	GFX_TX15N

23 PCIE_LAN_RXP3 — AF6 GPP_RX3P — AJ2 GPP_TX3P — PCIE_LAN_TXP3_1 — C538 SCD1U10V2KX-4GP — PCIE_LAN_TXP3 23
23 PCIE_LAN_RXN3 — AF7 GPP_RX3N — AJ1 GPP_TX3N — PCIE_LAN_TXN3_1 — C537 SCD1U10V2KX-4GP — PCIE_LAN_TXN3 23
25 PCIE_MC_RXP2 — AH4 GPP_RX2P — AH2 GPP_TX2P — PCIE_MC_TXP_2_1 — C536 SCD1U10V2KX-4GP — PCIE_MC_TXP2 25
25 PCIE_MC_RXN2 — AH5 GPP_RX2N — AH1 GPP_TX2N — PCIE_MC_TXN_2_1 — C535 SCD1U10V2KX-4GP — PCIE_MC_TXN2 25

GPP_RX1P/SB_RX3P — AE9 — AC6 GPP_TX1P/SB_TX3P
GPP_RX1N/SB_RX3N — AE8 — AE6 GPP_TX1N/SB_TX3N
GPP_RX0P/SB_RX2P — AG2 — AE2 GPP_TX0P/SB_TX2P
GPP_RX0N/SB_RX2N — AG1 — AE1 GPP_TX0N/SB_TX2N

RC610 RC610 RC610 RC610

15 A_RXP_3 — AJ3 NC#AJ3 — AK2 NC#AK2 — A_TXP_3_1 — C540 SCD1U10V2KX-4GP — A_TXP_3 15
15 A_RXN_3 — AK4 NC#AK4 — AK1 NC#AK1 — A_TXN_3_1 — C539 SCD1U10V2KX-4GP — A_TXN_3 15
15 A_RXP_2 — AL4 NC#AL4 — AL2 NC#AL2 — A_TXP_2_1 — C542 SCD1U10V2KX-4GP — A_TXP_2 15
15 A_RXN_2 — AM3 NC#AM3 — AL1 NC#AL1 — A_TXN_2_1 — C541 SCD1U10V2KX-4GP — A_TXN_2 15

15 A_RXP_1 — AH8 SB_RX1P — AN3 SB_TX1P — A_TXP_1_1 — C543 SCD1U10V2KX-4GP — A_TXP_1 15
15 A_RXN_1 — AJ8 SB_RX1N — AN4 SB_TX1N — A_TXN_1_1 — C544 SCD1U10V2KX-4GP — A_TXN_1 15
15 A_RXP_0 — AF8 SB_RX0P — AM4 SB_TX0P — A_TXP_0_1 — C545 SCD1U10V2KX-4GP — A_TXP_0 15
15 A_RXN_0 — AF9 SB_RX0N — AM5 SB_TX0N — A_TXN_0_1 — C546 SCD1U10V2KX-4GP — A_TXN_0 15

3 NB_SRCCLK — F2 GFX_CLKP — AN6 PCE_ISET — PCE_TXSET
3 NB_SRCCLK# — F1 GFX_CLKN — AM6 PCE_NCAL — PCE_ISET
3 ALINK_CLK_NB — D2 SB_CLKP — AK5 PCE_PCAL — PCE_PCAL
3 ALINK_CLK_NB# — E1 SB_CLKN — AK7 PCE_TXISET — PCE_NCAL

15 BM_REQ — R87 0R2J-2-GP — BM_REQ_1 — K11 BMREQ# — PCIE CLK

RC415ME-GP

71.RC415.A0U

RC415

R92 8K25R3F-2-GP — R97 150R3F-GP — R405 100R2F-L1-GP-U — R401 10KR3F-L-GP — 1D2V_S0

	RC610	RC415
R401	1.47K	10K
R405	2K	100R
R97	562R	150R

Adjust PCI-E Amp. R->Small then Amp->Large

FSB SPEED CLK Strap

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	------
0	1	1	166MHZ

8,13 DAC_SDAT — R426 4K7R2J-2-GP — 3D3V_NB
R427 4K7R2J-2-GP — DY

8,13 DAC_SCL — R425 4K7R2J-2-GP — 3D3V_NB

Q24 CH3904PT-GP — RC415
B — R437 4K7R2J-2-GP — SB_PWRGD# 37 — RC415

8 STRP_DATA — R67 4K7R2J-2-GP — 3D3V_NB
R70 4K7R2J-2-GP — DY

STRP_DATA:Debug strap
DEFAULT:0

High, E2PROM STRAPING
Low, Memory Channel STRAPING

This strap select the CPU I/O voltage level.

0:MOBILE (1.4V or above)
1:DESKTOP(1.4V or below)

Daytona

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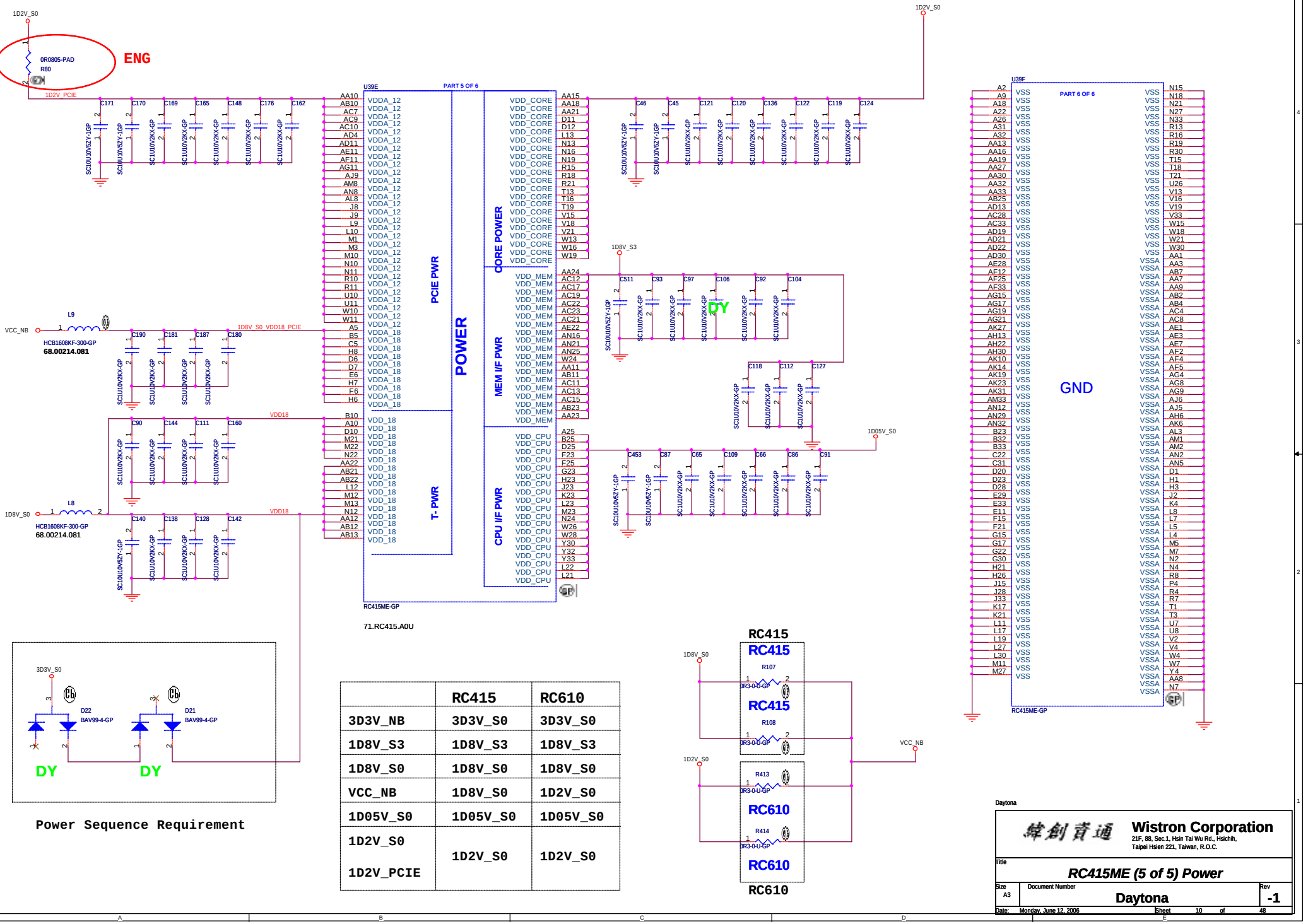
Title: RC415ME (4 of 5) PCI-E & Strap

Size	Document Number	Rev
A3	Daytona	-1

Date: Tuesday, June 13, 2006 Sheet 9 of 48



	RC415	RC610
3D3V_NB	3D3V_S0	3D3V_S0
1D8V_S3	1D8V_S3	1D8V_S3
1D8V_S0	1D8V_S0	1D8V_S0
VCC_NB	1D8V_S0	1D2V_S0
1D05V_S0	1D05V_S0	1D05V_S0
1D2V_S0 1D2V_PCIE	1D2V_S0	1D2V_S0

Daytona

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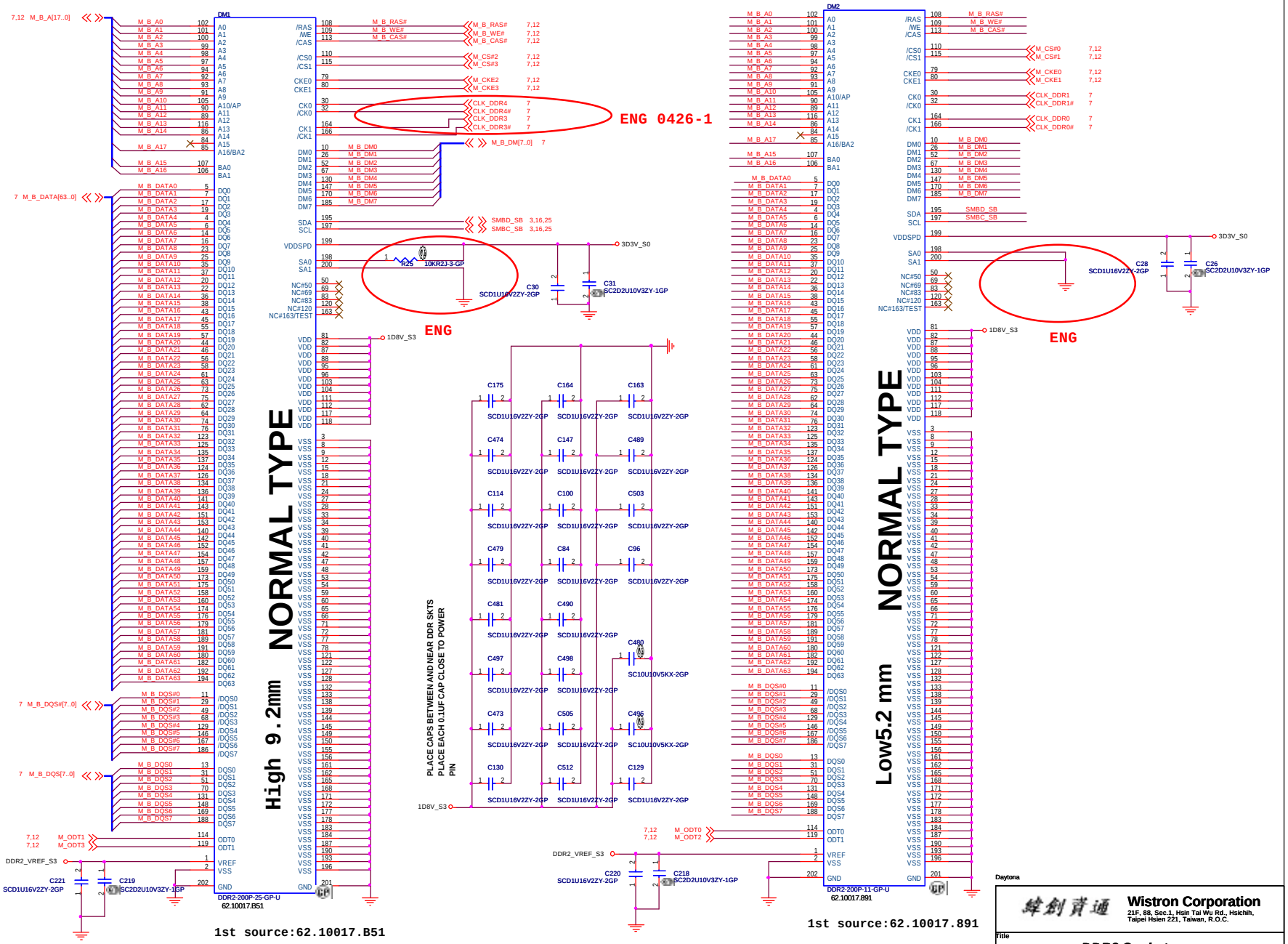
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RC415ME (5 of 5) Power*

Size	Document Number	Rev
A3	Daytona	-1

Date: Monday, June 12, 2006 Sheet 10 of 48


DM1
DM2
High 9.2mm NORMAL TYPE
Low5.2 mm NORMAL TYPE
ENG 0426-1
ENG
ENG
PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN
DDR2-200P-25-GP-U
62.10017.B51
DDR2-200P-11-GP-U
62.10017.891
1st source:62.10017.B51
1st source:62.10017.891
Daytona
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
Daytona
Rev
-1
Date: Wednesday, June 28, 2006
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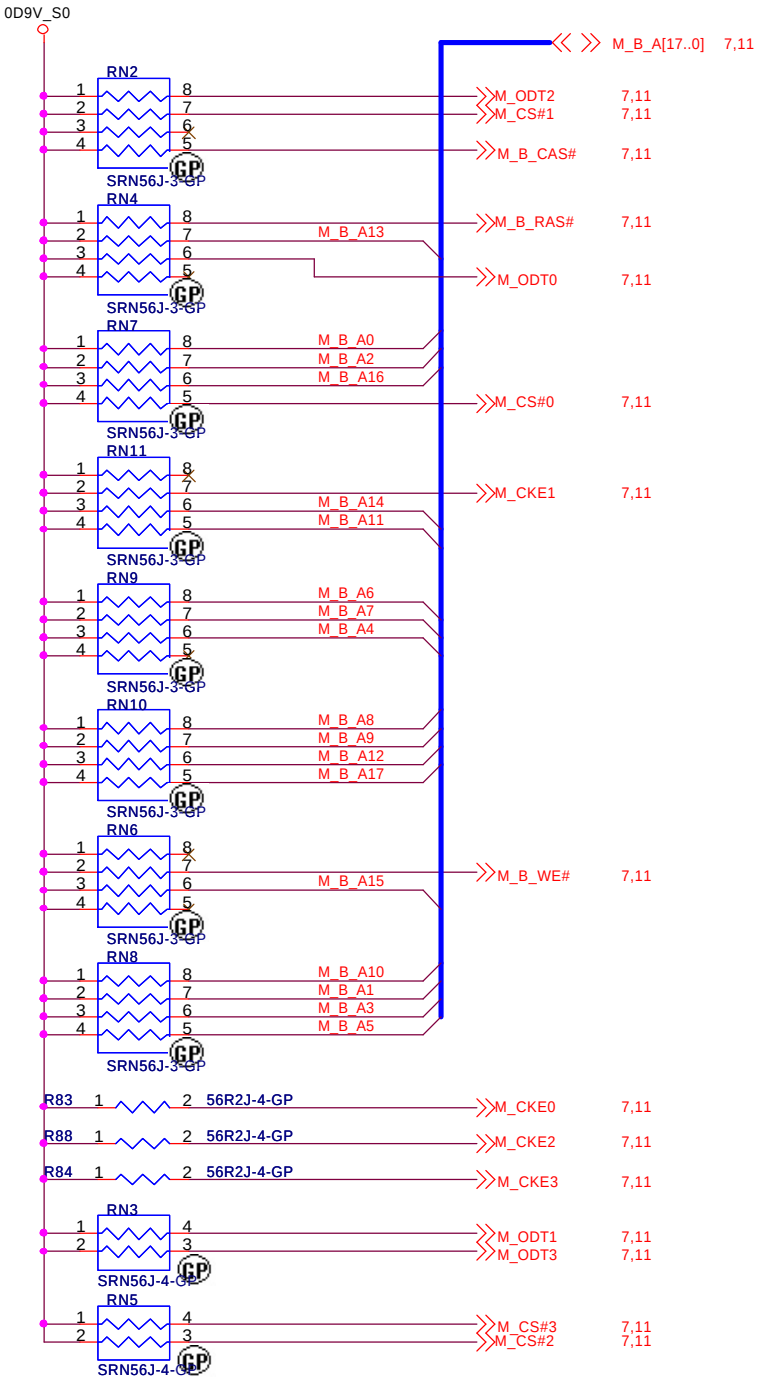
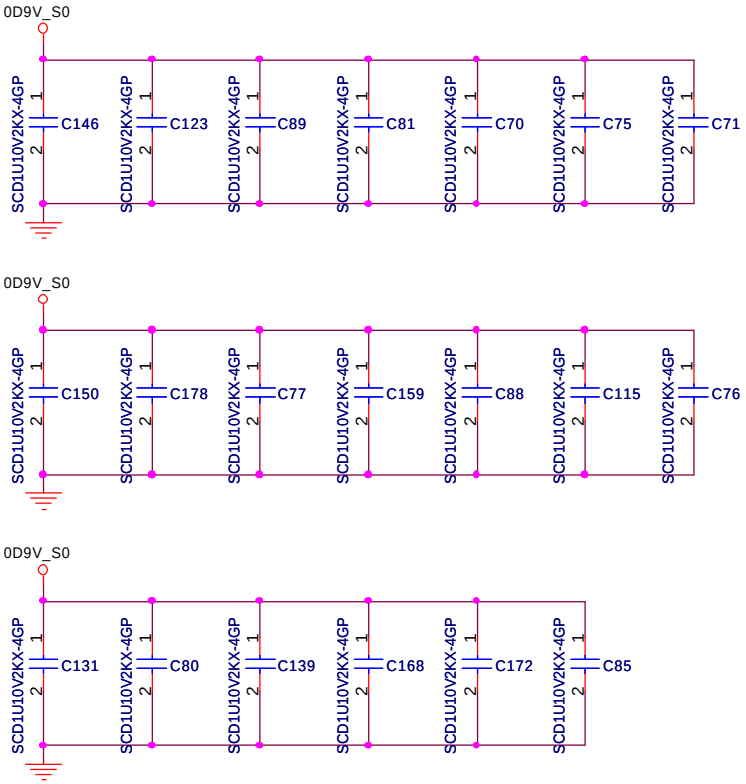
PARALLEL TERMINATION



PLACE 1 CAP FOR EVERY 2 BITS TERMINATED TO 0D9V_S0



Daytona

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Terminator Resistor***

Size	Document Number	Rev
A4	Daytona	-1

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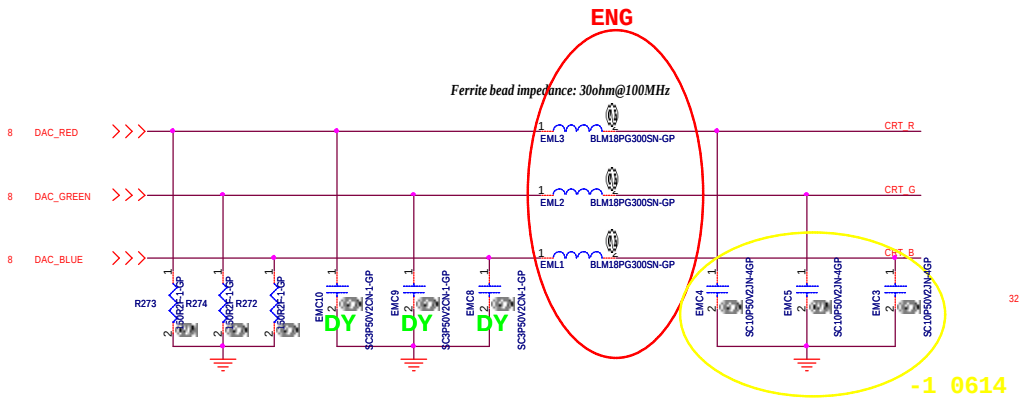
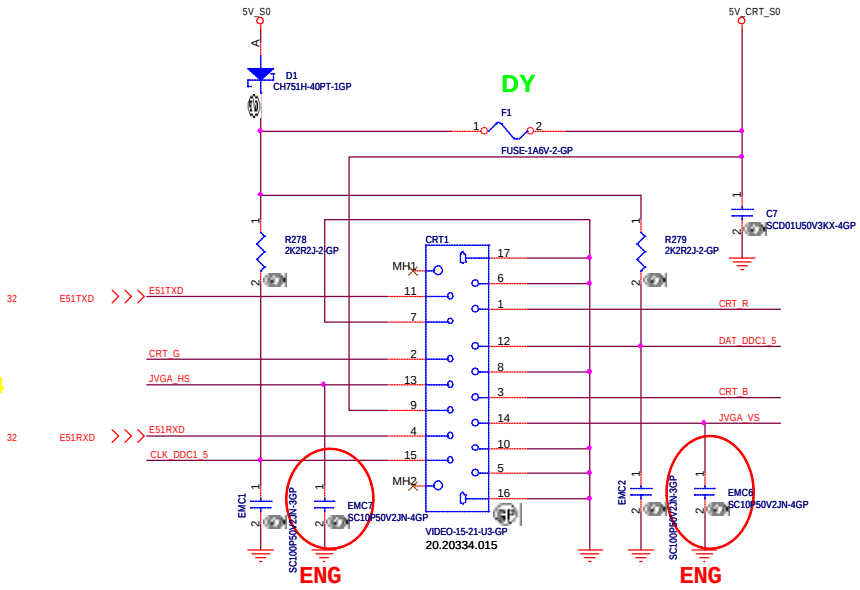
CRT I/F & CONNECTOR

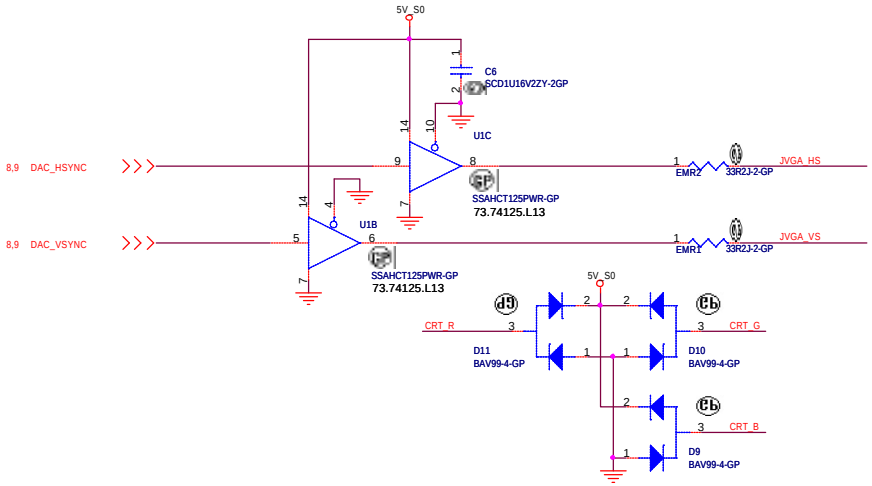




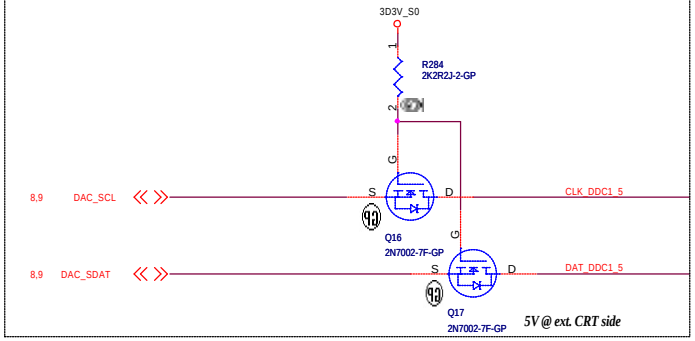
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.*

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



DAC_CLK & DATA level shift



Daytona

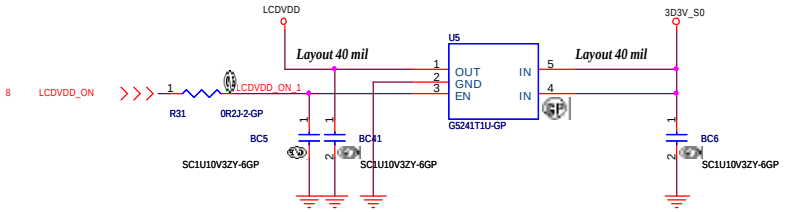
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

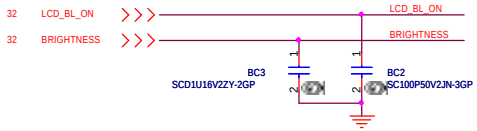
Title: *CRT Connector*

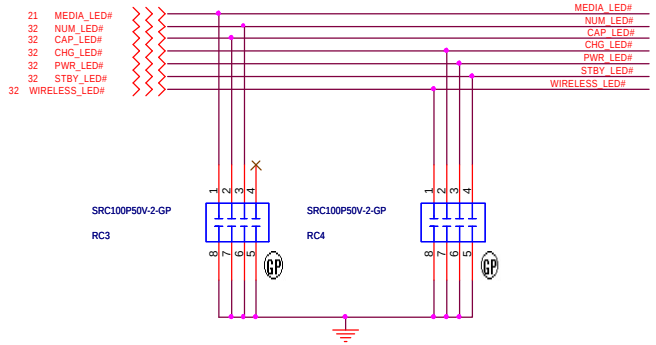
Size	Document Number	Rev
A3	Daytona	-1

Date: Wednesday, June 28, 2006 Sheet 13 of 48

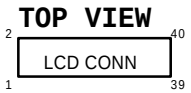
LCD & INVERTER INTERFACE

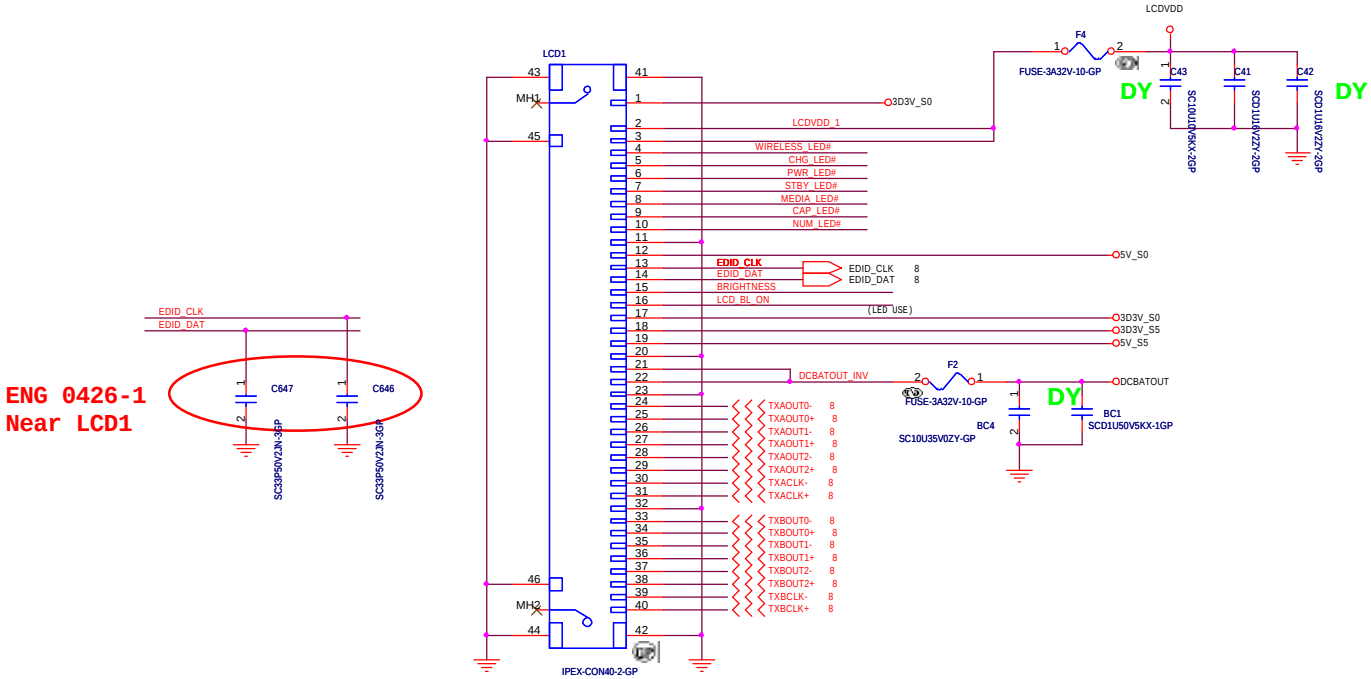






LCD CONN

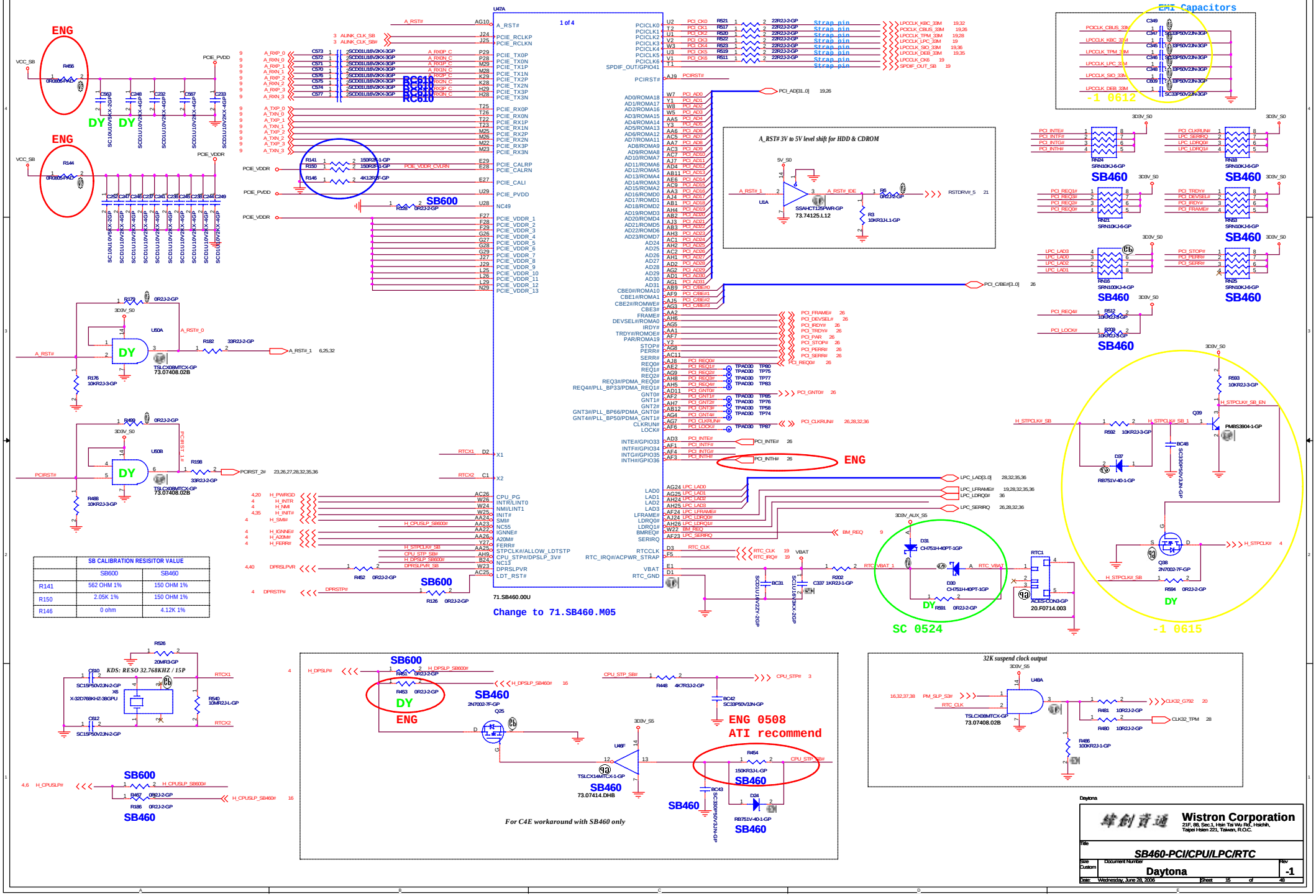


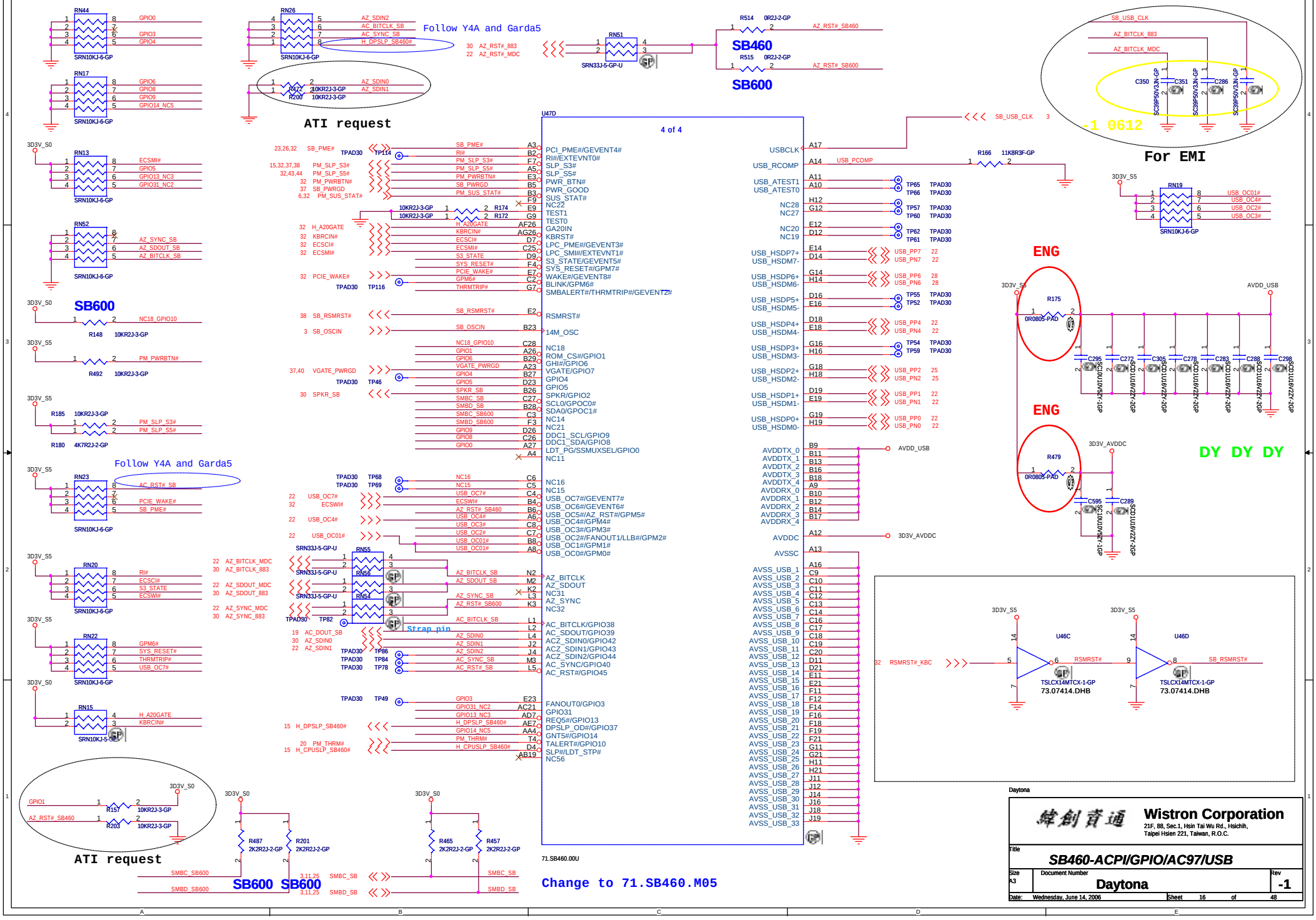


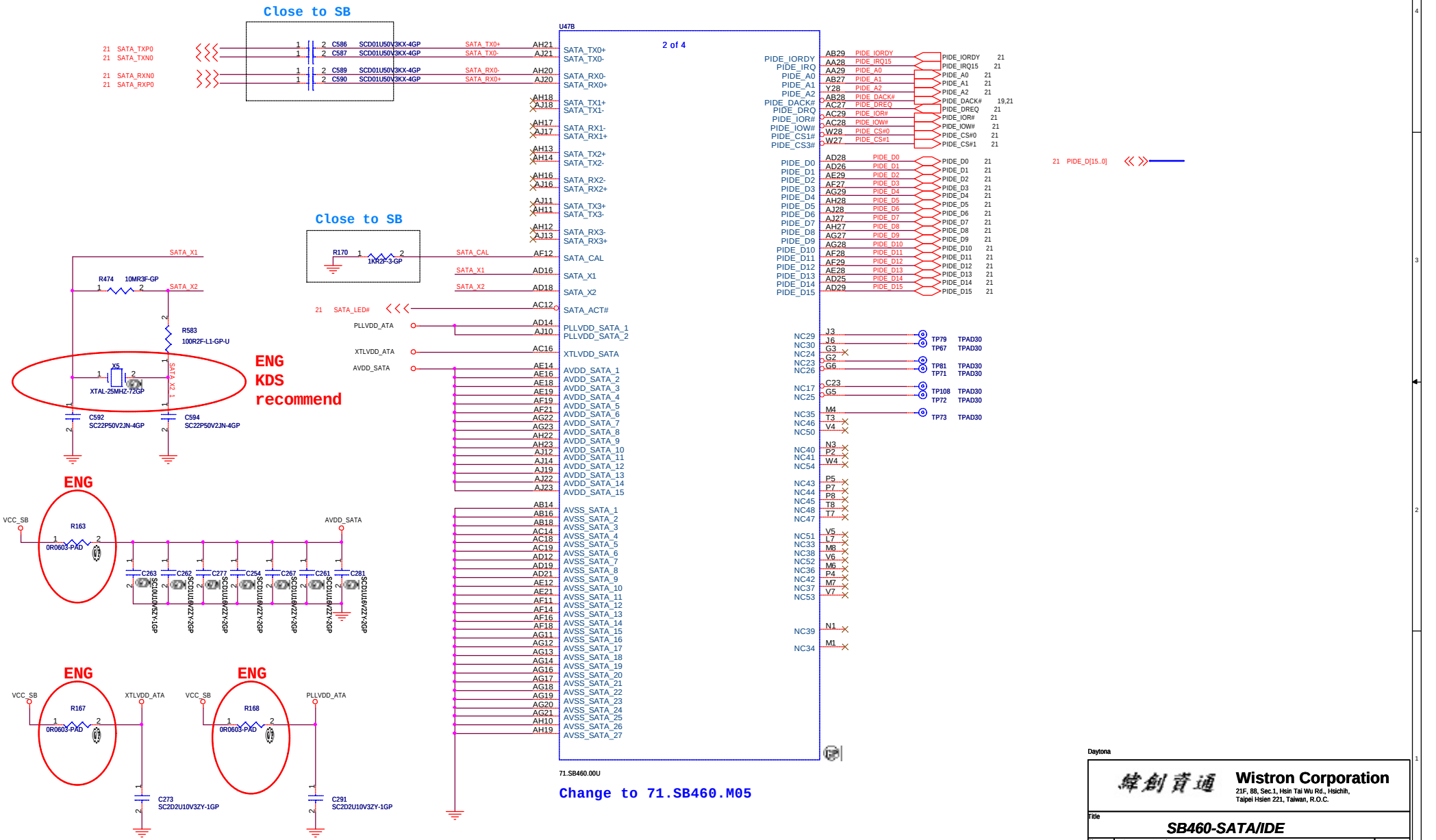
ENG 0426-1
Near LCD1

Daytona

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LCD & Inverter Connector*		
Size: A3	Document Number: Daytona	Rev: -1
Date: Tuesday, June 13, 2006	Sheet 14 of 48	


ENG
DY
SB600
SB460
RC610
EMI Capacitors
-1 0612
A_RST# 3V to 5V level shift for HDD & CDROM
SSAHCT125PWR-GP
73.74125.112
TSLCX08MTCX-GP
73.07408.02B
SB SB CALIBRATION RESISITOR VALUE
SB600
SB460
R141 562 OHM 1% 150 OHM 1%
R150 2.05K 1% 150 OHM 1%
R146 0 ohm 4.12K 1%
KDS: RESO 32.768KHZ / 15P
Change to 71.SB460.M05
SC 0524
-1 0615
ENG 0508
ATI recommend
For C4E workaround with SB460 only
32K suspend clock output
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB460-PCI/CPU/LPC/RTC
Daytona
Wednesday, June 28, 2006
15 of 48


RN44
GPIO0
GPIO3
GPIO4
SRN10KJ-6-GP
RN17
GPIO6
GPIO8
GPIO9
GPIO14_NC5
RN26
AZ_SDIN2
AC_BITCLK_SB
AC_SYNC_SB
H_DPSLP_SB460#
Follow Y4A and Garda5
30 AZ_RST#_883
22 AZ_RST#_MDC
RN51
SRN33J-5-GP-U
R514 0R2J-2-GP
AZ_RST#_SB460
SB460
R515 0R2J-2-GP
AZ_RST#_SB600
SB600
R472 10KR2J-3-GP
R200 10KR2J-3-GP
AZ_SDIN0
AZ_SDIN1
ATI request
SB_USB_CLK
AZ_BITCLK_883
AZ_BITCLK_MDC
C350
C351
C286
SC39P50V3JN-GP
-1 0612
For EMI
RN13
ECSMI#
GPIO5
GPIO13_NC3
GPIO31_NC2
RN52
AZ_SYNC_SB
AZ_SDOUT_SB
AZ_BITCLK_SB
SB600
R148 10KR2J-3-GP
NC18_GPIO10
R492 10KR2J-3-GP
PM_PWRBTN#
R185 10KR2J-3-GP
PM_SLP_S3#
PM_SLP_S5#
R180 4K7R2J-2-GP
Follow Y4A and Garda5
RN23
AC_RST#_SB
PCIE_WAKE#
SB_PME#
RN20
RI#
ECSCI#
S3_STATE
ECSWI#
22 AZ_BITCLK_MDC
30 AZ_BITCLK_883
22 AZ_SDOUT_MDC
30 AZ_SDOUT_883
22 AZ_SYNC_MDC
30 AZ_SYNC_883
RN22
GPM6#
SYS_RESET#
THRMTRIP#
USB_OC7#
RN15
H_A20GATE
KBRCIN#
GPIO1
AZ_RST#_SB460
R157 10KR2J-3-GP
R203 10KR2J-3-GP
ATI request
R487 2K2R2J-2-GP
R201 2K2R2J-2-GP
SB600
R465 2K2R2J-2-GP
R457 2K2R2J-2-GP
SB600
SMBC_SB600
SMBD_SB600
3,11,25 SMBC_SB
3,11,25 SMBD_SB
U47D
4 of 4
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
NC22
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT22#
RSMRST#
14M_OSC
NC18
ROM_CS#/GPIO1
GHI#/GPIO6
VGATE/GPIO7
GPIO4
GPIO5
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
NC14
NC21
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LDT_PG/SSMUXSEL/GPIO0
NC11
NC16
NC15
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/AZ_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/FANOUT1/LLB#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
NC31
AZ_SYNC
NC32
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
FANOUT0/GPIO3
GPIO31
REQ5#/GPIO13
DPSLP_OD#/GPIO37
GNT5#/GPIO14
TALERT#/GPIO10
SLP#/LDT_STP#
NC56
USBCLK
USB_RCOMP
USB_ATEST1
USB_ATEST0
NC28
NC27
NC20
NC19
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
AVSS_USB_25
AVSS_USB_26
AVSS_USB_27
AVSS_USB_28
AVSS_USB_29
AVSS_USB_30
AVSS_USB_31
AVSS_USB_32
AVSS_USB_33
71.SB460.00U
Change to 71.SB460.M05
R166 11K8R3F-GP
RN19
USB_OC01#
USB_OC4#
USB_OC2#
USB_OC3#
ENG
R175 0R0805-PAD
AVDD_USB
C295
C272
C305
C278
C283
C288
C298
SCD1U16V2ZY-2GP
SC10U10V3ZY-1GP
ENG
R479 0R0805-PAD
3D3V_AVDDC
C595
C289
DY DY DY
U46C
U46D
TSLCX14MTCX-1-GP
73.07414.DHB
RSMRST#_KBC
RSMRST#
SB_RSMRST#
Daytona
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB460-ACPI/GPIO/AC97/USB
Size A3
Document Number
Daytona
Rev -1
Date: Wednesday, June 14, 2006
Sheet 16 of 48



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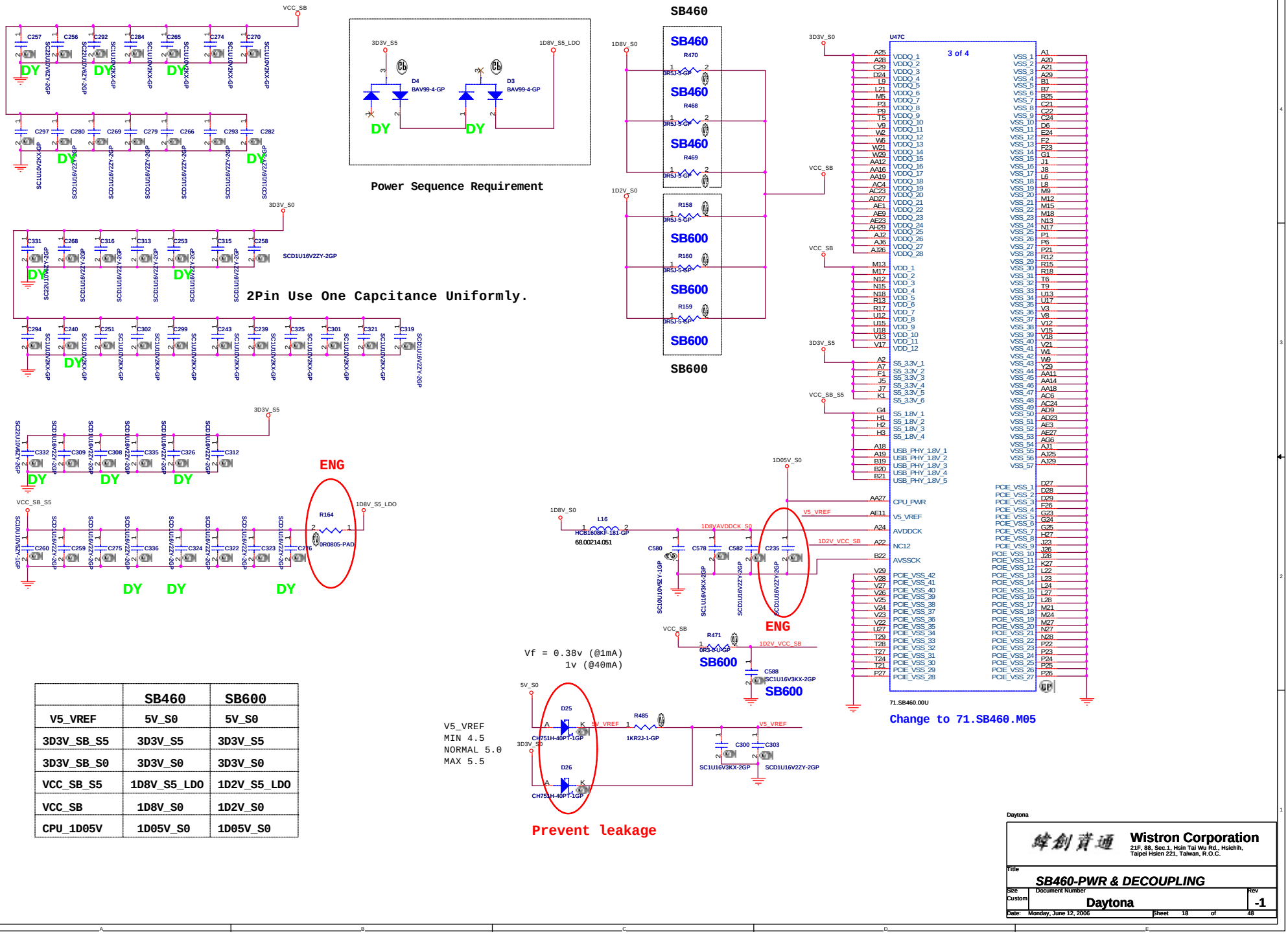
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB460-SATA/IDE

Size	Document Number	Rev
A3	Daytona	-1

Date: Tuesday, June 13, 2006 Sheet 17 of 48



	SB460	SB600
V5_VREF	5V_S0	5V_S0
3D3V_SB_S5	3D3V_S5	3D3V_S5
3D3V_SB_S0	3D3V_S0	3D3V_S0
VCC_SB_S5	1D8V_S5_LDO	1D2V_S5_LDO
VCC_SB	1D8V_S0	1D2V_S0
CPU_1D05V	1D05V_S0	1D05V_S0

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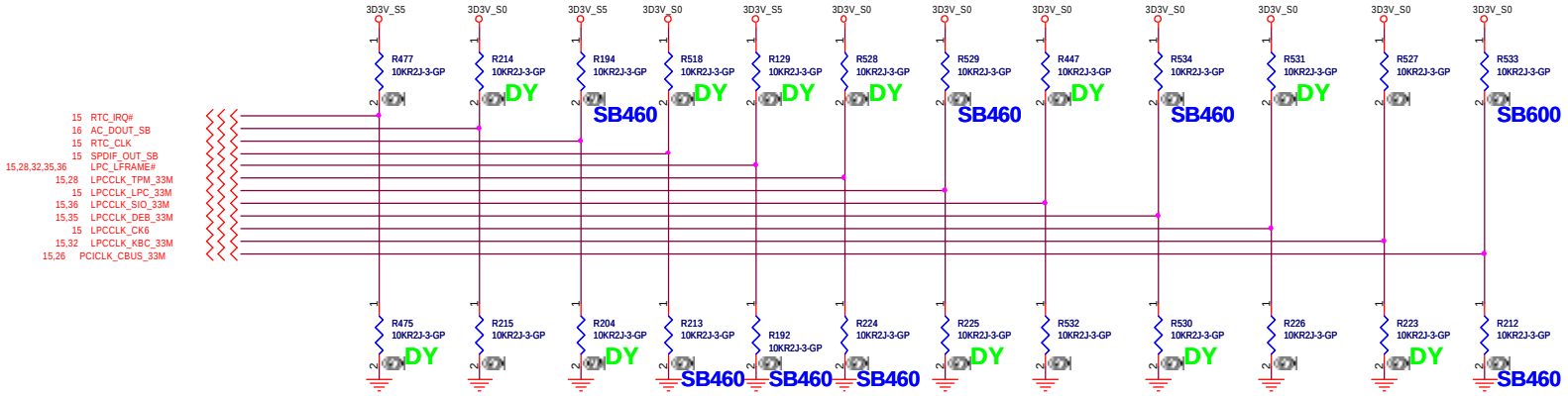
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB460-PWR & DECOUPLING**

Size	Document Number	Rev
Custom	Daytona	-1

Date: Monday, June 12, 2006 Sheet 18 of 48



REQUIRED STRAPS

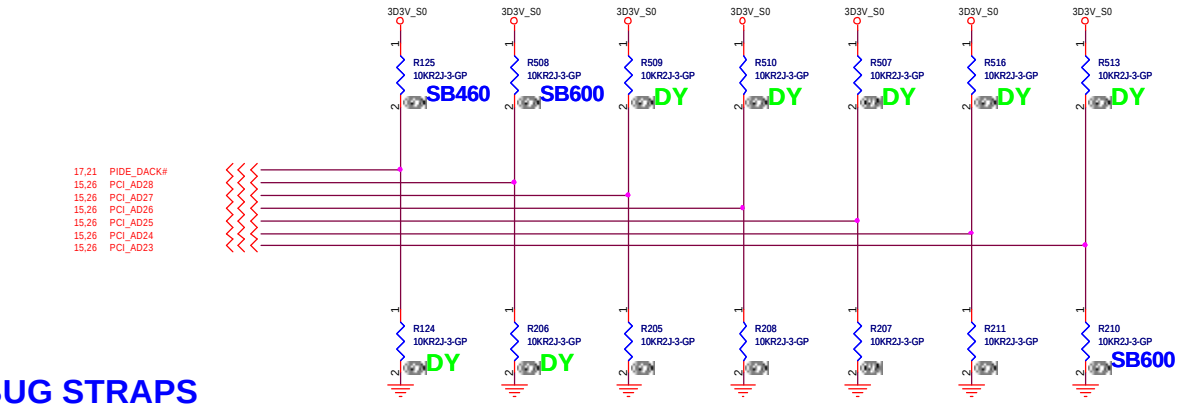
PCI_CLK0 LPCCLK_KBC_33M
PCI_CLK1 PCICLK_CBUS_33M
PCI_CLK2 LPCCLK_TPM_33M
PCI_CLK3 LPCCLK_LPC_33M
PCI_CLK4 LPCCLK_SIO_33M
PCI_CLK5 LPCCLK_DEB_33M
PCI_CLK6 LPCCLK_CK6

	AC_DOUT_SB	RTC_CLK	PCI_CLK4	PCI_CLK6	SB600 PCI_CLK0 / PCI_CLK1	SB460 PCI_CLK0 / PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM	ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM DEFAULT; L, H = LPC II ROM; L, L = FWH ROM. NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT		

SB460 ONLY STRAPS

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#
	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY	SB460 ONLY

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



2.2K IF USED FOR SB600.
10K IF USED FOR SB460.

DEBUG STRAPS

	PIDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED
	SB460 ONLY	SB600 ONLY					SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

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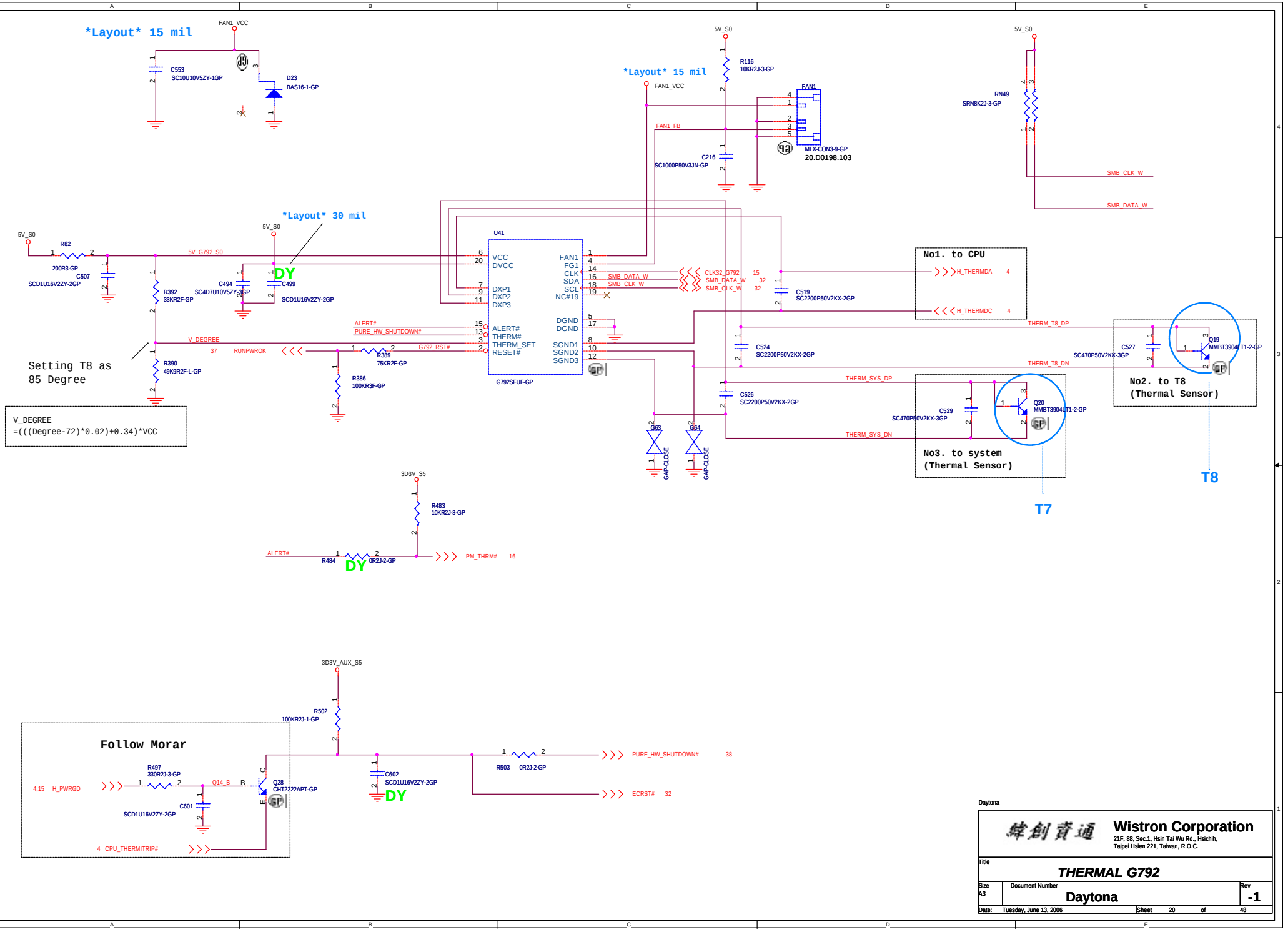
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB450-STRAPPING(5 of 5)

Size: A3 | Document Number: Daytona | Rev: -1

Date: Tuesday, June 13, 2006 | Sheet 19 of 48



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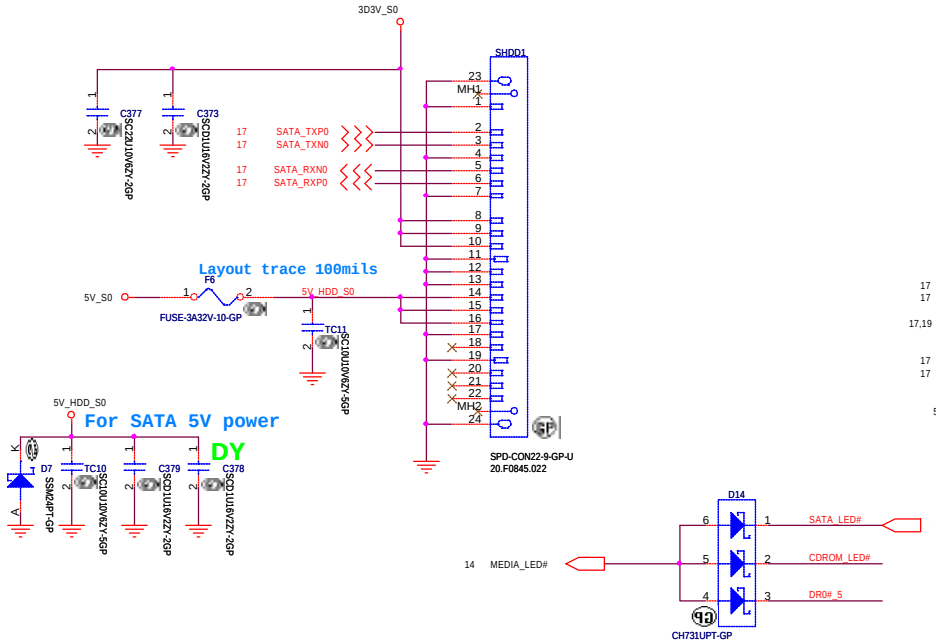
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL G792

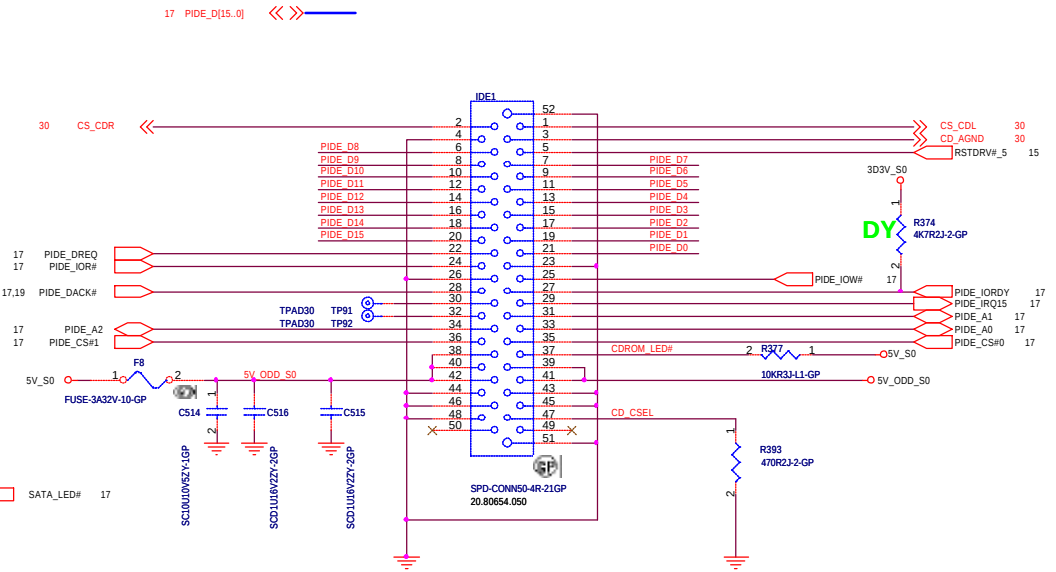
Size	Document Number	Rev
A3	Daytona	-1

Date: Tuesday, June 13, 2006 Sheet 20 of 48

SATA HDD Connector

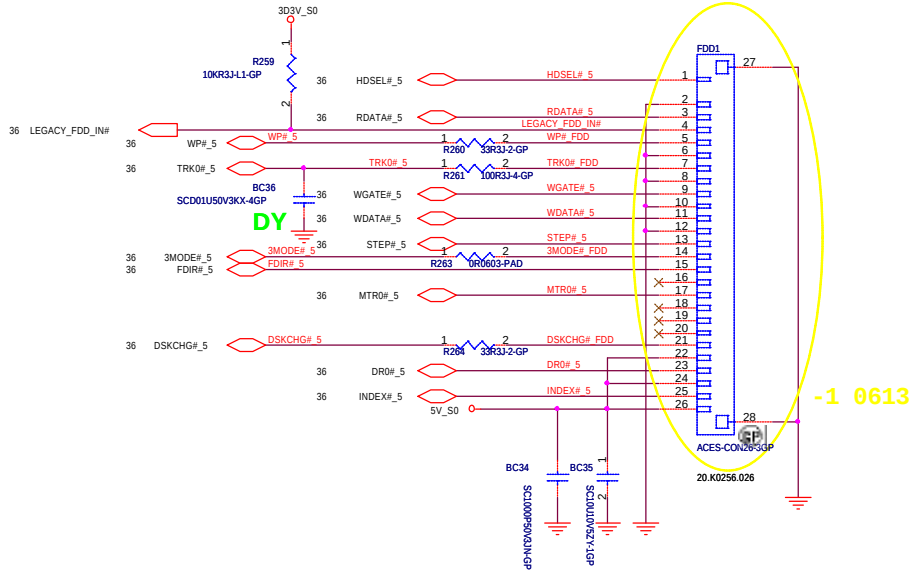


CD-ROM CONN



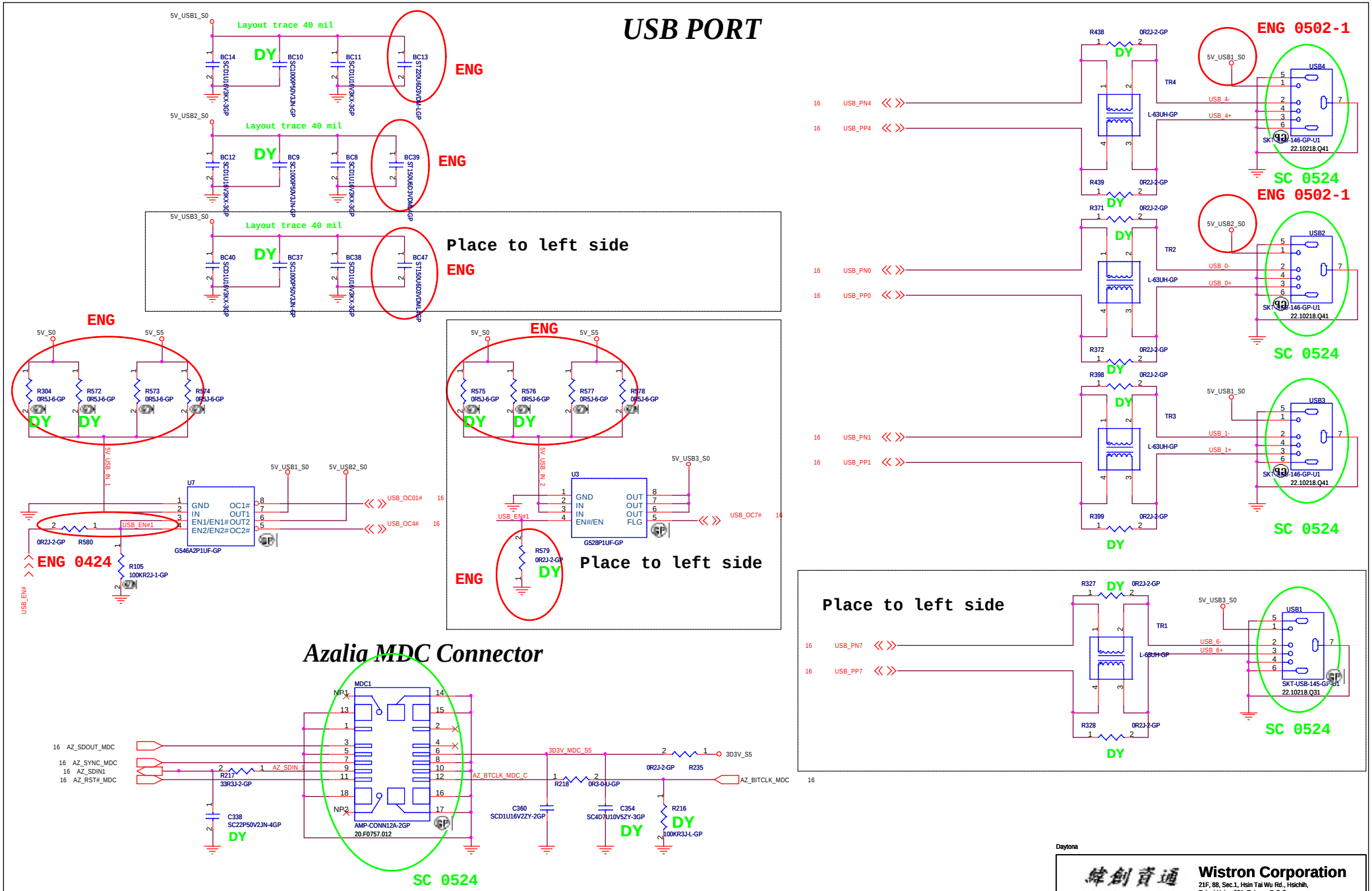
FDD Connector

ENG FDD PIN DEFIND SWAP



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD / ODD / FDD CONN		
Size: A3	Document Number: Daytona	Rev: -1
Date: Wednesday, June 14, 2006	Sheet 21 of 48	

USB PORT



Azalia MDC Connector

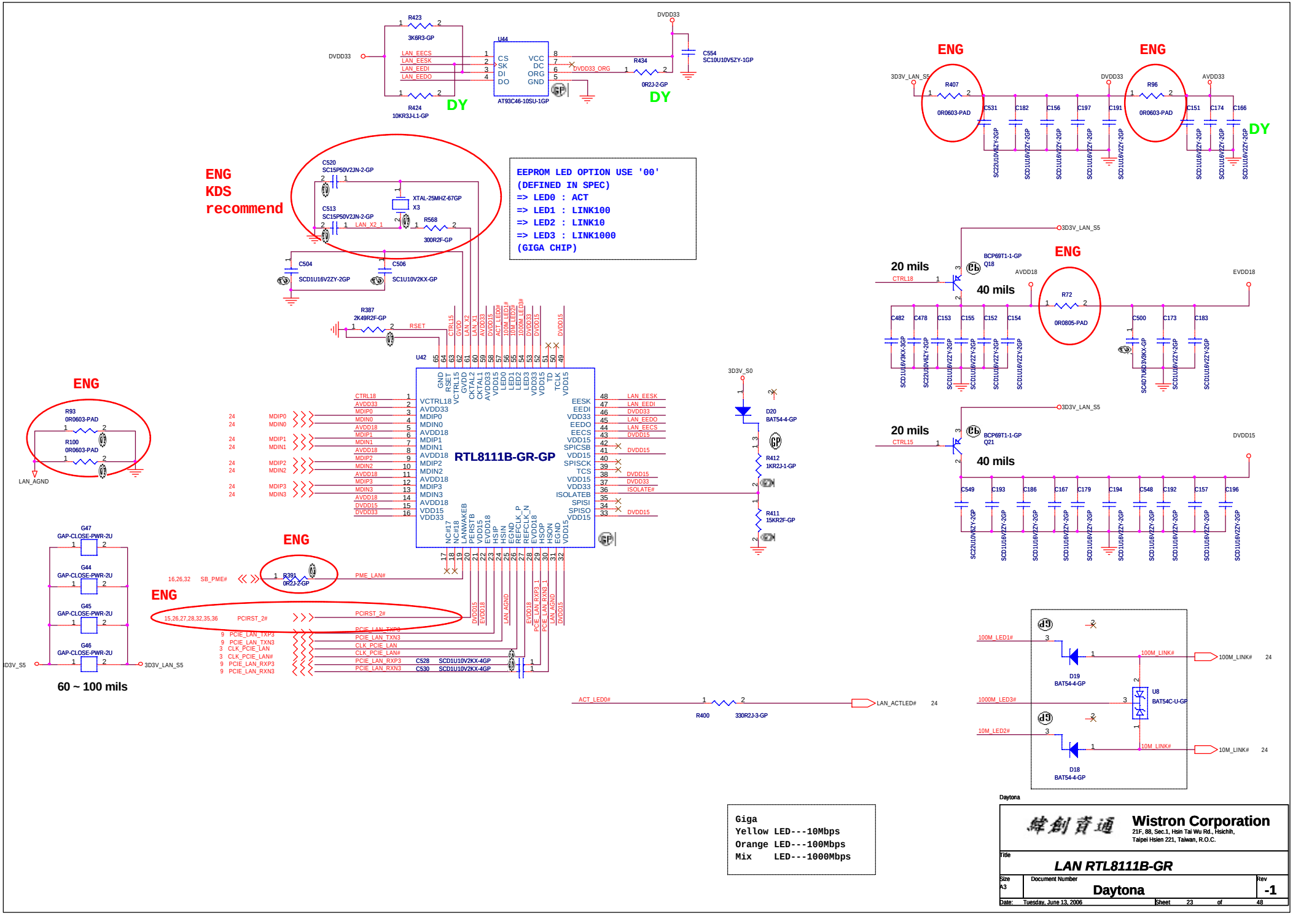
Daytona

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC Connector

Size	Document Number	Rev
A3	Daytona	-1

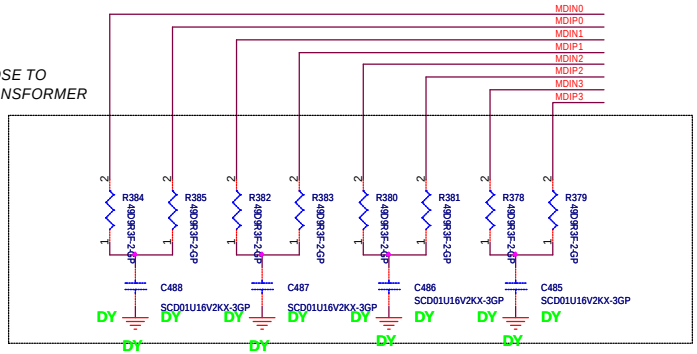
Date: Tuesday, July 25, 2006 Sheet 22 of 48

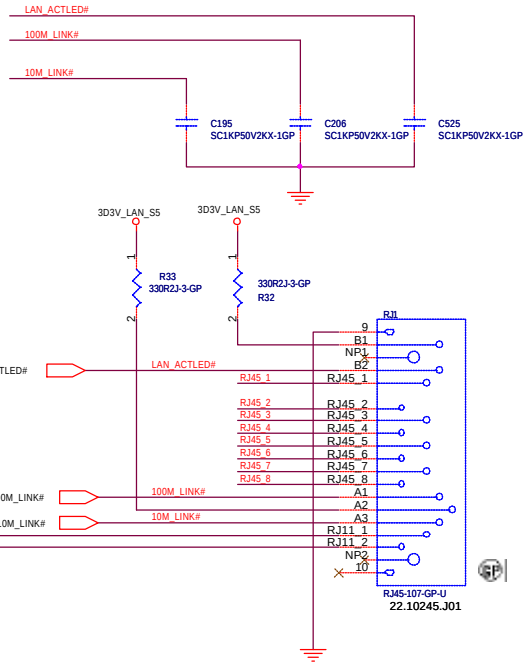

ENG
KDS
recommend
EEPROM LED OPTION USE '00'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK100
=> LED2 : LINK10
=> LED3 : LINK1000
(GIGA CHIP)
RTL8111B-GR-GP
U42
U44
AT93C46-10SU-1GP
DY
ENG
20 mils
40 mils
60 ~ 100 mils
Giga
Yellow LED---10Mbps
Orange LED---100Mbps
Mix LED---1000Mbps
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN RTL8111B-GR
Daytona
Tuesday, June 13, 2006
Sheet 23 of 48

LAN Connector

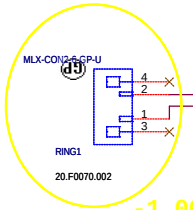
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

CLOSE TO TRANSFORMER

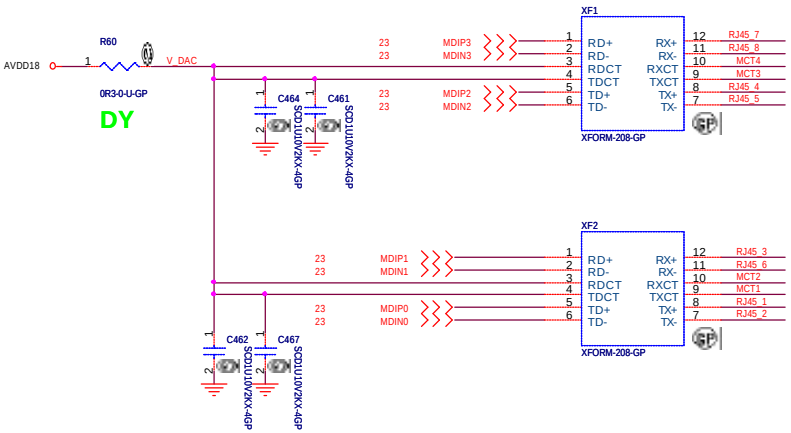


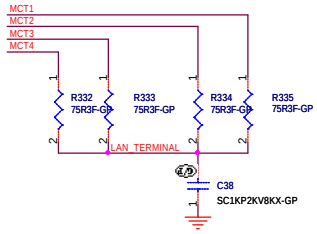


10/100/1000Mbps Lan Transformer



-1 0615





DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

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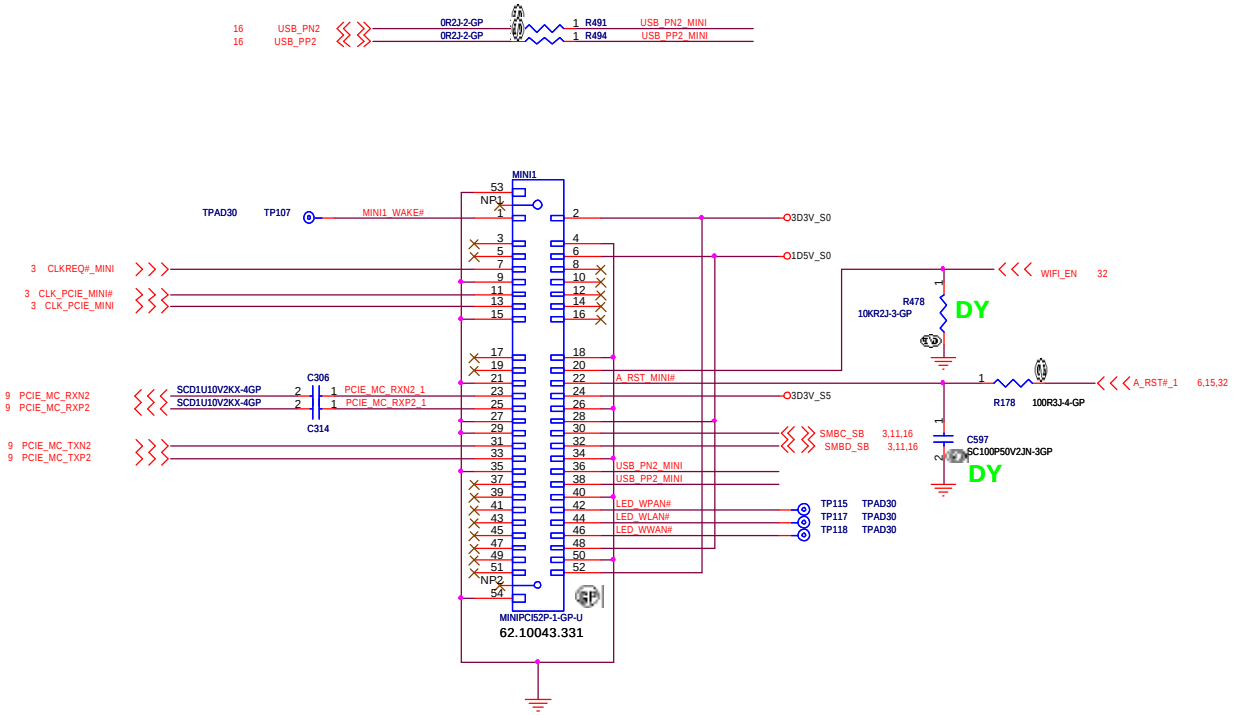
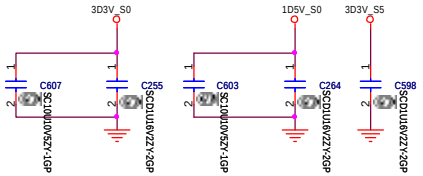
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN Connector	
Size A3	Document Number Daytona	Rev -1
Date: Wednesday, June 28, 2006	Sheet 24 of 48	

Mini Card Connector





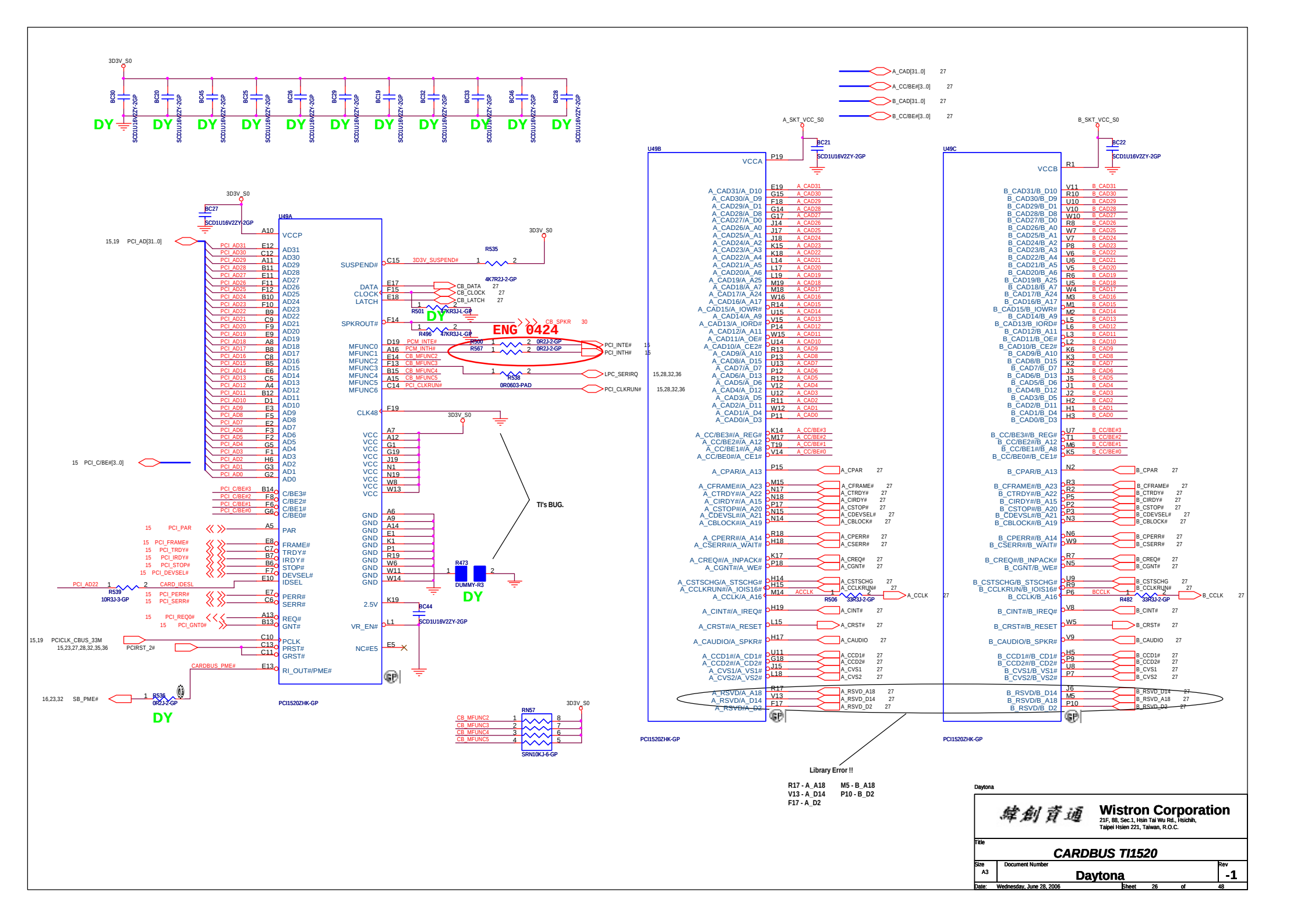
Daytona

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD

Size	Document Number	Rev
A3	Daytona	-1

Date: Tuesday, June 13, 2006 Sheet 25 of 48


3D3V_S0
BC30
BC20
BC45
BC25
BC26
BC29
BC19
BC32
BC33
BC46
BC28
SCD1U16V2ZY-2GP
DY
U49A
PCI1520ZHK-GP
U49B
U49C
BC27
BC21
BC22
A_SKT_VCC_S0
B_SKT_VCC_S0
A_CAD[31..0] 27
A_CC/BE#[3..0] 27
B_CAD[31..0] 27
B_CC/BE#[3..0] 27
15,19 PCI_AD[31..0]
15 PCI_C/BE#[3..0]
15,19 PCICLK_CBUS_33M
15,23,27,28,32,35,36 PCIRST_2#
16,23,32 SB_PME#
CARDBUS_PME#
CARD_IDSEL
SUSPEND#
3D3V_SUSPEND#
R535 4K7R2J-2-GP
DATA
CLOCK
LATCH
CB_DATA 27
CB_CLOCK 27
CB_LATCH 27
R501 47KR3J-GP
SPKROUT#
CB_SPKR 30
R496 47KR3J-GP
ENG 0424
R500 0R2J-2-GP
R567 0R2J-2-GP
PCI_INTE# 15
PCI_INTH# 15
MFUNC0 PCM_INT#
MFUNC1
MFUNC2 CB_MFUNC2
MFUNC3 CB_MFUNC3
MFUNC4 CB_MFUNC4
MFUNC5 CB_MFUNC5
MFUNC6 PCI_CLKRUN#
R538 0R0603-PAD
LPC_SERIRQ 15,28,32,36
PCI_CLKRUN# 15,28,32,36
CLK48
TI's BUG.
R473 DUMMY-R3
DY
2.5V
VR_EN#
NC#E5
BC44
R539 10R3J-3-GP
R536 0R2J-2-GP
RN57 SRN10KJ-6-GP
CB_MFUNC2
CB_MFUNC3
CB_MFUNC4
CB_MFUNC5
R506 33R3J-2-GP
R482 33R3J-2-GP
ACCLK
BCCLK
A_CCLK 27
B_CCLK 27
Library Error !!
R17 - A_A18
V13 - A_D14
F17 - A_D2
M5 - B_A18
P10 - B_D2
Daytona
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
CARDBUS TI1520
Size A3
Document Number Daytona
Rev -1
Date: Wednesday, June 28, 2006
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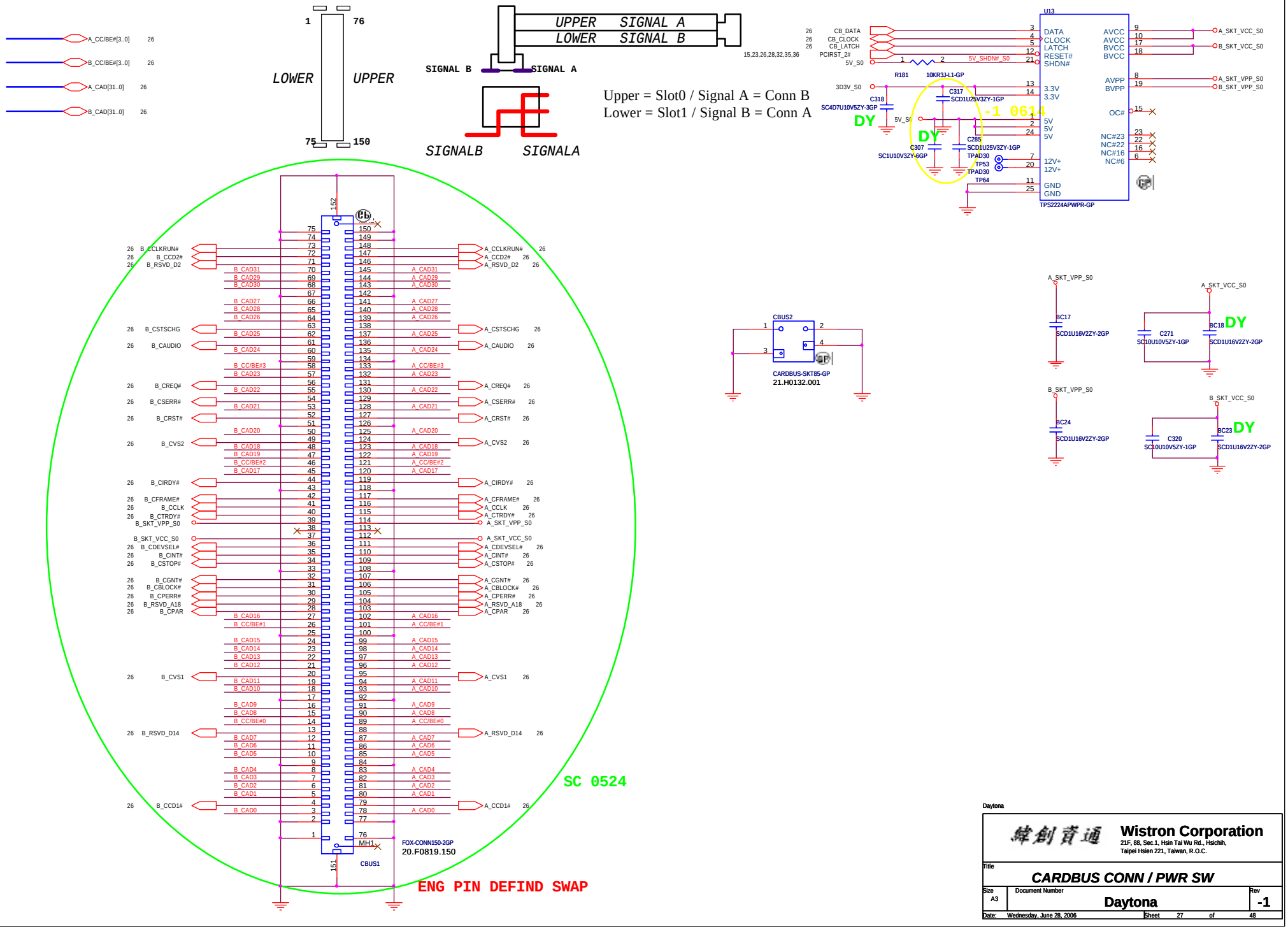
A_CC/BE#[3..0] 26
B_CC/BE#[3..0] 26
A_CAD[31..0] 26
B_CAD[31..0] 26
1
76
LOWER
UPPER
75
150
UPPER SIGNAL A
LOWER SIGNAL B
SIGNAL B
SIGNAL A
SIGNALB
SIGNALA
15,23,26,28,32,35,36
Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A
U13
DATA
CLOCK
LATCH
RESET#
SHDN#
3.3V
5V
12V+
GND
AVCC
BVCC
AVPP
BVPP
OC#
NC#23
NC#22
NC#16
NC#6
TPS2224APWPR-GP
CB_DATA
CB_CLOCK
CB_LATCH
PCIRST_2#
5V_S0
3D3V_S0
5V_SHDN#_S0
R181
10KR3J-L1-GP
C317
SCD1U25V3ZY-1GP
C318
SC4D7U10V5ZY-3GP
C307
SC1U10V3ZY-6GP
C285
TPAD30
TP53
TP64
DY
-1 0614
A_SKT_VCC_S0
B_SKT_VCC_S0
A_SKT_VPP_S0
B_SKT_VPP_S0
CBUS2
CARDBUS-SKT85-GP
21.H0132.001
BC17
BC18
BC24
BC23
C271
C320
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
B_CCLKRUN#
B_CCD2#
B_RSVD_D2
B_CSTSCHG
B_CAUDIO
B_CREQ#
B_CSERR#
B_CRST#
B_CVS2
B_CIRDY#
B_CFRAME#
B_CCLK
B_CTRDY#
B_SKT_VPP_S0
B_SKT_VCC_S0
B_CDEVSEL#
B_CINT#
B_CSTOP#
B_CGNT#
B_CBLOCK#
B_CPERR#
B_RSVD_A18
B_CPAR
B_CVS1
B_RSVD_D14
B_CCD1#
A_CCLKRUN#
A_CCD2#
A_RSVD_D2
A_CSTSCHG
A_CAUDIO
A_CREQ#
A_CSERR#
A_CRST#
A_CVS2
A_CIRDY#
A_CFRAME#
A_CCLK
A_CTRDY#
A_SKT_VPP_S0
A_SKT_VCC_S0
A_CDEVSEL#
A_CINT#
A_CSTOP#
A_CGNT#
A_CBLOCK#
A_CPERR#
A_RSVD_A18
A_CPAR
A_CVS1
A_RSVD_D14
A_CCD1#
B_CAD31
B_CAD29
B_CAD30
B_CAD27
B_CAD28
B_CAD26
B_CAD25
B_CAD24
B_CC/BE#3
B_CAD23
B_CAD22
B_CAD21
B_CAD20
B_CAD18
B_CAD19
B_CC/BE#2
B_CAD17
B_CAD16
B_CC/BE#1
B_CAD15
B_CAD14
B_CAD13
B_CAD12
B_CAD11
B_CAD10
B_CAD9
B_CAD8
B_CC/BE#0
B_CAD7
B_CAD6
B_CAD5
B_CAD4
B_CAD3
B_CAD2
B_CAD1
B_CAD0
A_CAD31
A_CAD29
A_CAD30
A_CAD27
A_CAD28
A_CAD26
A_CAD25
A_CAD24
A_CC/BE#3
A_CAD23
A_CAD22
A_CAD21
A_CAD20
A_CAD18
A_CAD19
A_CC/BE#2
A_CAD17
A_CAD16
A_CC/BE#1
A_CAD15
A_CAD14
A_CAD13
A_CAD12
A_CAD11
A_CAD10
A_CAD9
A_CAD8
A_CC/BE#0
A_CAD7
A_CAD6
A_CAD5
A_CAD4
A_CAD3
A_CAD2
A_CAD1
A_CAD0
MH1
FOX-CONN150-2GP
20.F0819.150
CBUS1
SC 0524
ENG PIN DEFIND SWAP
Daytona
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
CARDBUS CONN / PWR SW
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A3
Document Number
Daytona
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-1
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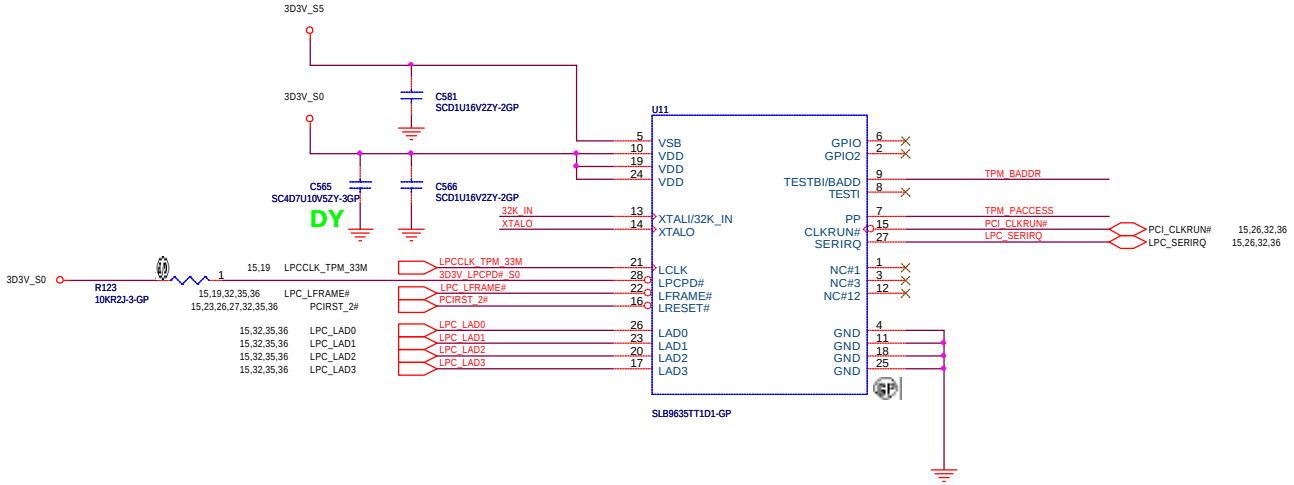
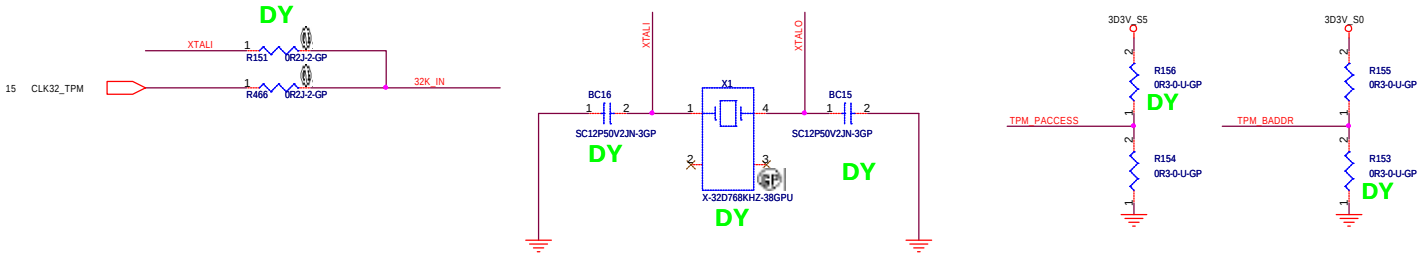
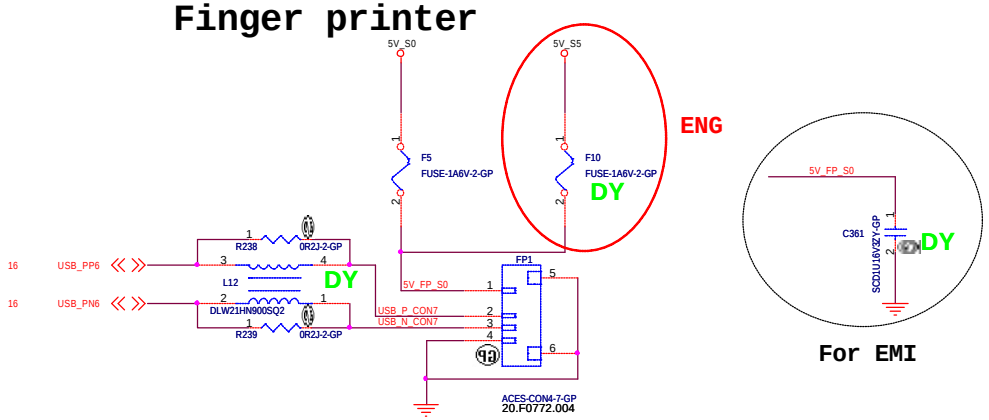
TPM 1.2





Finger printer



For EMI

Daytona

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPM 1.2 / FP***	
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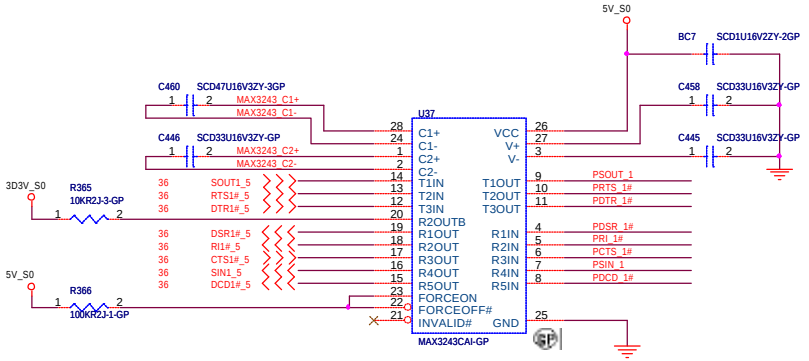
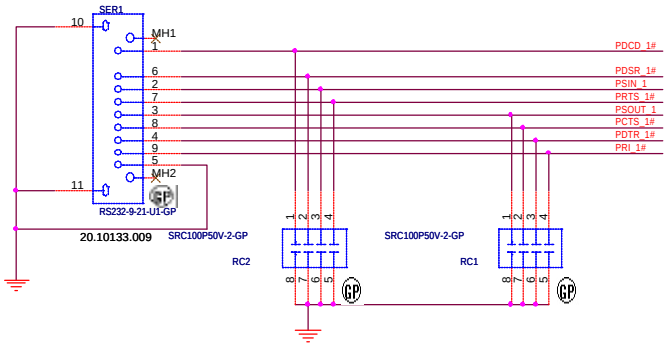
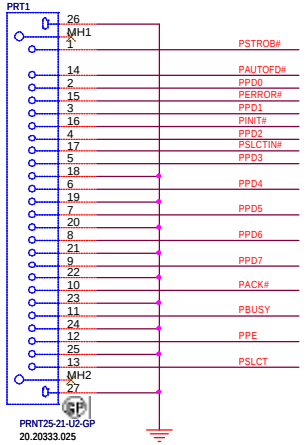
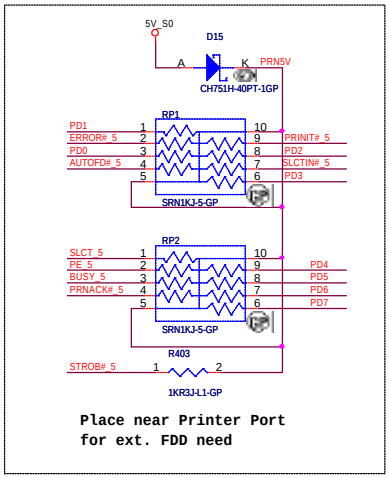
SERIAL PORT

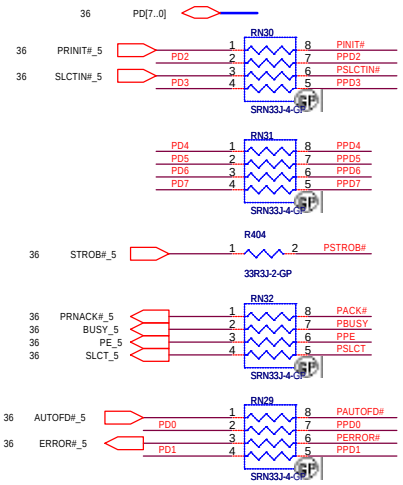


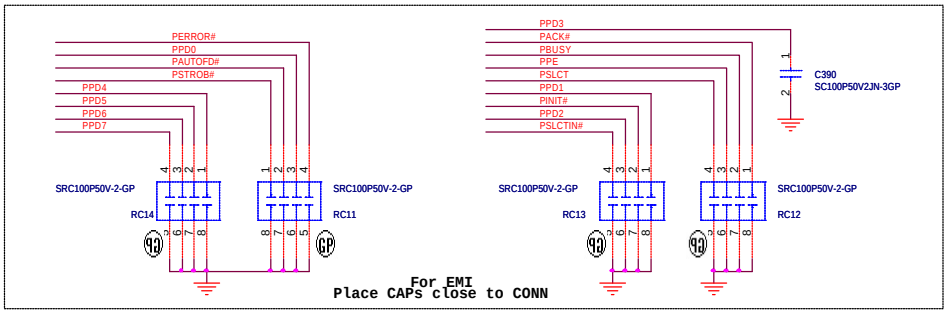


PRINTER PORT









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Title: *Parallel Port / Serial Port*

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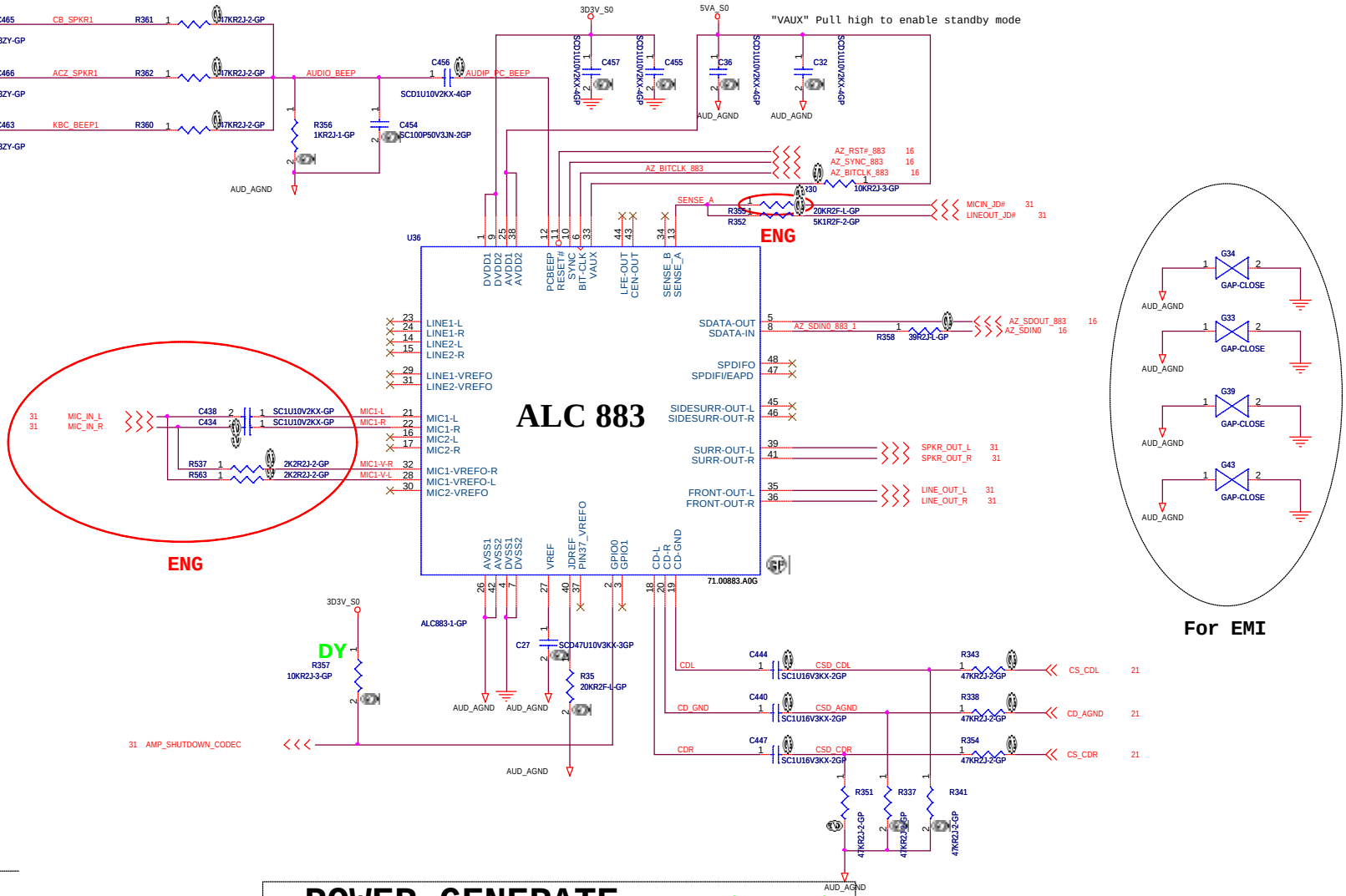

1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input

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Title: Azalia Codec_ALC883

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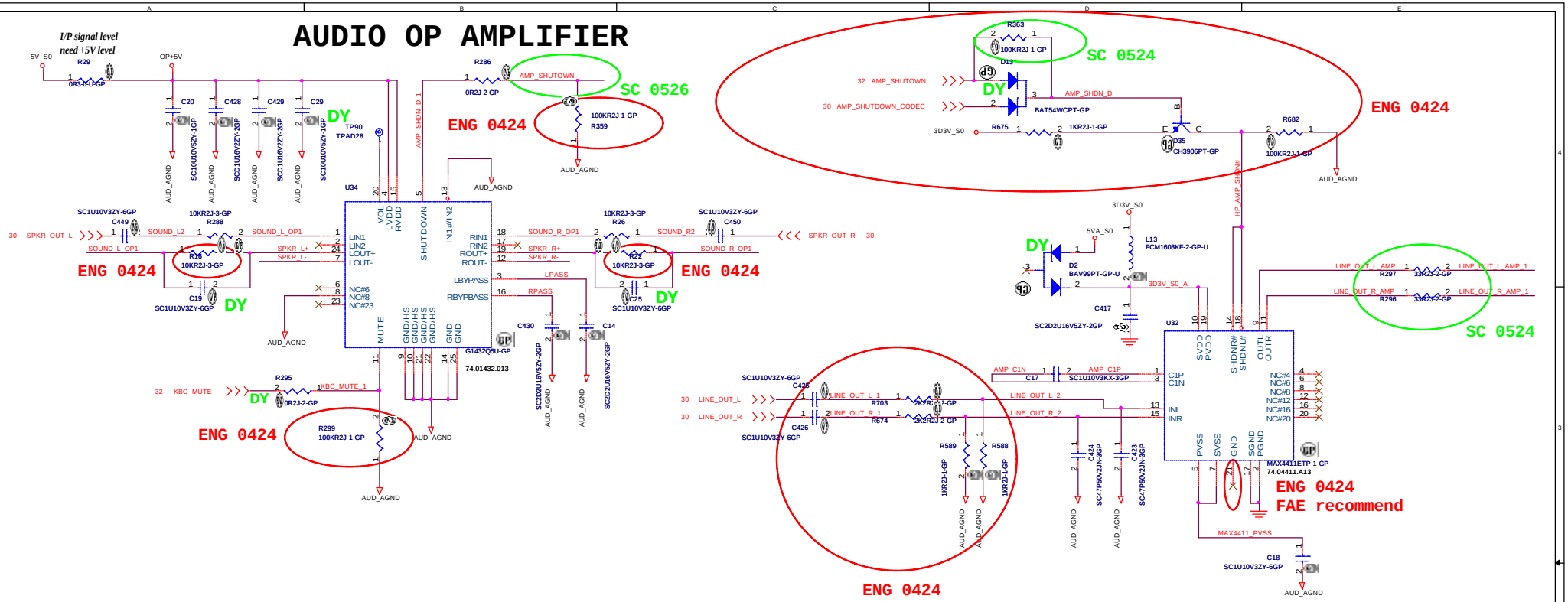
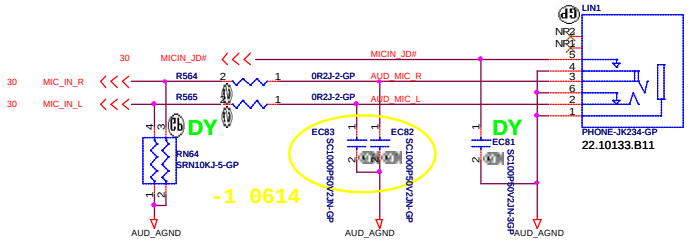
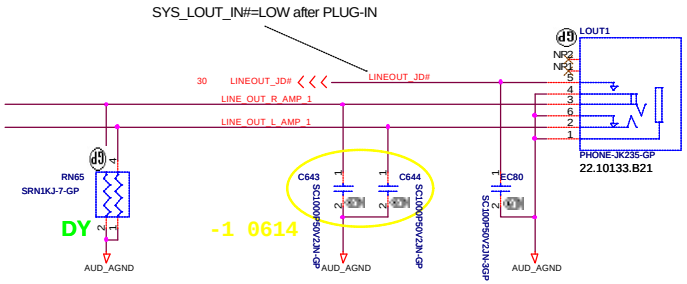
AUDIO OP AMPLIFIER



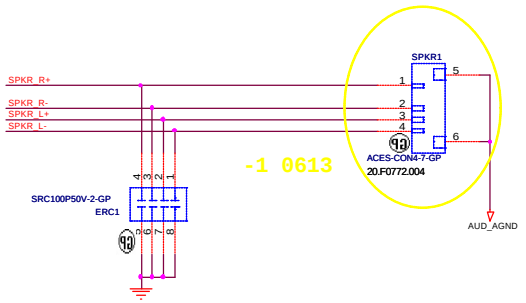
MIC IN ENG Modify



LINE OUT ENG Modify



Internal Speaker



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio AMP and Jack	
Size: Custom	Document Number: Daytona	Rev: -1
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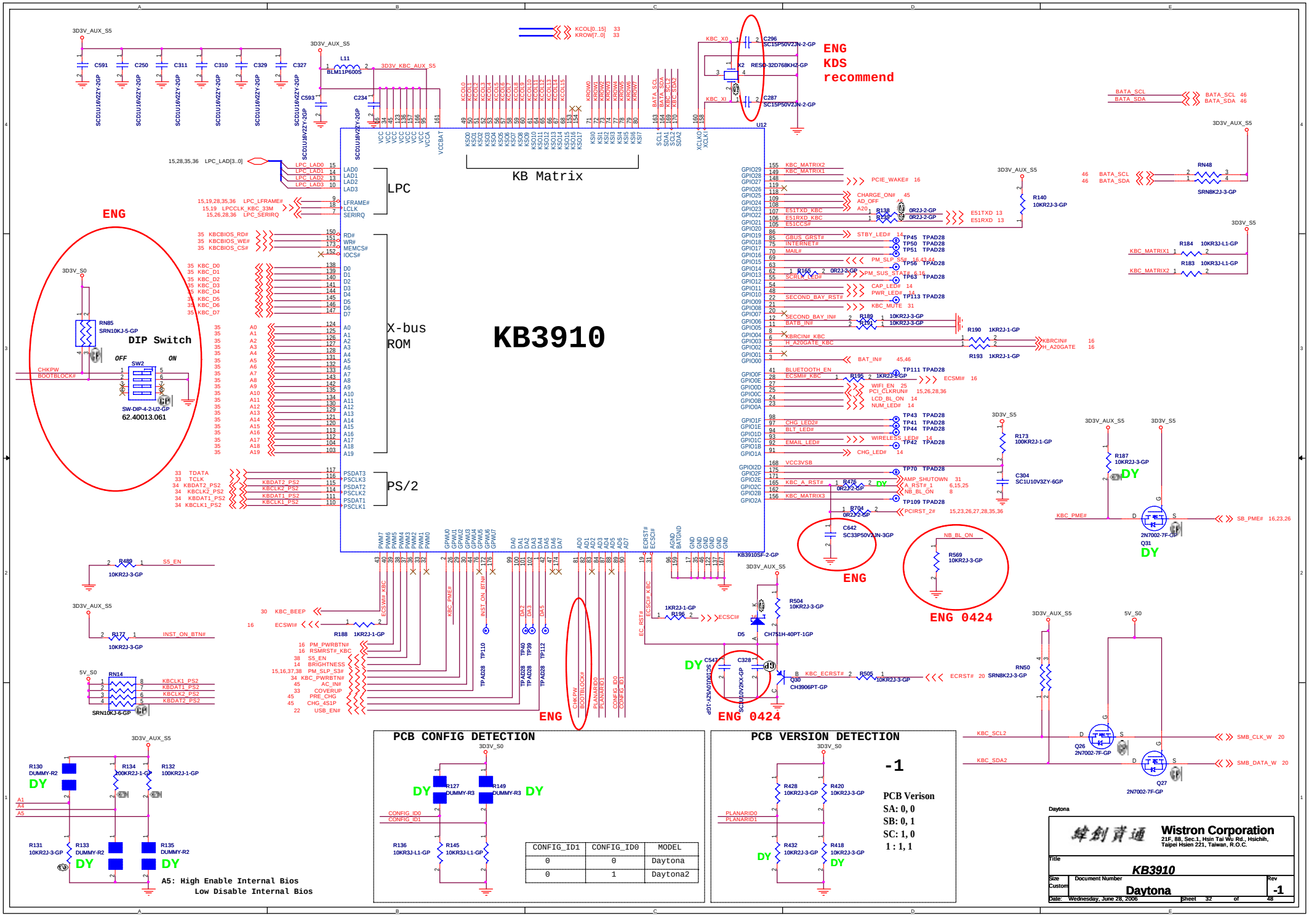
KB3910
ENG
KDS
recommend
LPC
X-bus
ROM
PS/2
KB Matrix
DIP Switch
62.40013.061
ENG 0424
PCB CONFIG DETECTION
PCB VERSION DETECTION
-1
PCB Verison
SA: 0, 0
SB: 0, 1
SC: 1, 0
1 : 1, 1
CONFIG_ID1 | CONFIG_ID0 | MODEL
0 | 0 | Daytona
0 | 1 | Daytona2
A5: High Enable Internal Bios
Low Disable Internal Bios
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KB3910
Size
Custom
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Daytona
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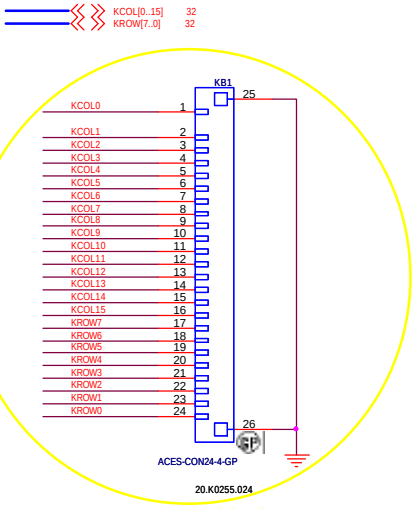
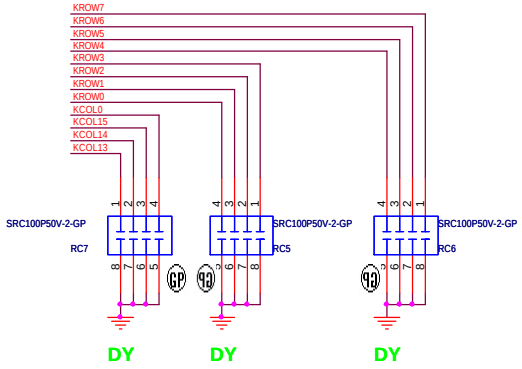
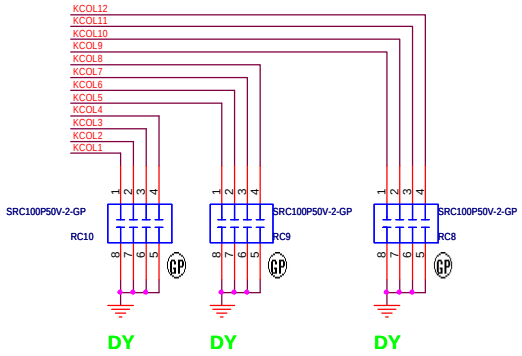
ENG 0502

Internal KeyBoard Connector



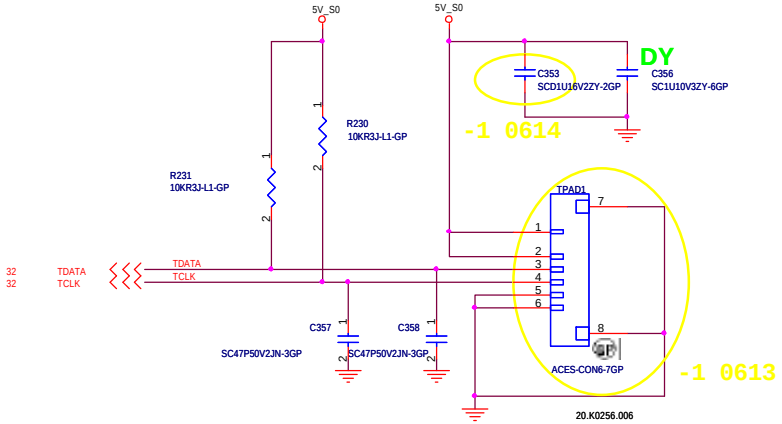
-1 0613





TouchPad Connector

< 6V/1.1A >



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	KB/TOUCH_PAD		
Size: A3	Document Number: Daytona		Rev: -1
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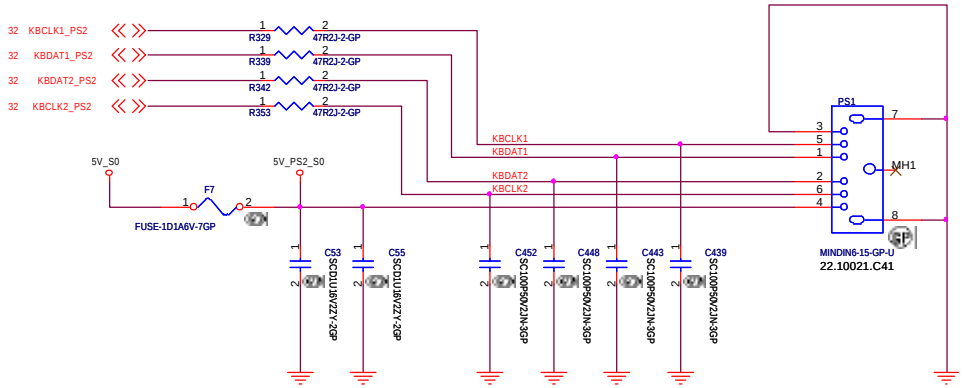
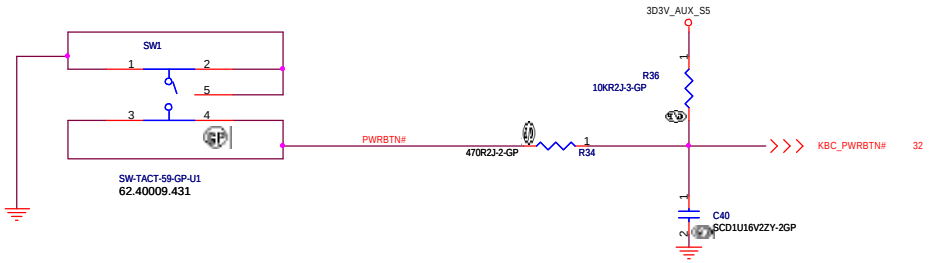
PS/2 CONN



POWER BUTTON



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Taipei Hsien 221, Taiwan, R.O.C.

Title	PS2/LAUCH CONN	
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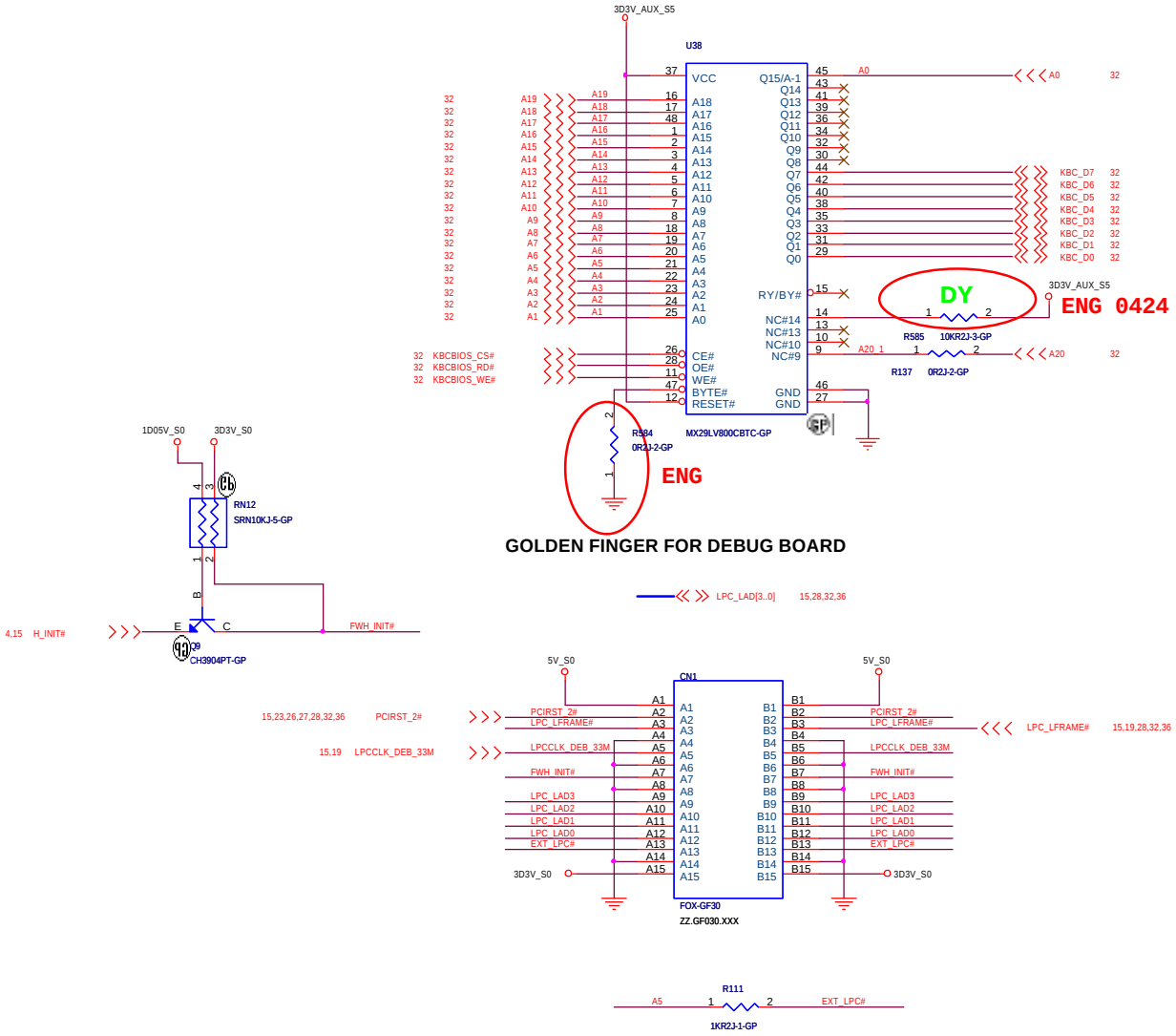

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03

Daytona

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LPC / Debug Port*

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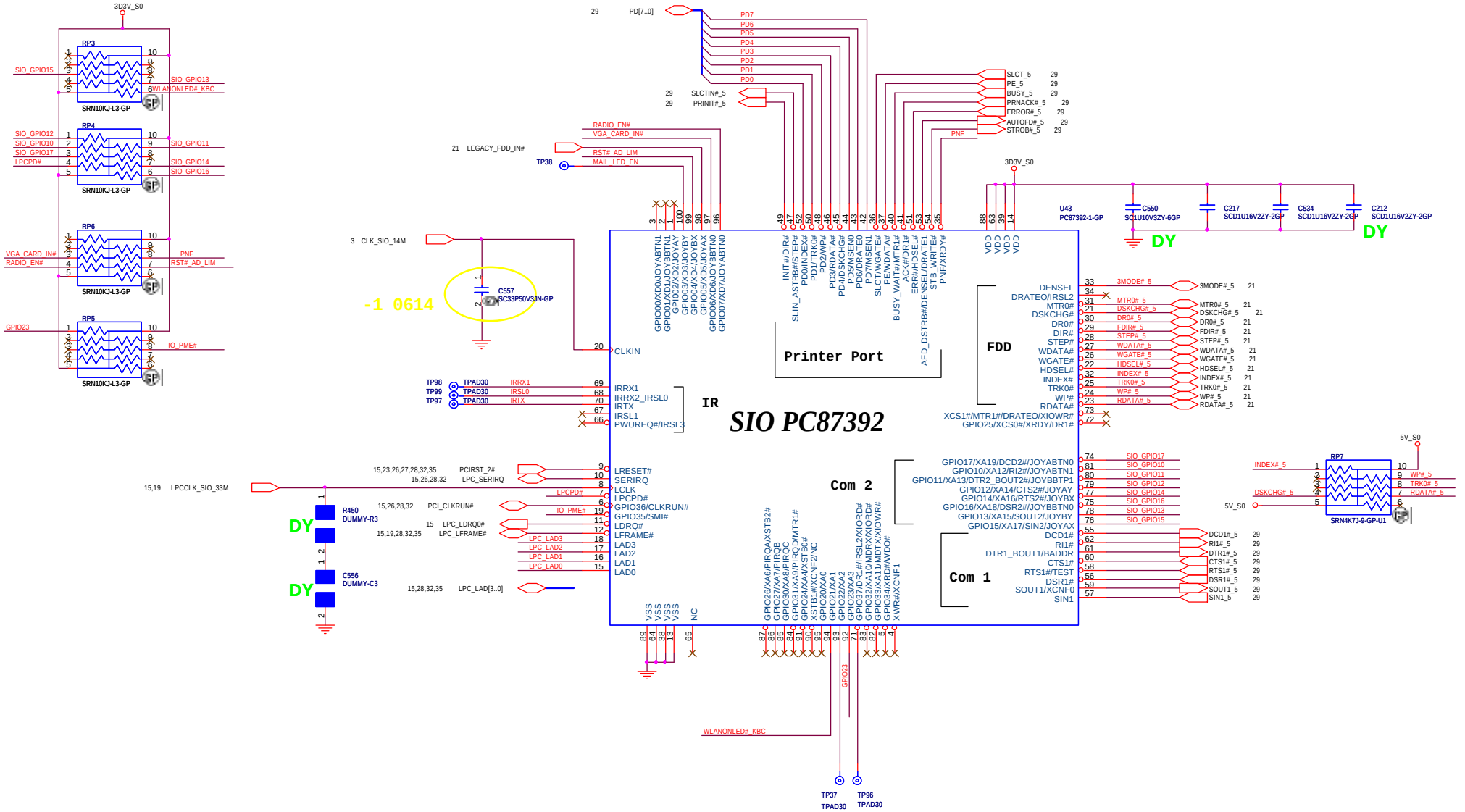
SIO PC87392
Printer Port
FDD
IR
Com 2
Com 1
-1 0614
DY
3D3V_S0
5V_S0
RP3
RP4
RP6
RP5
RP7
SRN10KJ-L3-GP
SRN4K7J-9-GP-U1
U43
PC87392-1-GP
C557
SC33P50V3JN-GP
C550
SC1U10V3ZY-6GP
C217
SCD1U16V2ZY-2GP
C534
SCD1U16V2ZY-2GP
C212
SCD1U16V2ZY-2GP
R450
DUMMY-R3
C556
DUMMY-C3
TP38
TP37
TP96
TP98
TP99
TP97
CLKIN
IRRX1
IRRX2_IRSL0
IRTX
IRSL1
PWUREQ#/IRSL3
LRESET#
SERIRQ
LCLK
LPCPD#
GPIO36/CLKRUN#
GPIO35/SMI#
LDRQ#
LFRAME#
LAD3
LAD2
LAD1
LAD0
PD[7..0]
SLCTIN#_5
PRINIT#_5
SLCT_5
PE_5
BUSY_5
PRNACK#_5
ERROR#_5
AUTOFD#_5
STROB#_5
PNF
RADIO_EN#
VGA_CARD_IN#
RST#_AD_LIM
MAIL_LED_EN
LEGACY_FDD_IN#
CLK_SIO_14M
DENSEL
DRATEO/IRSL2
MTR0#
DSKCHG#
DR0#
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK0#
WP#
RDATA#
XCS1#/MTR1#/DRATEO/XIOWR#
GPIO25/XCS0#/XRDY/DR1#
GPIO17/XA19/DCD2#/JOYABTN0
GPIO10/XA12/RI2#/JOYABTN1
GPIO11/XA13/DTR2_BOUT2#/JOYBBTP1
GPIO12/XA14/CTS2#/JOYAY
GPIO14/XA16/RTS2#/JOYBX
GPIO16/XA18/DSR2#/JOYBBTN0
GPIO13/XA15/SOUT2/JOYBY
GPIO15/XA17/SIN2/JOYAX
DCD1#
RI1#
DTR1_BOUT1/BADDR
CTS1#
RTS1#/TEST
DSR1#
SOUT1/XCNF0
SIN1
WLANONLED#_KBC
PCIRST_2#
LPC_SERIRQ
LPCCLK_SIO_33M
PCI_CLKRUN#
LPC_LDRQ0#
LPC_LFRAME#
LPC_LAD[3..0]
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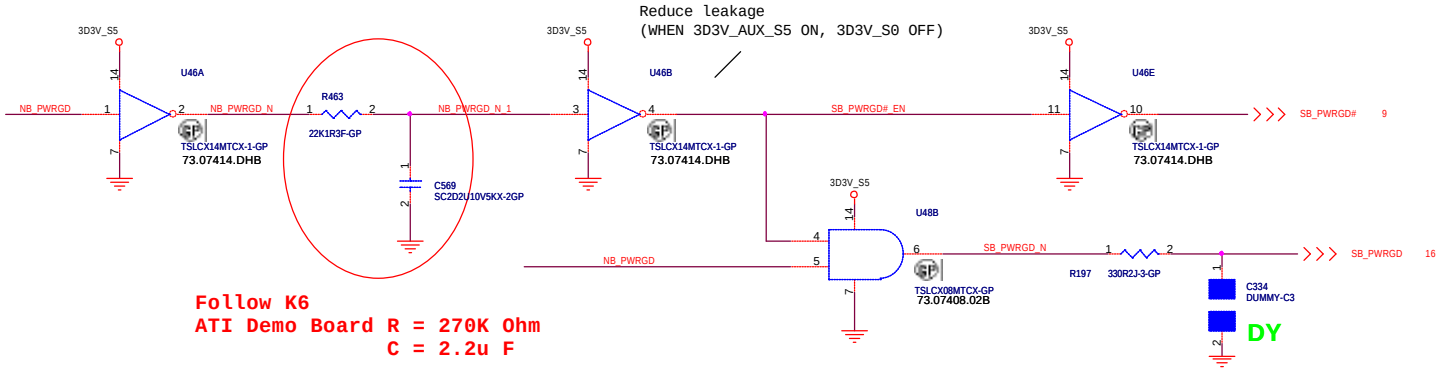
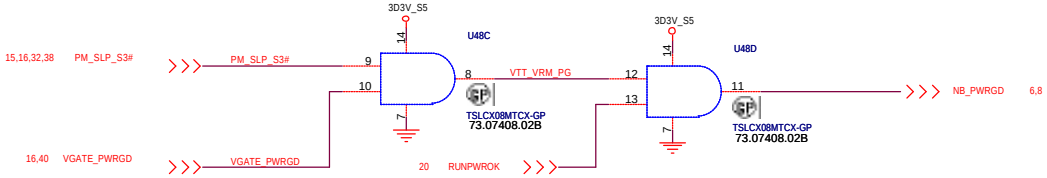
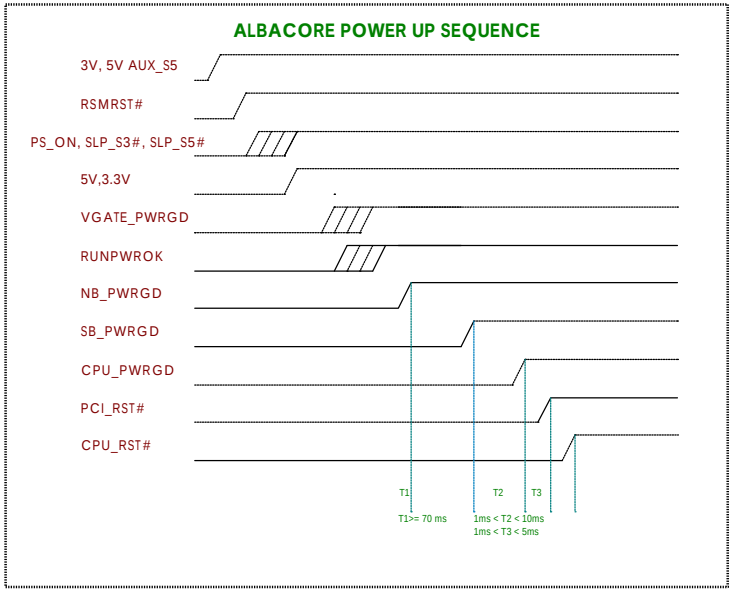
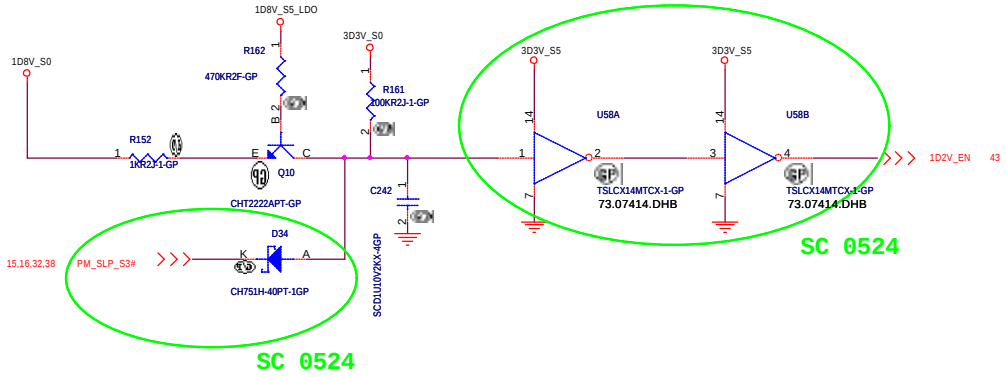


For RC415, SB_PWRGD need to be 65ms after NB_PWRGD





1D2V_S0 should not exceed 1D8V_S0 by more than 0.6V.



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Title: **POWER_ON_LOGIC**

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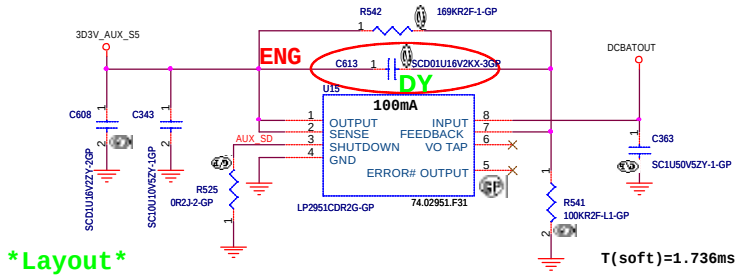
Date: Tuesday, June 13, 2006 Sheet 37 of 48

Aux Power

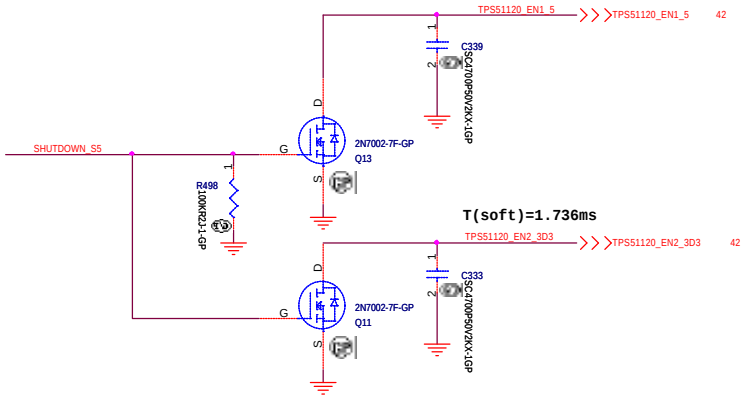


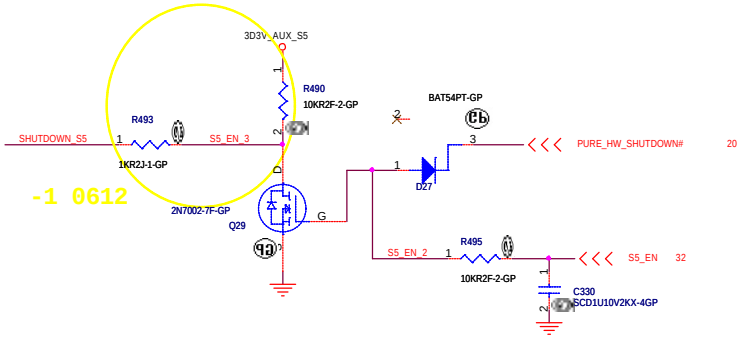
Vout = Vref*(1 + R1/R2)
Vref = 1.235V

T(soft)=1.736ms

Layout
15 mil

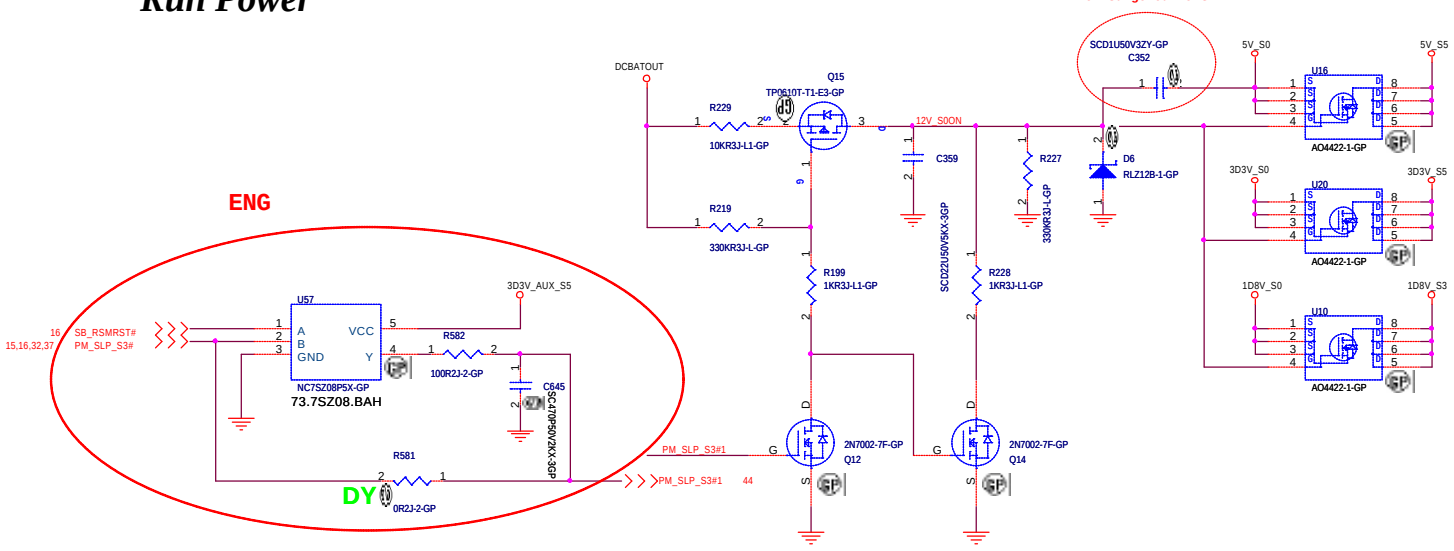
KBC KB3910 need 3D3V_AUX_S5





Run Power

For surge current



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Title: PWRPLANE&RESETLOGIC

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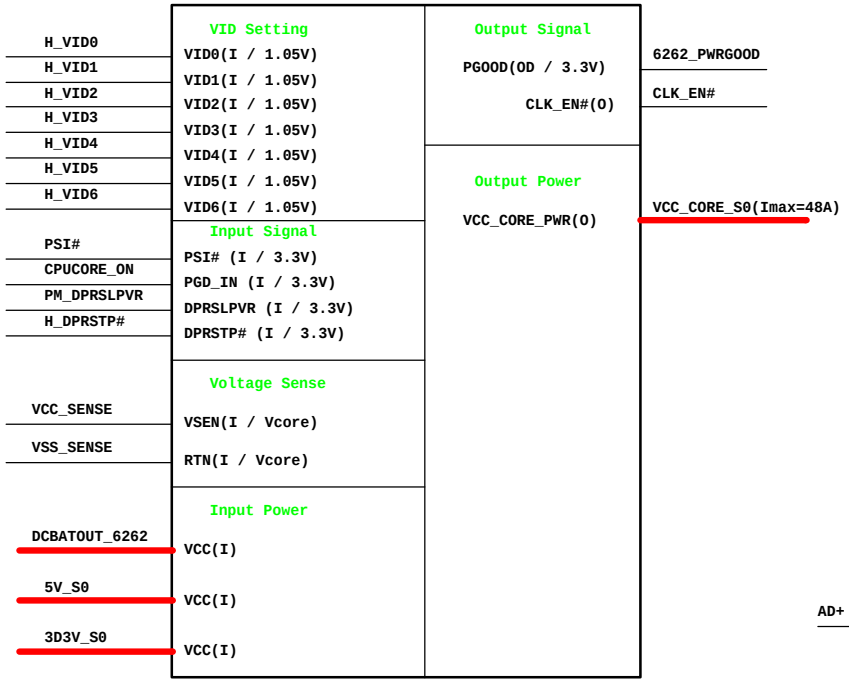
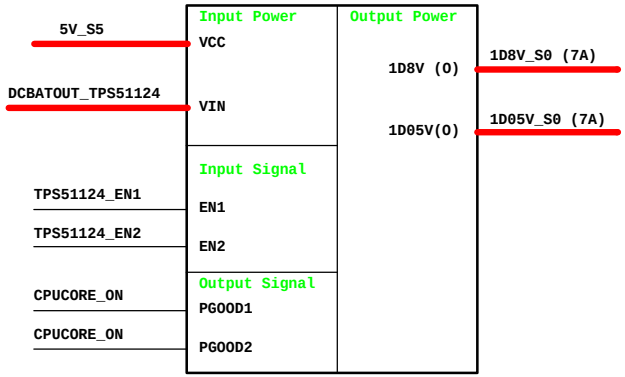
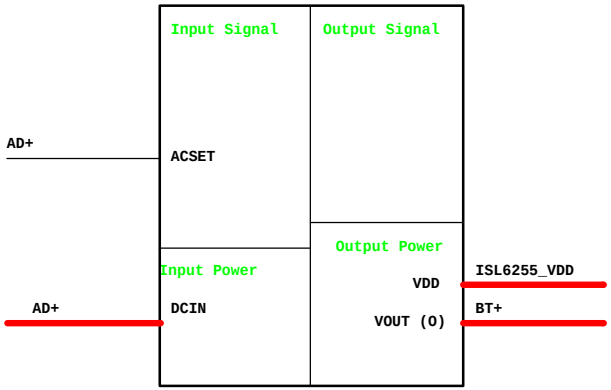
CPU_CORE
Intersil ISL6262



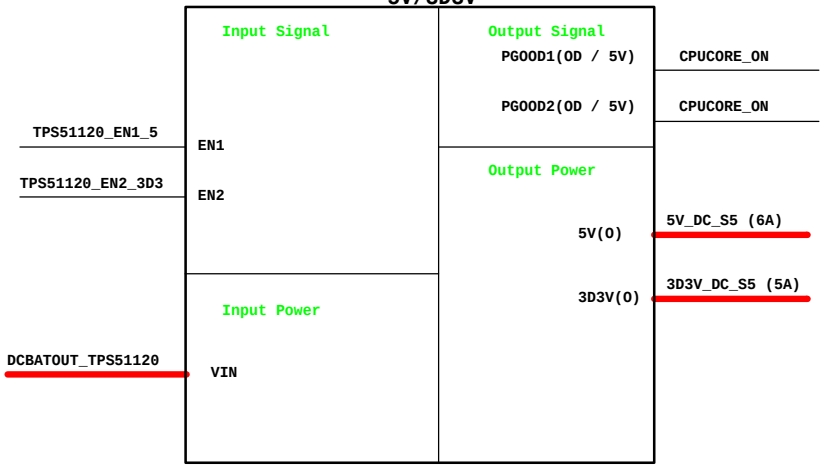
TPS51124
1D8V/1D05V



Charger MAX8725



TPS51120
5V/3D3V



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Title: POWER BLOCK DIAGRAM

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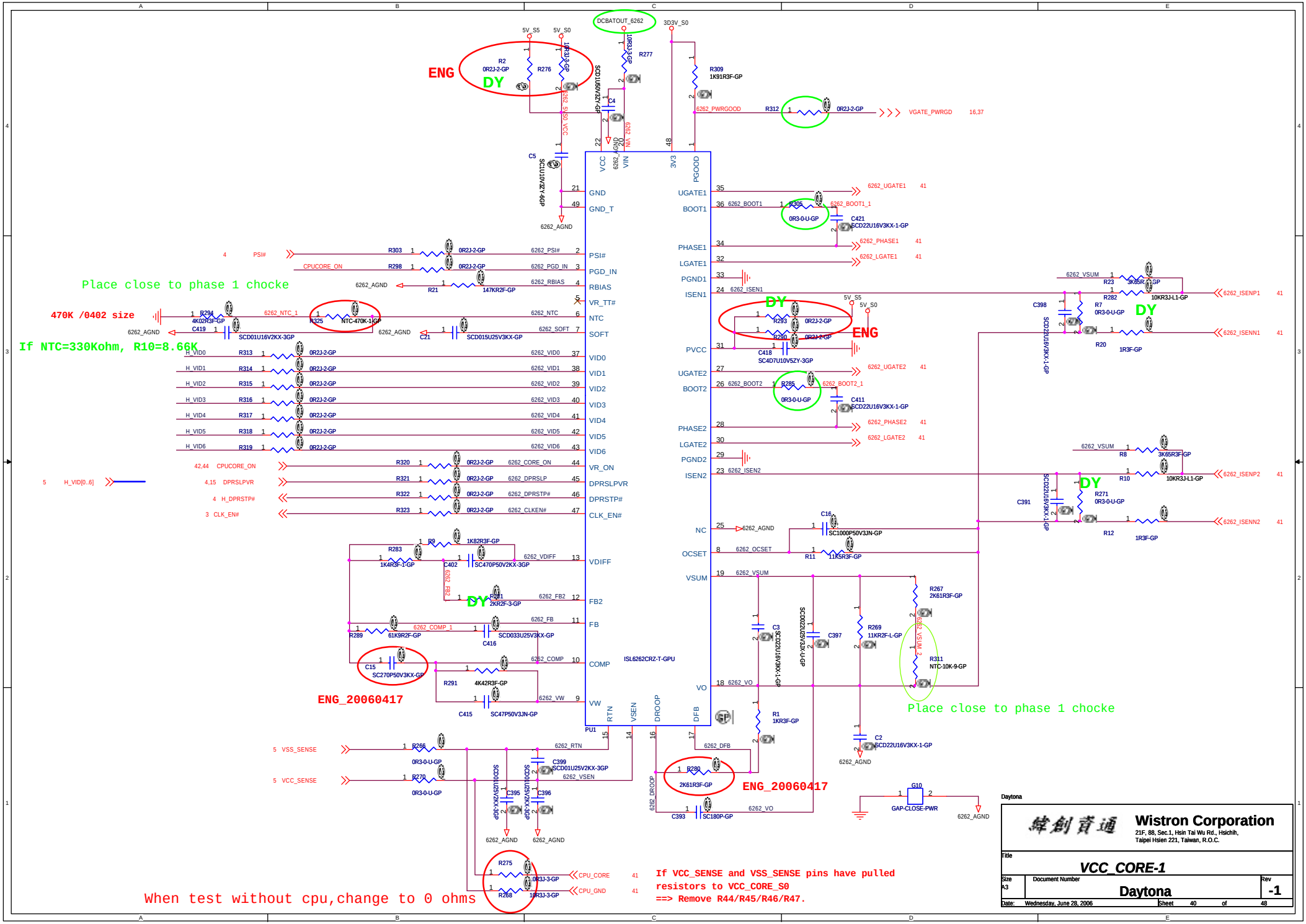
ENG
DY
DCBATOUT_6262
3D3V_S0
5V_S5
5V_S0
R2 0R2J-2-GP
R276
R277
R309 1K91R3F-GP
6262_PWRGOOD
R312 0R2J-2-GP
VGATE_PWRGD 16,37
C4
C5
6262_AGND
VCC
VIN
3V3
PGOOD
GND
GND_T
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC
OCSET
VSUM
VO
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
DPRSTP#
CLK_EN#
VDIFF
FB2
FB
COMP
VW
RTN
VSEN
DROOP
DFB
PU1
ISL6262CRZ-T-GPU
Place close to phase 1 chocke
470K /0402 size
If NTC=330Kohm, R10=8.66K
R294 4K02R3F-GP
R325 NTC-470K-1-GP
C419
C21
R21 147KR2F-GP
R303
R298
CPUCORE_ON
PSI#
H_VID[0..6]
DPRSLPVR
H_DPRSTP#
CLK_EN#
CPUCORE_ON
R313
R314
R315
R316
R317
R318
R319
R320
R321
R322
R323
R283 1K4R3F-1-GP
R9 1K82R3F-GP
C402 SC470P50V2KX-3GP
R281 2KR2F-3-GP
R289 61K9R2F-GP
C416 SCD033U25V3KX-GP
C15 SC270P50V3KX-GP
R291 4K42R3F-GP
C415 SC47P50V3JN-GP
ENG_20060417
R205 0R3-0-U-GP
C421 SCD22U16V3KX-1-GP
R293
R280
C418 SC4D7U10V5ZY-3GP
R285 0R3-0-U-GP
C411 SCD22U16V3KX-1-GP
C16 SC1000P50V3JN-GP
R11 11K5R3F-GP
R267 2K61R3F-GP
C3 SCD22U25V3KX-U-GP
C397
R269 11KR2F-L-GP
R311 NTC-10K-9-GP
R1 1K5R3F-GP
C2 SCD22U16V3KX-1-GP
R280 2K61R3F-GP
C393 SC180P-GP
G10 GAP-CLOSE-PWR
R23 3K65R3F-GP
R282 10KR3J-L1-GP
R7 0R3-0-U-GP
R20 1R3F-GP
C398 SCD22U16V3KX-1-GP
R8 3K65R3F-GP
R10 10KR3J-L1-GP
R271 0R3-0-U-GP
R12 1R3F-GP
C391 SCD22U16V3KX-1-GP
6262_VSUM
6262_ISENP1
6262_ISENN1
6262_ISENP2
6262_ISENN2
6262_UGATE1
6262_BOOT1
6262_PHASE1
6262_LGATE1
6262_UGATE2
6262_BOOT2
6262_PHASE2
6262_LGATE2
6262_ISEN1
6262_ISEN2
6262_OCSET
6262_VO
6262_DFB
6262_RTN
6262_VSEN
6262_VDIFF
6262_FB2
6262_FB
6262_COMP_1
6262_COMP
6262_VW
6262_PSI#
6262_PGD_IN
6262_RBIAS
6262_NTC_1
6262_NTC
6262_SOFT
6262_VID0
6262_VID1
6262_VID2
6262_VID3
6262_VID4
6262_VID5
6262_VID6
6262_CORE_ON
6262_DPRSLP
6262_DPRSTP#
6262_CLKEN#
Place close to phase 1 chocke
ENG_20060417
5 VSS_SENSE
5 VCC_SENSE
R266 0R3-0-U-GP
R270 0R3-0-U-GP
C399 SCD01U25V2KX-3GP
C395 SCD01U25V2KX-3GP
C396 SCD01U25V2KX-3GP
R275 10R3J-3-GP
R268 10R3J-3-GP
CPU_CORE 41
CPU_GND 41
When test without cpu,change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
==> Remove R44/R45/R46/R47.
Daytona
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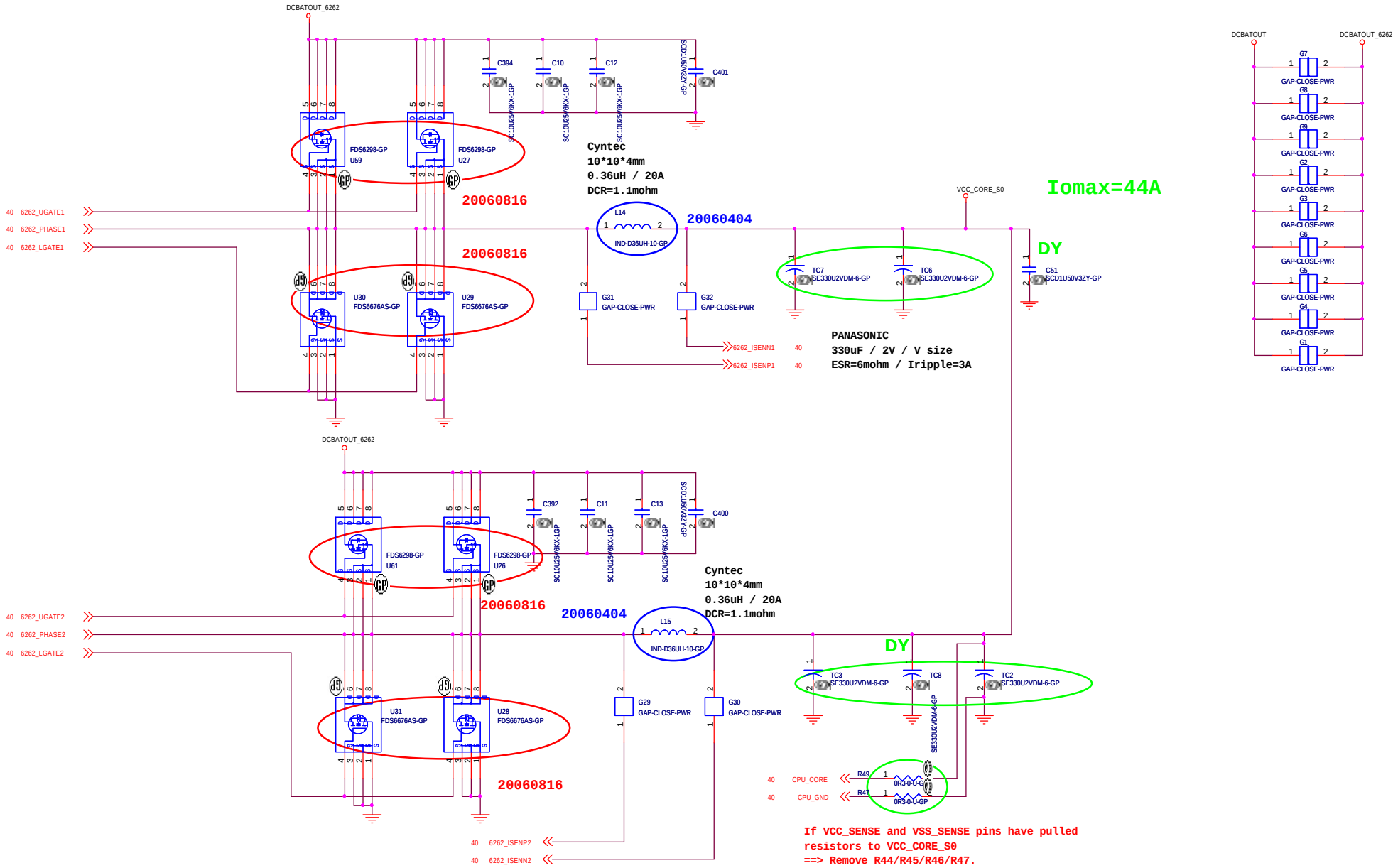
Title
VCC_CORE-1
Size A3
Document Number
Daytona
Rev -1
Date: Wednesday, June 28, 2006
Sheet 40 of 48



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Title: VCC_CORE_2

Size: A3 | Document Number: Daytona | Rev: -1

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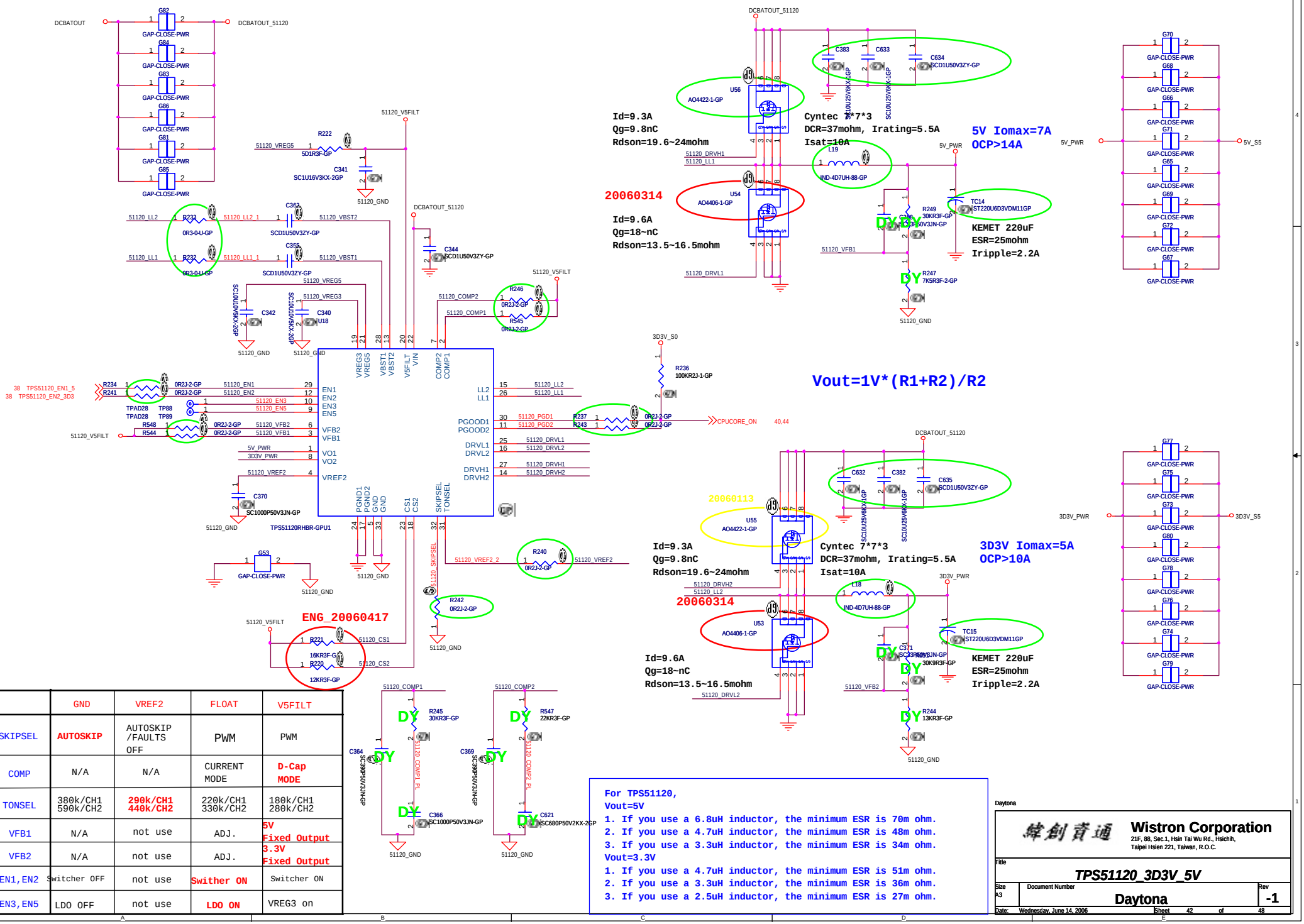

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	**290k/CH1 440k/CH2**	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swither ON**	Switcher ON
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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Title: TPS51120_3D3V_5V

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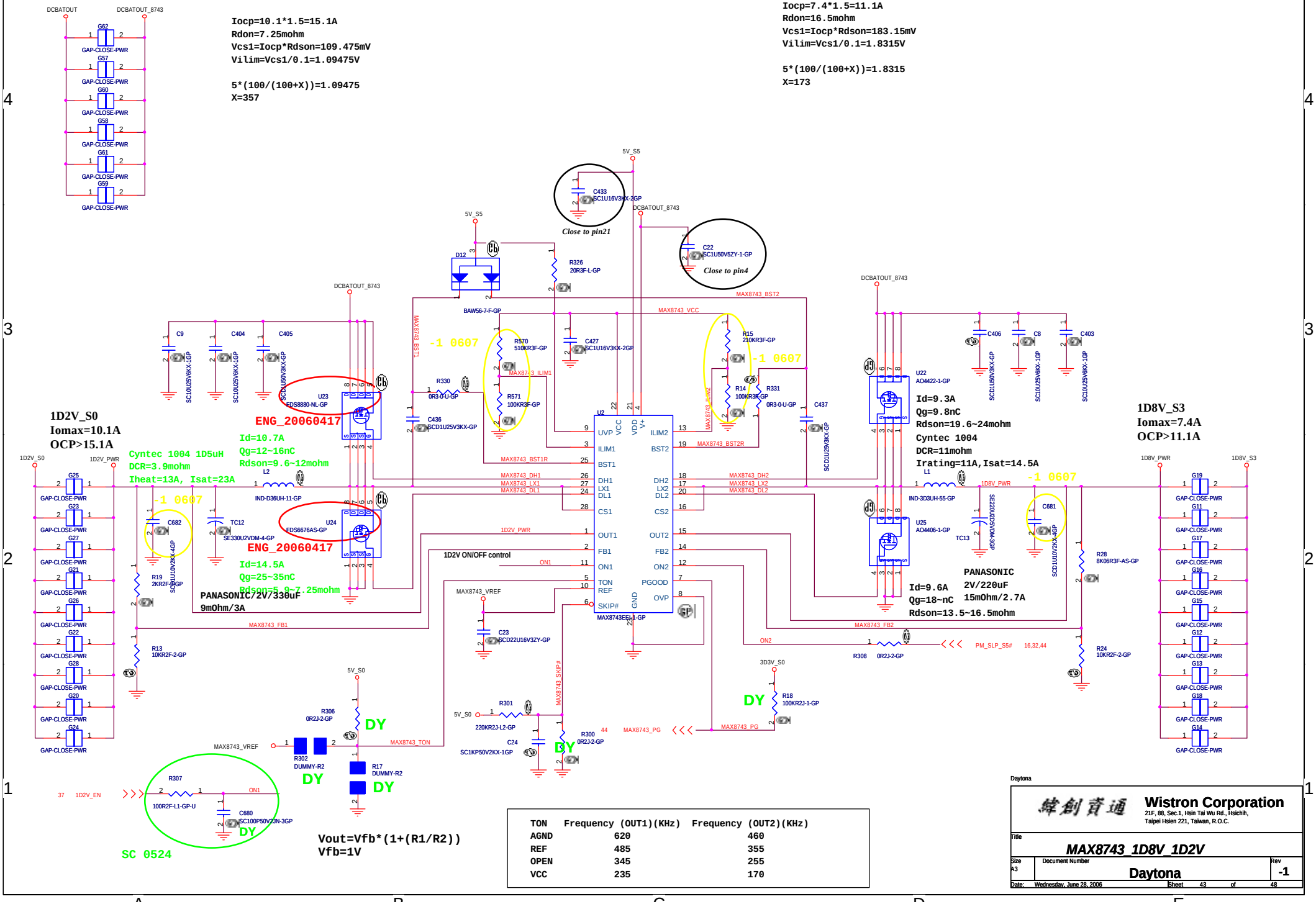
Date: Wednesday, June 14, 2006 | Sheet 42 of 48


Iocp=10.1*1.5=15.1A
Rdon=7.25mohm
Vcs1=Iocp*Rdson=109.475mV
Vilim=Vcs1/0.1=1.09475V
5*(100/(100+X))=1.09475
X=357
Iocp=7.4*1.5=11.1A
Rdon=16.5mohm
Vcs1=Iocp*Rdson=183.15mV
Vilim=Vcs1/0.1=1.8315V
5*(100/(100+X))=1.8315
X=173
1D2V_S0
Iomax=10.1A
OCP>15.1A
Cyntec 1004 1D5uH
DCR=3.9mohm
Iheat=13A, Isat=23A
ENG_20060417
Id=10.7A
Qg=12~16nC
Rdson=9.6~12mohm
ENG_20060417
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC/2V/330uF
9mOhm/3A
1D2V ON/OFF control
Close to pin21
Close to pin4
-1 0607
Id=9.3A
Qg=9.8nC
Rdson=19.6~24mohm
Cyntec 1004
DCR=11mohm
Irating=11A,Isat=14.5A
1D8V_S3
Iomax=7.4A
OCP>11.1A
Id=9.6A
Qg=18~nC
Rdson=13.5~16.5mohm
PANASONIC
2V/220uF
15mOhm/2.7A
DY
SC 0524
Vout=Vfb*(1+(R1/R2))
Vfb=1V
TON Frequency (OUT1)(KHz) Frequency (OUT2)(KHz)
AGND 620 460
REF 485 355
OPEN 345 255
VCC 235 170
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Daytona
MAX8743_1D8V_1D2V
Size A3
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Daytona
Rev -1
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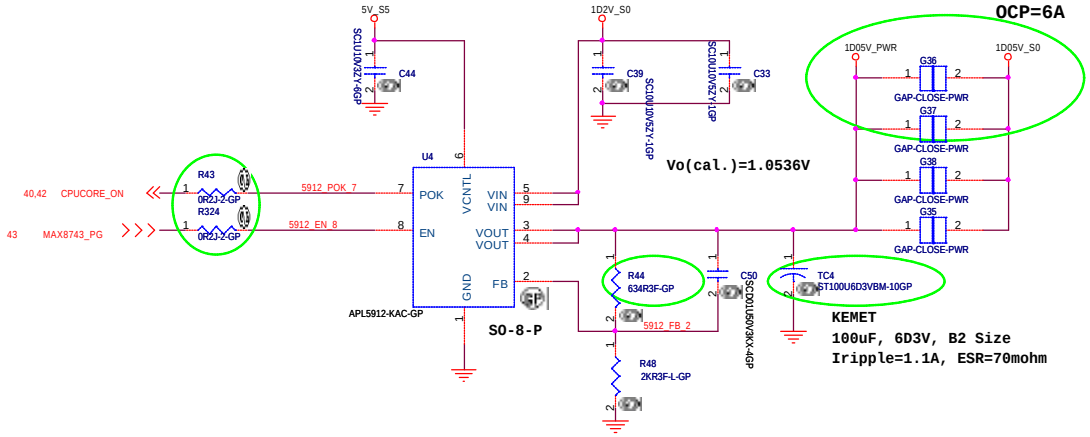
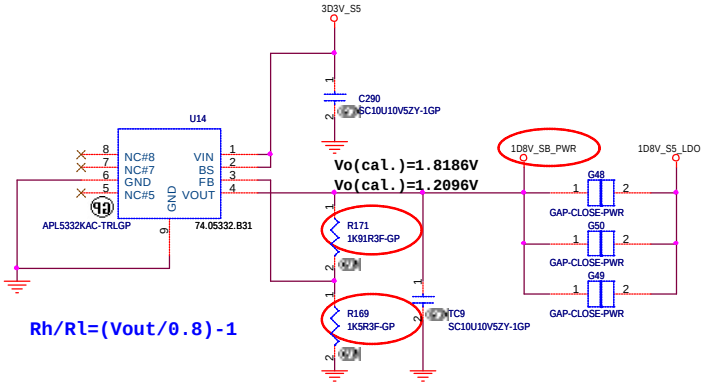
1D05V_S0
Iomax=3A



Vo=0.8*(1+(R1/R2))

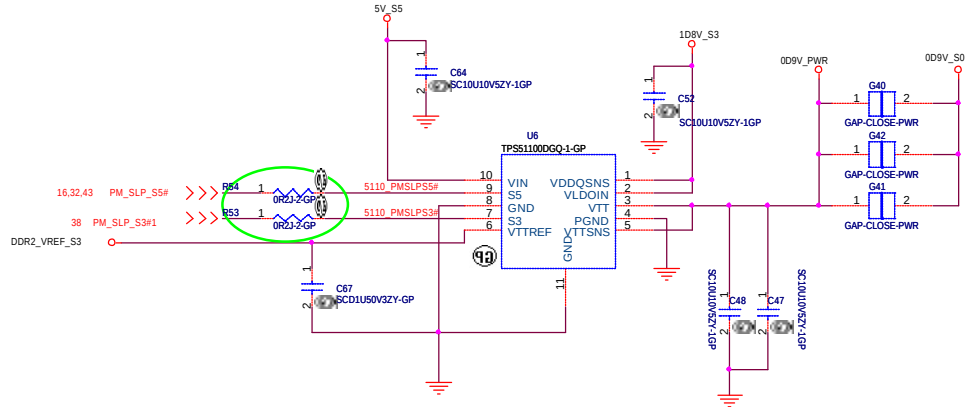
1D8V or 1D2V
Iomax=0.2A



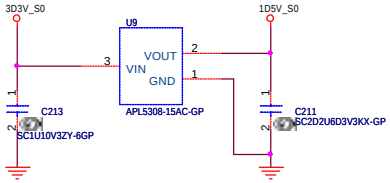
Rh/Rl=(Vout/0.8)-1

SB460=>1D8V (Rh=1K91ohm ,Rl=1K5ohm)
SB600=>1D2V (Rh=768ohm ,Rl=1K5ohm)

0D9V
Iomax=1.5A



1D5V_S0
Iomax=120mA



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Title: 1D5V/0D9V/1D05V/1D8V		
Size: A3	Document Number: Daytona	Rev: -1
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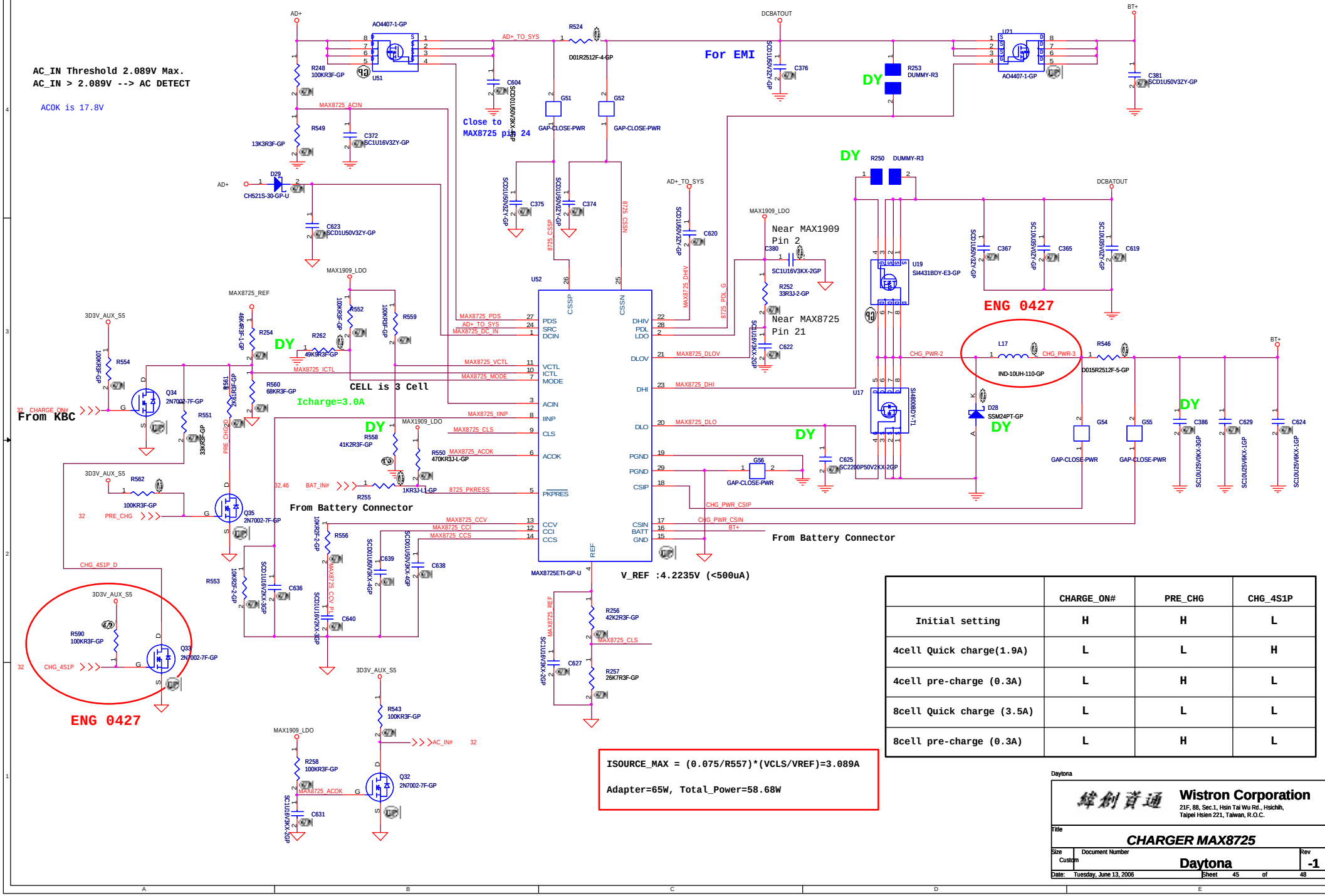

	CHARGE_ON#	PRE_CHG	CHG_4S1P
Initial setting	H	H	L
4cell Quick charge(1.9A)	L	L	H
4cell pre-charge (0.3A)	L	H	L
8cell Quick charge (3.5A)	L	L	L
8cell pre-charge (0.3A)	L	H	L

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Title: CHARGER MAX8725

Size: Custom | Document Number: Daytona | Rev: -1

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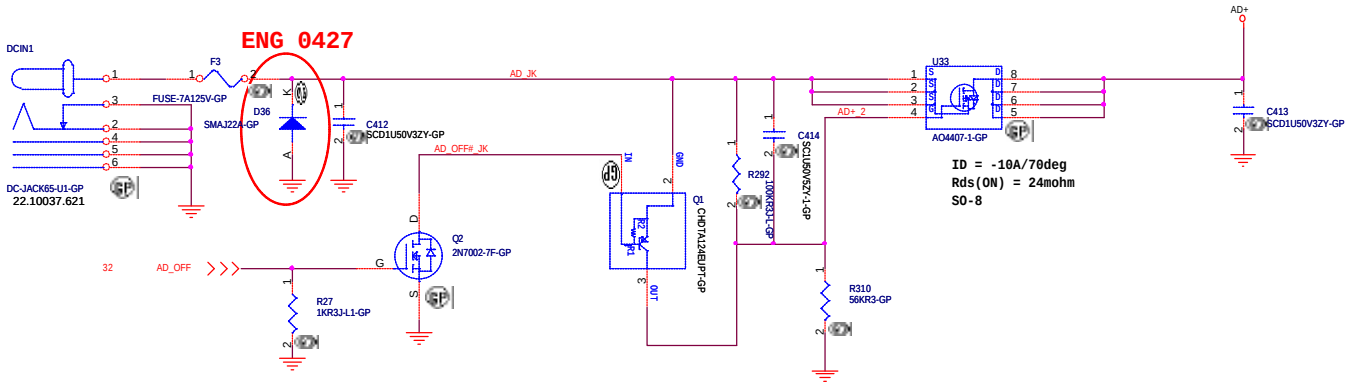
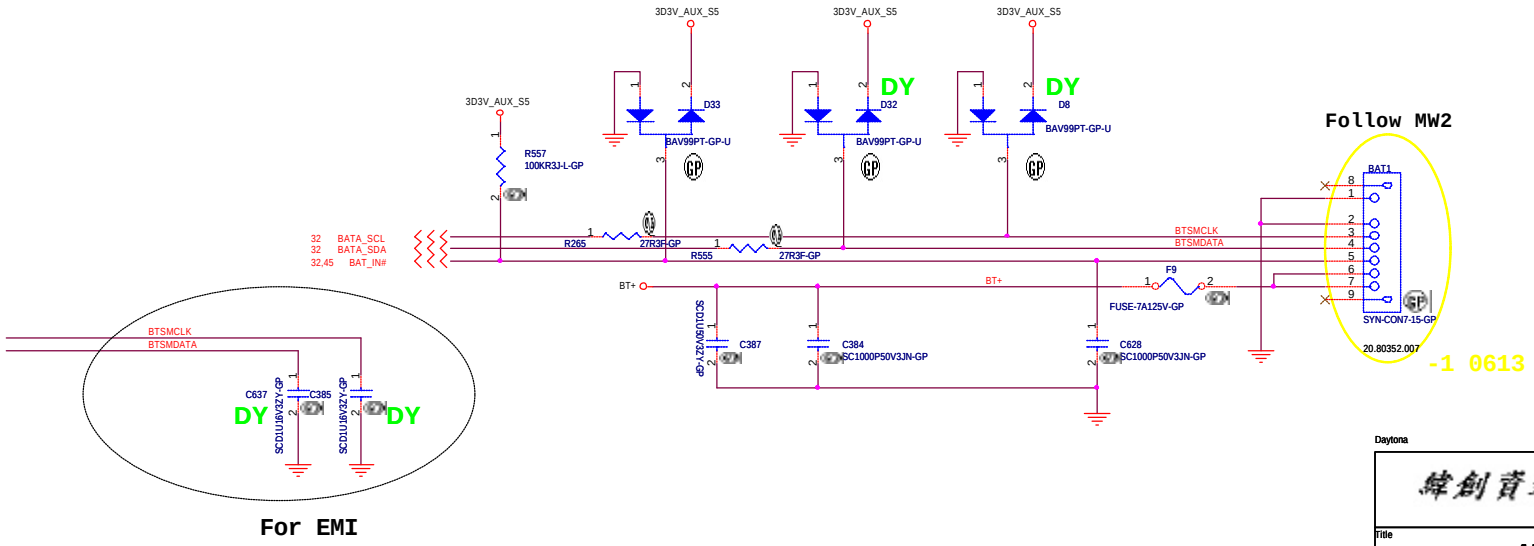
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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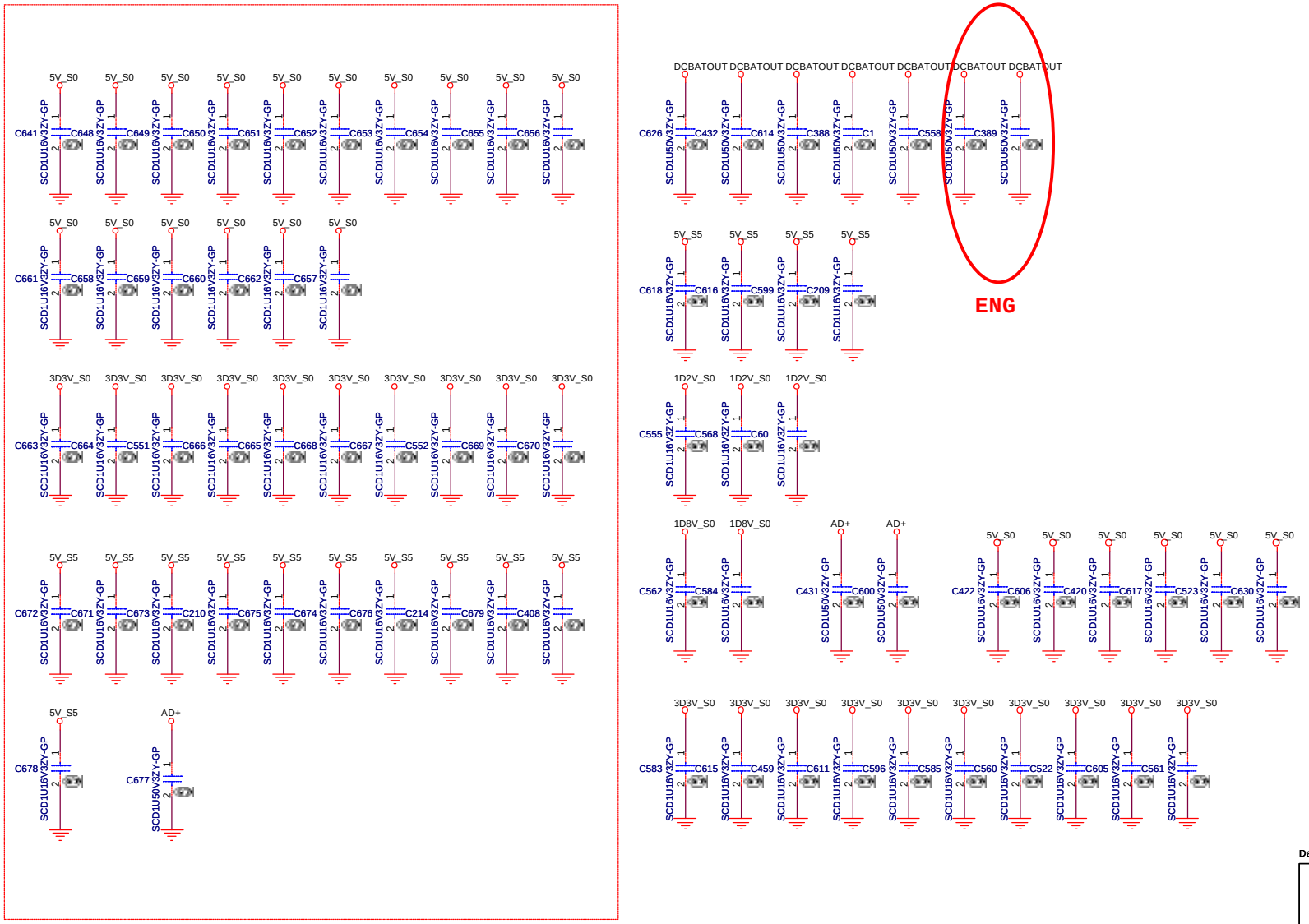
Title: *AD/BAT CONN*		
Size: A3	Document Number: Daytona	Rev: -1
Date: Wednesday, June 14, 2006	Sheet 46 of 48	



Daytona

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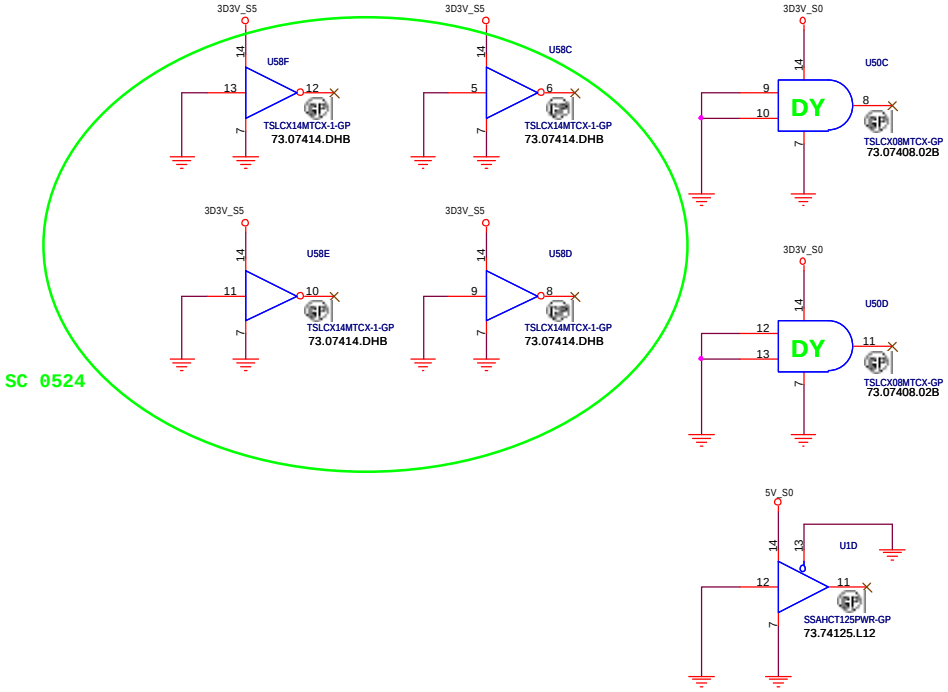
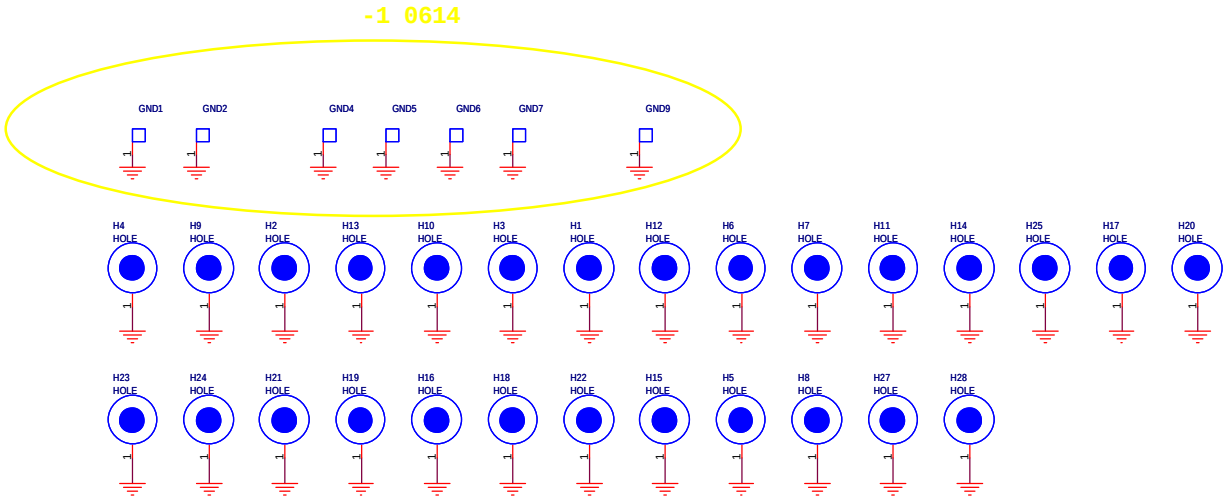
Title	***EMI***	
Size: Custom	Document Number: **Daytona**	Rev: **-1**
Date: Monday, June 12, 2006	Sheet 47 of 48	





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Title: ***MISC***

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