MODEL:	REV:	CHANGE LIST:
ZL5 MotherBoard	1A	FIRST RELEASE
	2A	01. Page2 : Unstaff R202 for correct clock setting 02. Page3 : Delete JP2, Unstaff C561 and C559 ~ C562, C567 change P/N to CH6101M9A07 due to the height limitaion 03. Page5 : Change DDR MD terminator resistor array to 56ohm 4P2R type 04. Page9 : Change R20 to 6.2K, Unstaff C13 05. Page10 : Modify the CRT circuit due to the bad signal quality of CM2009 (Delete U1, Add D25, D28 ~ D32, Q35, Q36, R405, R404, R406, U31, U32) 06. Page11 : RN5, RN7, RN8, RN11, RN20, RN21 change P/N to CJ282084N01 07. Page12 : Modify the power good circuit (Delete D15, Add R402, R403) 08. Page16 : Modify the lan led circuit to fit to the right led color definition (R350, R353 change to pull high, Add D26, D27, CN3 change footprint) 09. Page17 : CN7, CN8 change footprint 10. Page19 : HOLE25 change to TOP layer 11. Page20 : Cancel the HOLD# ciruit (Unstaff R95, R111, D5, D7, Q17, Staff Q15, R99) 12. Page21 : SW2, SW3 change P/N to DHPPS11BD0 13. Page22 : Add PR123, PD16, PC149; PD13 change P/N to BC05FA20Z01; PU12 change P/N to AL001999W16 14. Page23 : PR63 change to 11K/F; PD15 change P/N to BC10QS04C01; Staff PC77 1000P 15. Page25 : PL8, PL9 change size to RC0805; PD8, PD9 change P/N to BC10QS04C01 16. Page26 : Unstaff PQ4; PR101, PR105 change P/N to CS31003B919; PU9 change P/N to AJ017720W06 17. Delete JP1, JP2 ~ JP6 18. U20 change P/N to AJ007600T25 19. L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L18, L24, L26, L27, L40, L43, L47, L48, L49, L50 change P/N to CX0QNT03004 20. PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35, Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q26, Q27, Q34 change P/N to BAM70020074
	3A	01. Page2 : Staff R176 33ohm for 302ELV clock 02. Page4 : Staff C131, C175, C188, C189 03. Page9 : Staff R295(0ohm), R294 change P/N to CS00002JB03, Unstaff Y4, C31, C554 for 302ELV clock; Add C710 ~ C713, R407 ~ R410 for EMI reserved. 04. Page10 : D17 change p/n to BC05FA20Z01 to enlarge the current limit; L1 ~ L3 change p/n to CX808600101 for EMI 05. Page12 : C633, C634 change P/N to CH01806JB07 to adjust RTC accuracy; Add JP1 for RTC reset 06. Page15 : Add C709 07. Page17 : Unstaff CN8, CN10; Add C700 ~ C708 for EMI 08. Page19 : Delete HOLE18; Staff PAD4 for modem cable
	3B	01. Page17 : L36, R274, R279 change p/n to CX8HS121001; Staff R270, R273 100pF 02. Page18 : L54, L55 change p/n to CX8HS121001; Unstaff R260, R261, R265, R271, R278 03. Page19 : Staff PAD9(FDMK1004010) for EMI 04. Page22 : Unstaff PR112 for thermal shutdown working properly 05. Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q18, Q26, Q27, Q34, Q35, Q36, PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35 change p/n to BAN70020Z13

MODEL : ZL5 MB

PAGE	FROM	TO
1	3A	3B
2	3A	3B
3	3A	3B
4	3A	3B
5	3A	3B
6	3A	3B
7	3A	3B
8	3A	3B
9	3A	3B
10	3A	3B
11	3A	3B
12	3A	3B
13	3A	3B
14	3A	3B
15	3A	3B
16	3A	3B
17	3A	3B
18	3A	3B
19	3A	3B
20	3A	3B
21	3A	3B
22	3A	3B
23	3A	3B
24	3A	3B
25	3A	3B
26	3A	3B

Quanta Computer Inc.	PROJECT : ZL5	APPROVE BY: SAINT LIN	DRAWING BY:DILBERT YU	REV 3B
	MB ASSY'S P/N : 31ZL5MB0009	PROJECT LEADER: SAINT LIN	DOCUMENT NO:	DATE :2005/3/9

COVER SHEET 1 OF 1

ZL5
Block Diagram

CLK-GEN
ICS 952801
Page 2

HOST 200MHz
ZCLK 133MHz
AGP 66MHz
PCI 33MHz
USB 48MHz
REF 14.318MHz

3V/5V
Page 22

3V_ALWAYS
5VPCU
3V_S5
1.8V_S5
3VSUS
5VSUS
+3V
+5V
15V

2.5V/1.25V
Page 23

2.5VSUS
1.25VREF
+2.5V
DDR_VTT

1.2V/1.5V 1.8V
Page 24

+1.2V_HT
+1.5V
+1.8V

CPU CORE
Page 25

VCC_CORE

BATTERY CHARGER
Page 26

DDR SO-DIMM
Page 5

DDR 333

CPU
AMD Athlon64
SMT uPGA754
Page 3,4

Thermal
Thermal sensor & Fan

HyperTransport
16x16
1600MT/s

NB
SIS M760GX
(698 PIN BGA)
Page 6,7,8

RGB

CRT
1x D-SUB 15-Pin
Page 10

INTA#

DVO

LVDS Transmitter
SIS302ELV
Page 9

LVDS

LCD
15" XGA/WXGA
Page 10

MuTIOL(1GB/s)

SB
SIS 963L
(371 PIN BGA)
Page 11,12,13

HDD
Primary Master
Page 19

ATA 66/100

ODD
Secondary Master
Page 19

ATA 66/100

USB
3x connector
Page 15

USB 2.0

MINI USB
(BLUETOOTH)
Page 15

REQ0#, GNT0#
INTB#, INTC# IDSEL : AD22

PCI 2.2 133MB/s (33MHZ)

Mini PCI
WLAN 802.11A/G
Page 15

Antenna

REQ1#, GNT1#
INTD# IDSEL : AD17

CardBus
TI PCI1410
Page 14

PC Card
1x type-I/II

MII

LAN PHY
RTL8201CP
Page 16

Transformer
Page 16

RJ-45
Page 16

AC'97 2.1

MDC1.5
56K MODEM
Page 17

RJ-11
Page 16

AC97 Codec
ALC203
Page 17

MIC-In Jack

Line-In Jack

AMP
MAX9755
Page 18

HP-Out Jack

Int. Speaker

LPC

Int. Keyboard
87-Key
Page 21

Touch Pad
6-Button
Page 21

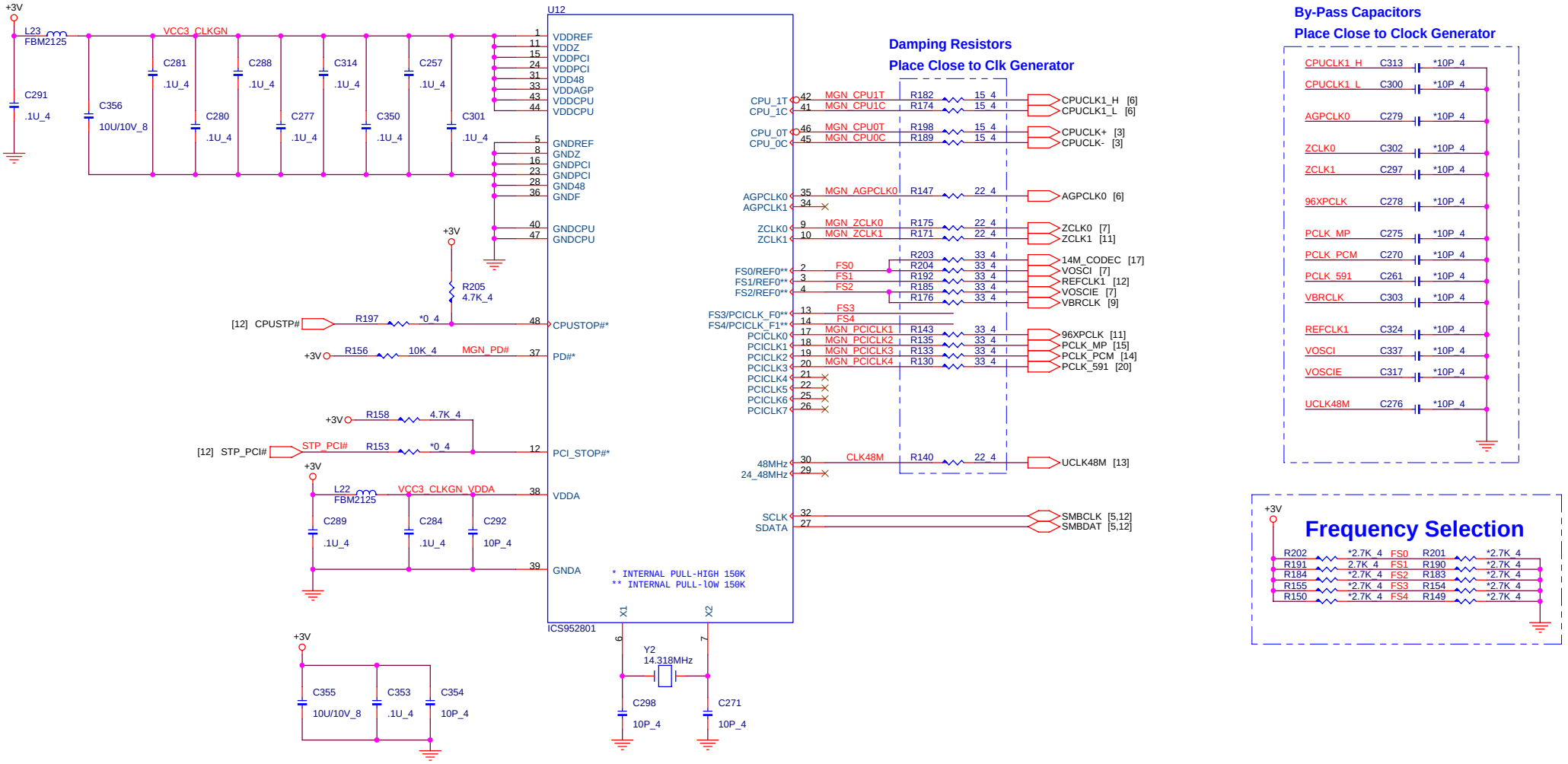
EC
NS PC97551
Page 20

BIOS
Page 20

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	3B

Date: Thursday, March 10, 2005 Sheet 1 of 26



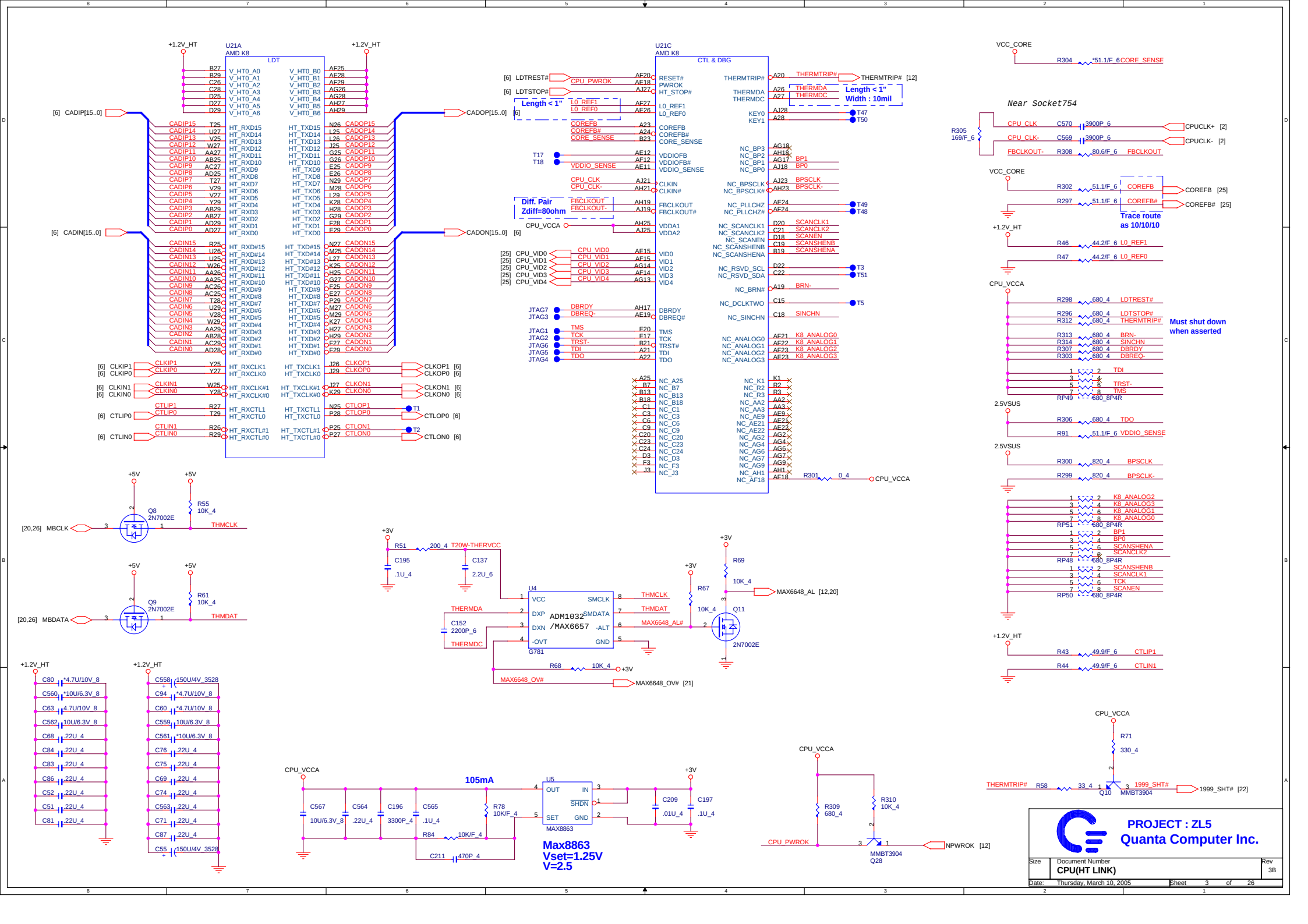
CLK Table for SiS M760 (Not For ICS ICS-952801)

SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

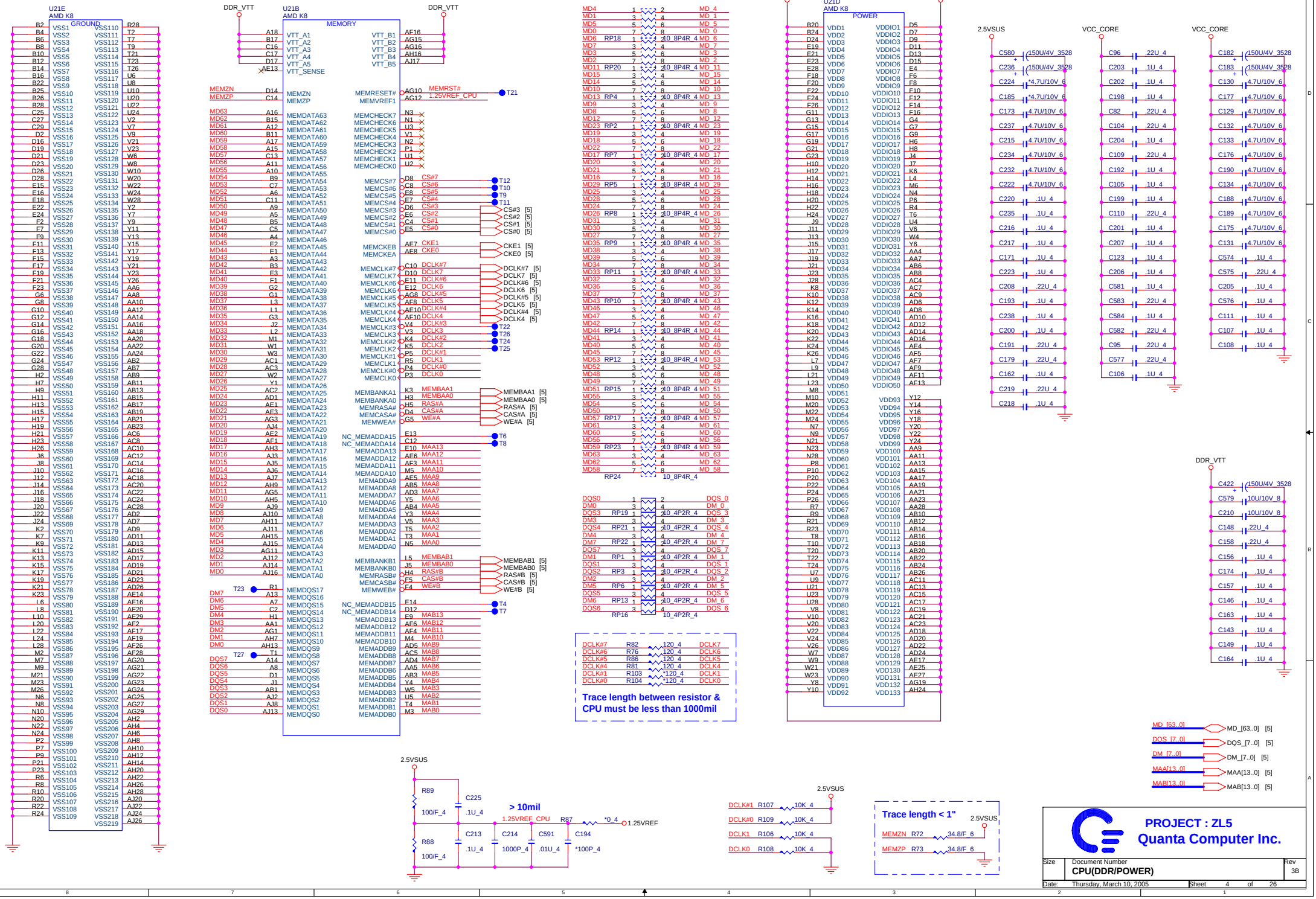
SiS 755/M760 CLOCK								
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
1	0	0	0	0	180	135	67.5	33.75
1	0	0	0	1	185	132.14	66.07	33.04
1	0	0	1	0	190	135.71	67.08	33.93
1	0	0	1	1	195	130	65	32.5
1	0	1	0	0	205	136.66	68.33	34.17
1	0	1	0	1	210	140	70	35
1	0	1	1	0	215	129	64.5	32.25
1	0	1	1	1	220	132	66	33
1	1	0	0	0	66.66	66.66	66.66	33.33
1	1	0	0	1	66.66	100	66.66	33.33
1	1	0	1	0	100	100	66.66	33.33
1	1	0	1	1	100	133.33	66.66	33.33
1	1	1	0	0	133	100	66.66	33.33
1	1	1	0	1	133	133.33	66.66	33.33
1	1	1	1	0	166	100	66.66	33.33
1	1	1	1	1	166	133.33	66.66	33.33

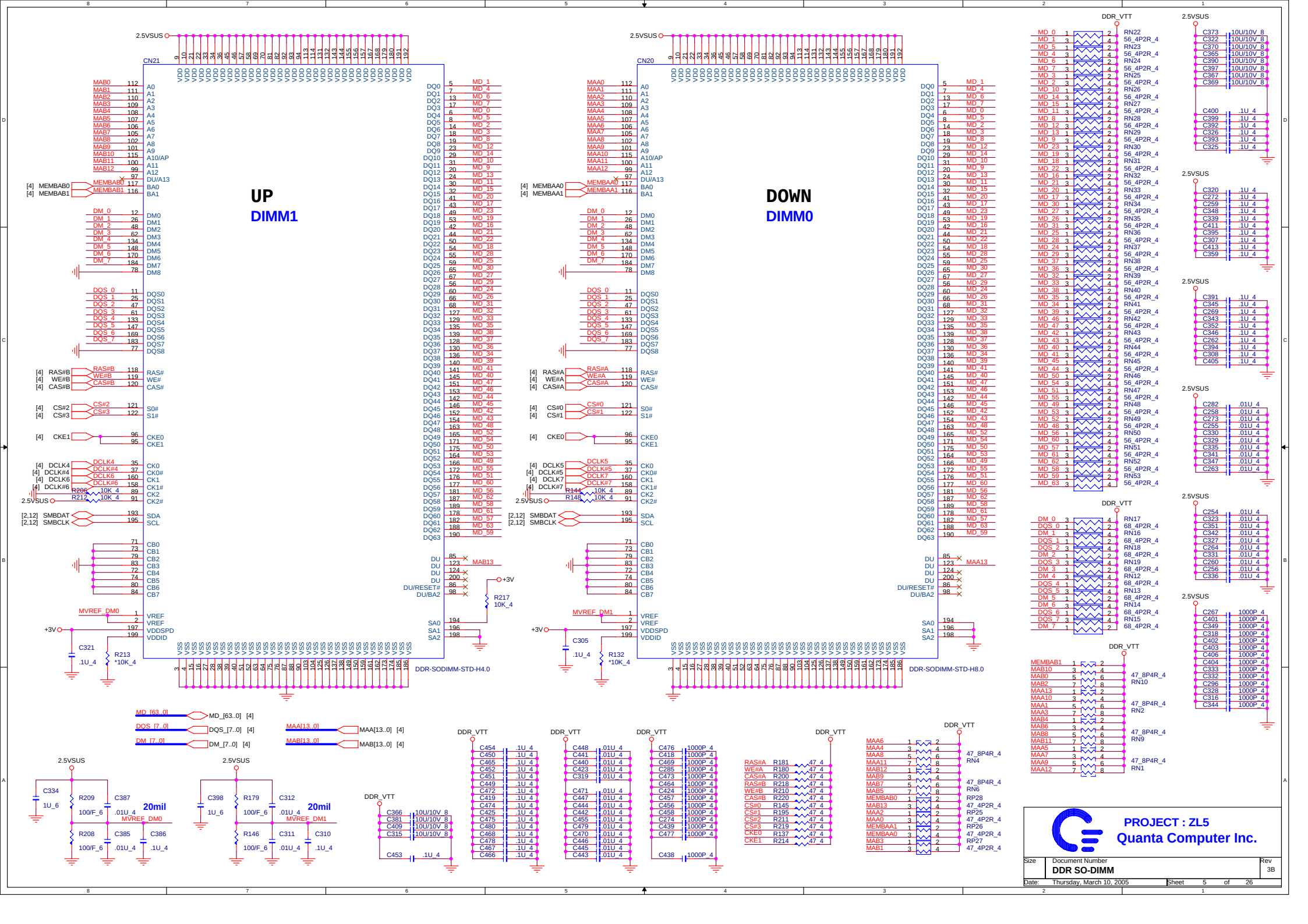
PROJECT : ZL5
Quanta Computer Inc.

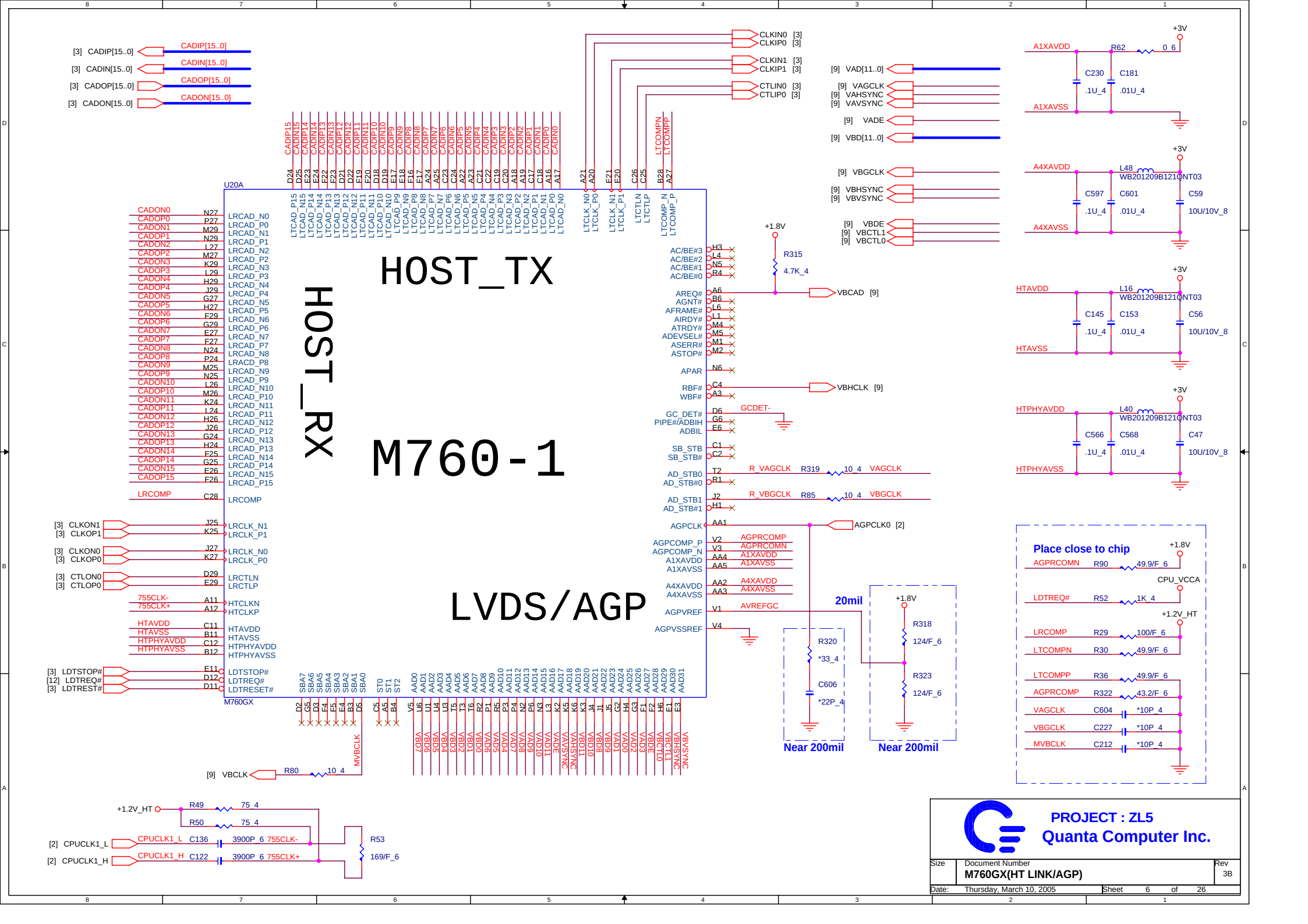
Size	Document Number	Rev
	CLOCK GENERATOR	3B
Date: Thursday, March 10, 2005	Sheet 2 of 26	

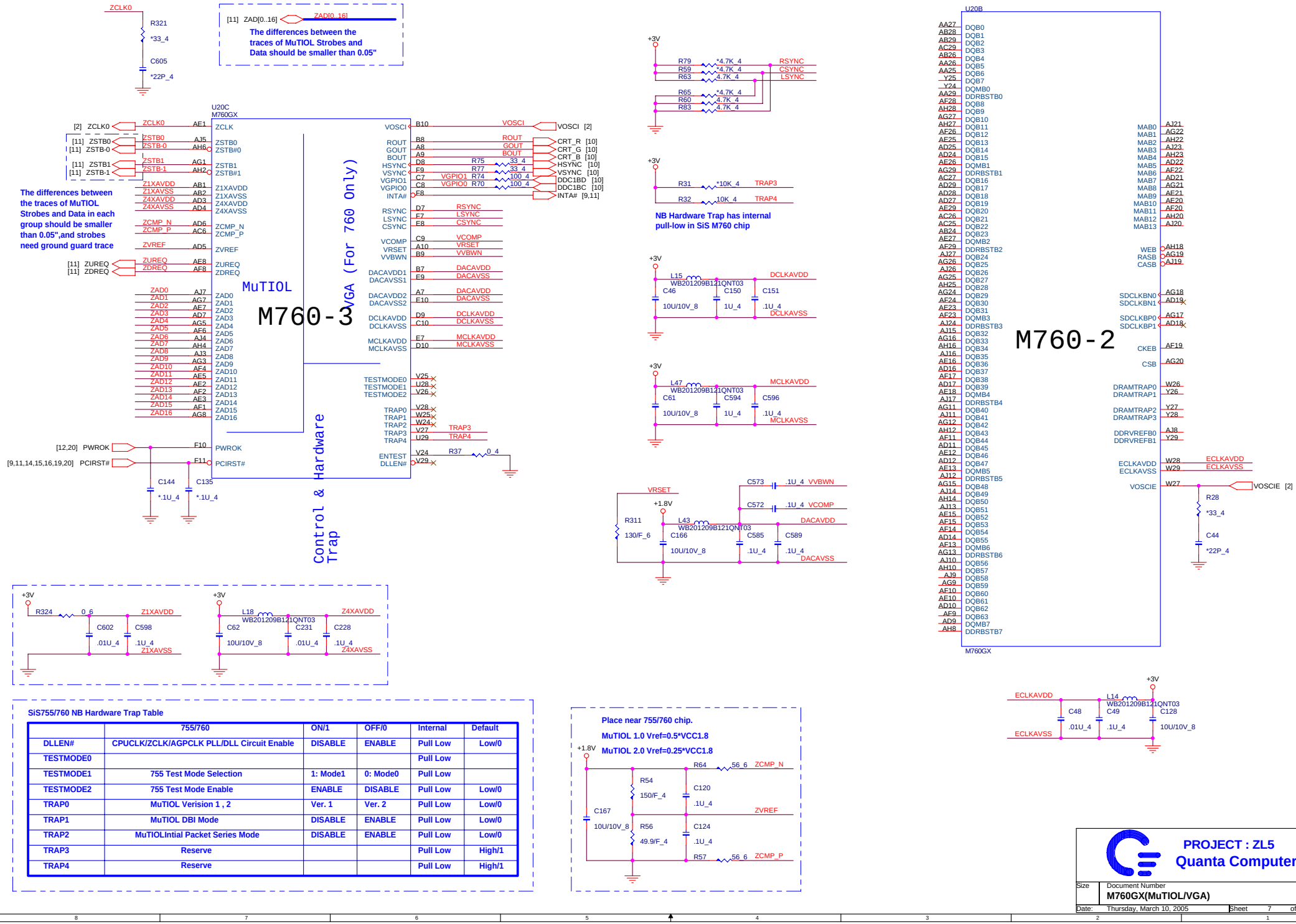

U21A
AMD K8
LDT
U21C
AMD K8
CTL & DBG
Near Socket754
Length < 1"
Width : 10mil
Length < 1"
Diff. Pair
Zdiff=80ohm
Trace route
as 10/10/10
Must shut down
when asserted
105mA
Max8863
Vset=1.25V
V=2.5
PROJECT : ZL5
Quanta Computer Inc.
CPU(HT LINK)
Thursday, March 10, 2005

CPU DDR/POWER I/F




UP
DIMM1
DOWN
DIMM0
CN21
CN20
2.5VSUS
DDR_VTT
+3V
MVREF_DM0
MVREF_DM1
DDR-SODIMM-STD-H4.0
DDR-SODIMM-STD-H8.0
MD_[63..0]
DQS_[7..0]
DM_[7..0]
MAA[13..0]
MAB[13..0]
20mil
PROJECT : ZL5
Quanta Computer Inc.
DDR SO-DIMM
Thursday, March 10, 2005
Sheet 5 of 26


HOST_TX
HOST_RX
M760-1
LVDS/AGP
U20A
M760GX
[3] CADIP[15..0]
[3] CADIN[15..0]
[3] CADOP[15..0]
[3] CADON[15..0]
CADIP[15..0]
CADIN[15..0]
CADOP[15..0]
CADON[15..0]
CLKIN0 [3]
CLKIP0 [3]
CLKIN1 [3]
CLKIP1 [3]
CTLIN0 [3]
CTLIP0 [3]
[9] VAD[11..0]
[9] VAGCLK
[9] VAHSYNC
[9] VAVSYNC
[9] VADE
[9] VBD[11..0]
[9] VBGCLK
[9] VBHSYNC
[9] VBVSYNC
[9] VBDE
[9] VBCTL1
[9] VBCTL0
+3V
A1XAVDD
R62
0_6
C230
.1U_4
C181
.01U_4
A1XAVSS
A4XAVDD
L48
WB201209B121CNT03
C597
.1U_4
C601
.01U_4
C59
10U/10V_8
A4XAVSS
HTAVDD
L16
WB201209B121CNT03
C145
.1U_4
C153
.01U_4
C56
10U/10V_8
HTAVSS
HTPHYAVDD
L40
WB201209B121CNT03
C566
.1U_4
C568
.01U_4
C47
10U/10V_8
HTPHYAVSS
+1.8V
R315
4.7K_4
VBCAD [9]
VBHCLK [9]
GCDET-
R_VAGCLK
R319
10_4
VAGCLK
R_VBGCLK
R85
10_4
VBGCLK
AGPCLK0 [2]
AGPRCOMP
AGPRCOMN
A1XAVDD
A1XAVSS
A4XAVDD
A4XAVSS
AVREFGC
20mil
R320
*33_4
C606
*22P_4
R318
124/F_6
R323
124/F_6
Near 200mil
Near 200mil
Place close to chip
+1.8V
AGPRCOMN
R90
49.9/F_6
CPU_VCCA
LDTREQ#
R52
1K_4
+1.2V_HT
LRCOMP
R29
100/F_6
LTCOMPN
R30
49.9/F_6
LTCOMPP
R36
49.9/F_6
AGPRCOMP
R322
43.2/F_6
VAGCLK
C604
*10P_4
VBGCLK
C227
*10P_4
MVBCLK
C212
*10P_4
[9] VBCLK
R80
10_4
+1.2V_HT
R49
75_4
R50
75_4
[2] CPUCLK1_L
CPUCLK1_L
C136
3900P_6
755CLK-
[2] CPUCLK1_H
CPUCLK1_H
C122
3900P_6
755CLK+
R53
169/F_6
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
M760GX(HT LINK/AGP)
Rev
3B
Date: Thursday, March 10, 2005
Sheet 6 of 26



755/760		ON/1	OFF/0	Internal	Default
DLLEN#	CPUCLK/ZCLK/AGPCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	Pull Low	Low/0
TESTMODE0				Pull Low	
TESTMODE1	755 Test Mode Selection	1: Mode1	0: Mode0	Pull Low	
TESTMODE2	755 Test Mode Enable	ENABLE	DISABLE	Pull Low	Low/0
TRAP0	MuTIOL Verision 1 , 2	Ver. 1	Ver. 2	Pull Low	Low/0
TRAP1	MuTIOL DBI Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP2	MuTIOLIntial Packet Series Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP3	Reserve			Pull Low	High/1
TRAP4	Reserve			Pull Low	High/1

Size	Document Number	Rev
	M760GX(MuTIOL/VGA)	3B
Date: Thursday, March 10, 2005	Sheet 7 of 26	

If Support SiS M760LV IVDD=1.5V

M760-4

Power

M760-5

Power

LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

Place these capacitors under 760 solder side.

PROJECT : ZL5

Quanta Computer Inc.

Size	Document Number	Rev
	M760GX(POWER)	3B
Date: Thursday, March 10, 2005	Sheet 8 of 26	

302ELV/302LV

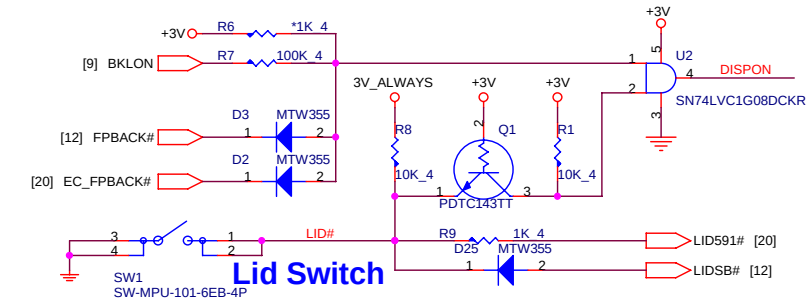
U18

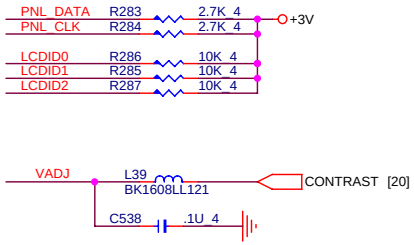
302ELV

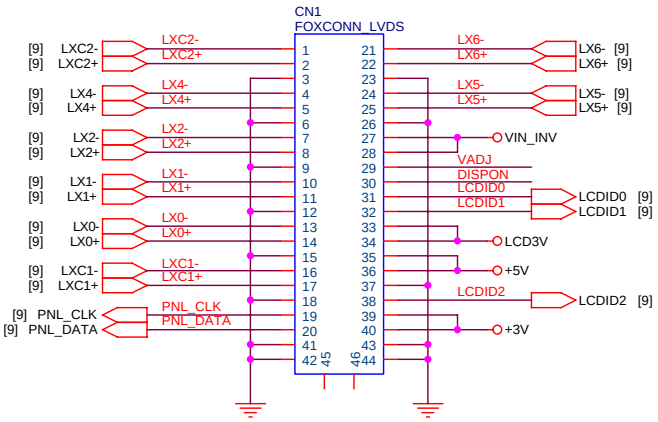
Reserved for EMI, Place close to U18

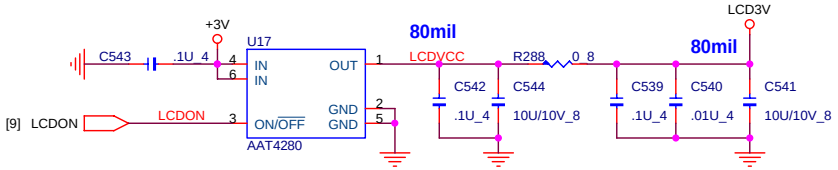
PROJECT : ZL5
Quanta Computer Inc.

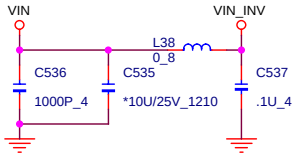
Size	Document Number	Rev
	302ELV(LVDS)	3B
Date: Thursday, March 10, 2005	Sheet 9 of 26	

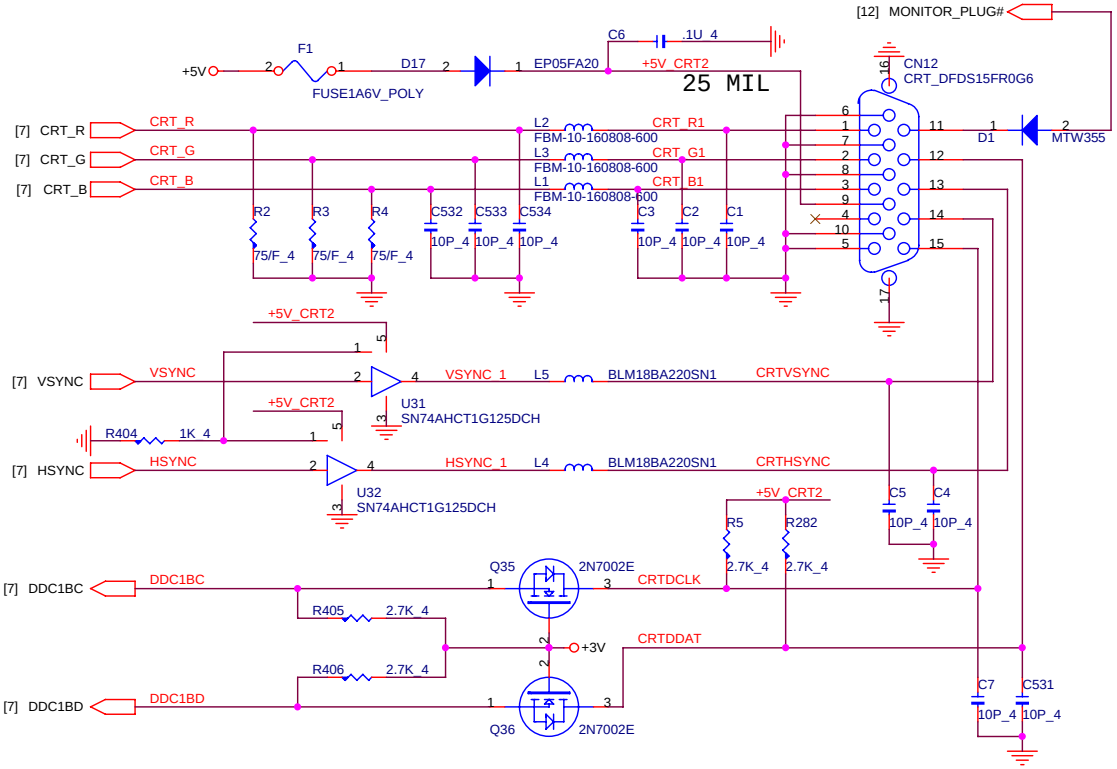


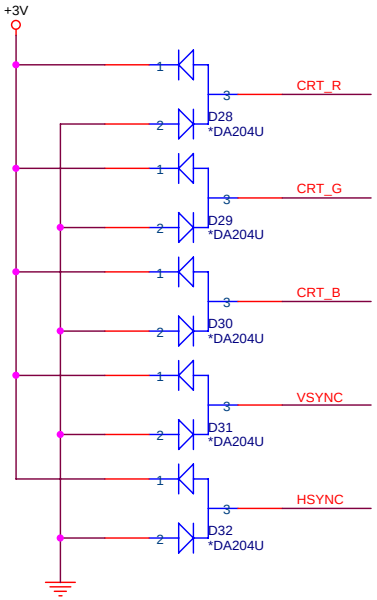






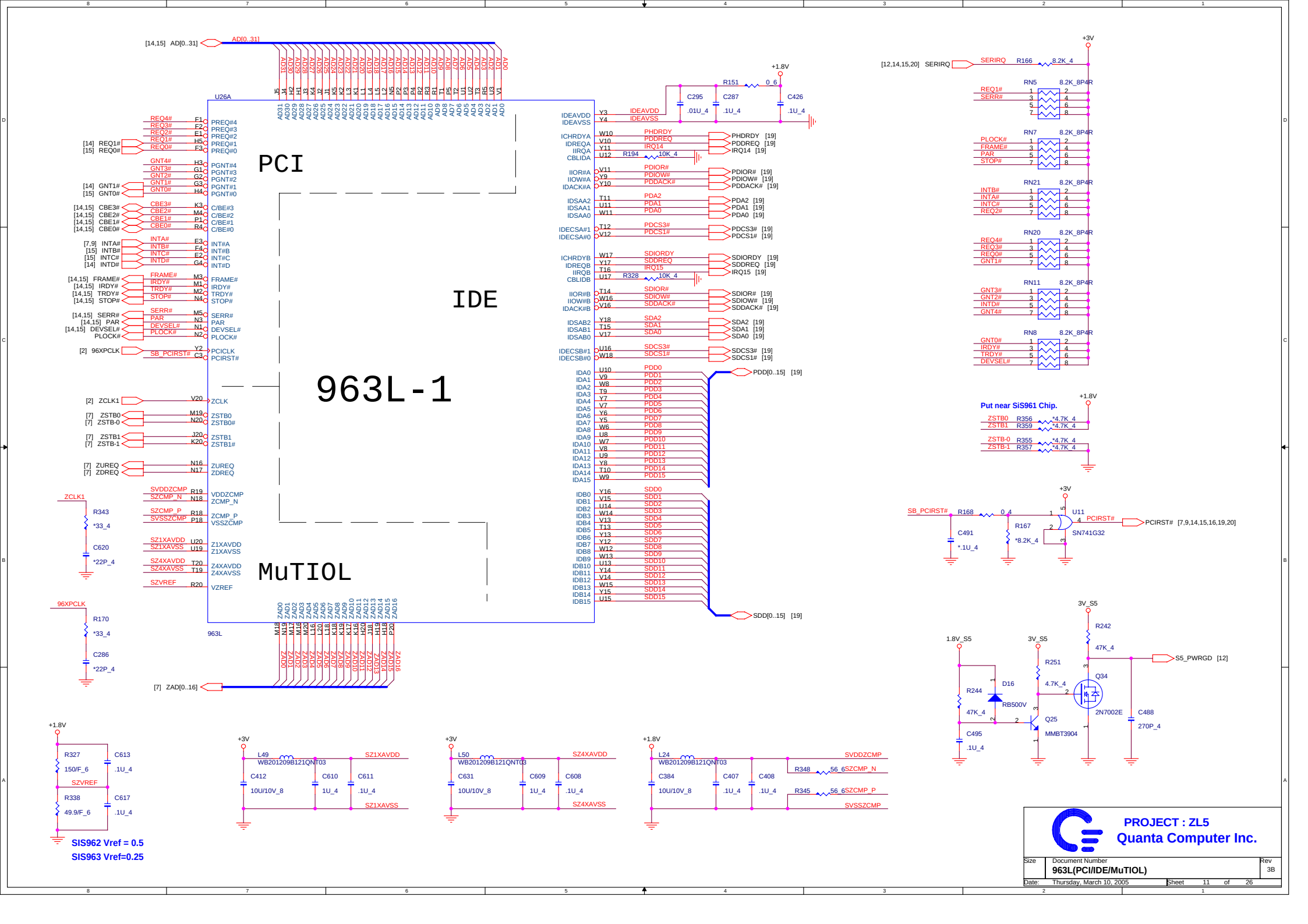


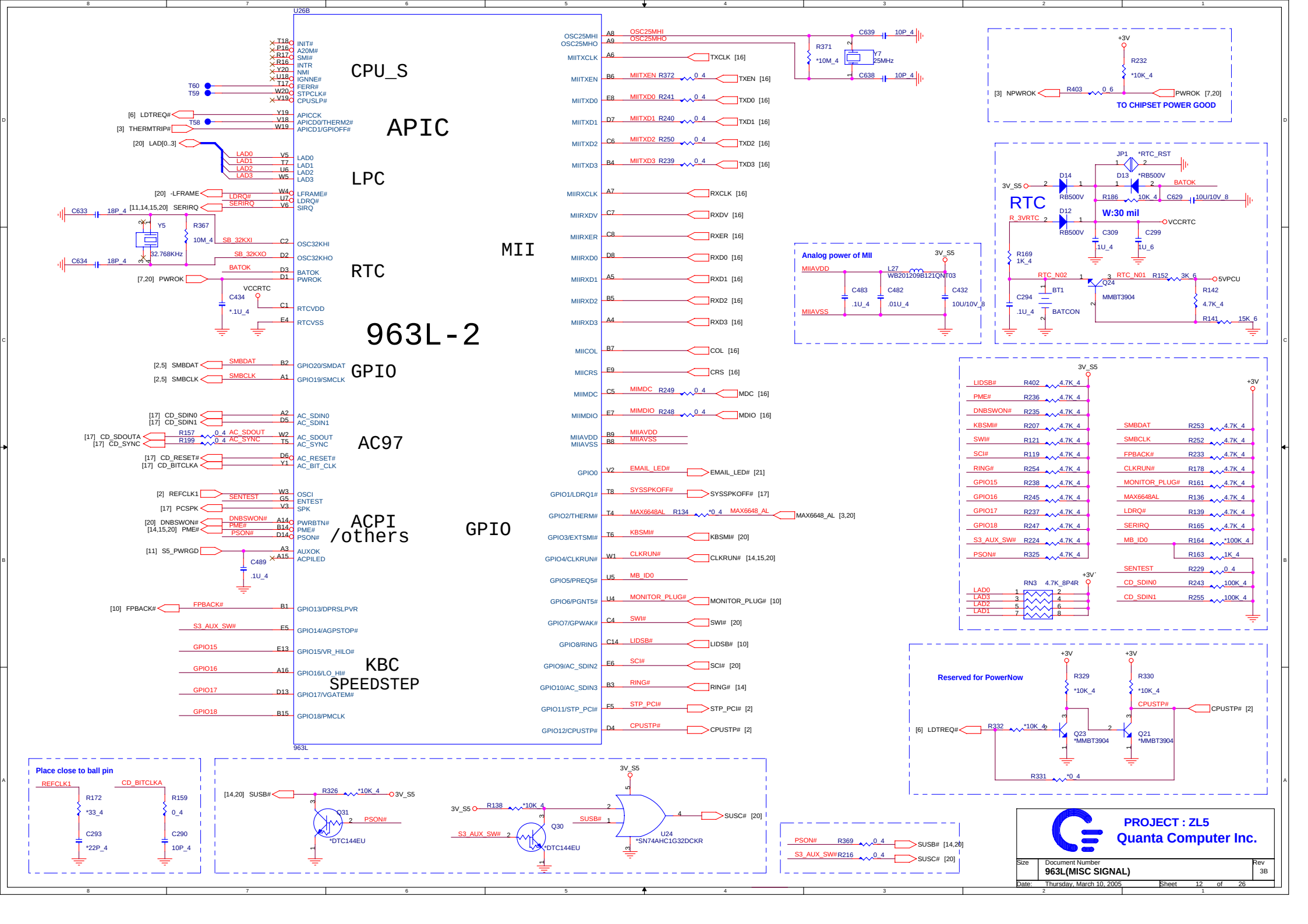


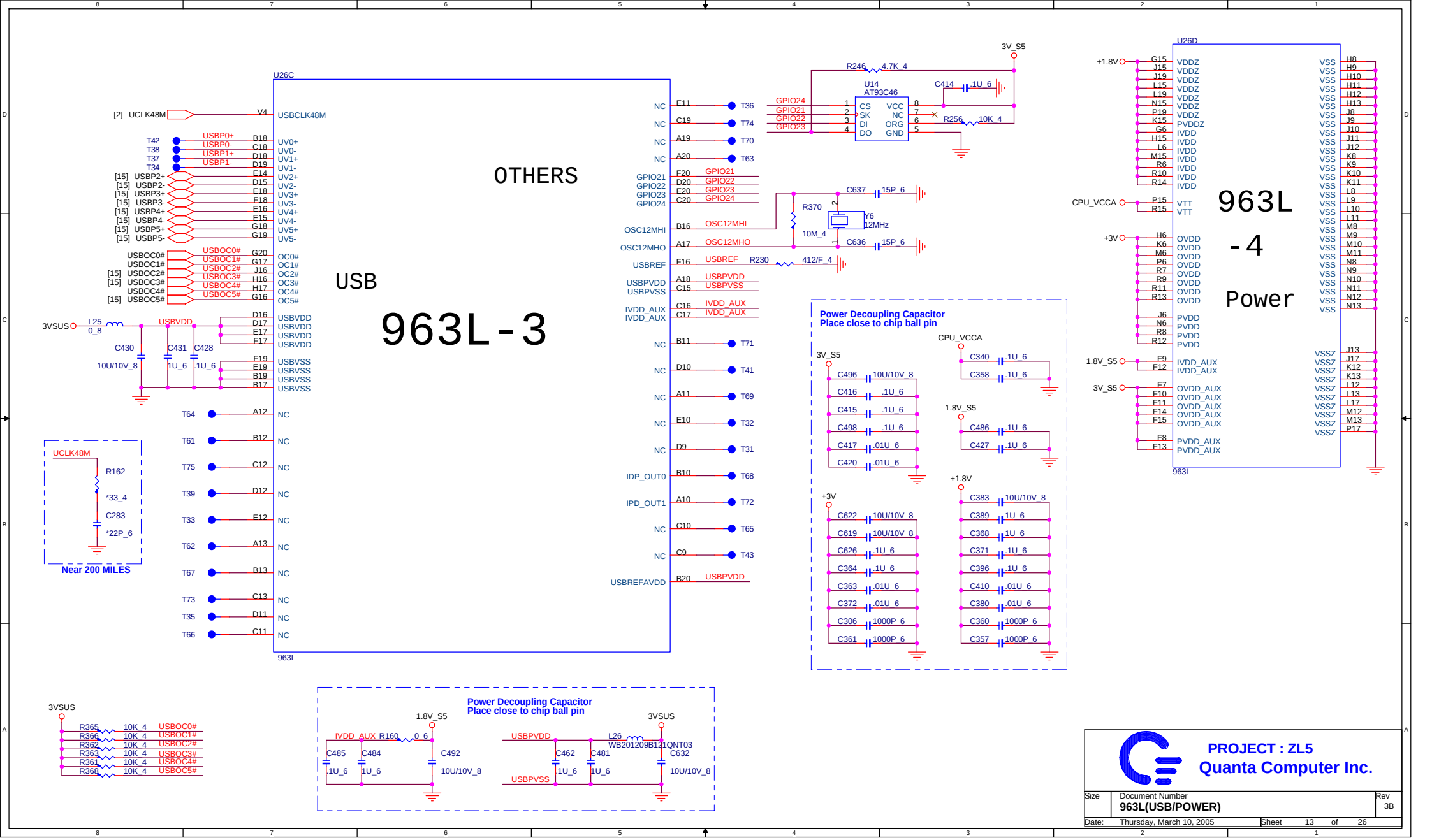


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS	3B
Date: Thursday, March 10, 2005	Sheet 10 of 26	


PCI
IDE
963L-1
MuTIOL
U26A
963L
Put near SiS961 Chip.
SIS962 Vref = 0.5
SIS963 Vref=0.25
PROJECT : ZL5
Quanta Computer Inc.
963L(PCI/IDE/MuTIOL)
Thursday, March 10, 2005


U26B
963L-2
CPU_S
APIC
LPC
RTC
MII
GPIO
AC97
ACPI /others
GPIO
KBC SPEEDSTEP
963L
INIT#
A20M#
SMI#
INTR
NMI
IGNNE#
FERR#
STPCLK#
CPUSLP#
APICCK
APICD0/THERM2#
APICD1/GPIOFF#
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ#
SIRQ
OSC32KHI
OSC32KHO
BATOK
PWROK
RTCVDD
RTCVSS
GPIO20/SMDAT
GPIO19/SMCLK
AC_SDIN0
AC_SDIN1
AC_SDOUT
AC_SYNC
AC_RESET#
AC_BIT_CLK
OSCI
ENTEST
SPK
PWRBTN#
PME#
PSON#
AUXOK
ACPILED
GPIO13/DPRSLPVR
GPIO14/AGPSTOP#
GPIO15/VR_HILO#
GPIO16/LO_HI#
GPIO17/VGATEM#
GPIO18/PMCLK
OSC25MHI
OSC25MHO
MIITXCLK
MIITXEN
MIITXD0
MIITXD1
MIITXD2
MIITXD3
MIIRXCLK
MIIRXDV
MIIRXER
MIIRXD0
MIIRXD1
MIIRXD2
MIIRXD3
MIICOL
MIICRS
MIIMDC
MIIMDIO
MIIAVDD
MIIAVSS
GPIO0
GPIO1/LDRQ1#
GPIO2/THERM#
GPIO3/EXTSMI#
GPIO4/CLKRUN#
GPIO5/PREQ5#
GPIO6/PGNT5#
GPIO7/GPWAK#
GPIO8/RING
GPIO9/AC_SDIN2
GPIO10/AC_SDIN3
GPIO11/STP_PCI#
GPIO12/CPUSTP#
TXCLK [16]
TXEN [16]
TXD0 [16]
TXD1 [16]
TXD2 [16]
TXD3 [16]
RXCLK [16]
RXDV [16]
RXER [16]
RXD0 [16]
RXD1 [16]
RXD2 [16]
RXD3 [16]
COL [16]
CRS [16]
MDC [16]
MDIO [16]
EMAIL_LED# [21]
SYSSPKOFF# [17]
MAX6648_AL [3,20]
KBSMI# [20]
CLKRUN# [14,15,20]
MONITOR_PLUG# [10]
SWI# [20]
LIDSB# [10]
SCI# [20]
RING# [14]
STP_PCI# [2]
CPUSTP# [2]
Analog power of MII
L27 WB201209B121QNT03
C483 .1U_4
C482 .01U_4
C432 10U/10V_8
RTC
W:30 mil
JP1 *RTC_RST
D14 RB500V
D13 *RB500V
D12 RB500V
BATOK
R186 10K_4
C629 10U/10V_8
C309 .1U_4
C299 1U_6
R169 1K_4
RTC_N02
RTC_N01
R152 3K_6
Q24 MMBT3904
R142 4.7K_4
R141 15K_6
C294 .1U_4
BT1 BATCON
TO CHIPSET POWER GOOD
R232 *10K_4
R403 0_6
Reserved for PowerNow
R329 *10K_4
R330 *10K_4
R332 *10K_4
Q23 *MMBT3904
Q21 *MMBT3904
R331 *0_4
Place close to ball pin
R172 *33_4
C293 *22P_4
R159 0_4
C290 10P_4
Q31 *DTC144EU
Q30 *DTC144EU
U24 *SN74AHC1G32DCKR
PROJECT : ZL5
Quanta Computer Inc.
963L(MISC SIGNAL)
Thursday, March 10, 2005
Sheet 12 of 26


U26C
USB
963L-3
OTHERS
963L
U26D
963L
-4
Power
963L
U14
AT93C46
Power Decoupling Capacitor
Place close to chip ball pin
Near 200 MILES
Power Decoupling Capacitor
Place close to chip ball pin
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
963L(USB/POWER)
Rev
3B
Date: Thursday, March 10, 2005
Sheet 13 of 26

ID Select : AD17
Interrupt Pin : INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

U13
PCI1410A

U15
TPS2211A

CARDBUS SLOT

CN22

FOX_WZ21131-G2

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA(PCI1410)	3B

Date: Thursday, March 10, 2005 Sheet 14 of 26

ID Select : AD22
Interrupt Pin : INTB# , INTC#
Request Indicate : REQ0#
Grant Indicate : GNT0#

PCLK_MP R66 *22_4 C161 *10P_4

IDSEL_MP R48 150_4 AD22

[11,14] AD[0..31] AD[0..31]

MINI-PCI

CN17

[21] WIRELESS_LED
[20] RF_EN
D4 MTW355
[11] INTC#
[2] PCLK_MP
[11] REQ0#
[11,14] CBE3#
[11,14] CBE2#
[11,14] IRDY#
[12,14,20] CLKRUN#
[11,14] SERR#
R42 10K_4
[11,14] CBE1#

1	TIP	RING	2
3	LAN1	LAN2	4
5	LAN3	LAN4	6
7	LAN5	LAN6	8
9	LAN7	LAN8	10
11	LED_GP	LED_YP	12
13	LED_GN	LED_YN	14
15	NC1	NC2	16
17	-INTB	+5V	18
19	+3V	-INTA	20
21	R(IRQ3)	R(IRQ4)	22
23	GND	+3VAUX	24
25	PCICLK	-RST	26
27	GND	+3V	28
29	-REQ	-GNT	30
31	+3V	GND	32
33	AD31	-PME	34
35	AD29	(V)	36
37	GND	AD30	38
39	AD27	+3V	40
41	AD25	AD28	42
43	(V)	AD26	44
45	-CBE3	AD24	46
47	AD23	IDSEL	48
49	GND	GND	50
51	AD21	AD22	52
53	AD19	AD20	54
55	GND	PAR	56
57	AD17	AD18	58
59	-CBE2	AD16	60
61	-IRDY	GND	62
63	+3V	-FRAME	64
65	-CLKRUN	-TRDY	66
67	-SERR	-STOP	68
69	GND	+3V	70
71	-PERR	-DEVSEL	72
73	-CBE1	GND	74
75	AD14	AD15	76
77	GND	AD13	78
79	AD12	AD11	80
81	AD10	GND	82
83	GND	AD9	84
85	AD8	-CBE0	86
87	AD7	+3V	88
89	+3V	AD6	90
91	AD5	AD4	92
93	(V)	AD2	94
95	AD3	AD0	96
97	+5V	(V)	98
99	AD1	SERIRQ	100
101	GND	GND	102
103	SYNC	M66EN	104
105	SDIN0	SDOUT	106
107	BITCLK	SDIN1	108
109	-AC_PRIMARY	-RESET	110
111	BEEP	-MPCICACK	112
113	AGND	AGND	114
115	+MIC	+SPK	116
117	-MIC	-SPK	118
119	AGND	AGND	120
121	-RI	NC4	122
123	+5VA	+3VAUX	124
	GND	GND	
125			126

MINIPCI_DGMC4000382

+3V, +5V, 3VSUS

INTB# [11]
PCIRST# [7,9,11,14,16,19,20]
GNT0# [11]
PME# [12,14,20]
PAR [11,14]
FRAME# [11,14]
TRDY# [11,14]
STOP# [11,14]
DEVSEL# [11,14]
CBE0# [11,14]
SERIRQ [11,12,14,20]

SDIN1_MINI R33 *10K_4 3V_S5

VIN, +5V

C221 .1U_6
C557 .1U_6
C50 .1U_6
C709 .1U_6

+3V: C186 .1U_4, C54 .1U_4, C53 .1U_4, C169 .1U_4
+5V: C41 .1U_4, C187 .1U_4
VIN: C642 *.01U_6, C683 *.01U_6, C684 *.1U_6, C641 *.1U_6, C640 *.1U_6, C682 *10U/25V_1210

[20] USBPWR_ON# R94 0_4 R92 *0_4

U6 TPS2061DGNR
5VSUS, USBPWRON#
USBPWR2 R100 0_4 USBOC2# [13]
R96 *6.34K/F_6

U9 TPS2061DGNR
5VSUS, USBPWRON#
USBPWR3 R124 0_4 USBOC3# [13]
R122 *6.34K/F_6

U16 TPS2061DGNR
5VSUS, USBPWRON#
USBPWR5 R267 0_4 USBOC5# [13]
R268 *6.34K/F_6

USB2POWER
C240 47U/6.3V_1210
USBPWR2 L19 BK2125HS330
[13] USBP2-
[13] USBP2+
L17 DLW21HN900SQ2L
C226 *10P_4
C233 *10P_4
BUSBP2-
BUSBP2+
CN18 USB_DFHD04MR671

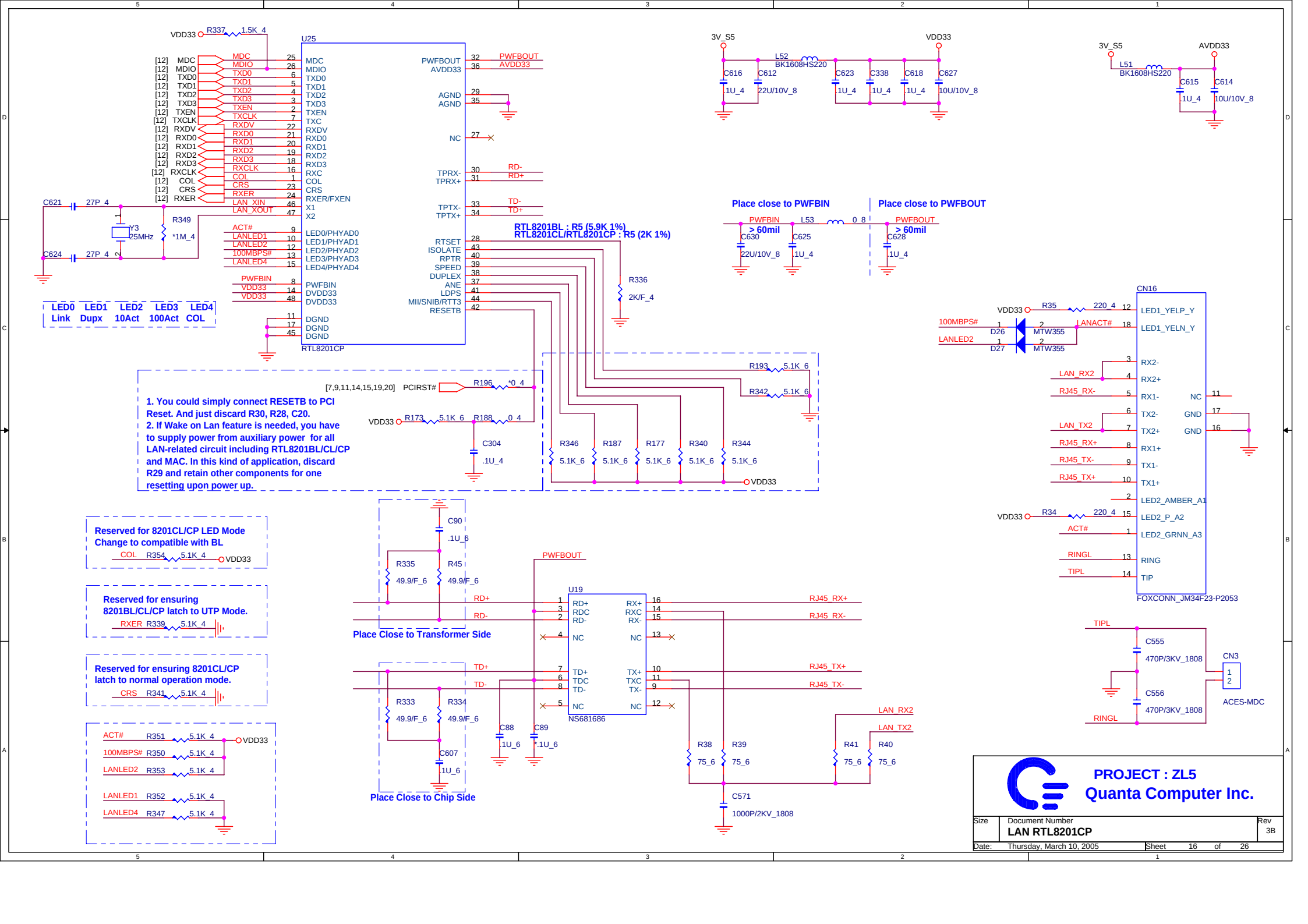
USB3POWER
C251 47U/6.3V_1210
USBPWR3 L21 BK2125HS330
[13] USBP3-
[13] USBP3+
L20 DLW21HN900SQ2L
C243 *10P_4
C246 *10P_4
BUSBP3-
BUSBP3+
CN19 USB_DFHD04MR671

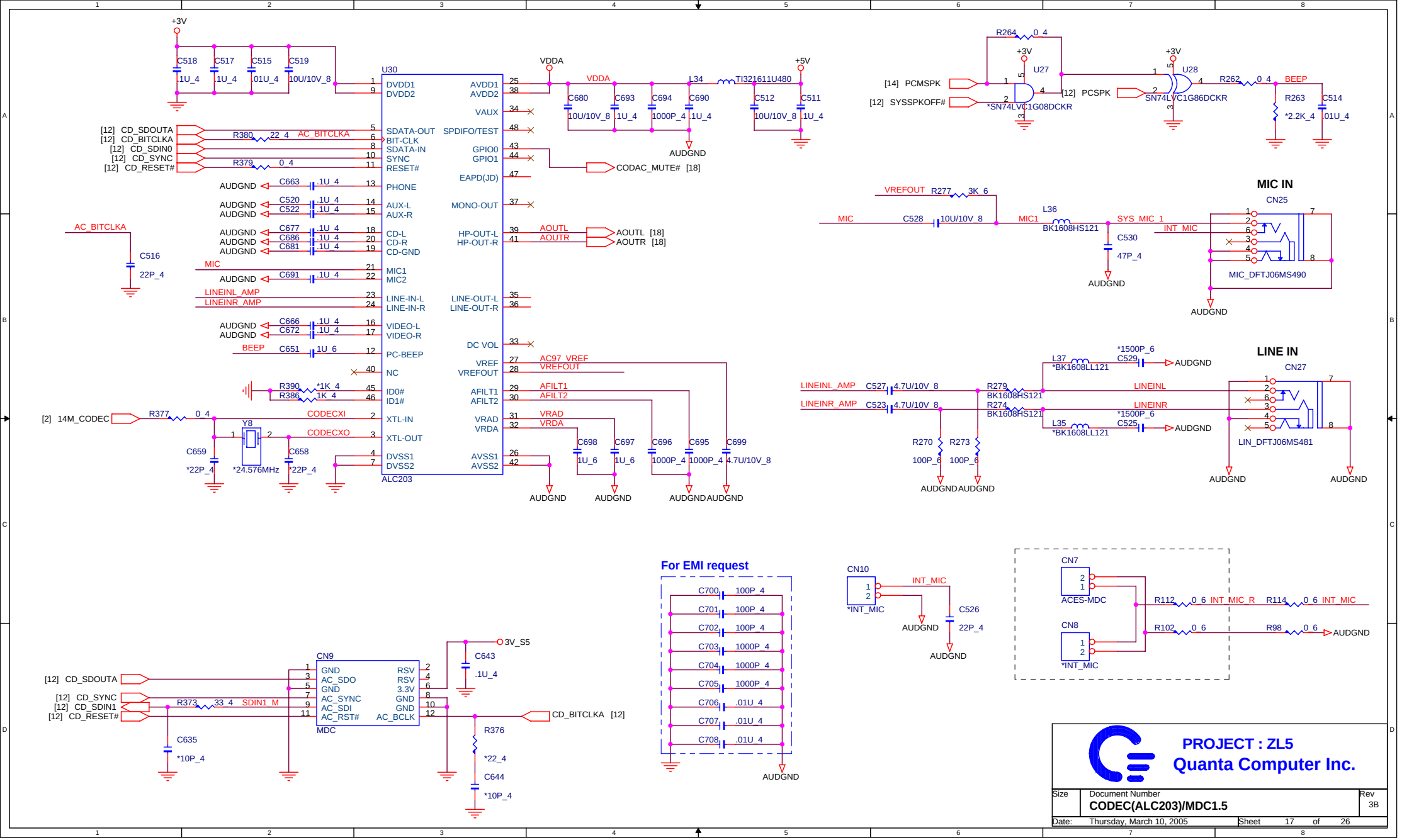
USB5POWER
C521 47U/6.3V_1210
USBPWR5 L32 BK2125HS330
[13] USBP5-
[13] USBP5+
L33 DLW21HN900SQ2L
C678 *10P_4
C679 *10P_4
BUSBP5-
BUSBP5+
CN24 USB_DFHD04MR671

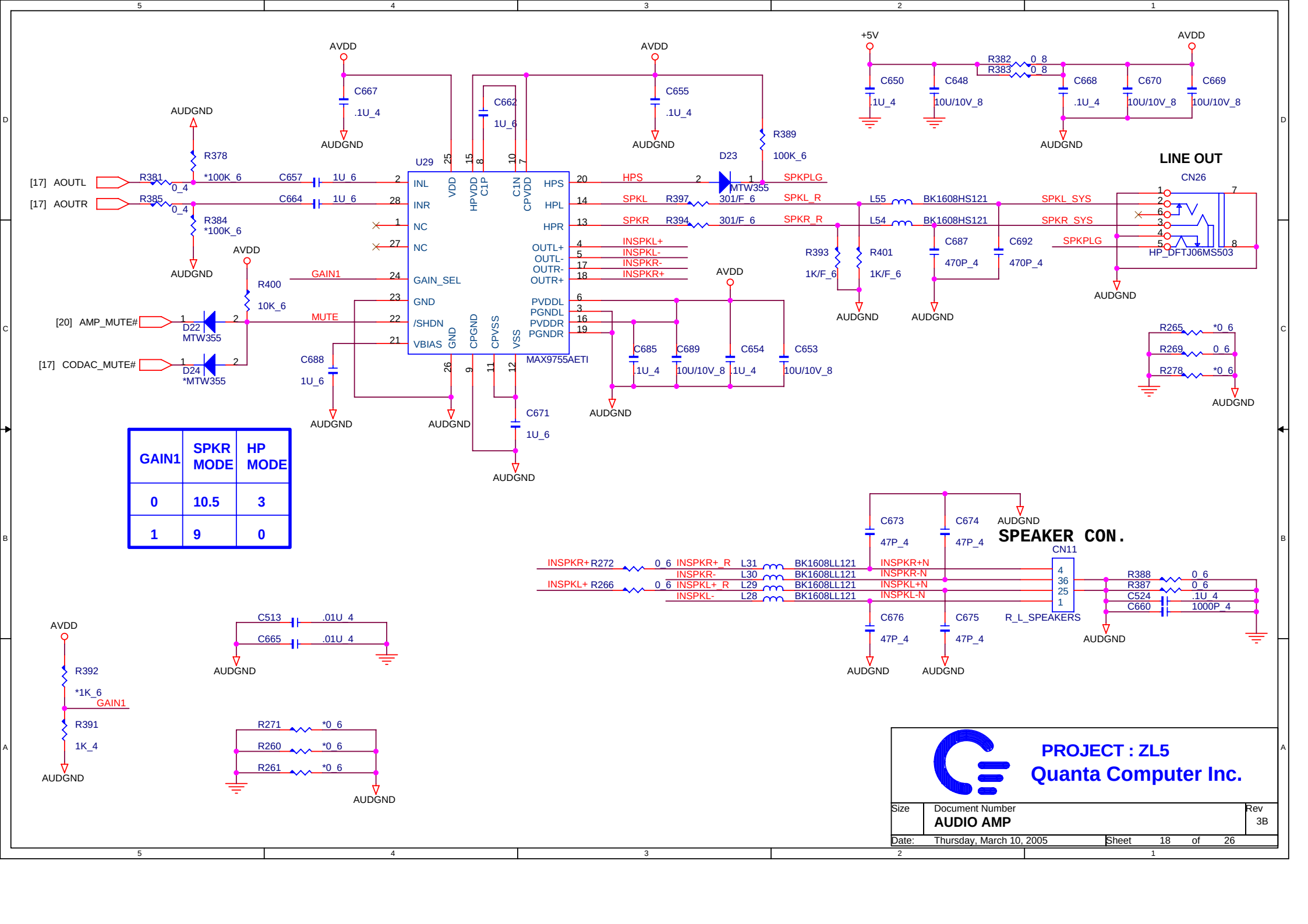
BT_POWERON# [20]
Q29 AO3403
3VSUS
C590 10U/10V_8
BT_POWER
L42 BK2125HS330
[13] USBP4+
[13] USBP4-
L41 DLW21HN900SQ2L
C587 *10P_4
C588 *10P_4
BUSBP4+
BUSBP4-
[21] BT_LED
C586 .01U_4
CN5 PTWO_MINIUSB

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI/USB	3B
Date: Thursday, March 10, 2005	Sheet 15 of 26	


U25
RTL8201CP
RTL8201BL : R5 (5.9K 1%)
RTL8201CL/RTL8201CP : R5 (2K 1%)
LED0 LED1 LED2 LED3 LED4
Link Dupx 10Act 100Act COL
1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.
Reserved for 8201CL/CP LED Mode Change to compatible with BL
Reserved for ensuring 8201BL/CL/CP latch to UTP Mode.
Reserved for ensuring 8201CL/CP latch to normal operation mode.
Place Close to Transformer Side
Place Close to Chip Side
Place close to PWFBIN
Place close to PWFBOUT
U19
NS681686
CN16
FOXCONN_JM34F23-P2053
CN3
ACES-MDC
PROJECT : ZL5
Quanta Computer Inc.
LAN RTL8201CP
Thursday, March 10, 2005
Sheet 16 of 26


U30
ALC203
DVDD1
DVDD2
AVDD1
AVDD2
VAUX
SDATA-OUT
BIT-CLK
SDATA-IN
SYNC
RESET#
SPDIFO/TEST
GPIO0
GPIO1
EAPD(JD)
PHONE
MONO-OUT
AUX-L
AUX-R
CD-L
CD-R
CD-GND
HP-OUT-L
HP-OUT-R
MIC1
MIC2
LINE-IN-L
LINE-IN-R
LINE-OUT-L
LINE-OUT-R
VIDEO-L
VIDEO-R
PC-BEEP
DC VOL
NC
VREF
VREFOUT
ID0#
ID1#
AFILT1
AFILT2
XTL-IN
XTL-OUT
VRAD
VRDA
DVSS1
DVSS2
AVSS1
AVSS2
+3V
VDDA
+5V
AUDGND
AOUTL
AOUTR
AC97_VREF
CODAC_MUTE# [18]
[12] CD_SDOUTA
[12] CD_BITCLKA
[12] CD_SDIN0
[12] CD_SYNC
[12] CD_RESET#
AC_BITCLKA
MIC
LINEINL_AMP
LINEINR_AMP
BEEP
[2] 14M_CODEC
CODECXI
CODECXO
*24.576MHz
R264
U27
U28
SN74LVC1G08DCKR
SN74LVC1G86DCKR
[14] PCMSPK
[12] SYSSPKOFF#
[12] PCSPK
MIC IN
CN25
MIC_DFTJ06MS490
INT_MIC
SYS_MIC_1
LINE IN
CN27
LIN_DFTJ06MS481
LINEINL
LINEINR
*BK1608LL121
BK1608HS121
CN9
MDC
GND
AC_SDO
AC_SYNC
AC_SDI
AC_RST#
AC_BCLK
RSV
3.3V
3V_S5
CD_BITCLKA [12]
For EMI request
CN10
*INT_MIC
CN7
ACES-MDC
CN8
R112
R114
R102
R98
INT_MIC_R
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
CODEC(ALC203)/MDC1.5
Rev
3B
Date: Thursday, March 10, 2005
Sheet 17 of 26

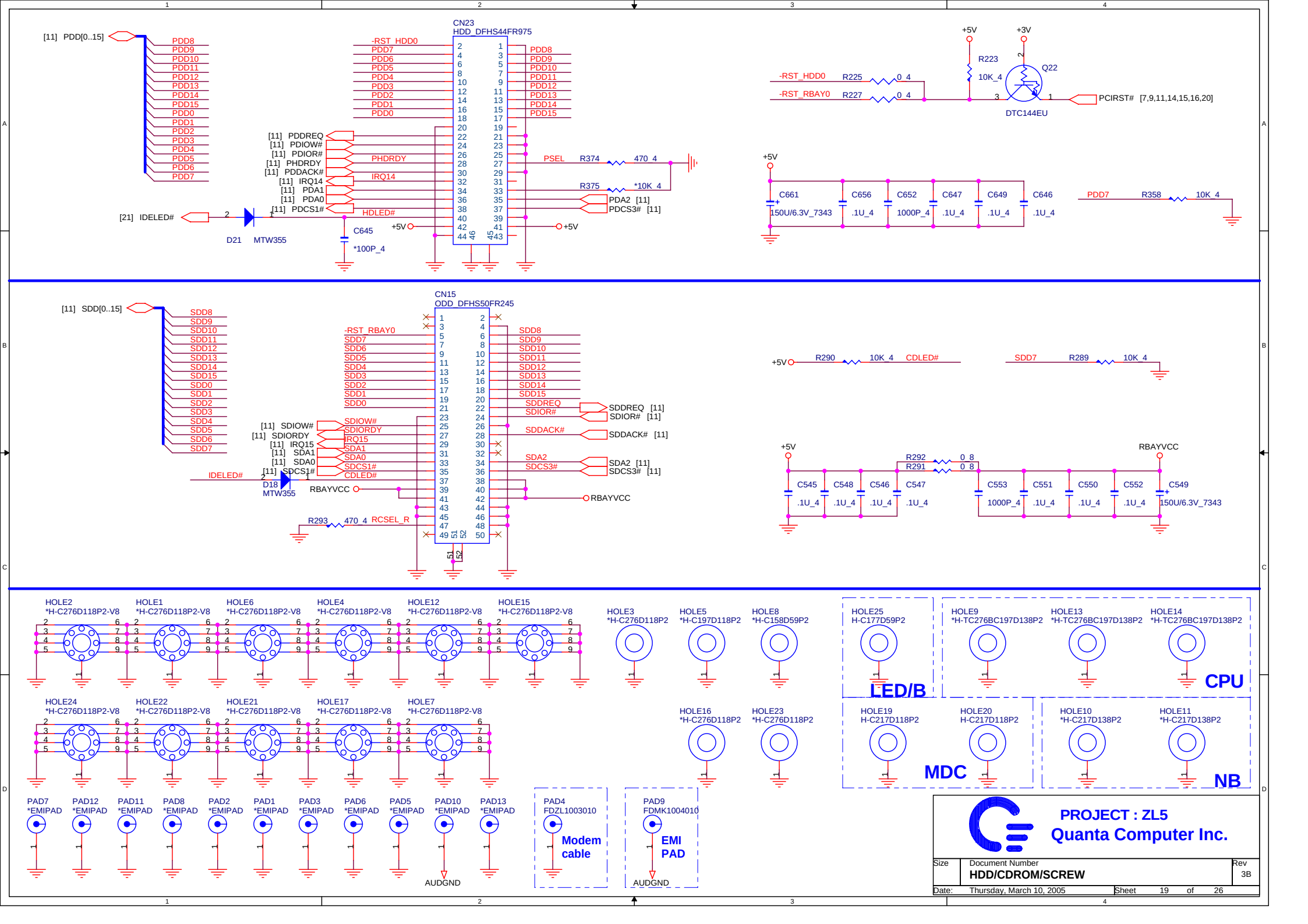


GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

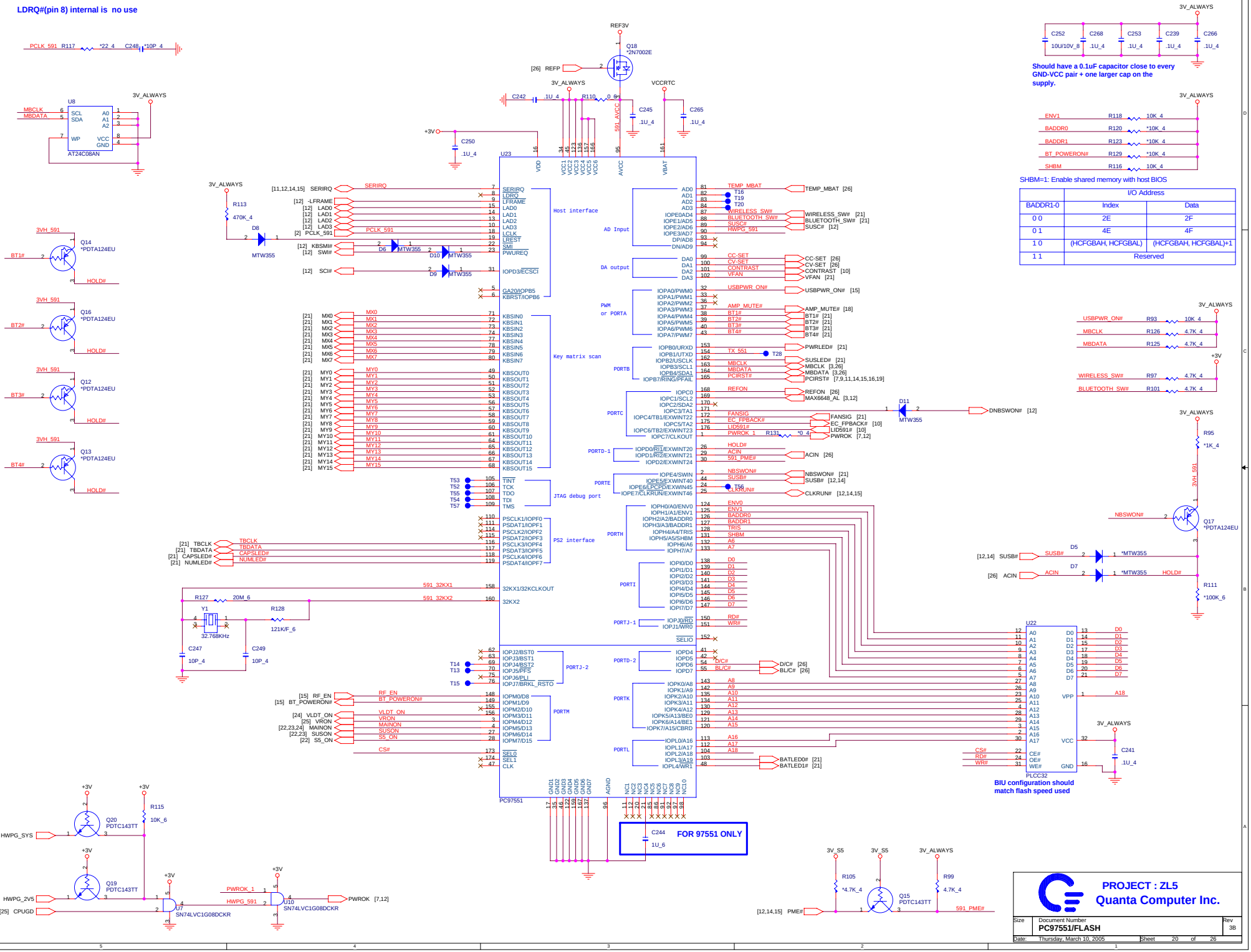
PROJECT : ZL5

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP	3B
Date: Thursday, March 10, 2005	Sheet 18 of 26	


[11] PDD[0..15]
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
CN23
HDD_DFHS44FR975
-RST_HDD0
[11] PDDREQ
[11] PDIOW#
[11] PDIOR#
PHDRDY
[11] PHDRDY
[11] PDDACK#
IRQ14
[11] IRQ14
[11] PDA1
[11] PDA0
[11] PDCS1#
HDLED#
[21] IDELED#
D21 MTW355
C645
*100P_4
+5V
PSEL
R374 470_4
R375 *10K_4
PDA2 [11]
PDCS3# [11]
+3V
R223 10K_4
Q22
-RST_RBAY0
R225 0_4
R227 0_4
DTC144EU
PCIRST# [7,9,11,14,15,16,20]
C661 150U/6.3V_7343
C656 .1U_4
C652 1000P_4
C647 .1U_4
C649 .1U_4
C646 .1U_4
PDD7 R358 10K_4
[11] SDD[0..15]
SDD8
SDD9
SDD10
SDD11
SDD12
SDD13
SDD14
SDD15
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
CN15
ODD_DFHS50FR245
-RST_RBAY0
SDDREQ
SDIOR#
SDDACK#
[11] SDIOW#
[11] SDIORDY
SDIOW#
SDIORDY
IRQ15
[11] IRQ15
[11] SDA1
[11] SDA0
[11] SDCS1#
CDLED#
SDA2
SDCS3#
SDDREQ [11]
SDIOR# [11]
SDDACK# [11]
SDA2 [11]
SDCS3# [11]
IDELED#
D18 MTW355
RBAYVCC
R293 470_4 RCSEL_R
R290 10K_4 CDLED#
SDD7 R289 10K_4
R292 0_8
R291 0_8
C545 .1U_4
C548 .1U_4
C546 .1U_4
C547 .1U_4
C553 1000P_4
C551 .1U_4
C550 .1U_4
C552 .1U_4
C549 150U/6.3V_7343
HOLE2 *H-C276D118P2-V8
HOLE1 *H-C276D118P2-V8
HOLE6 *H-C276D118P2-V8
HOLE4 *H-C276D118P2-V8
HOLE12 *H-C276D118P2-V8
HOLE15 *H-C276D118P2-V8
HOLE3 *H-C276D118P2
HOLE5 *H-C197D118P2
HOLE8 *H-C158D59P2
HOLE25 H-C177D59P2
HOLE9 *H-TC276BC197D138P2
HOLE13 *H-TC276BC197D138P2
HOLE14 *H-TC276BC197D138P2
LED/B
CPU
HOLE24 *H-C276D118P2-V8
HOLE22 *H-C276D118P2-V8
HOLE21 *H-C276D118P2-V8
HOLE17 *H-C276D118P2-V8
HOLE7 *H-C276D118P2-V8
HOLE16 *H-C276D118P2
HOLE23 *H-C276D118P2
HOLE19 H-C217D118P2
HOLE20 H-C217D118P2
HOLE10 *H-C217D138P2
HOLE11 *H-C217D138P2
MDC
NB
PAD7 *EMIPAD
PAD12 *EMIPAD
PAD11 *EMIPAD
PAD8 *EMIPAD
PAD2 *EMIPAD
PAD1 *EMIPAD
PAD3 *EMIPAD
PAD6 *EMIPAD
PAD5 *EMIPAD
PAD10 *EMIPAD
PAD13 *EMIPAD
AUDGND
PAD4 FDZL1003010
Modem cable
PAD9 FDMK1004010
EMI PAD
AUDGND
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
HDD/CDROM/SCREW
Rev 3B
Date: Thursday, March 10, 2005
Sheet 19 of 26

LDRQ#(pin 8) internal is no use

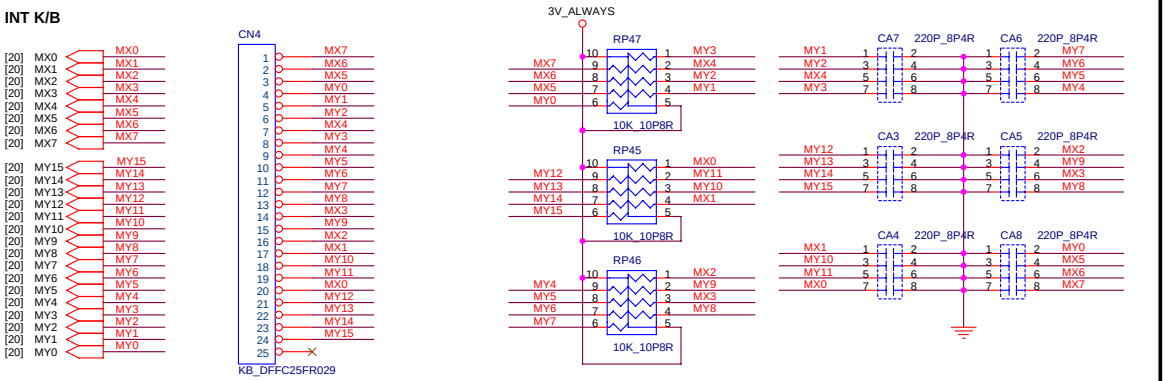


PROJECT : ZL5
Quanta Computer Inc.

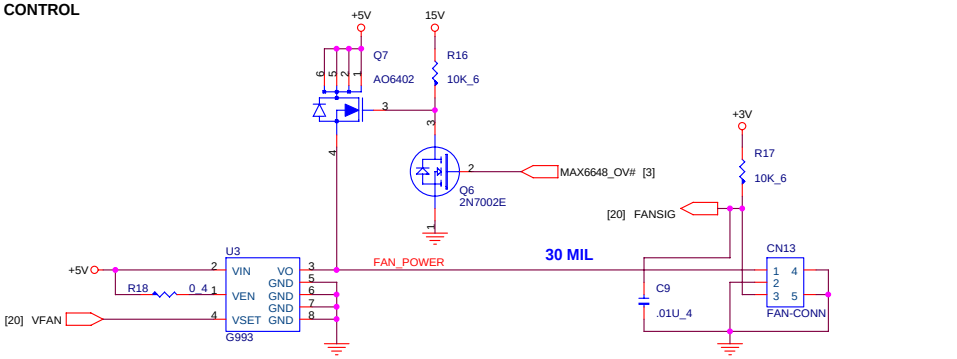
Size	Document Number	Rev
	PC97551/FLASH	3B

Date: Thursday, March 10, 2005 Sheet 20 of 26

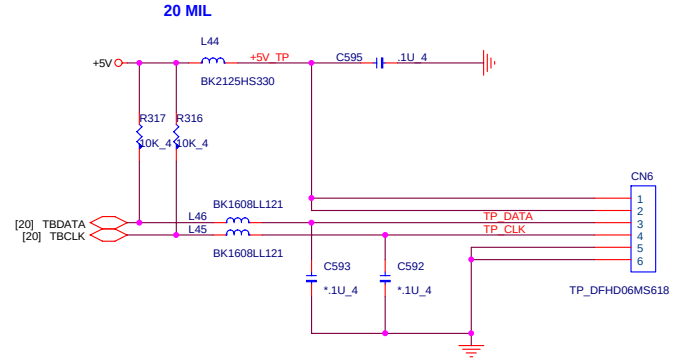
INT K/B

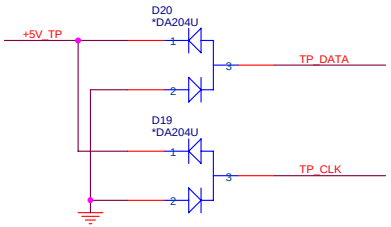


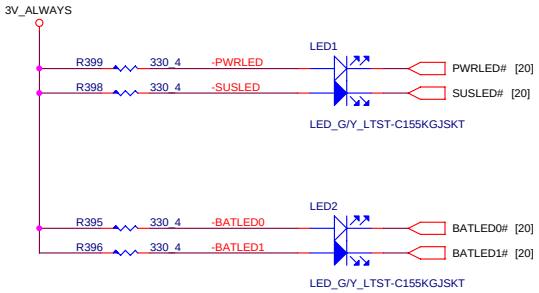
FAN CONTROL

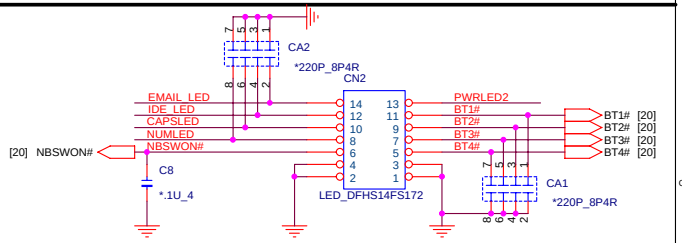


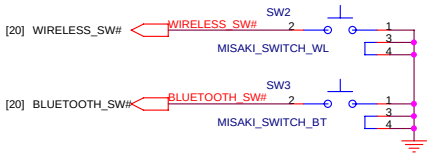
TOUCH PAD

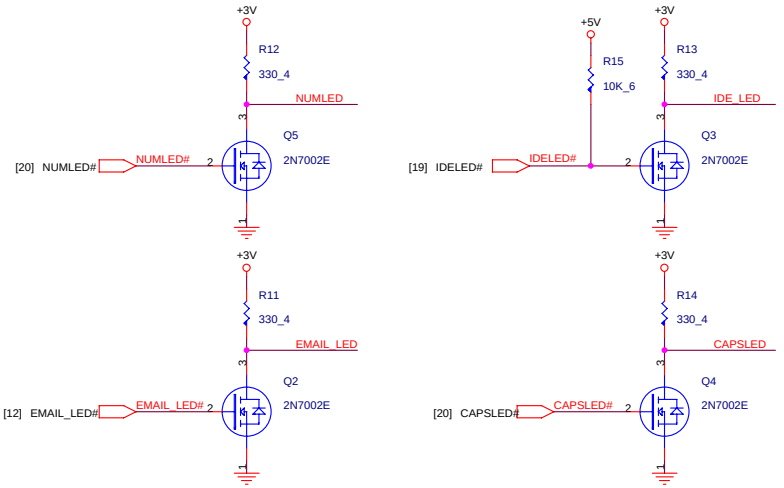


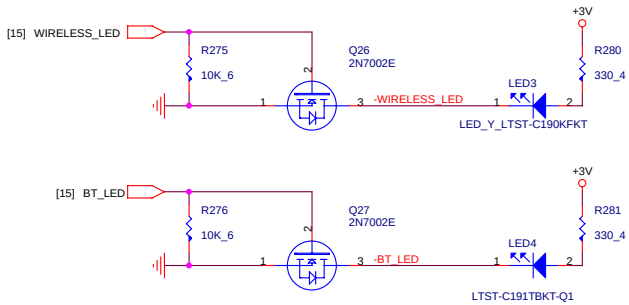






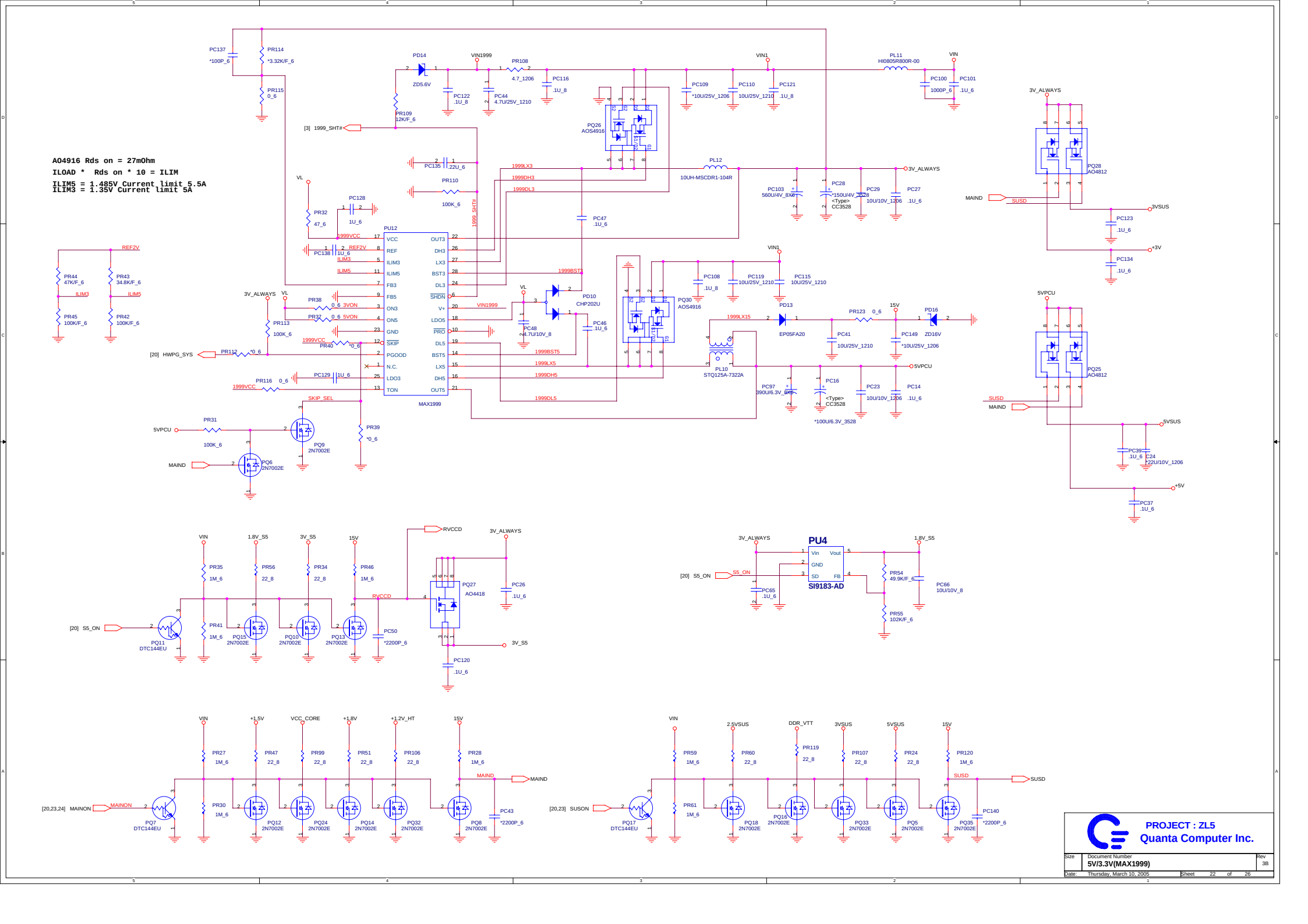


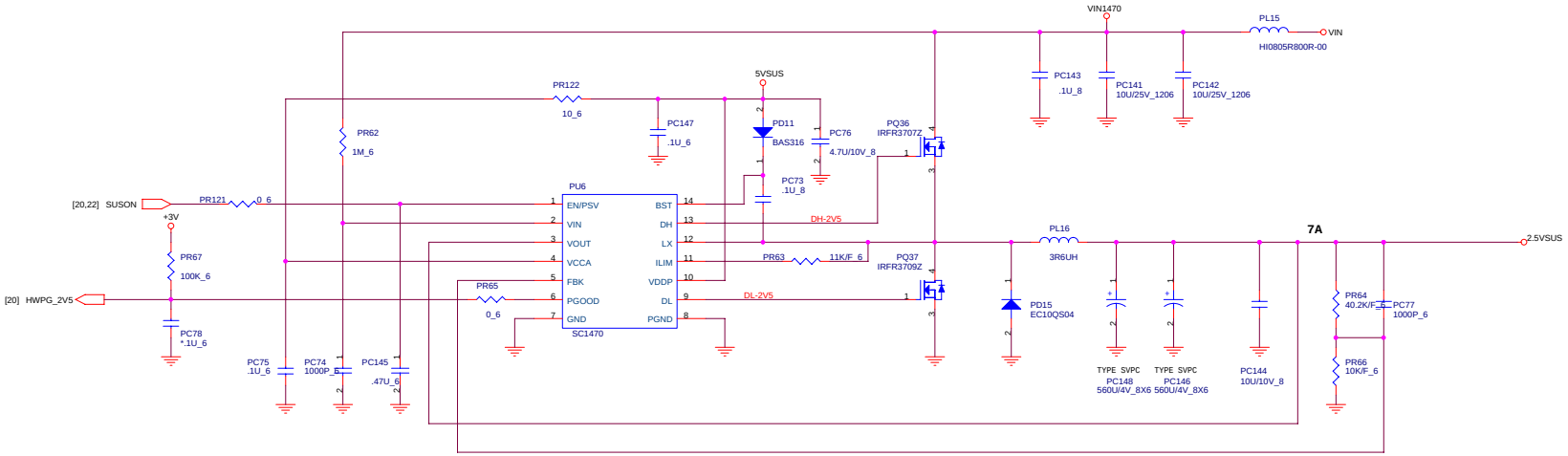


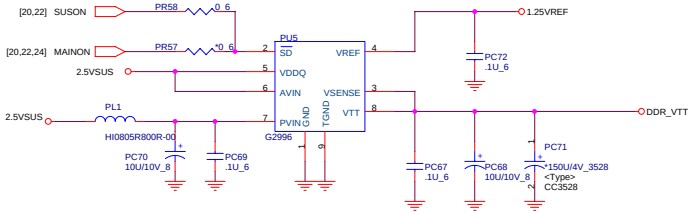


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	TP/FAN/SWITCH/LED/KB	3B
Date: Thursday, March 10, 2005	Sheet 21 of 26	

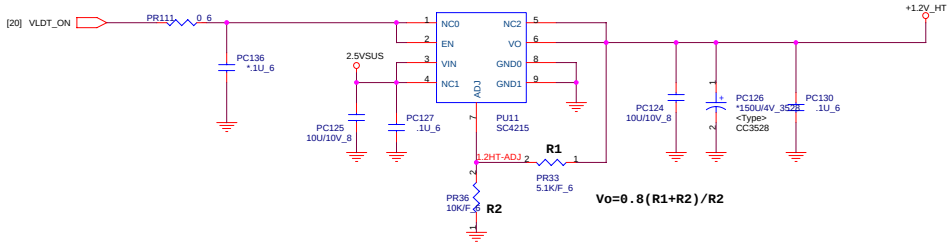

AO4916 Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM5 = 1.485V Current limit 5.5A
ILIM3 = 1.35V Current limit 5A
MAX1999
PU4
SI9183-AD
PROJECT : ZL5
Quanta Computer Inc.
5V/3.3V(MAX1999)
Thursday, March 10, 2005

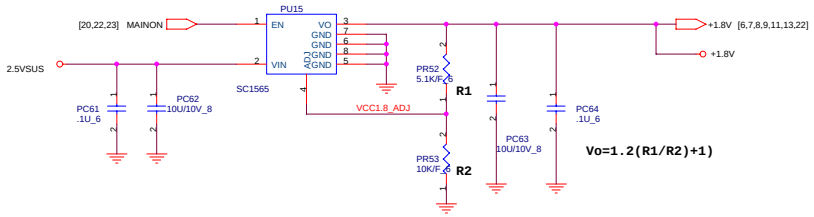


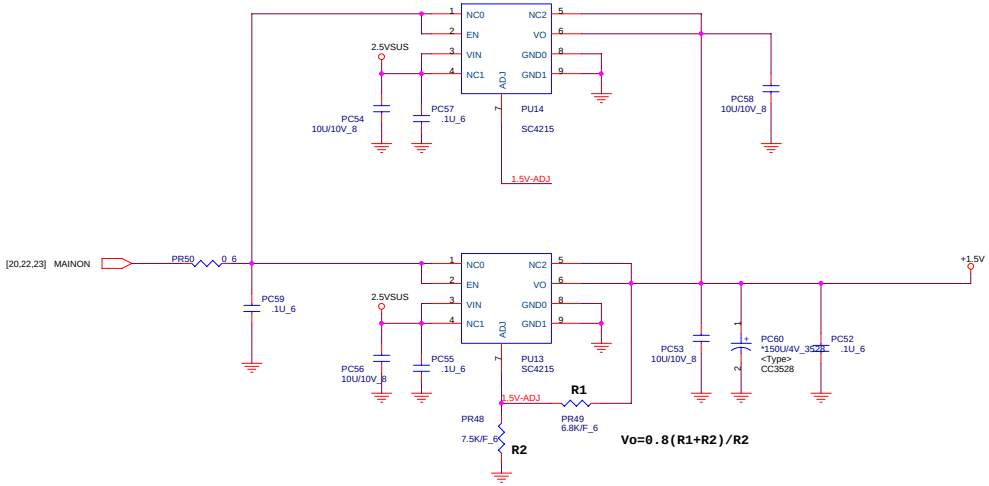


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS/+1.25TERM	3B
Date: Thursday, March 10, 2005	Sheet 23 of 25	







PROJECT : ZL5
Quanta Computer Inc.

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	+1.5V/+1.8V/+1.2V	3B
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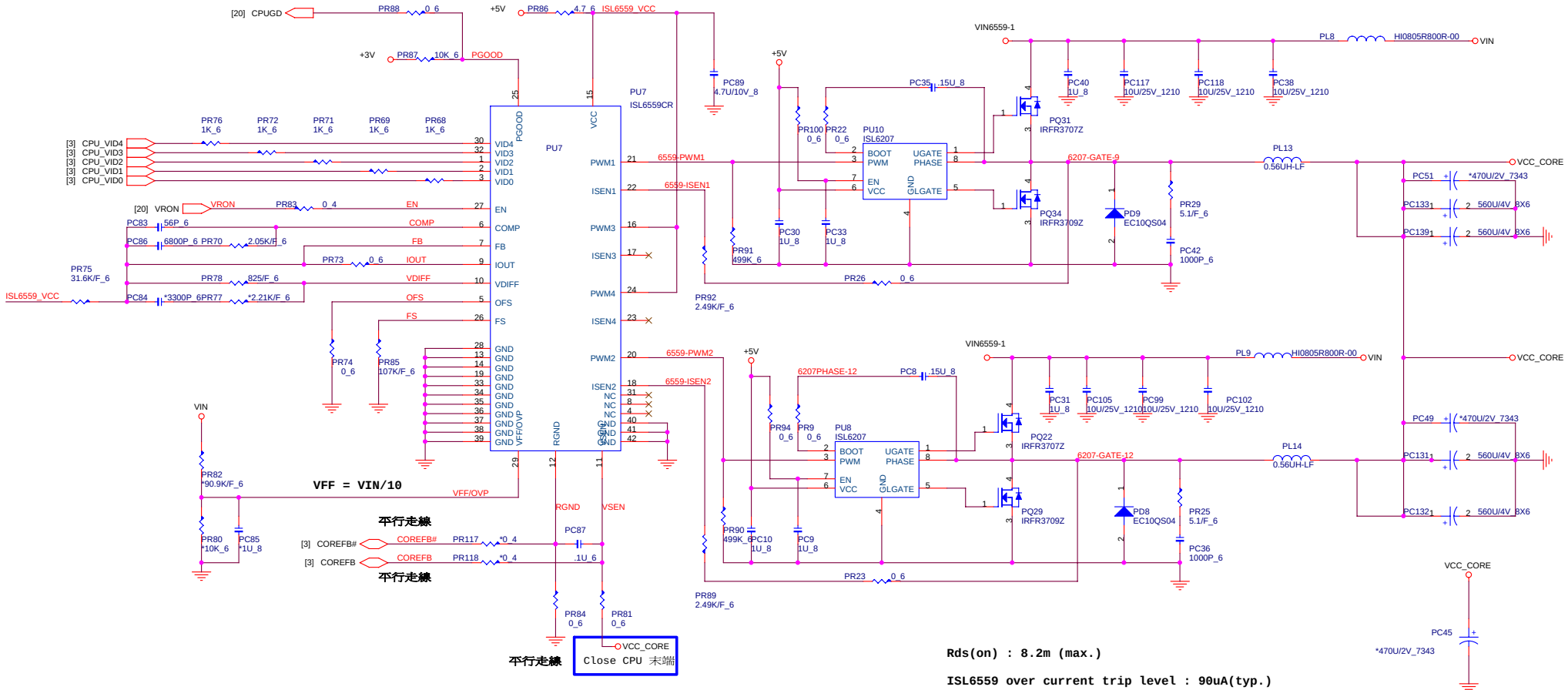
Vcore



Rds(on) : 8.2m (max.)

ISL6559 over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
AMD LPM 35W current 28A

Rds(on) * Io(phase) = Rsen * Isen
8.2m*1.3*(28A/2) = Rsen*60uA
Rsen = 2.48K ~ 2.49K
OCP : 28A*1.5 = 42A

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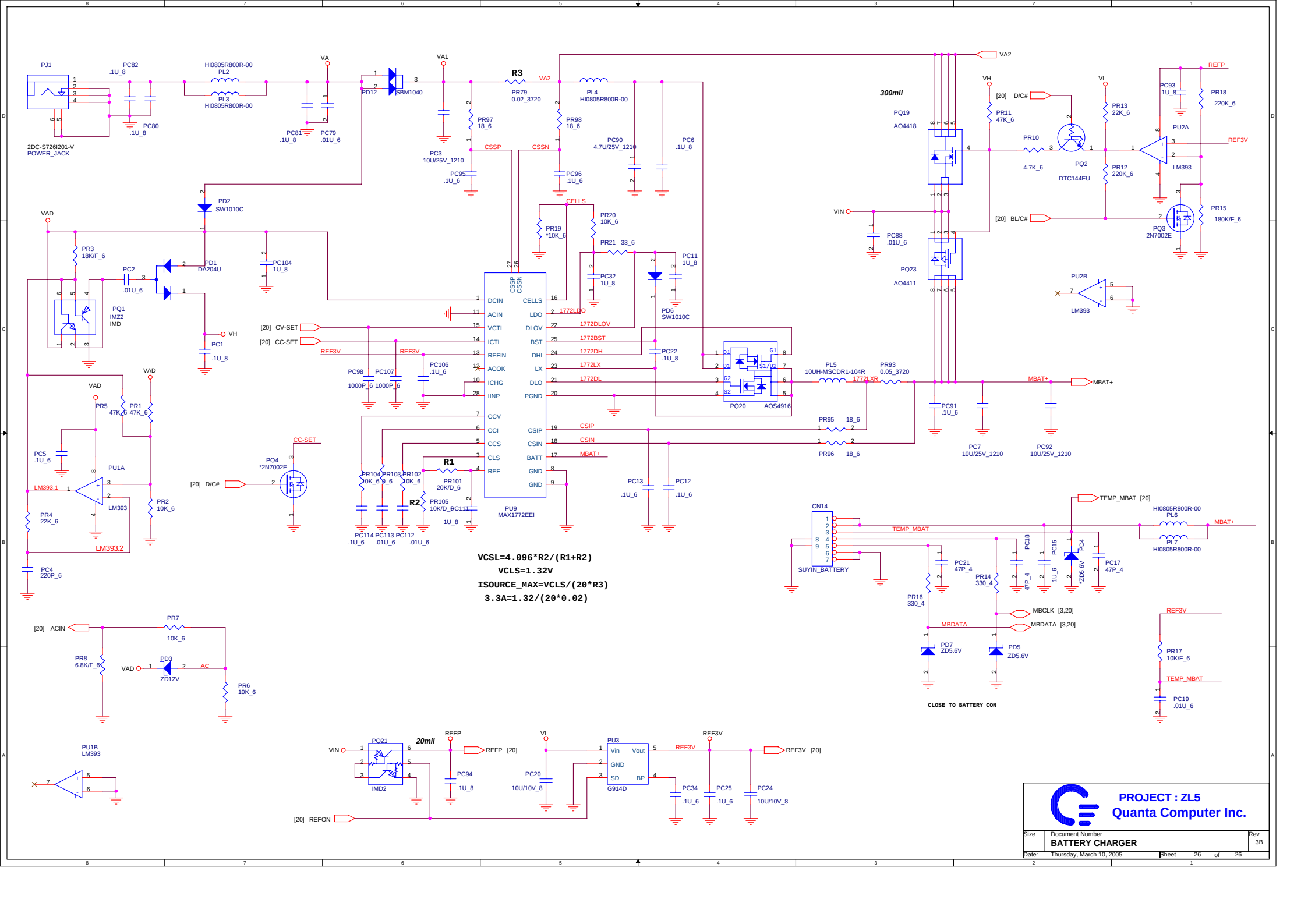

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	BATTERY CHARGER	3B
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