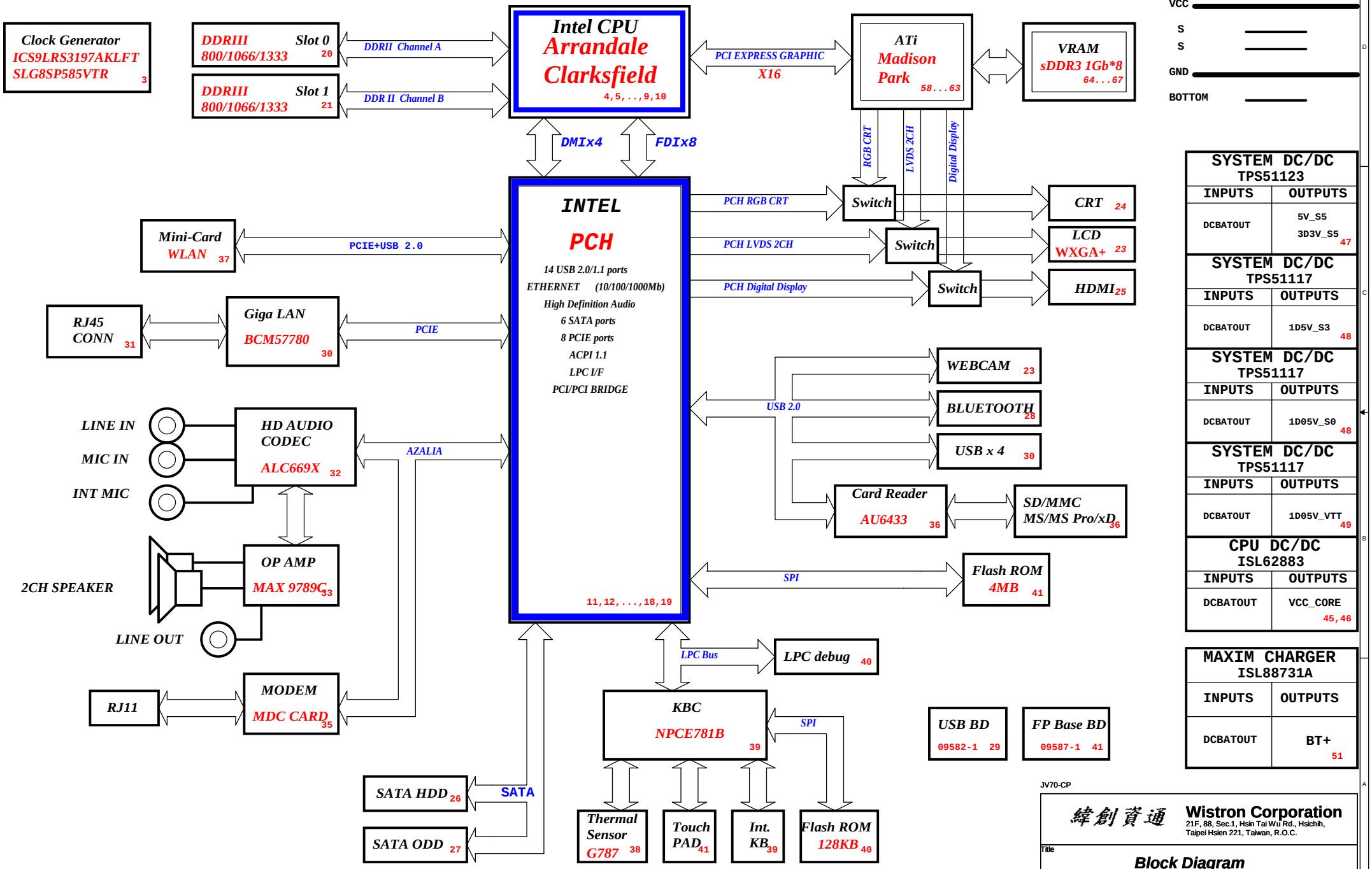
JV70-CP Block Diagram

Project code: 91.4GC01.001
PCB P/N : 48.4GC01.011
REVISION : 09293--1

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM



SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 48

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 49

CPU DC/DC ISL62883	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

MAXIM CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard WLAN

USB

Pair	*Device*
0	*USB1*
1	*USB2*
2	*USB4*
3	*MINICARD1*
4	*WECAM*
5	*NC*
6	*NC*
7	*NC*
8	*NC*
9	*USB3(HS)*
10	*Finger Print*
11	*Blue Tooth*
12	*NC*
13	*Cardreader*

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

JV70-CP

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Title: *Table of Content*

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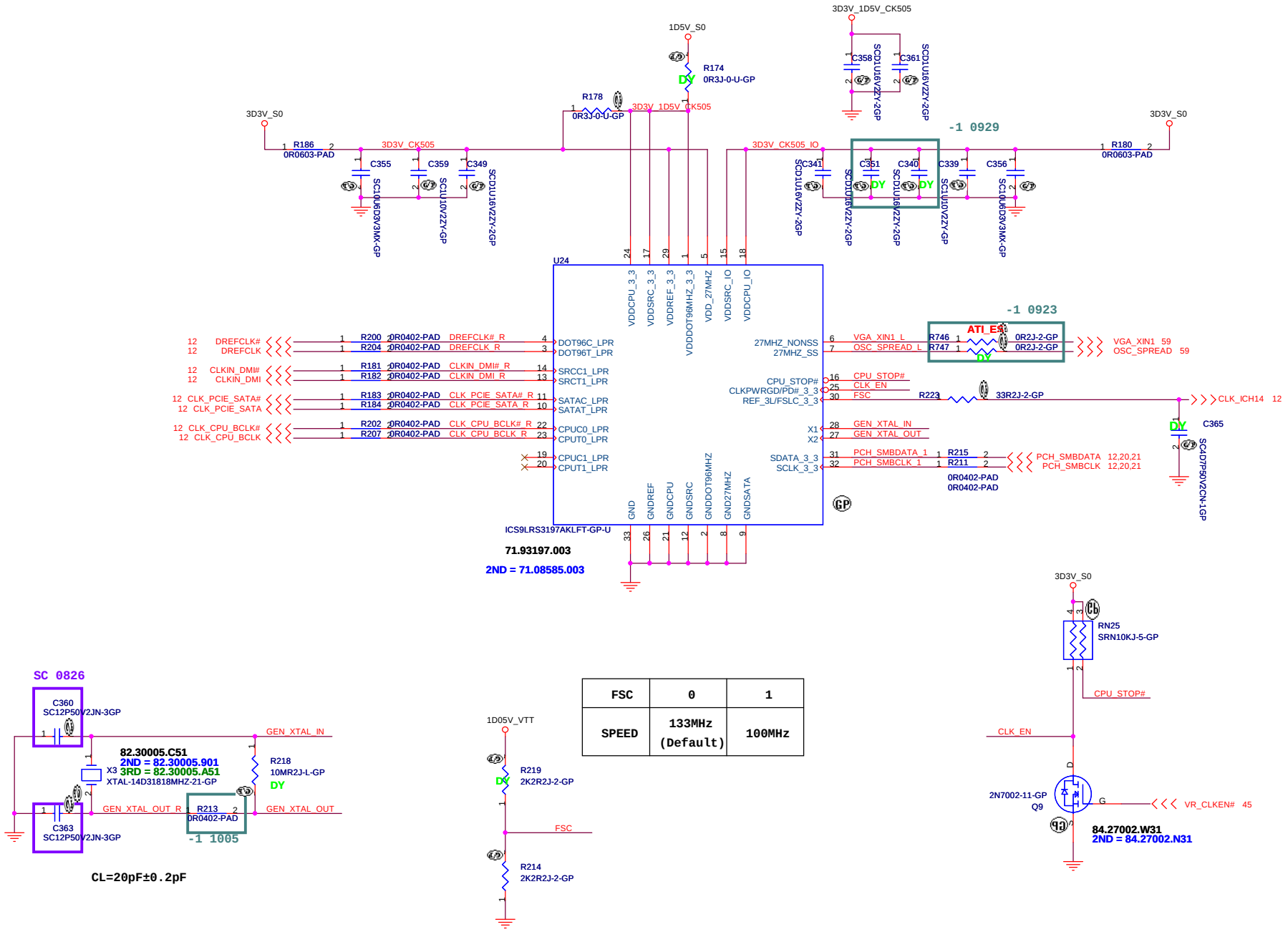

JV70-CP

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Title: Clock Generator

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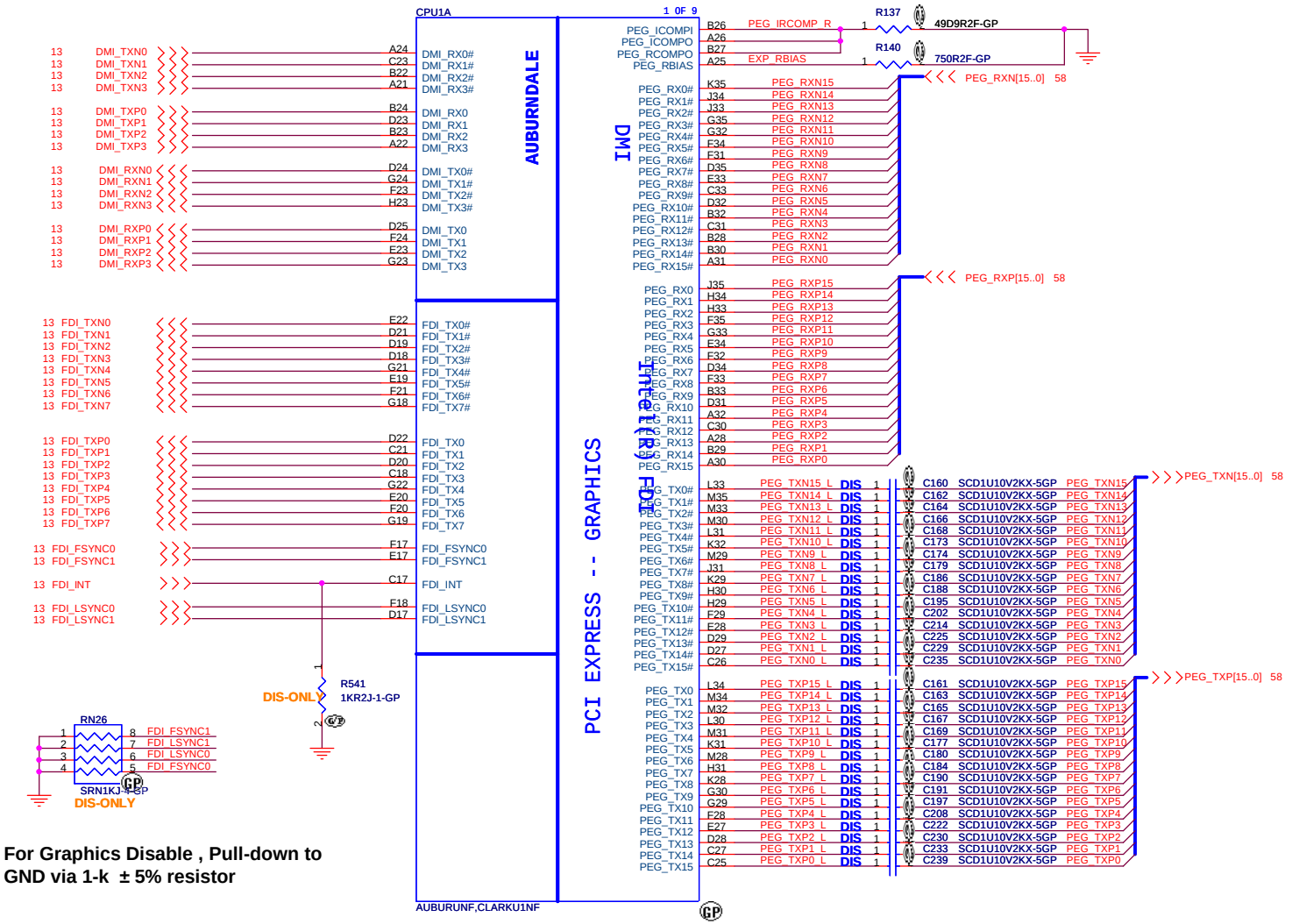

For Graphics Disable , Pull-down to GND via 1-k ± 5% resistor

JV70-CP

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Title	***CPU (1/7)***
Size A3	Document Number **JV70-CP** Rev **-1**
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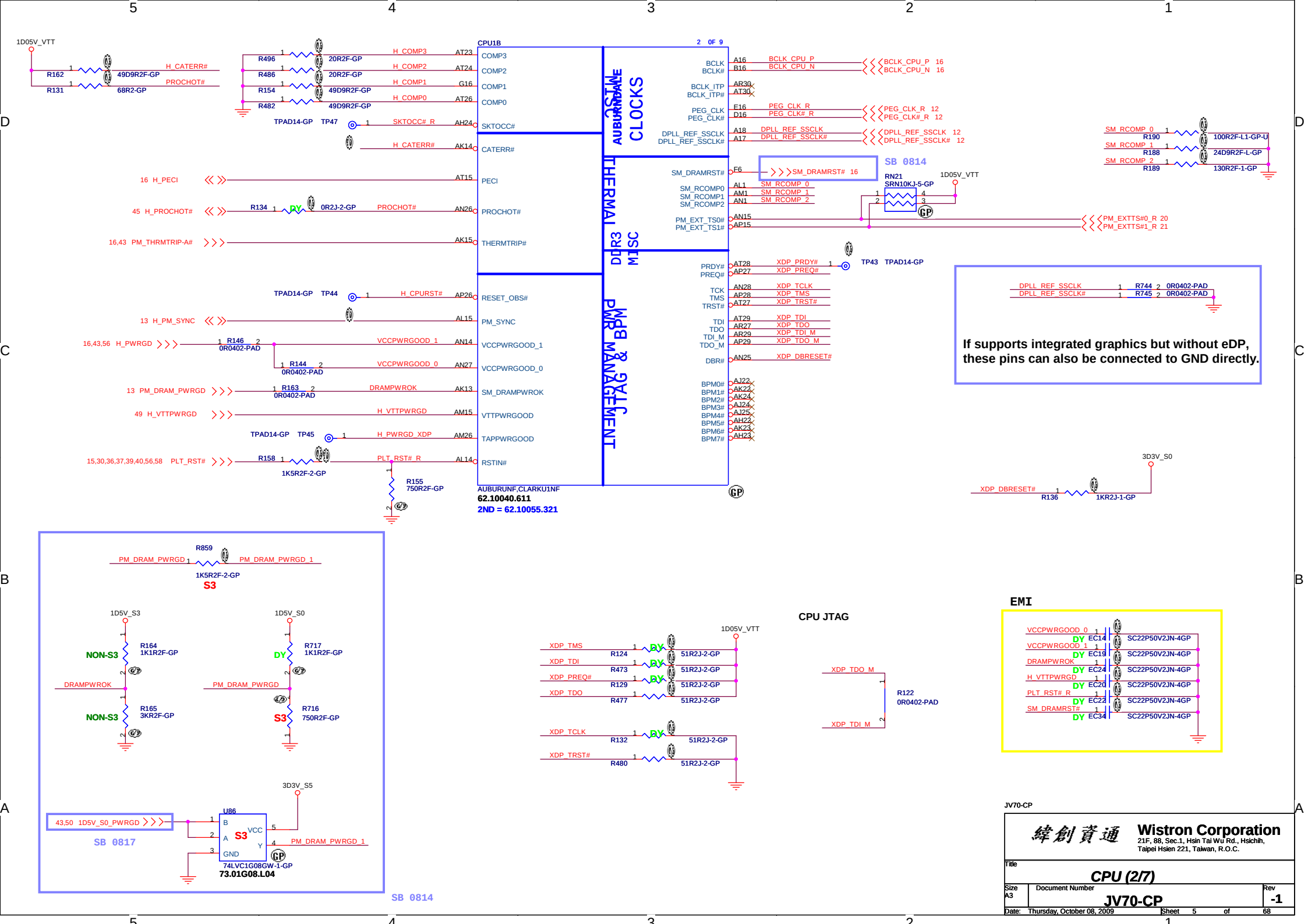

JV70-CP

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Title: CPU (2/7)

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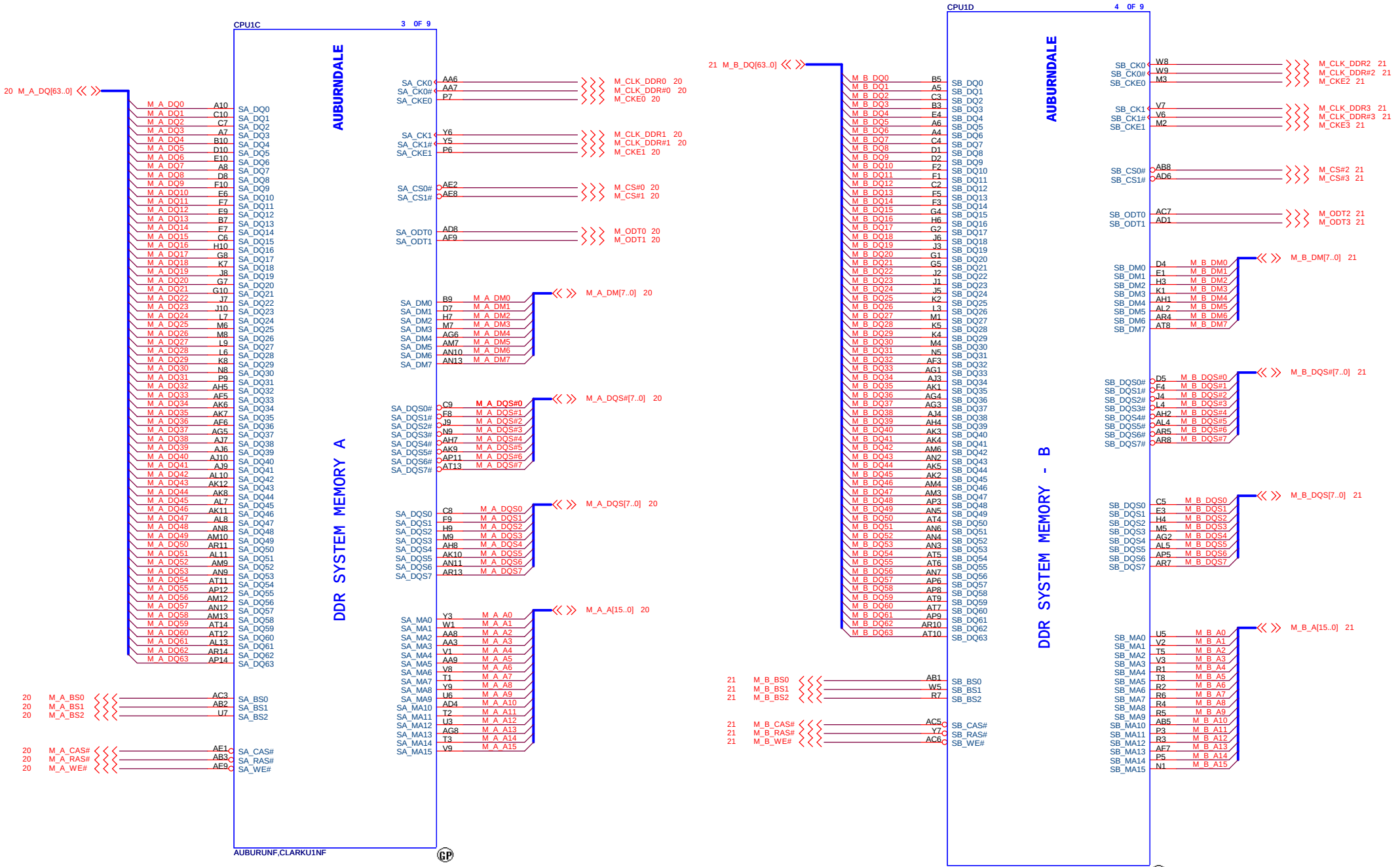
CPU1C
3 0F 9
AUBURNDALE
DDR SYSTEM MEMORY A
20 M_A_DQ[63..0]
M_A_DQ0 A10
M_A_DQ1 C10
M_A_DQ2 C7
M_A_DQ3 A7
M_A_DQ4 B10
M_A_DQ5 D10
M_A_DQ6 E10
M_A_DQ7 A8
M_A_DQ8 D8
M_A_DQ9 F10
M_A_DQ10 E6
M_A_DQ11 F7
M_A_DQ12 E9
M_A_DQ13 B7
M_A_DQ14 E7
M_A_DQ15 C6
M_A_DQ16 H10
M_A_DQ17 G8
M_A_DQ18 K7
M_A_DQ19 J8
M_A_DQ20 G7
M_A_DQ21 G10
M_A_DQ22 J7
M_A_DQ23 J10
M_A_DQ24 L7
M_A_DQ25 M6
M_A_DQ26 M8
M_A_DQ27 L9
M_A_DQ28 L6
M_A_DQ29 K8
M_A_DQ30 N8
M_A_DQ31 P9
M_A_DQ32 AH5
M_A_DQ33 AF5
M_A_DQ34 AK6
M_A_DQ35 AK7
M_A_DQ36 AF6
M_A_DQ37 AG5
M_A_DQ38 AJ7
M_A_DQ39 AJ6
M_A_DQ40 AJ10
M_A_DQ41 AJ9
M_A_DQ42 AL10
M_A_DQ43 AK12
M_A_DQ44 AK8
M_A_DQ45 AL7
M_A_DQ46 AK11
M_A_DQ47 AL8
M_A_DQ48 AN8
M_A_DQ49 AM10
M_A_DQ50 AR11
M_A_DQ51 AL11
M_A_DQ52 AM9
M_A_DQ53 AN9
M_A_DQ54 AT11
M_A_DQ55 AP12
M_A_DQ56 AM12
M_A_DQ57 AN12
M_A_DQ58 AM13
M_A_DQ59 AT14
M_A_DQ60 AT12
M_A_DQ61 AL13
M_A_DQ62 AR14
M_A_DQ63 AP14
SA_DQ0 SA_DQ1 SA_DQ2 SA_DQ3 SA_DQ4 SA_DQ5 SA_DQ6 SA_DQ7 SA_DQ8 SA_DQ9 SA_DQ10 SA_DQ11 SA_DQ12 SA_DQ13 SA_DQ14 SA_DQ15 SA_DQ16 SA_DQ17 SA_DQ18 SA_DQ19 SA_DQ20 SA_DQ21 SA_DQ22 SA_DQ23 SA_DQ24 SA_DQ25 SA_DQ26 SA_DQ27 SA_DQ28 SA_DQ29 SA_DQ30 SA_DQ31 SA_DQ32 SA_DQ33 SA_DQ34 SA_DQ35 SA_DQ36 SA_DQ37 SA_DQ38 SA_DQ39 SA_DQ40 SA_DQ41 SA_DQ42 SA_DQ43 SA_DQ44 SA_DQ45 SA_DQ46 SA_DQ47 SA_DQ48 SA_DQ49 SA_DQ50 SA_DQ51 SA_DQ52 SA_DQ53 SA_DQ54 SA_DQ55 SA_DQ56 SA_DQ57 SA_DQ58 SA_DQ59 SA_DQ60 SA_DQ61 SA_DQ62 SA_DQ63
20 M_A_BS0
20 M_A_BS1
20 M_A_BS2
AC3 AB2 U7
SA_BS0 SA_BS1 SA_BS2
20 M_A_CAS#
20 M_A_RAS#
20 M_A_WE#
AE1 AB3 AE9
SA_CAS# SA_RAS# SA_WE#
SA_CK0 AA6
SA_CK0# AA7
SA_CKE0 P7
M_CLK_DDR0 20
M_CLK_DDR#0 20
M_CKE0 20
SA_CK1 Y6
SA_CK1# Y5
SA_CKE1 P6
M_CLK_DDR1 20
M_CLK_DDR#1 20
M_CKE1 20
SA_CS0# AE2
SA_CS1# AE8
M_CS#0 20
M_CS#1 20
SA_ODT0 AD8
SA_ODT1 AF9
M_ODT0 20
M_ODT1 20
SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7
M_A_DM[7..0] 20
SA_DQS0# C9 M_A_DQS#0
SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7
M_A_DQS#[7..0] 20
SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7
M_A_DQS[7..0] 20
SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
AUBURUNF,CLARKU1NF
62.10040.611
2ND = 62.10055.321
CPU1D
4 0F 9
AUBURNDALE
DDR SYSTEM MEMORY - B
21 M_B_DQ[63..0]
M_B_DQ0 B5
M_B_DQ1 A5
M_B_DQ2 C3
M_B_DQ3 B3
M_B_DQ4 E4
M_B_DQ5 A6
M_B_DQ6 A4
M_B_DQ7 C4
M_B_DQ8 D1
M_B_DQ9 D2
M_B_DQ10 F2
M_B_DQ11 F1
M_B_DQ12 C2
M_B_DQ13 E5
M_B_DQ14 F3
M_B_DQ15 G4
M_B_DQ16 H6
M_B_DQ17 G2
M_B_DQ18 J6
M_B_DQ19 J3
M_B_DQ20 G1
M_B_DQ21 G5
M_B_DQ22 J2
M_B_DQ23 J1
M_B_DQ24 J5
M_B_DQ25 K2
M_B_DQ26 L3
M_B_DQ27 M1
M_B_DQ28 K5
M_B_DQ29 K4
M_B_DQ30 M4
M_B_DQ31 N5
M_B_DQ32 AF3
M_B_DQ33 AG1
M_B_DQ34 AJ3
M_B_DQ35 AK1
M_B_DQ36 AG4
M_B_DQ37 AG3
M_B_DQ38 AJ4
M_B_DQ39 AH4
M_B_DQ40 AK3
M_B_DQ41 AK4
M_B_DQ42 AM6
M_B_DQ43 AN2
M_B_DQ44 AK5
M_B_DQ45 AK2
M_B_DQ46 AM4
M_B_DQ47 AM3
M_B_DQ48 AP3
M_B_DQ49 AN5
M_B_DQ50 AT4
M_B_DQ51 AN6
M_B_DQ52 AN4
M_B_DQ53 AN3
M_B_DQ54 AT5
M_B_DQ55 AT6
M_B_DQ56 AN7
M_B_DQ57 AP6
M_B_DQ58 AP8
M_B_DQ59 AT9
M_B_DQ60 AT7
M_B_DQ61 AP9
M_B_DQ62 AR10
M_B_DQ63 AT10
SB_DQ0 SB_DQ1 SB_DQ2 SB_DQ3 SB_DQ4 SB_DQ5 SB_DQ6 SB_DQ7 SB_DQ8 SB_DQ9 SB_DQ10 SB_DQ11 SB_DQ12 SB_DQ13 SB_DQ14 SB_DQ15 SB_DQ16 SB_DQ17 SB_DQ18 SB_DQ19 SB_DQ20 SB_DQ21 SB_DQ22 SB_DQ23 SB_DQ24 SB_DQ25 SB_DQ26 SB_DQ27 SB_DQ28 SB_DQ29 SB_DQ30 SB_DQ31 SB_DQ32 SB_DQ33 SB_DQ34 SB_DQ35 SB_DQ36 SB_DQ37 SB_DQ38 SB_DQ39 SB_DQ40 SB_DQ41 SB_DQ42 SB_DQ43 SB_DQ44 SB_DQ45 SB_DQ46 SB_DQ47 SB_DQ48 SB_DQ49 SB_DQ50 SB_DQ51 SB_DQ52 SB_DQ53 SB_DQ54 SB_DQ55 SB_DQ56 SB_DQ57 SB_DQ58 SB_DQ59 SB_DQ60 SB_DQ61 SB_DQ62 SB_DQ63
21 M_B_BS0
21 M_B_BS1
21 M_B_BS2
AB1 W5 R7
SB_BS0 SB_BS1 SB_BS2
21 M_B_CAS#
21 M_B_RAS#
21 M_B_WE#
AC5 Y7 AC6
SB_CAS# SB_RAS# SB_WE#
SB_CK0 W8
SB_CK0# W9
SB_CKE0 M3
M_CLK_DDR2 21
M_CLK_DDR#2 21
M_CKE2 21
SB_CK1 V7
SB_CK1# V6
SB_CKE1 M2
M_CLK_DDR3 21
M_CLK_DDR#3 21
M_CKE3 21
SB_CS0# AB8
SB_CS1# AD6
M_CS#2 21
M_CS#3 21
SB_ODT0 AC7
SB_ODT1 AD1
M_ODT2 21
M_ODT3 21
SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7
M_B_DM[7..0] 21
SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
AUBURUNF,CLARKU1NF
62.10040.611
2ND = 62.10055.321
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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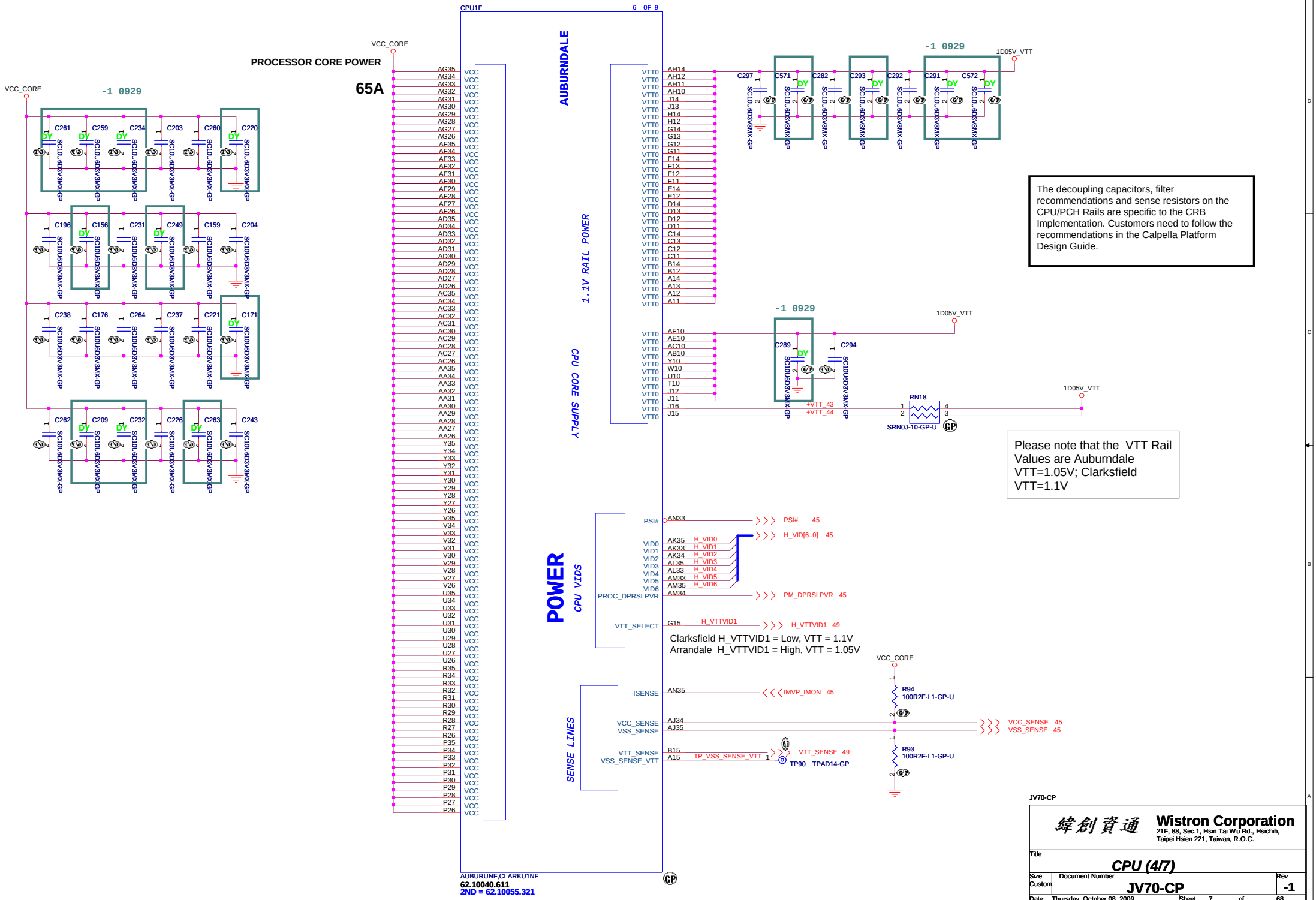

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

JV70-CP

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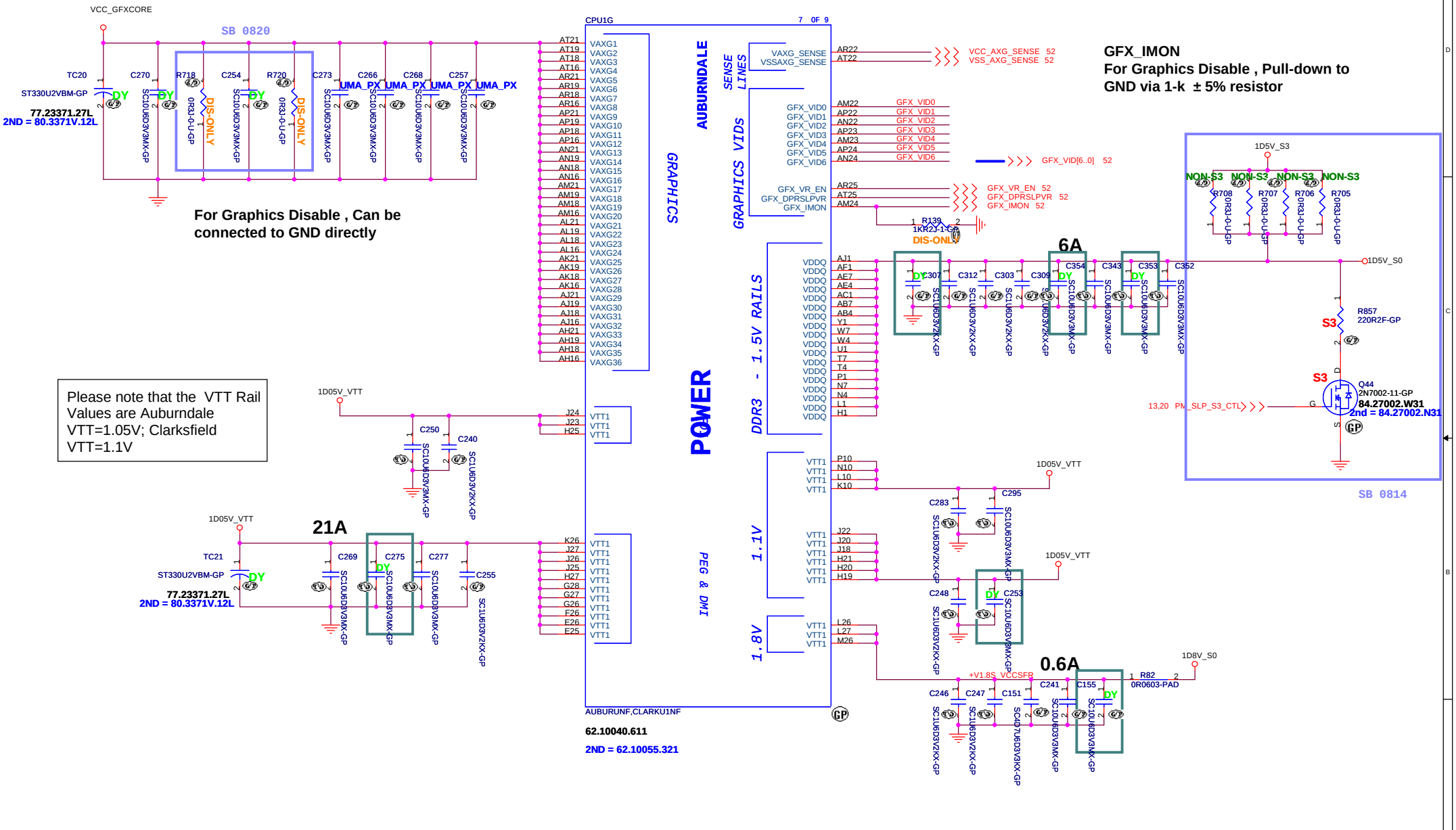
VCC_GFXCORE
SB 0820
TC20
ST330U2VBM-GP
77.23371.27L
2ND = 80.3371V.12L
R718
R720
DIS-ONLY
UMA_PX
For Graphics Disable , Can be connected to GND directly
CPU1G
AUBURNDALE
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
PEG & DMI
POWER
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 52
VSS_AXG_SENSE 52
GFX_VID[6..0] 52
GFX_VR_EN 52
GFX_DPRSLPVR 52
GFX_IMON 52
GFX_IMON
For Graphics Disable , Pull-down to GND via 1-k ± 5% resistor
R139
1KR2J-1-GP
DIS-ONLY
6A
0.6A
21A
1D05V_S3
1D05V_S0
1D05V_VTT
1D8V_S0
R857
220R2F-GP
Q44
2N7002-11-GP
84.27002.W31
2nd = 84.27002.N31
13,20 PM_SLP_S3_CTL
SB 0814
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
AUBURUNF,CLARKU1NF
62.10040.611
2ND = 62.10055.321
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (5/7)
Size A3
Document Number JV70-CP
Rev -1
Date: Thursday, October 08, 2009
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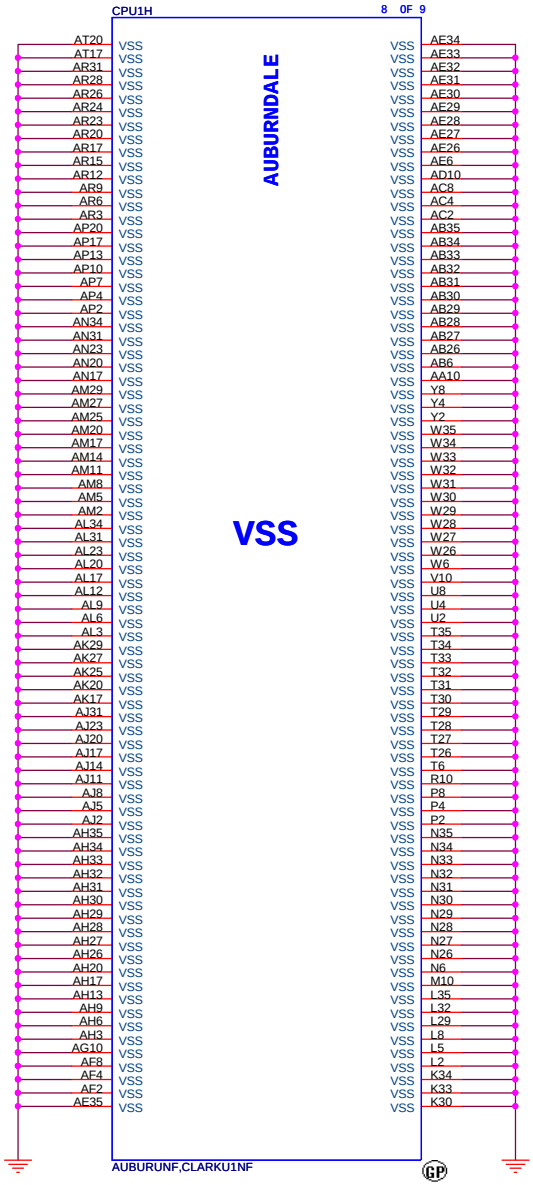
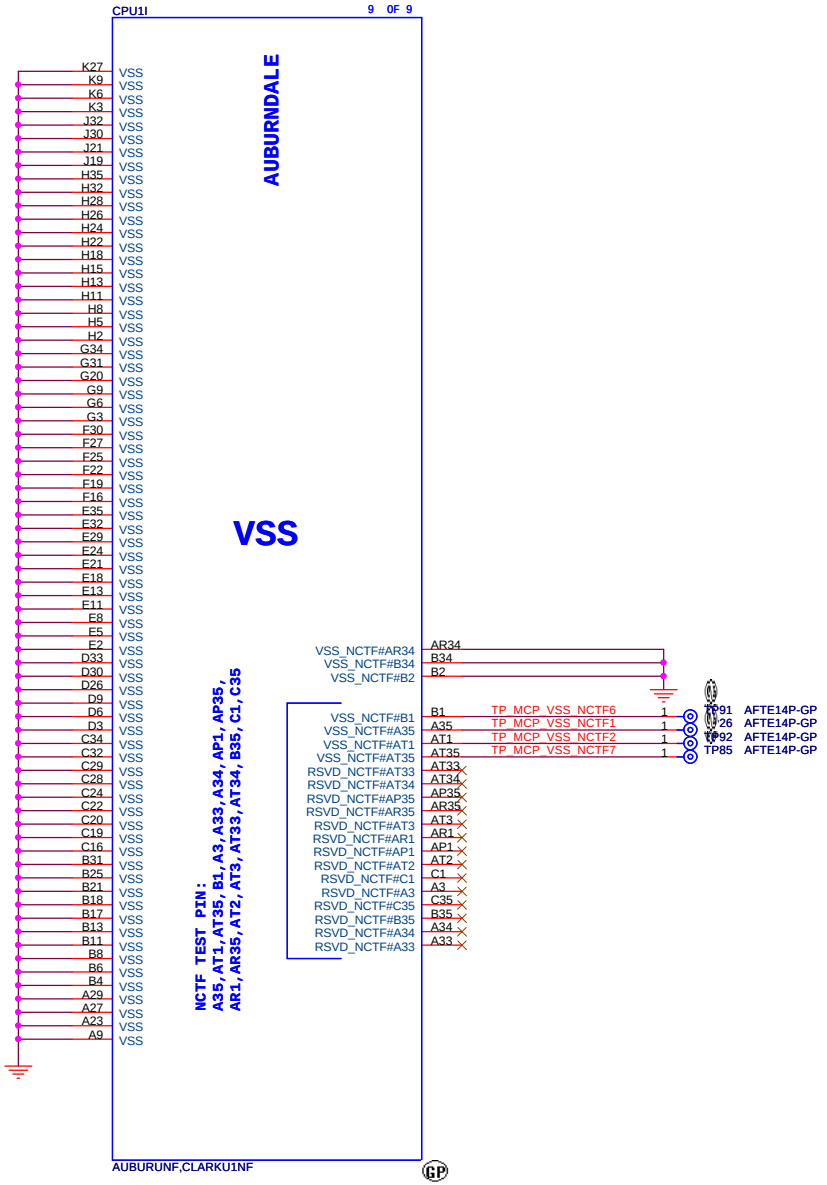


62.10040.611

2ND = 62.10055.321



62.10040.611

2ND = 62.10055.321

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Title: CPU (6/7)

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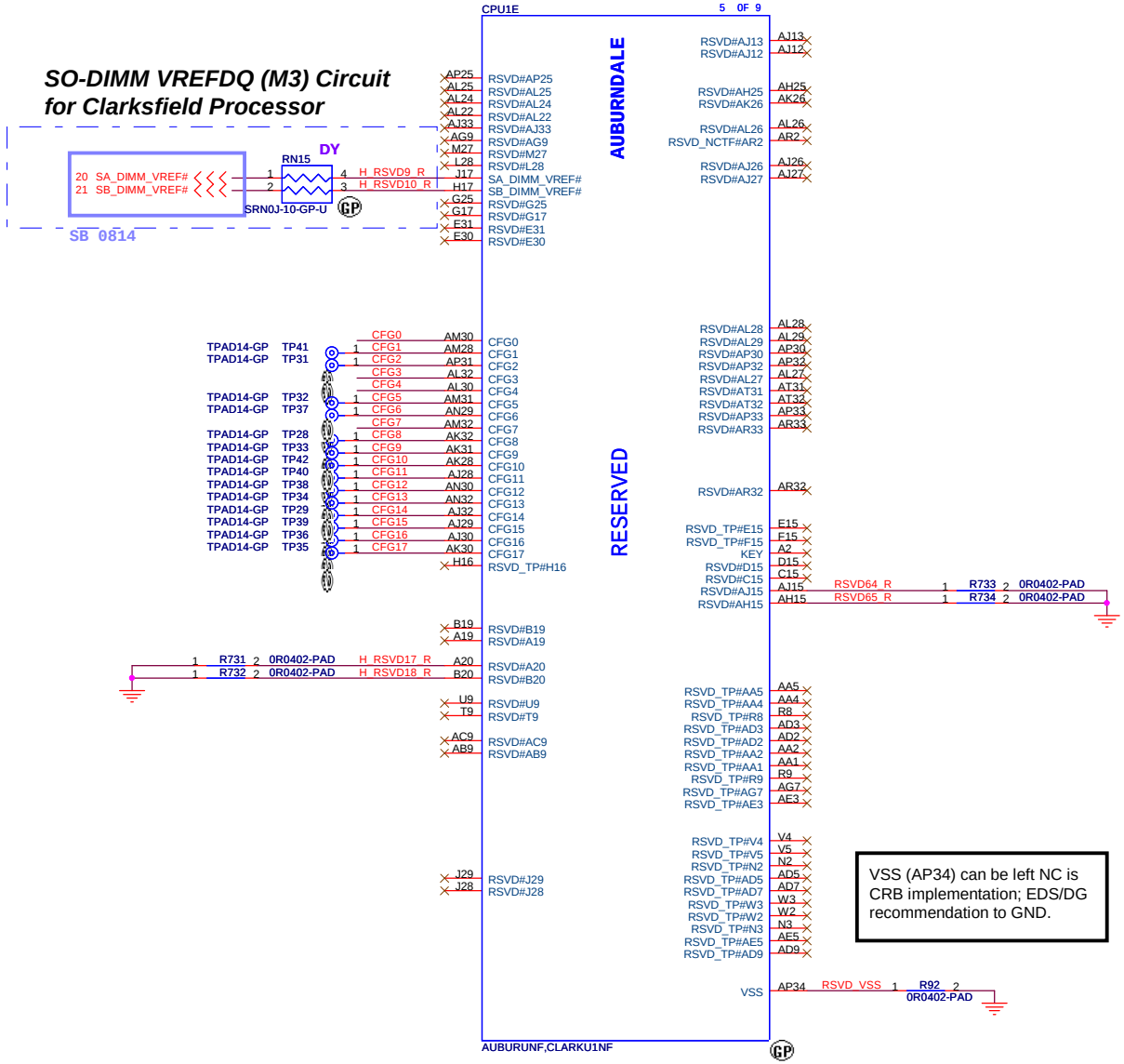
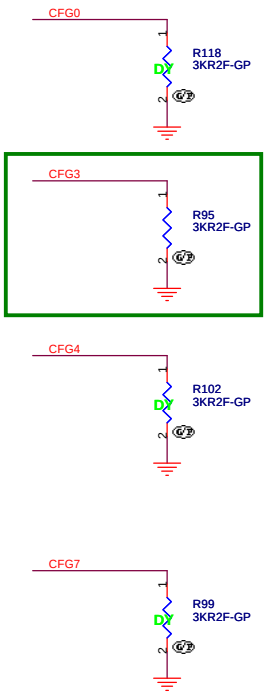
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



62.10040.611 **BOM change to 62.10055.321**

2ND = 62.10053.561

3RD = 62.10055.341



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

JV70-CP

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Title: **CPU (7/7)**

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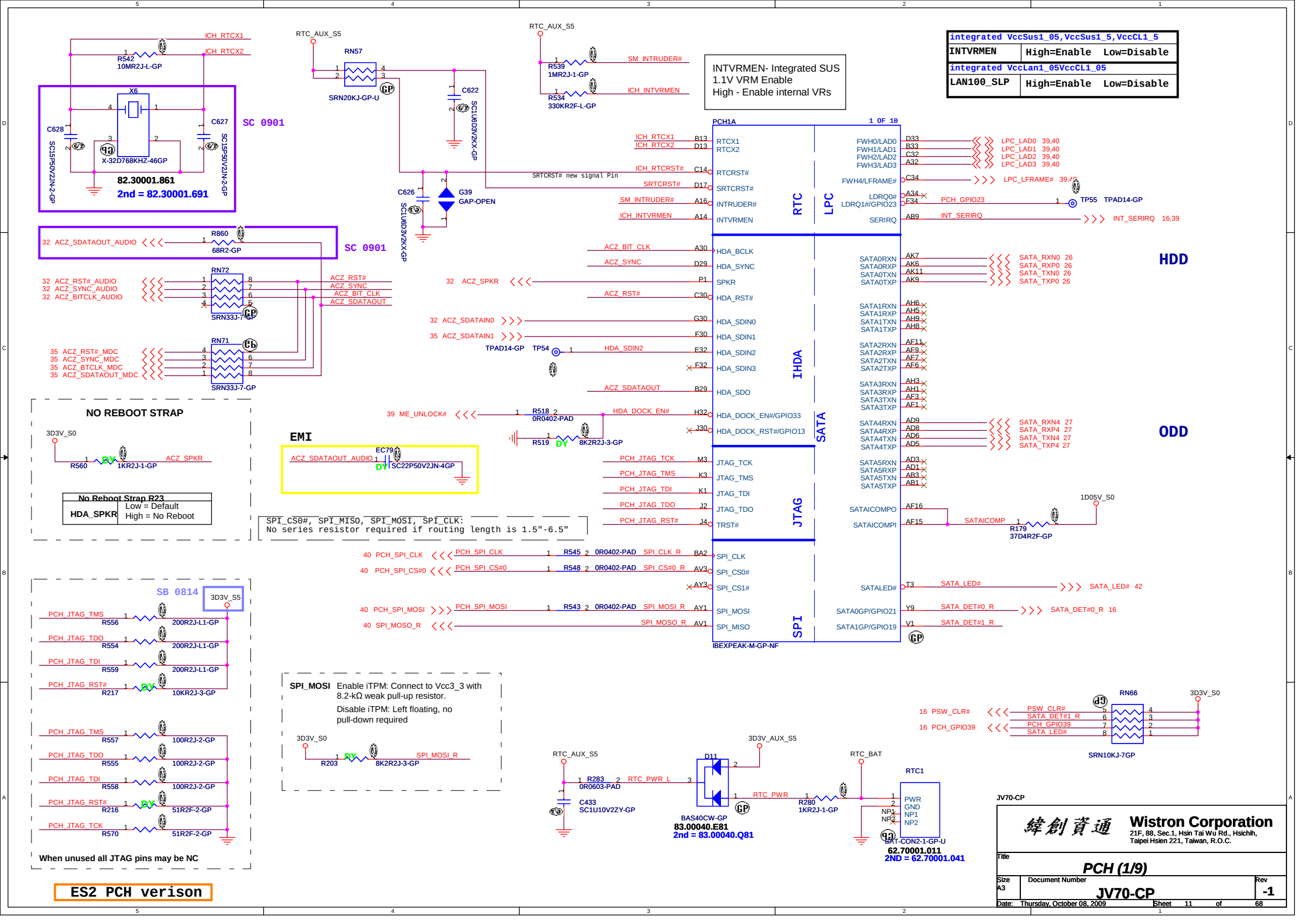
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
ODD
SC 0901
82.30001.861
2nd = 82.30001.691
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
EMI
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
SB 0814
When unused all JTAG pins may be NC
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
SRTCRST# new signal Pin
IBEXPEAK-M-GP-NF
83.00040.E81
2nd = 83.00040.Q81
62.70001.011
2ND = 62.70001.041
ES2 PCH verison
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (1/9)
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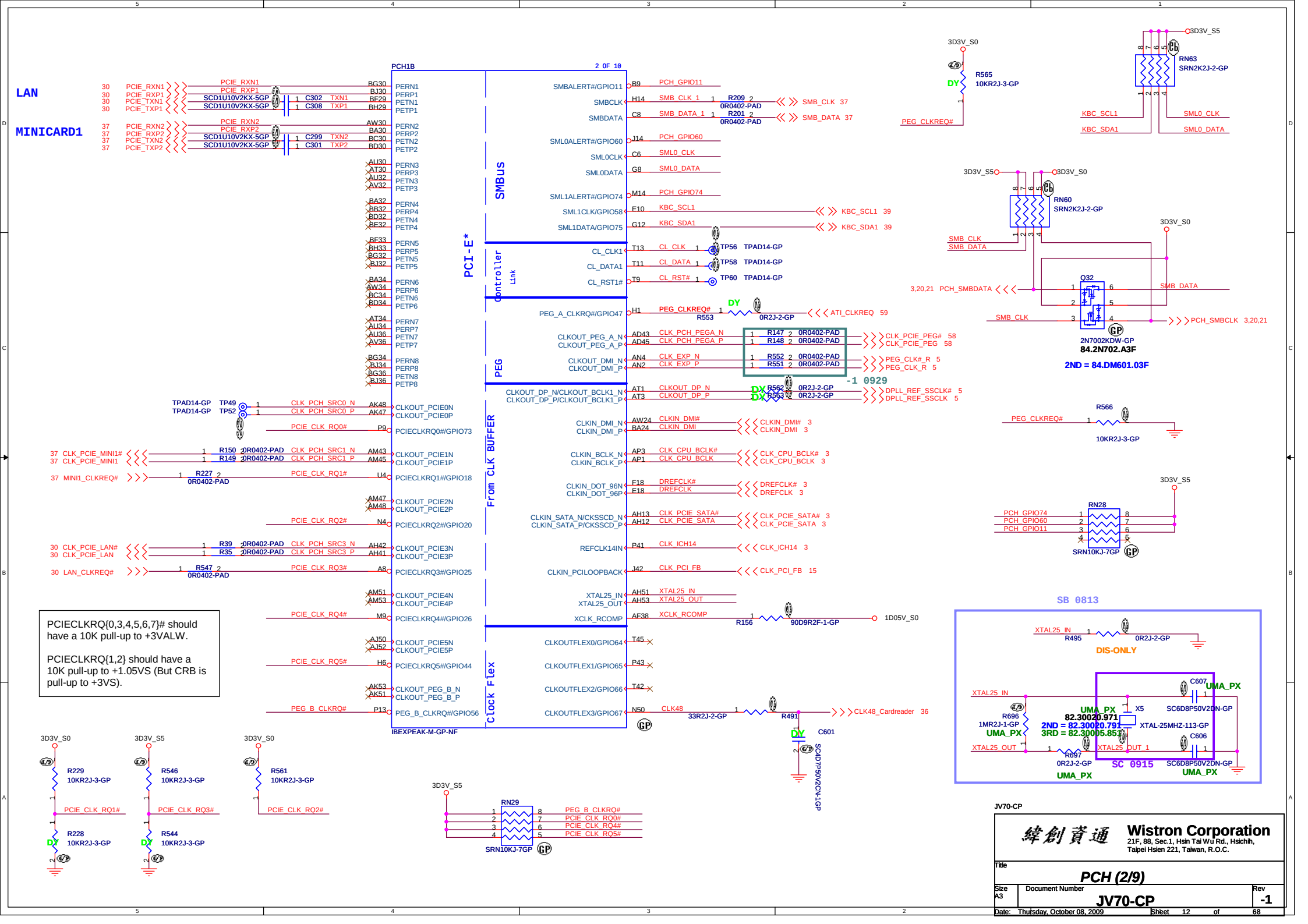
LAN
MINICARD1
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SB 0813
DIS-ONLY
SC 0915
JV70-CP
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
PCH (2/9)
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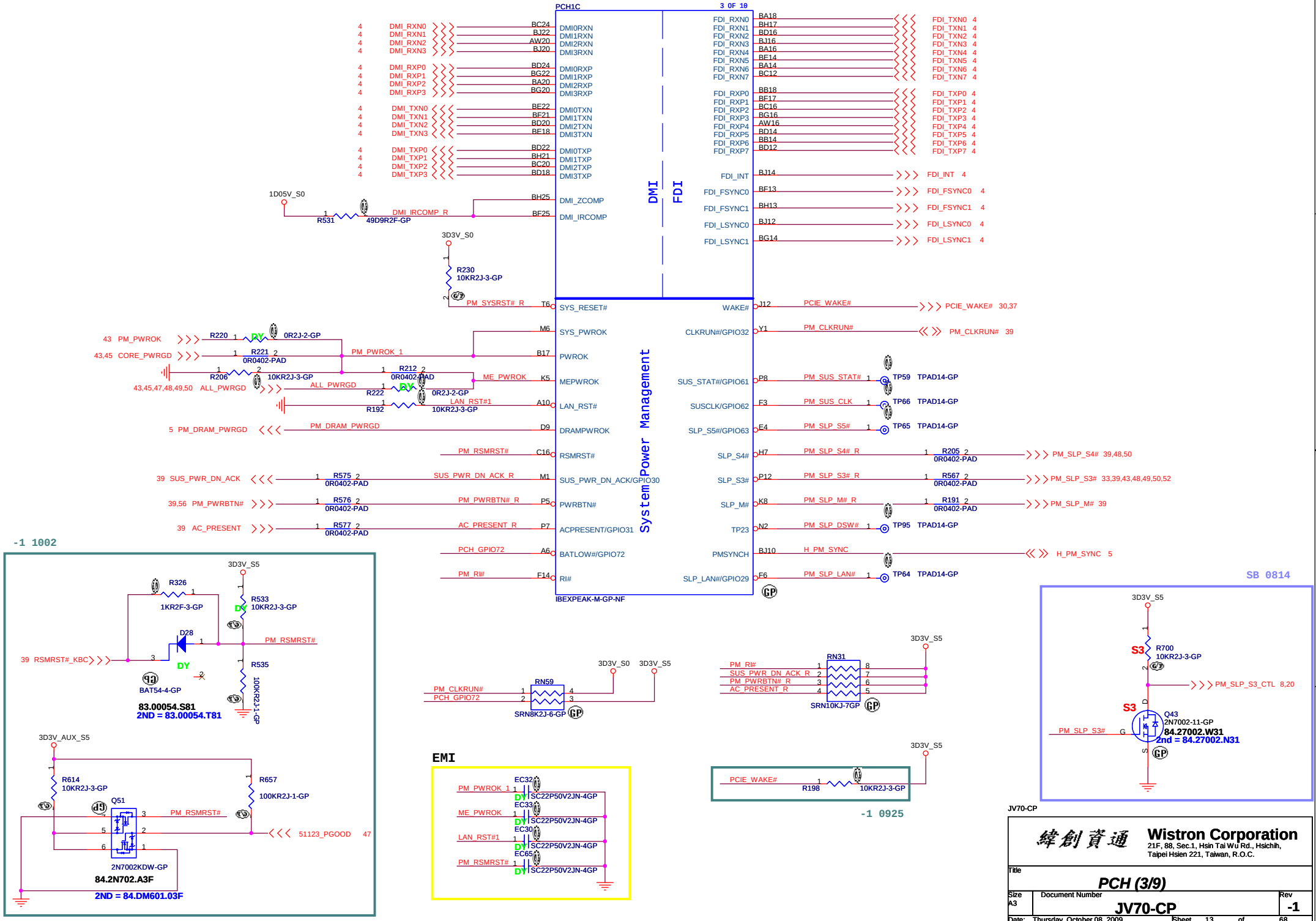

JV70-CP

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Title	PCH (3/9)	
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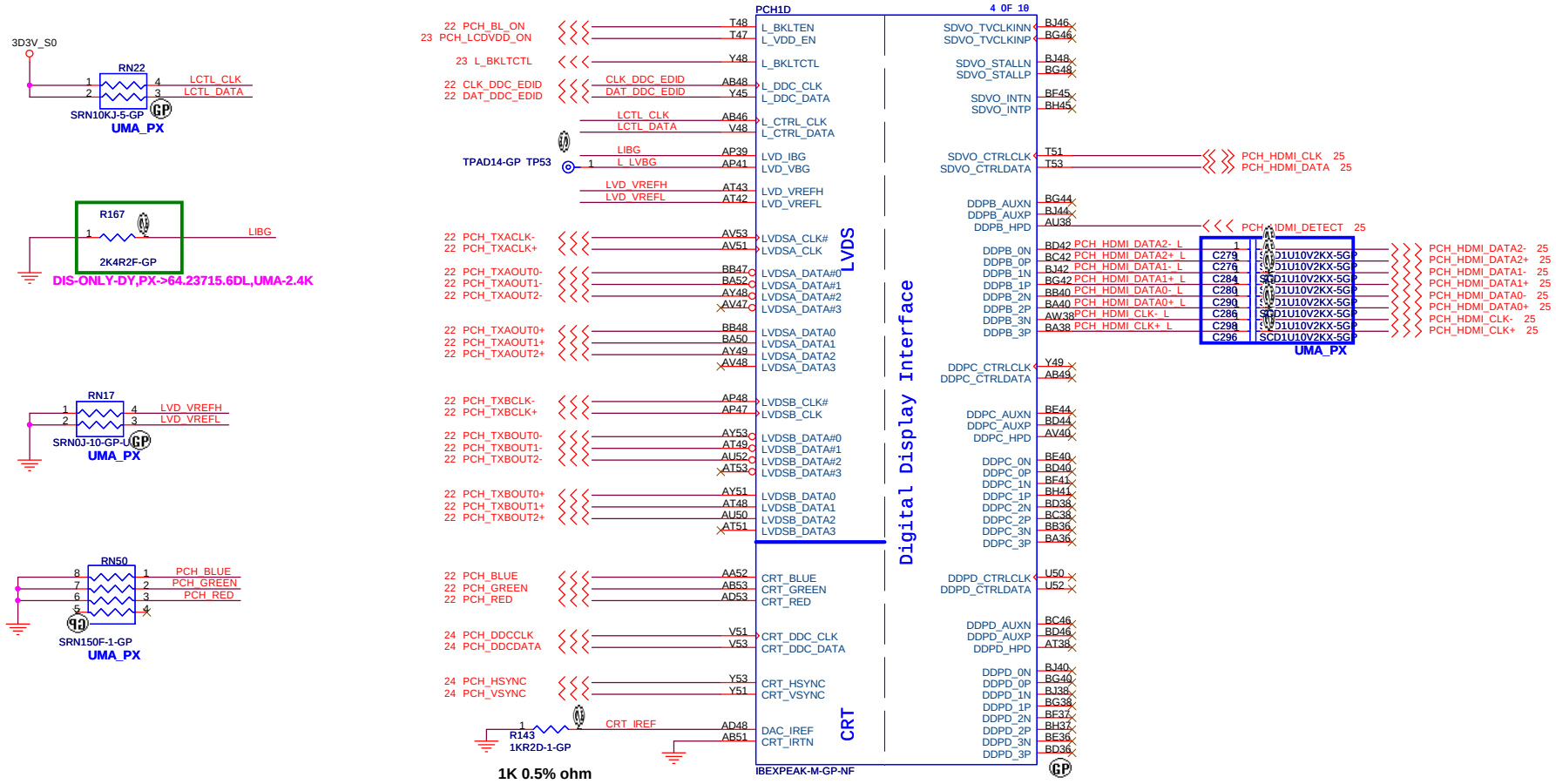

JV70-CP

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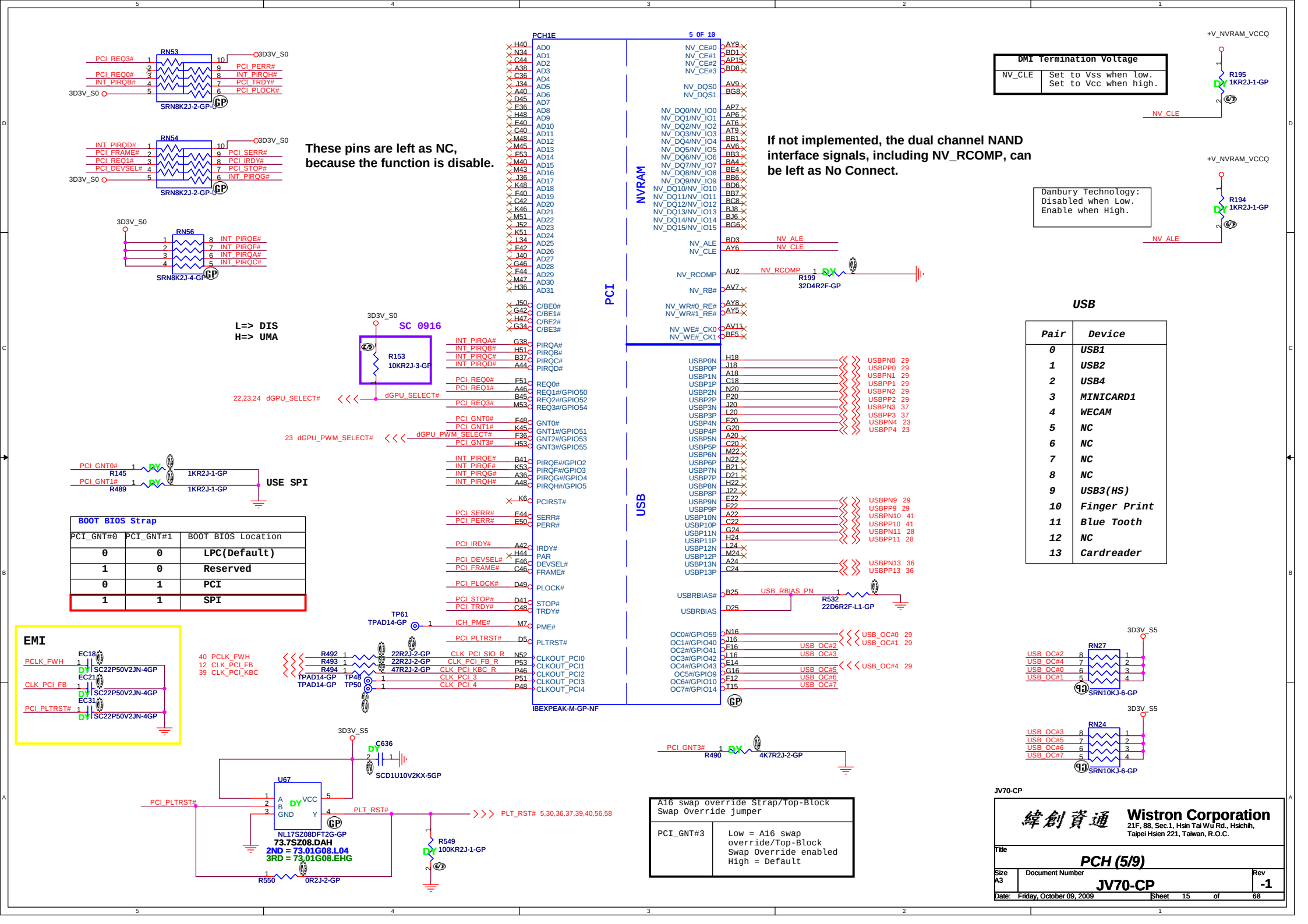
RN53
PCI_REQ3#
PCI_REQ0#
INT_PIRQB#
3D3V_S0
PCI_PERR#
INT_PIRQH#
PCI_TRDY#
PCI_PLOCK#
SRN8K2J-2-GP-U
RN54
INT_PIRQD#
PCI_FRAME#
PCI_REQ1#
PCI_DEVSEL#
PCI_SERR#
PCI_IRDY#
PCI_STOP#
INT_PIRQG#
SRN8K2J-2-GP-U
RN56
INT_PIRQE#
INT_PIRQF#
INT_PIRQA#
INT_PIRQC#
SRN8K2J-4-GP
These pins are left as NC, because the function is disable.
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.
DMI Termination Voltage
NV_CLE
Set to Vss when low.
Set to Vcc when high.
+V_NVRAM_VCCQ
R195
1KR2J-1-GP
NV_CLE
Danbury Technology:
Disabled when Low.
Enable when High.
R194
1KR2J-1-GP
NV_ALE
L=> DIS
H=> UMA
SC 0916
R153
10KR2J-3-GP
22,23,24 dGPU_SELECT#
23 dGPU_PWM_SELECT#
PCH1E
IBEXPEAK-M-GP-NF
PCI
NVRAM
USB
5 OF 10
NV_RCOMP
R199
32D4R2F-GP
USB
Pair
Device
0 USB1
1 USB2
2 USB4
3 MINICARD1
4 WECAM
5 NC
6 NC
7 NC
8 NC
9 USB3(HS)
10 Finger Print
11 Blue Tooth
12 NC
13 Cardreader
PCI_GNT0#
PCI_GNT1#
R145
R489
1KR2J-1-GP
USE SPI
BOOT BIOS Strap
PCI_GNT#0
PCI_GNT#1
BOOT BIOS Location
0 0 LPC(Default)
1 0 Reserved
0 1 PCI
1 1 SPI
EMI
PCLK_FWH
CLK_PCI_FB
PCI_PLTRST#
SC22P50V2JN-4GP
40 PCLK_FWH
12 CLK_PCI_FB
39 CLK_PCI_KBC
TP61
TPAD14-GP
R492
R493
R494
22R2J-2-GP
47R2J-2-GP
TP48
TP50
CLK_PCI_SIO_R
CLK_PCI_FB_R
CLK_PCI_KBC_R
CLK_PCI_3
CLK_PCI_4
USB_RBIAS_PN
R532
22D6R2F-L1-GP
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
RN27
RN24
SRN10KJ-6-GP
3D3V_S5
C636
SCD1U10V2KX-5GP
U67
NL17SZ08DFT2G-GP
73.7SZ08.DAH
2ND = 73.01G08.L04
3RD = 73.01G08.EHG
PLT_RST#
PLT_RST# 5,30,36,37,39,40,56,58
R549
100KR2J-1-GP
R550
0R2J-2-GP
PCI_GNT3#
R490
4K7R2J-2-GP
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (5/9)
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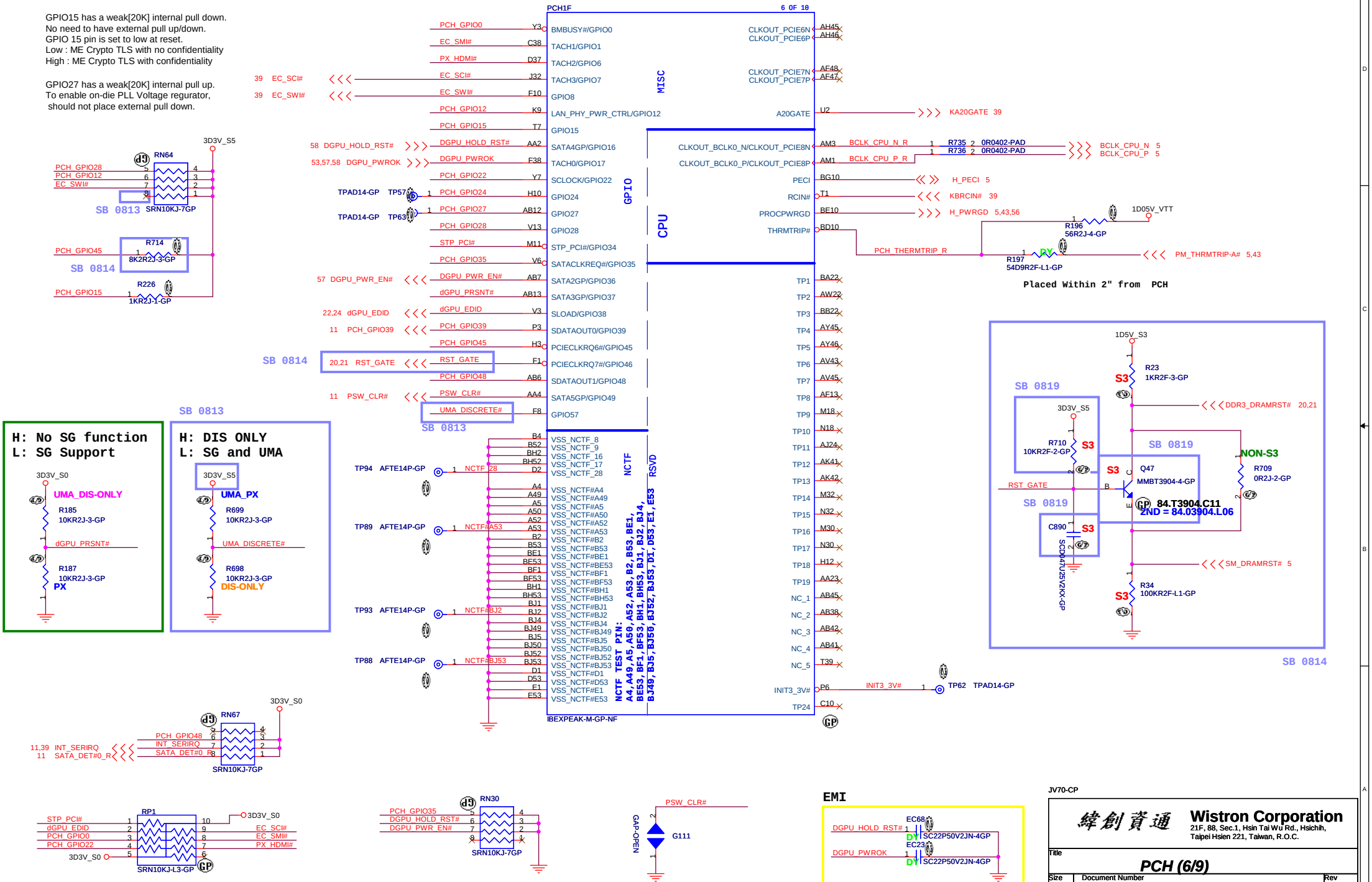
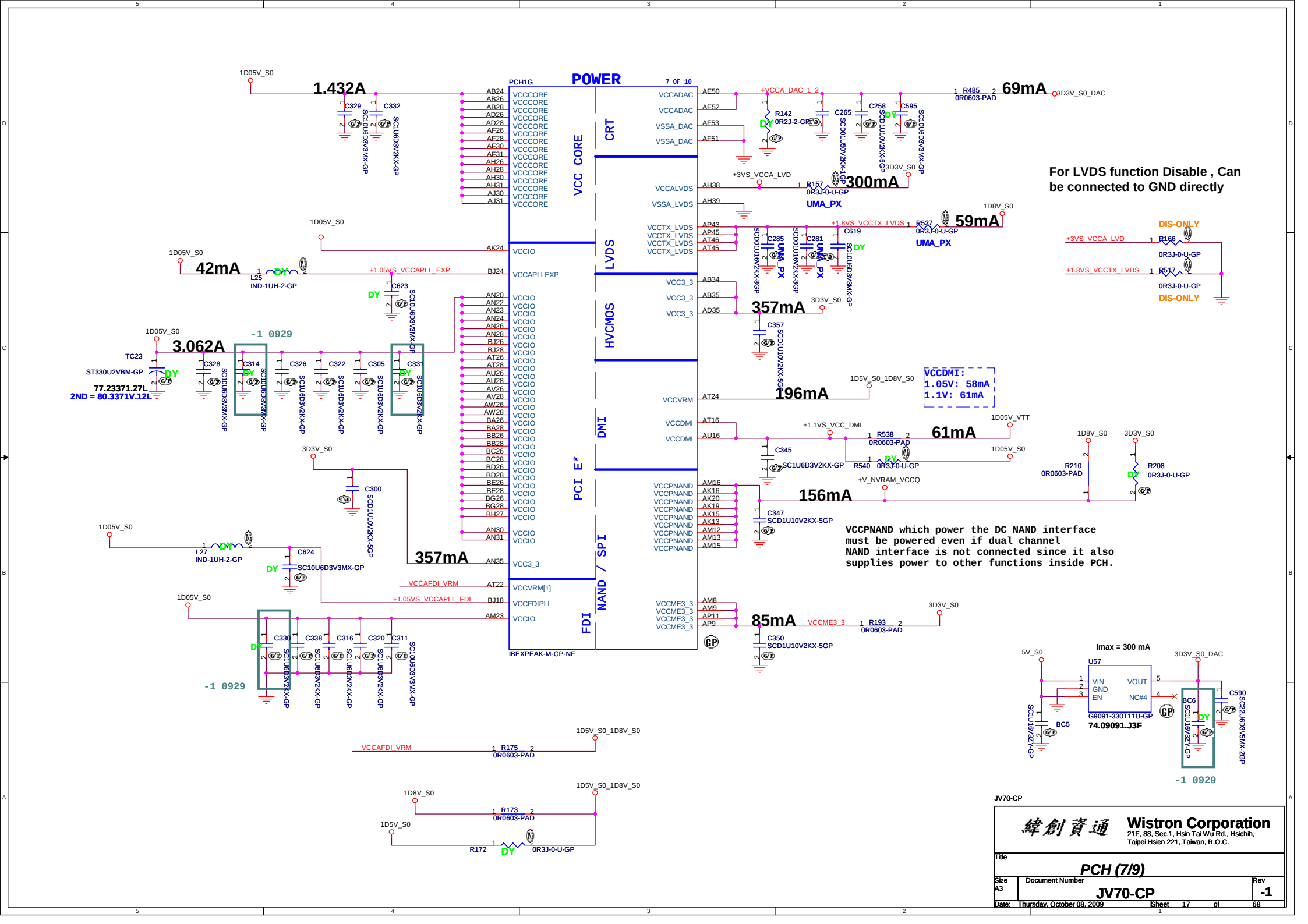
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.




POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
IBEXPEAK-M-GP-NF
1.432A
42mA
3.062A
357mA
69mA
300mA
59mA
357mA
196mA
61mA
156mA
85mA
For LVDS function Disable , Can be connected to GND directly
VCCDMI:
1.05V: 58mA
1.1V: 61mA
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
Imax = 300 mA
U57
G9091-330T11U-GP
74.09091.J3F
-1 0929
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
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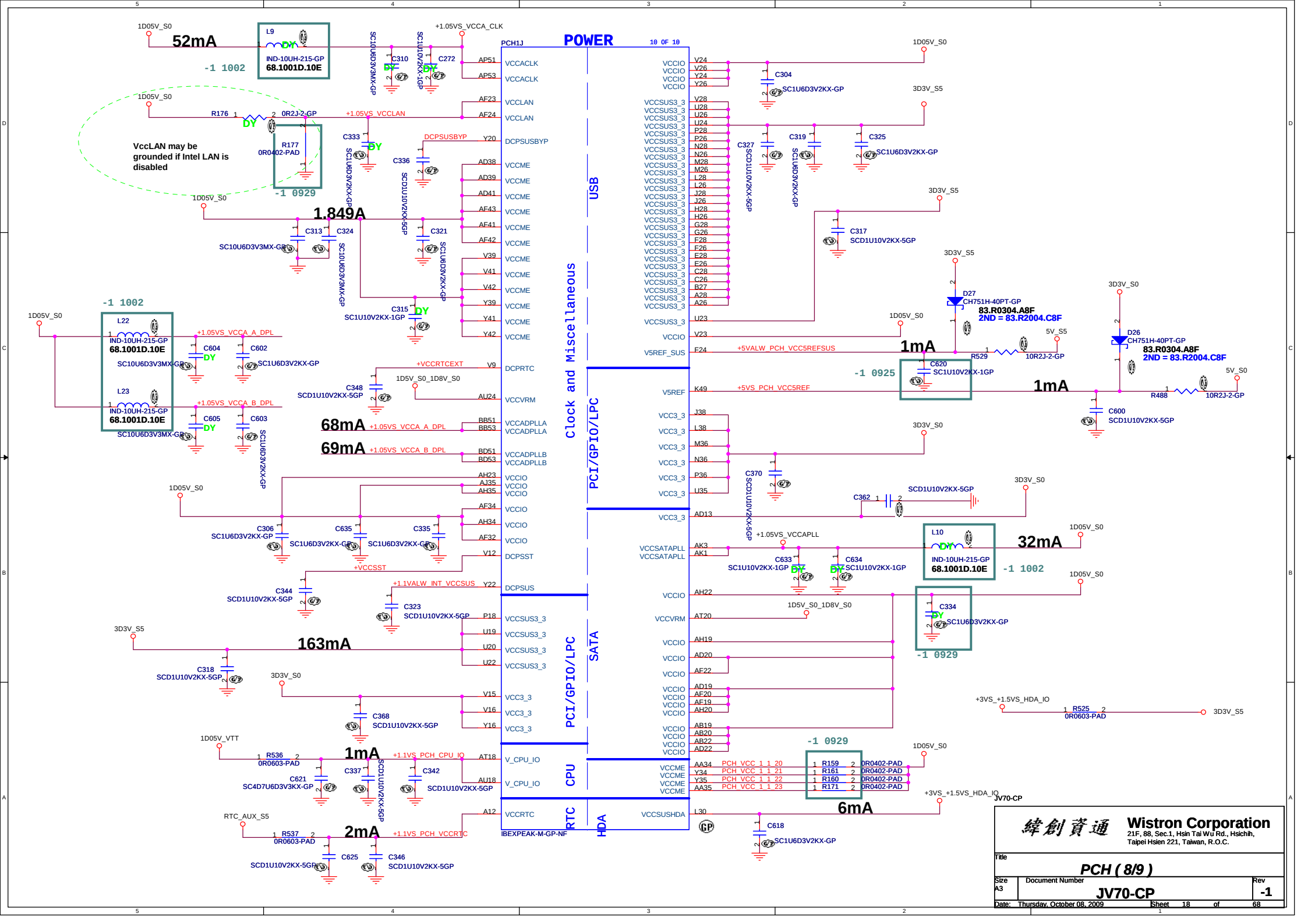
POWER
10 OF 10
PCH1J
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
32mA
VccLAN may be grounded if Intel LAN is disabled
-1 1002
-1 0929
-1 0925
83.R0304.A8F
2ND = 83.R2004.C8F
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Title
PCH (8/9)
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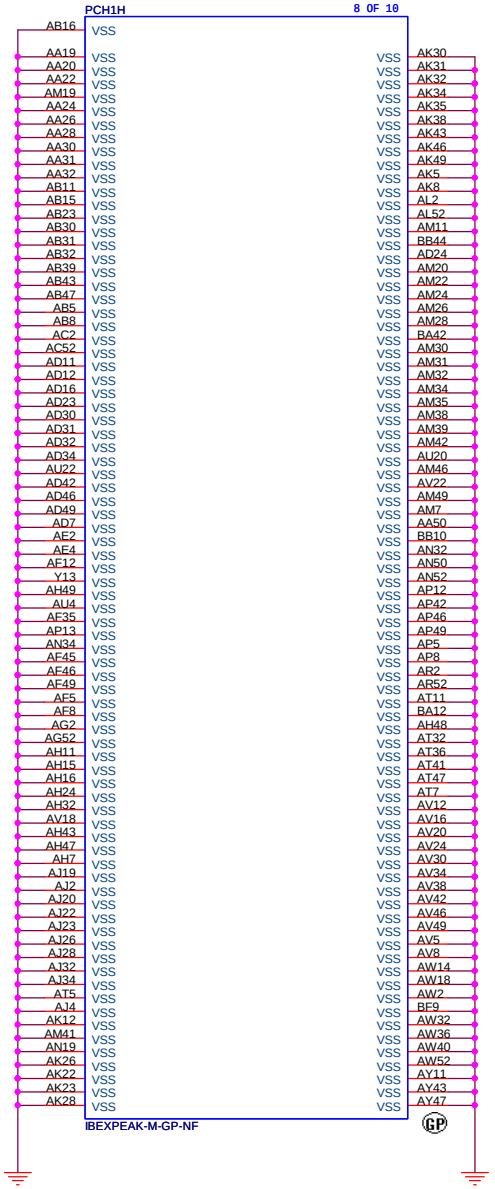

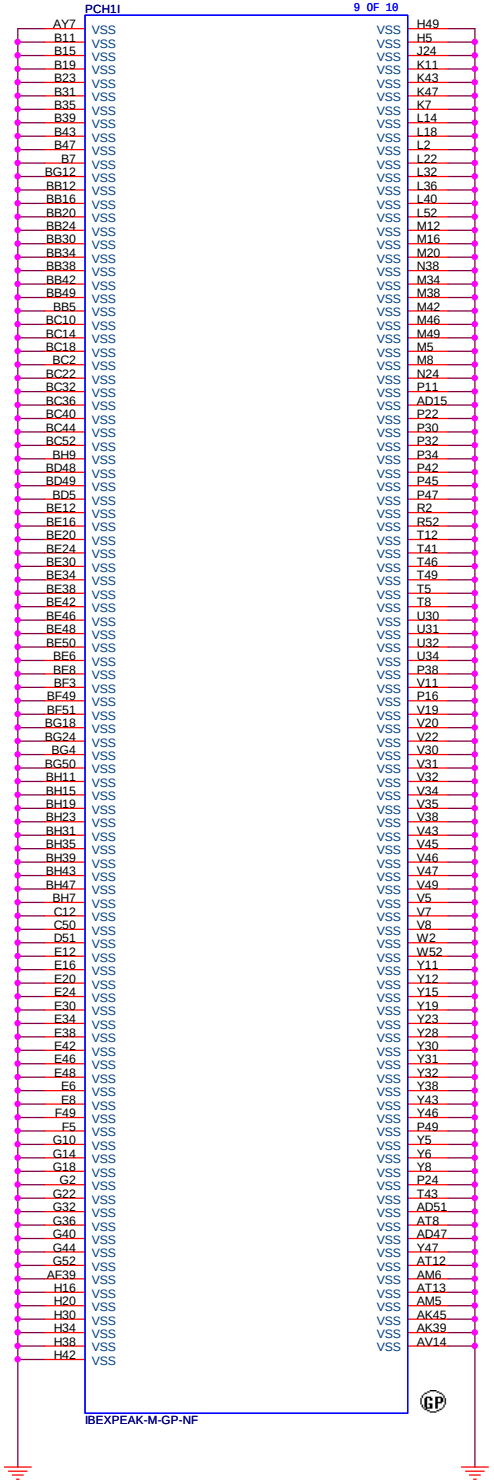

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Title: ***PCH (9/9)***

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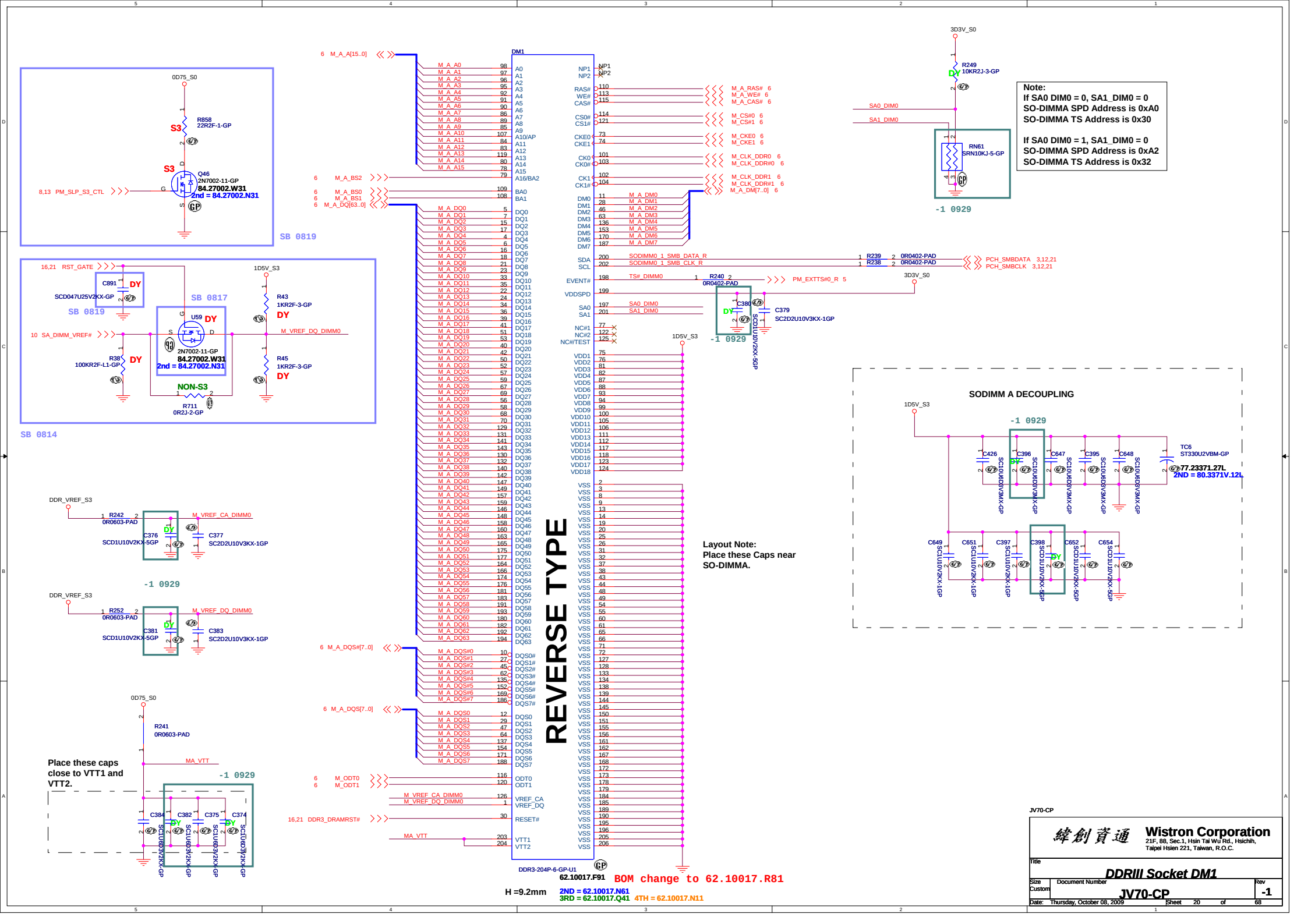
DM1
REVERSE TYPE
DDR3-204P-6-GP-U1
62.10017.F91
BOM change to 62.10017.R81
H =9.2mm
2ND = 62.10017.N61
3RD = 62.10017.Q41
4TH = 62.10017.N11
SB 0819
SB 0817
SB 0814
NON-S3
-1 0929
DY
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
SODIMM A DECOUPLING
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DDRIII Socket DM1
JV70-CP
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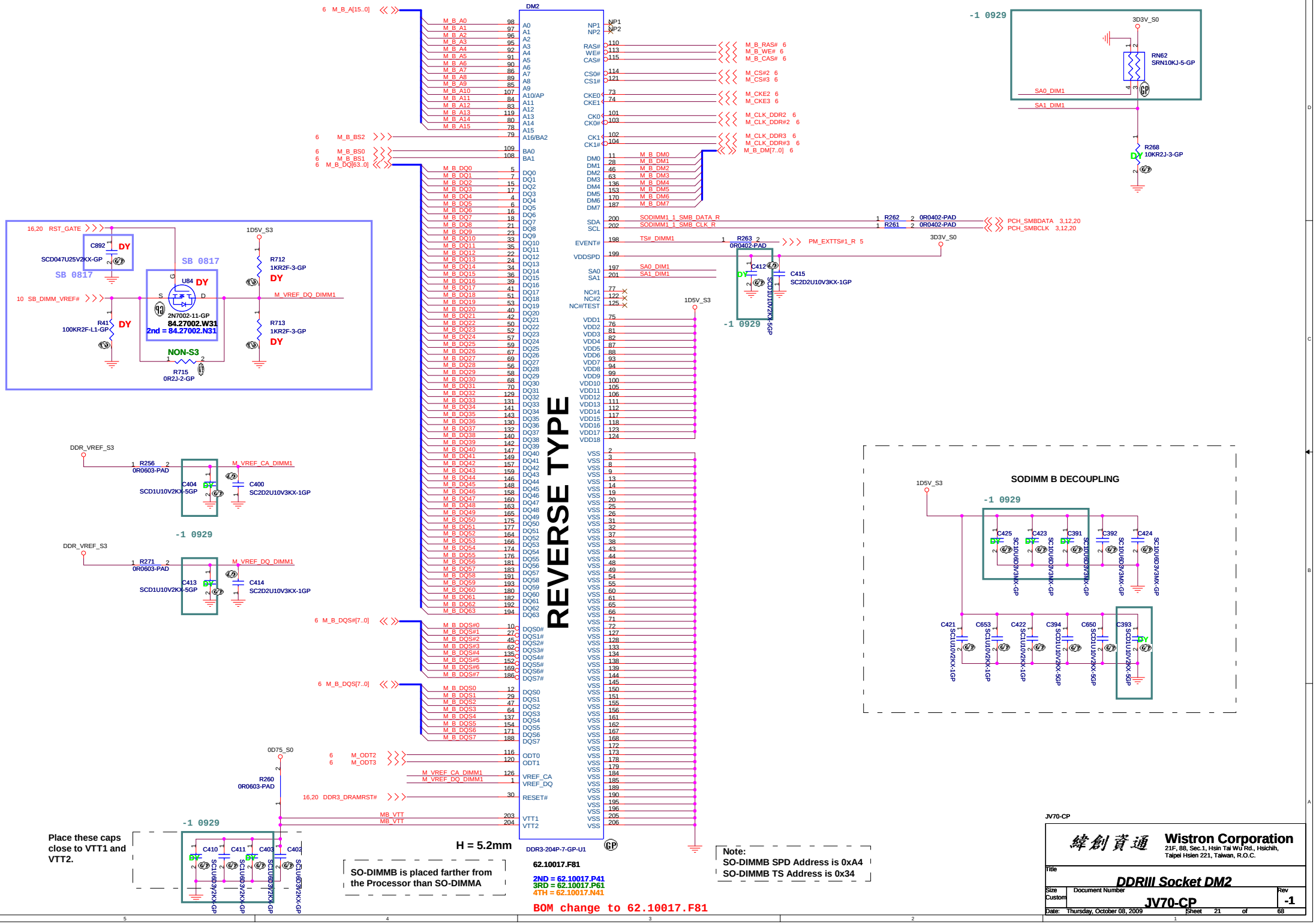
DM2
REVERSE TYPE
DDR3-204P-7-GP-U1
62.10017.F81
2ND = 62.10017.P41
3RD = 62.10017.P61
4TH = 62.10017.N41
BOM change to 62.10017.F81
H = 5.2mm
SO-DIMMB is placed farther from the Processor than SO-DIMMA
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SB 0817
NON-S3
SODIMM B DECOUPLING
-1 0929
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DDRIII Socket DM2
JV70-CP
Size Custom
Document Number
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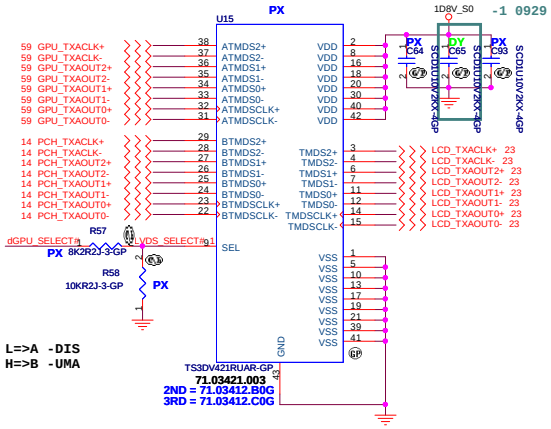
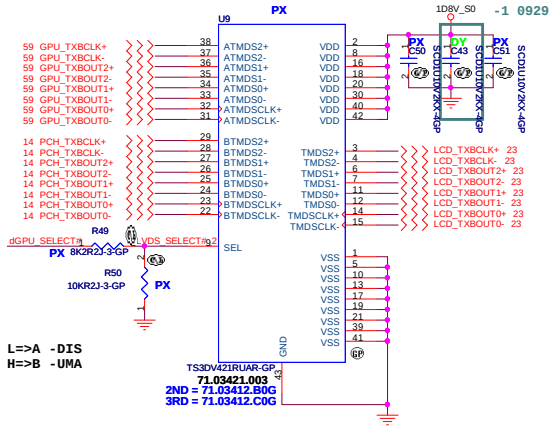
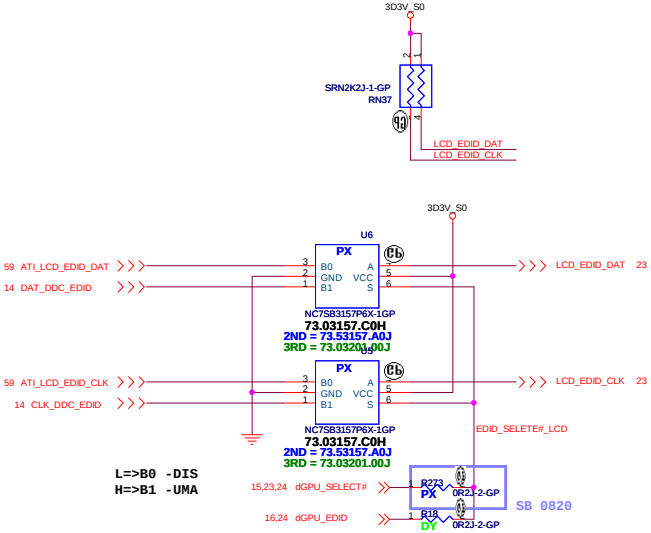
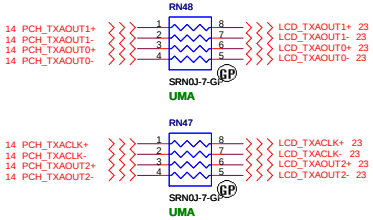
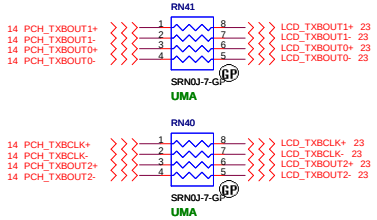
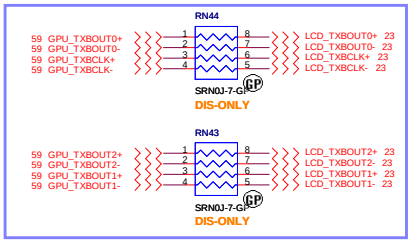


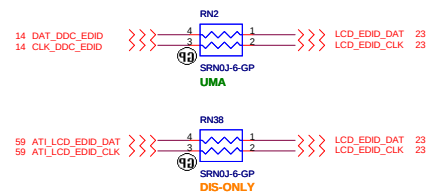








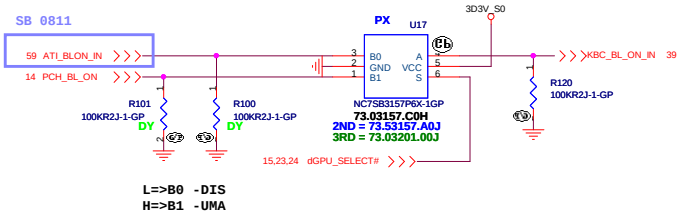


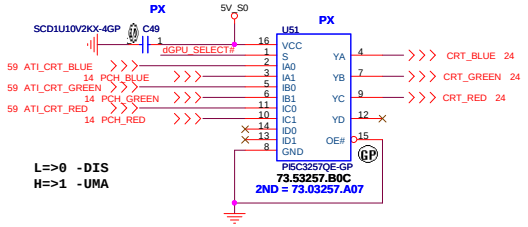


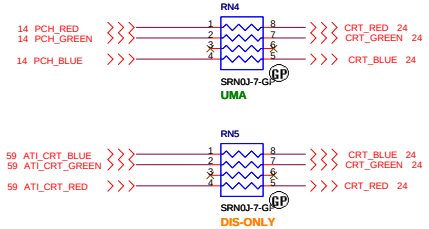
LVDS

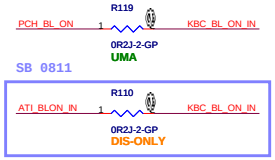
FUNCTION TABLE

$EL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-









CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

JV70-CP

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Title: PX_SWITCH

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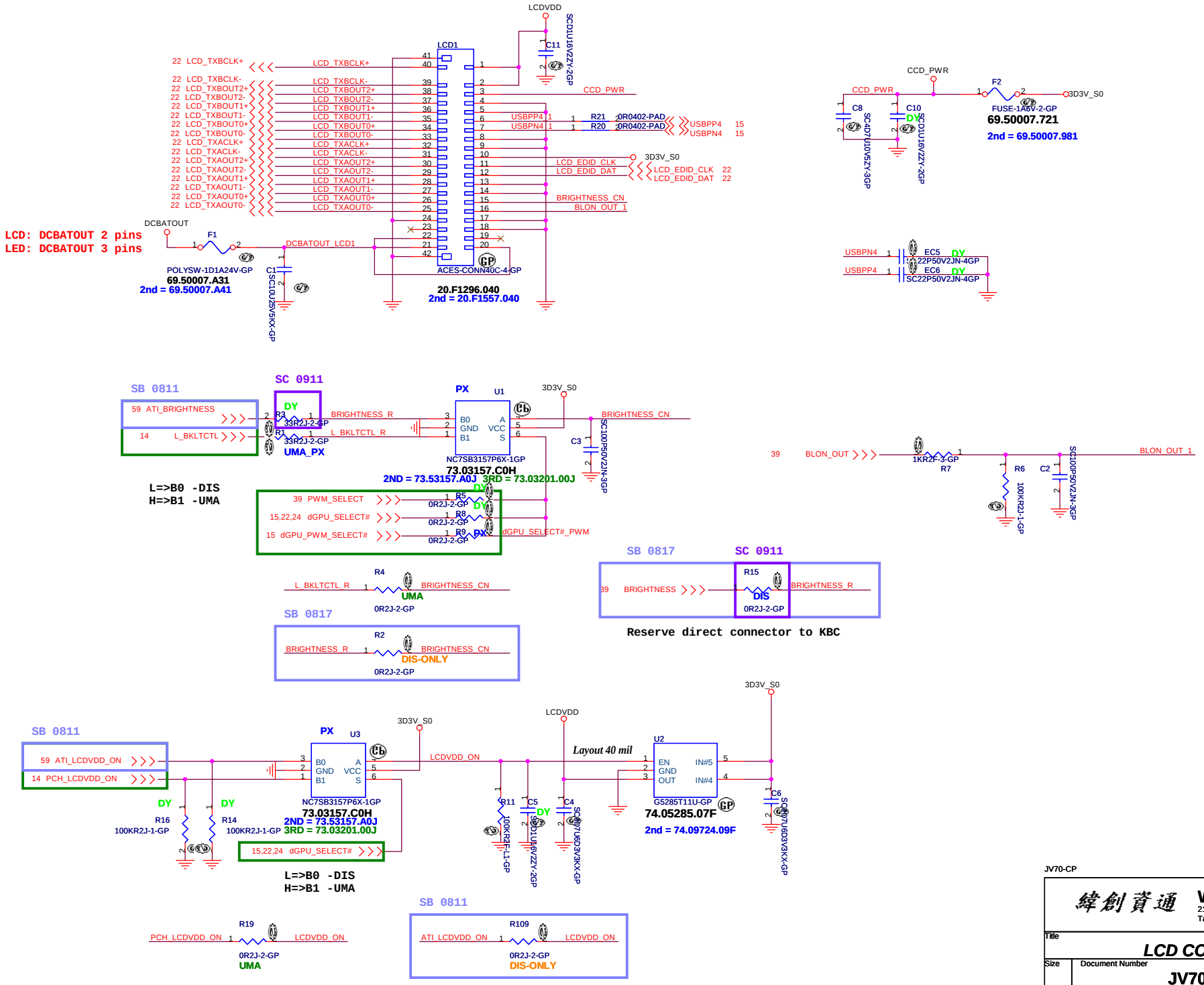
LCD/INVERTER/CCD CONN



JV70-CP

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
LCD CONN			
Size	Document Number		Rev
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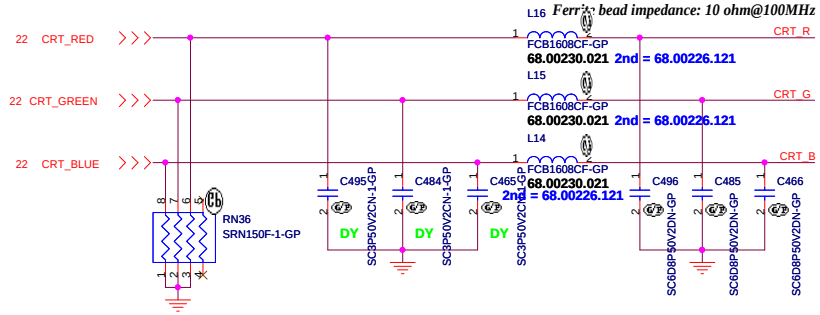
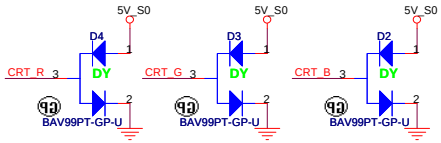
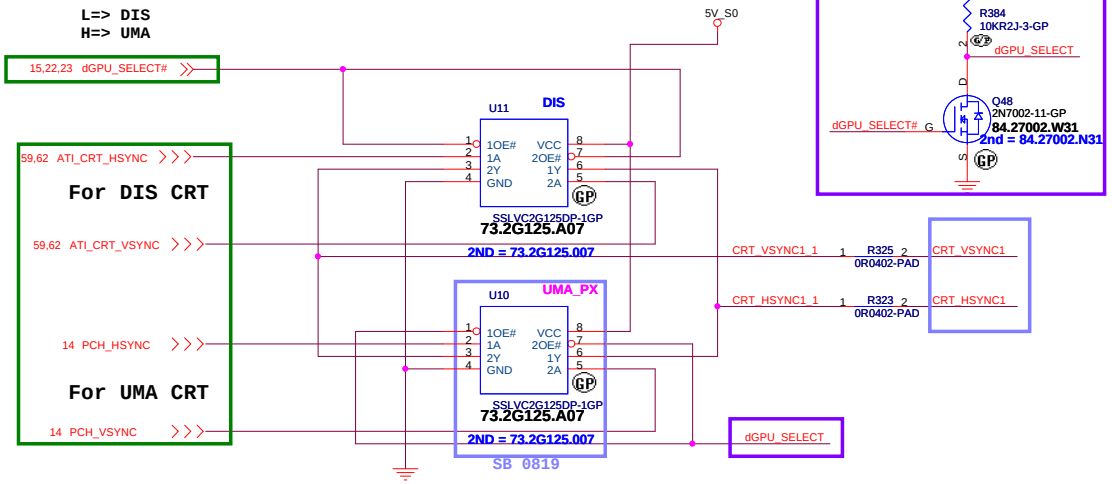
Layout Note:
Place these resistors close to the CRT-out connector



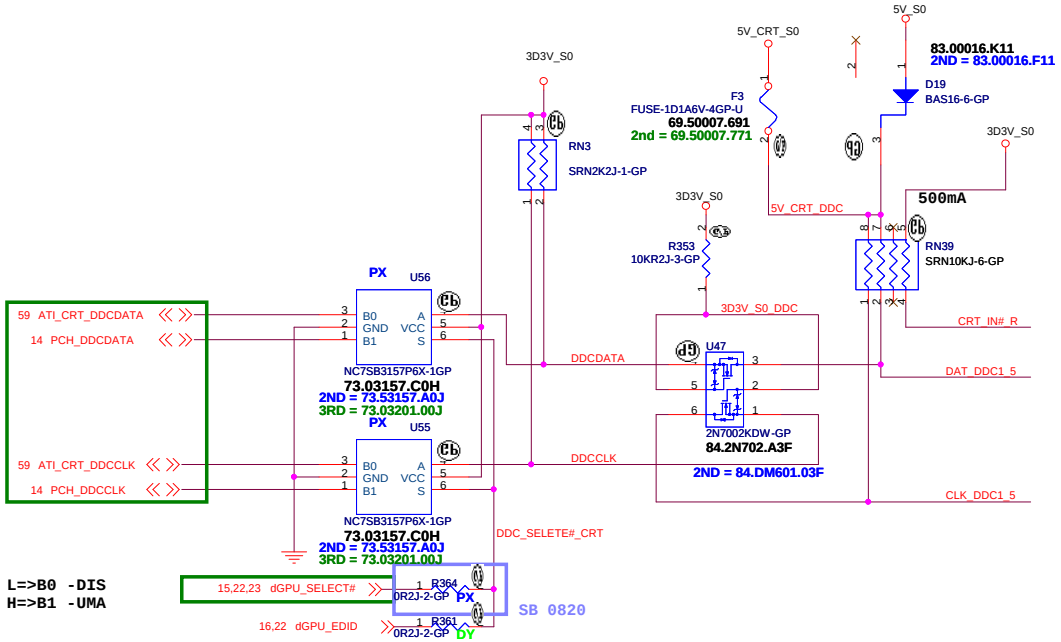
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



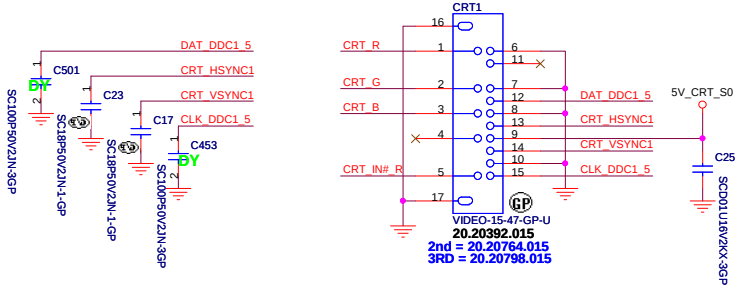
Hsync & Vsync level shift

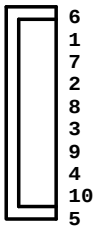


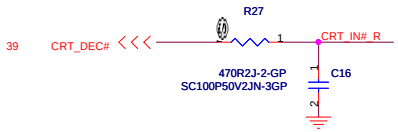
DDC_CLK & DATA level shift

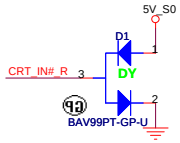


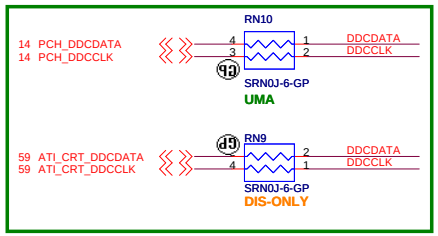
CRT I/F & CONNECTOR











JV70-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

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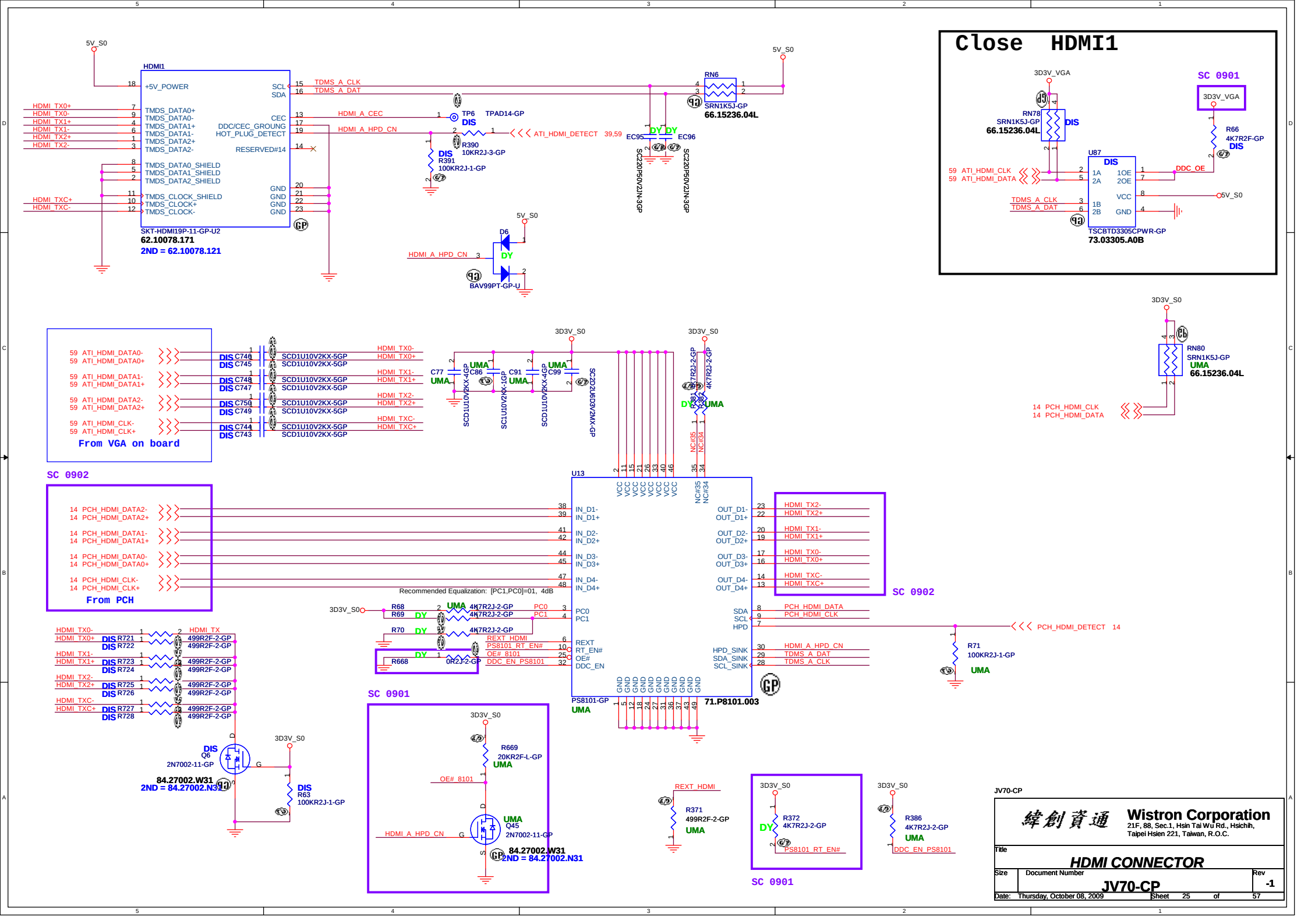
Close HDMI1
HDMI1
SKT-HDMI19P-11-GP-U2
62.10078.171
2ND = 62.10078.121
5V_S0
HDMI_TX0+
HDMI_TX0-
HDMI_TX1+
HDMI_TX1-
HDMI_TX2+
HDMI_TX2-
HDMI_TXC+
HDMI_TXC-
TMDS_A_CLK
TMDS_A_DAT
HDMI_A_CEC
HDMI_A_HPD_CN
ATI_HDMI_DETECT 39,59
TP6 TPAD14-GP
R390 10KR2J-3-GP
R391 100KR2J-1-GP
RN6 SRN1K5J-GP
66.15236.04L
EC95 SC220P50V2JN-3GP
EC96 SC220P50V2JN-3GP
D6 BAV99PT-GP-U
3D3V_VGA
RN78 SRN1K5J-GP
66.15236.04L
SC 0901
R66 4K7R2F-GP
U87 TSCBTD3305CPWR-GP
73.03305.A0B
DDC_OE
59 ATI_HDMI_CLK
59 ATI_HDMI_DATA
From VGA on board
SC 0902
From PCH
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
RN80 SRN1K5J-GP
66.15236.04L
U13
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
PCH_HDMI_DETECT 14
R71 100KR2J-1-GP
R721 R722 R723 R724 R725 R726 R727 R728
499R2F-2-GP
Q6 2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
R63 100KR2J-1-GP
R669 20KR2F-L-GP
Q45 2N7002-11-GP
R371 499R2F-2-GP
R372 4K7R2J-2-GP
R386 4K7R2J-2-GP
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
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-1
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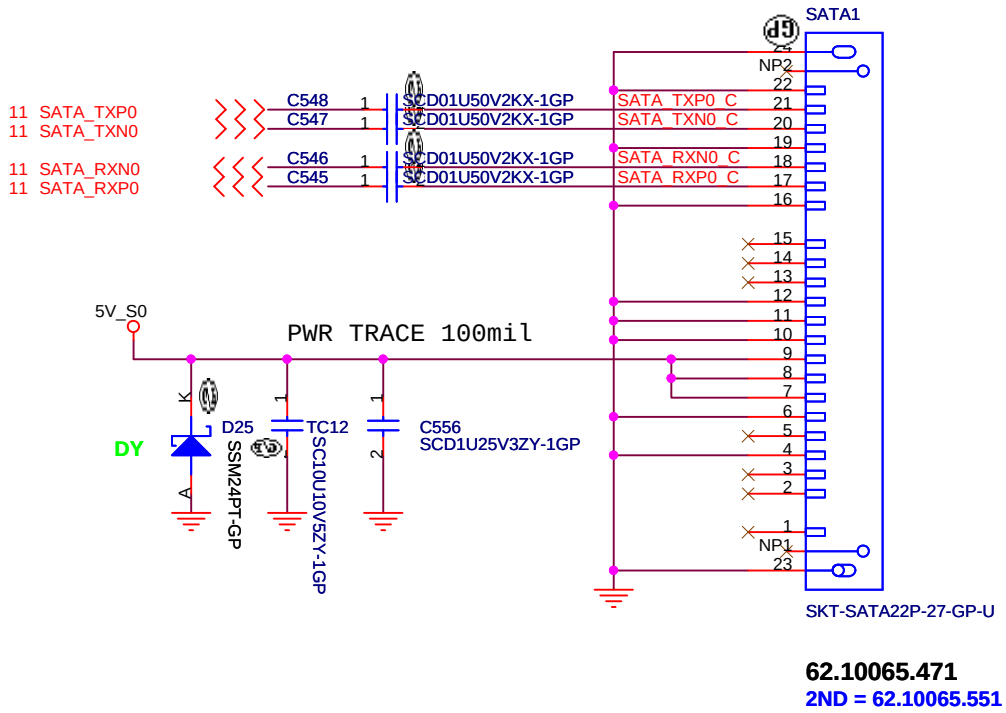
SATA Connector



62.10065.471
2ND = 62.10065.551

JV70-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD CONN***	
Size	Document Number **JV70-CP**	Rev -1
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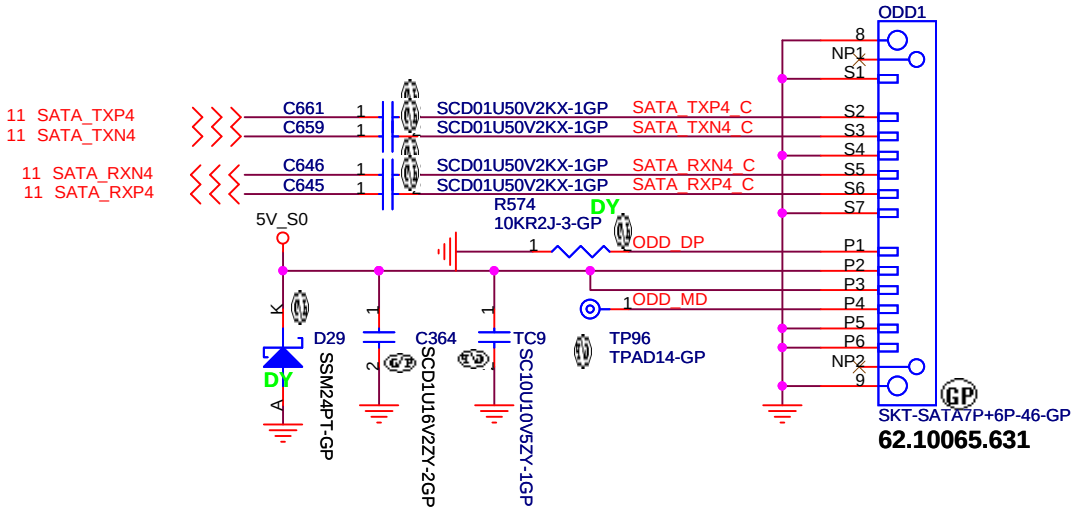
ODD Connector



JV70-CP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***ODD***	
Size	Document Number **JV70-CP**	Rev -1
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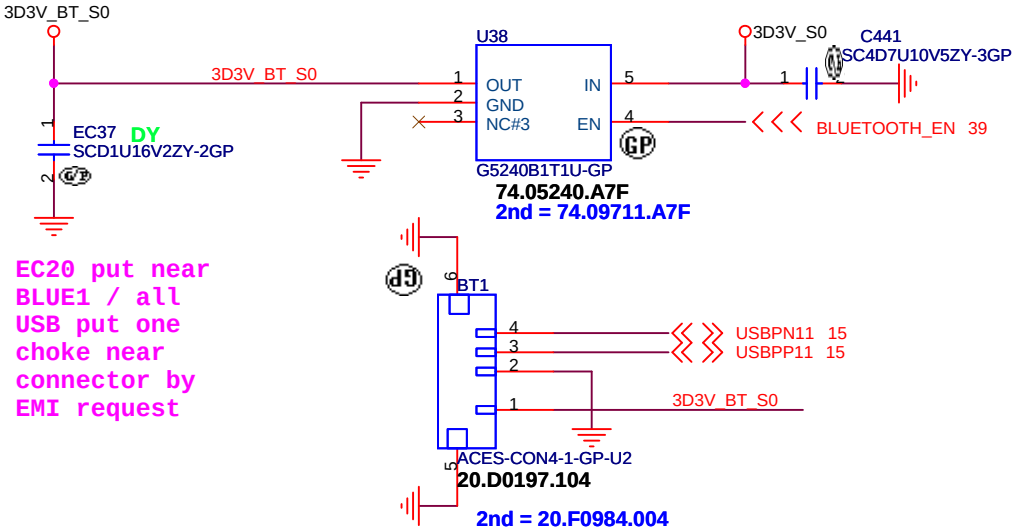
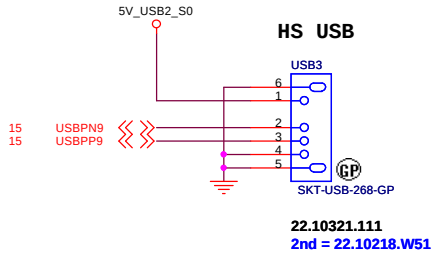
BLUETOOTH MODULE

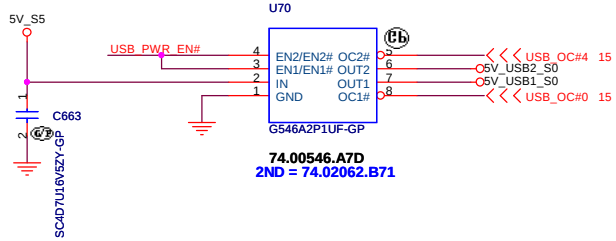


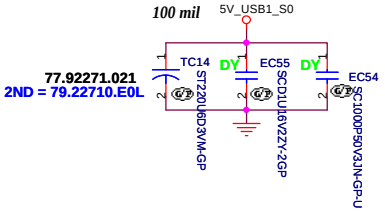
JV70-CP

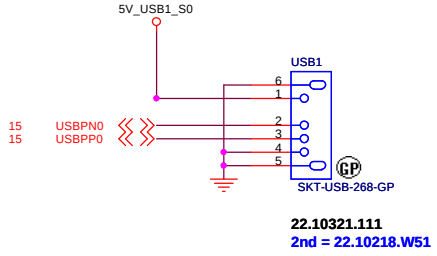
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

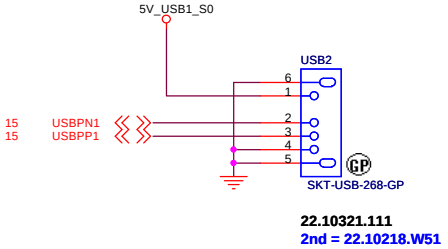
Title: ***BLUETOOTH***		
Size	Document Number: **JV70-CP**	Rev: -1
Date: Thursday, October 08, 2009	Sheet 28 of 68	

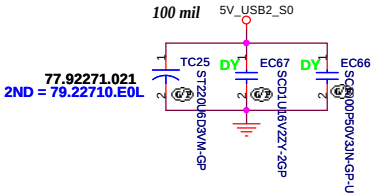


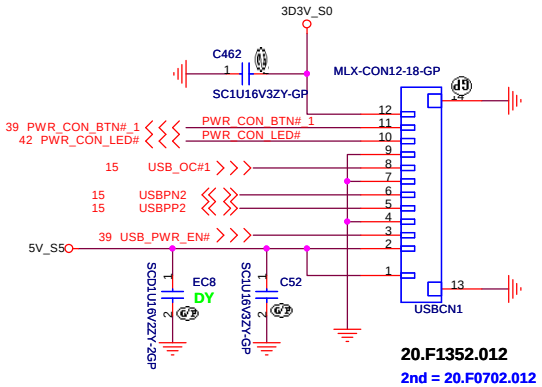


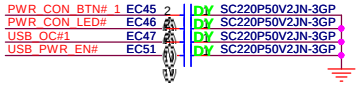












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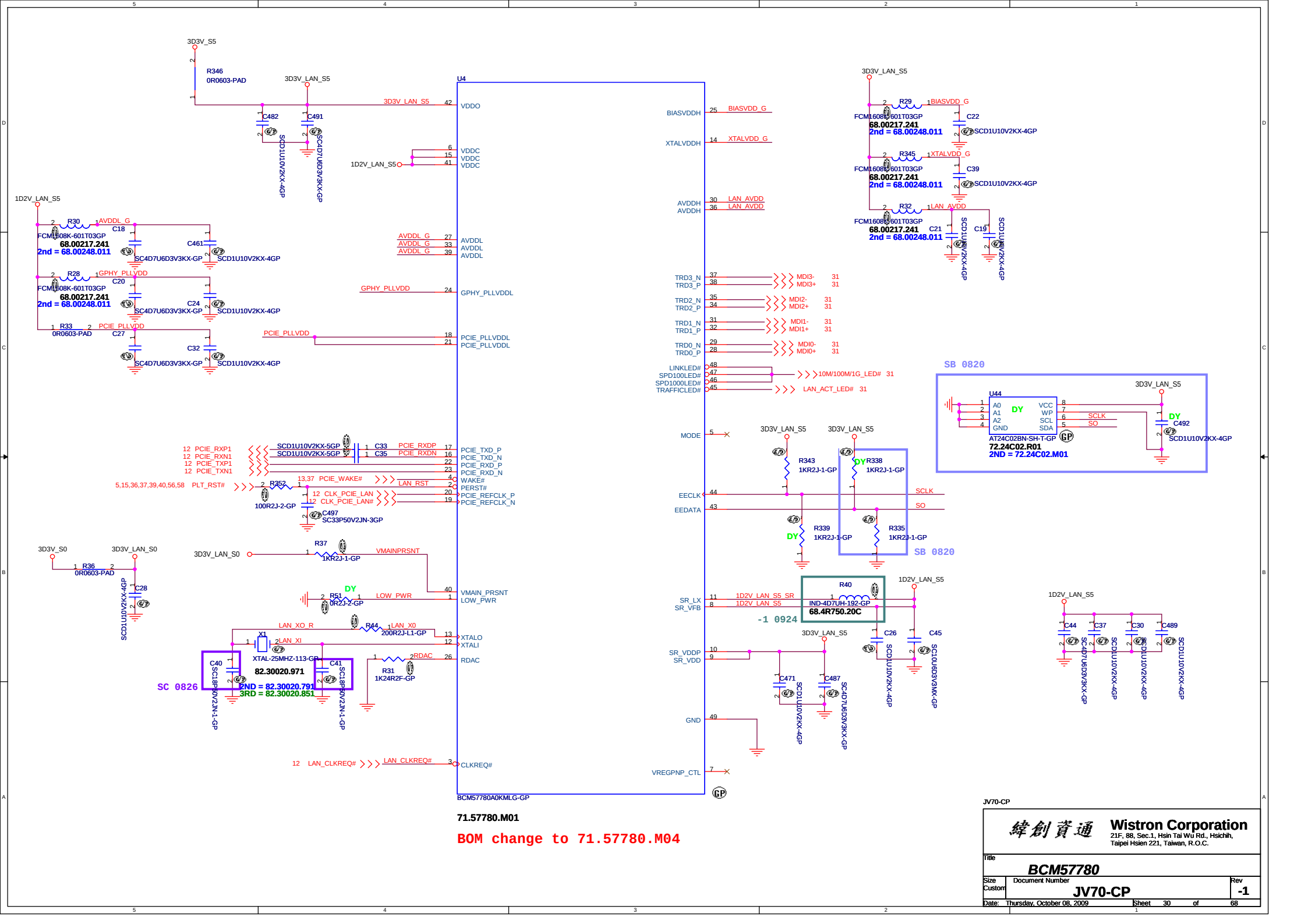
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **USB CONN**		
Size	Document Number: JV70-CP	Rev: -1
Date: Thursday, October 08, 2009	Sheet 29 of 68	


3D3V_S5
R346
0R0603-PAD
3D3V_LAN_S5
U4
VDDO
VDDC
VDDC
VDDC
1D2V_LAN_S5
C482
C491
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
BIASVDDH
XTALVDDH
AVDDH
AVDDH
BIASVDD_G
XTALVDD_G
LAN_AVDD
LAN_AVDD
R29
R345
R32
FCM1608K-601T03GP
68.00217.241
2nd = 68.00248.011
C22
C39
C21
C19
AVDDL_G
GPHY_PLLVDD
PCIE_PLLVDD
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
R30
R28
R33
C18
C461
C20
C24
C27
C32
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
10M/100M/1G_LED#
LAN_ACT_LED#
SB 0820
U44
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
DY
C492
SCLK
SO
MODE
EECLK
EEDATA
R343
R338
R339
R335
1KR2J-1-GP
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
VREGPNP_CTL
1D2V_LAN_S5_SR
R40
IND-4D7UH-192-GP
68.4R750.20C
-1 0924
C26
C45
C471
C487
SC10U8D3V3MX-GP
SC4D7U6D3V3KX-GP
PCIE_RXP1
PCIE_RXN1
PCIE_TXP1
PCIE_TXN1
PCIE_RXDP
PCIE_RXDN
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
PLT_RST#
PCIE_WAKE#
LAN_RST
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_REFCLK_P
PCIE_REFCLK_N
WAKE#
PERST#
R352
100R2J-2-GP
C497
SC33P50V2JN-3GP
C33
C35
SCD1U10V2KX-5GP
R37
VMAINPRSNT
VMAIN_PRSNT
LOW_PWR
R51
0R2J-2-GP
LAN_XO_R
LAN_XO
R44
200R2J-L1-GP
XTALO
XTALI
X1
XTAL-25MHZ-113-GP
RDAC
R31
1K24R2F-GP
C40
C41
SC18P50V2JN-1-GP
82.30020.971
2ND = 82.30020.791
3RD = 82.30020.851
SC 0826
LAN_CLKREQ#
CLKREQ#
BCM57780A0KMLG-GP
71.57780.M01
BOM change to 71.57780.M04
3D3V_S0
3D3V_LAN_S0
R36
C28
C44
C37
C30
C489
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size
Custom
Document Number
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Rev
-1
Date: Thursday, October 08, 2009
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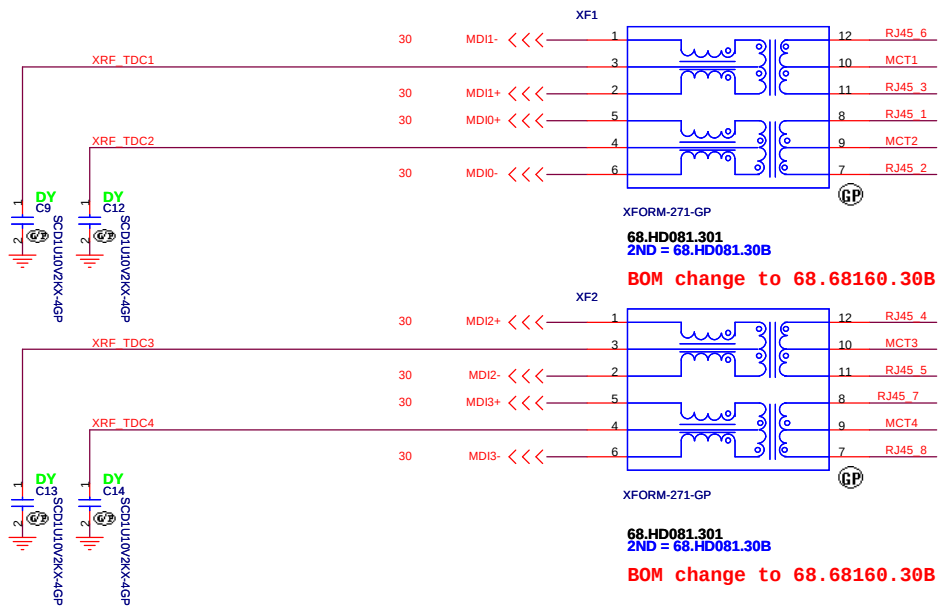
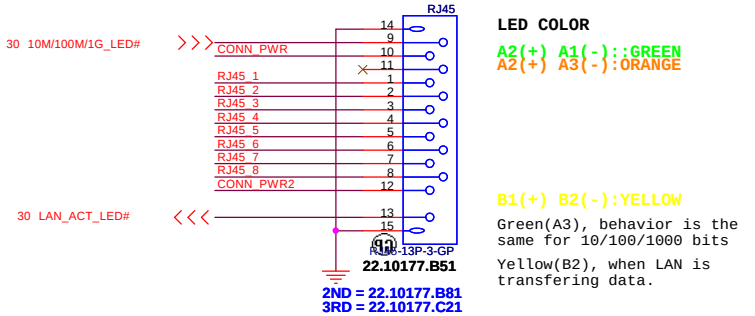
LAN Connector

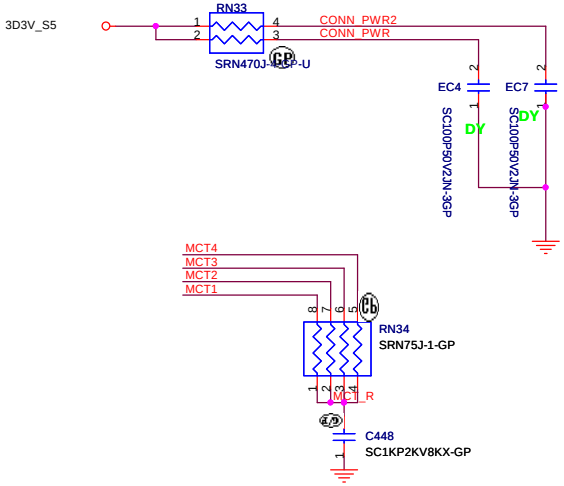
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

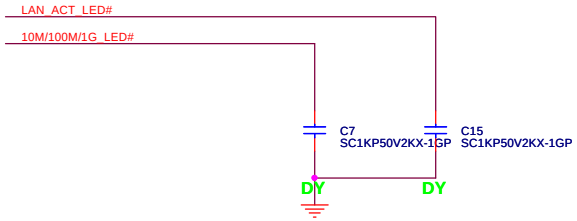
LAN Connector

GIGA Lan Transformer





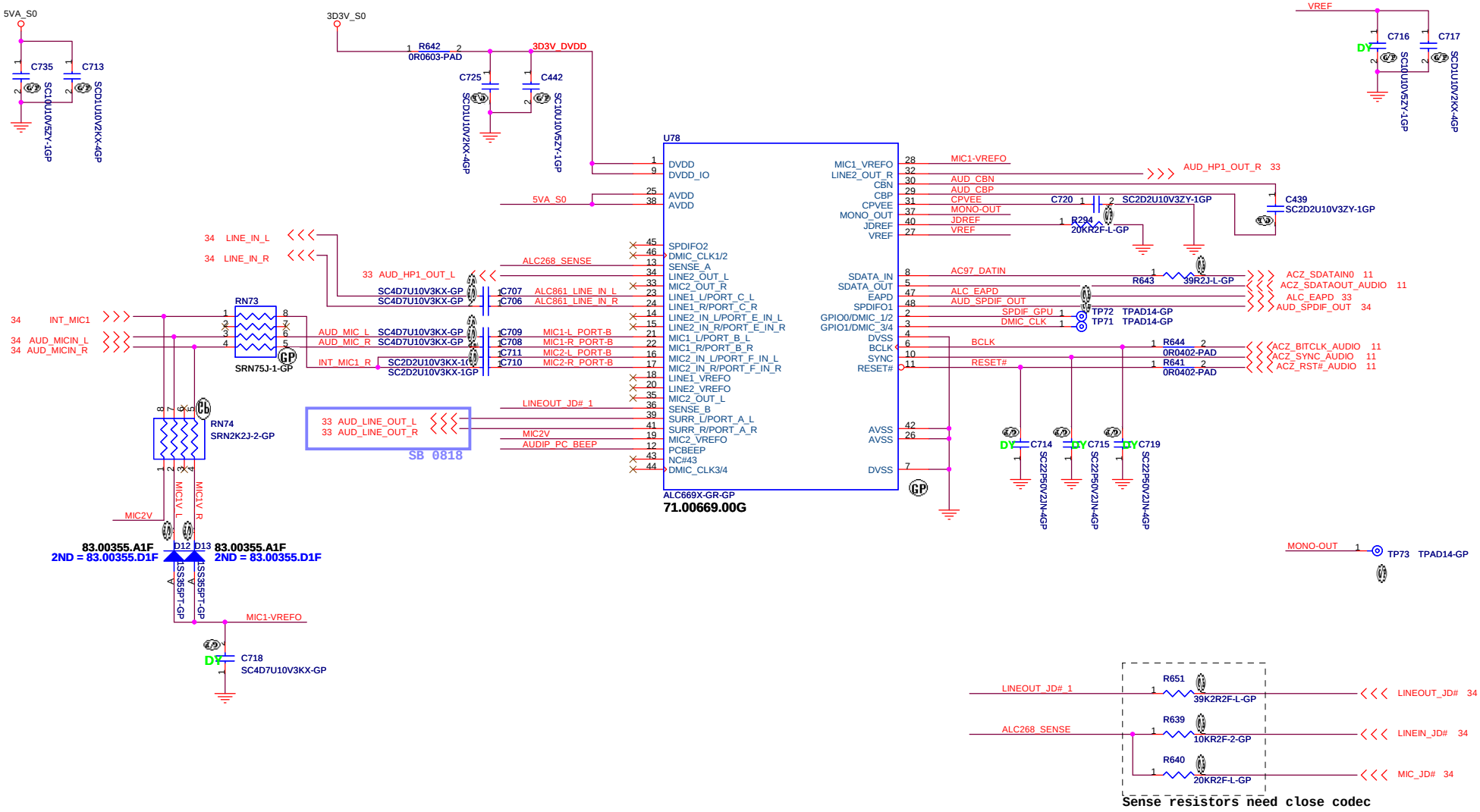




JV70-CP

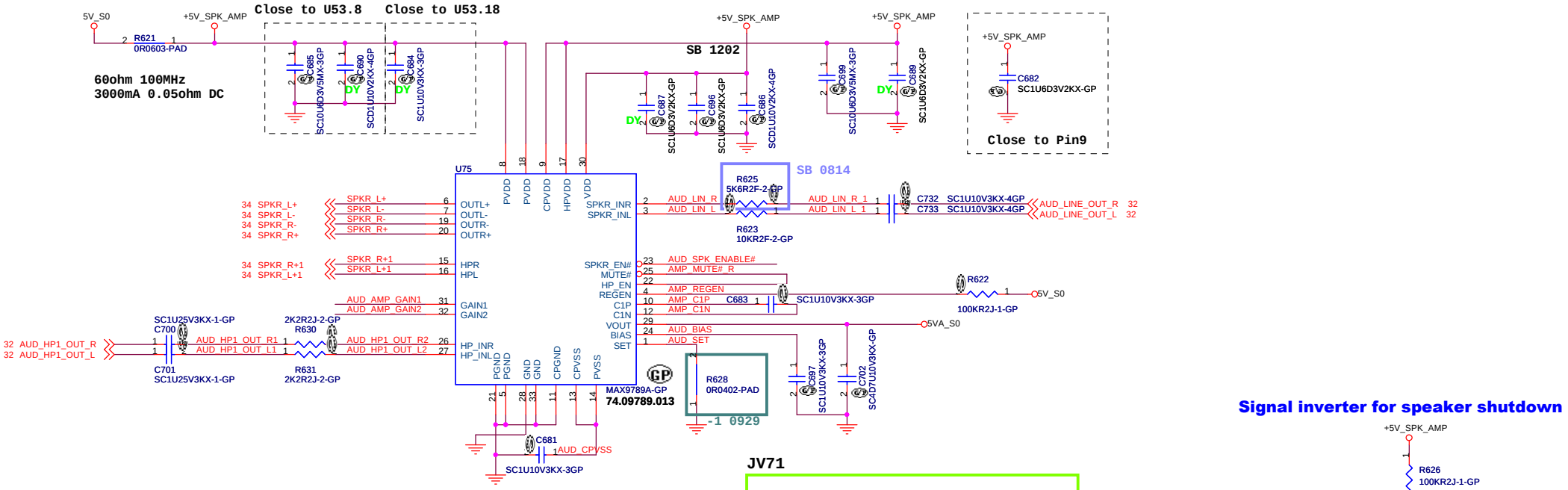
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

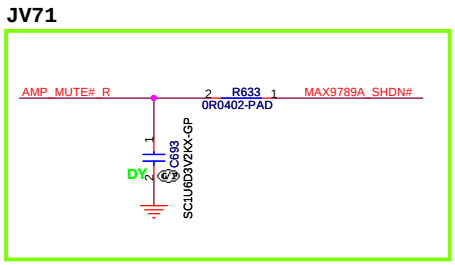
Title	LAN CONN	
Size A3	Document Number JV70-CP	Rev -1
Date: Thursday, October 08, 2009	Sheet 31 of 68	



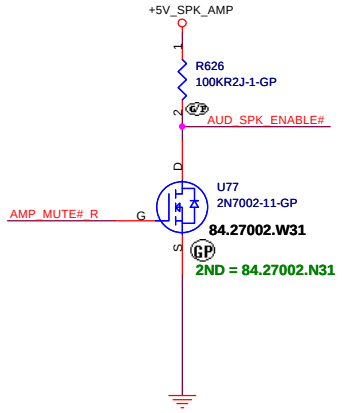
JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC669X***	
Size A3	Document Number **JV70-CP**	Rev **-1**
Date: Friday, October 09, 2009	Sheet 32 of 68	

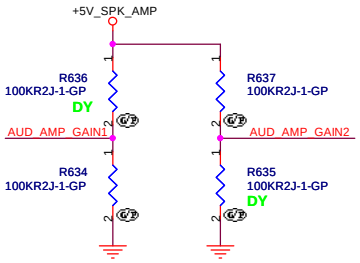




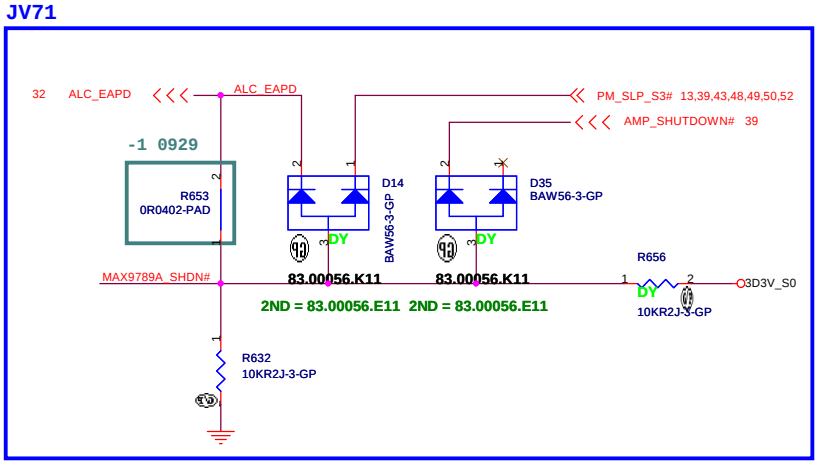
Signal inverter for speaker shutdown



GAIN SETTING



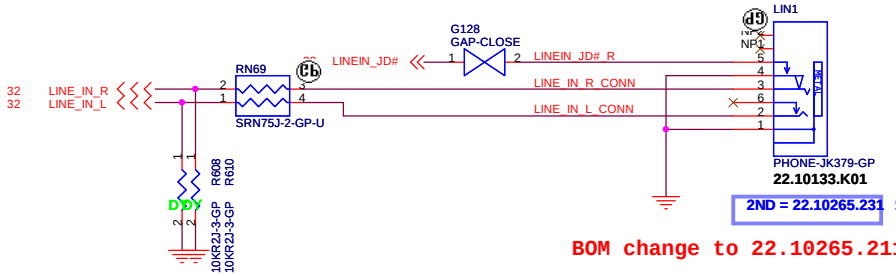
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



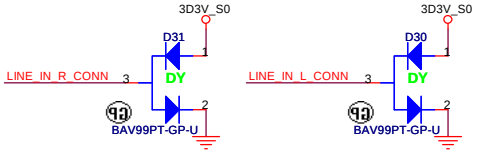
JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP MAX9789C		
Size	Document Number: JV70-CP	Rev: -1
Date: Thursday, October 08, 2009	Sheet 33 of 68	

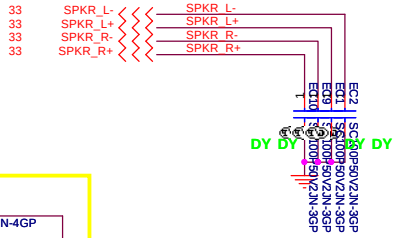
LINE IN

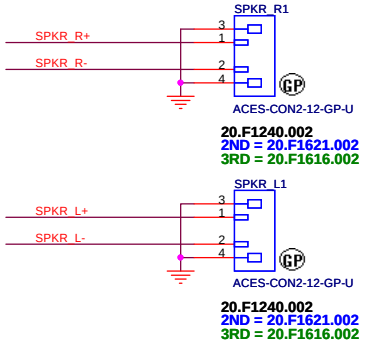


BOM change to 22.10265.211



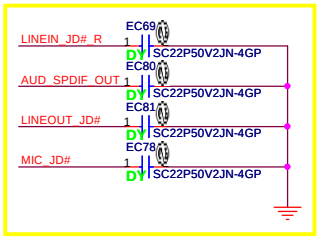
Internal Speaker

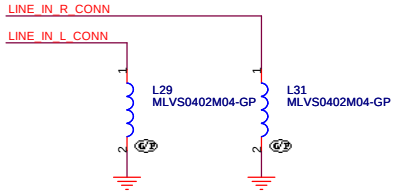




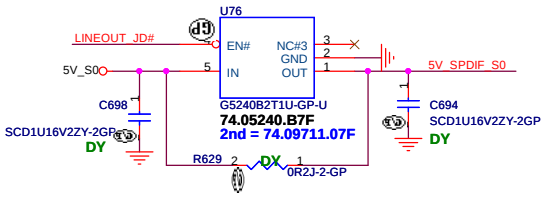
BOM change to 20.F1561.002

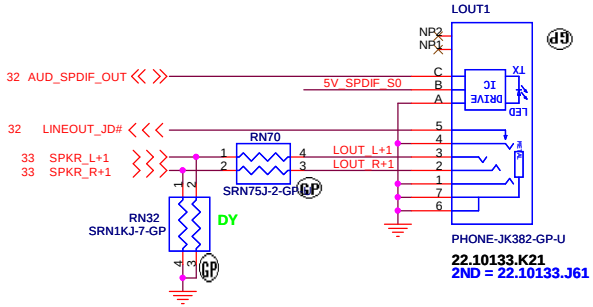
EMI

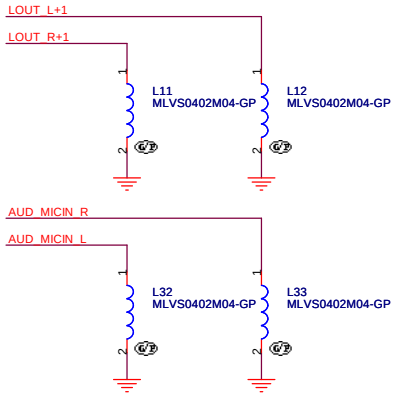




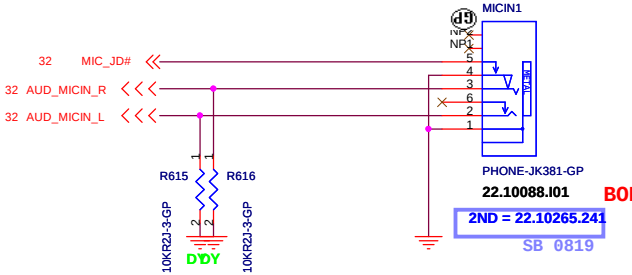
LINE OUT



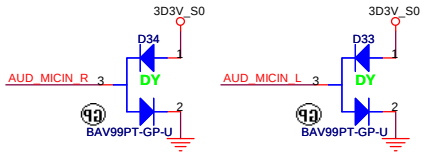




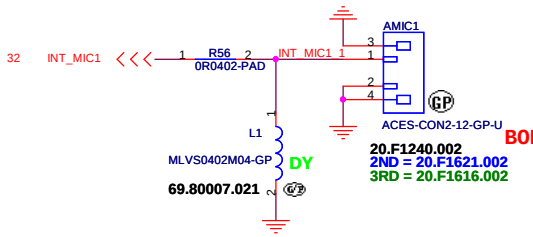
MIC IN



BOM change to 22.10265.201



Internal Mic



BOM change to 20.F1561.002

JV70-CP

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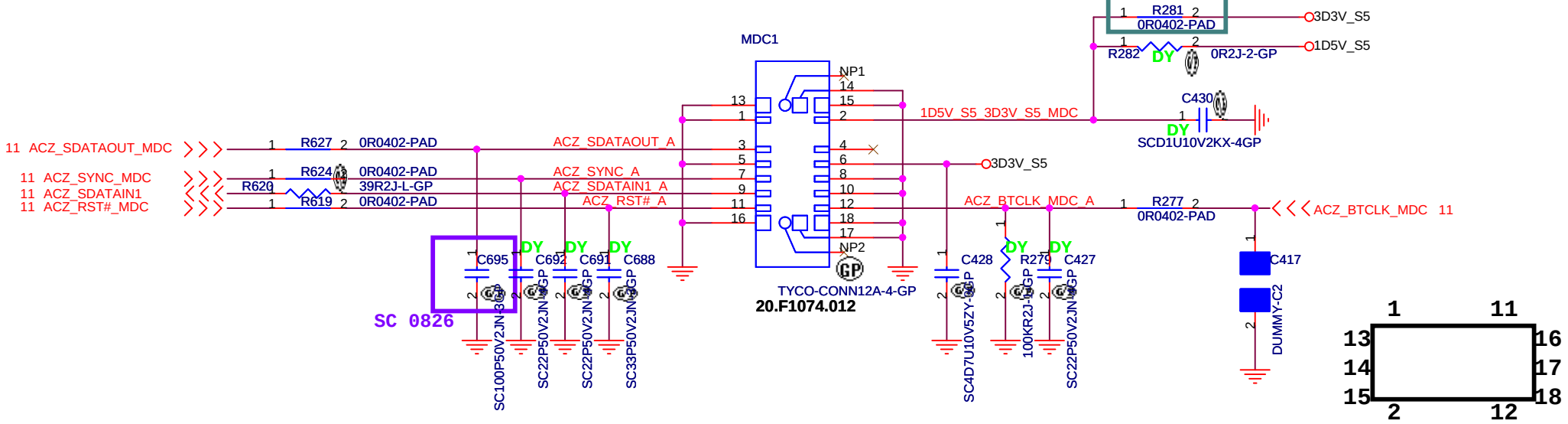
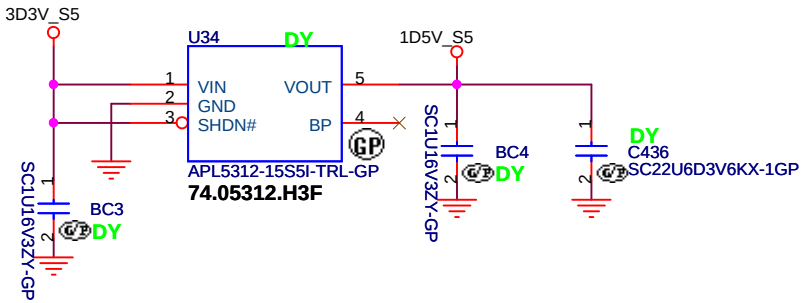
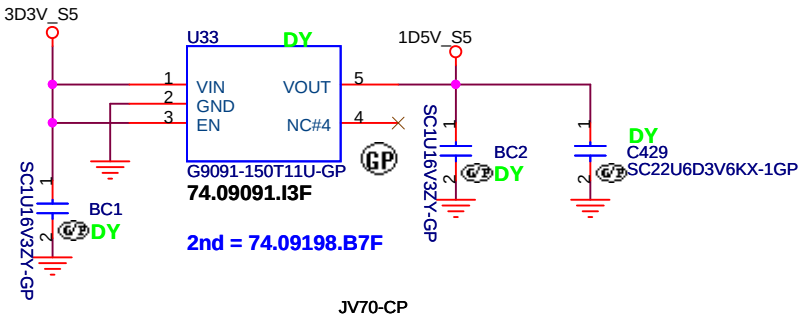
MDC 1.5 CONN

-1 0929







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Taipei Hsien 221, Taiwan, R.O.C.

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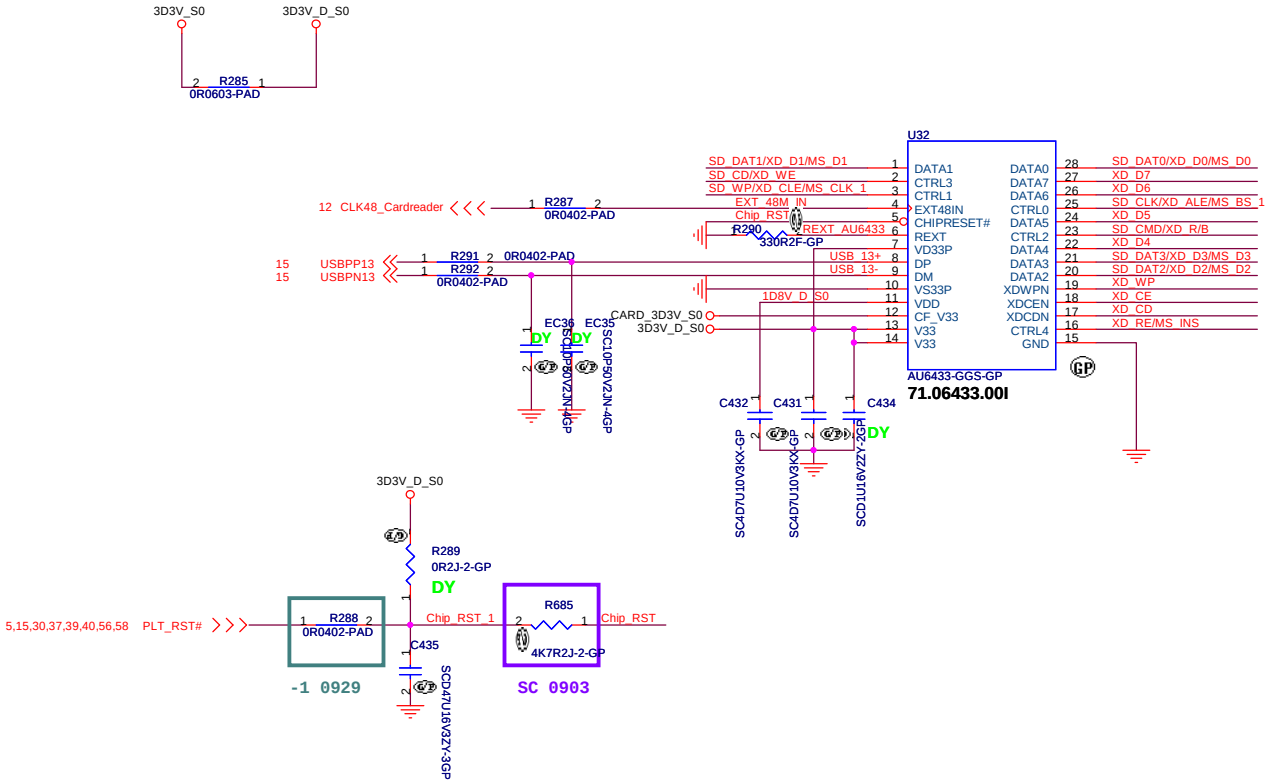
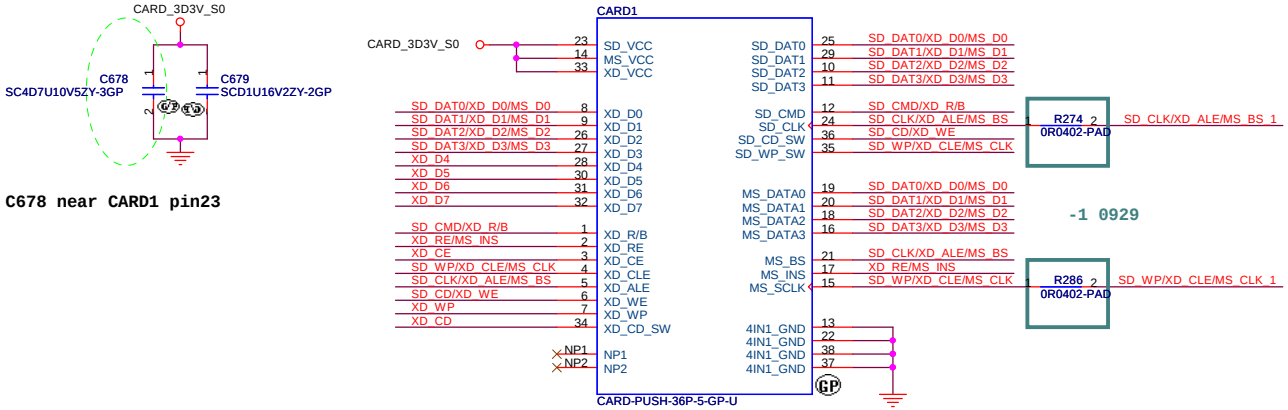
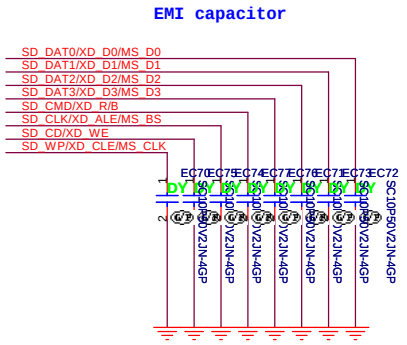


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





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Title: *Cardreader AU6433*		
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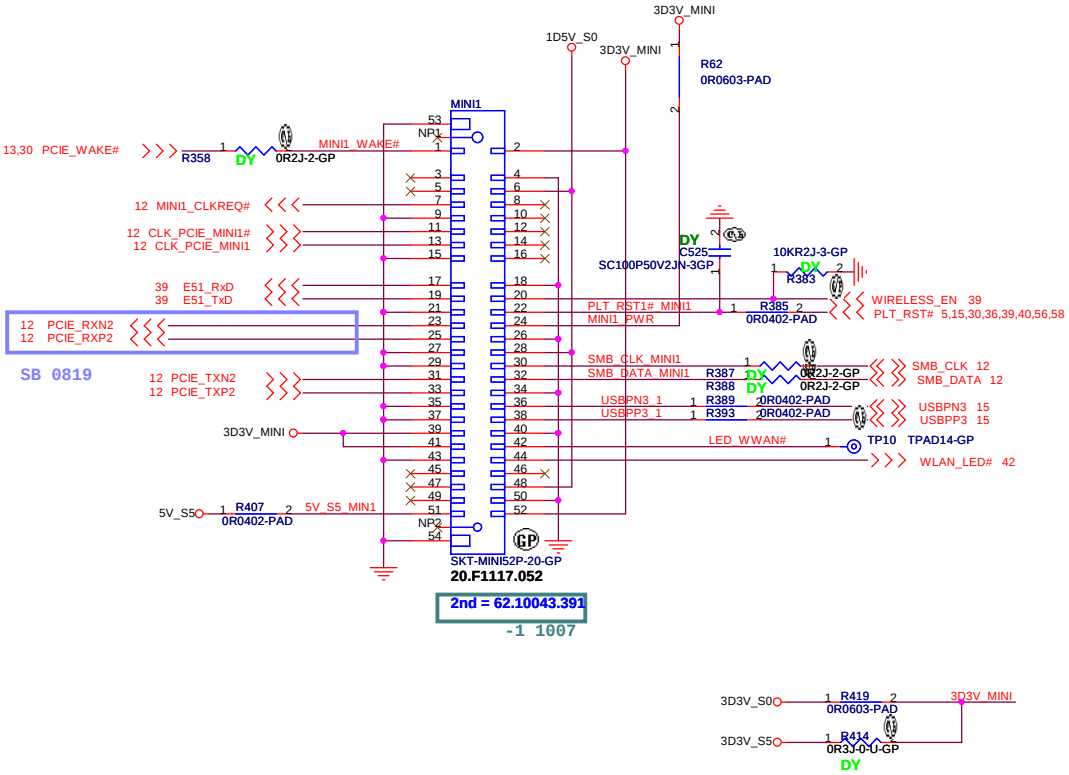
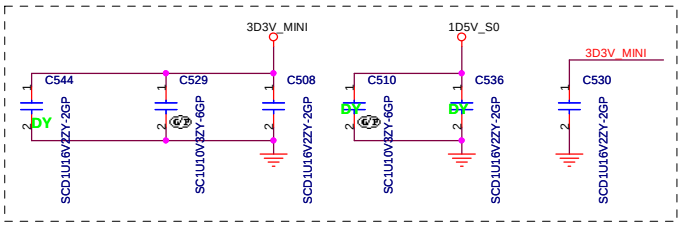
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector

JV70-CP

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Title		
MINI CARD		
Size: A3	Document Number: JV70-CP	Rev: -1
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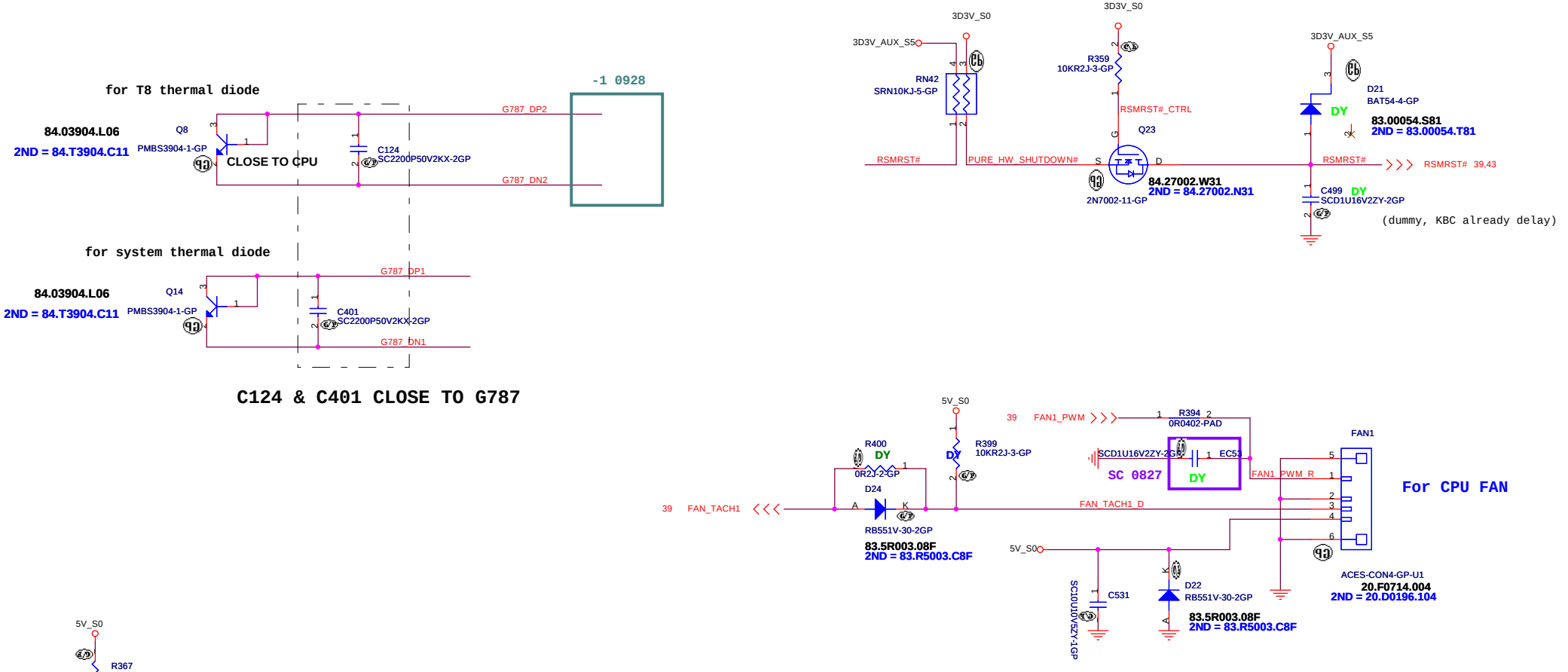

JV70-CP

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Title: ***Thermal/Fan Connector***

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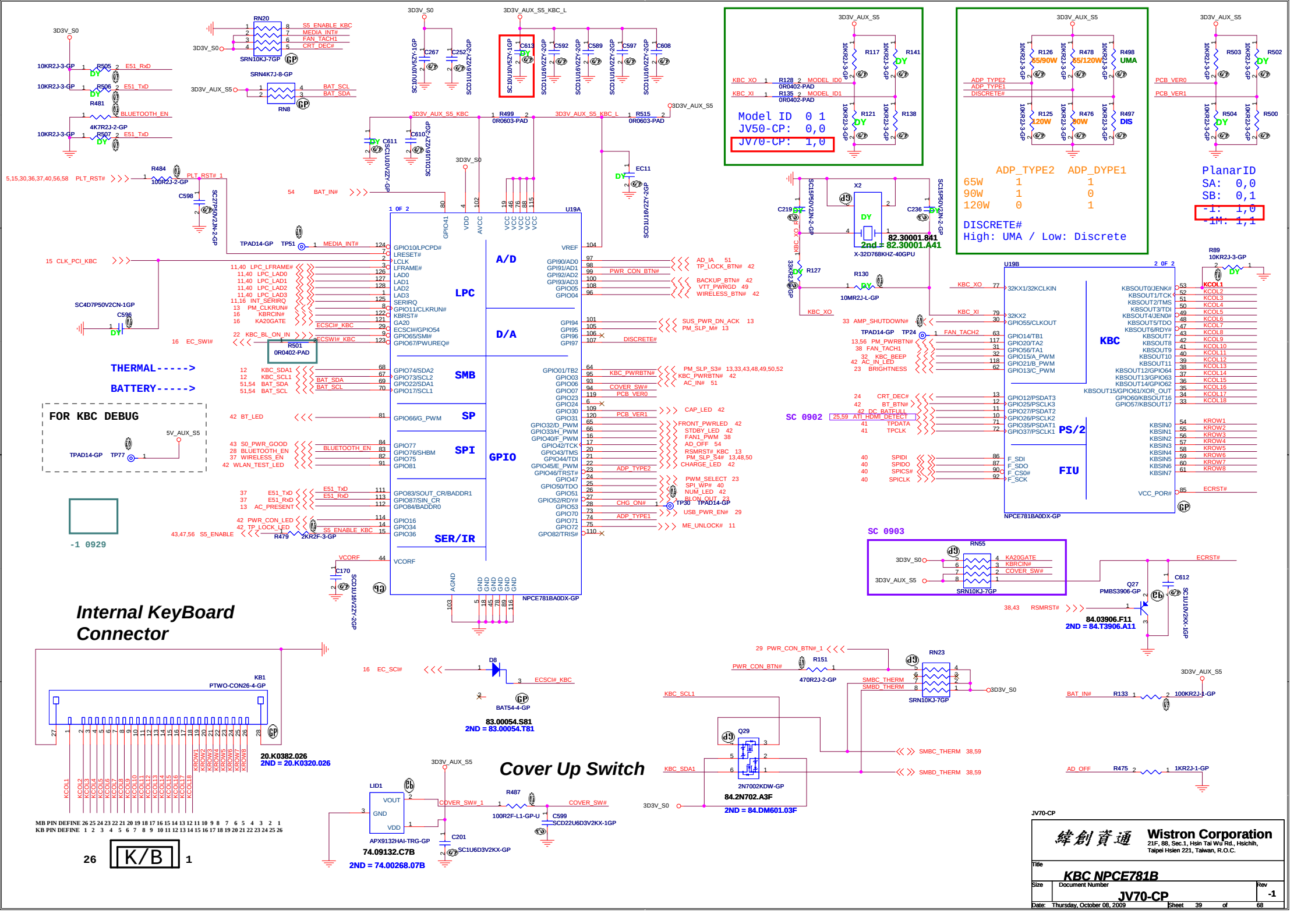
Model ID 0 1
JV50-CP: 0,0
JV70-CP: 1,0
ADP_TYPE2 ADP_DYPE1
65W 1 1
90W 1 0
120W 0 1
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
SC 0902
SC 0903
U19A
U19B
KBC
PS/2
FIU
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
NPCE781BA0DX-GP
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Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
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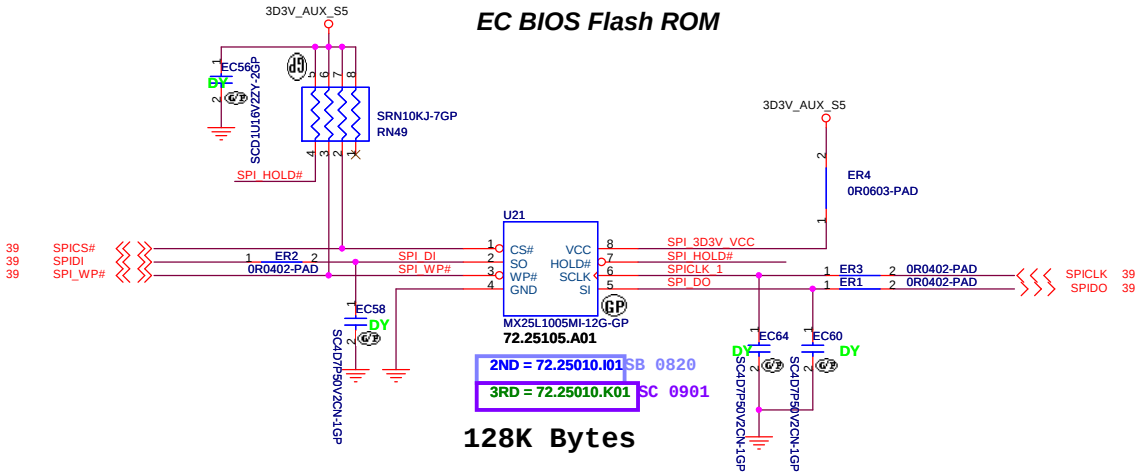
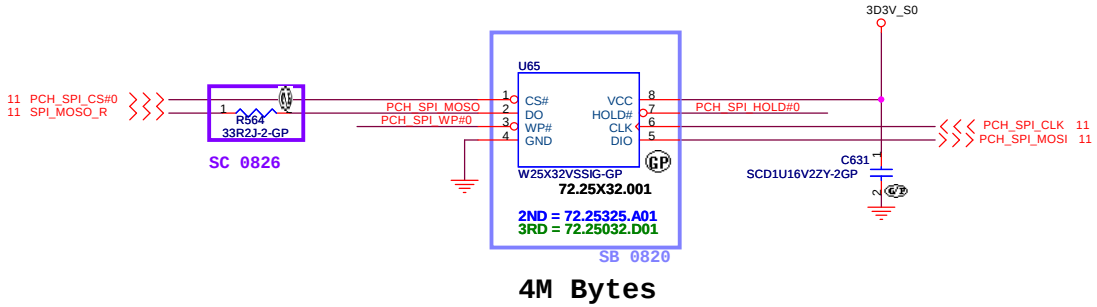
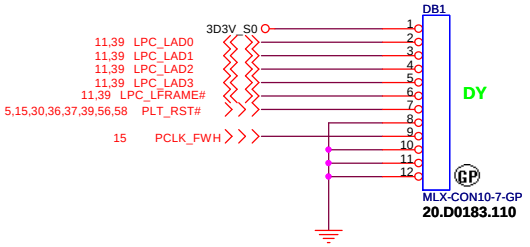
EC BIOS Flash ROM

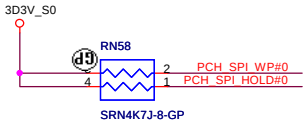


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





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Title: BIOS

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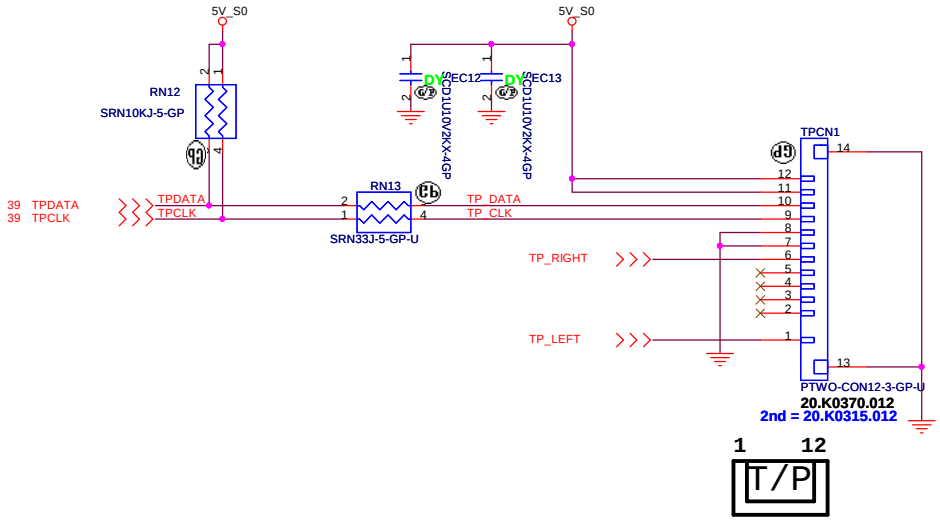
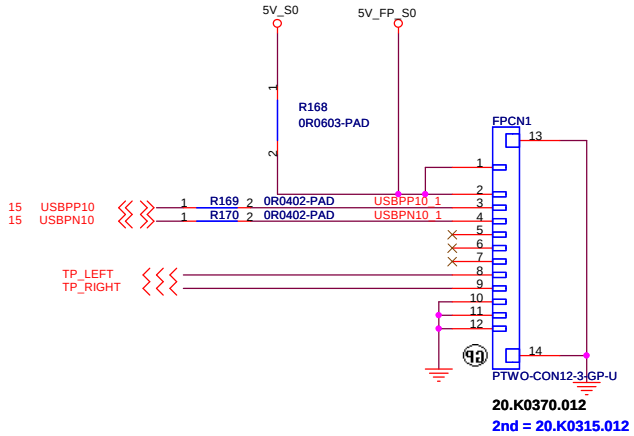
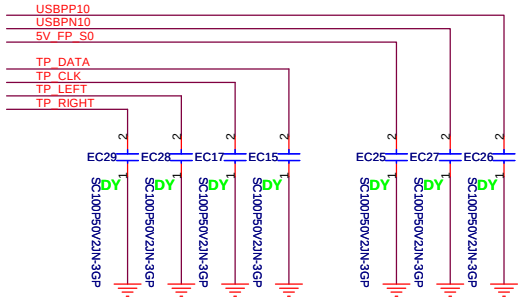
TOUCH PAD



Finger printer





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Title: *Touch PAD and FP*

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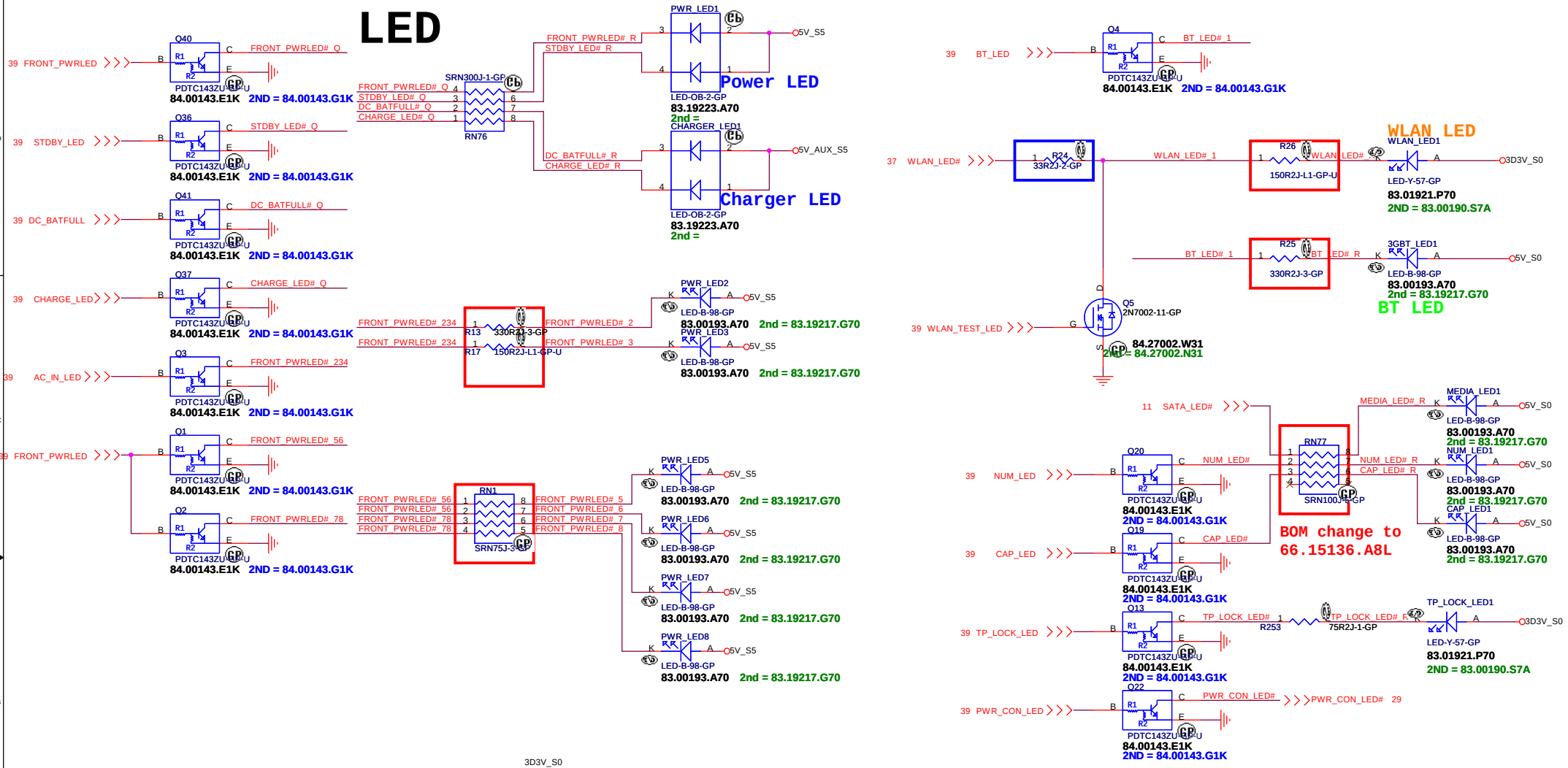
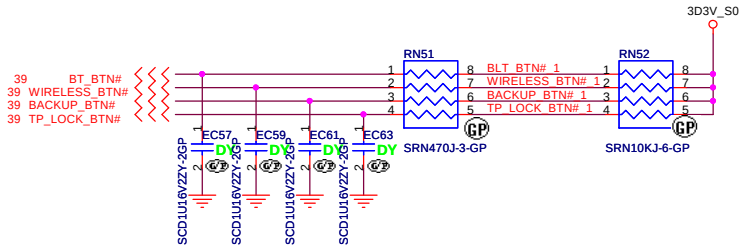
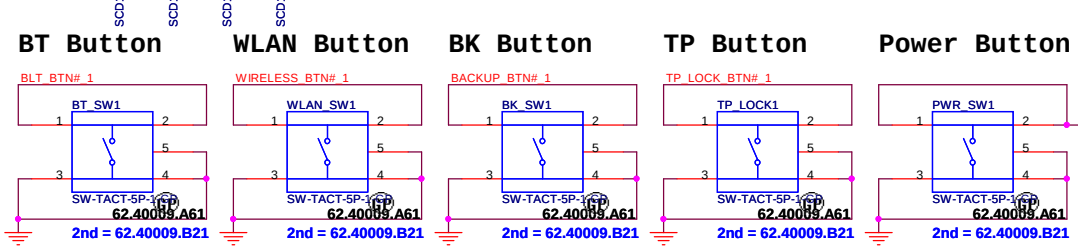
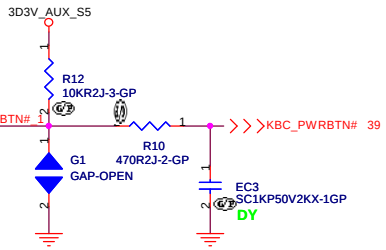
LED









JV70-CP

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Title: **LED&POWERBD CONN**

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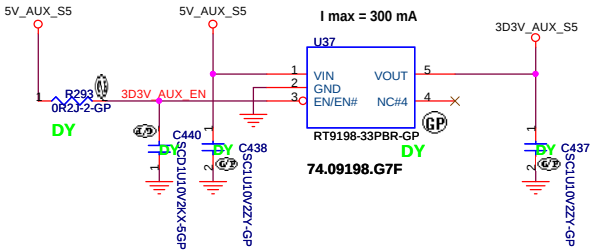
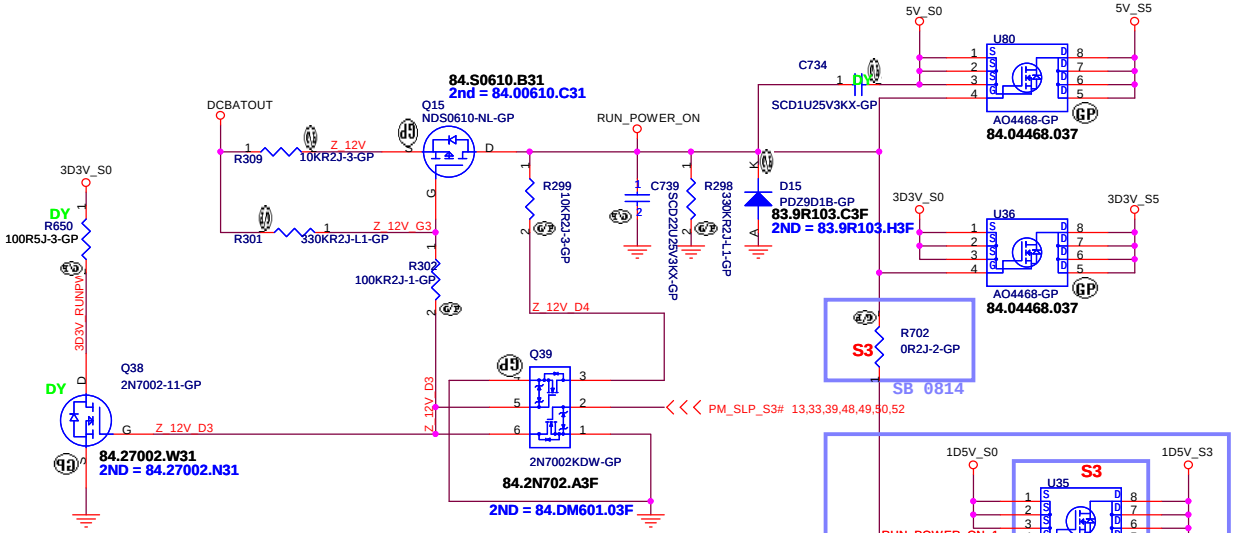
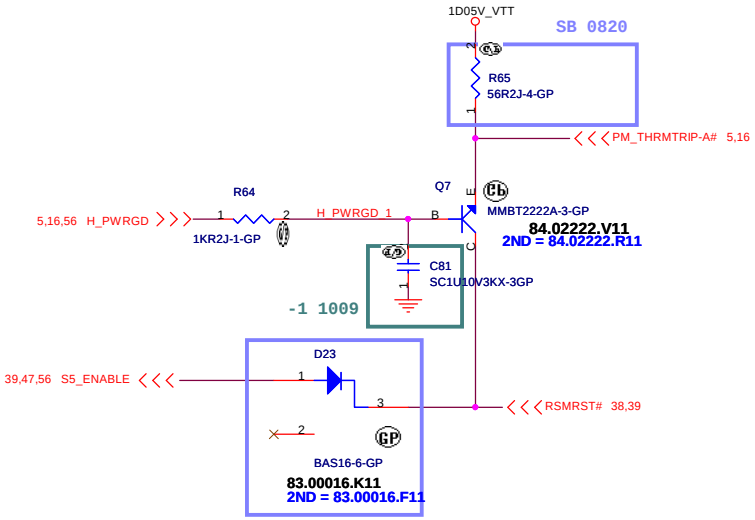
Aux Power

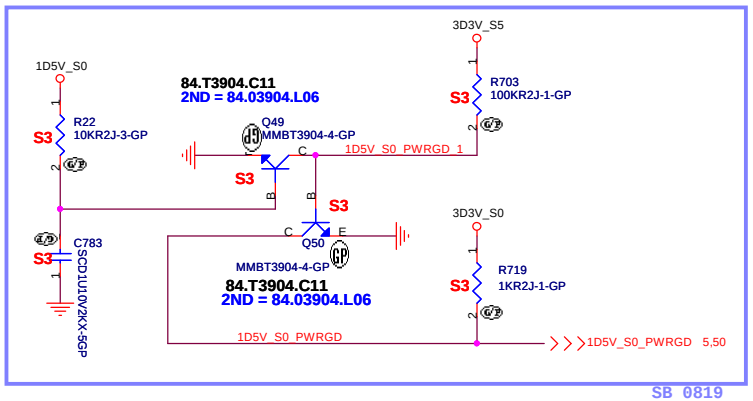
3D3V_AUX_S5

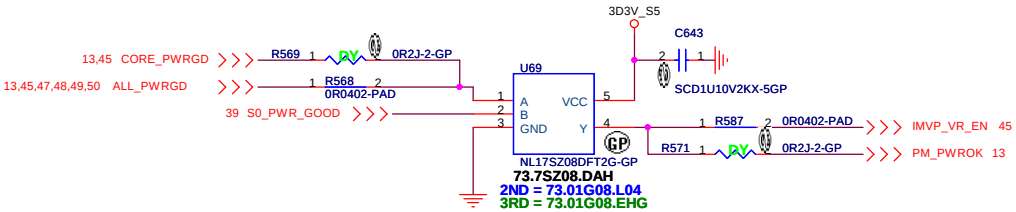


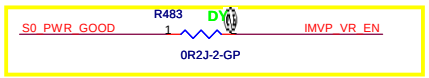
Run Power











JV70-CP

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Title: RUN POWER and 3D3V_AUX_S5

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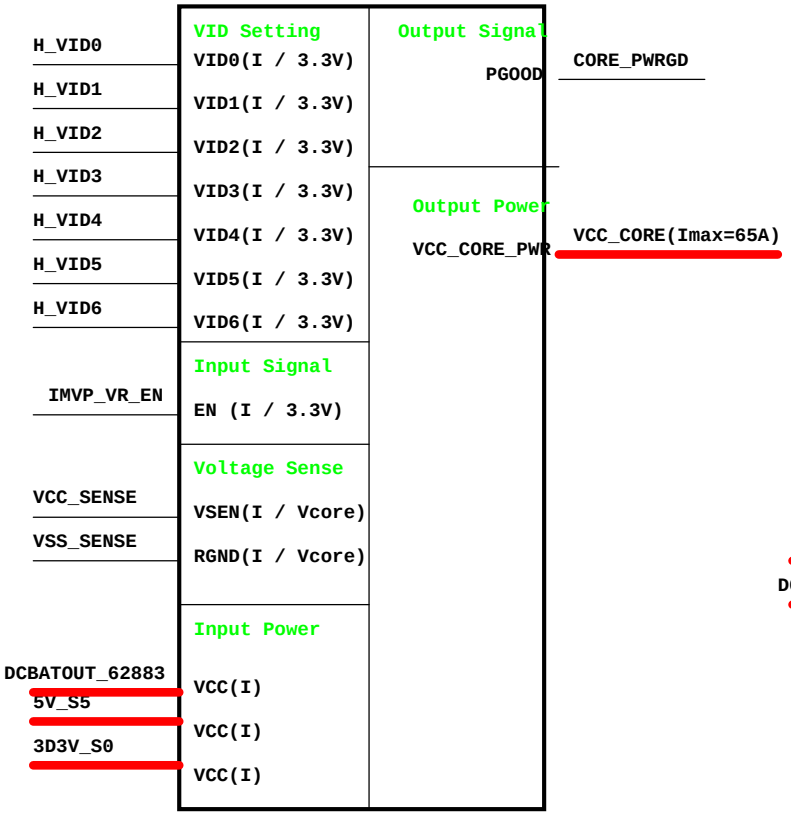
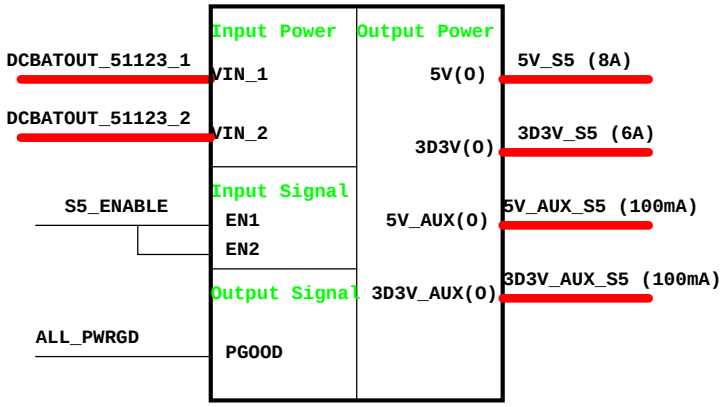
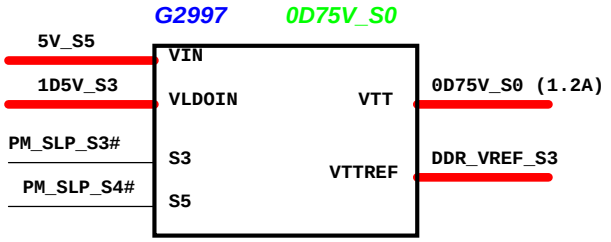
ISL62883 VCC_CORE



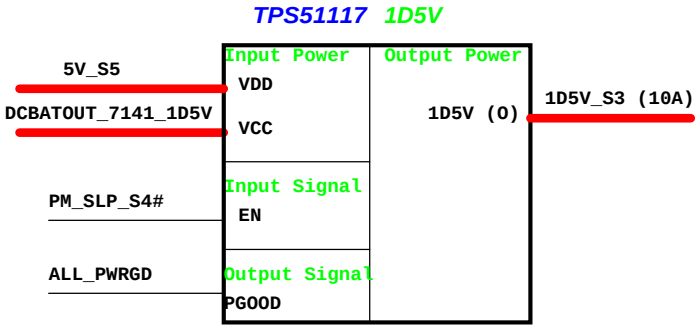
TPS51123 5V/3D3V



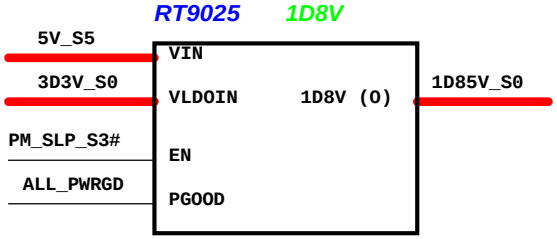
G2997 0D75V_S0



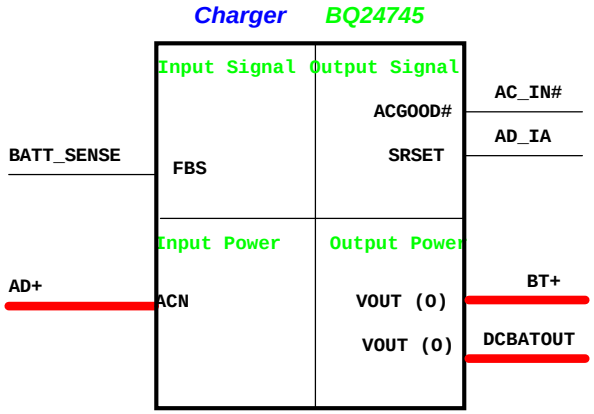
TPS51117 1D5V



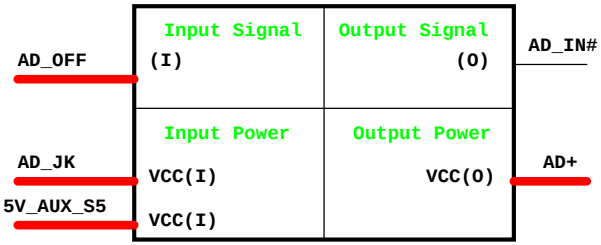
RT9025 1D8V



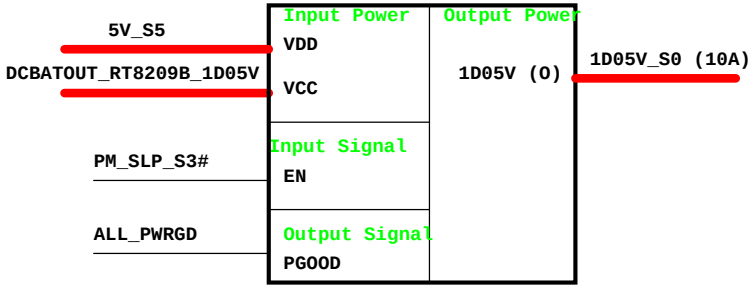
Charger BQ24745



Adapter



TPS51117 1D05V



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Title: **Power Block Diagram**

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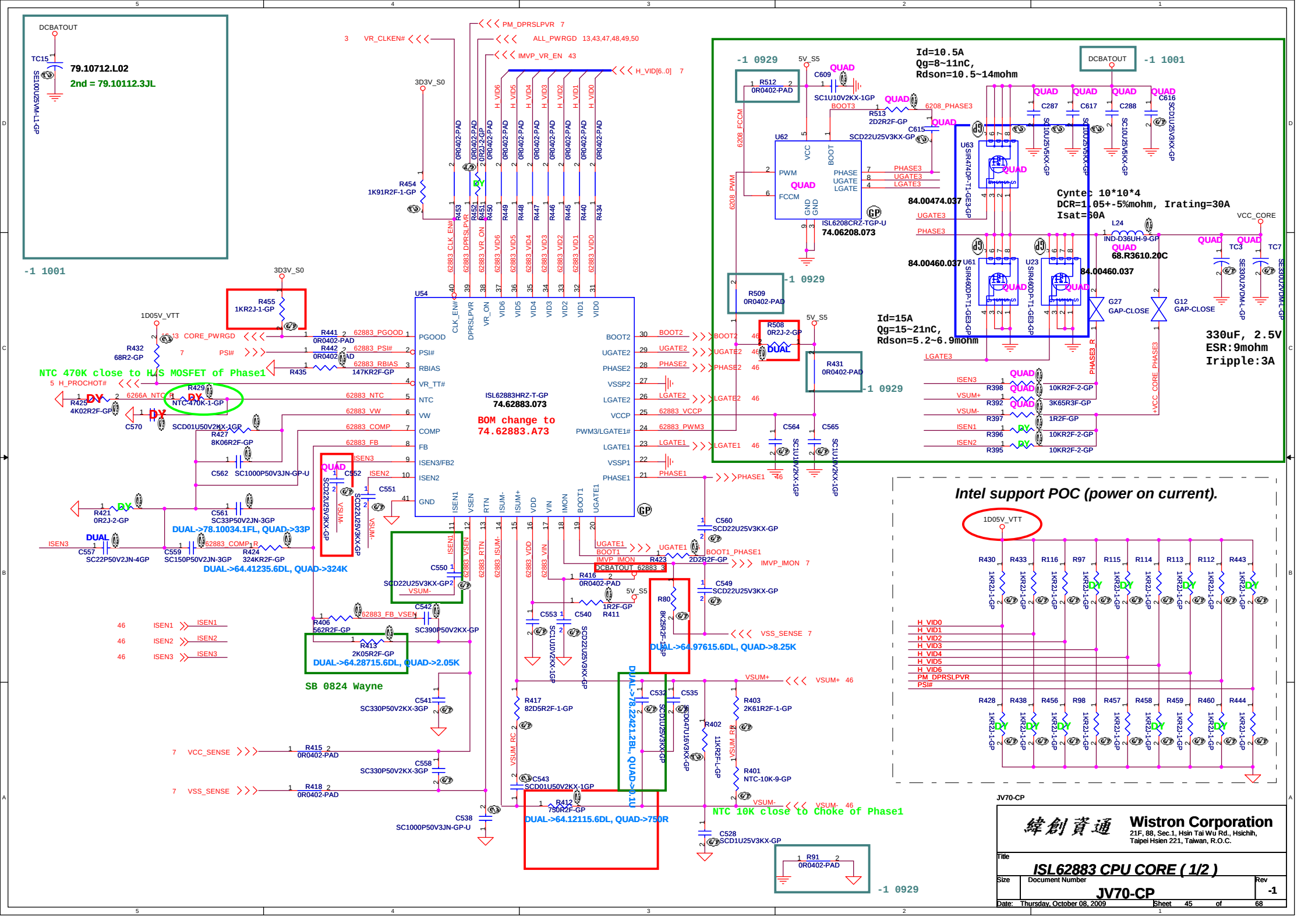
79.10712.L02
2nd = 79.10112.3JL
-1 1001
-1 0929
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=50A
84.00474.037
84.00460.037
ISL6208CRZ-TGP-U
74.06208.073
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
330uF, 2.5V
ESR:9mohm
Iripple:3A
ISL62883HRZ-T-GP
74.62883.073
BOM change to
74.62883.A73
NTC 470K close to H_S MOSFET of Phase1
DUAL->78.10034.1FL, QUAD->33P
DUAL->64.41235.6DL, QUAD->324K
DUAL->64.28715.6DL, QUAD->2.05K
SB 0824 Wayne
DUAL->64.97615.6DL, QUAD->8.25K
DUAL->78.22421.2BL, QUAD->0.1U
DUAL->64.12115.6DL, QUAD->750R
NTC 10K close to Choke of Phase1
Intel support POC (power on current).
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62883 CPU CORE (1/2)
JV70-CP
Thursday, October 08, 2009
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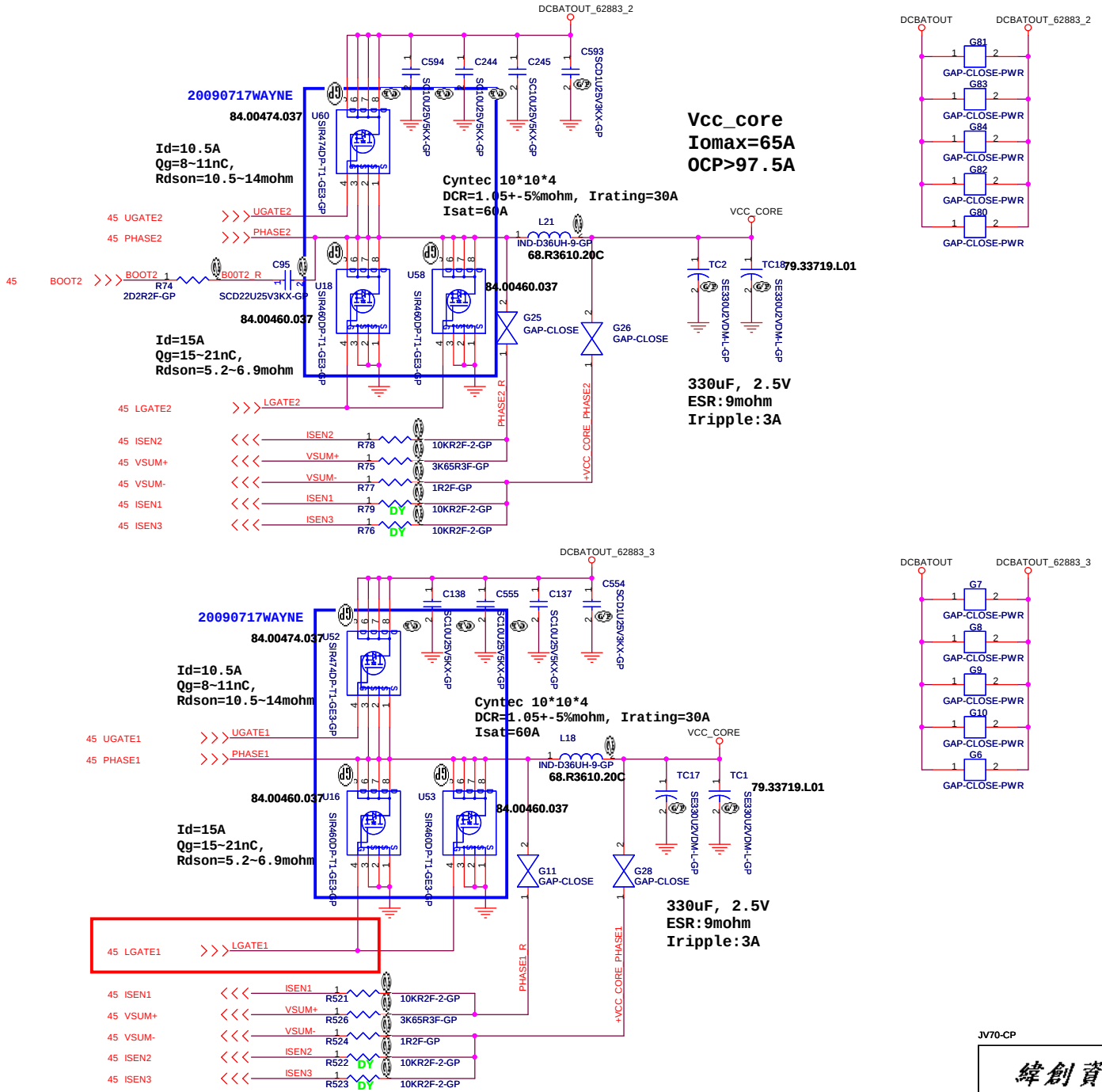
DCBATOUT_62883_2
20090717WAYNE
84.00474.037
U60
SIR474DP-T1-GE3-GP
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
C594
C244
C245
C593
SC10U25V5KX-GP
SCD1U25V3KX-GP
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=65A
OCP>97.5A
45 UGATE2
45 PHASE2
UGATE2
PHASE2
L21
IND-D36UH-9-GP
68.R3610.20C
VCC_CORE
45 BOOT2
BOOT2
R74
2D2R2F-GP
B00T2_R
C95
SCD22U25V3KX-GP
U18
U58
84.00460.037
SIR460DP-T1-GE3-GP
G25
GAP-CLOSE
G26
GAP-CLOSE
TC2
TC18
79.33719.L01
SE330U2VDM-L-GP
330uF, 2.5V
ESR:9mohm
Iripple:3A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
45 LGATE2
LGATE2
PHASE2_R
+VCC_CORE
PHASE2
45 ISEN2
45 VSUM+
45 VSUM-
45 ISEN1
45 ISEN3
ISEN2
VSUM+
VSUM-
ISEN1
ISEN3
R78
10KR2F-2-GP
R75
3K65R3F-GP
R77
1R2F-GP
R79
R76
DY
G81
G83
G84
G82
G80
GAP-CLOSE-PWR
DCBATOUT_62883_3
C138
C555
C137
C554
U52
U16
U53
G11
G28
TC17
TC1
45 UGATE1
45 PHASE1
45 LGATE1
45 ISEN1
45 VSUM+
45 VSUM-
45 ISEN2
45 ISEN3
R521
R526
R524
R522
R523
G7
G8
G9
G10
G6
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883 CPU CORE (1/2)
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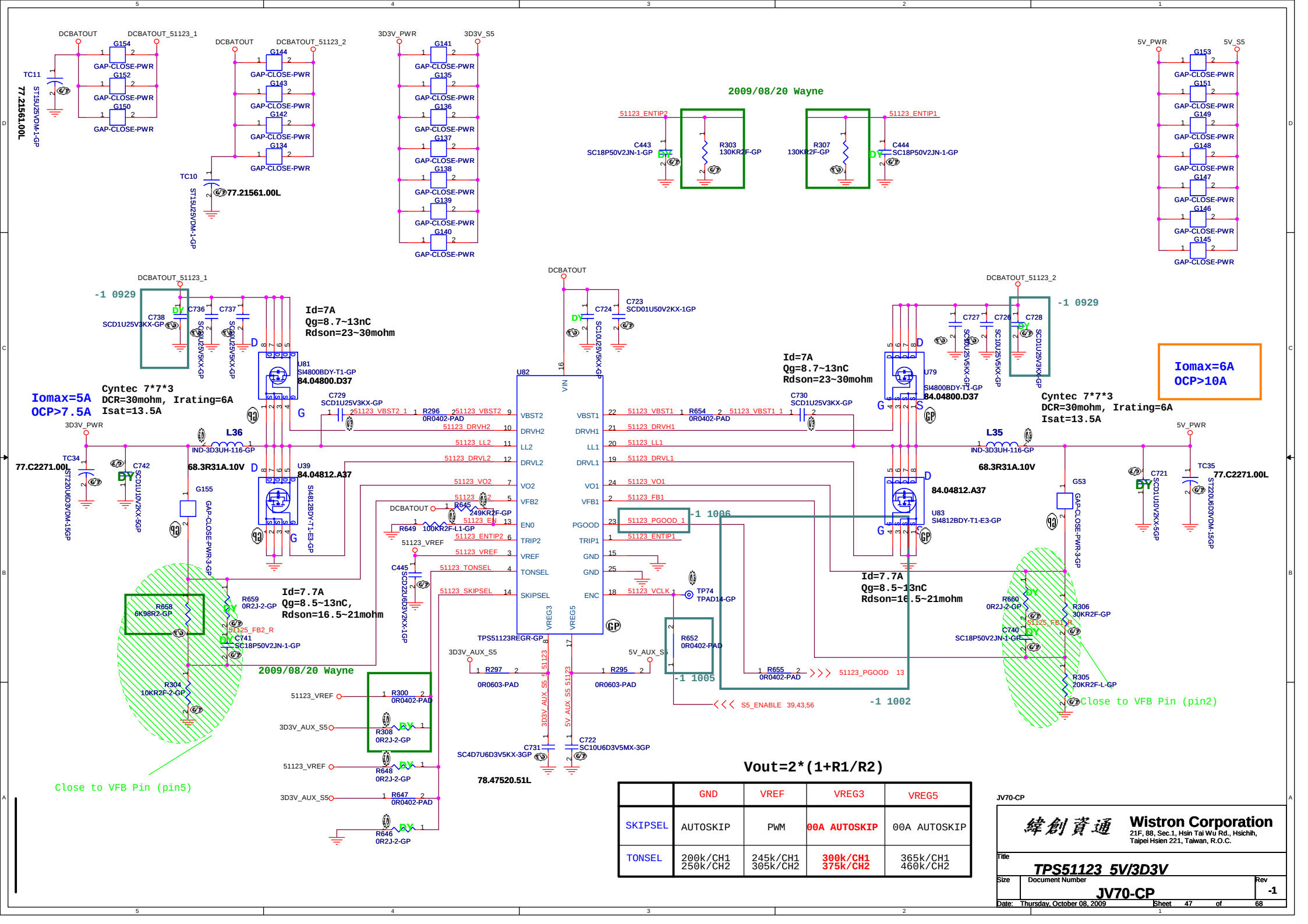

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

JV70-CP

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123 5V/3D3V

Size	Document Number	Rev
	JV70-CP	-1

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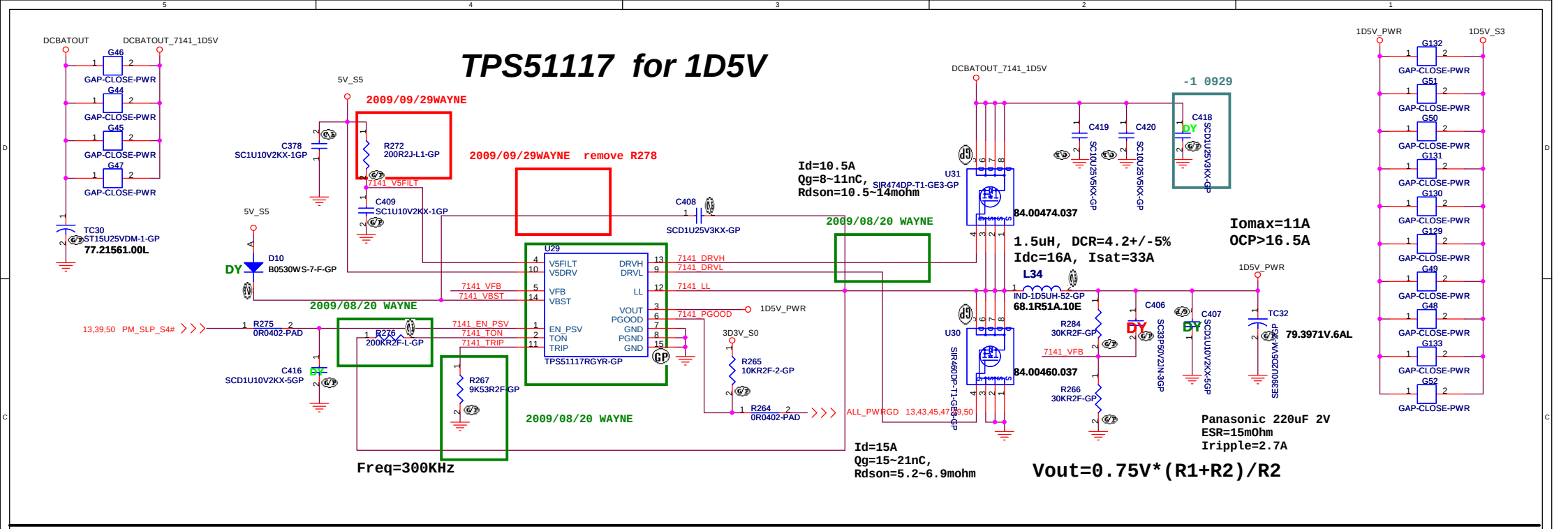

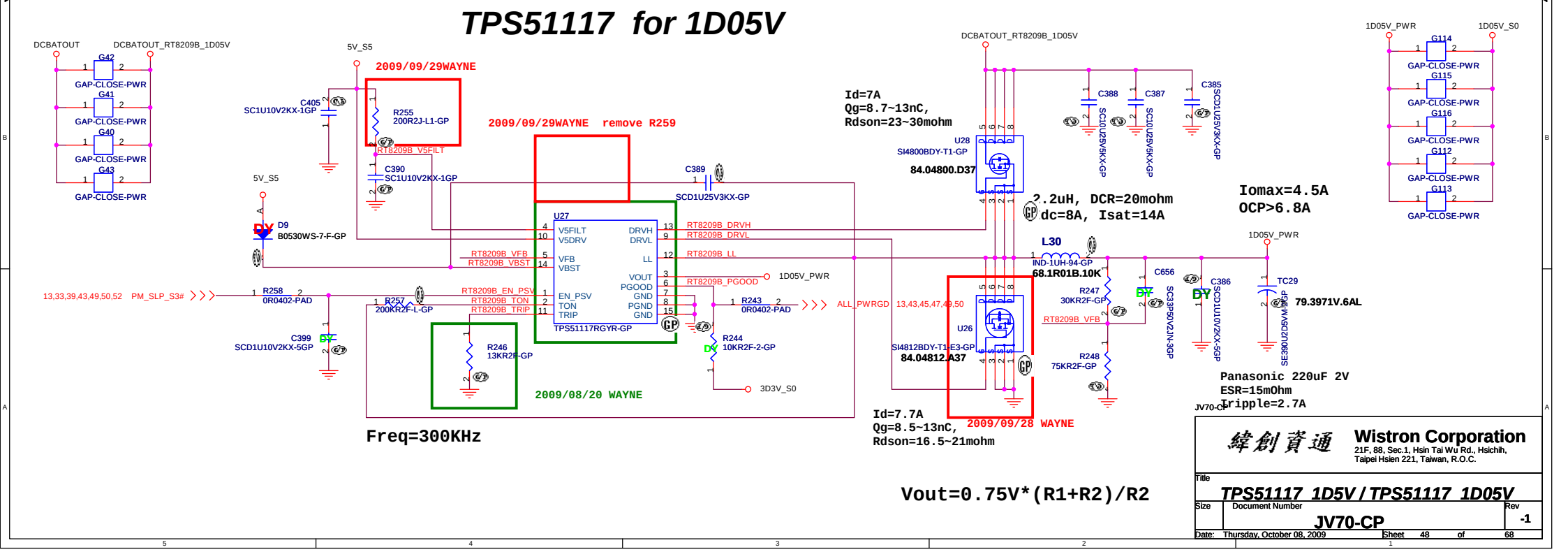

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51117_1D5V / TPS51117_1D05V***	
Size	Document Number: **JV70-CP**	Rev: -1
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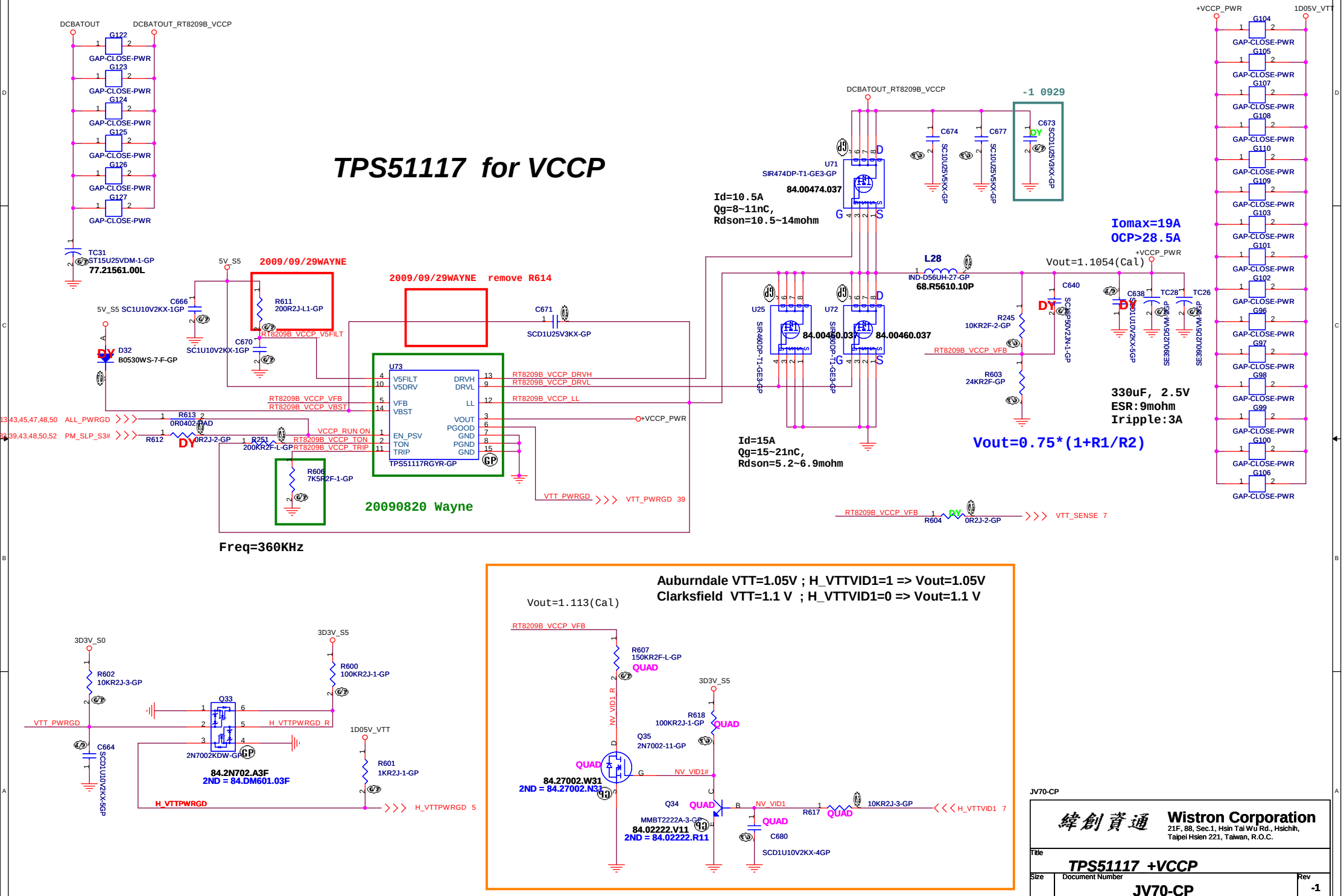
TPS51117 for VCCP



JV70-CP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 +VCCP

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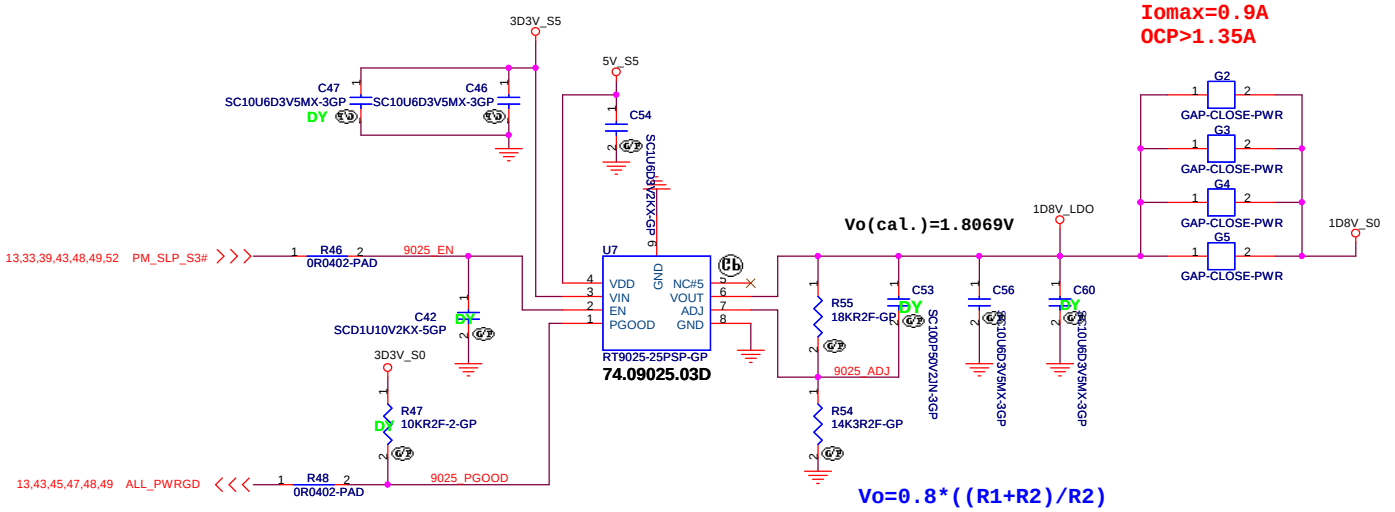
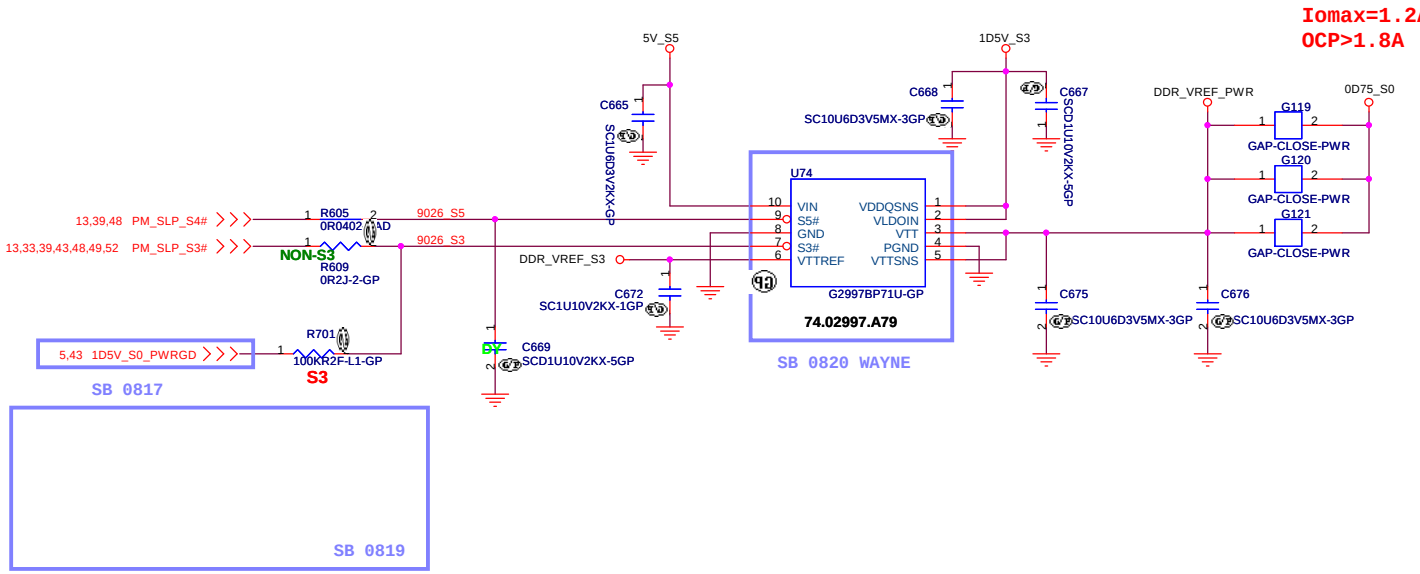
RT9025 for 1D8V_S0



G2997 for 0D75V_S3



JV70-CP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V/G2997_0D75

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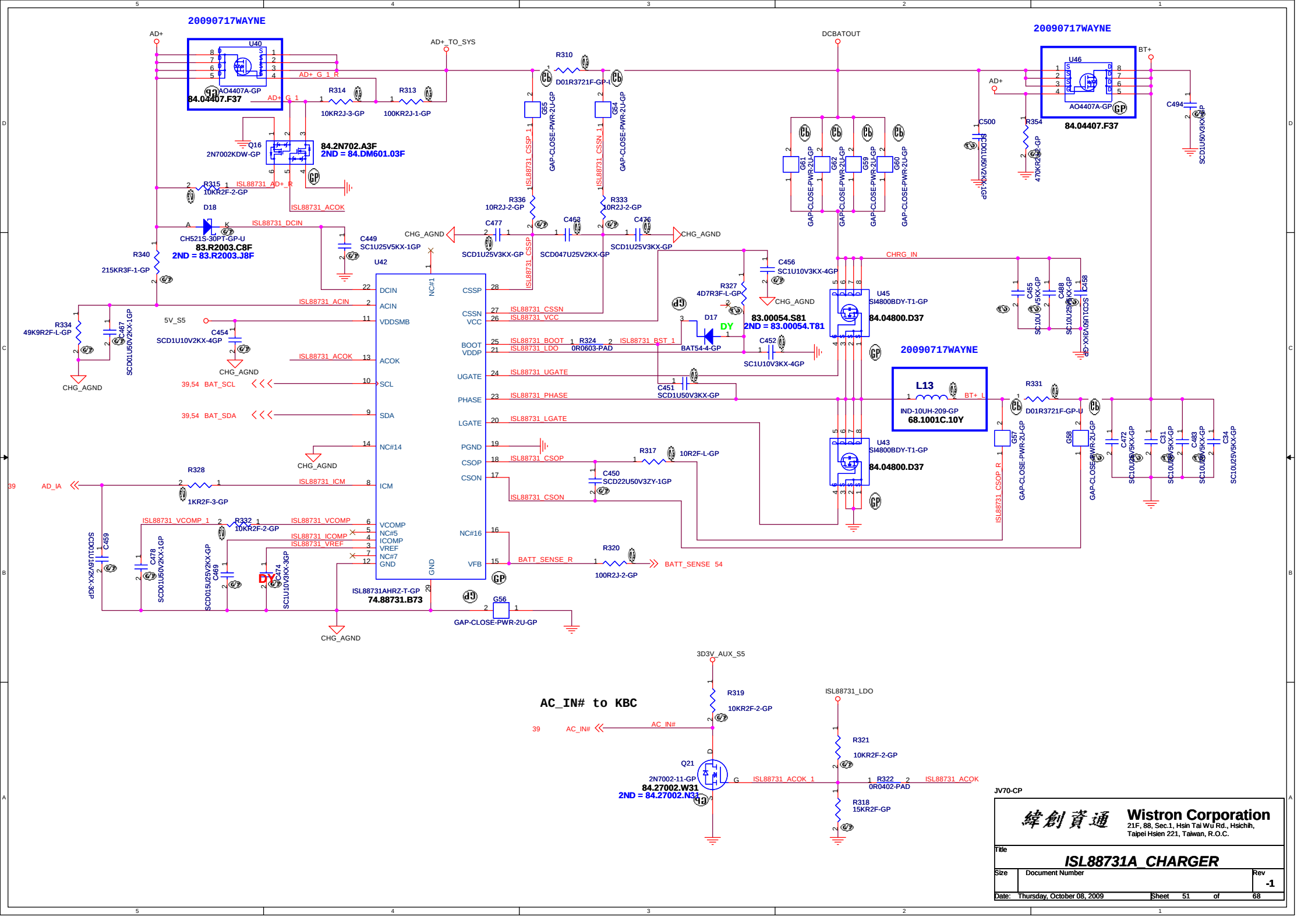
20090717WAYNE
AD+
U40
AO4407A-GP
84.04407.F37
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R314
10KR2J-3-GP
R313
100KR2J-1-GP
Q16
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R315
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D18
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
ISL88731_DCIN
R340
215KR3F-1-GP
C449
SC1U25V5KX-1GP
U42
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
74.88731.B73
R334
49K9R2F-L-GP
C467
SCD01U50V2KX-1GP
5V_S5
C454
SC1U10V2KX-4GP
CHG_AGND
39,54 BAT_SCL
39,54 BAT_SDA
R328
1KR2F-3-GP
AD_IA
ISL88731_VCOMP_1
R332
10KR2F-2-GP
C459
C478
C469
SCD015U25V2KX-GP
C474
SC1U10V3KX-3GP
DY
G56
GAP-CLOSE-PWR-2U-GP
R310
D01R3721F-GP-U
G55
G54
GAP-CLOSE-PWR-2U-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
R336
10R2J-2-GP
R333
10R2J-2-GP
C477
SCD1U25V3KX-GP
C463
SCD047U25V2KX-GP
C476
SCD1U25V3KX-GP
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
R324
0R0603-PAD
ISL88731_BST_1
D17
BAT54-4-GP
C452
SC1U10V3KX-4GP
C451
SCD1U50V3KX-GP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R317
10R2F-L-GP
C450
SCD22U50V3ZY-1GP
ISL88731_ICM
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
R320
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 54
DCBATOUT
GAP-CLOSE-PWR-2U-GP
C456
SC1U10V3KX-4GP
CHRG_IN
R327
4D7R3F-L-GP
83.00054.S81
2ND = 83.00054.T81
U45
SI4800BDY-T1-GP
84.04800.D37
U43
SI4800BDY-T1-GP
84.04800.D37
L13
IND-10UH-209-GP
68.1001C.10Y
BT+_L
R331
D01R3721F-GP-U
ISL88731_CSOP_R
C455
C488
C458
SC10U25V6KX-GP
SCD1U50V3KX-GP
U46
AO4407A-GP
84.04407.F37
BT+
C494
SCD1U50V3KX-GP
C500
SCD01U50V2KX-1GP
R354
470KR2J-GP
C472
C31
C483
C34
SC10U25V5KX-GP
3D3V_AUX_S5
AC_IN# to KBC
R319
10KR2F-2-GP
AC_IN#
Q21
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N33
ISL88731_ACOK_1
R321
10KR2F-2-GP
R322
0R0402-PAD
ISL88731_ACOK
R318
15KR2F-GP
ISL88731_LDO
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
Size
Document Number
Rev
-1
Date: Thursday, October 08, 2009
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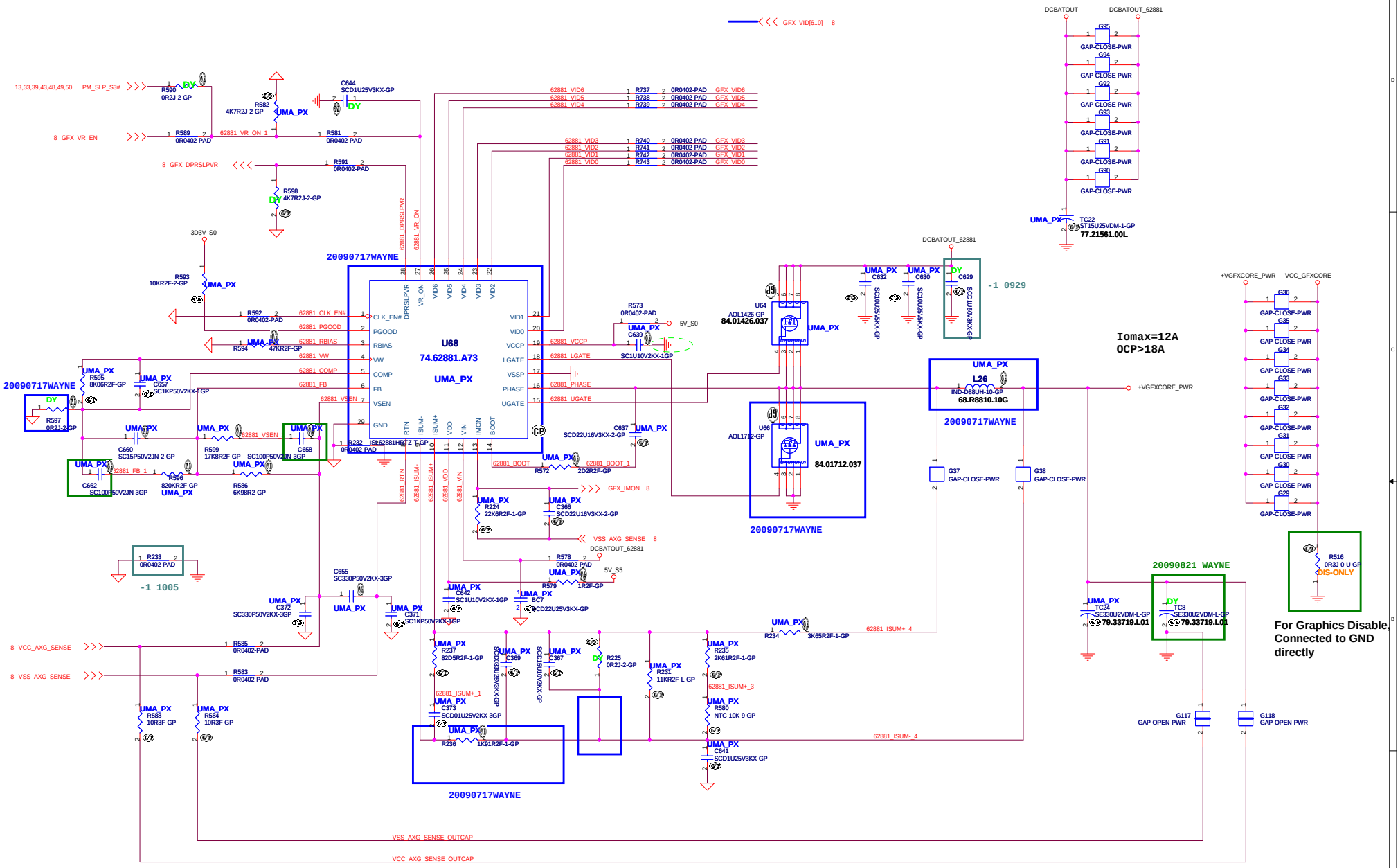

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881_+VCC_GFXCORE

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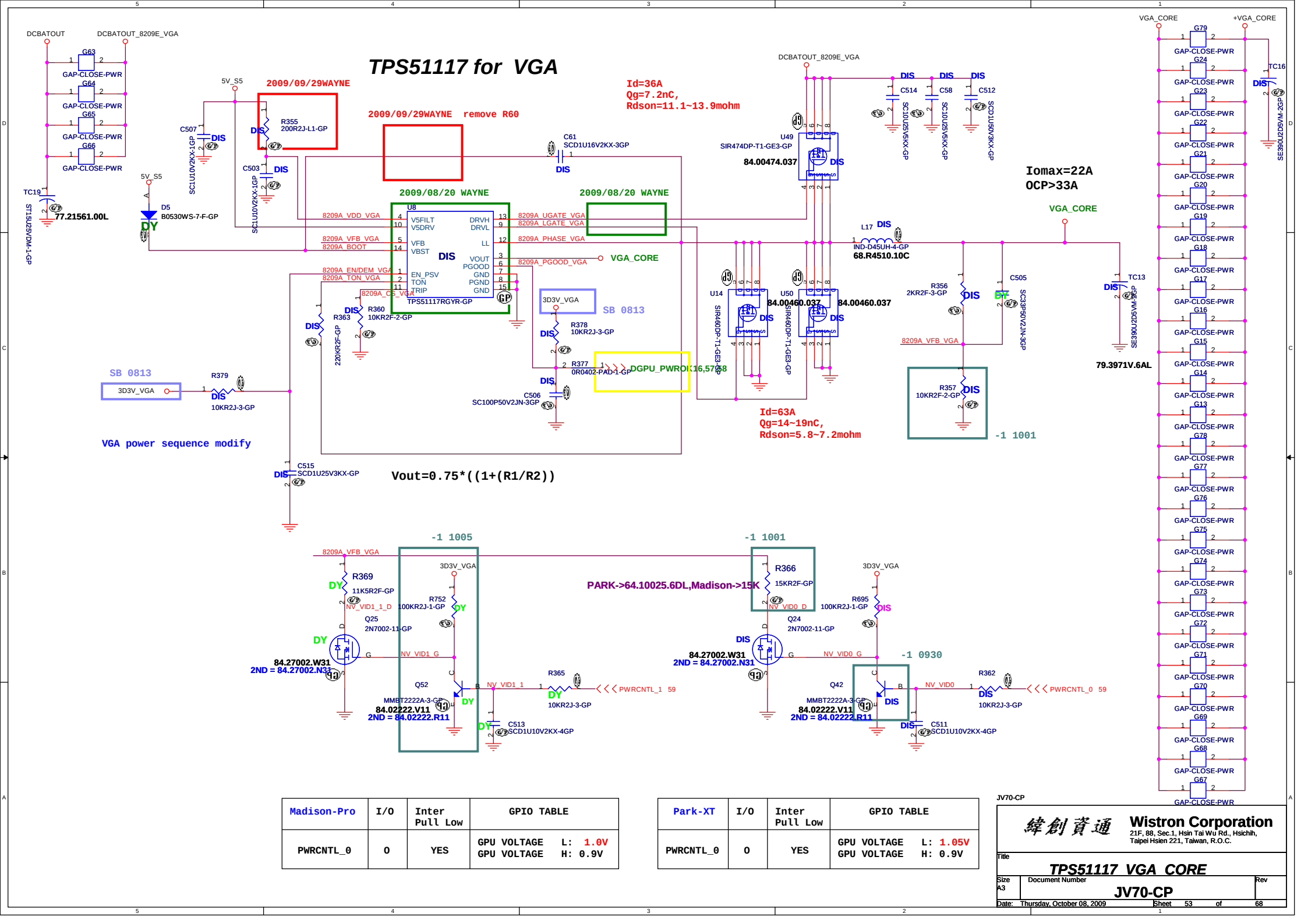

Madison-Pro	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.0V GPU VOLTAGE H: 0.9V

Park-XT	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.9V

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 VGA CORE

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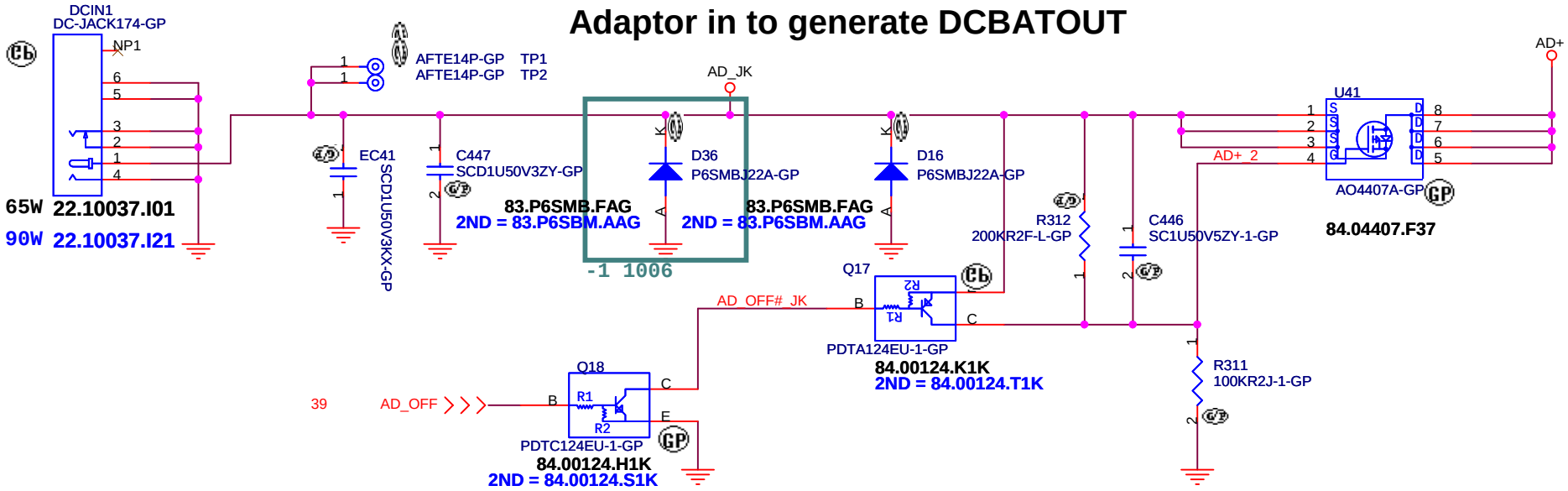
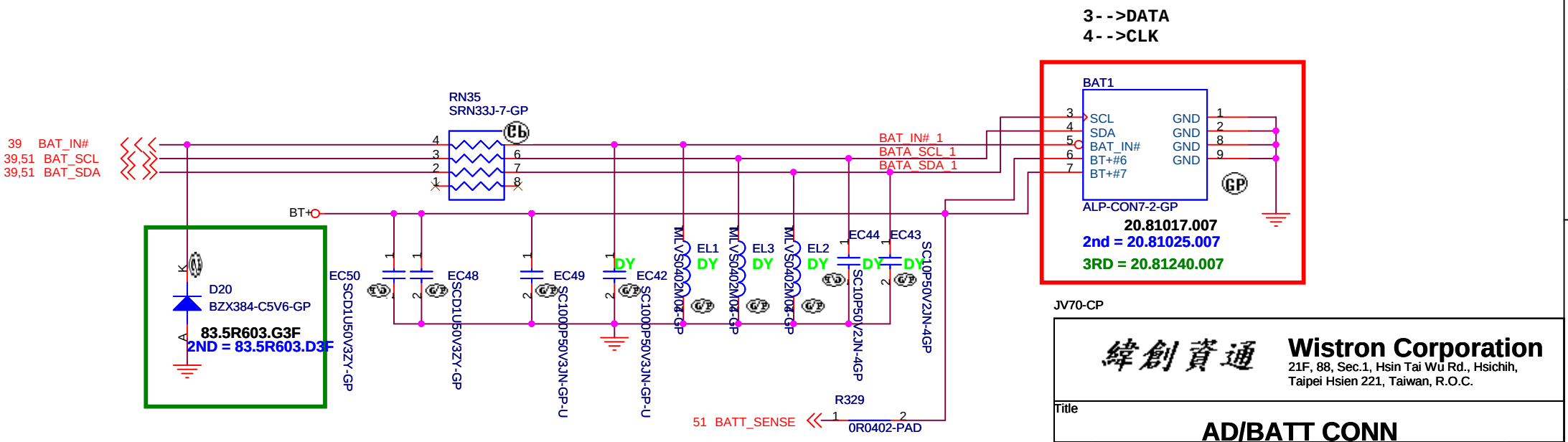
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

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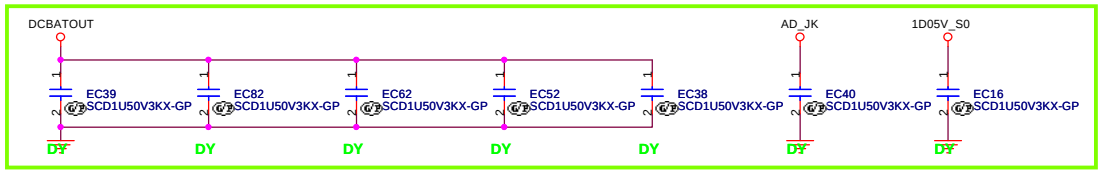
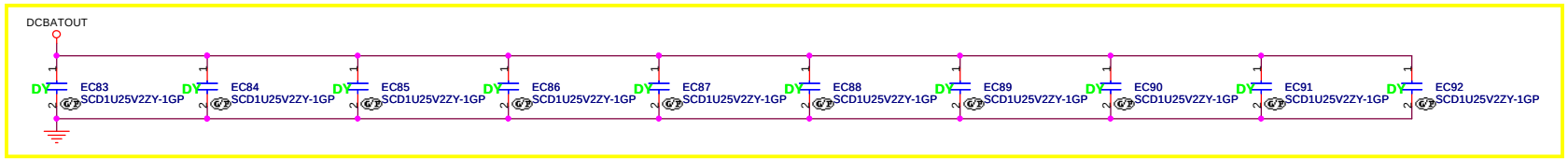
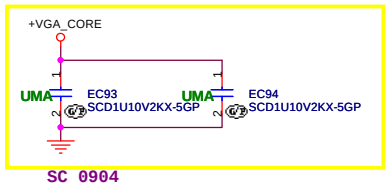
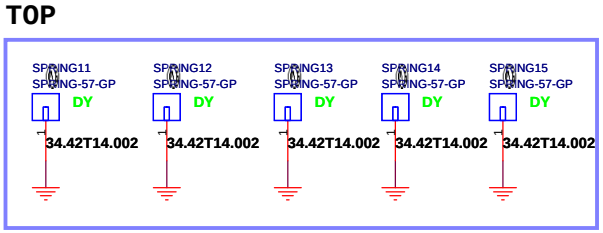
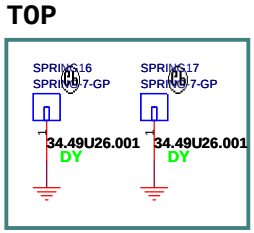


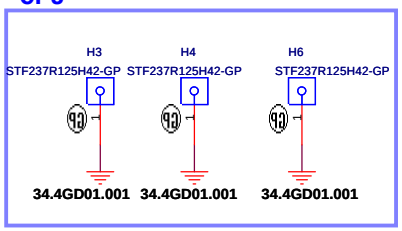


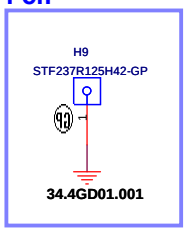


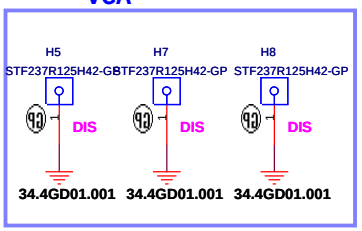


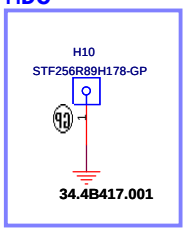


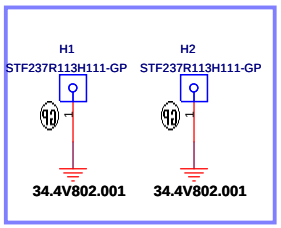
H1~H10 ALL IN TOP SIDE

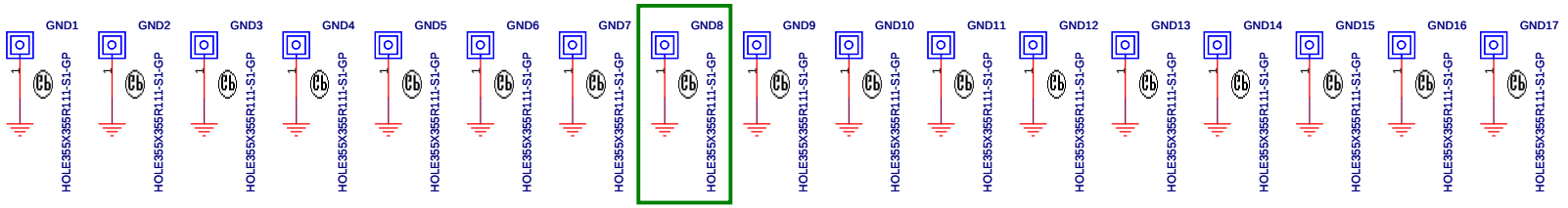


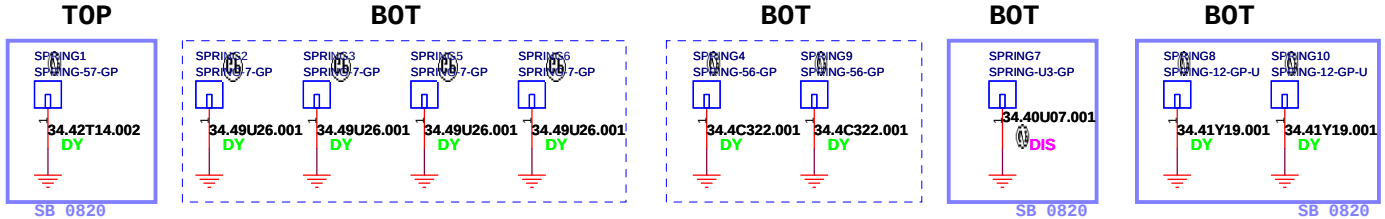












JV70-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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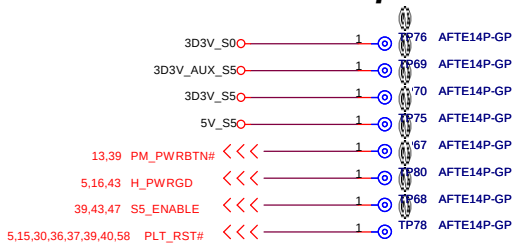
Check test point



Test Point放在Dimm Door打開可量測處

JV70-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AFTE_TP***	
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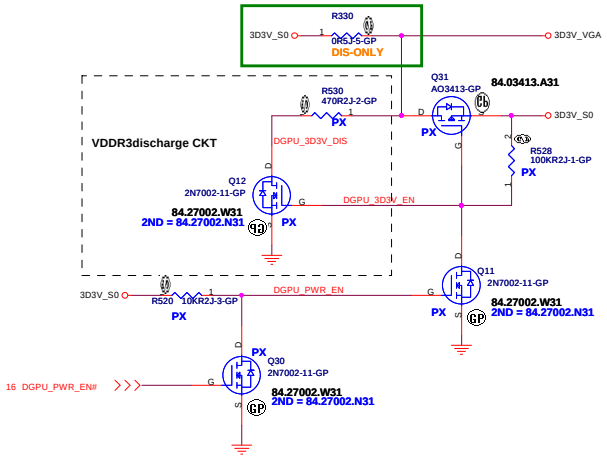
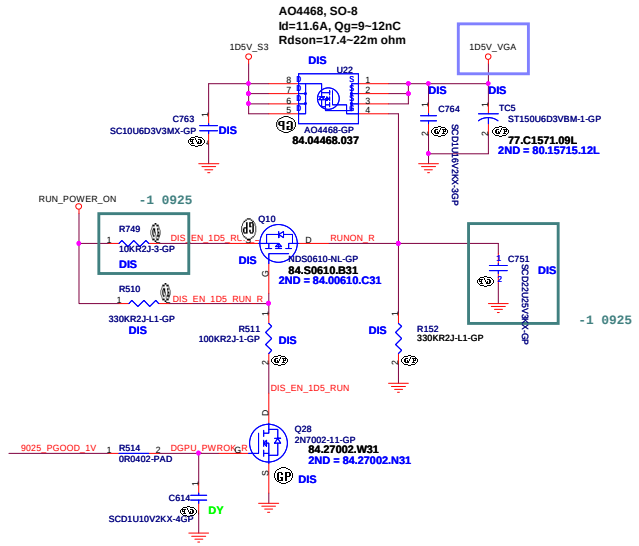
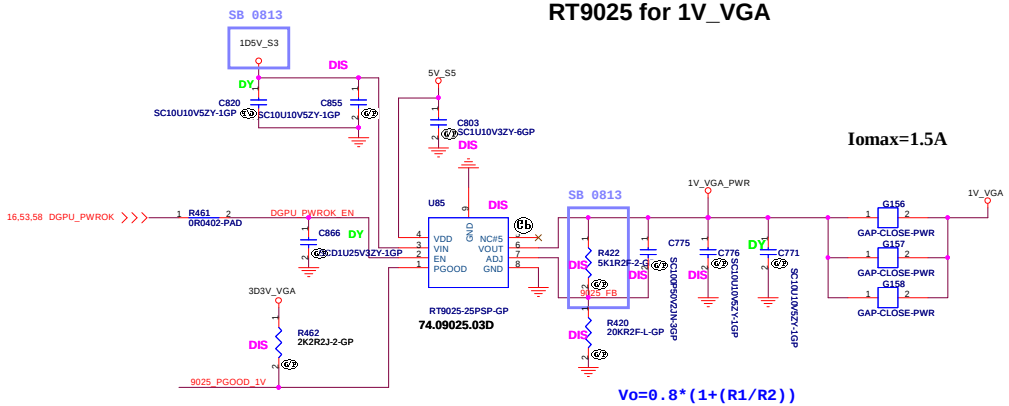
+3VS to 3.3V_DELAY Transfer

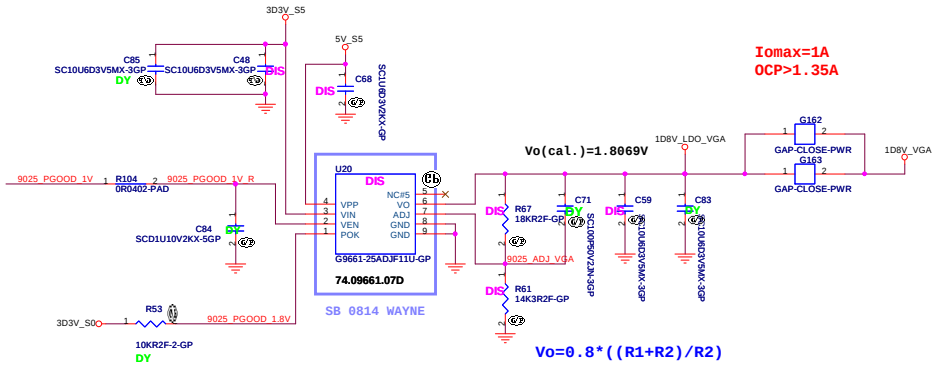




RT9025 for 1V_VGA



G9661 for 1D8V_VGA



JV70-CP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

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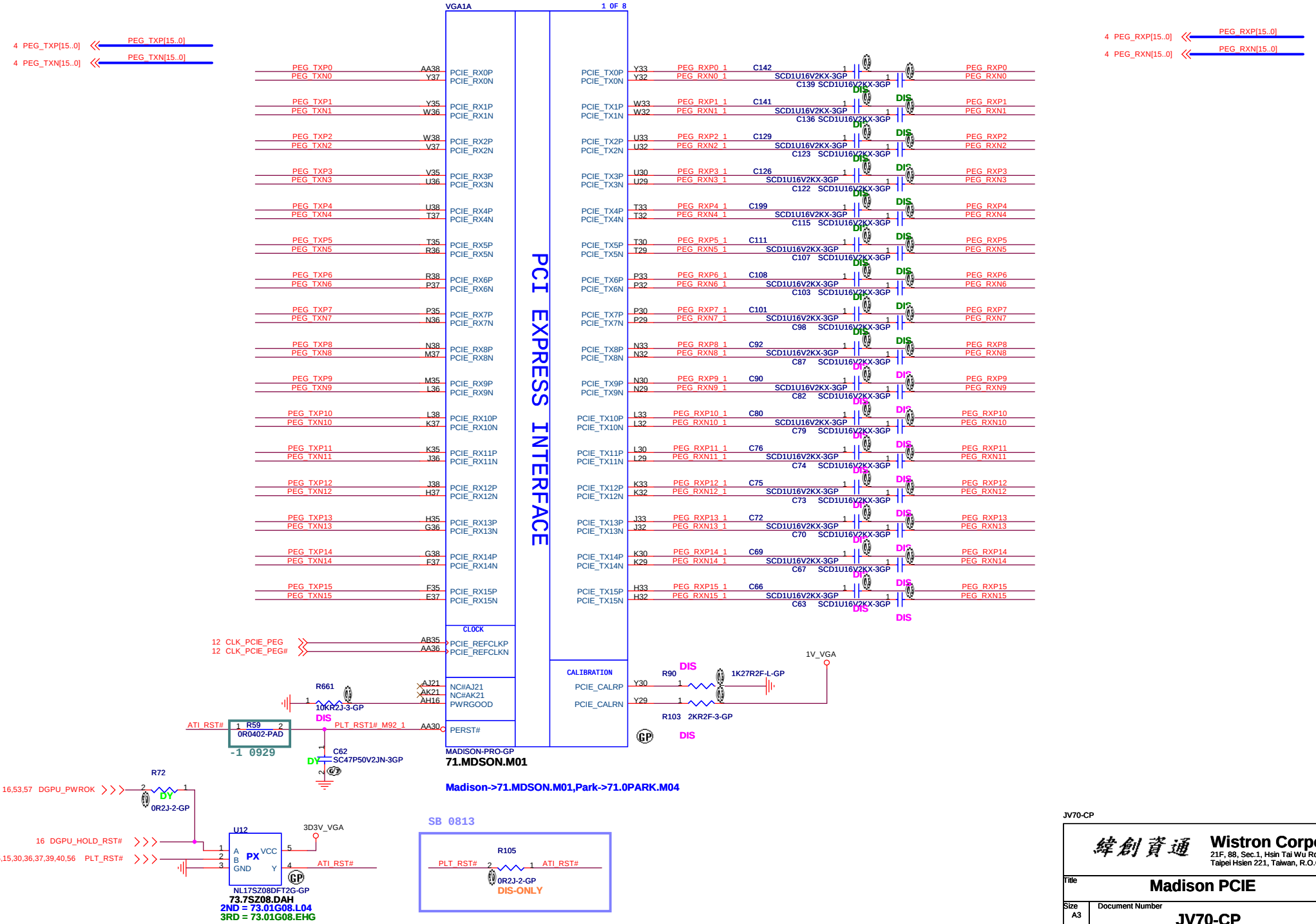
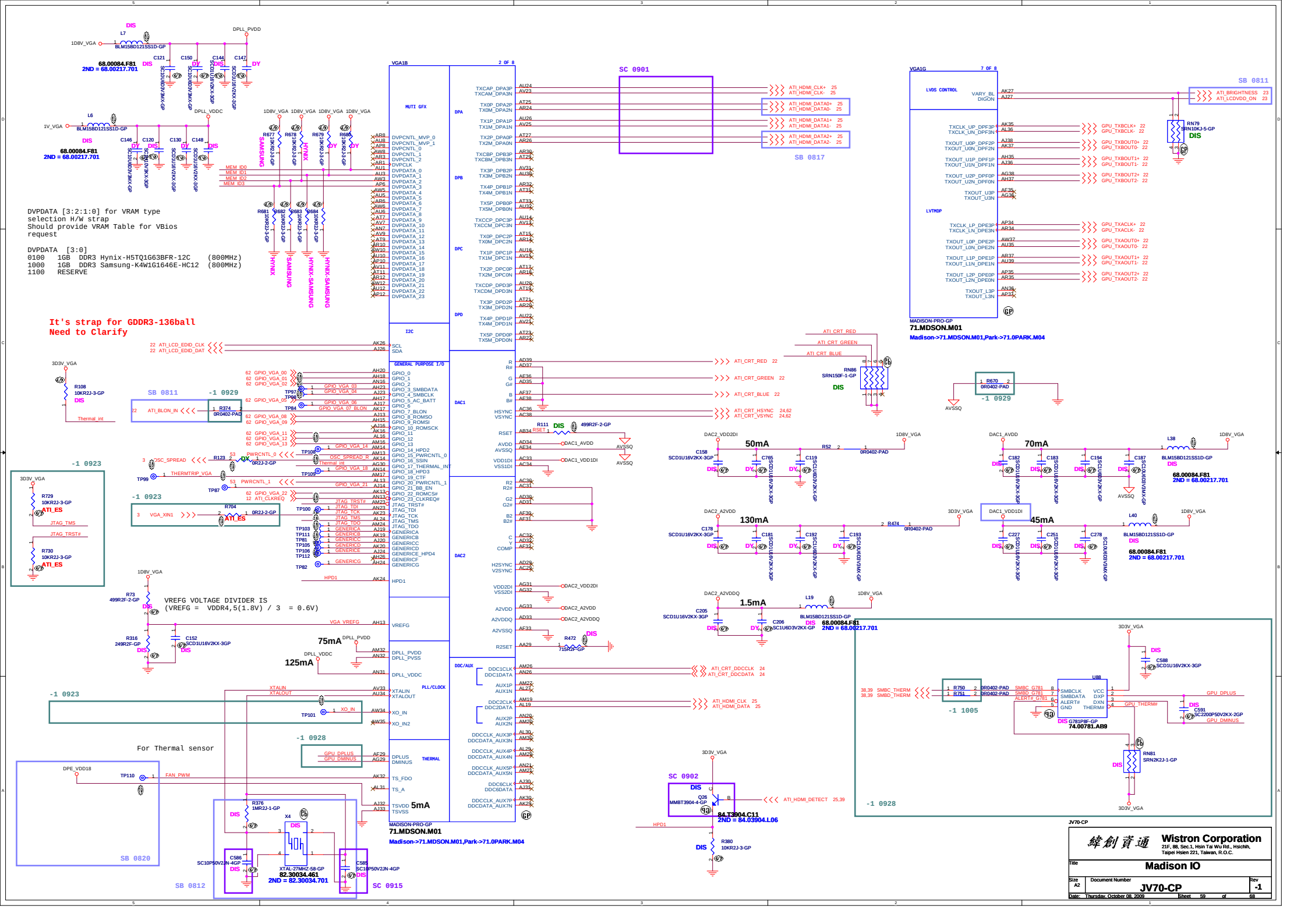
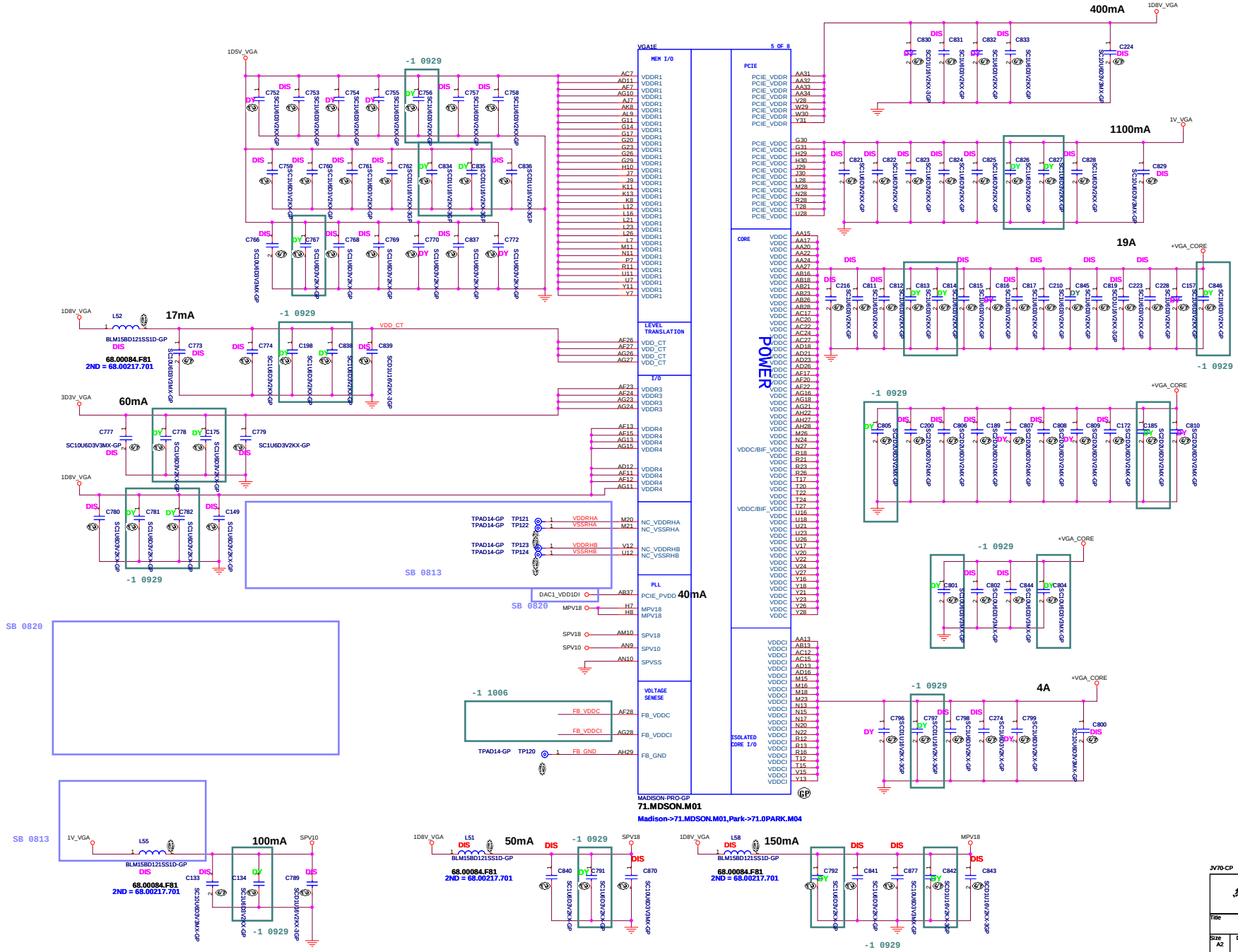


JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **Madison PCIE**		
Size: A3	Document Number: **JV70-CP**	Rev: -1
Date: Friday, October 09, 2009	Sheet 58 of 68	


DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 1GB DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
1000 1GB DDR3 Samsung-K4W1G1646E-HC12 (800MHz)
1100 RESERVE
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
SC 0901
SC 0902
SC 0915
SB 0811
SB 0812
SB 0817
SB 0820
71.MDSON.M01
Madison->71.MDSON.M01,Park->71.0PARK.M04
82.30034.461
2ND = 82.30034.701
84.T3904.C11
2ND = 84.03904.L06
74.00781.AB9
68.00084.F81
2ND = 68.00217.701
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison IO
JV70-CP
Rev -1
Thursday, October 08, 2009


400mA
1100mA
19A
17mA
60mA
40mA
4A
100mA
50mA
150mA
-1 0929
-1 1006
SB 0813
SB 0820
VGA1E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
MADISON-PRO-GP
71.MDSON.M01
Madison->71.MDSON.M01,Park->71.0PARK.M04
68.00084.F81
2ND = 68.00217.701
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
Size A2
Document Number JV70-CP
Rev -1
Date: Thursday, October 08, 2009
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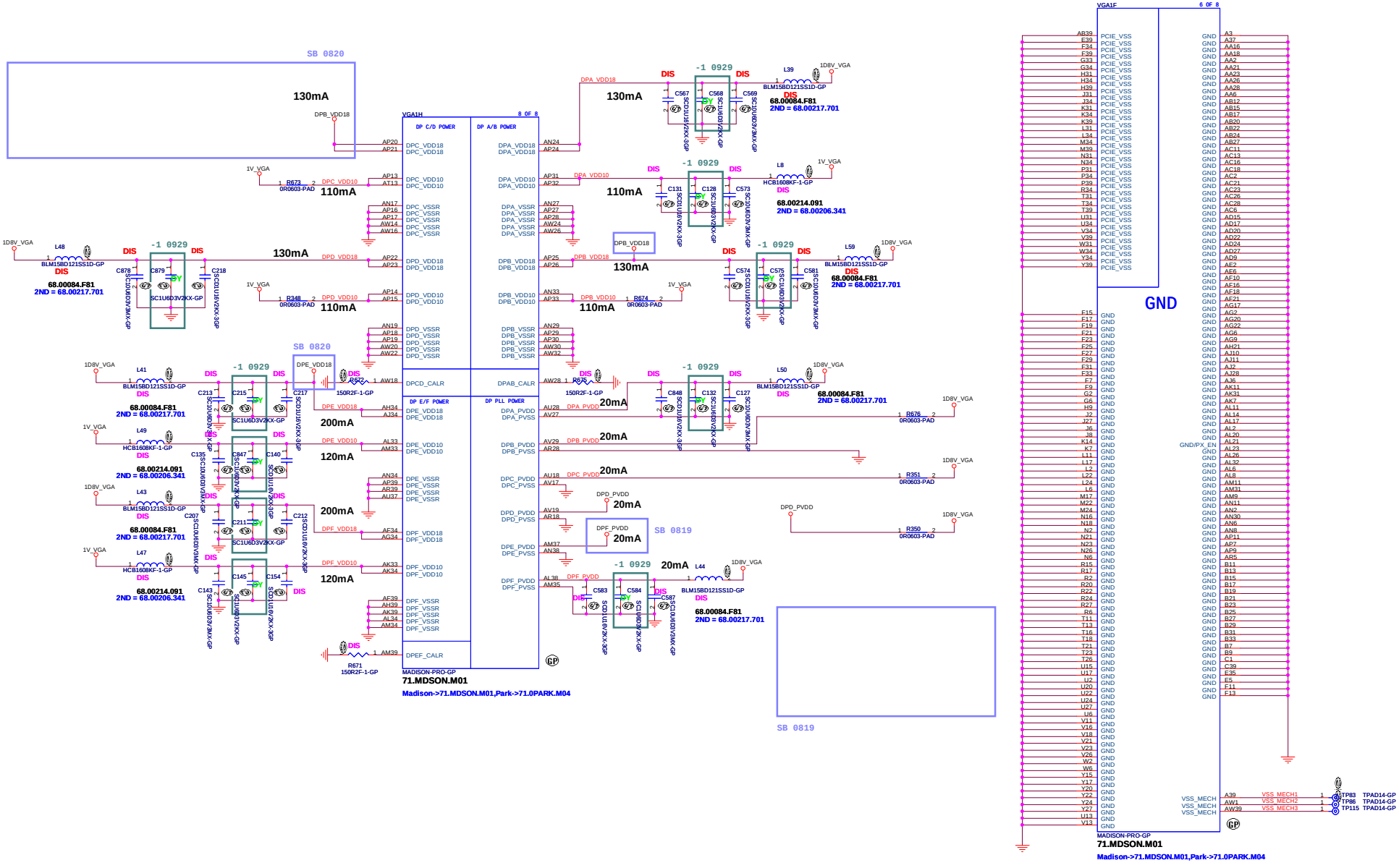

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DP POWER_GND

Size	Document Number	Rev
A2	JV70-CP	-1

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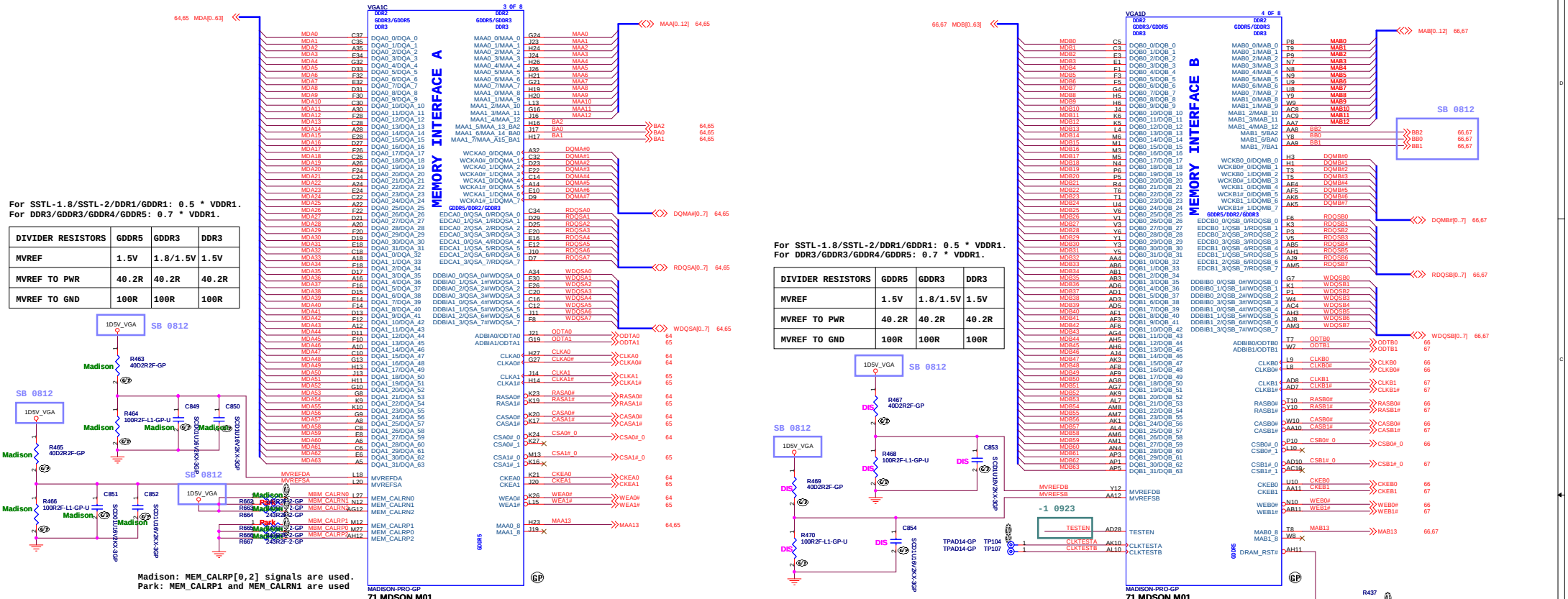


For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

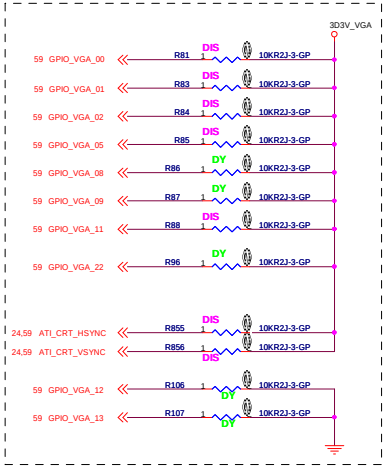
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

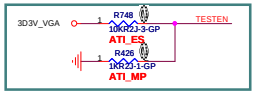
If BIOS_ROM_EN (GPIO22) = 0			If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures		GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	M25P05A	0100
	256MB	x001		M25P10A	0101
	64MB	x010		M25P20	0101
	32MB	x		M25P40	0101
	512MB	x		M25P80	0101
	1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
	2GB	x		Pm25LV010A	0101
	4GB	x			

HW STRAP PIN



Designator		For M97-M2	For Mannhatton
R_MEM_1	R471	10K	10K
R_MEM_2	R437	0R/Short	680R
R_MEM_3		DY	DY
C_MEM	C889	2.2nF	68pF

-1 0923



JV70-CP

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

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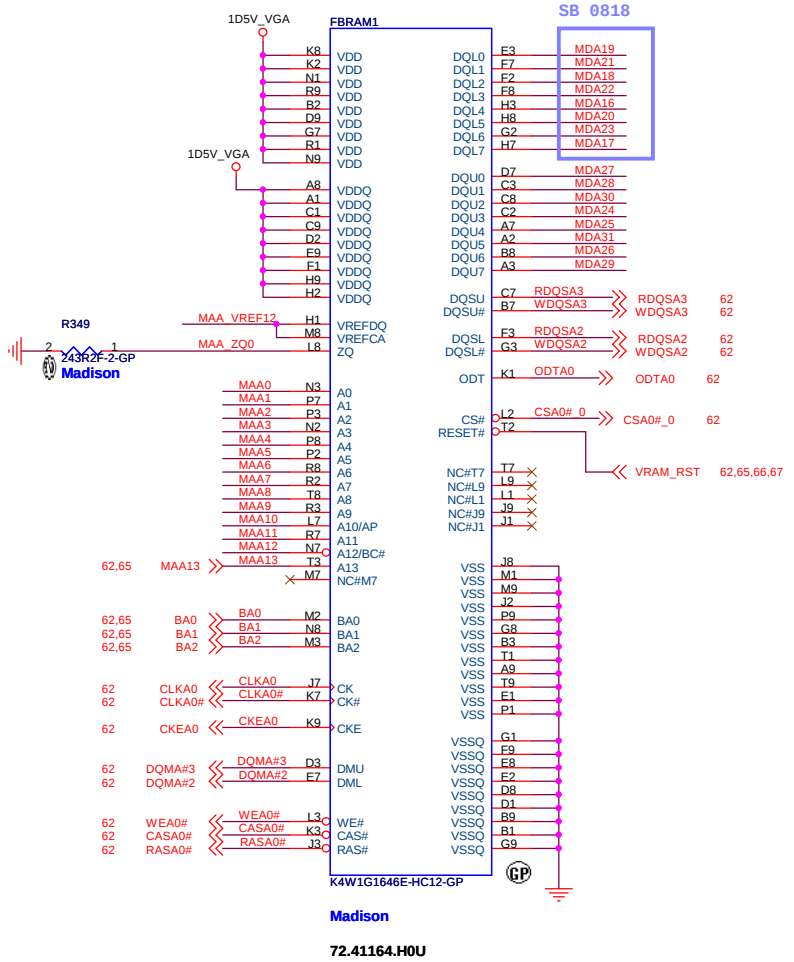
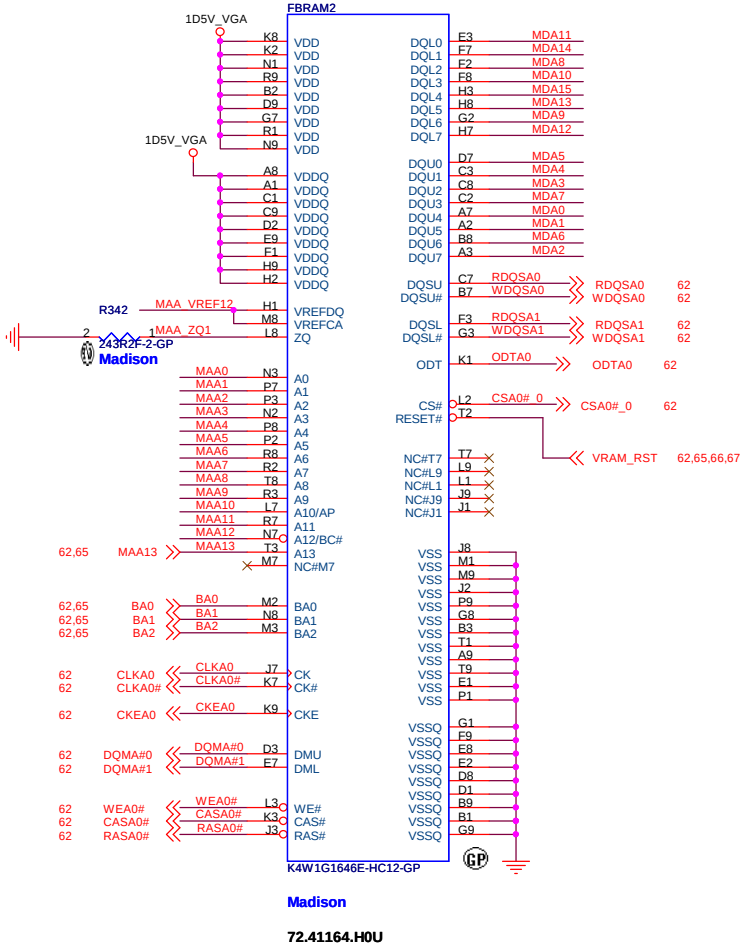
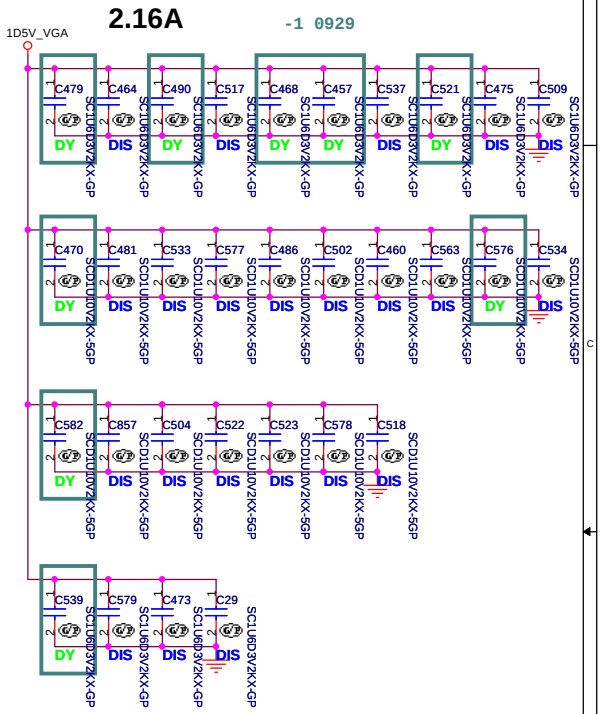
DDR3

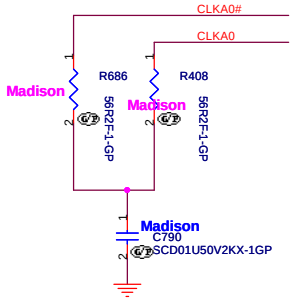


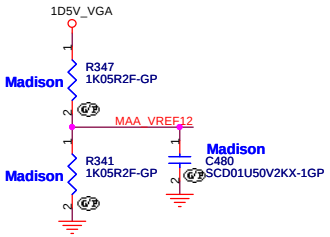




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

62,65 DQMA#[0..7]
62,65 RDQSA[0..7]
62,65 WDQSA[0..7]
62,65 MAA[0..12] MAA[0..12]
62,65 MDA[0..63] MDA[0..63]





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Title	*VRAM(1/4)*	
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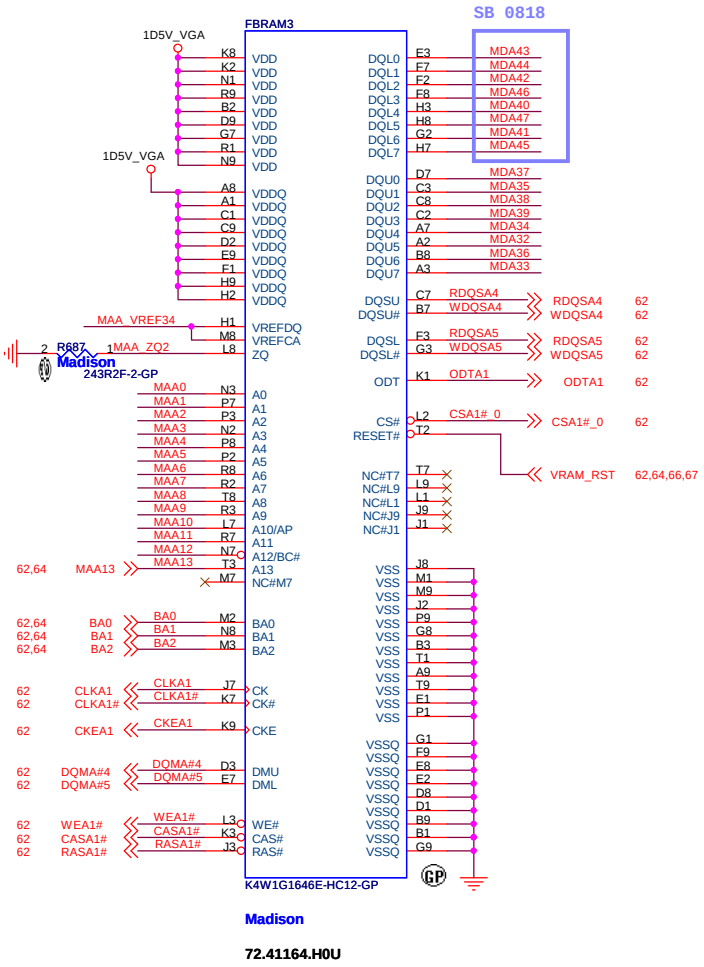
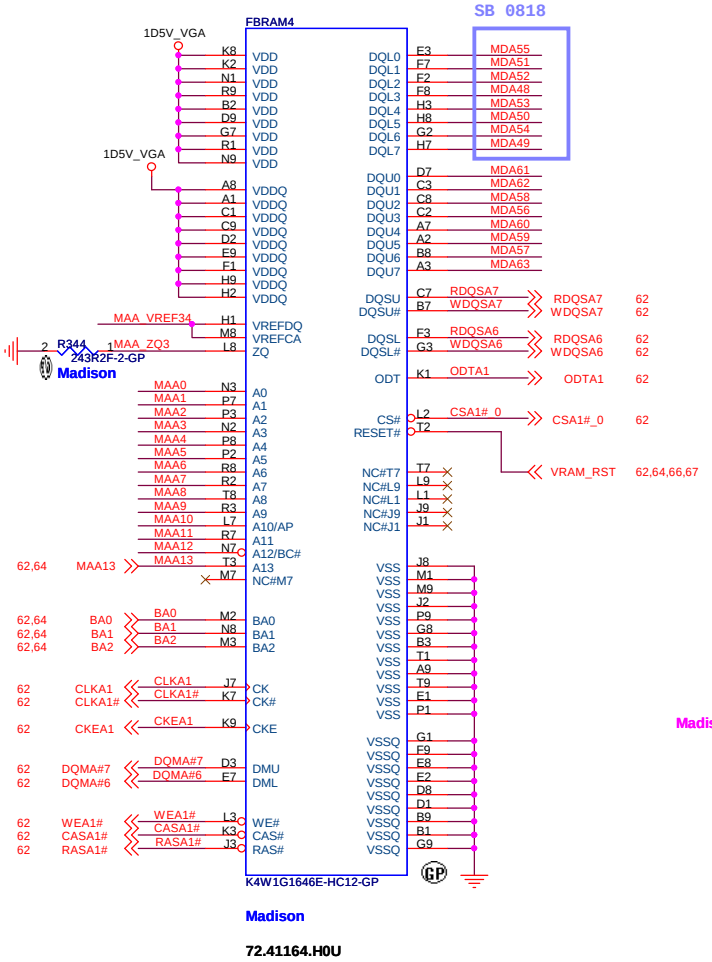
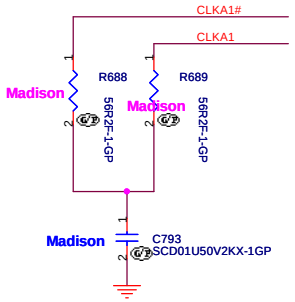
DDR3

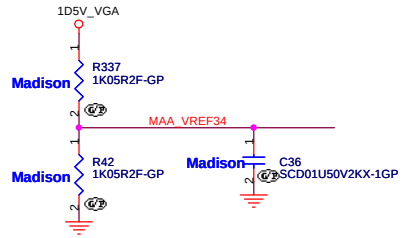






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

62,64 DQMA#[0..7]
62,64 RDQSA[0..7]
62,64 WDQSA[0..7]
62,64 MAA[0..12] MAA[0..12]
62,64 MDA[0..63] MDA[0..63]



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Title: ***VRAM(2/4)***

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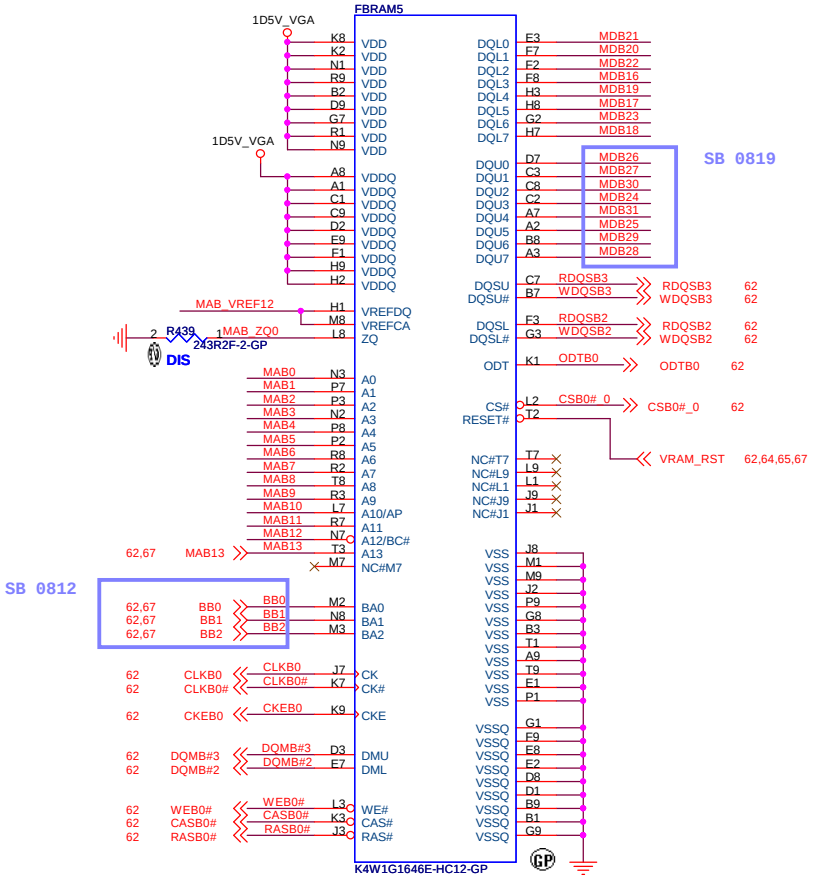
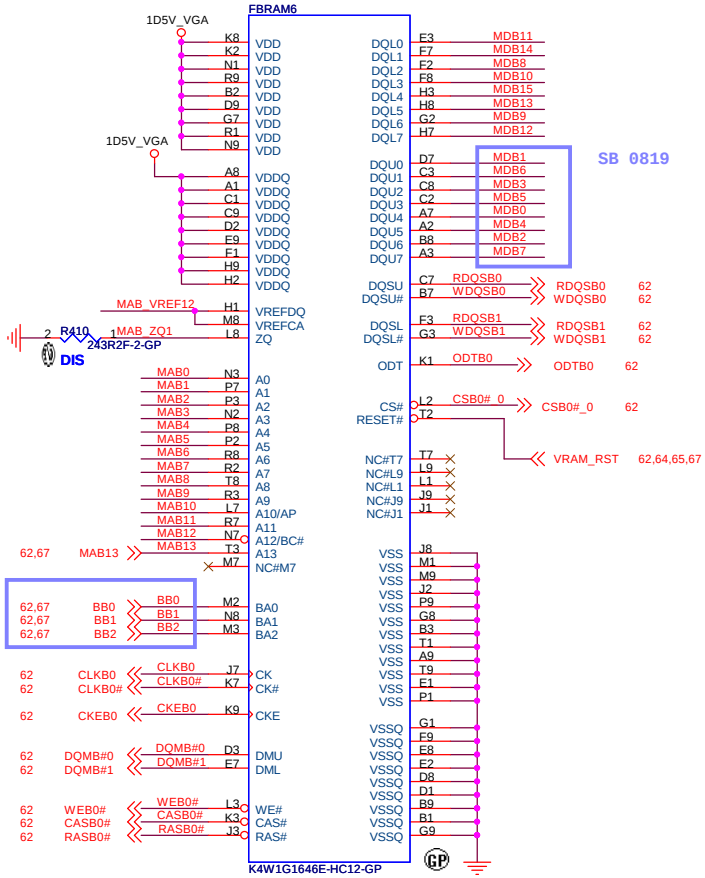
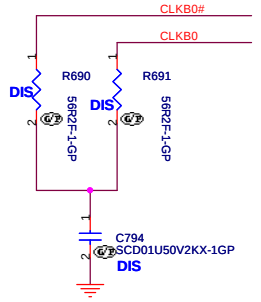
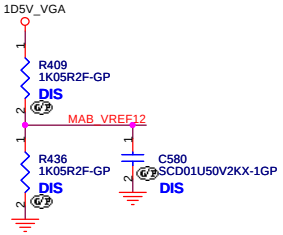
DDR3

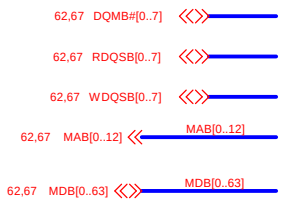




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	*VRAM(3/4)*	
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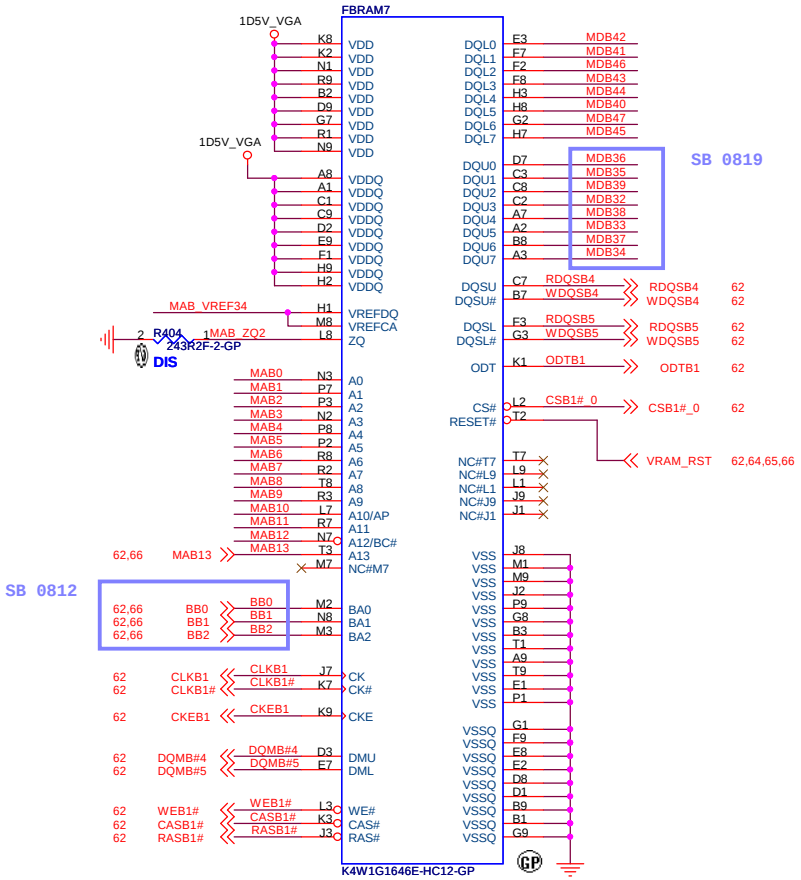
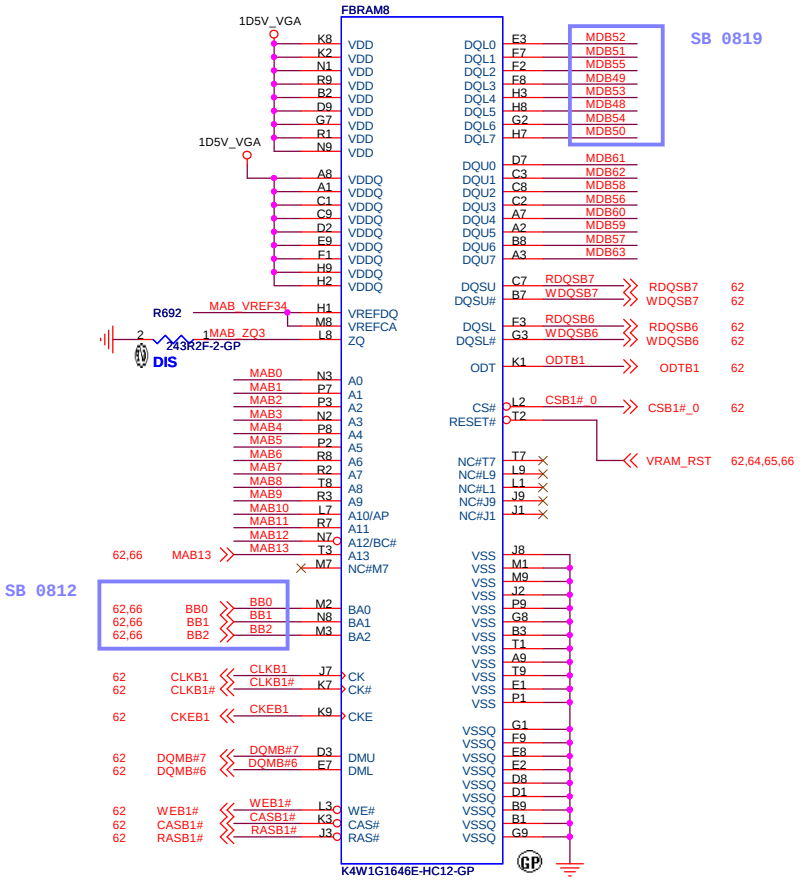
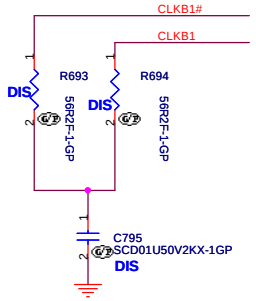
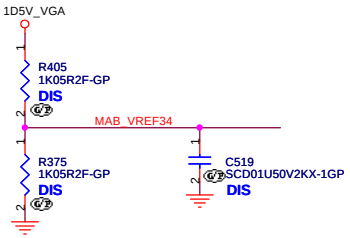
DDR3

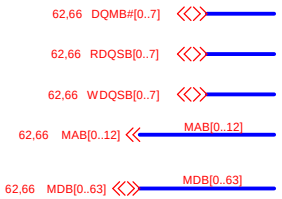




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4/4)***

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Title

Modify History

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