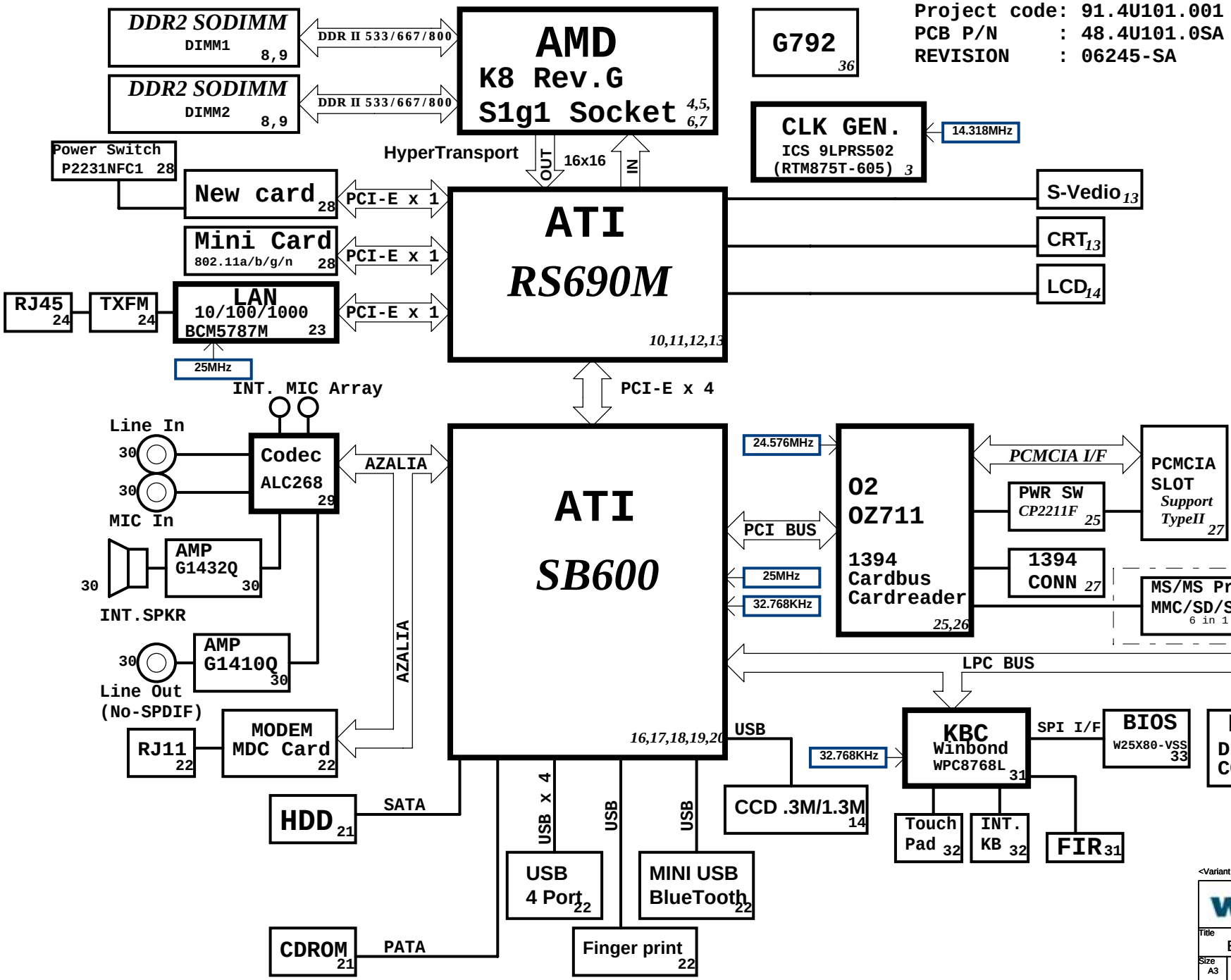
Orta Block Diagram



Project code: 91.4U101.001
PCB P/N : 48.4U101.0SA
REVISION : 06245-SA

PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE	
INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC	
INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC	
INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO	
INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO	
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO	
INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 1 of 46

SA: 07/31/06 Start

SB change
power team
1.change L7, L9 to 68.1R510.10D
2.changge U12 to 84.04706.037
3.change R66 to 10K ohm

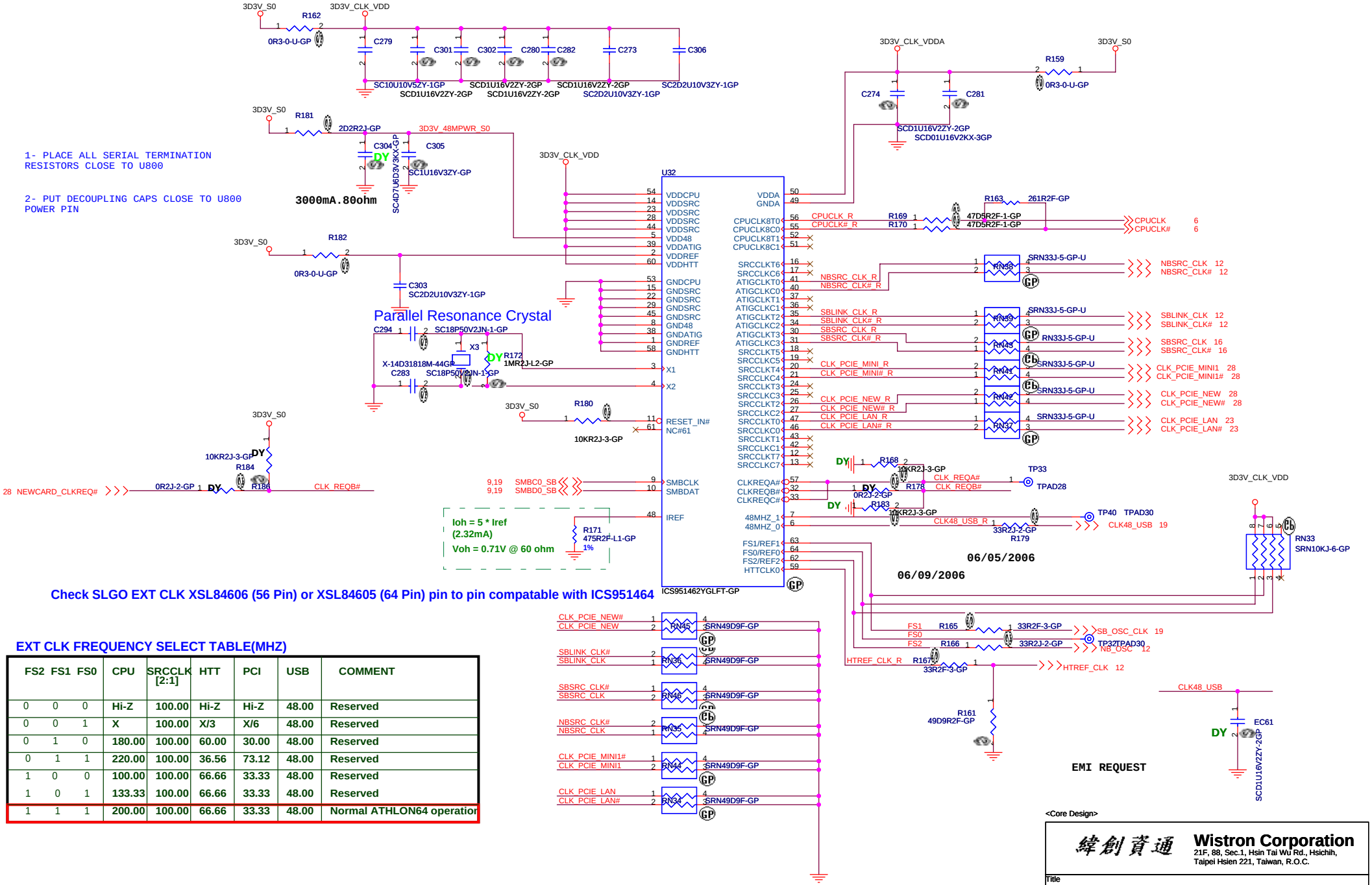
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 2 of 46



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

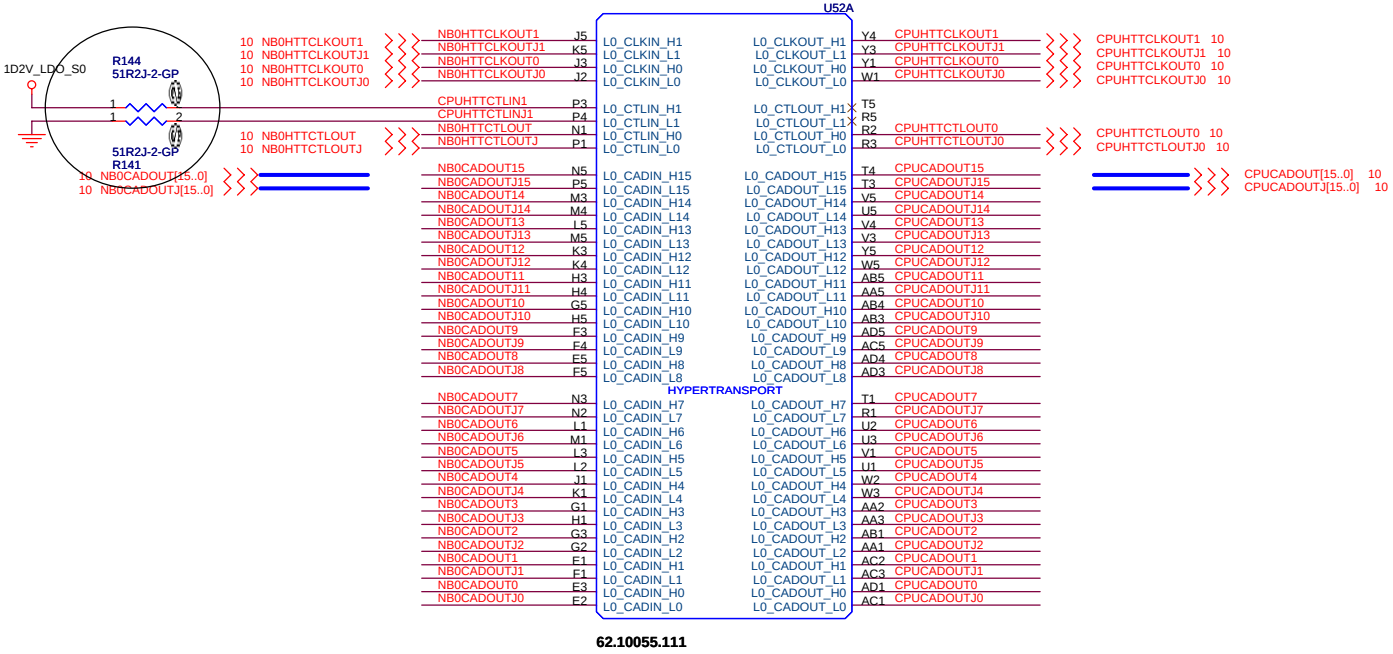
<Core Design>

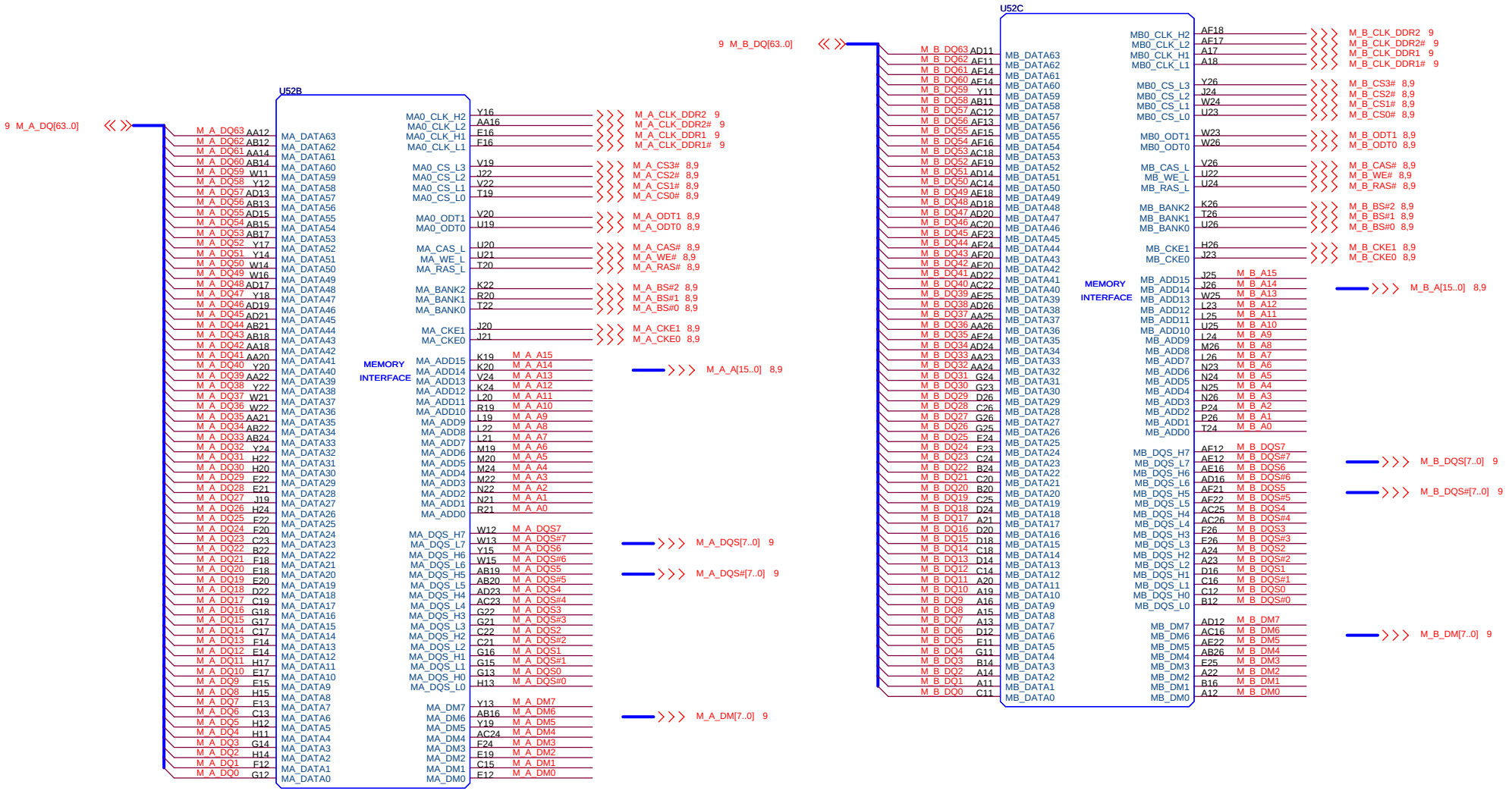
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 3 of 46


U52A
1D2V_LDO_S0
R144
51R2J-2-GP
R141
51R2J-2-GP
HYPERTRANSPORT
62.10055.111



LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

Near To CPU

20061031 for Power Test

Remove these resistor when using EVT CPU

Change;Add

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

VREF_DDR_CLAW

LAYOUT: Locate close to CPU.

HDT Connectors

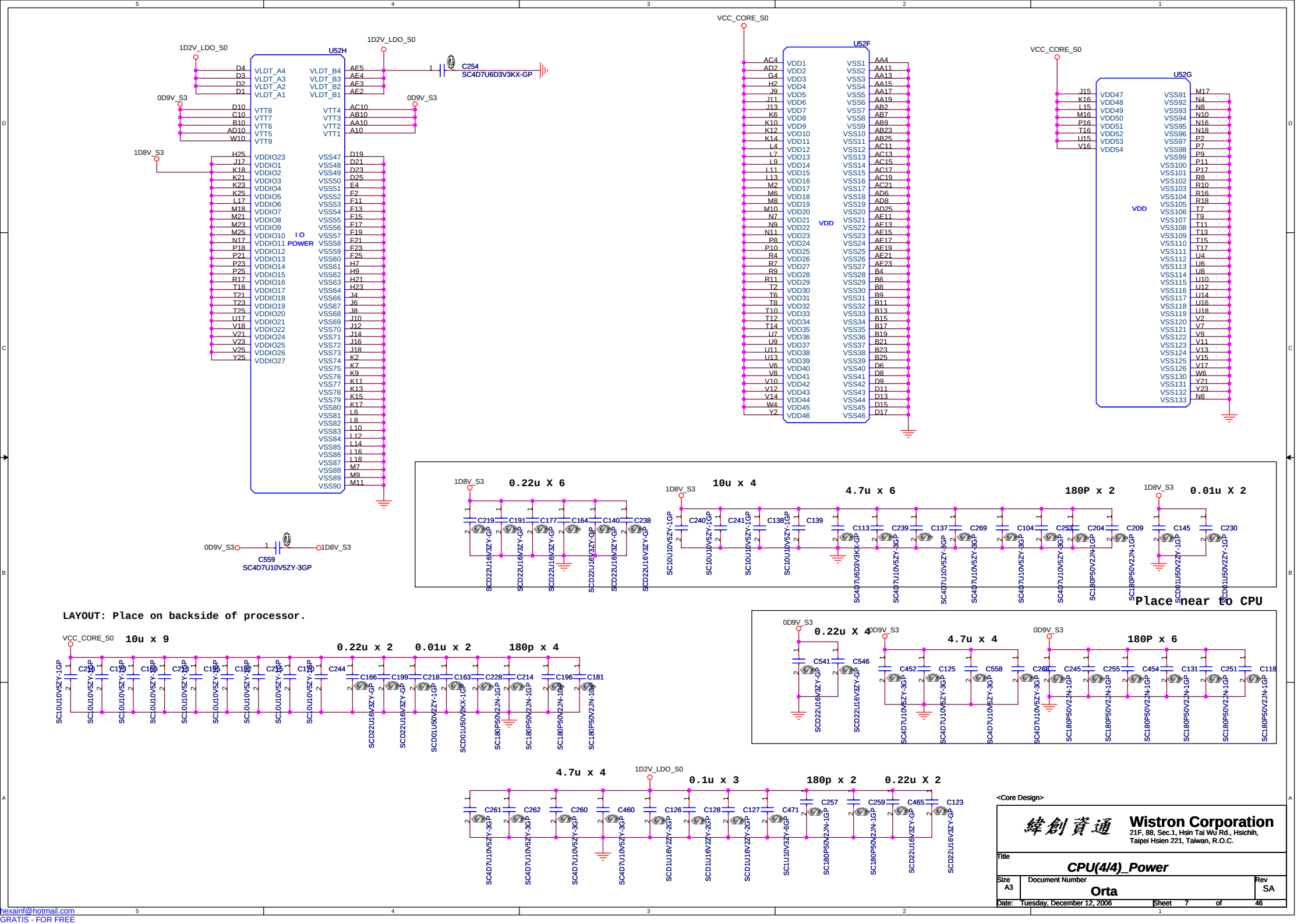
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

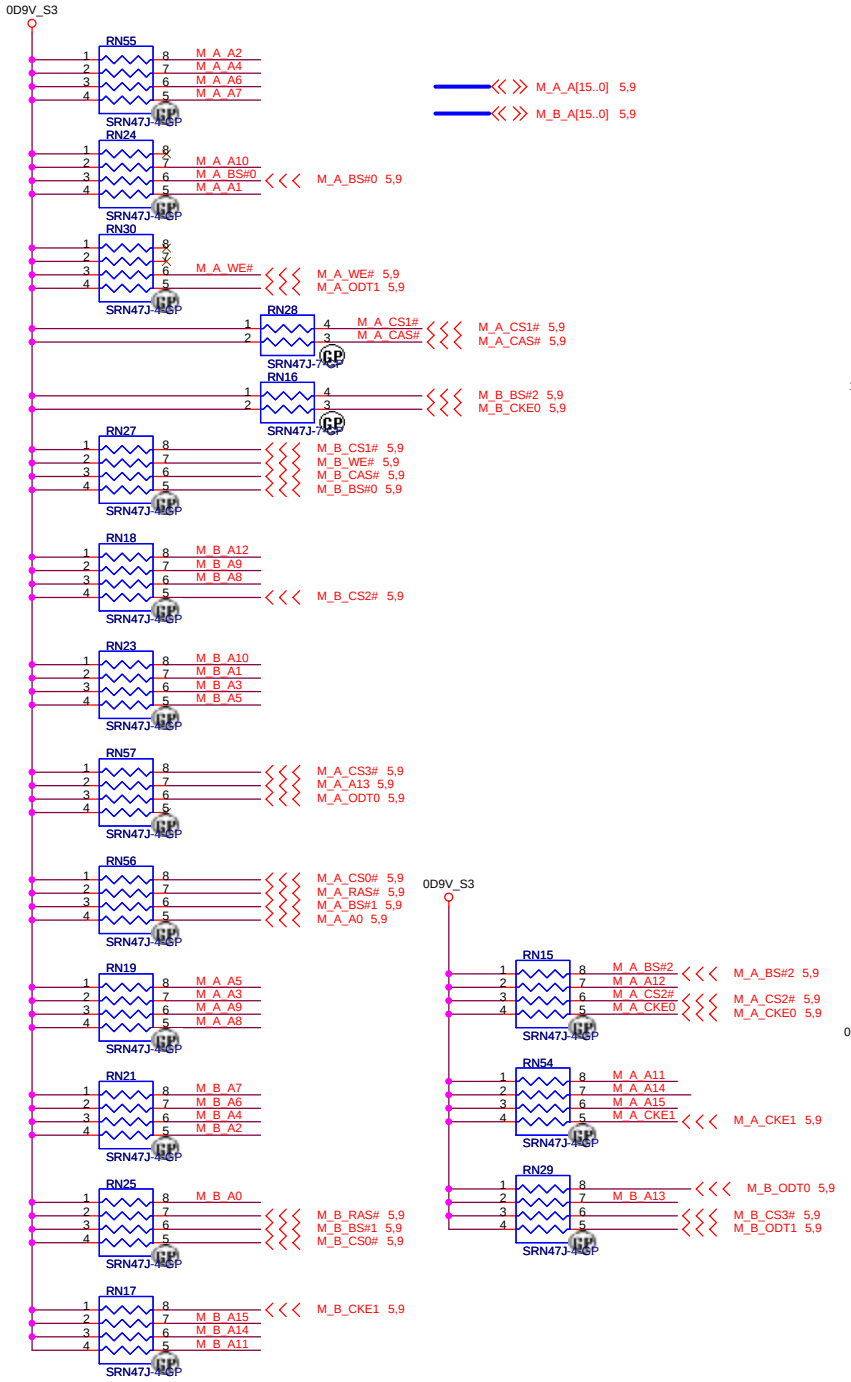
Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 6 of 46



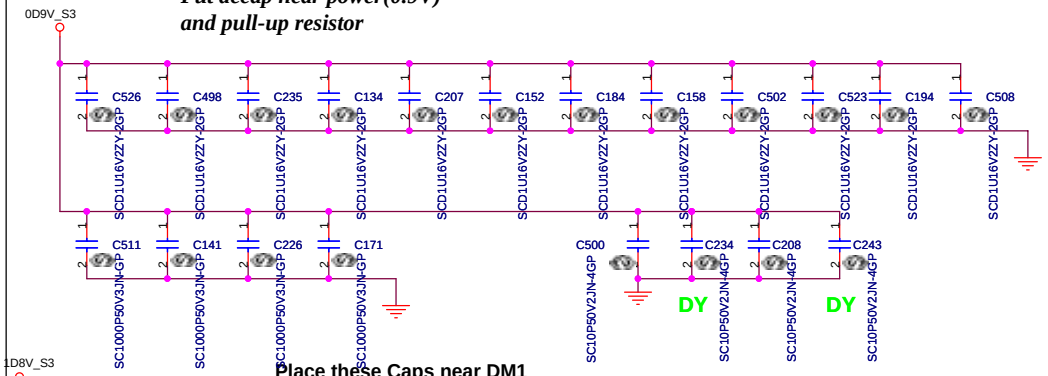
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

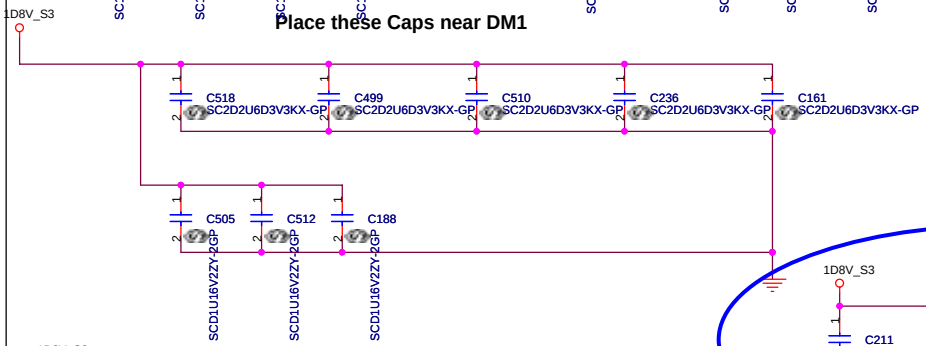


Decoupling Capacitor

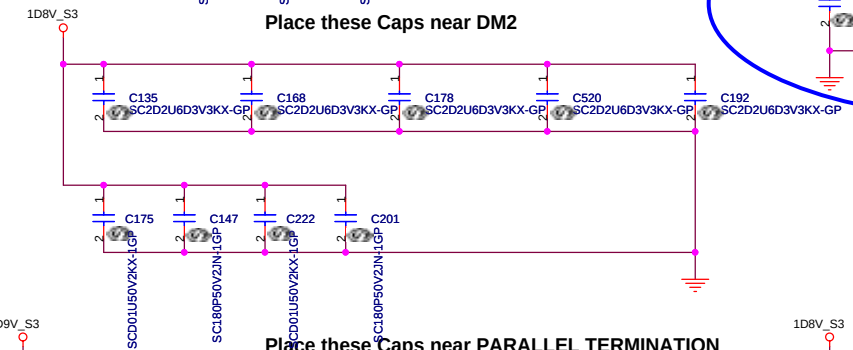
Put decap near power(0.9V) and pull-up resistor

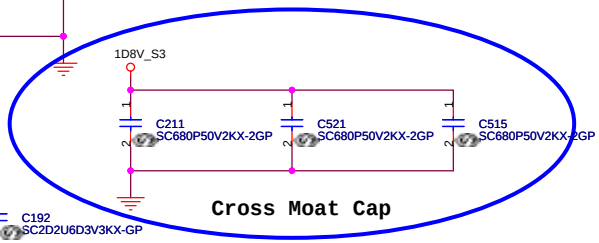


Place these Caps near DM1

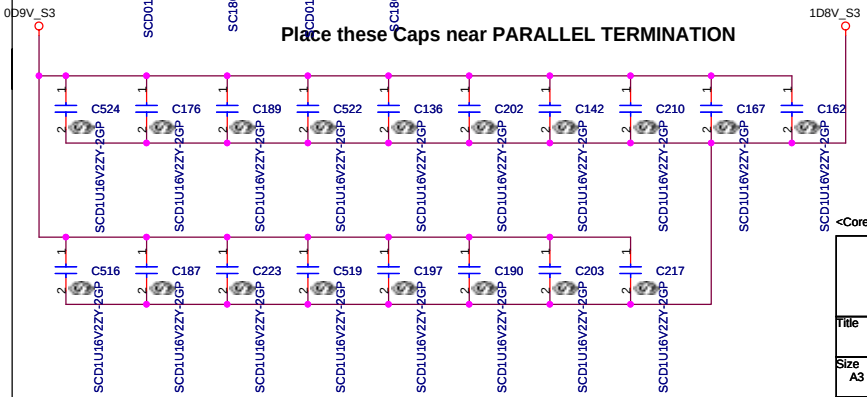


Place these Caps near DM2





Place these Caps near PARALLEL TERMINATION



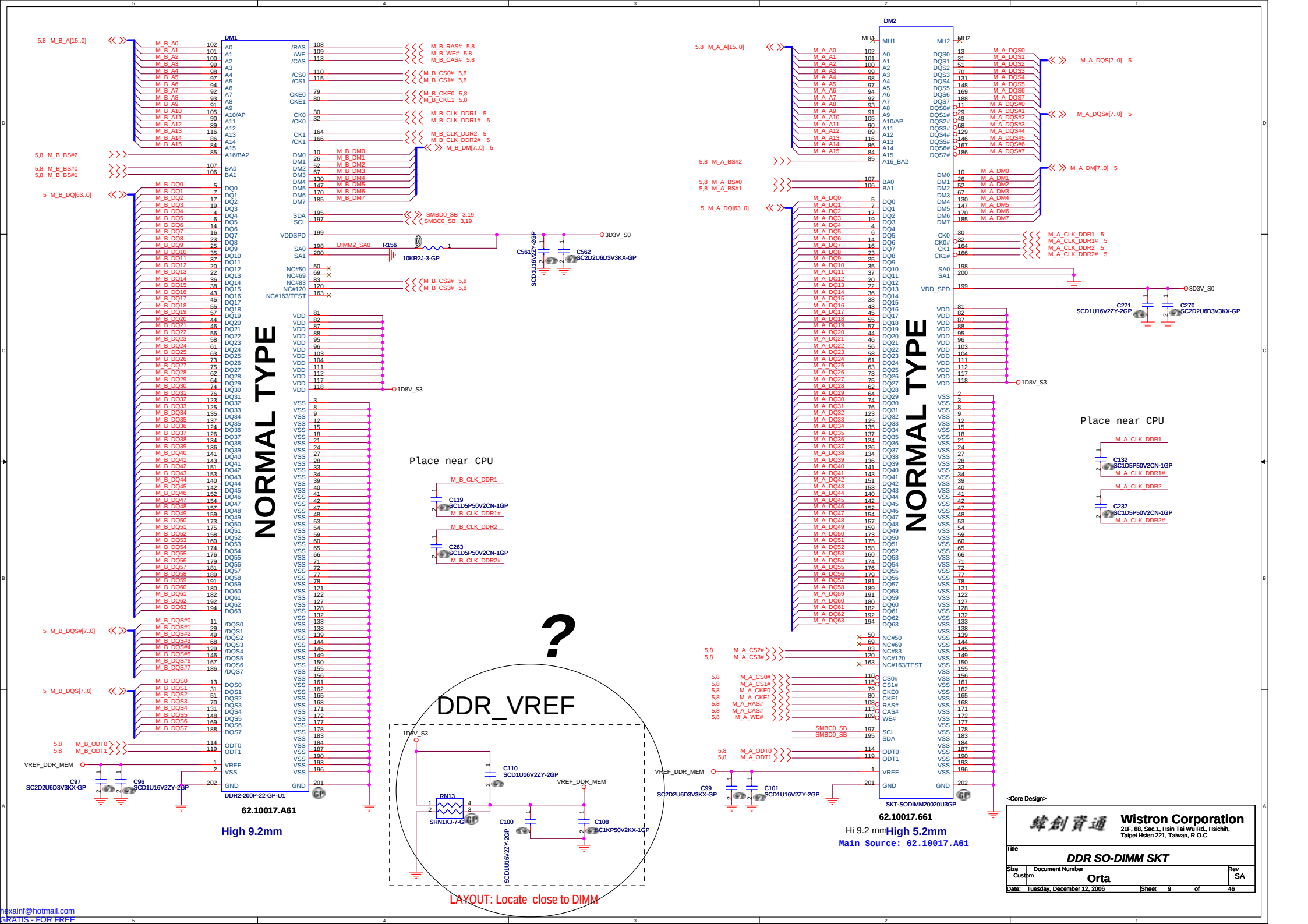
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

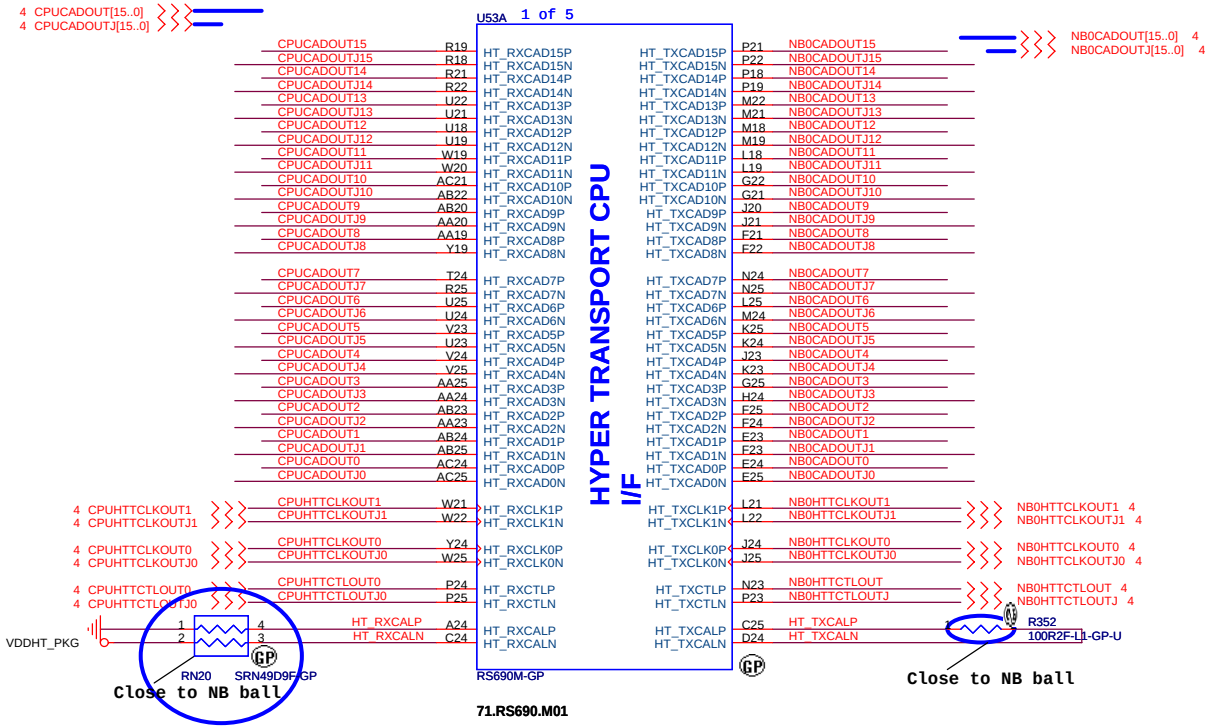
Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 8 of 46



CLAW HAMMER TO NB

NB TO CLAW HAMMER



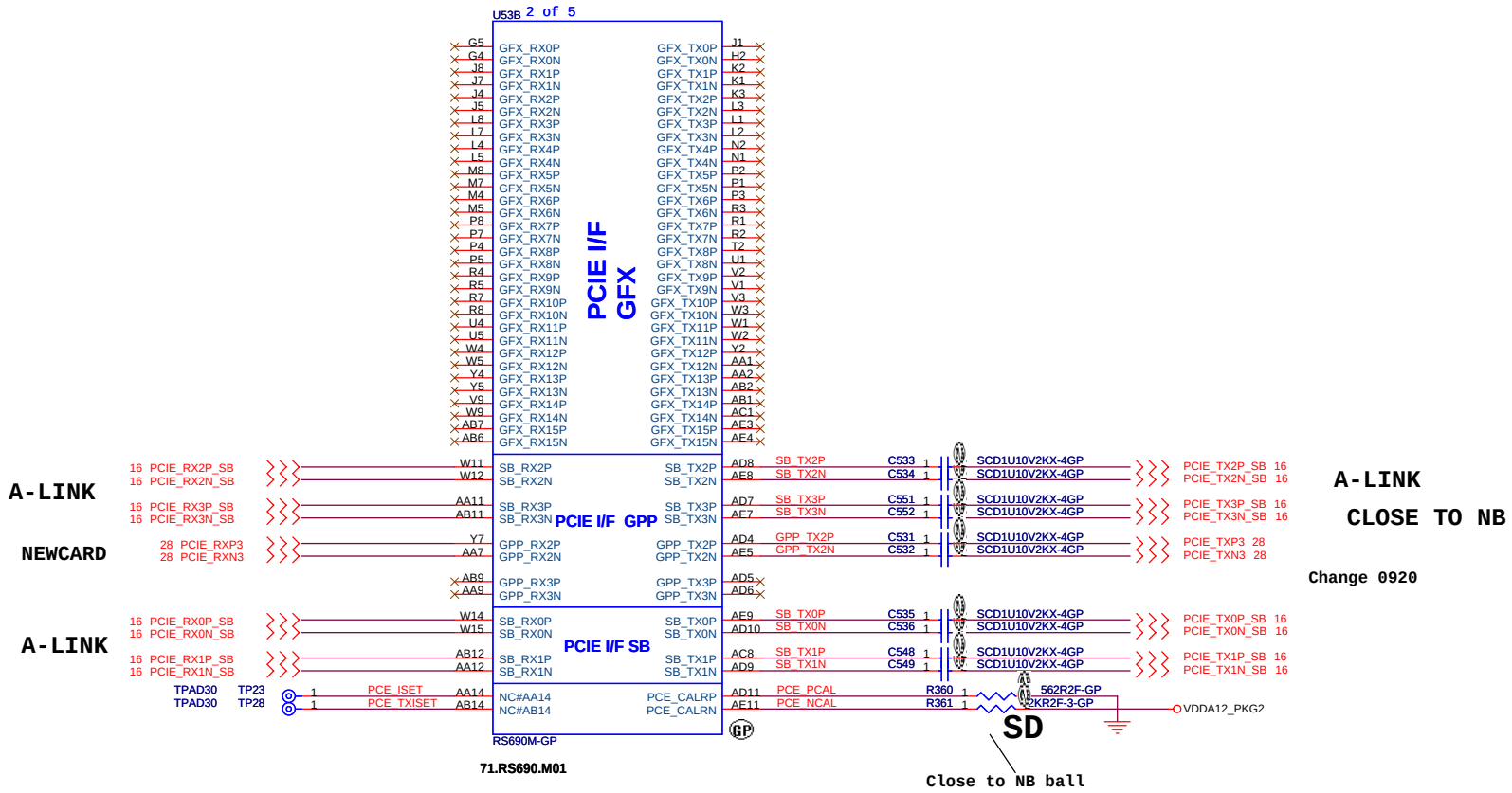
<Core Design>

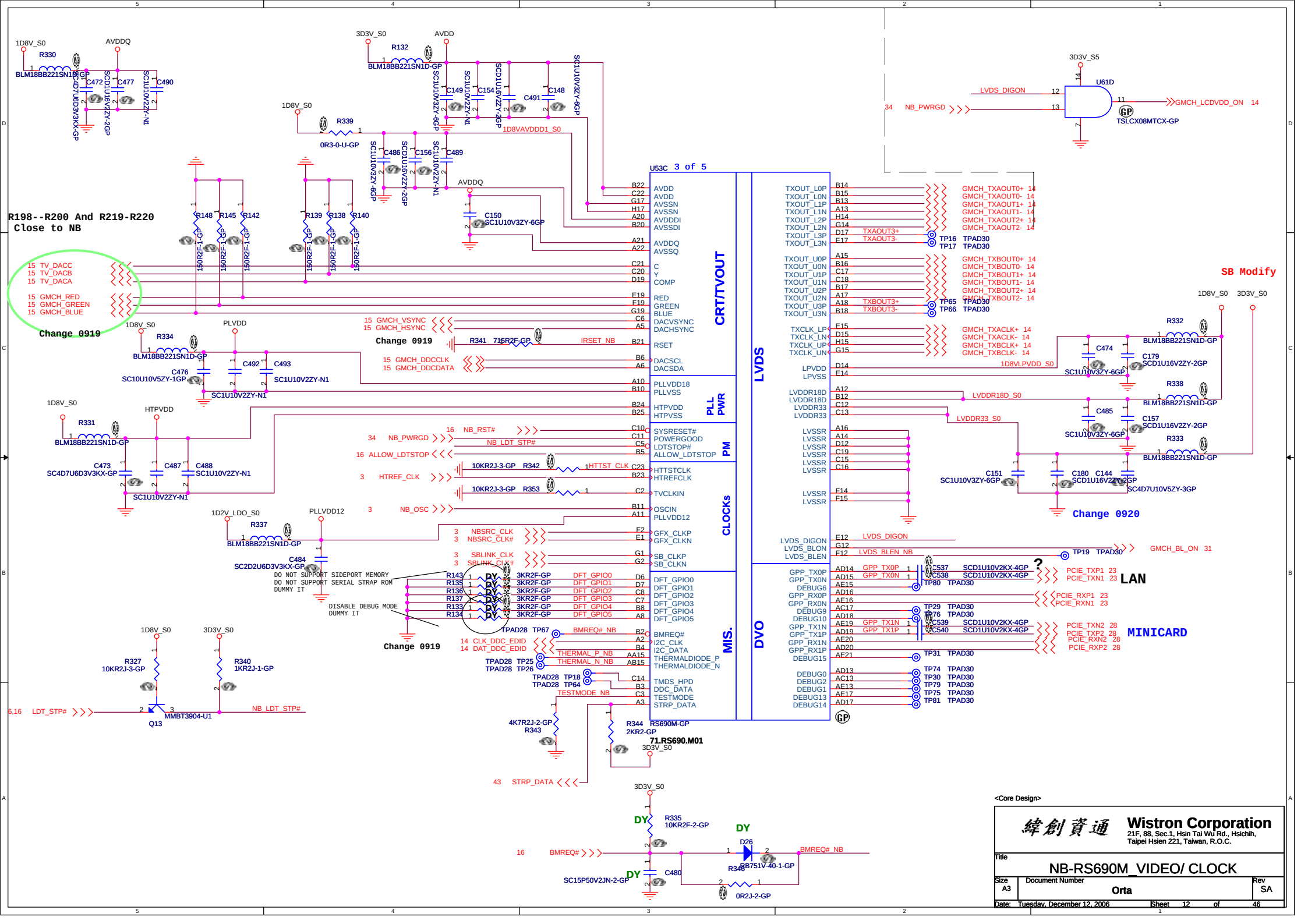
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

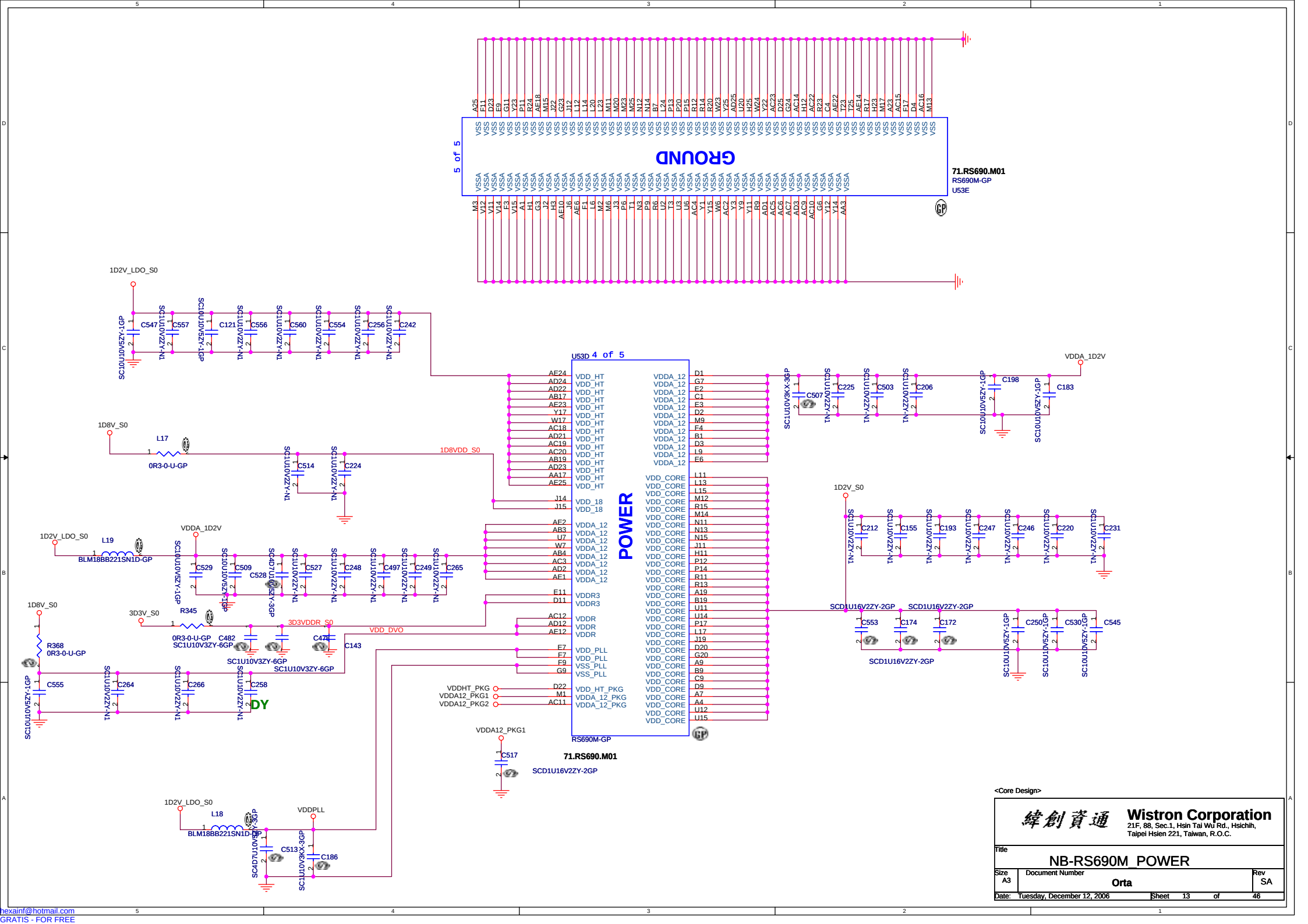
Title: NB-RS690M_HT

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 10 of 46




R198--R200 And R219-R220
Close to NB
Change 0919
Change 0920
SB Modify
LAN
MINICARD
U53C 3 of 5
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
DVO
71.RS690.M01
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
DISABLE DEBUG MODE
DUMMY IT
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_VIDEO/ CLOCK
Size A3
Document Number
Orta
Rev SA
Date: Tuesday, December 12, 2006
Sheet 12 of 46



<Core Design>

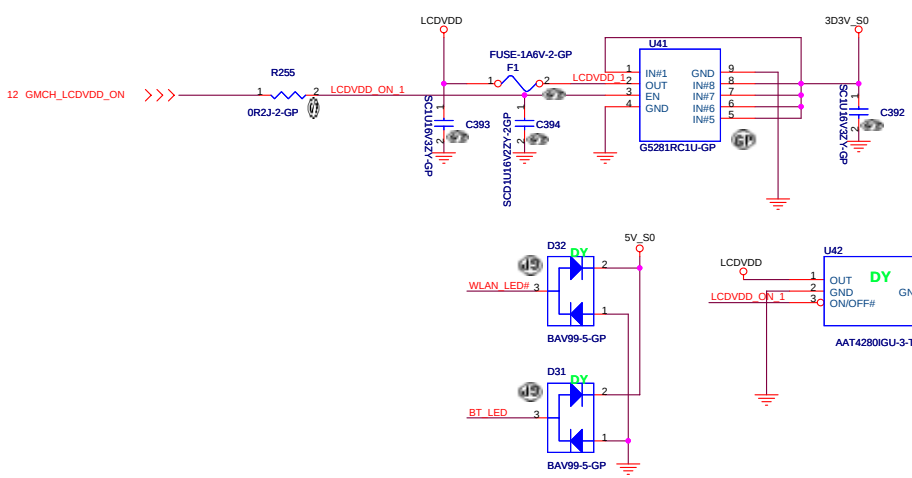
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

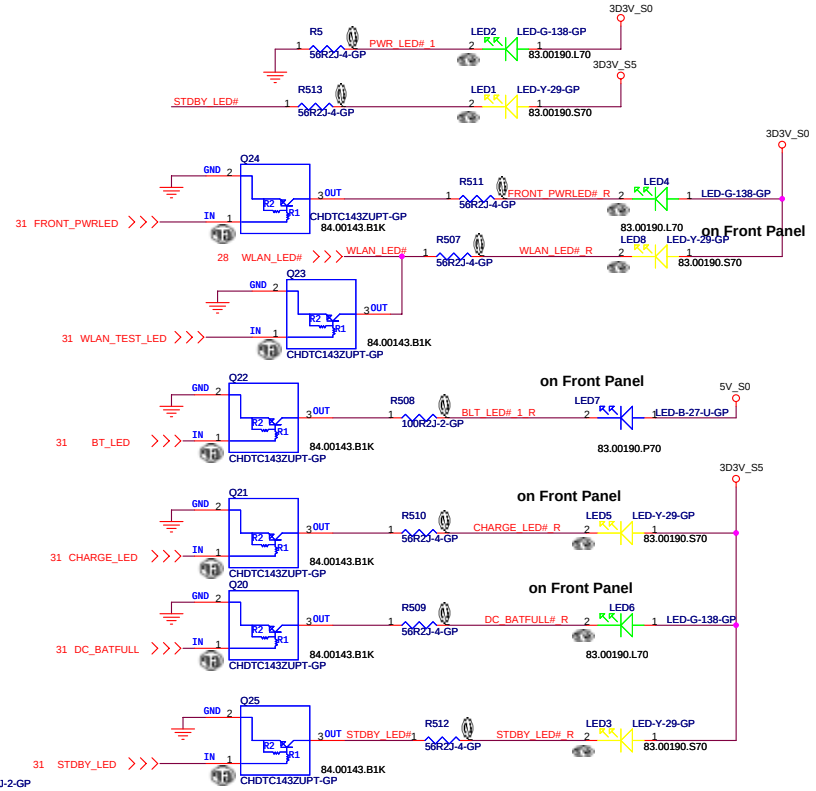
Title: NB-RS690M_POWER

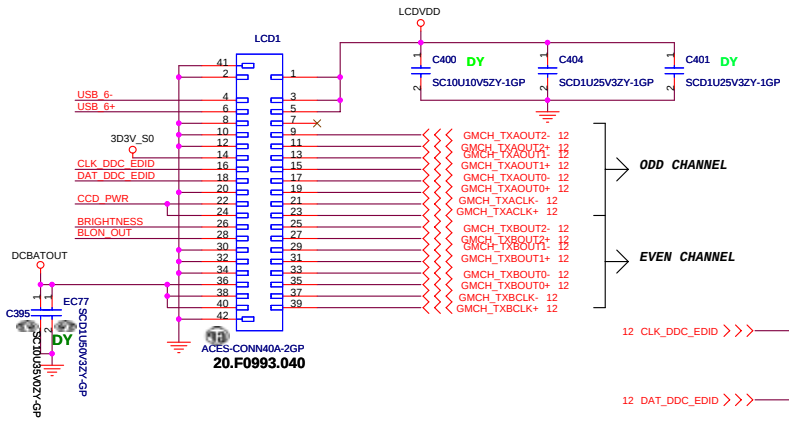
Size	Document Number	Rev
A3	Orta	SA

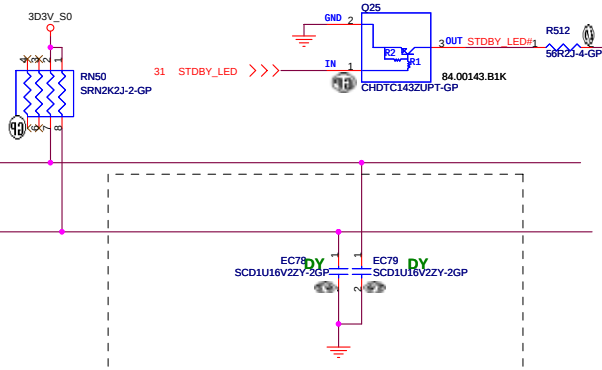
Date: Tuesday, December 12, 2006 Sheet 13 of 46

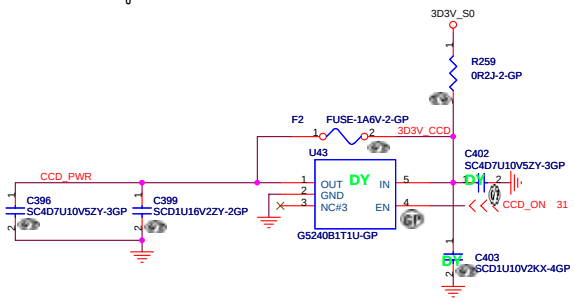
LCD/INVERTER CONN

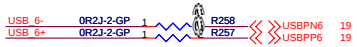


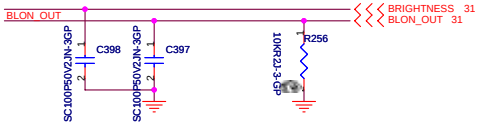


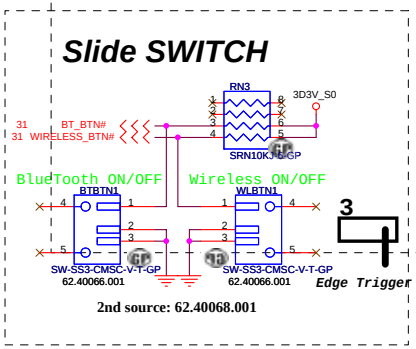


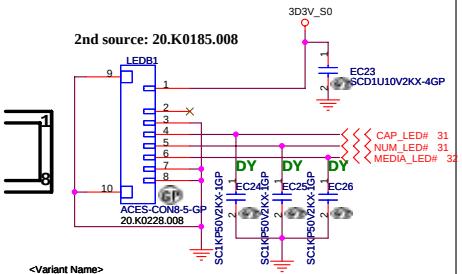












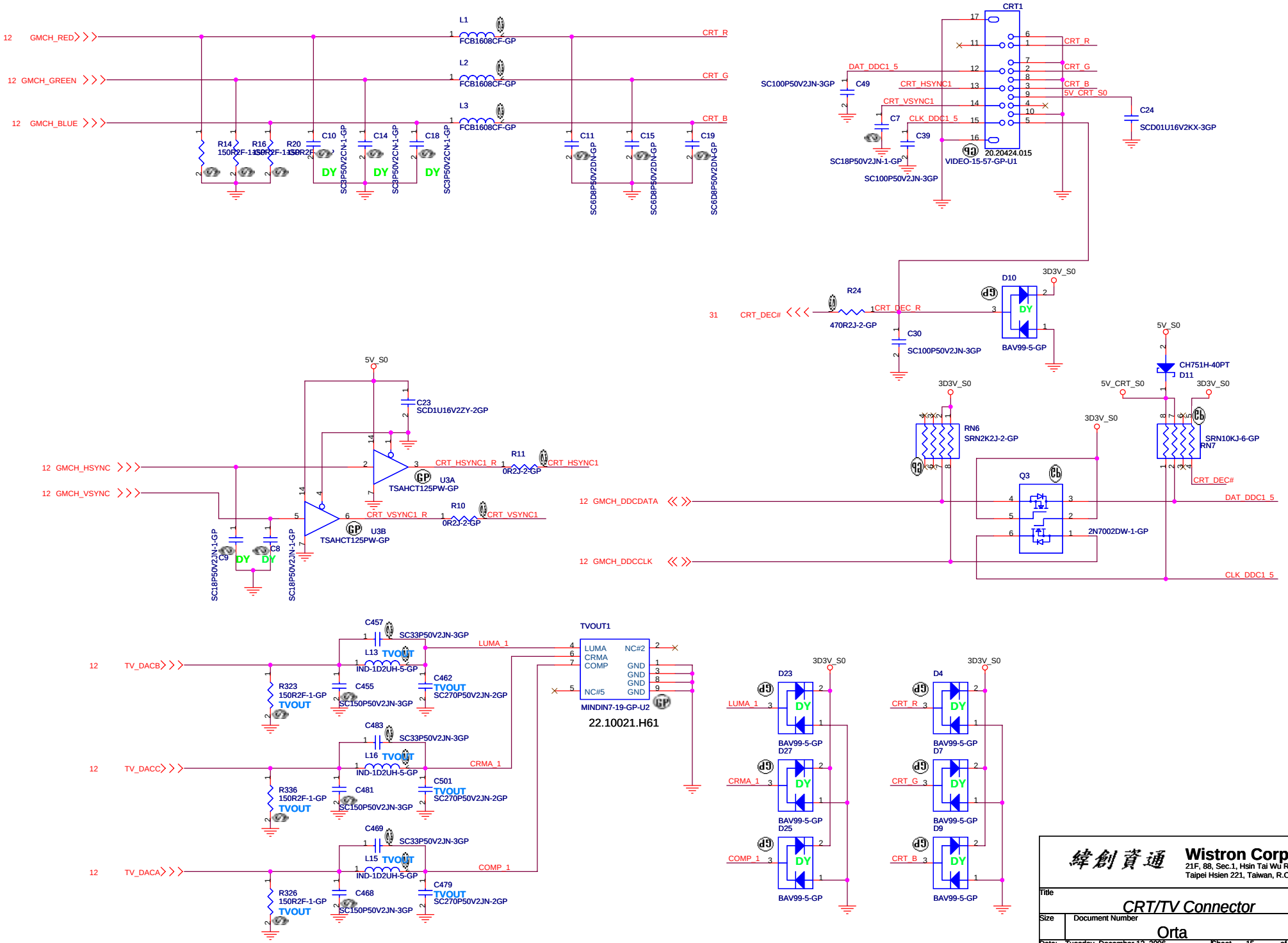
<variant_name><Variant Name></variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 14 of 46



Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

SB600 asserts PLTRST# to reset
devices on the platform.

Change 0921

PCIRST

U57A 1 of 4

SB600-GP

71.SB600.00U

2nd source: 20.D0198.103

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 16 of 46

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP

U57B 2 of 4

SATA_TXP0 SATA_TXN0 SATA_RXN0 SATA_RXP0

C586 C587 C590 C593

SATA_TXP0_SB SATA_TXN0_SB SATA_RXN0_SB SATA_RXP0_SB

SATA_TX0+ SATA_TX0- SATA_RX0- SATA_RX0+ SATA_TX1+ SATA_TX1- SATA_RX1- SATA_RX1+ SATA_TX2+ SATA_TX2- SATA_RX2- SATA_RX2+ SATA_TX3+ SATA_TX3- SATA_RX3- SATA_RX3+

SERIAL ATA

SATA

SATA_X1 SATA_X2

R381 10MR2J-L-GP

X5 XTAL-25MHZ-20GP

C582 SC10P50V2JN-4GP C576 SC10P50V2JN-4GP

According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.

R397 1KR2F-3-GP

3D3V_S0

R191 10KR2J-3-GP

SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67

32 SATA_LED#

PLLVDD_ATA XTLVDD_ATA AVDD_SATA

PLLVDD_SATA XTLVDD_SATA AVDD_SATA AVSS_SATA

SERIAL ATA POWER

IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#

IDE_PDIORDY INT_IRQ14 IDE_PDA0 IDE_PDA1 IDE_PDA2 IDE_PDDACK# IDE_PDDREQ IDE_PDIOR# IDE_PDIOW# IDE_PDCS1# IDE_PDCS3#

IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

ATA 66/100

SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32 LAN_RST#/GPIO13 ROM_RST#/GPIO14

TP54 TP45 TP50 TP101 TP46 TP41 TP47 TPAD30

SPI ROM

FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49 FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52 TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64 VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60

ALERT# 6,35 PSW_CLR# UMA_DIS CLK_ID FP_ID FP_ID 32 FP_DETECT# 32

HW MONITOR

AVDD AVSS

AVDD_HWM

R432 0R3-0-U-GP

C613 SCD1U16V2ZY-2GP C614 SC2D2U6D3V3KX-GP DY

3D3V_S0

R149 10KR2J-3-GP

FP_DETECT# PSW_CLR#

G41 GAP-OPEN

0 => DIS
1 => UMA

R214 10KR2J-3-GP ? R197 10KR2J-3-GP RTL R198 10KR2J-3-GP DY

UMA_DIS CLK_ID FP_ID

R217 10KR2J-3-GP DY R206 10KR2J-3-GP ICS R207 10KR2J-3-GP DY

SB600-GP

71.SB600.00U

SATA

3D3V_S0 XTLVDD_ATA R187 0R3-0-U-GP EC117 SCD1U16V2ZY-2GP C318 SC2D2U6D3V3KX-GP

1D2V_LDO_S0 PLLVDD_ATA R193 0R3-0-U-GP EC118 SCD1U16V2ZY-2GP C320 SC2D2U6D3V3KX-GP

1D2V_LDO_S0 R177 0R3-0-U-GP EC114 SCD1U16V2ZY-2GP C311 SC10U6D3V5KX-1GP

AVDD_SATA C307 SC10U6D3V5KX-1GP EC63 SCD1U16V2ZY-2GP DY EC65 SCD1U16V2ZY-2GP DY EC62 SCD1U16V2ZY-2GP DY EC60 SCD1U16V2ZY-2GP DY EC64 SCD1U16V2ZY-2GP

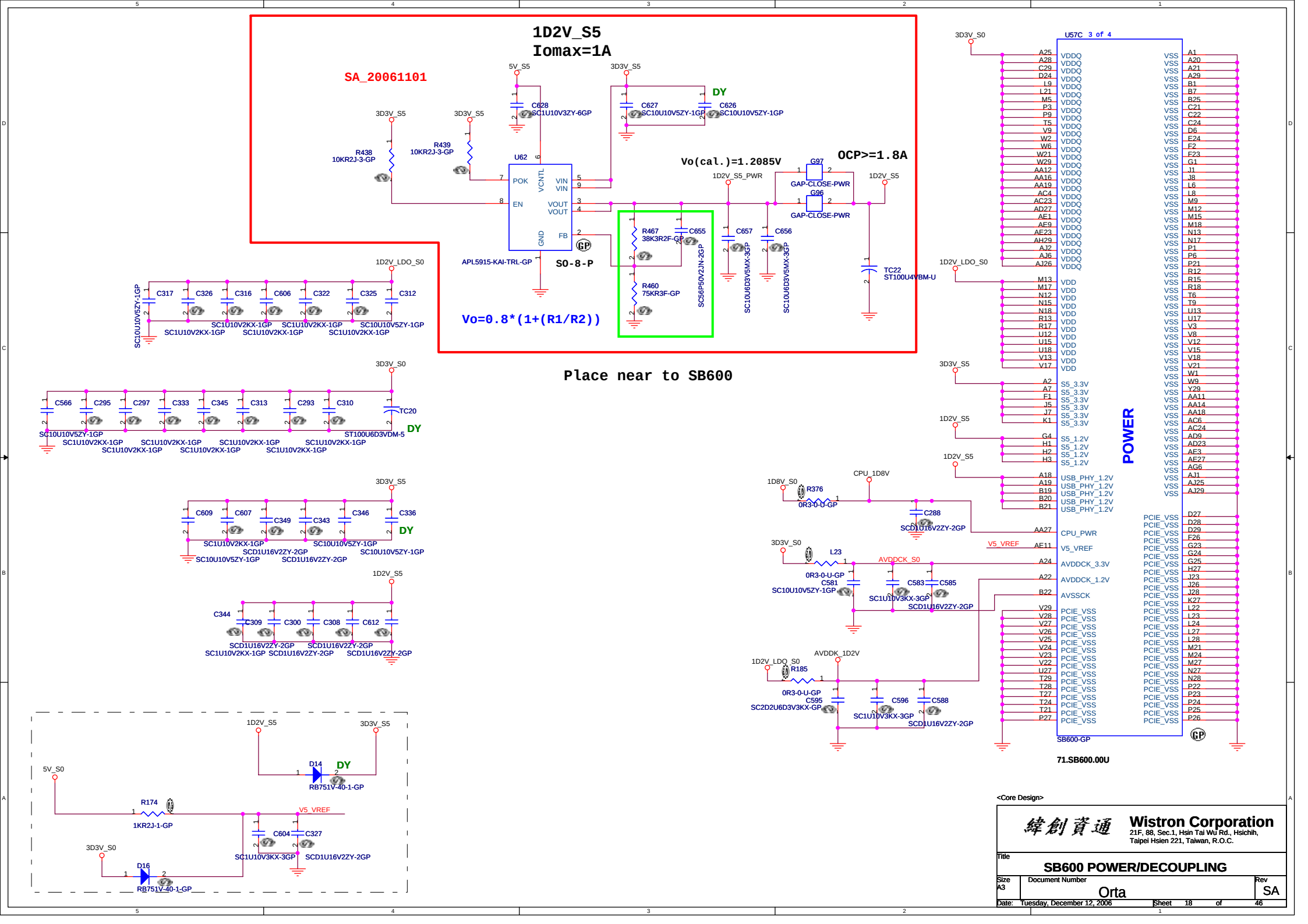
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

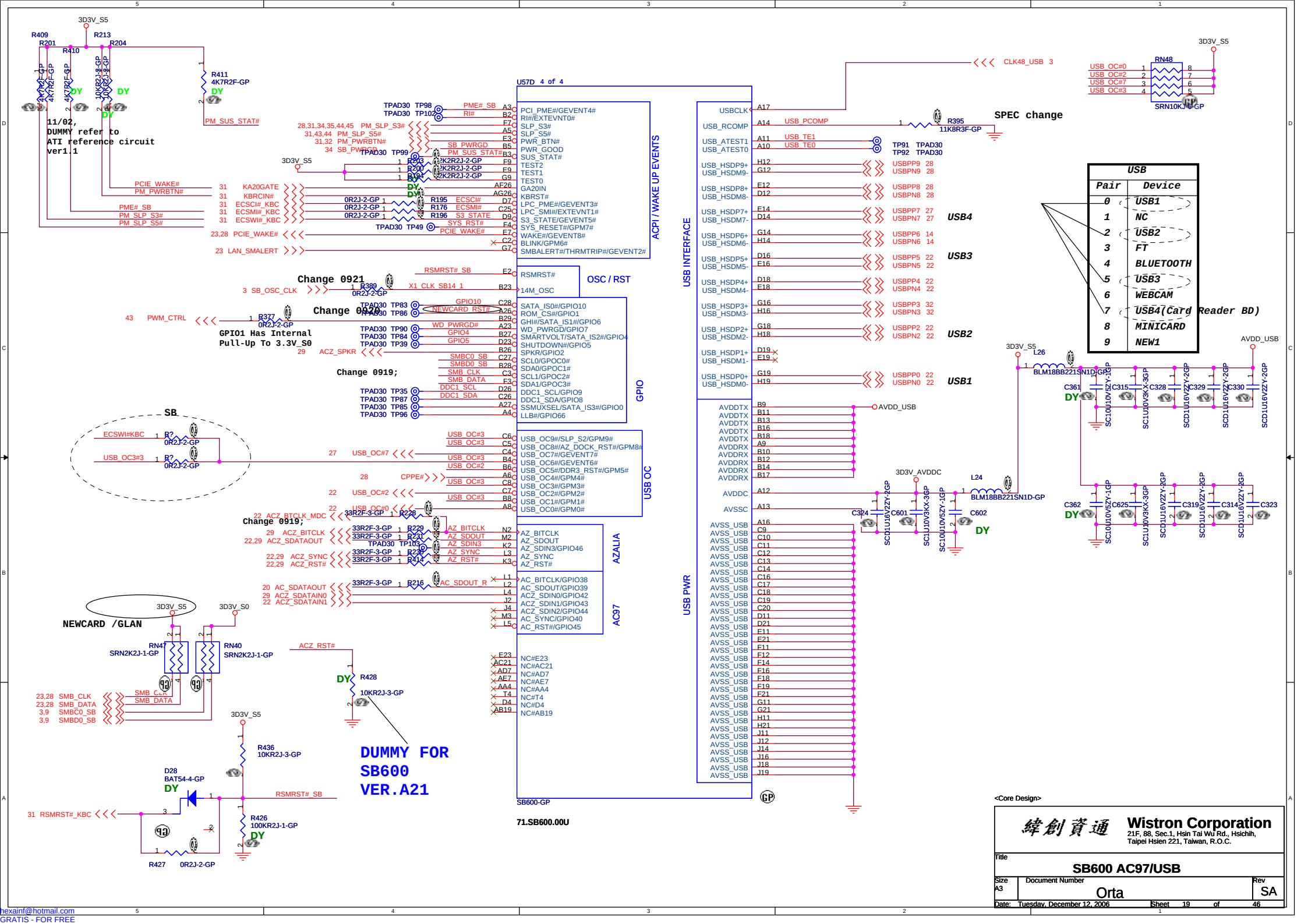
Size: A3 | Document Number: Orta | Rev: SA

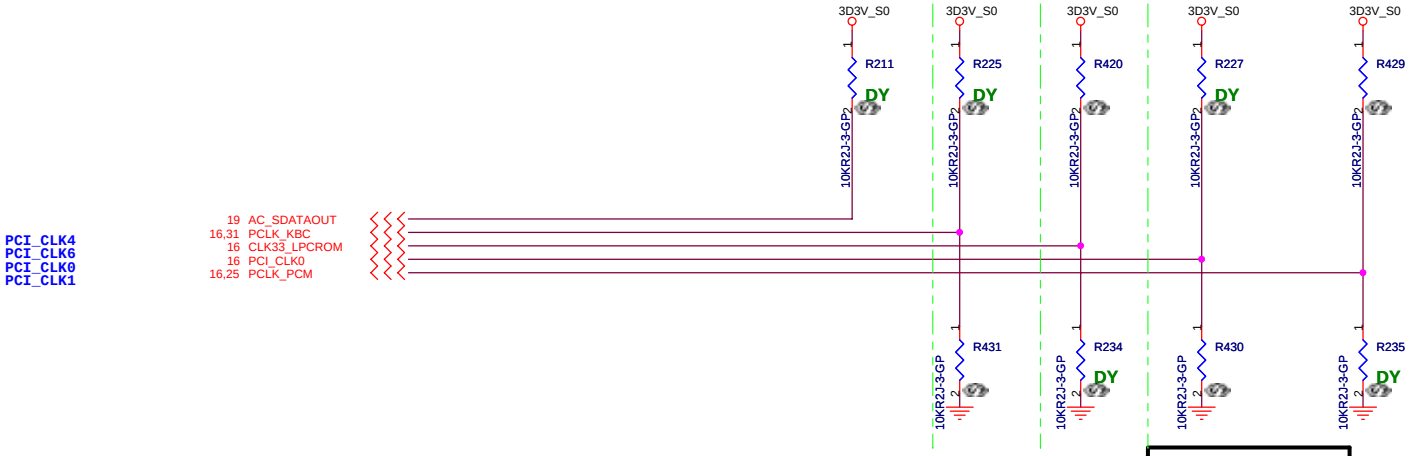
Date: Tuesday, December 12, 2006 | Sheet 17 of 46



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB600 POWER/DECOUPLING	
Size A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 18 of 46	

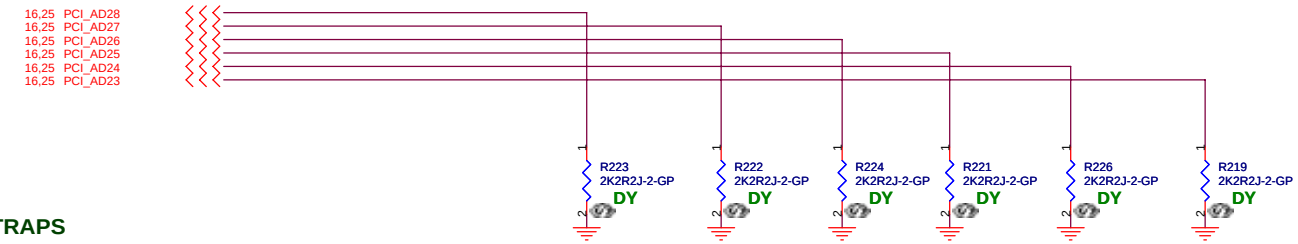




REQUIRED SYSTEM STRAPS

	SB600				
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

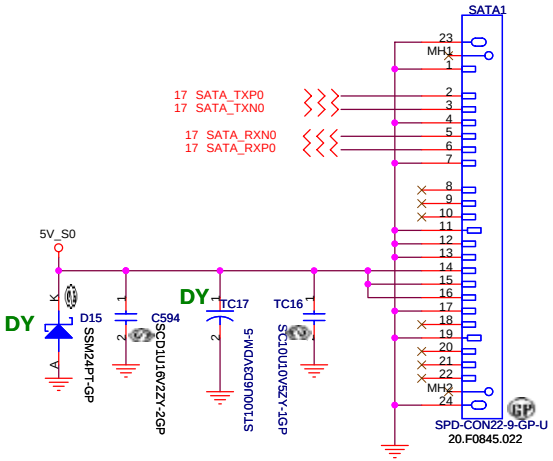
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

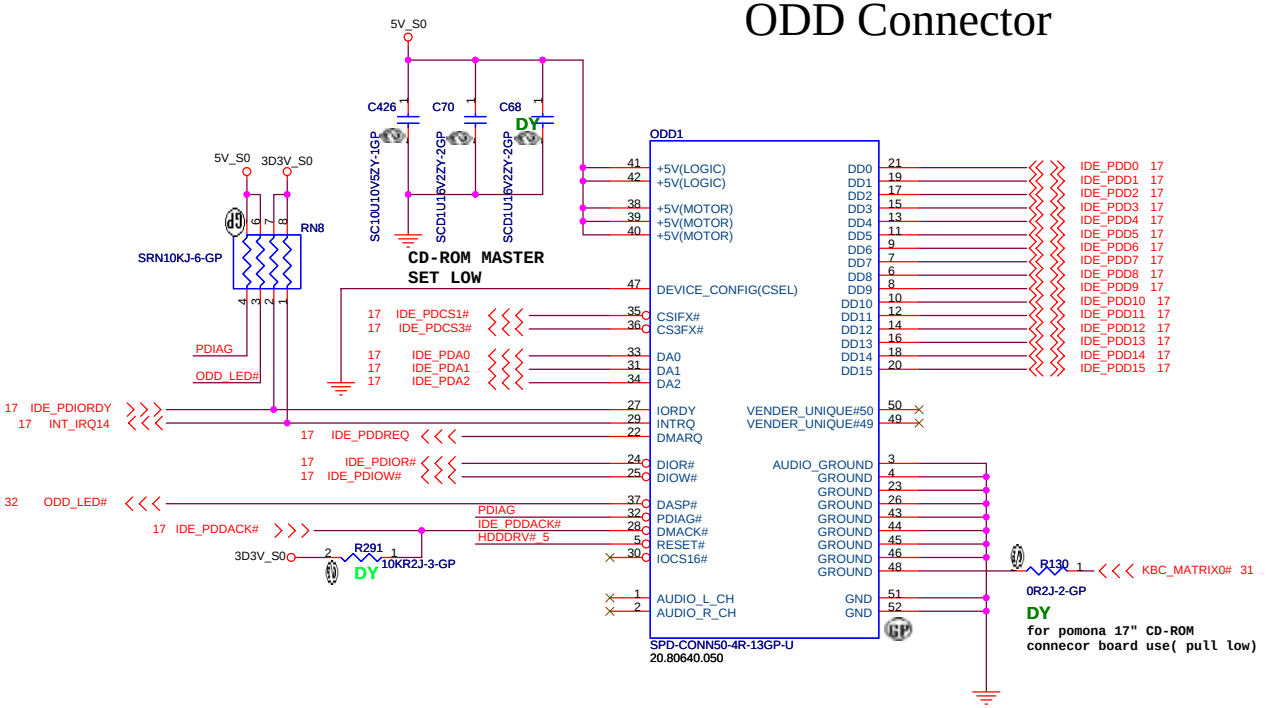
Size: A3 | Document Number: Orta | Rev: SA

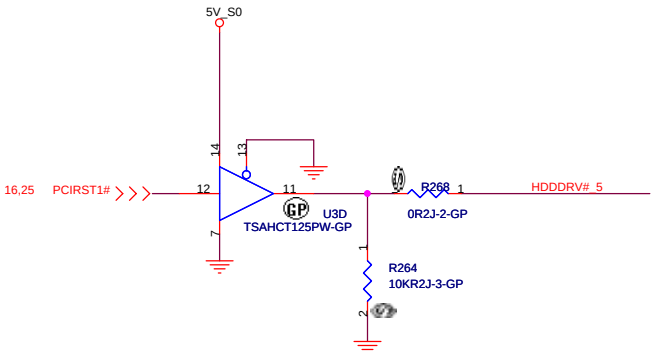
Date: Tuesday, December 12, 2006 | Sheet 20 of 46

SATA HD Connector



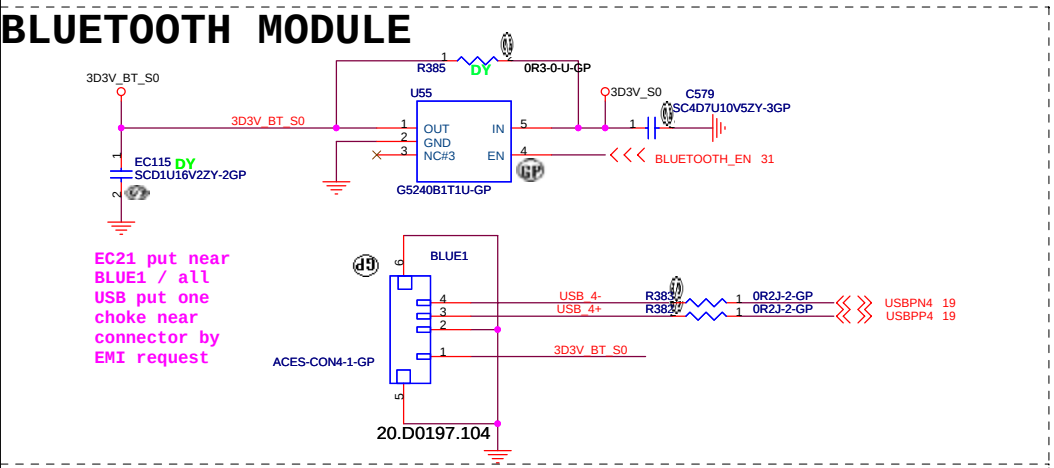
ODD Connector

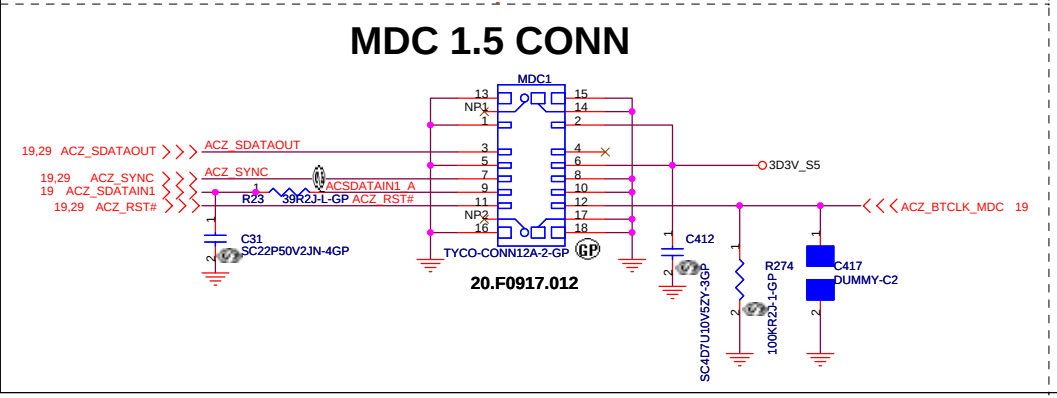


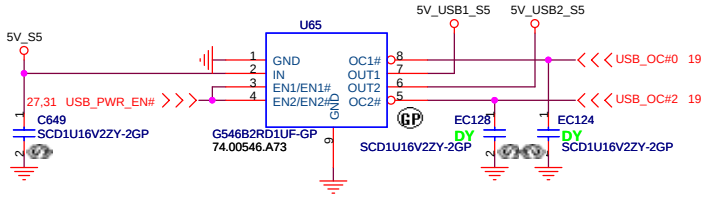


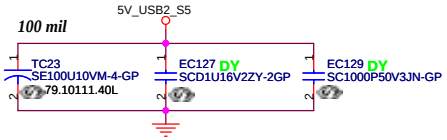
bom1

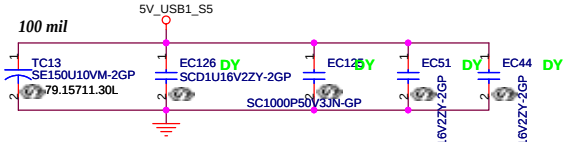
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDD and CDROM***
Size / Document Number	**Orta**
Rev	SA
Date: Tuesday, December 12, 2006	Sheet 21 of 46

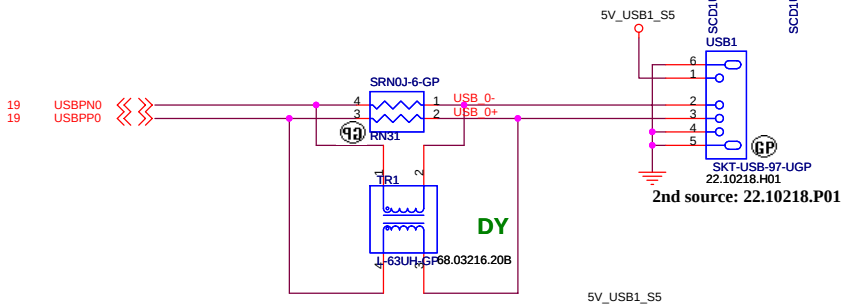


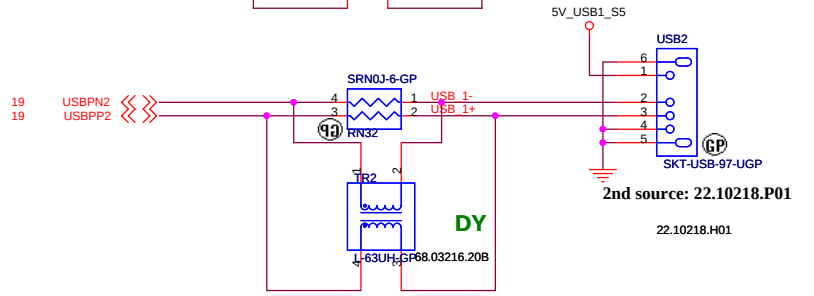


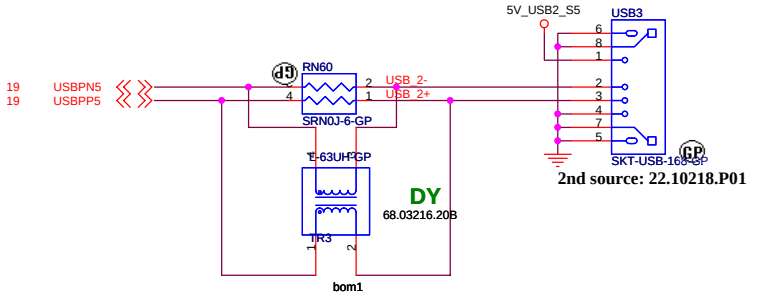










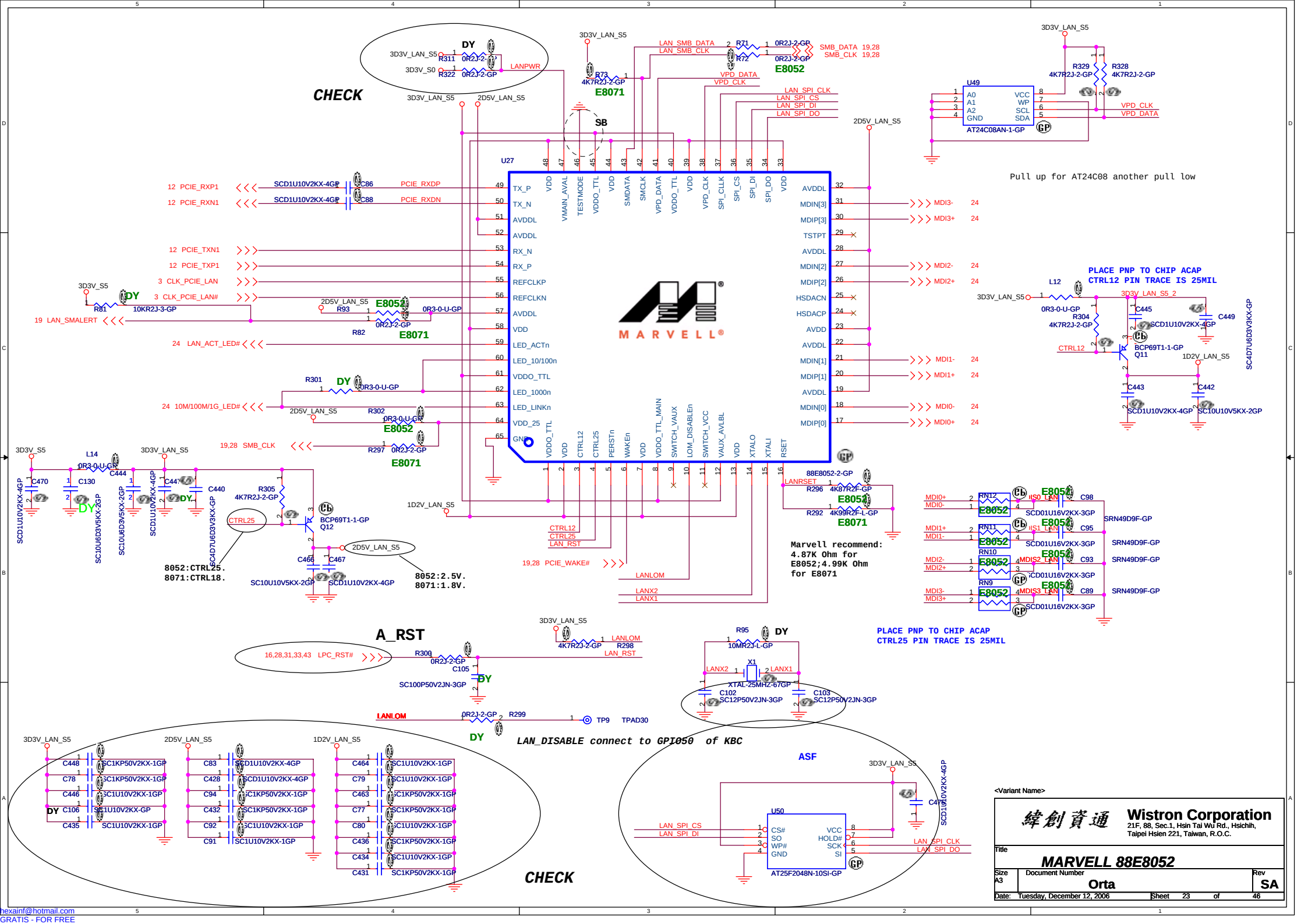


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC / BLUETOOTH**

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 22 of 46



<Variant Name>

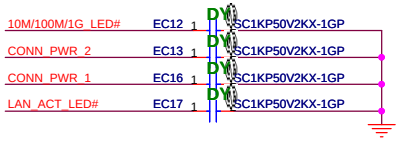
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

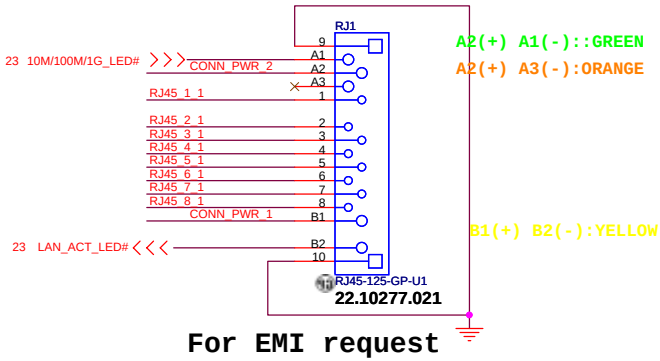
Title: MARVELL 88E8052

Size	Document Number	Rev
A3	Orta	SA

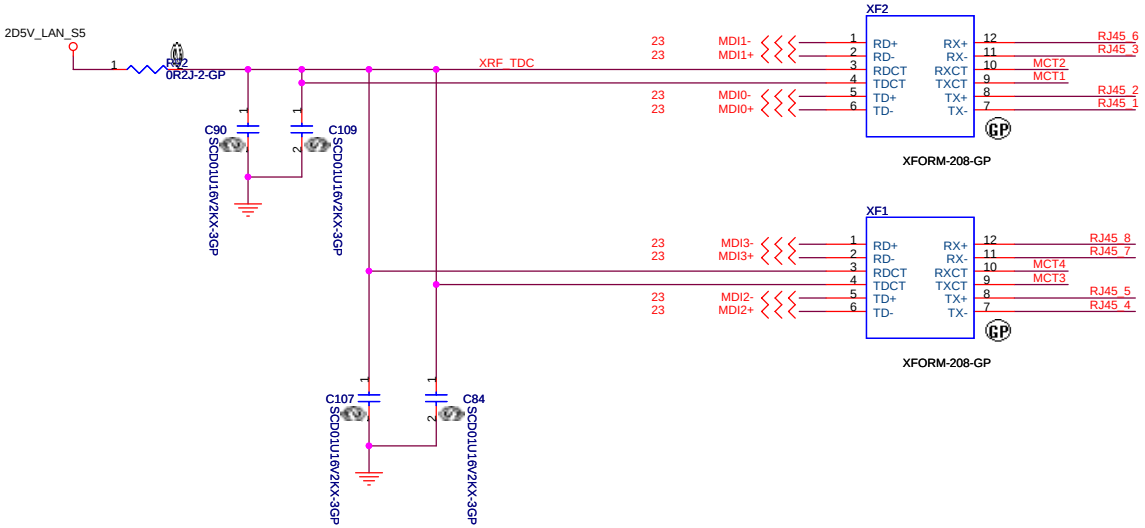
Date: Tuesday, December 12, 2006 Sheet 23 of 46

LAN Connector

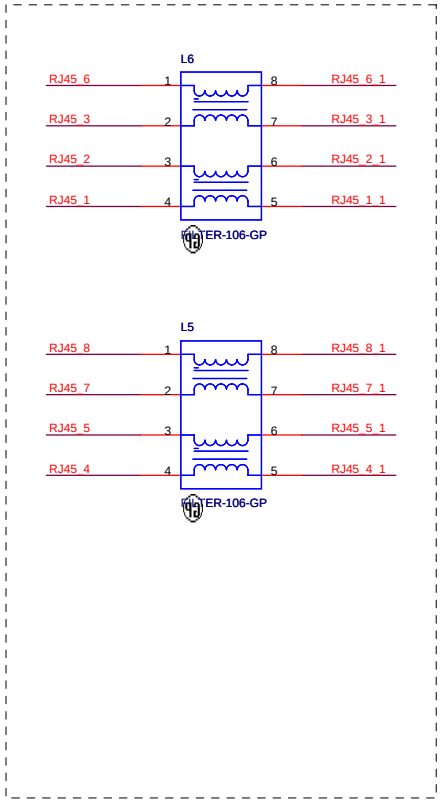




GIGA Lan Transformer



For EMI request

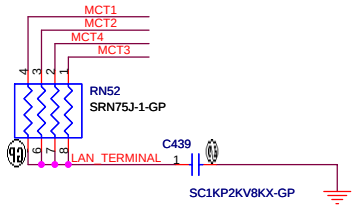


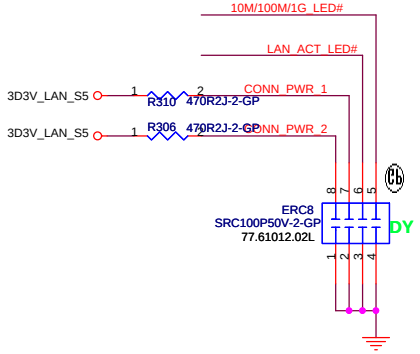
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





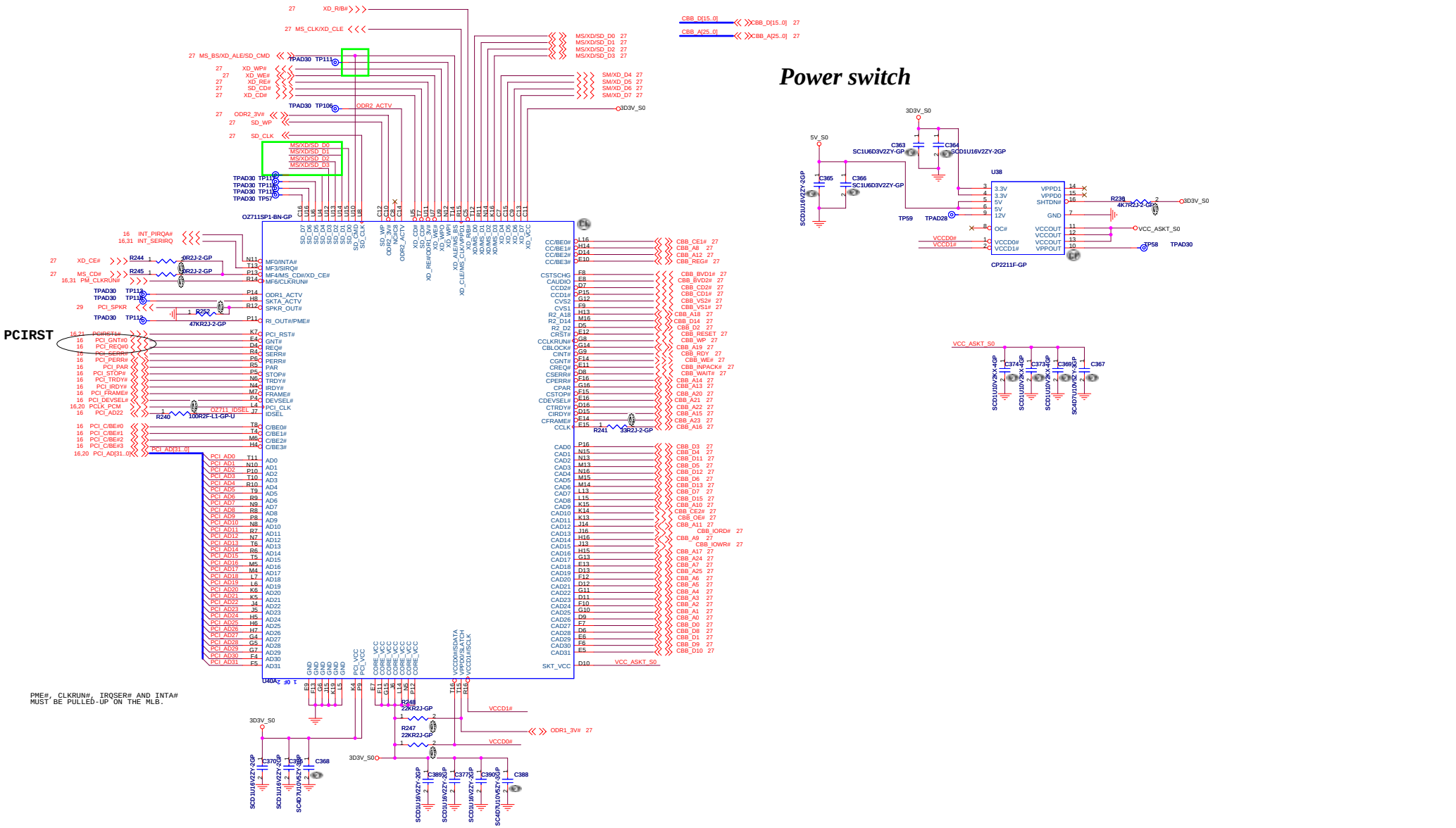
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 24 of 46



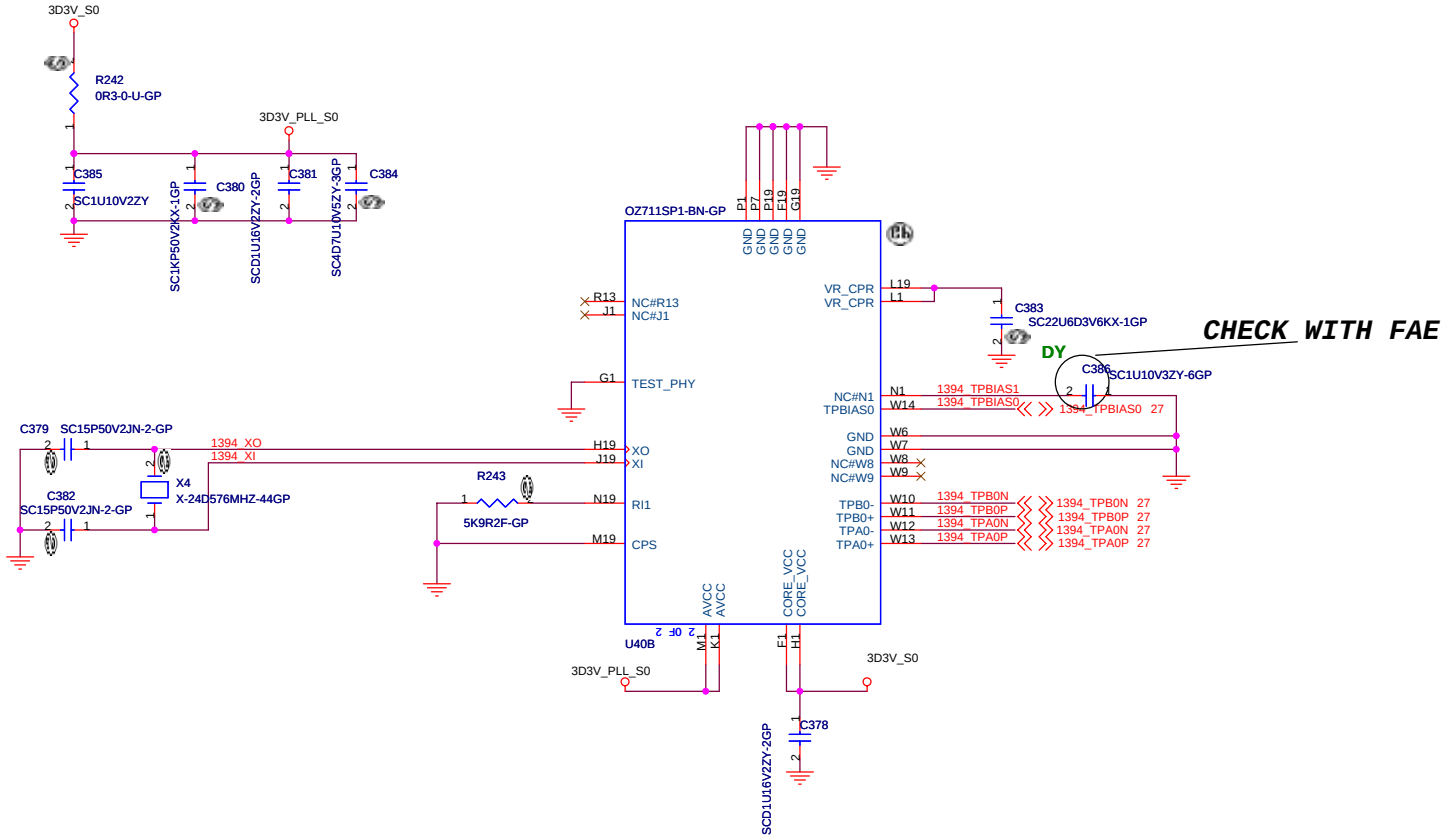
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: OZ711SP1 (1 of 2)

Size | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 25 of 46



<Variant Name>

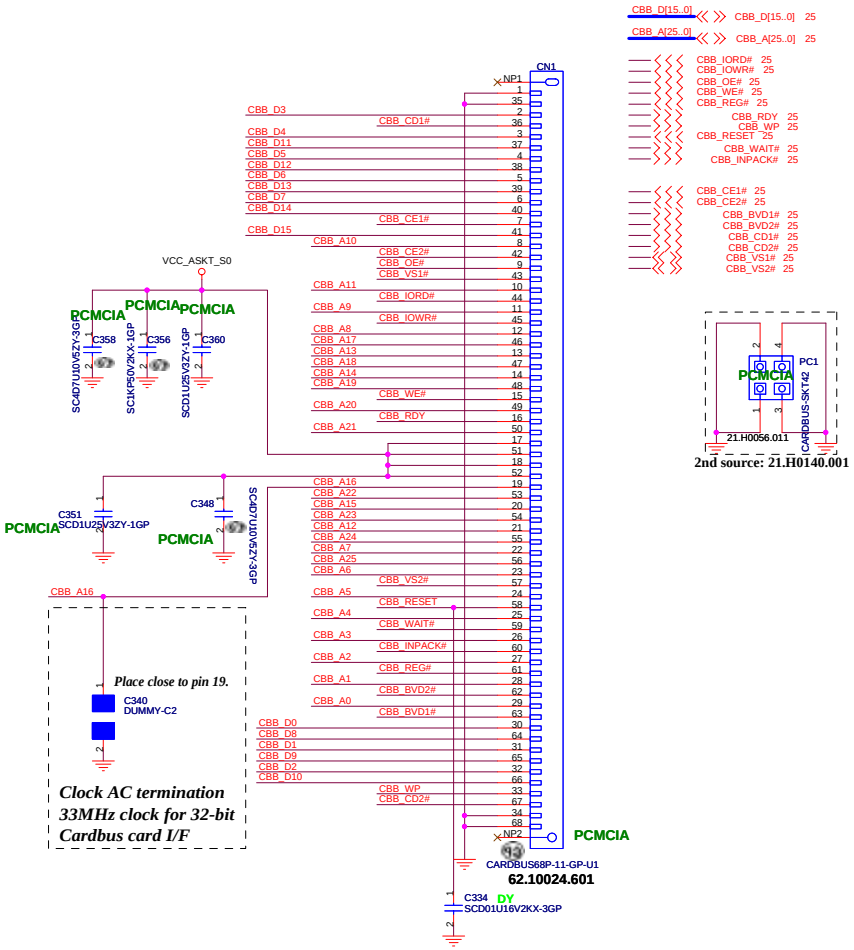
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *OZ711SP1 (2 of 2)*

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 26 of 46

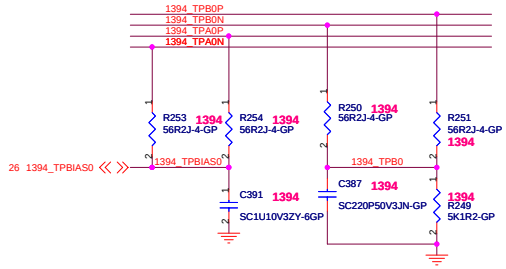
PCMCIA Socket

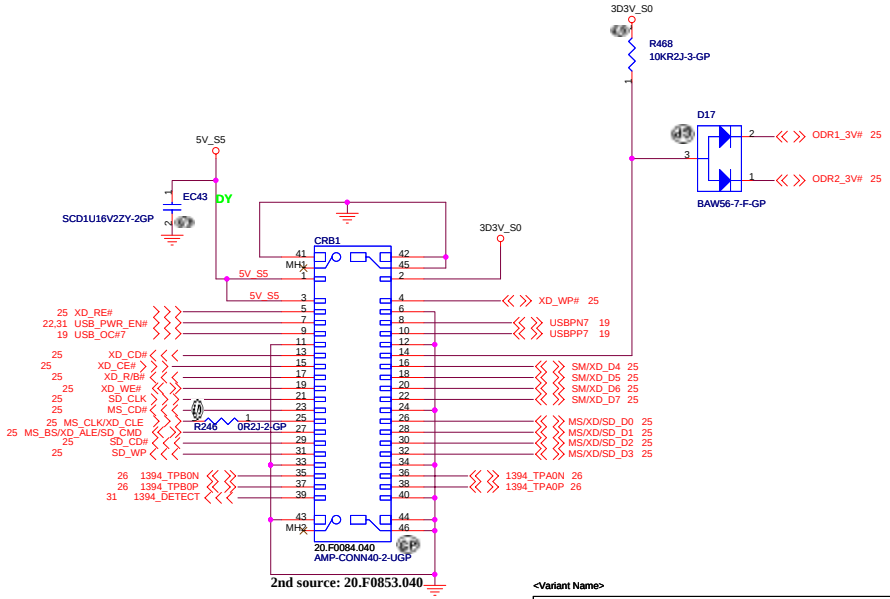


Cardbus I/F

2nd source: 21.H0140.001

CLOSE TO CHIP





2nd source: 20.F0853.040

XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

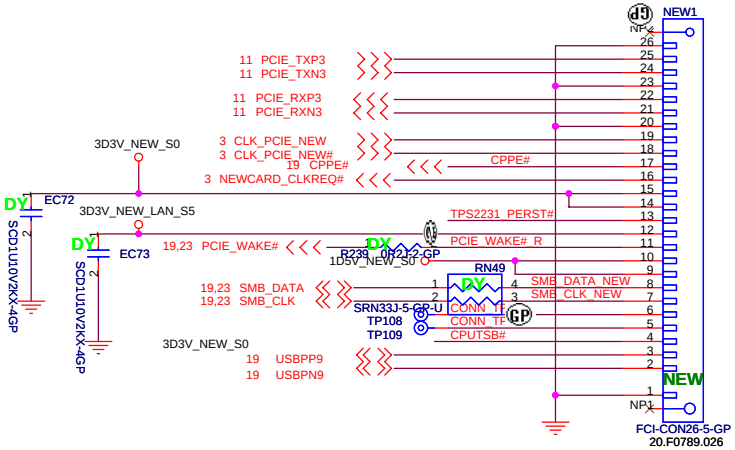
Size	Document Number	Rev
	Orta	SA

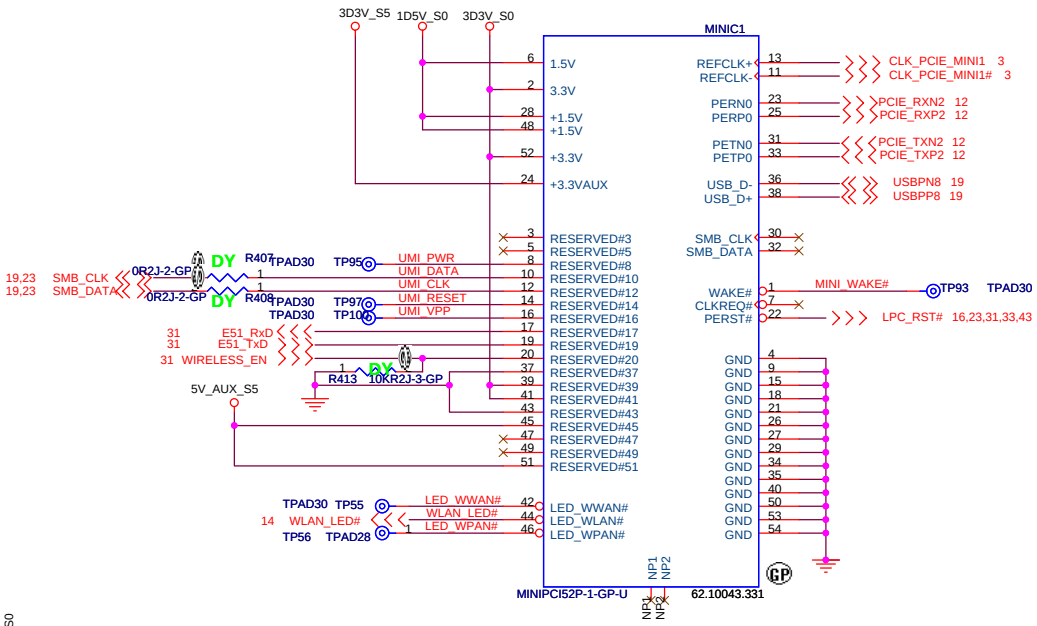
Date: Tuesday, December 12, 2006 Sheet 27 of 46

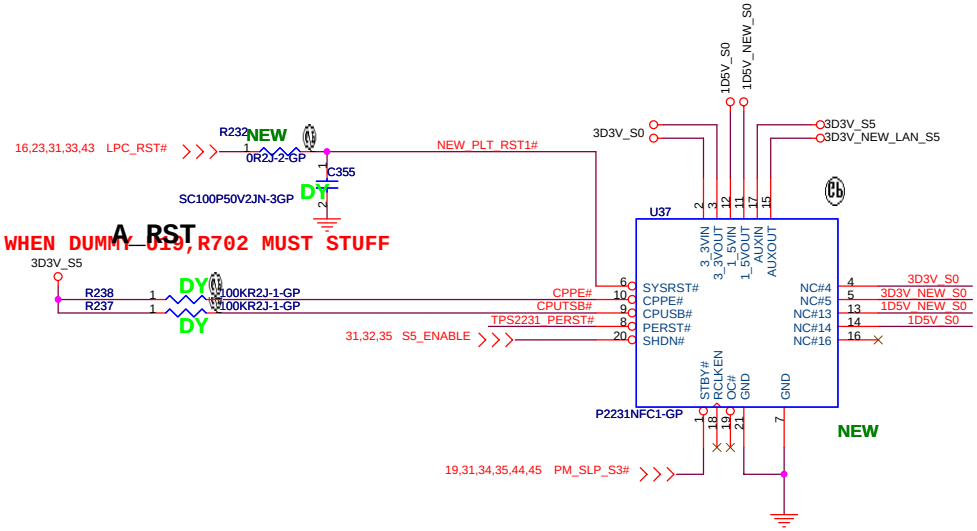
Mini Card Connector

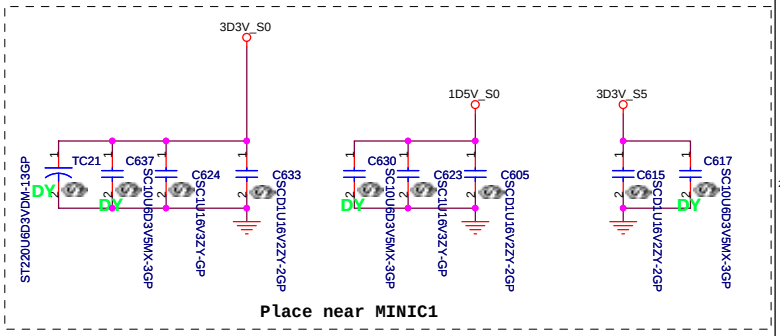
NEWCARD Connector

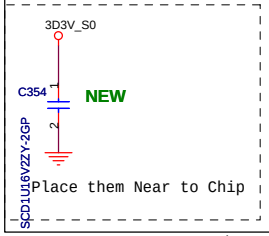
Reserve the symbol for bottom side connector

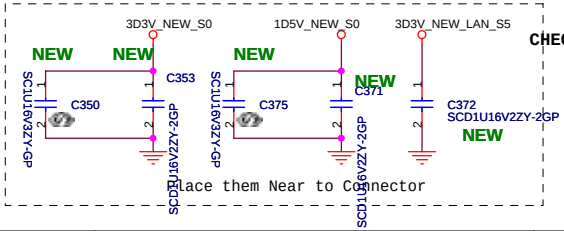








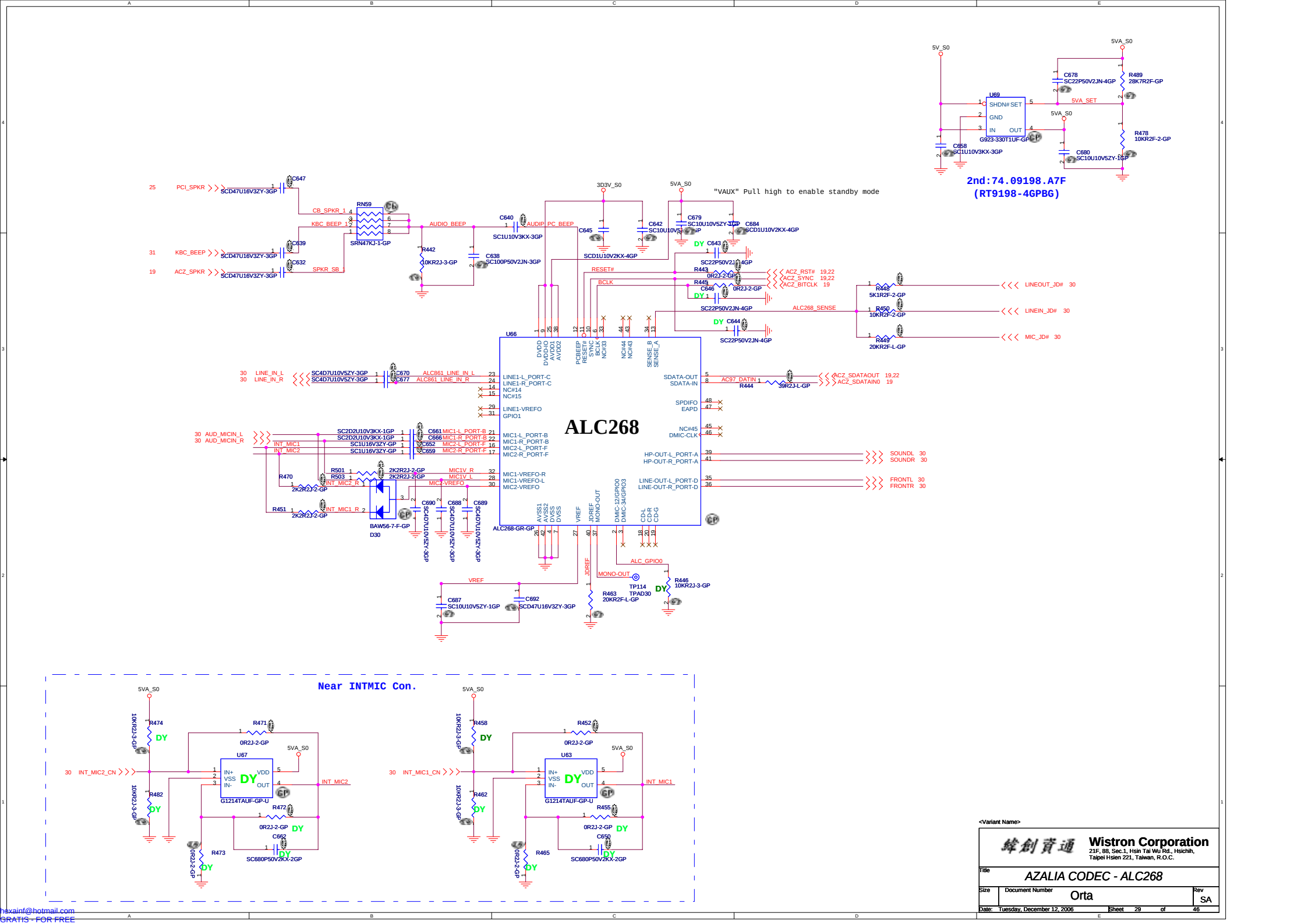




CHECK WITH COLUMBIA

bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size	Document Number **Orta**	Rev SA
Date: Tuesday, December 12, 2006	Sheet 28 of 46	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

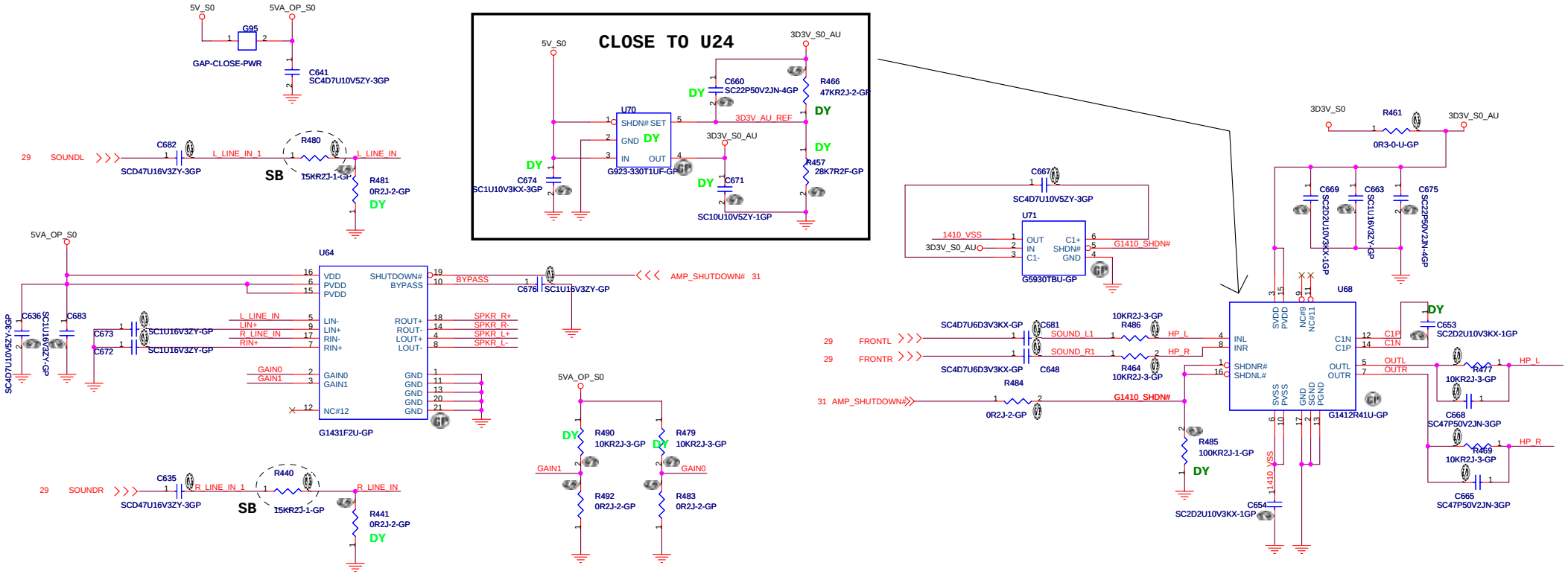
Title: AZALIA CODEC - ALC268

Size	Document Number	Rev
	Orta	SA

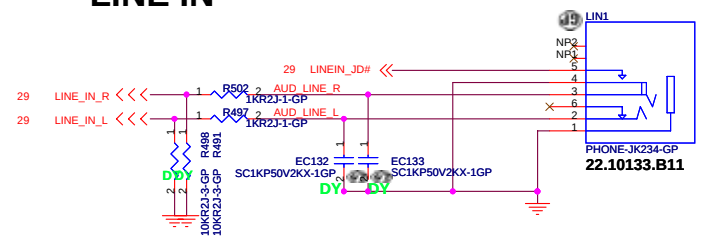
Date: Tuesday, December 12, 2006 Sheet 29 of 46

AUDIO OP AMPLIFIER

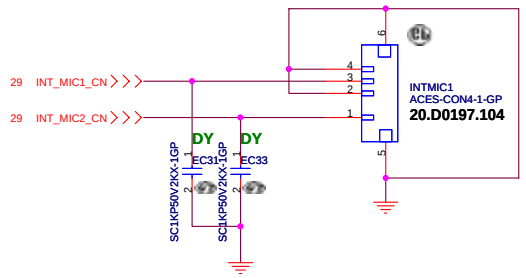
KBC_MUTE_GPIO8



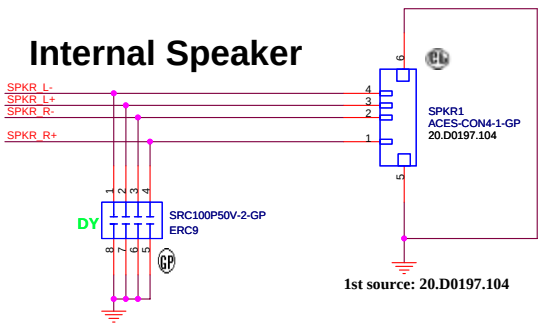
LINE IN



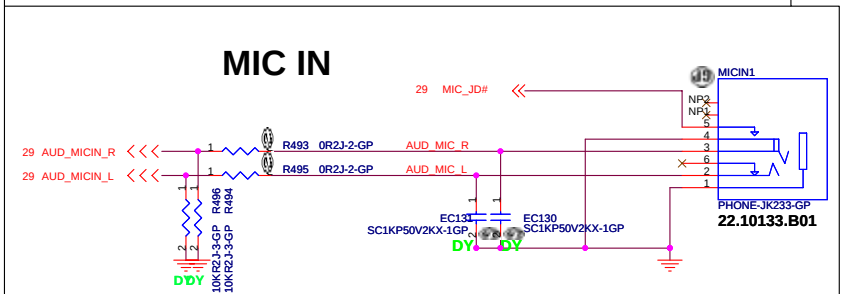
Internal Microphone



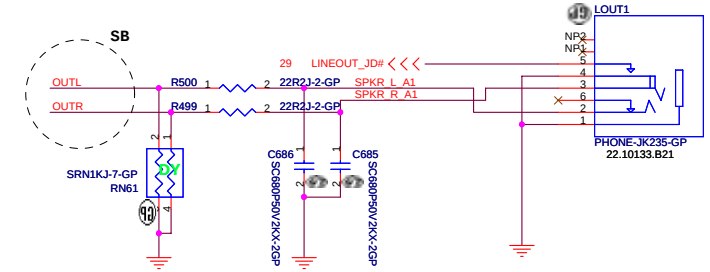
Internal Speaker



MIC IN



LINE OUT



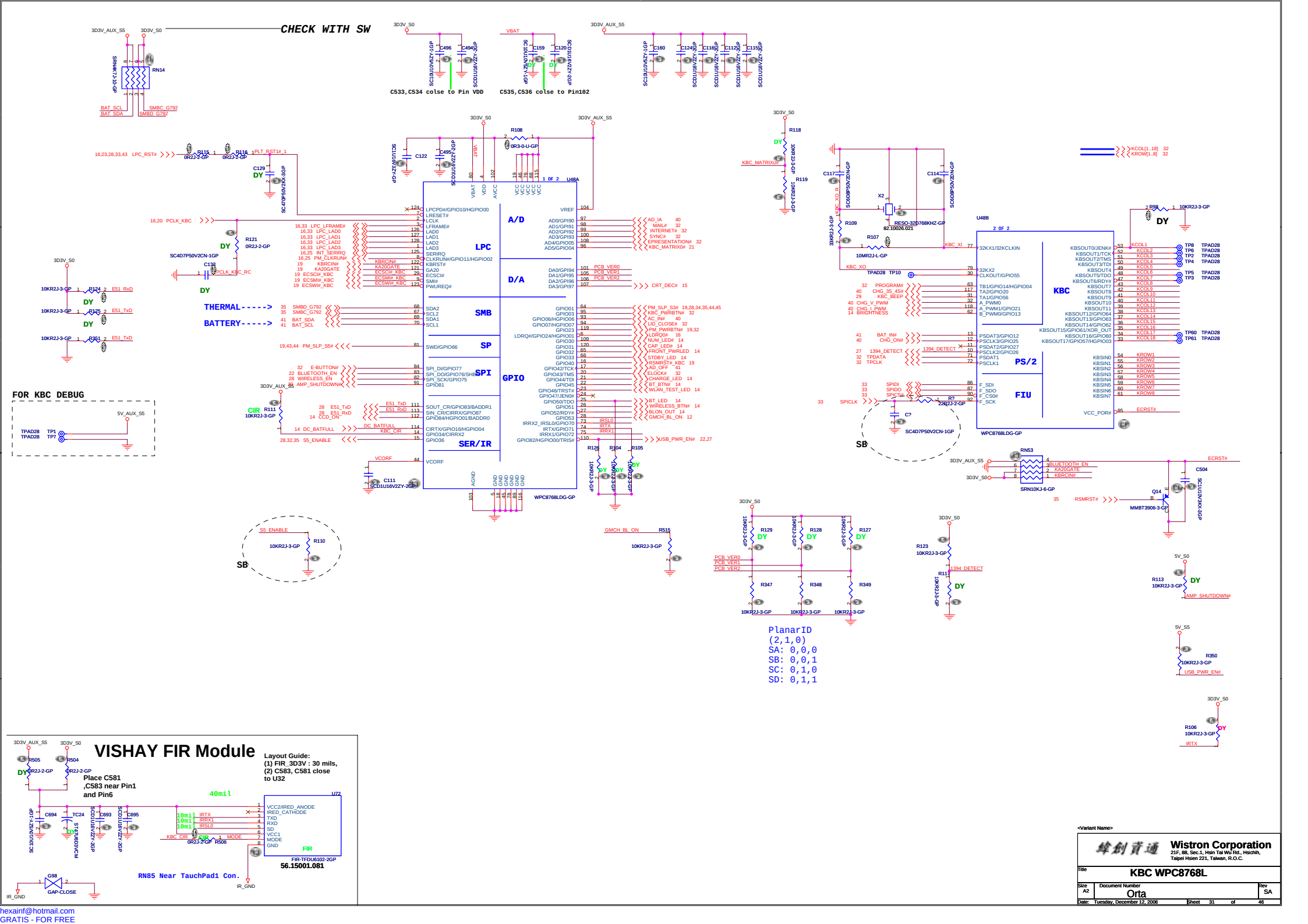
<Variant Name>

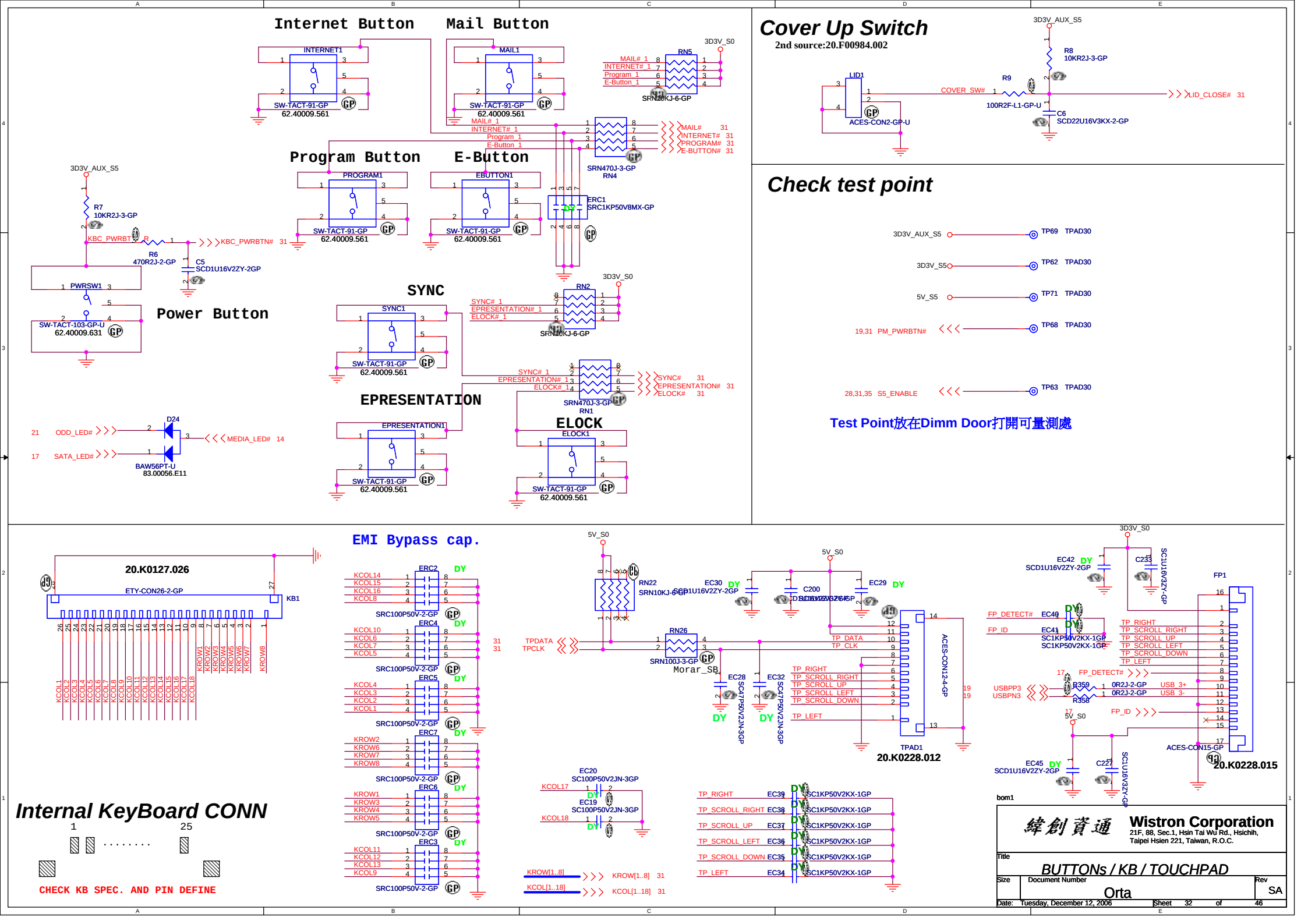
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

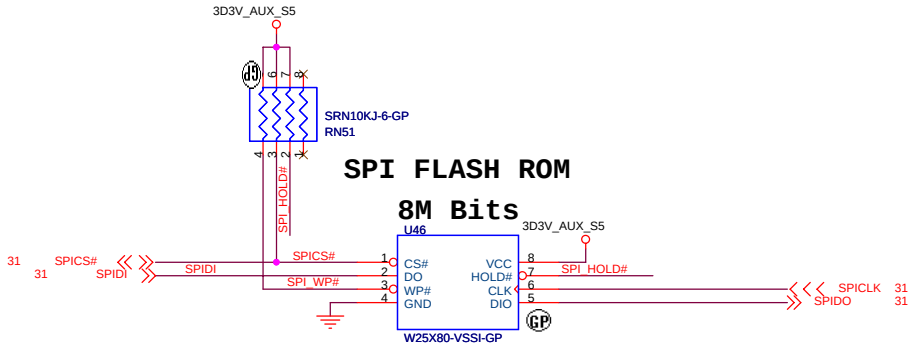
Title: *AUDIO AMP AND JACK*

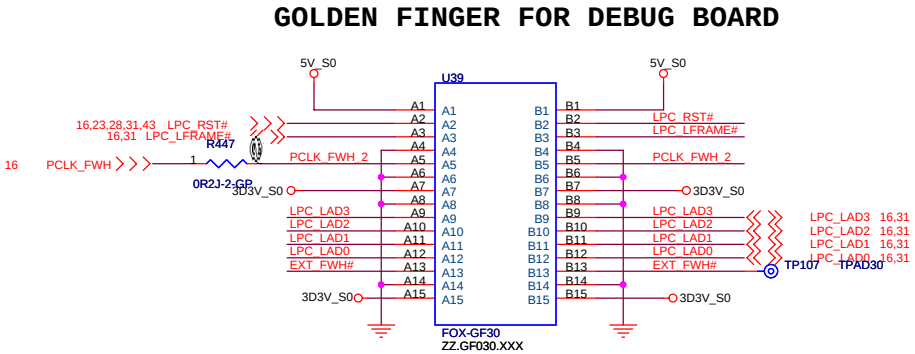
Size | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 30 of 46




Internet Button
Mail Button
Program Button
E-Button
Power Button
SYNC
EPRESENTATION
ELOCK
Cover Up Switch
2nd source:20.F00984.002
Check test point
Test Point放在Dimm Door打開可量測處
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
20.K0127.026
20.K0228.012
20.K0228.015
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
Orta
Tuesday, December 12, 2006



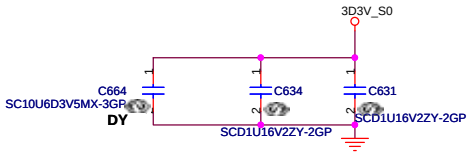


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

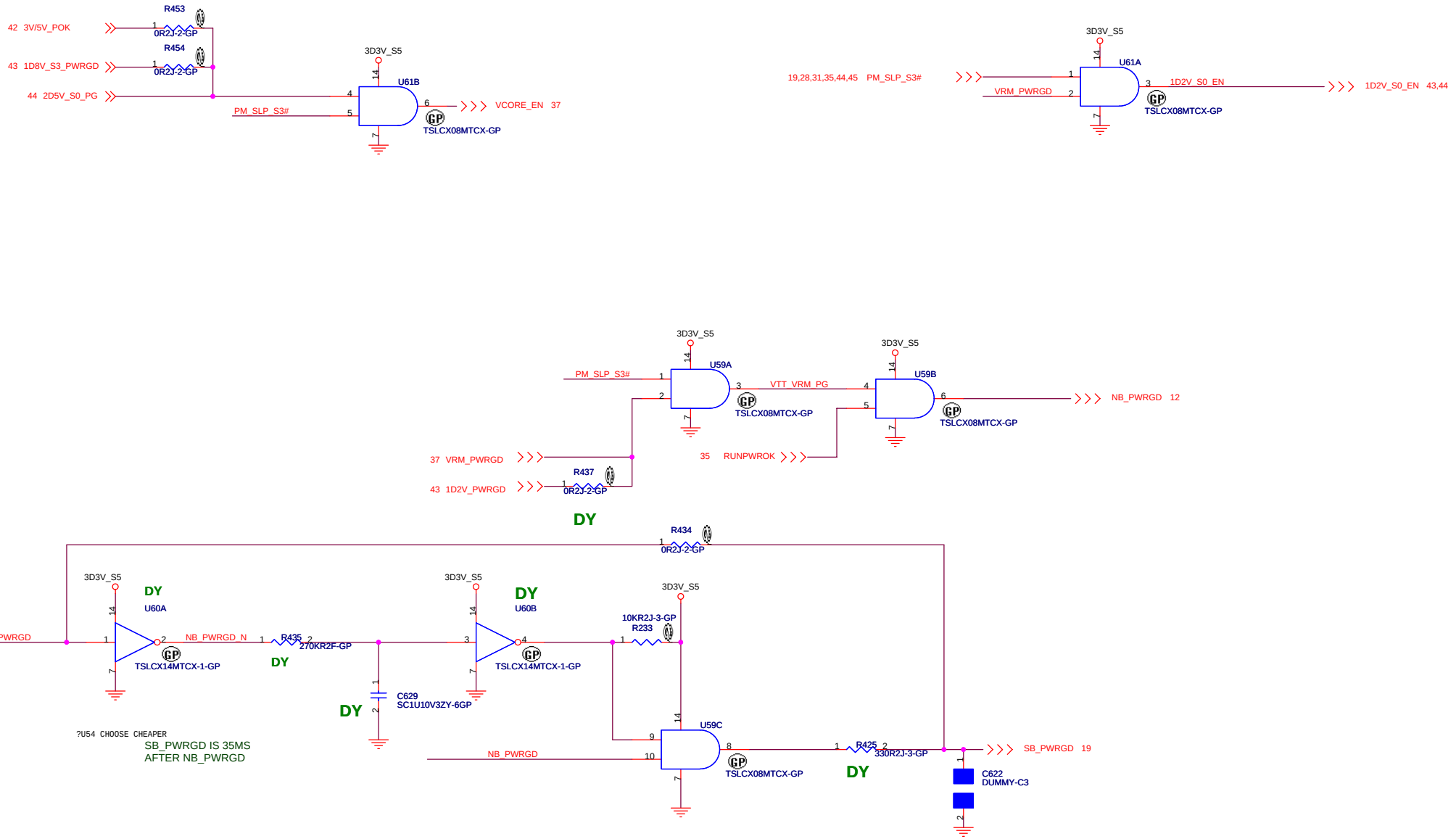
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 33 of 46	



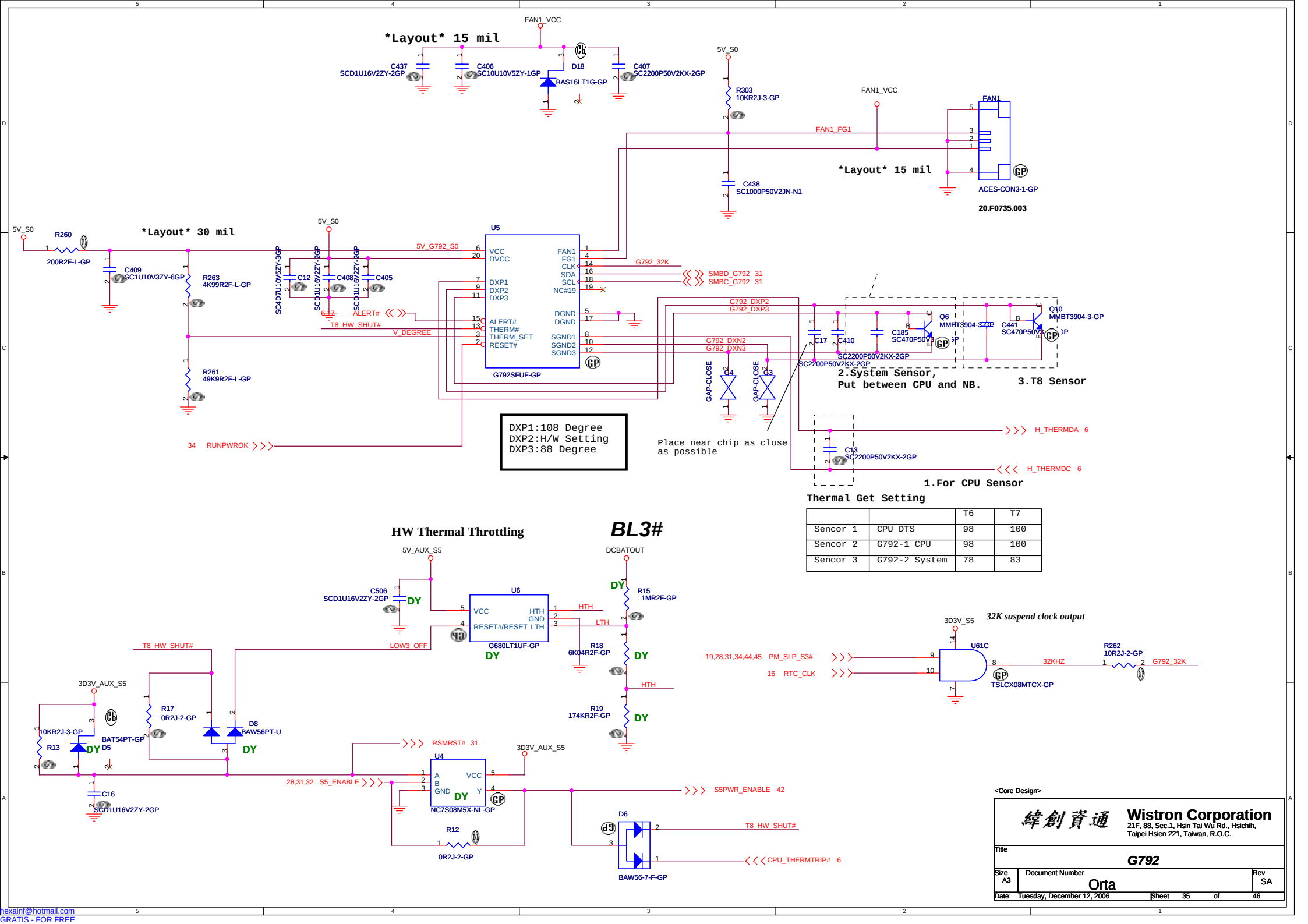
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 34 of 46



		T6	T7
Sencor 1	CPU DTS	98	100
Sencor 2	G792-1 CPU	98	100
Sencor 3	G792-2 System	78	83

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 35 of 46

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

Input Signal
(I)

Output Signal
(O)

AD_OFF
AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD_JK
5V_AUX_S5
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

1D2V (6.5A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

ISL6268_VGA_CORE

VGA_CORE_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

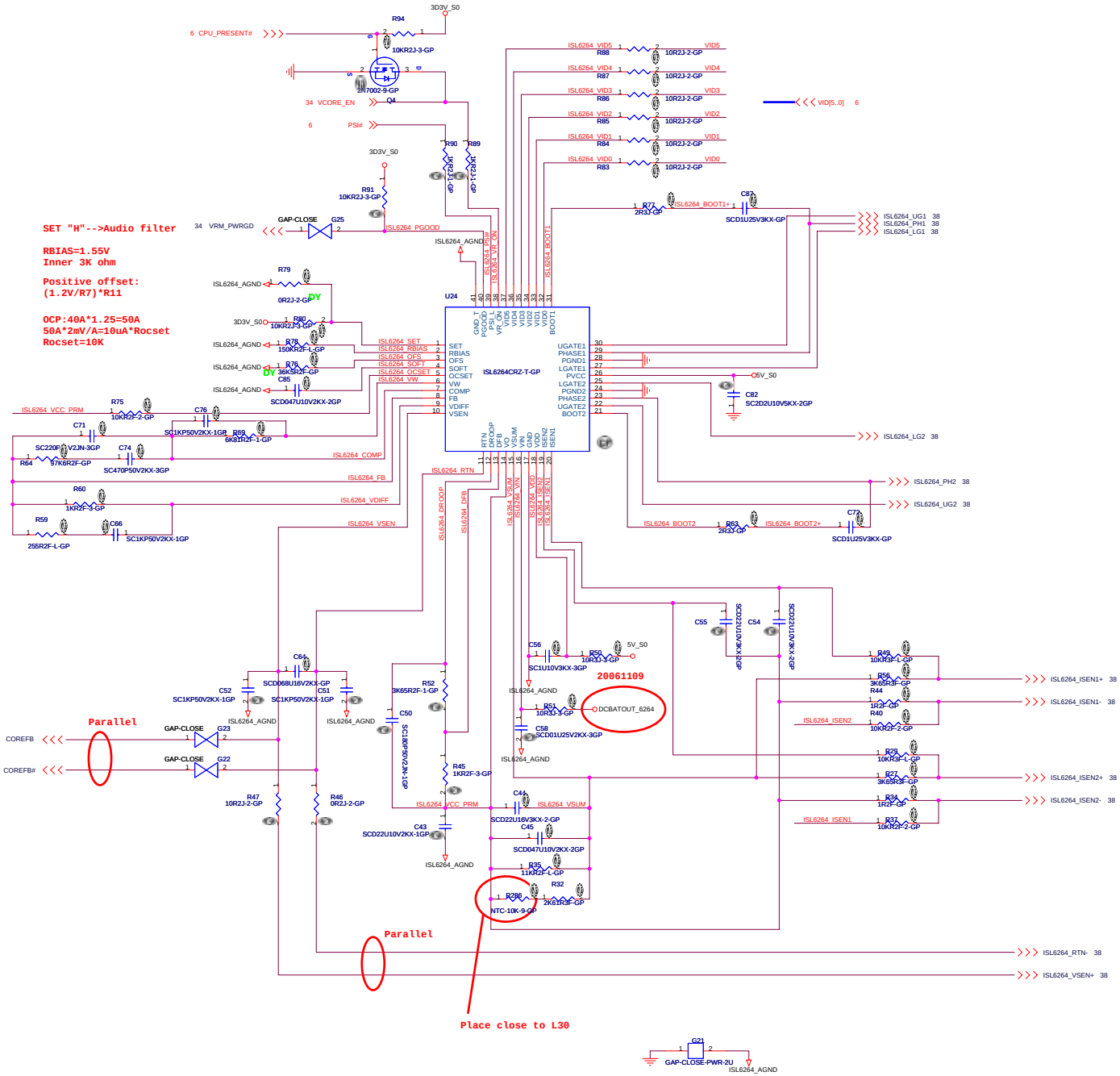
Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 36 of 46

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

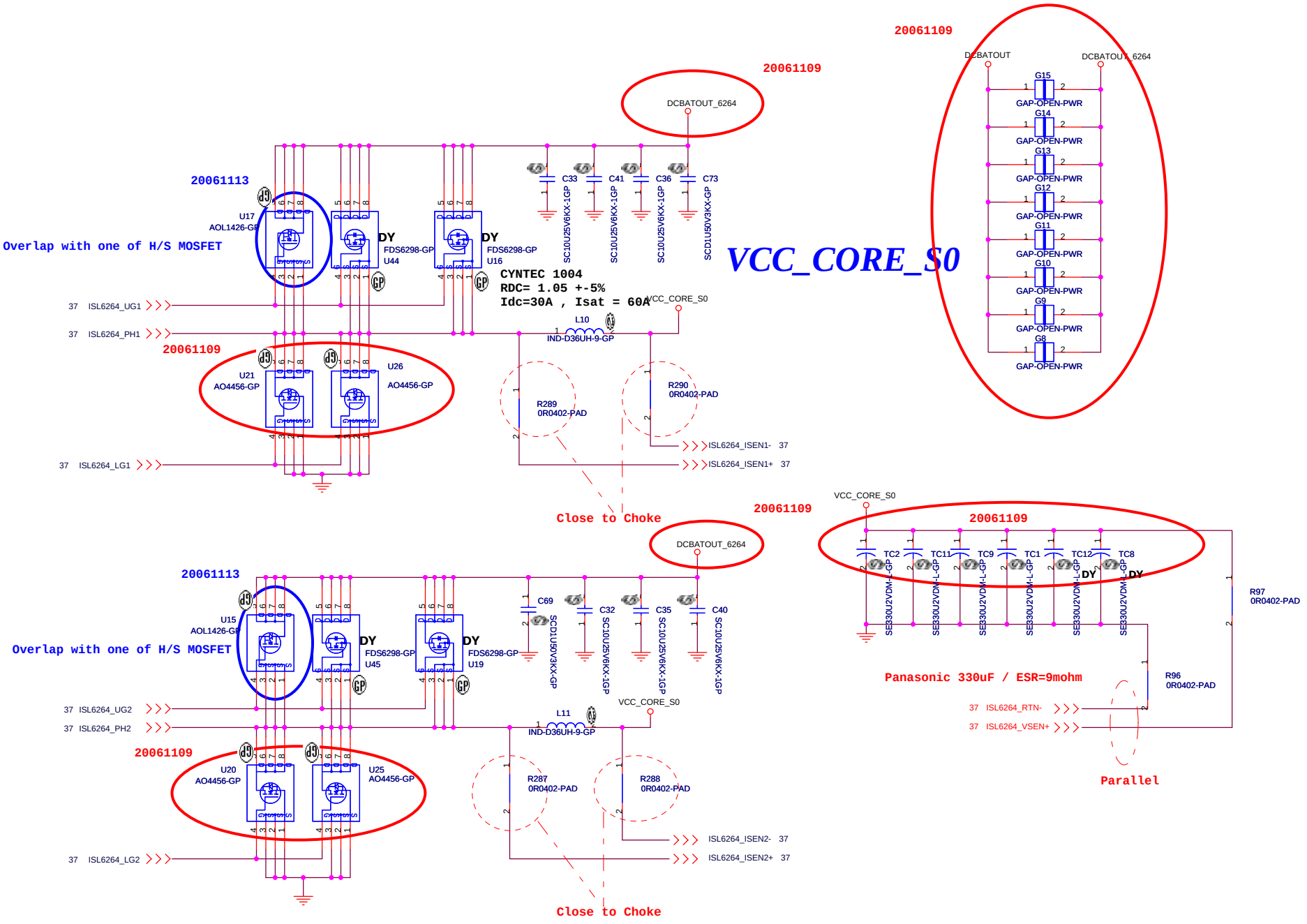
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1
Size: A2 | Document Number: Orta | Rev: SA
Date: Tuesday, December 12, 2006 | Sheet 37 of 46



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

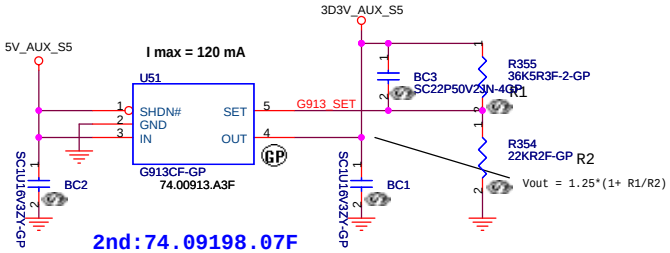
Title: *CPU Vcore Power_2*

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 38 of 46

Aux Power

3D3V_AUX_S5

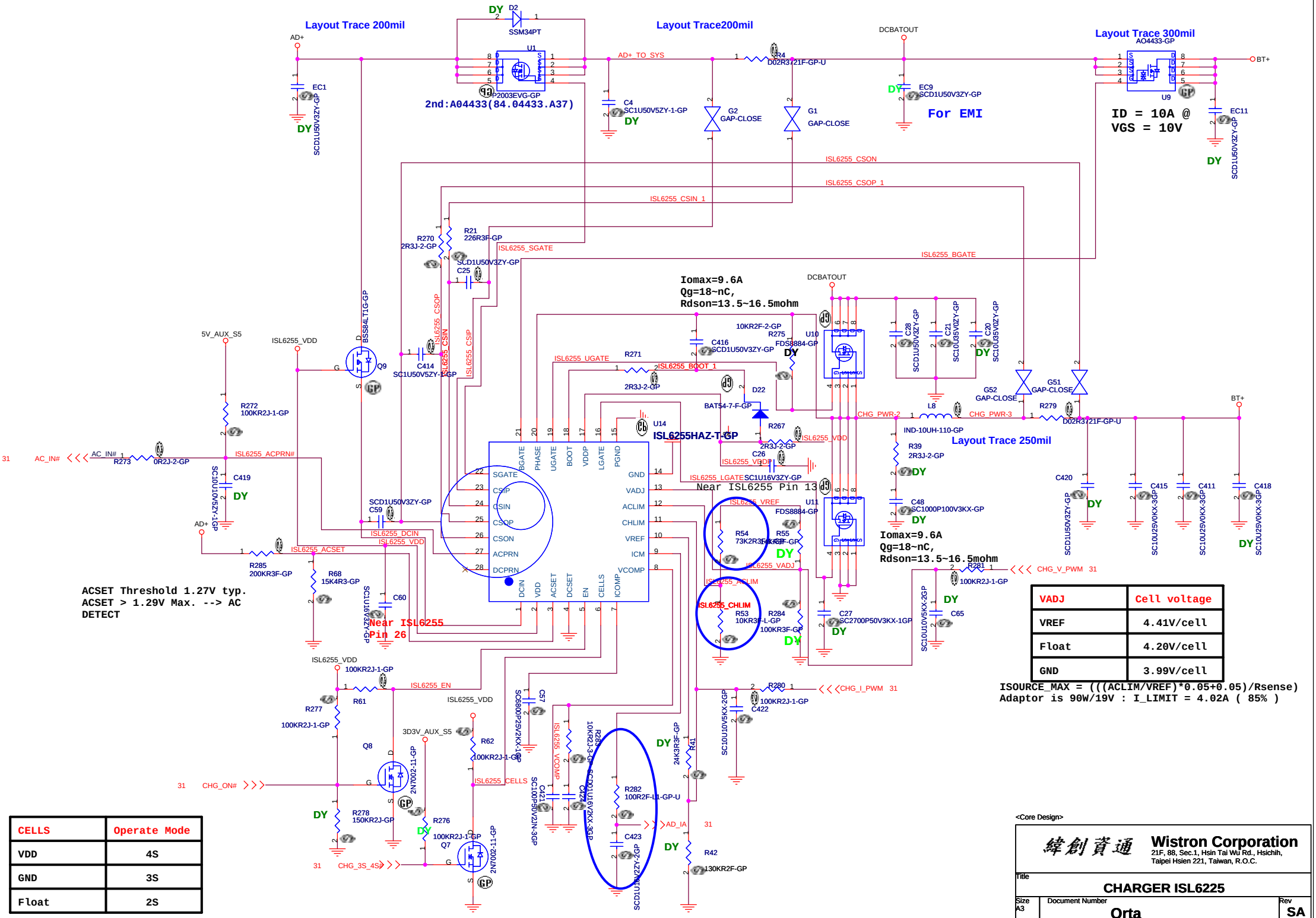


2nd:74.09198.07F
(RT9198-33PBG)

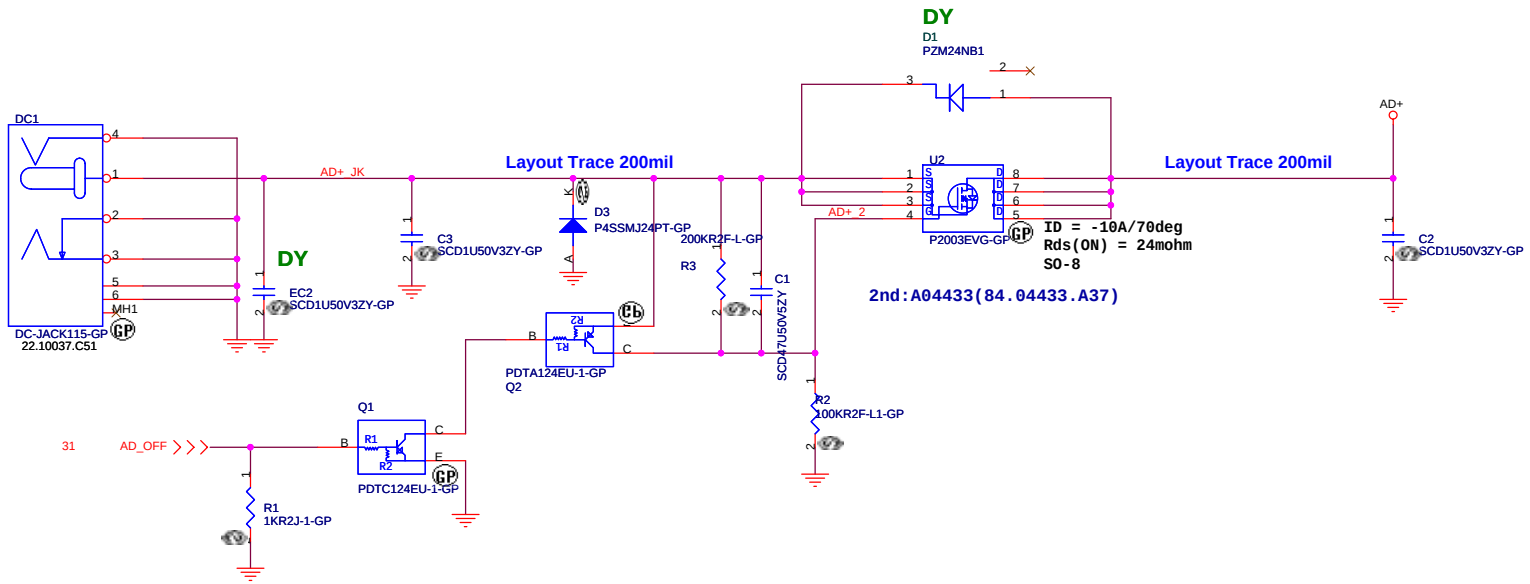
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

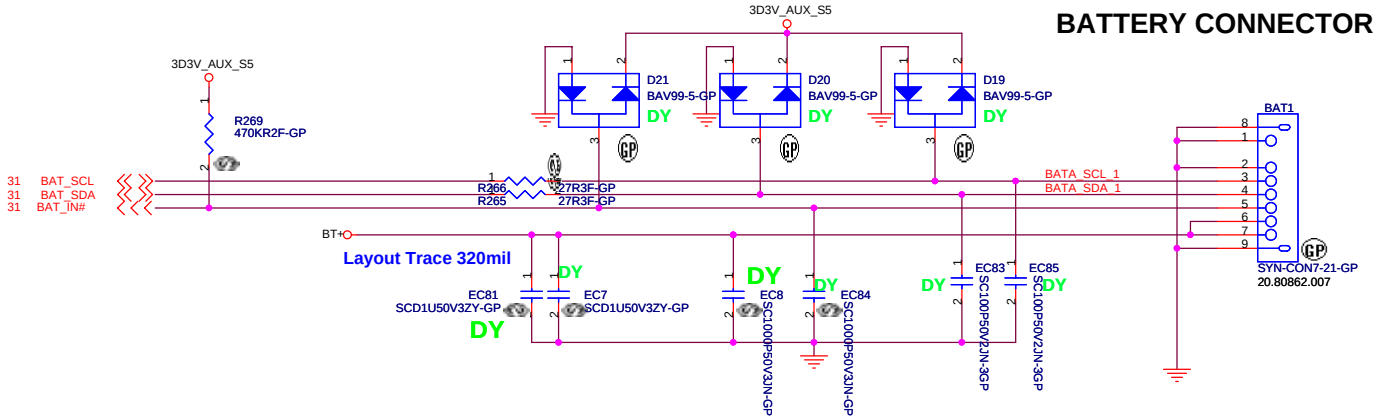
Title: *3D3V_AUX*		
Size: A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 39 of 46	


Layout Trace 200mil
Layout Trace200mil
Layout Trace 300mil
Layout Trace 250mil
2nd:A04433(84.04433.A37)
For EMI
ID = 10A @
VGS = 10V
Iomax=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
Near ISL6255 Pin 13
Near ISL6255
Pin 26
ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT
ISL6255HAZ-T-GP
AD+
AD+_TO_SYS
DCBATOUT
BT+
5V_AUX_S5
3D3V_AUX_S5
ISL6255_VDD
ISL6255_CSON
ISL6255_CSOP_1
ISL6255_CSIN_1
ISL6255_SGATE
ISL6255_BGATE
ISL6255_UGATE
ISL6255_BOOT_1
ISL6255_LGATE
ISL6255_VREF
ISL6255_VADJ
ISL6255_ACLIM
ISL6255_CHLIM
ISL6255_ACPRN#
ISL6255_DCIN
ISL6255_ACSET
ISL6255_EN
ISL6255_CELLS
CHG_PWR-2
CHG_PWR-3
AC_IN#
CHG_ON#
CHG_3S_4S
CHG_I_PWM
CHG_V_PWM
AD_IA
SSM34PT
AO4433-GP
FDS8884-GP
BSS84LT1G-GP
BAT54-7-F-GP
IND-10UH-110-GP
GAP-CLOSE
U1
U9
U10
U11
U14
Q7
Q8
Q9
D2
D22
EC1
EC9
EC11
C4
C414
C416
C419
C420
C422
C423
C424
C59
C60
C65
C25
R4
R21
R267
R270
R271
R272
R273
R275
R276
R277
R278
R279
R280
R281
R282
R284
R285
R39
R41
R42
R53
R54
R55
R61
R62
R68
C26
C27
C48
L8
G51
G52
VADJ
Cell voltage
VREF
4.41V/cell
Float
4.20V/cell
GND
3.99V/cell
ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)
CELLS
Operate Mode
VDD
4S
GND
3S
Float
2S
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER ISL6225
Size A3
Document Number
Orta
Rev SA
Date: Tuesday, December 12, 2006
Sheet 40 of 46

Adaptor in to generate DCBATOUT



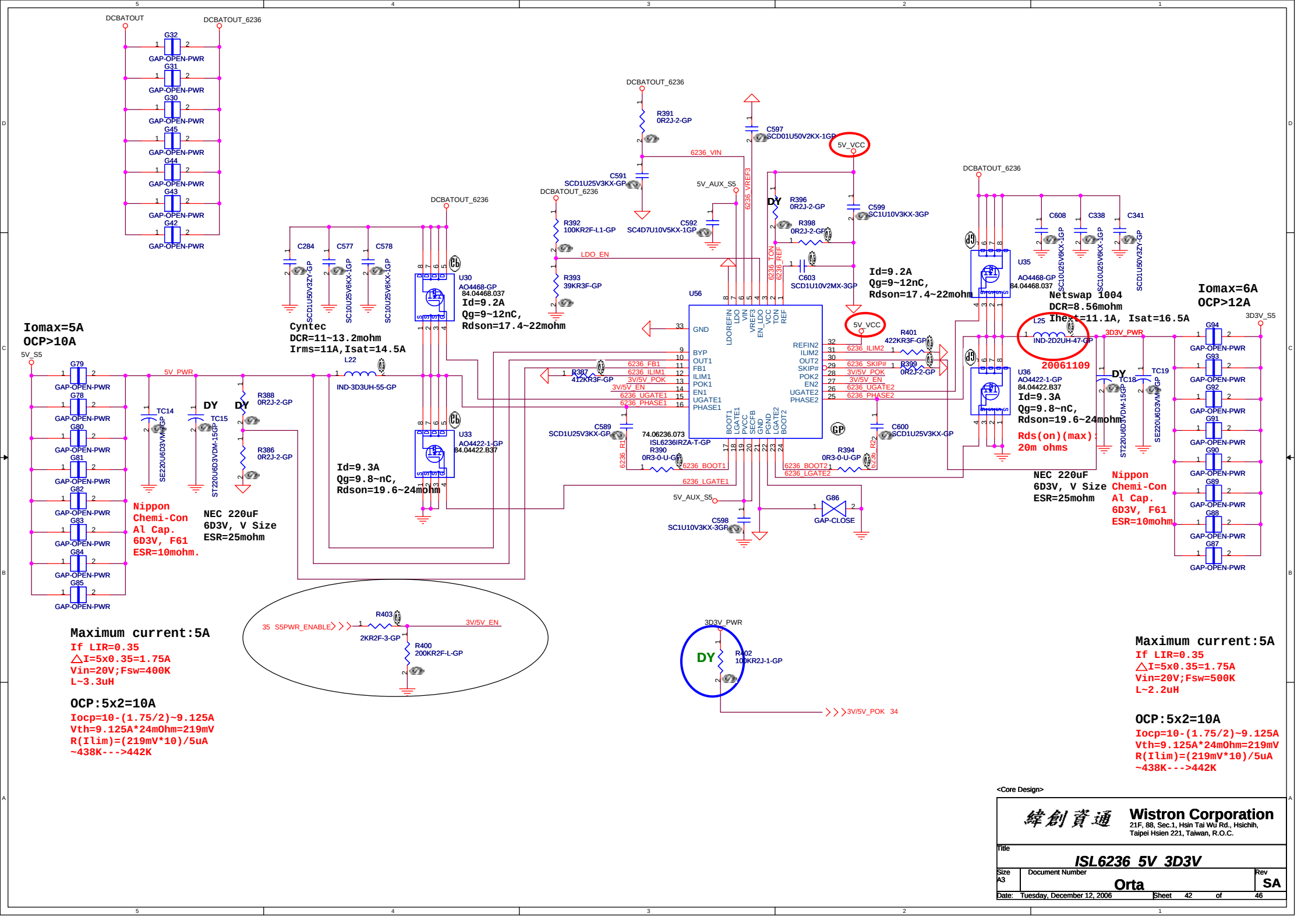
BATTERY CONNECTOR

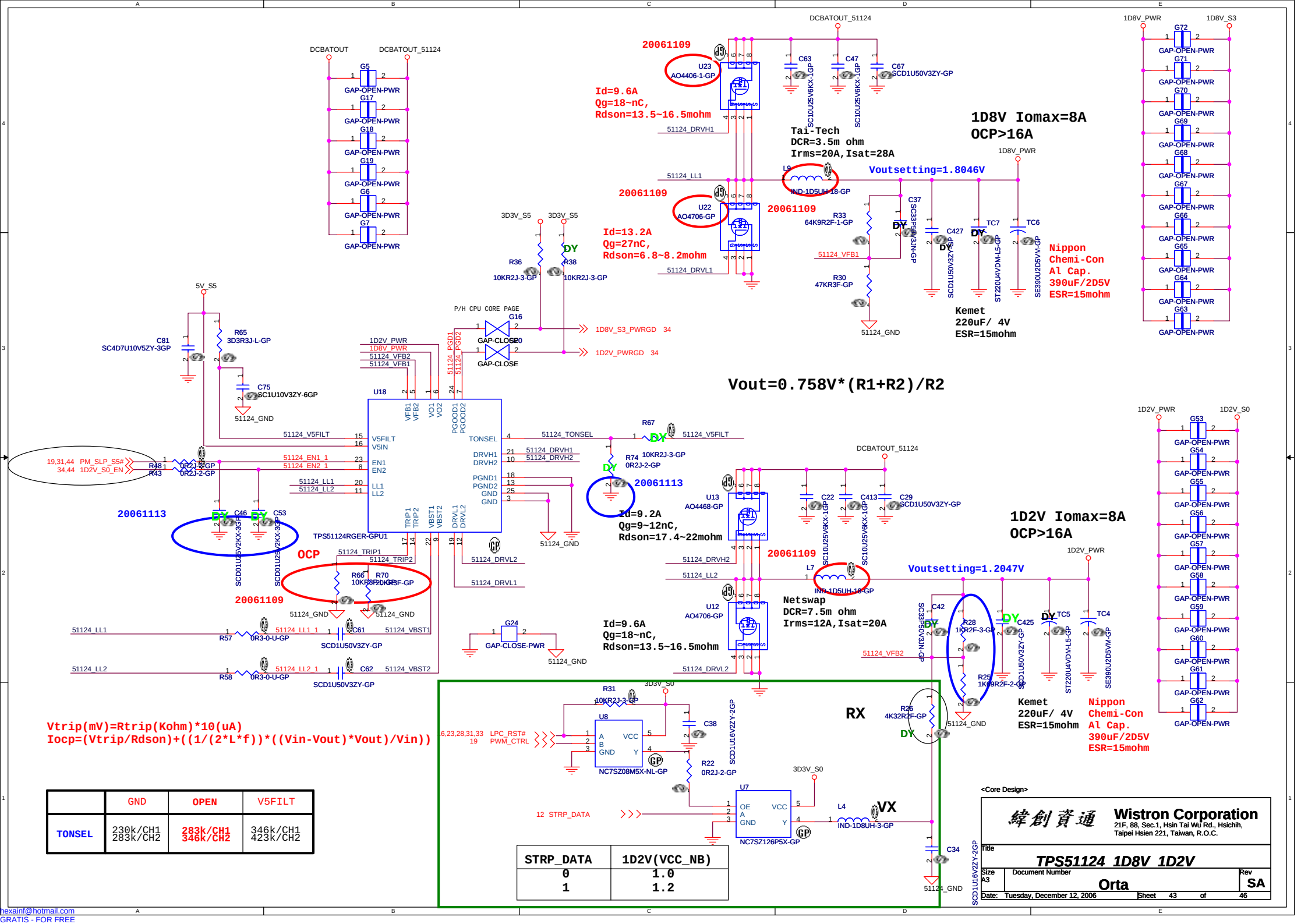


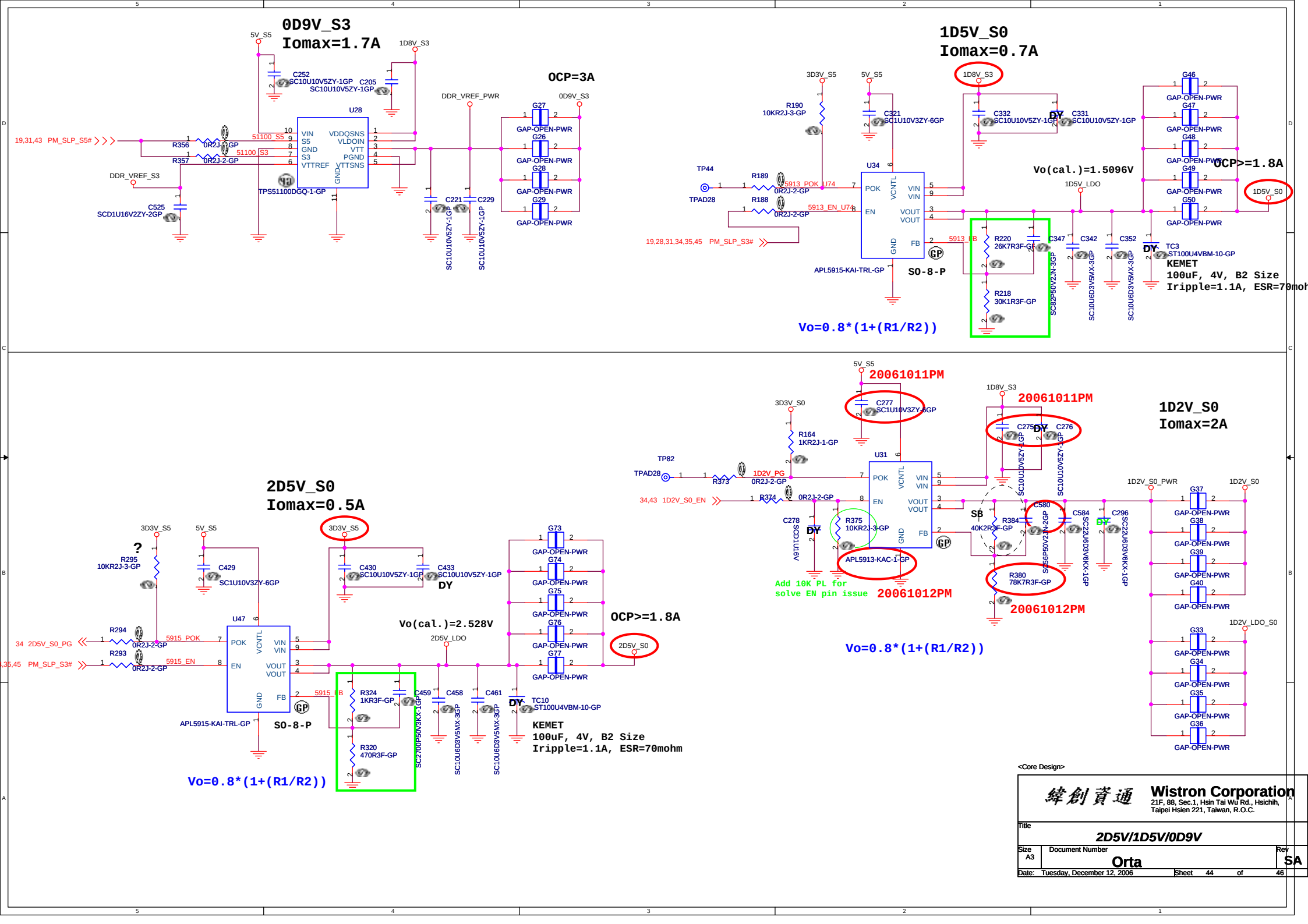
<Variant Name>

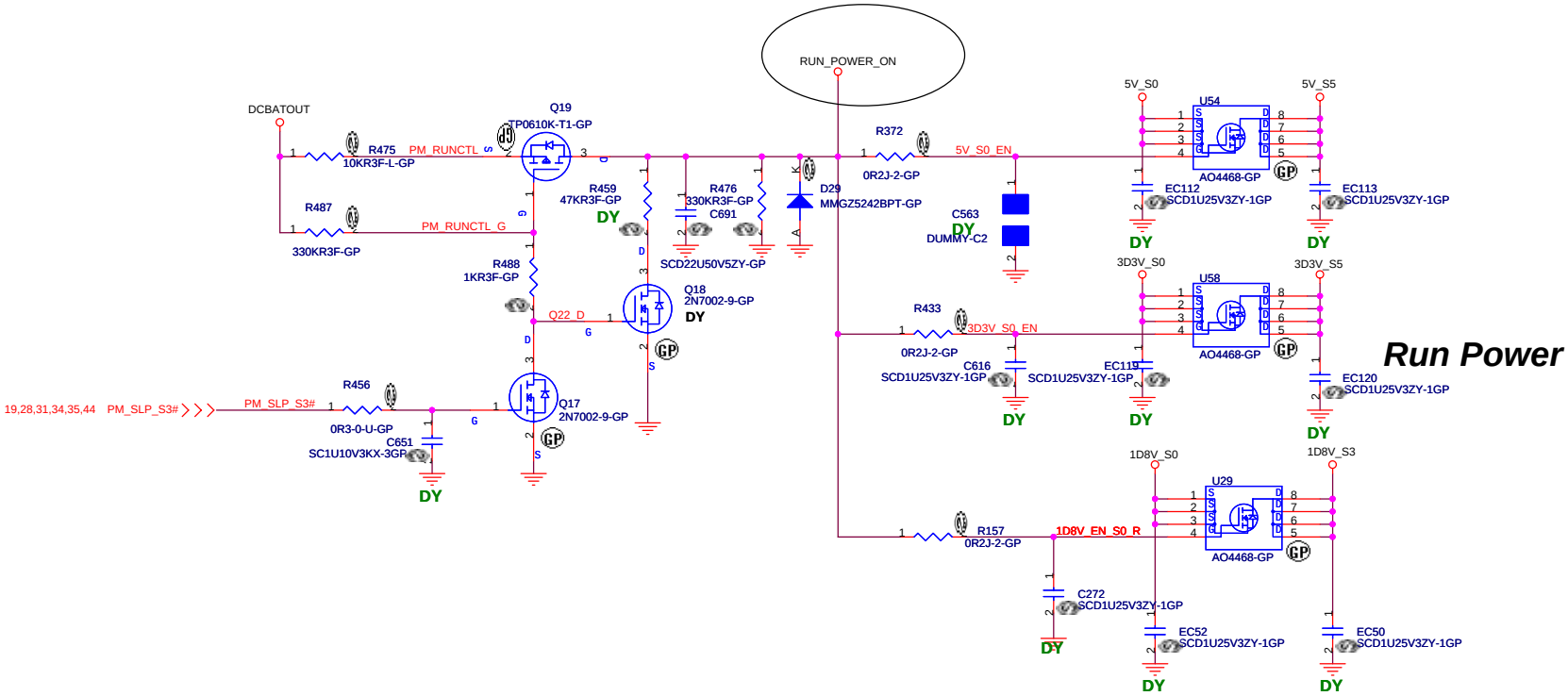
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Orta	Rev SA
Date: Tuesday, December 12, 2006	Sheet 41 of 46	

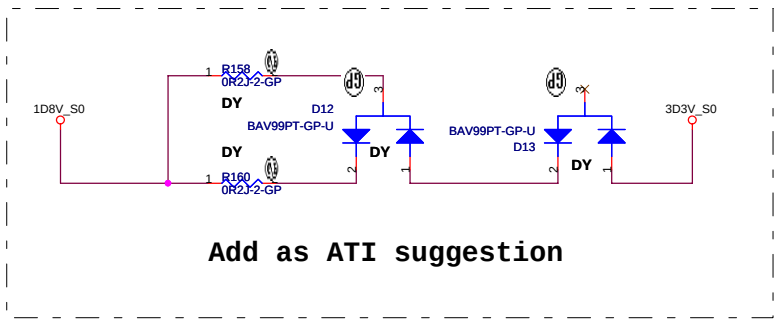

DCBATOUT
DCBATOUT_6236
G32 GAP-OPEN-PWR
G31 GAP-OPEN-PWR
G30 GAP-OPEN-PWR
G45 GAP-OPEN-PWR
G44 GAP-OPEN-PWR
G43 GAP-OPEN-PWR
G42 GAP-OPEN-PWR
Iomax=5A
OCP>10A
5V_S5
G79 GAP-OPEN-PWR
G78 GAP-OPEN-PWR
G80 GAP-OPEN-PWR
G81 GAP-OPEN-PWR
G82 GAP-OPEN-PWR
G83 GAP-OPEN-PWR
G84 GAP-OPEN-PWR
G85 GAP-OPEN-PWR
5V_PWR
TC14 SE220U6D3VM-GP
TC15 ST220U6D3VDM-15GP
DY
R388 0R2J-2-GP
R386 0R2J-2-GP
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
NEC 220uF 6D3V, V Size ESR=25mohm
L22 IND-3D3UH-55-GP
Cyntec DCR=11~13.2mohm Irms=11A,Isat=14.5A
C284 SCD1U50V3ZY-GP
C577 SC10U25V6KX-1GP
C578 SC10U25V6KX-1GP
U30 AO4468-GP 84.04468.037
Id=9.2A Qg=9~12nC, Rdson=17.4~22mohm
U33 AO4422-1-GP 84.04422.B37
Id=9.3A Qg=9.8~nC, Rdson=19.6~24mohm
R391 0R2J-2-GP
C591 SCD1U25V3KX-GP
R392 100KR2F-L1-GP
R393 39KR3F-GP
LDO_EN
C592 SC4D7U10V5KX-1GP
6236_VIN
5V_AUX_S5
C597 SCD01U50V2KX-1GP
5V_VCC
R396 0R2J-2-GP
R398 0R2J-2-GP
C599 SC1U10V3KX-3GP
C603 SCD1U10V2MX-3GP
U56
74.06236.073 ISL6236IRZA-T-GP
R387 412KR3F-GP
R390 0R3-0-U-GP
C589 SCD1U25V3KX-GP
C598 SC1U10V3KX-3GP
G86 GAP-CLOSE
R401 422KR3F-GP
R399 0R2J-2-GP
C600 SCD1U25V3KX-GP
R394 0R3-0-U-GP
6236_FB1
6236_ILIM1
3V/5V_POK
3V/5V_EN
6236_UGATE1
6236_PHASE1
6236_ILIM2
6236_SKIP#
6236_UGATE2
6236_PHASE2
6236_BOOT1
6236_LGATE1
6236_BOOT2
6236_LGATE2
R403 2KR2F-3-GP
R400 200KR2F-L-GP
35 S5PWR_ENABLE
3V/5V_EN
3D3V_PWR
R402 100KR2J-1-GP
3V/5V_POK 34
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
Id=9.2A Qg=9~12nC, Rdson=17.4~22mohm
U35 AO4468-GP 84.04468.037
C608 SC10U25V6KX-1GP
C338 SC10U25V6KX-1GP
C341 SCD1U50V3ZY-GP
Netswap 1004 DCR=8.56mohm Ihent=11.1A, Isat=16.5A
L25 IND-2D2UH-47-GP
20061109
U36 AO4422-1-GP 84.04422.B37
Id=9.3A Qg=9.8~nC, Rdson=19.6~24mohm
Rds(on)(max): 20m ohms
TC18 ST220U6D3VDM-15GP
TC19 SE220U6D3VM-GP
NEC 220uF 6D3V, V Size ESR=25mohm
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm
Iomax=6A
OCP>12A
3D3V_S5
3D3V_PWR
G94 GAP-OPEN-PWR
G93 GAP-OPEN-PWR
G92 GAP-OPEN-PWR
G91 GAP-OPEN-PWR
G90 GAP-OPEN-PWR
G89 GAP-OPEN-PWR
G88 GAP-OPEN-PWR
G87 GAP-OPEN-PWR
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6236 5V 3D3V
Size A3
Document Number
Orta
Rev SA
Date: Tuesday, December 12, 2006
Sheet 42 of 46


DCBATOUT
DCBATOUT_51124
20061109
U23
AO4406-1-GP
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
51124_DRVH1
Tai-Tech
DCR=3.5m ohm
Irms=20A,Isat=28A
1D8V Iomax=8A
OCP>16A
51124_LL1
L9
IND-1D5UH-18-GP
Voutsetting=1.8046V
1D8V_PWR
20061109
U22
AO4706-GP
Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm
51124_DRVL1
R33
64K9R2F-1-GP
51124_VFB1
R30
47KR3F-GP
51124_GND
Kemet
220uF/ 4V
ESR=15mohm
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm
Vout=0.758V*(R1+R2)/R2
5V_S5
C81
SC4D7U10V5ZY-3GP
R65
3D3R3J-L-GP
C75
SC1U10V3ZY-6GP
U18
TPS51124RGER-GPU1
VFB1
VFB2
VO1
VO2
PGOOD1
PGOOD2
V5FILT
V5IN
EN1
EN2
LL1
LL2
TONSEL
DRVH1
DRVH2
PGND1
PGND2
GND
TRIP1
TRIP2
VBST1
VBST2
DRVL1
DRVL2
R67
R74 10KR2J-3-GP
0R2J-2-GP
20061113
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
U13
AO4468-GP
20061109
L7
IND-1D5UH-18-GP
Voutsetting=1.2047V
Netswap
DCR=7.5m ohm
Irms=12A,Isat=20A
U12
AO4706-GP
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
1D2V Iomax=8A
OCP>16A
OCP
R66
R70
10KR3F-GP
R57
R58
0R3-0-U-GP
SCD1U50V3ZY-GP
SCD1U25V2KX-3GP
R31
10KR2J-3-GP
U8
NC7SZ08M5X-NL-GP
R22
0R2J-2-GP
U7
NC7SZ126P5X-GP
L4
IND-1D8UH-3-GP
RX
VX
R26
4K32R2F-GP
R28
1KR2F-3-GP
R25
1K99R2F-2-GP
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
TONSEL
GND
OPEN
V5FILT
230k/CH1
283k/CH2
283k/CH1
346k/CH2
346k/CH1
423k/CH2
STRP_DATA
1D2V(VCC_NB)
0
1.0
1
1.2
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51124 1D8V 1D2V
Orta
Size A3
Document Number
Rev SA
Date: Tuesday, December 12, 2006
Sheet 43 of 46
hexainf@hotmail.com
GRATIS - FOR FREE


0D9V_S3
Iomax=1.7A
OCP=3A
5V_S5
1D8V_S3
C252
SC10U10V5ZY-1GP
C205
SC10U10V5ZY-1GP
U28
DDR_VREF_PWR
0D9V_S3
19,31,43 PM_SLP_S5#
R356
0R2J-1-GP
R357
0R2J-2-GP
51100_S5
51100_S3
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
TPS51100DGQ-1-GP
DDR_VREF_S3
C525
SCD1U16V2ZY-2GP
C221
C229
SC10U10V5ZY-1GP
G27
G26
G28
G29
GAP-OPEN-PWR
1D5V_S0
Iomax=0.7A
Vo(cal.)=1.5096V
OCP>=1.8A
3D3V_S5
5V_S5
1D8V_S3
R190
10KR2J-3-GP
C321
SC1U10V3ZY-6GP
C332
SC10U10V5ZY-1GP
DY
C331
SC10U10V5ZY-1GP
TP44
TPAD28
R189
0R2J-2-GP
5913_POK_U74
R188
0R2J-2-GP
5913_EN_U74
19,28,31,34,35,45 PM_SLP_S3#
U34
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5915-KAI-TRL-GP
SO-8-P
5913_FB
R220
26K7R3F-GP
R218
30K1R3F-GP
SC82P50V2JN-3GP
1D5V_LDO
C347
C342
C352
SC10U6D3V5MX-3GP
TC3
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
G46
G47
G48
G49
G50
Vo=0.8*(1+(R1/R2))
2D5V_S0
Iomax=0.5A
Vo(cal.)=2.528V
OCP>=1.8A
3D3V_S5
5V_S5
R295
10KR2J-3-GP
C429
SC1U10V3ZY-6GP
C430
SC10U10V5ZY-1GP
C433
SC10U10V5ZY-1GP
DY
U47
34 2D5V_S0_PG
R294
0R2J-2-GP
R293
0R2J-2-GP
5915_POK
5915_EN
5915_FB
2D5V_LDO
2D5V_S0
R324
1KR3F-GP
R320
470R3F-GP
C459
C458
C461
SC2700P50V3KX-1GP
SC10U6D3V5MX-3GP
TC10
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
G73
G74
G75
G76
G77
Vo=0.8*(1+(R1/R2))
1D2V_S0
Iomax=2A
20061011PM
20061012PM
3D3V_S0
C277
SC1U10V3ZY-6GP
R164
1KR2J-1-GP
TP82
TPAD28
R373
1D2V_PG
0R2J-2-GP
34,43 1D2V_S0_EN
R374
0R2J-2-GP
U31
C278
SCD1U16V
R375
10KR2J-3-GP
APL5913-KAC-1-GP
Add 10K PL for
solve EN pin issue
C275
C276
SC10U10V5ZY-1GP
SB
40K2R3F-GP
R384
C580
C584
C296
SC22U6D3V6KX-1GP
R380
78K7R3F-GP
SC369P50V2JN-2GP
1D2V_S0_PWR
1D2V_LDO_S0
G37
G38
G39
G40
G33
G34
G35
G36
Vo=0.8*(1+(R1/R2))
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
2D5V/1D5V/0D9V
Size
A3
Document Number
Orta
Rev
SA
Date: Tuesday, December 12, 2006
Sheet 44 of 46



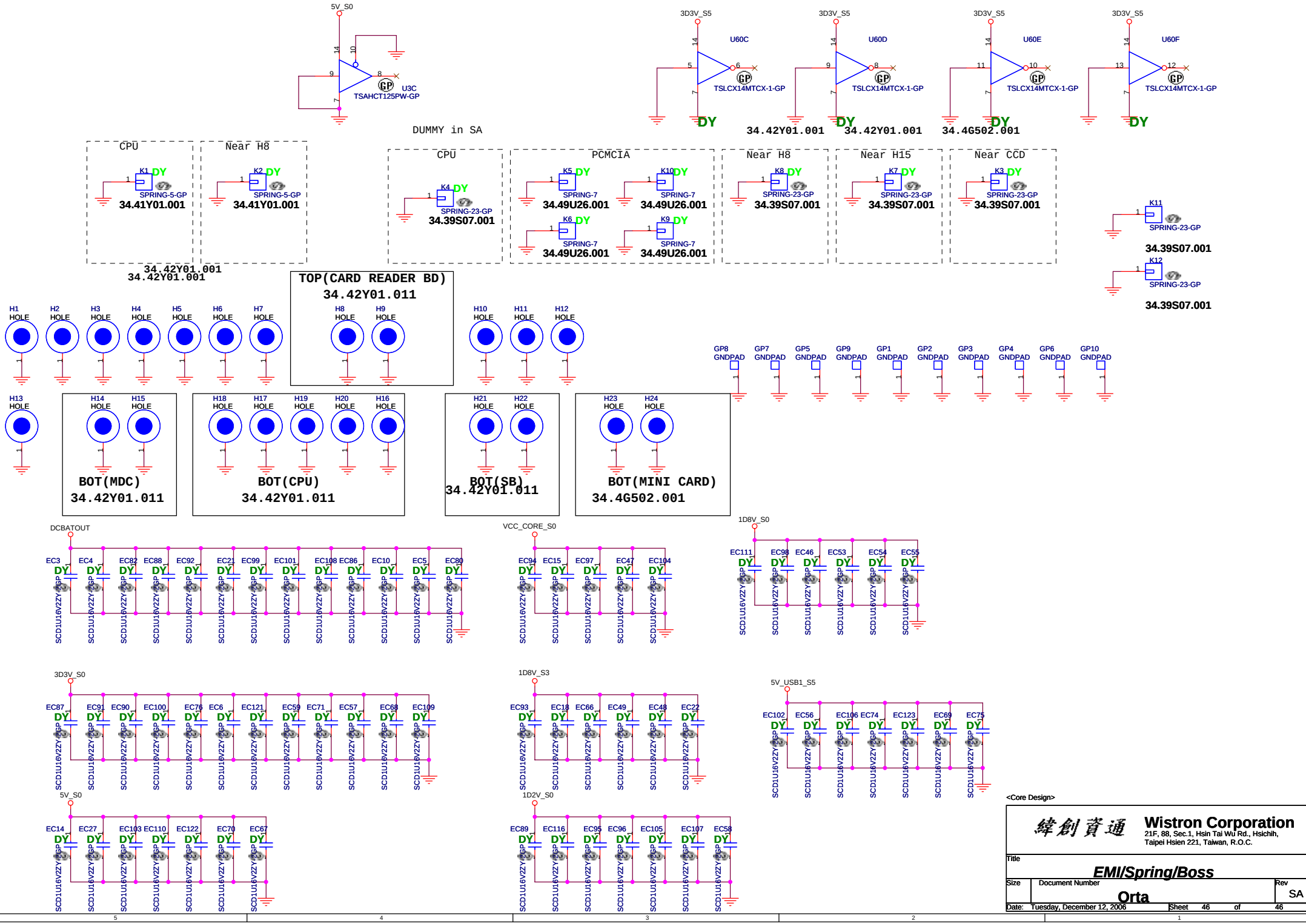
Run Power



Power On Logic

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWR CTL LOGIC / PWR PLANE***
Size: A3	Document Number: Orta
Rev: SA	
Date: Tuesday, December 12, 2006	Sheet 45 of 46


5V_S0
U3C
TSAHCT125PW-GP
DUMMY in SA
3D3V_S5
U60C
U60D
U60E
U60F
TSLCX14MTCX-1-GP
DY
34.42Y01.001
34.42Y01.001
34.4G502.001
CPU
Near H8
CPU
PCMCIA
Near H8
Near H15
Near CCD
K1 DY
K2 DY
K4 DY
K5 DY
K10 DY
K8 DY
K7 DY
K3 DY
K6 DY
K9 DY
K11
K12
SPRING-5-GP
SPRING-23-GP
SPRING-7
34.41Y01.001
34.41Y01.001
34.39S07.001
34.49U26.001
34.49U26.001
34.49U26.001
34.49U26.001
34.39S07.001
34.39S07.001
34.39S07.001
34.42Y01.001
34.42Y01.001
TOP(CARD READER BD)
34.42Y01.011
H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H8 HOLE
H9 HOLE
H10 HOLE
H11 HOLE
H12 HOLE
H13 HOLE
H14 HOLE
H15 HOLE
H18 HOLE
H17 HOLE
H19 HOLE
H20 HOLE
H16 HOLE
H21 HOLE
H22 HOLE
H23 HOLE
H24 HOLE
BOT(MDC)
34.42Y01.011
BOT(CPU)
34.42Y01.011
BOT(SB)
34.42Y01.011
BOT(MINI CARD)
34.4G502.001
GP8 GNDPAD
GP7 GNDPAD
GP5 GNDPAD
GP9 GNDPAD
GP1 GNDPAD
GP2 GNDPAD
GP3 GNDPAD
GP4 GNDPAD
GP6 GNDPAD
GP10 GNDPAD
DCBATOUT
VCC_CORE_S0
1D8V_S0
3D3V_S0
1D8V_S3
5V_USB1_S5
5V_S0
1D2V_S0
SCD1U16V2ZY-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
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Date: Tuesday, December 12, 2006
Sheet 46 of 46