ZY7 SYSTEM BLOCK DIAGRAM

AMD Smarter Choice

CPU CORE ISL6265A PAGE 29

NB CORE (RT8202) PAGE XX

DDR II SMDDR_VTERM 1.8VSUS(TPS51116REGR) PAGE 31

SYSTEM POWER ISL6237 PAGE 28

SYSTEM CHARGER (ISL6251A) PAGE 27

DDRII-SODIMM1 PAGE 7 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 7 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

CPU Fan

HT3 LINK

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

LVDS PAGE 18 — LVDS

SWITCH — CRT, HDMI

MXM Connector PAGE 17 — PCI-Express 16X

Internal selector Resistor PAGE 17 — LVDS, CRT, HDMI

NORTH BRIDGE
RX780 / RS780M
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

PCI-E

PCIE2 / 3 X2 — Mini PCI-E Card Wireless /TV PAGE 19

PCIE1 X1 — Express Card (NEW CARD) PAGE 19

PCIE4 X1 — LAN PCIE-LAN BCM5764M (10/100/GagaLAN) PAGE 21 — RJ45 PAGE 21

PCIE5 X1 — JMB385 4 IN 1 CARD READER PAGE 24

PCIE X4

DVI-D PAGE 26
CRT PAGE 26
AUDIO PAGE 26
LAN PAGE 26
USB PAGE 26
DOCKING

HDMI PAGE 18
CRT PAGE 18
M/B

SATA - HDD PAGE 20 — SATA0

SATA - HDD PAGE 20 — SATA1

ODD(SATA) PAGE 20 — SATA4

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13,14,15,16

USB2.0 — 1,11 / 3,4 / 8,9 / 5 / 6 / 2 / 10 / 7

USB2.0 Ports x4 PAGE 19
Bluetooth x1 PAGE 19
PC-cam x1 PAGE 18
Fingerprint x1 PAGE 19
USB Docking x1 PAGE 19

PCI BUS / 33MHz

O2 OZ601 PAGE 23 — PCMCIA CARD BUS PAGE 23

Azalia

Azalia AudioController RealTek ALC268 PAGE 22

MDC 1.5 PAGE 22

LPC

Keyboard PAGE 25

KBC (WPCE775) PAGE 25

Touch Pad PAGE 20

SPI ROM PAGE 25

Audio Amplifier

Int MIC

Speaker

SPIDF/Phone Jack

Line in

MIC Jack

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTF#	OZ601

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	Block Diagram	1A

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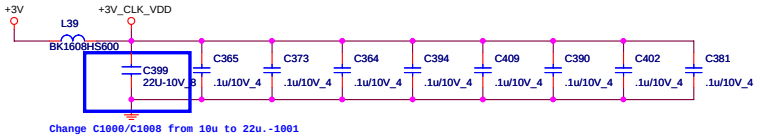
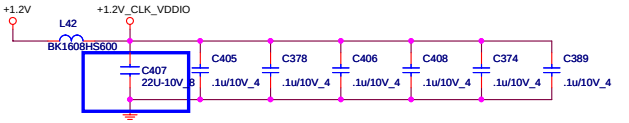
CLK_GEN_SLG8SP628





ICS9LPRS480 P/N :

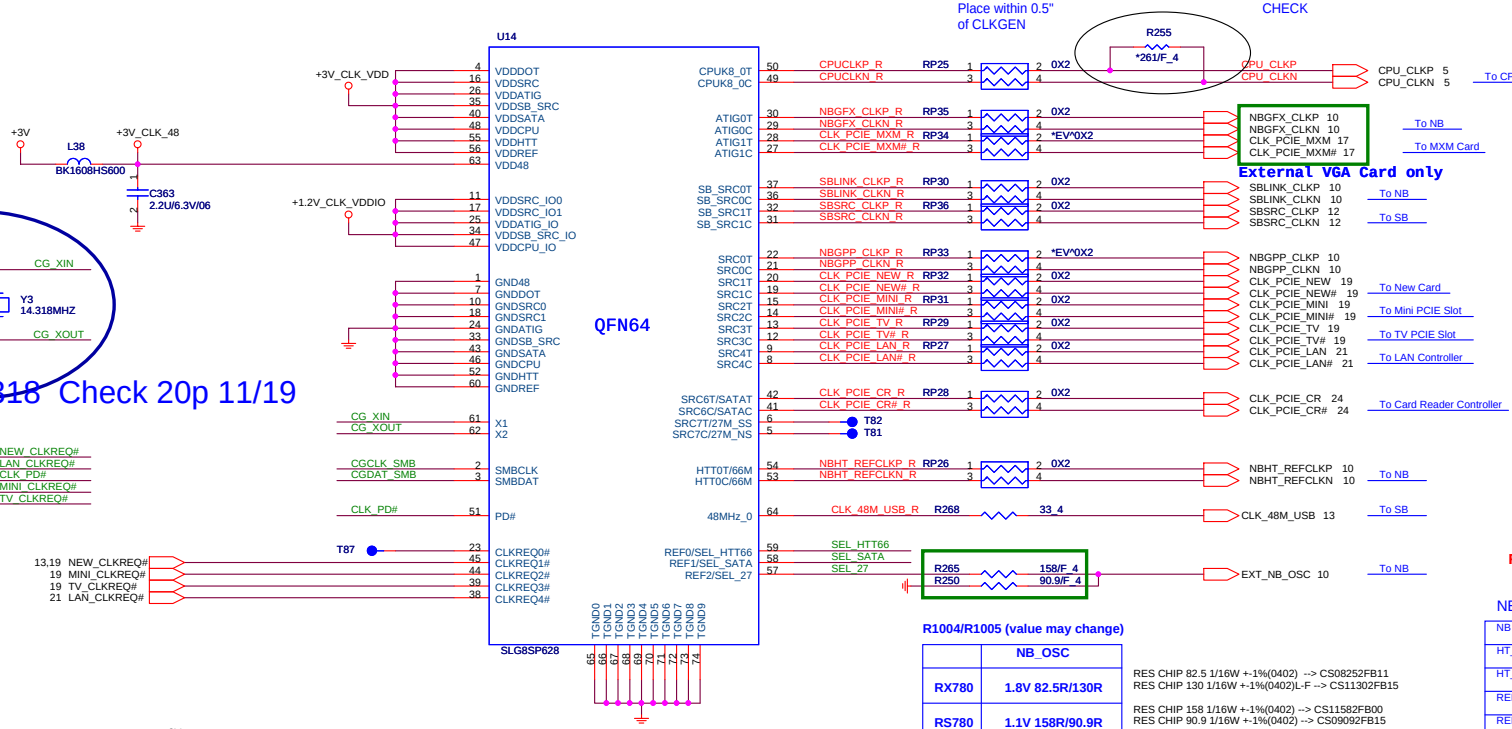
SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

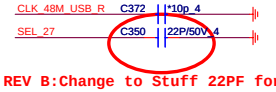
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

CHECK



Follow CLK ~~14.318~~ Check 20p 11/19



REV B:Change to Stuff 22PF for EMI request --0215

R1004/R1005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

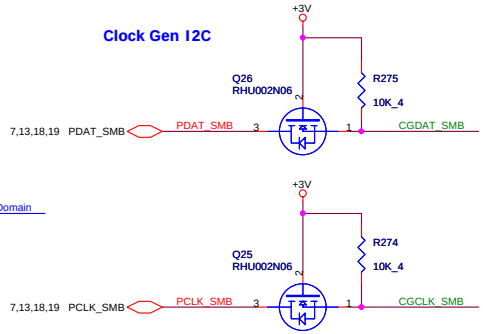
RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

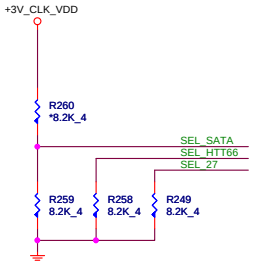
NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Clock Gen I2C



Check Chipset Power Domain



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

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	CLOCK GENERATOR_SLG8SP628	1A

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8 HT_RXD#[15..0] HT_RXD#[15..0]
8 HT_RXD[15..0] HT_RXD[15..0]
8 HT_TXD[15..0] HT_TXD[15..0]
8 HT_TXD#[15..0] HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN

U25A — HT LINK

D1	VLDT_A0		VLDT_B0	AE2	
D2	VLDT_A1		VLDT_B1	AE3	
D3	VLDT_A2		VLDT_B2	AE4	
D4	VLDT_A3		VLDT_B3	AE5	
HT_RXD0	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_TXD0	
HT_RXD#0	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_TXD#0	
HT_RXD1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_TXD1	
HT_RXD#1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_TXD#1	
HT_RXD2	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_TXD2	
HT_RXD#2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_TXD#2	
HT_RXD3	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_TXD3	
HT_RXD#3	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_TXD#3	
HT_RXD4	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_TXD4	
HT_RXD#4	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_TXD#4	
HT_RXD5	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_TXD5	
HT_RXD#5	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_TXD#5	
HT_RXD6	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_TXD6	
HT_RXD#6	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_TXD#6	
HT_RXD7	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_TXD7	
HT_RXD#7	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_TXD#7	
HT_RXD8	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_TXD8	
HT_RXD#8	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_TXD#8	
HT_RXD9	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_TXD9	
HT_RXD#9	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_TXD#9	
HT_RXD10	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_TXD10	
HT_RXD#10	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_TXD#10	
HT_RXD11	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_TXD11	
HT_RXD#11	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_TXD#11	
HT_RXD12	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_TXD12	
HT_RXD#12	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_TXD#12	
HT_RXD13	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_TXD13	
HT_RXD#13	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_TXD#13	
HT_RXD14	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_TXD14	
HT_RXD#14	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_TXD#14	
HT_RXD15	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_TXD15	
HT_RXD#15	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_TXD#15	
8 HT_CPU_UPCLK0	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_DWNCLK0 8	
8 HT_CPU_UPCLK#0	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_DWNCLK#0 8	
8 HT_CPU_UPCLK1	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_DWNCLK1 8	
8 HT_CPU_UPCLK#1	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_DWNCLK#1 8	
8 HT_CPU_UPCTL0	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_DWNCTL0 8	
8 HT_CPU_UPCTL#0	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_DWNCTL#0 8	
8 HT_CPU_UPCTL1	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_DWNCTL1 8	
8 HT_CPU_UPCTL#1	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_DWNCTL#1 8	

C519 4.7u/6.3V_6

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

NO STUB for HT3

R135 *51_4 R133 *51_4

VLDT_RUN

HOLE27 *MINI_HOLE HOLE28 MINI_HOLE HOLE36 MINI_HOLE HOLE37 MINI_HOLE

HOLE9 CPU_HOLE HOLE10 CPU_HOLE HOLE19 CPU_HOLE HOLE20 CPU_HOLE

HOLE8 MXM_HOLE HOLE17 MXM_HOLE HOLE16 MXM_HOLE HOLE7 MXM_HOLE

HOLE6 *EV^MXM1_HOLE HOLE21 *EV^MXM1_HOLE HOLE11 MDC_HOLE HOLE13 MDC_HOLE

HOLE14 *H-C295D118P2 HOLE5 *H-C295D118P2 HOLE2 *H-C295D118P2 HOLE23 *H-C295D118P2

HOLE4 *H-C295D118P2 HOLE35 *H-C295D118P2 HOLE25 *H-C295D118P2 HOLE24 *H-C295D118P2

ADOGND

HOLE32 *H-C295D118P2 HOLE34 *H-C295D118P2 HOLE33 *H-C295D118P2 HOLE1 *H-C295D118P2

HOLE39 *FAN_HOLE HOLE38 FAN_HOLE HOLE15 *NONP_HOLE1 HOLE3 *H-C295D118P2

REV B: Add Hole39 for ME request---0215

HOLE26 ODD1_HOLE HOLE30 ODD1_HOLE HOLE31 HDD1_HOLE HOLE29 HDD1_HOLE HOLE22 HDD2_HOLE HOLE18 HDD2_HOLE

PAD2 EMIPAD PAD3 EMIPAD PAD1 *EMIPAD

SPAD1 *SPAD

+1.2V VLDT_RUN

L50 FBJ3216HS800_1206

L54 FBJ3216HS800_1206

80 ohm(4A)

C555 4.7u/6.3V_6 C560 4.7u/6.3V_6 C569 .22U_4 C527 .22U_4 C522 180P_4 C565 180P_4

Note:on MCP77,(HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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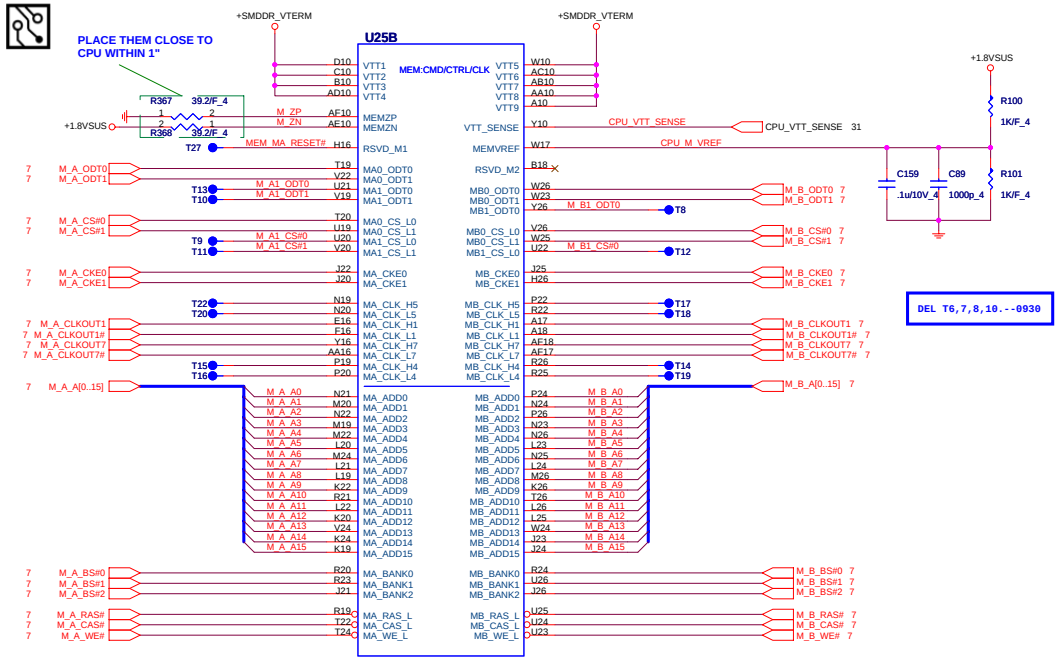
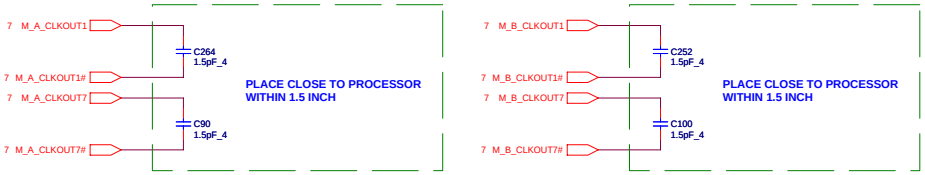
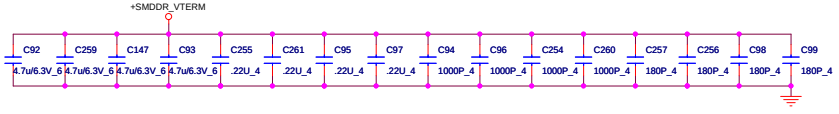
	AMD Griffin HT I/F	1A
Date: Thursday, June 26, 2008	Sheet 3 of 35	

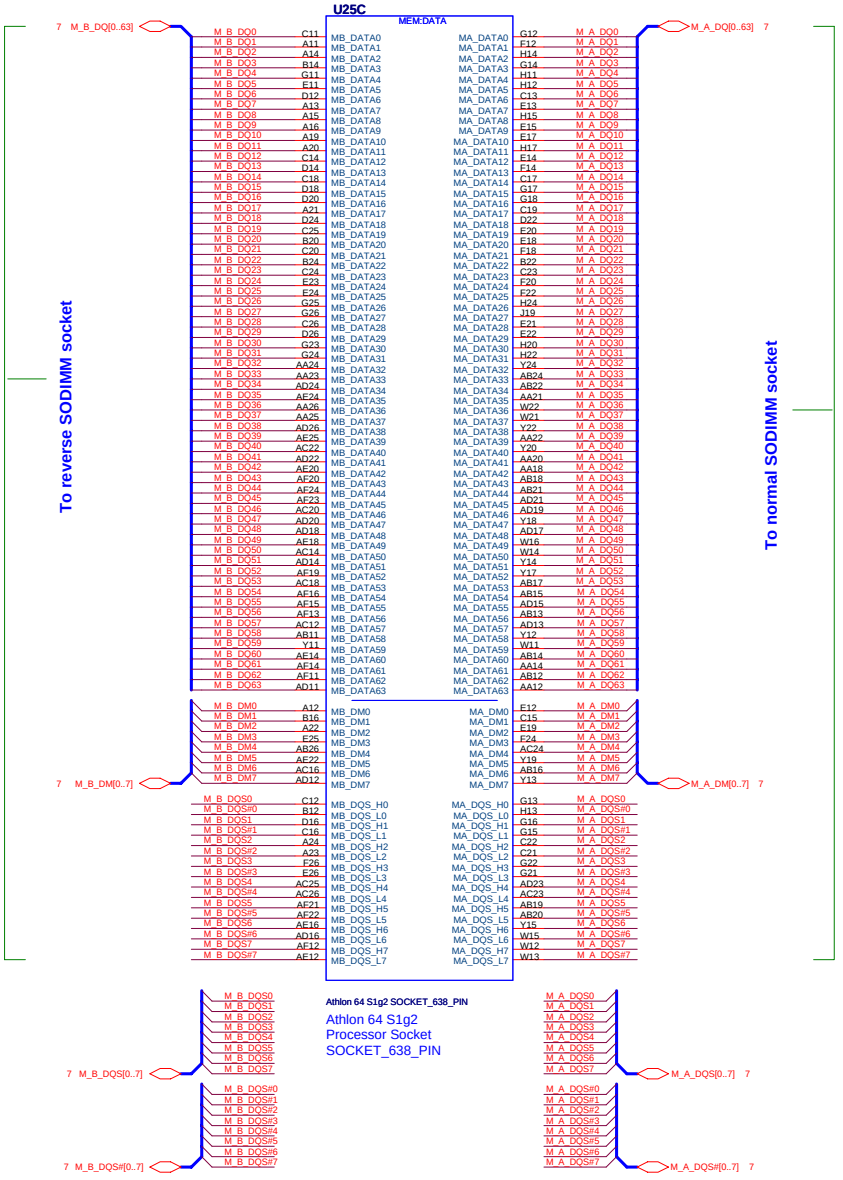
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

Processor DDR2 Memory Interface









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PROJECT : ZY7			
Size	Document Number		Rev
	AMD Griffin DDRII MEMORY I/F		1A
Date: Thursday, June 26, 2008	Sheet 4 of 35		

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V — L57 BLM18PG330SN1D_6 — CPU_VDDA_RUN

C602 100U-6.3V_3528 | C593 4.7u/6.3V_B | C235 .22U_4 | C246 3300p/50V_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

+1.8VSUS — R363 390_4 CPU_SID; R366 390_4 CPU_SIC; R374 *390_4; R373 1K/F_4 CPU_ALERT

390 Ohm

Need Check .-1001

+1.8VSUS — Q15 2N7002 — R93 *0_4 — 16,29,32 CPU_COREPG

R97 1K_4 | R96 100K_4 | R92 300_4 | 11/19

Q16 MMBT3904 — R87 0_4 CPU_THERMTRIP_L# — R91 33_4 — SYS_SHDN# 28,32

13 CPU_THERMTRIP#

CPU_CLKP C262 3900P_4 — CPU_CLKN C263 3900P_4 — R175 169/F_6

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
place them to CPU within 1.5"

2 CPU_CLKP
2 CPU_CLKN

VLDT_RUN — R132 44.2/F_4 CPU_HTREF0 — R129 44.2/F_4 CPU_HTREF1

connect to CPU CORE power FB

Add Pull H/L RES.--0610

Add Pull H/L RES.--0610

route as differential as short as possible testpoint under package

U25D

CPU_VDDA_RUN — F8 VDDA1, F9 VDDA2

CPU_CLKIN_SC_P — A9 CLKIN_H
CPU_CLKIN_SC_N — A8 CLKIN_L

LDT_RST# — B7 RESET_L
PWRGD_C — A7 PWROK
LDT_STOP# — F10 LDTSTOP_L
CPU_LDT_REQ#_CPU — C6 LDTREQ_L

CPU_SIC — AF4 SIC
CPU_SID — AE5 SID
CPU_ALERT — AE6 ALERT_L

CPU_HTREF0 — R6 HT_REF0
CPU_HTREF1 — P6 HT_REF1

29 CPU_VDD0_FB_H — F6 VDD0_FB_H
29 CPU_VDD0_FB_L — E6 VDD0_FB_L

29 CPU_VDD1_FB_H — Y6 VDD1_FB_H
29 CPU_VDD1_FB_L — AB6 VDD1_FB_L

CPU_DBRDY — G10 DBRDY
CPU_TMS — AA9 TMS
CPU_TCK — AC9 TCK
CPU_TRST# — AD9 TRST_L
CPU_TDI — AF9 TDI

T91 CPU_TEST23_TSTUPD — AD7 TEST23

T32 CPU_TEST18_PLLTEST1 — H10 TEST18
T29 CPU_TEST19_PLLTEST0 — G9 TEST19

T34 CPU_TEST25_H_BYPASSCLK_H — E9 TEST25_H
T31 CPU_TEST25_L_BYPASSCLK_L — E8 TEST25_L

T94 CPU_TEST21_SCANEN — AB8 TEST21
T90 CPU_TEST20_SCANCLK2 — AE7 TEST20
T168 CPU_TEST24_SCANCLK1 — AE7 TEST24
T93 CPU_TEST22_SCANSHIFTEN — AE8 TEST22
T1 CPU_TEST12_SCANSHIFTENB — AC8 TEST12
T92 CPU_TEST27_SINGLECHAIN — AF8 TEST27

R165 0_4 CPU_TEST9_ANALOGIN — C2 TEST9
AA6 TEST6

A3 RSVD1, A5 RSVD2, B3 RSVD3, B5 RSVD4, C1 RSVD5

KEY1 M11, KEY2 W10

A6 SVC — CPU_SVC_R
A4 SVD — CPU_SVD_R

AF6 THERMTRIP_L — CPU_THERMTRIP_L#
AC7 PROCHOT_L — CPU_PROCHOT#
AA8 MEMHOT_L — CPU_MEMHOT#

W7 THERMDC — CPU_THERMDC
W8 THERMDA — CPU_THERMDA

W9 VDDIO_FB_H — CPU_VDDIO_FB_H 31
Y9 VDDIO_FB_L — CPU_VDDIO_FB_L 31

H6 VDDNB_FB_H — VDD_NB_FB_H 29
G6 VDDNB_FB_L — VDD_NB_FB_L 29

E10 DBREQ_L — CPU_DBREQ#
AF9 TDO — CPU_TDO

J7 TEST28_H — CPU_TEST28_H_PLLCHRZ_P — T25
H8 TEST28_L — CPU_TEST28_L_PLLCHRZ_N — T26

D7 TEST17 — CPU_TEST17_BP3 — T35
E7 TEST16 — CPU_TEST16_BP2 — T33
E7 TEST15 — CPU_TEST15_BP1 — T106
C7 TEST14 — CPU_TEST14_BP0 — T105

C3 TEST7, K8 TEST10, C4 TEST8

C9 TEST29_H — CPU_TEST29_H_FBCLKOUT_P — T36
C8 TEST29_L — CPU_TEST29_L_FBCLKOUT_N — T104

H18 RSVD10, H19 RSVD9, AA7 RSVD8, D5 RSVD7, C5 RSVD6

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

+1.8VSUS — R435 300_4 — 12 CPU_PWRGD — R439 0_4 — PWRGD_C — C652 .1u/10V_4

+1.8VSUS — R447 300_4 — 10,12 CPU_LDT_STOP# — R446 0_4 — LDT_STOP#

+1.8VSUS — R436 300_4 — 10,12 CPU_LDT_RST# — R437 0_4 — LDT_RST#

Add pull up

+1.8VSUS — R448 300_4 — CPU_LDT_REQ#_CPU — R449 0_4 — CPU_LDT_REQ# — CPU_LDT_REQ# 10

+1.8VSUS — R89 300_4 — R90 330_4 — Q14 MMBT3904 — CPU_PROCHOT# — R88 *0_4 — EC_PROCHOT# 25 — SB_PROCHOT# 12

+1.8VSUS — R122 *300_4 — R99 *330_4 — Q17 *MMBT3904 — CPU_MEMHOT# — CPUMEMHOT# 25

connect to CPU CORE power controlier

VID Override Circuit

+1.8VSUS — R434 1K_4 — R433 1K_4

CPU_SVC_R — R432 0_4 — SVC 29 — Serial VID Clock
CPU_SVD_R — R431 0_4 — SVD 29 — Serial VID Data
CPU_PWRGD — R438 0_4 — PGD_IN 29

R442 *220_4 | R441 *220_4

VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

+1.8VSUS

CPU_TEST27_SINGLECHAIN — R369 300_4
CPU_TEST25_L_BYPASSCLK_L — R559 300_4

CPU_TEST18_PLLTEST1 — R141 300_4
CPU_TEST19_PLLTEST0 — R140 300_4
CPU_TEST15_BP1 — R450 300_4
CPU_TEST14_BP0 — R451 300_4

CPU_TEST21_SCANEN — R383 300_4
CPU_TEST20_SCANCLK2 — R371 300_4
CPU_TEST24_SCANCLK1 — R372 300_4
CPU_TEST22_SCANSHIFTEN — R370 300_4
CPU_TEST12_SCANSHIFTENB — R379 300_4
CPU_TEST25_H_BYPASSCLK_H — R560 300_4
CPU_TEST23_TSTUPD — R561 300_4

HDT CONNECTOR

+1.8VSUS — R532 300_4 — CPU_DBREQ#

CN22 *ASP-68200-07-25P-LDV

CPU_DBRDY, CPU_TCK, CPU_TMS, CPU_TDI, CPU_TRST#, CPU_TDO

GND1, RSVD1, RSVD0, DBREQ_L, DBRDY, TCK, TMS, TDI, TRST_L, TDO, VCC_PROC_IO_21, VCC_PROC_IO_23, RESET_L, KEY
GND2, GND4, GND6, GND8, GND10, GND12, GND14, GND16, GND18, GND20, GND22, GND26

H_LDT_RST#

CPU H/W MONITOR

2/20/08' Reserve 0 ohm for CPU thermal issue on C-test

15 MIL

+3V — R112 47/F_6 — 3V_THM — C105 .1u/10V_4 — R615 *0_4 — CPU_THERMDC — C102 2200P_4 — CPU_THERMDA

10 mil trace / 10 mil space

Address 98H

U6 G781: VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND

KBSMDAT, KBSMCLK

R105 10K_4 — Q37 2N7002E — To SB GPIO — THERM_ALERT# 13

R107 4.7K_4 — Q41 2N7002E — 2ND_MBDATA 25

R108 4.7K_4 — Q40 2N7002E — 2ND_MBCLK 25

R104 10K_4 — To FAN — CPUFAN#_ON 20

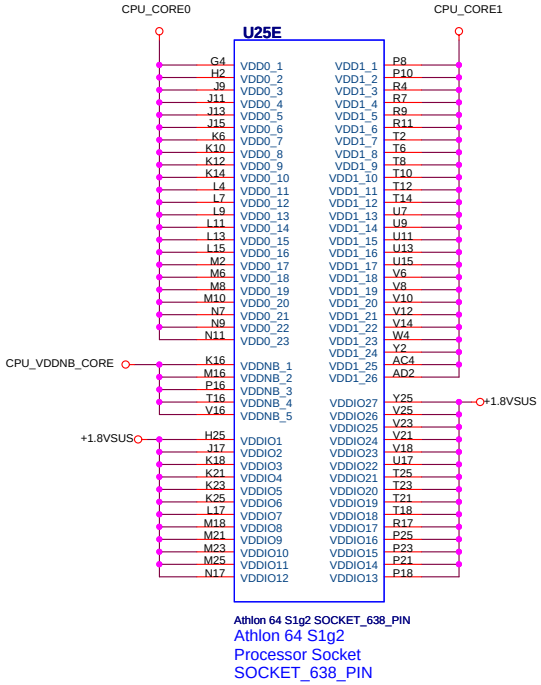
+1.8VSUS — R462 10K_4 — R456 1K/F_4 — H_LDT_RST# — LDT_RST# — Q51 MMBT3904

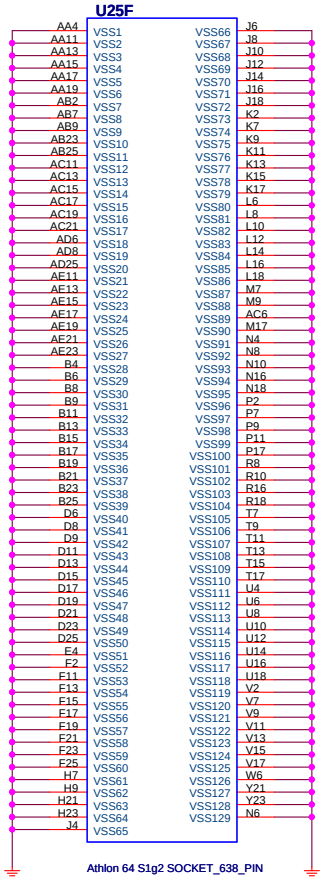
Quanta Computer Inc.
PROJECT : ZY7

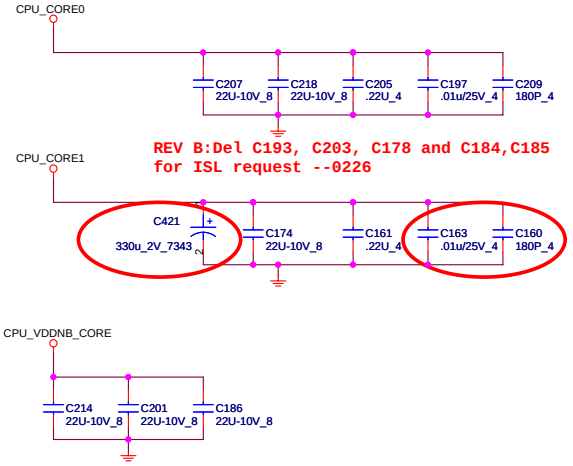
Size	Document Number	Rev
	AMD Griffin CTRL & DEBUG	1A

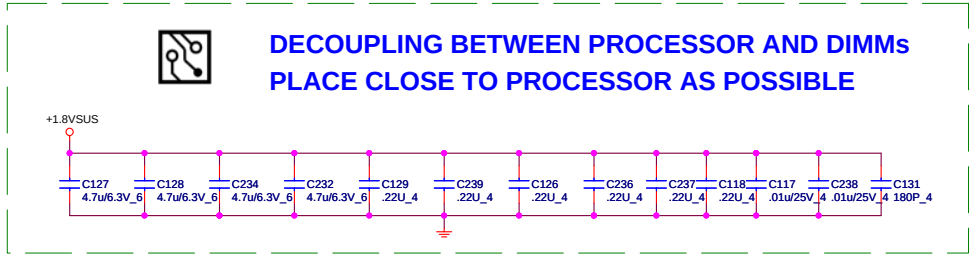
Date: Thursday, June 26, 2008 Sheet 5 of 35

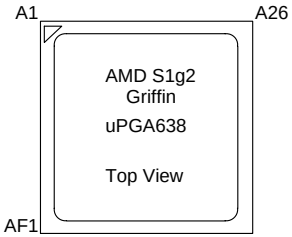
PROCESSOR POWER AND GROUND



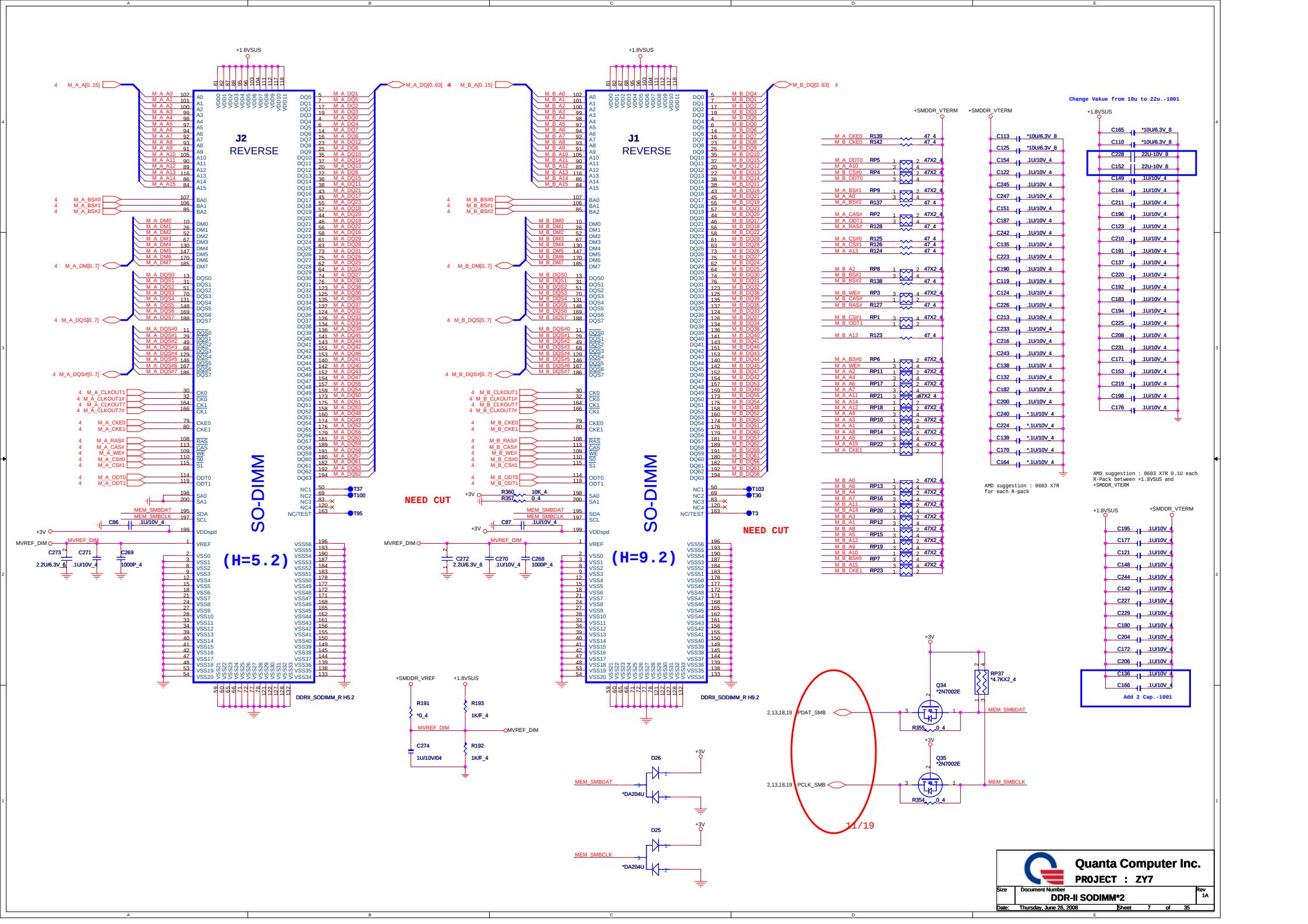








Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: AMD Griffin PWR & GND	Rev 1A
Date: Thursday, June 26, 2008	Sheet 6 of 35	


J2
REVERSE
SO-DIMM
(H=5.2)
DDRII_SODIMM_R H5.2
J1
REVERSE
SO-DIMM
(H=9.2)
DDRII_SODIMM_R H9.2
NEED CUT
NEED CUT
+1.8VSUS
+SMDDR_VTERM
+SMDDR_VREF
+3V
MVREF_DIM
Change Vakue from 10u to 22u.-1001
AMD suggestion : 0603 X7R 0.1U each R-Pack between +1.8VSUS and +SMDDR_VTERM
AMD suggestion : 0603 X7R for each R-pack
Add 2 Cap.-1001
Q34 *2N7002E
Q35 *2N7002E
RP37 *4.7KX2_4
D26 *DA204U
D25 *DA204U
2,13,18,19 PDAT_SMB
2,13,18,19 PCLK_SMB
MEM_SMBDAT
MEM_SMBCLK
11/19
Quanta Computer Inc.
PROJECT : ZY7
DDR-II SODIMM*2
Rev 1A
Date: Thursday, June 26, 2008
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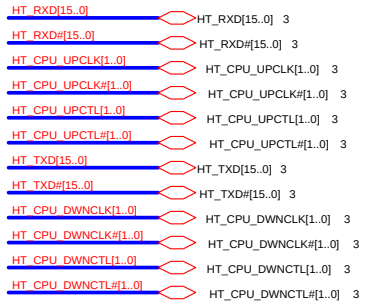
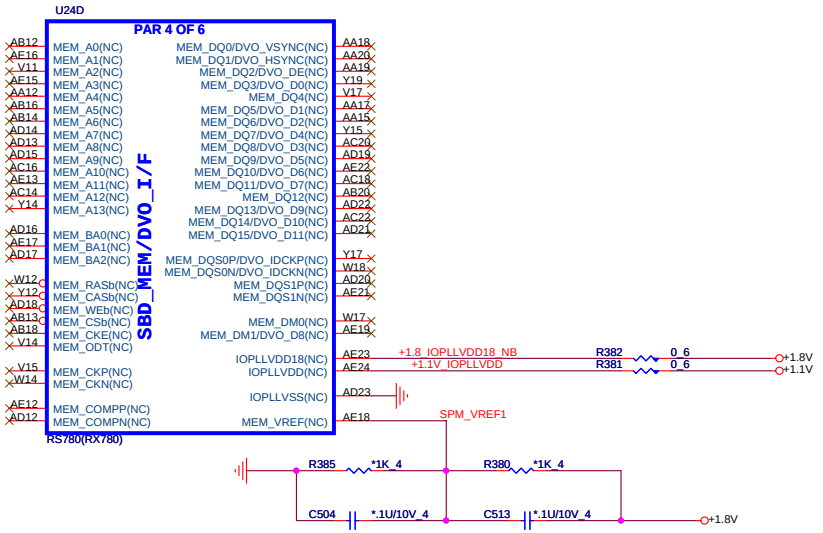


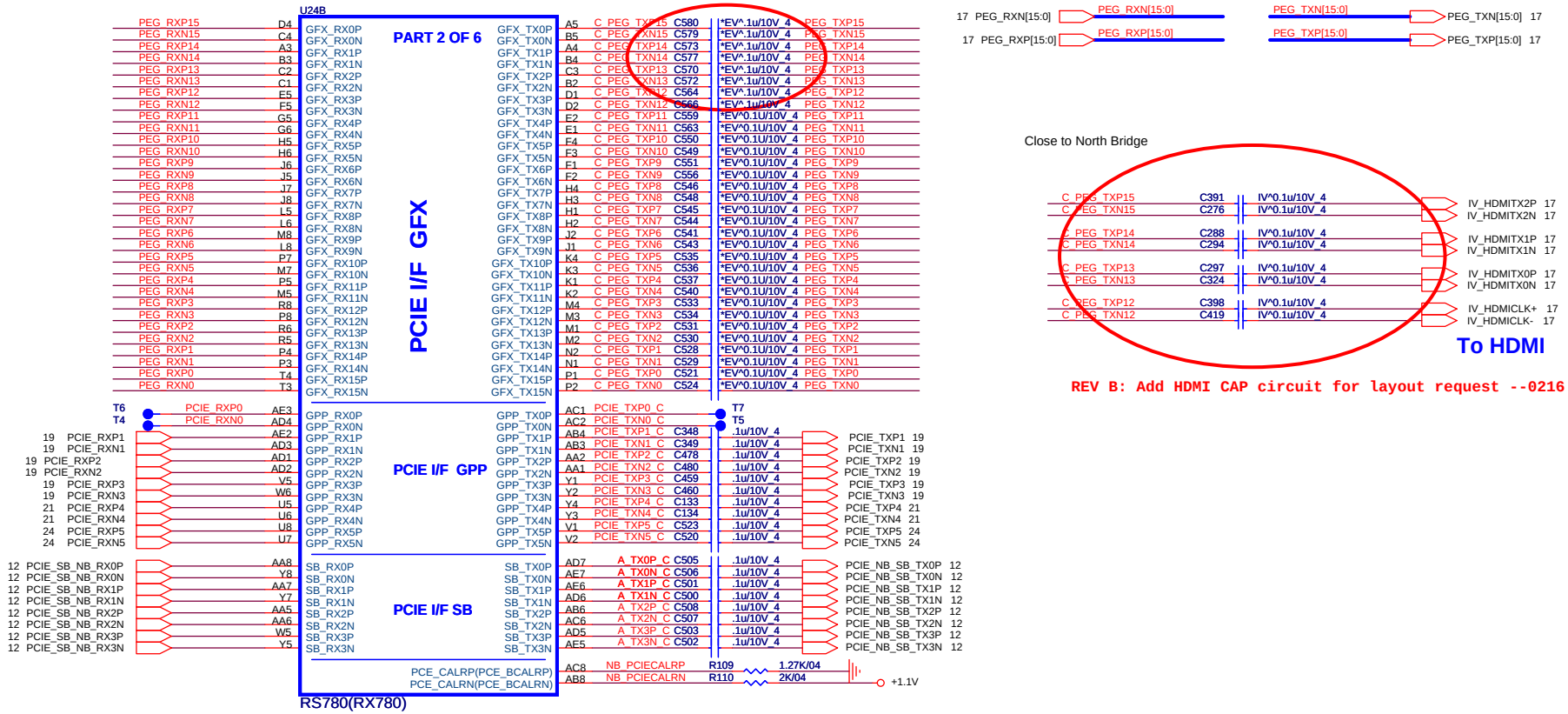
signals	RS780	RX780
HT_TXCALP	R641 301ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R661 301 ohm 1%	R661 1.21k ohm 1%
HT_RXCALN		

This block is for UMA RS780 only , RX780 can remove all component



Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/4	1A
Date: Thursday, June 26, 2008	Sheet 8 of 35	



Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: RX780/RS780-PCIE I/F 2/4 — Rev: 1A
Date: Thursday, June 26, 2008	Sheet 9 of 35

Need Check RGB Pull Low RES value!--1026

REV E: Change R393 value from 150ohm to 133ohm following AMD change---0214

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
5,12 CPU_LDT_RST# R146 *0_4 NB_RST#_IN
RS780
12 NB_PLTRST# R155 0_4
North Bridge RESET

U24C
PART 3 OF 6
RS780(RX780)

CRT/TVOUT
AVDD1(NC) F12
AVDD2(NC) E12
AVDDDI(NC) F14
AVSSDI(NC) G15
AVDDQ(NC) H15
AVSSQ(NC) H14
C_Pr(DFT_GPIO5) F17
Y(DFT_GPIO2) F17
COMP_Pb(DFT_GPIO4) F15
RED(DFT_GPIO0) G18
REDb(NC) G17
GREEN(DFT_GPIO1) E18
GREENb(NC) E18
BLUE(DFT_GPIO3) F18
BLUEb(NC) E19
DAC_HSYNC(PWM_GPIO4) A11
DAC_VSYNC(PWM_GPIO6) B11
DAC_SDA(PCE_TCALRN) E8
DAC_SCL(PCE_RCALRN) F8
DAC_RSET(PWM_GPIO1) G14
TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19 LA_DATAP3 T24
TXOUT_L3N(DBG_GPIO2) B19 LA_DATAN3 T28
TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18 LB_DATAP3 T21
TXOUT_U3N(NC) D19 LB_DATAN3 T23
TXCLK_LP(DBG_GPIO1) B16
TXCLK_LN(DBG_GPIO3) A16
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17

PLL PWR / LVTM
PLLVDD(NC) A12
PLLVDD18(NC) D14
PLLVSS(NC) B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7
VDDLTP18(NC) A13
VSSLTP18(NC) B13
VDDLT18_1(NC) A15
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

PM
SYSRESETb D8
POWERGOOD A10
LDTSTOPb C10
ALLOW_LDTSTOP C12

CLOCKs
HT_REFCLKP C25
HT_REFCLKN C24
REFCLK_P/OSCIN(OSCIN) E11
REFCLK_N(PWM_GPIO3) F11
GFX_REFCLKP T2
GFX_REFCLKN T1
GPP_REFCLKP U1
GPP_REFCLKN U2
SBLINK_CLKP V4
SBLINK_CLKN V3
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) F7
LVDS_ENA_BL(PWM_GPIO2) G12

MIS.
I2C_DATA
I2C_CLK
DDC_DATA/AUX0N(NC)
DDC_CLK/AUX0P(NC)
AUX1P(NC)
AUX1N(NC)
STRP_DATA B10
RSVD G11
AUX_CAL(NC) C8
TMDS_HPD(NC) D9
HPD(NC) D10
TVCLKIN(PWM_GPIO5) D12
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13

+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
+1.8V_VDDLTP18_NB
+1.8V_VDDLT_18_NB
NB_RST#_IN
NB_PWRGD_IN
NB_LDT_STOP#
ALLOW_LDTSTOP
NBHT_REFCLKP
NBHT_REFCLKN
EXT_NB_OSC
NB_REFCLK_P
NB_REFCLK_N
NBGFX_CLKP
NBGFX_CLKN
NBGPP_CLKP
NBGPP_CLKN
SBLINK_CLKP
SBLINK_CLKN
NB_I2C_DATA
NB_I2C_CLK
HDTV_DET
RS740_DFT_GPIO0
RS740_DFT_GPIO1
+NB_CORE_ON
STRP_DATA
RS780_AUX_CAL
INT_HDMI_HPD_R
SUS_STAT#_NB
R_NB_THRMDA
R_NB_THRMDC
TEST_EN

R136 *150R_4 TV_C/R1
R130 *150R_4 TV_Y/G1
R134 *150R_4 TV_COMP1
17 INT_CRT_RED R148 IV^0_4 IV^133R_4 CRT_R_1
17 INT_CRT_GRN R149 IV^0_4 IV^150R_4 CRT_G_1
17 INT_CRT_BLU R150 IV^0_4 IV^150R_4 CRT_B_1
R151 IV^0_4
R152 IV^0_4
R153 IV^150R_4
17 INT_HSYNC R408 IV^0_4 HSYNC_INT
17 INT_VSYNC R407 IV^0_4 VSYNC_INT
17 INT_CRT_DDCDAT R162 IV^0_4 DDCDATA_INT
17 INT_CRT_DDCCLK R163 IV^0_4 DDCCLK_INT
R159 715R/06 DAC_RSET_NB
R418 4.7K/04 HDTV_DET
R171 4.7K/04
R172 4.7K/04
R167 0R/04 NB_REFCLK_P
R166 0_4 NB_REFCLK_N
2 NBGFX_CLKP
2 NBGFX_CLKN
2 NBGPP_CLKP
2 NBGPP_CLKN
2 SBLINK_CLKP
2 SBLINK_CLKN
17 INT_LVDS_EDIDDATA R414 IV^0_4 NB_I2C_DATA
17 INT_LVDS_EDIDCLK R415 IV^0_4 NB_I2C_CLK
17 INT_HDMI_DATA R410 IV^0_4 HDTV_DET
17 INT_HDMI_CLK R409 IV^0_4
T99 RS740_DFT_GPIO0
T101 RS740_DFT_GPIO1
30 +NB_CORE_ON R428 0_4 STRP_DATA
T102 RS780_AUX_CAL
R164 IV^0_4
R157 IV^0_4
R144 IV^0_4
INT_LVDS_DIGON 17
INT_LVDS_BL_BRGHT 18
INT_LVDS_BLON 17
SWAP BLON/BRGHT.--1108
RS780 only
R417 IV^0_4 INT_HDMI_HPD 17
T98
R168 0R/04 SUS_STAT# 13
T96
T97
R413 1.82K/04

RS780 only
VDDG_NB
R416 IV^4.7K/04 NB_I2C_DATA
R412 IV^4.7K/04 NB_I2C_CLK
Change PU from +3V to VDDG_NB.--1015

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
RX780
RS780_AUX_CAL R419 *3K/04

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
INT_VSYNC R424 3K_4 +3V

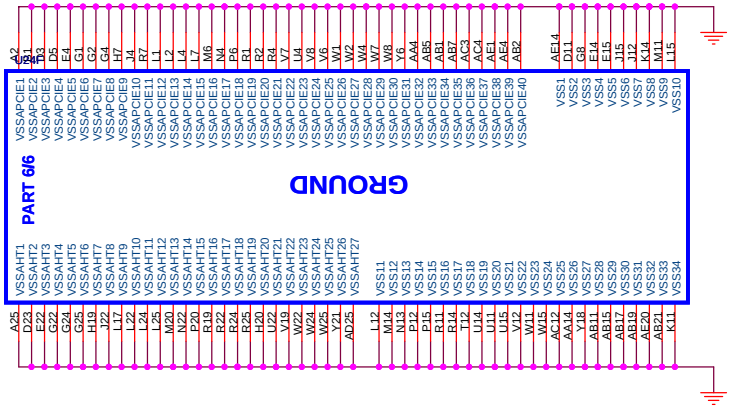
Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
INT_HSYNC R426 3K/04 +3V
R425 *3K_4

For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA R423 *10K_4 VDDG_NB
R427 2.2K_4

REV B: Change PU from +3V_S5 to +3V follow AMD CRB suggest.--0201
+3V L21 TI160808U300 +3V_AVDD_NB C241 10U/6.3V/06
AVDD-DAC Analog not applicable to RX780
+1.1V L56 BLM18PG221SN1D +1.1V_PLLVDD C575 2.2U/6.3V/06
PLLVDD - Graphics PLL not applicable to RX780
+1.8V L22 TI160808U300 +1.8V_PLLVDD18 C248 10U/6.3V/08 C217 10U/6.3V/06
PLLVDD18 - Graphics PLL not applicable to RX780
+1.8V R158 TI160808U300 +1.8V_AVDDDI_NB C221 10U/6.3V/06
AVDDI-DAC Digital not applicable to RX780
L20 TI160808U300 +1.8V_AVDDQ_NB C215 10U/6.3V/06
AVDDQ-DAC Bandgap Reference not applicable to RX780
+1.8V BLM18PG221SN1D L55 +1.8V_VDDLTP18_NB C574 2.2U/6.3V/06 C601 100p/50V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
BLM21PG221SN1D L53 +1.8V_VDDLT_18_NB C646 100p/50V_6 C576 4.7u/6.3V_6 C571 .1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
REV B: Add C601,C646,C647,C648 100PF for EMI request.--0201

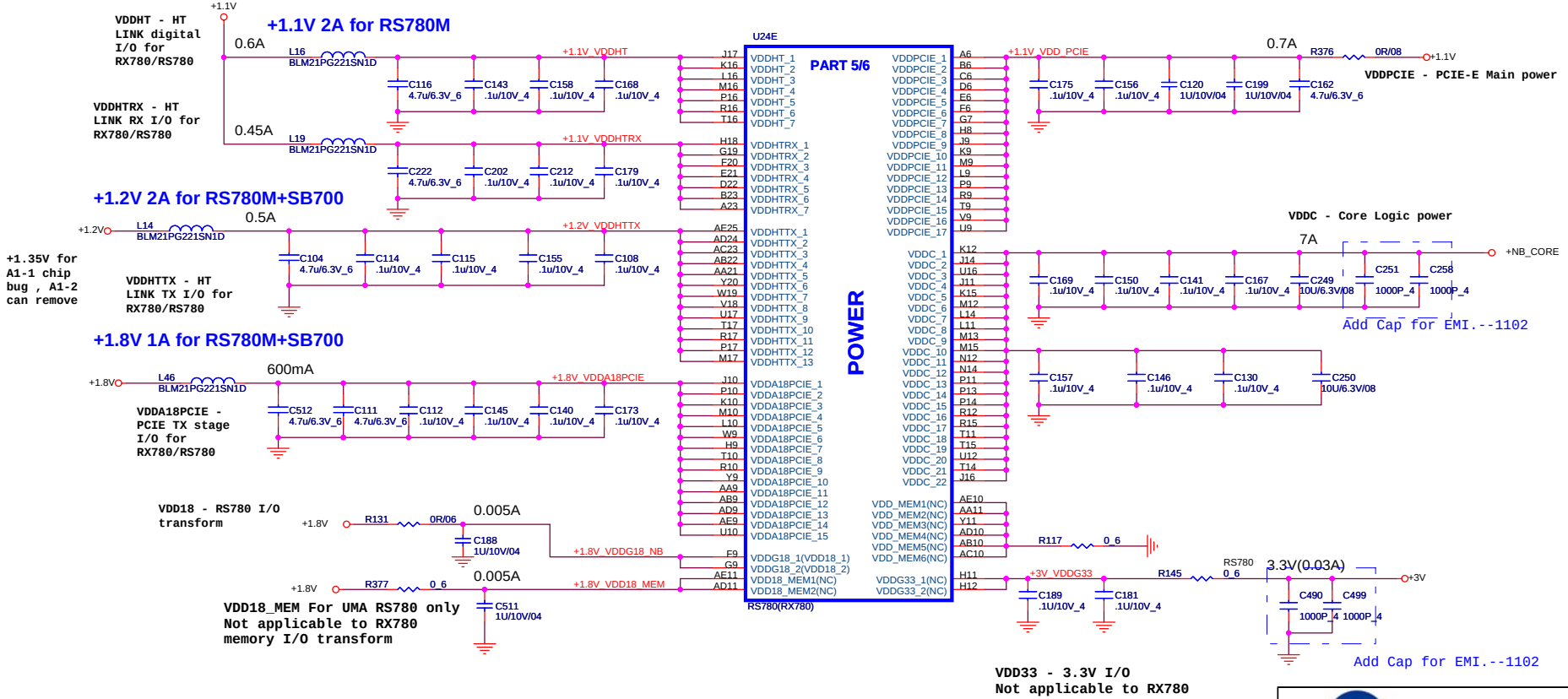
+1.8V TI160808U300 L18 20mils width +1.8V_VDDA18PCIEPLL C230 4.7U/6.3V/06
VDDA18PCIEPLL -PCIE PLL
L17 20mils width +1.8V_VDDA18HTPLL TI160808U300 C647 100p/50V_6 C107 4.7U/6.3V/06
VDDA18HTPLL -HT LINK PLL
+1.8V VDDG_NB R452 *4.7K_4
5,12 CPU_LDT_STOP# Q30 *BSS138_NL/SOT23 NB_LDT_STOP#
R459 0_4
C:REV Change it follow AMD suggest.
5 CPU_LDT_REQ# R460 0_4 ALLOW_LDTSTOP
12 ALLOW_LDTSTOP
RX780 +1.8V R457 *0R/06 VDDG_NB
RS780 +3V R458 0_6 C648 100p/50V_6

Quanta Computer Inc.
PROJECT : ZY7
Size Document Number RX780/RS780-SYS I/F 3/4 Rev 1A
Date: Thursday, June 26, 2008 Sheet 10 of 35

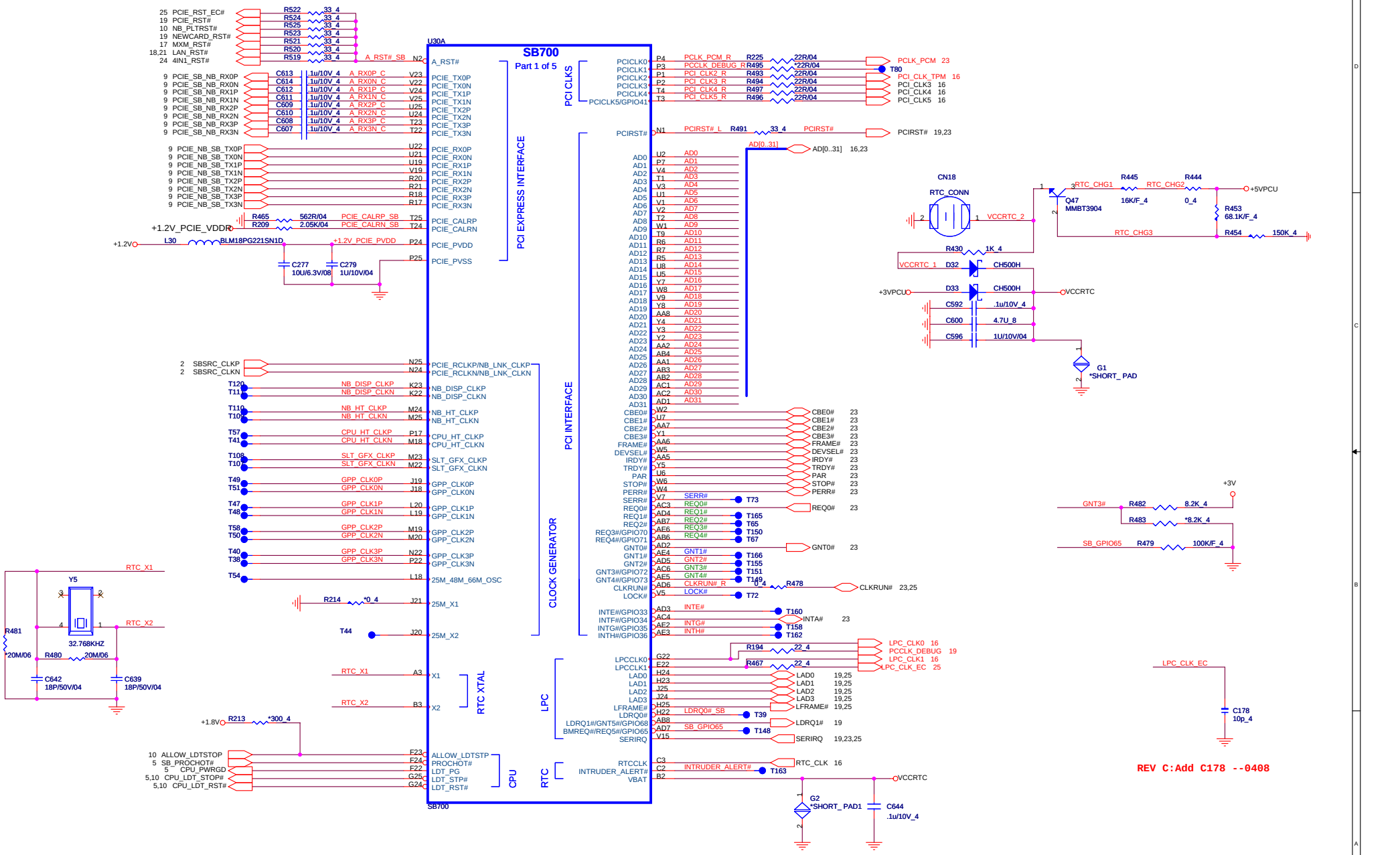


RX780/RS780 POWER DIFFERENCE TABLE

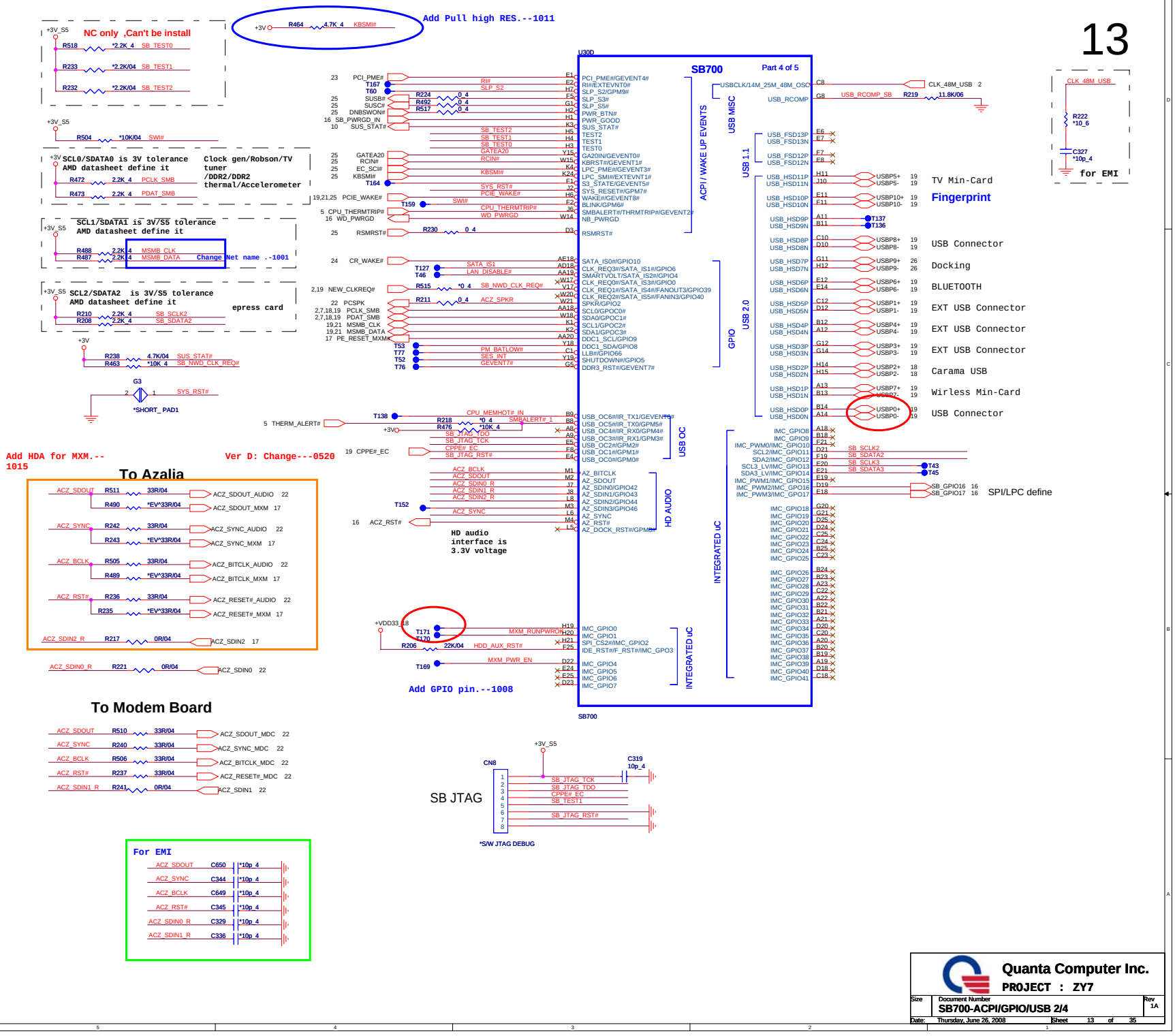
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: RX780/RS780-POWER 4/4 — Rev: 1A
Date: Thursday, June 26, 2008	Sheet 11 of 35



Quanta Computer Inc.			
PROJECT : ZY7			
Size	Document Number		Rev
	SB700-PCIE/PCI/CPU/LPC 1/4		1A
Date: Thursday, June 26, 2008	Sheet 12	of 35	



Quanta Computer Inc.			
PROJECT : ZY7			
Size	Document Number		Rev
	SB700-ACPI/GPIO/USB 2/4		1A
Date: Thursday, June 26, 2008		Sheet 13 of 35	

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

SATA1

SATA2

SATA ODD

U30B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

PLVDD_SATA--
SATA PLL
POWER

XTLVDD_SATA-- SATA
crystal power

5mA

Change from +3V to +3V_S5.--1212

AVDD--H/W monitor
Analog power

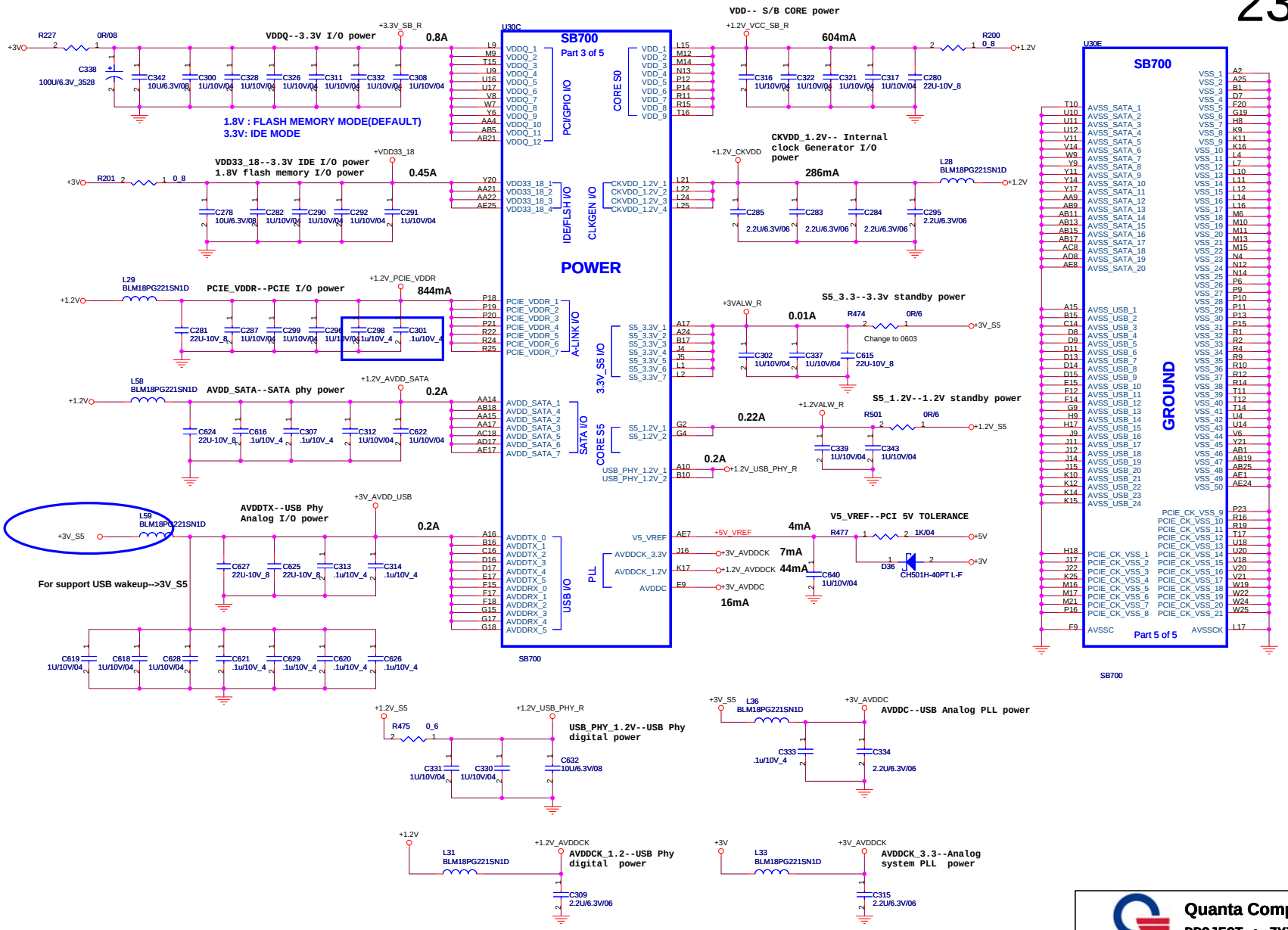
77mA

1mA

Place near
ball

Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: SB700-SATA/IDE/HWM/SPI 3/4	Rev 1A
Date: Thursday, June 26, 2008	Sheet 14 of 35	

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

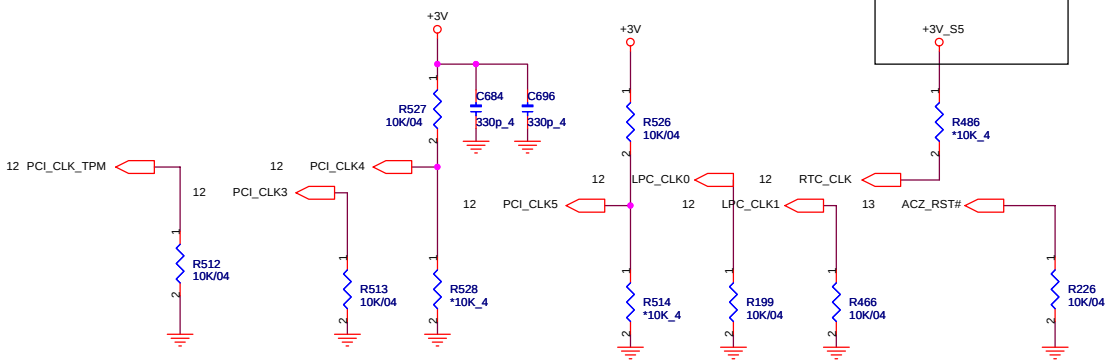


Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: SB700-PWR/DECOUPLING 4/4 | Rev 1A
Date: Thursday, June 26, 2008 | Sheet 15 of 35

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

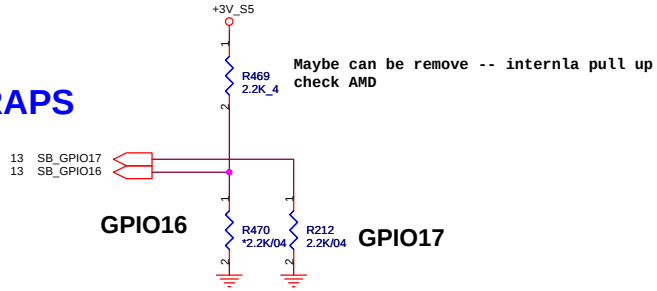
REV C:Add C684 and C696 --0408

It must ready refore RSMRST#



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

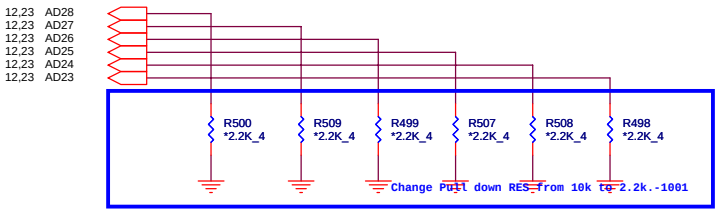
REQUIRED STRAPS



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

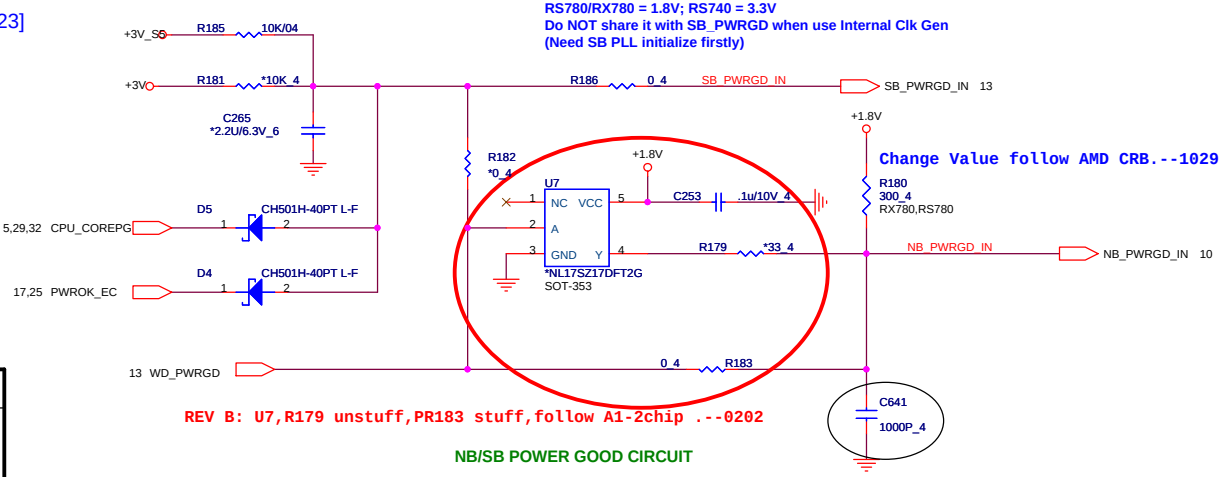
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



REV B: U7,R179 unstuff,PR183 stuff,follow A1-2chip .--0202

NB/SB POWER GOOD CIRCUIT

REV B: Add 1N Capacitor to Smoothing NB_PWRGD_IN ---0202

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	SB700-STRAPS,PWRGD	1A
Date: Thursday, June 26, 2008	Sheet 16 of 35	

REV B:Del MXM_POWEREN circuit
follow AMD request--0214

CN16B

CN16A

*EV^MXM_TYPEII

Q42 *EV^2N7002

Q43 *EV^2N7002

Q38 *EV^DTA114YUA

Q39 *EV^2N7002

D30 *BAS316

Quanta Computer Inc.
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Size	Document Number	Rev
	MXM	1A

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REV C: unstuff R3, Q1,Q4,Q5, Add and stuff D17, D21---0410

To IV/EV VGA Hot Plug Detect

Quanta Computer Inc.	
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To NEW-CARD & EXT. USB

650mA 2A 1.3A 275mA

CN9 NEW CARD_CON20X2

PDAT_SMB PCLK_SMB USBON# CPPE# NEWCARD_RST# 12 NEW_CLKREQ# 2,13 CLK_PCIE_NEW# 2 CLK_PCIE_NEW 2 PCIE_RXN1 9 PCIE_RXP1 9 PCIE_TXN1 9 PCIE_TXP1 9

USBP1- USBP1+ USBP3- USBP3+ USBP4- USBP4+

CL-2M2012-121JT L79 L80

Fingerprint

+3VSUS +3V R207 *0_6 R198 0_6 CN7 Finger_H1.95

USBP10- USBP10+ RN7 0_4P2R BUSBP10- BUSBP10+ L23 *DLW21HN900SQ2L

REV C:Add R198 and R207 --0408

Bluetooth

+3VSUS Q29 AO3403 BT_POWER 20mil C464 4.7u/6.3V_6 CN11 USB_BT_5P

BT_POWERON# BT_LED

USBP6+ USBP6- RN15 0_4P2R BUSBP6+ BUSBP6- L45 *DLW21HN900SQ2L

INT. USB

REV B:Modify it for ESD issue on 2/20

USBP8+ USBP8- RN14 *0_4P2R BUSBP8+ BUSBP8- L32 CL-2M2012-121JT D37 D38 R0IV18_ESD SYUIN_USB CN21 C617 470p_4 USBPWRP1

Add CAP--1107

+5VPCU C293 10u/10V_8 C286 1u/10V_4 U8 RT9711BPF IN1 IN2 EN# GND GND-C OUT3 OUT2 OUT1 OC# 60mil USBPWR1 R196 *6.34K/F_4 USBON#

USBP0+ USBP0- RN13 *0_4P2R BUSBP0+ BUSBP0- L26 CL-2M2012-121JT D34 D35 R0IV18_ESD SYUIN_USB CN19 60mil USBPWRP1 L27 TI201209G121_8_3A C590 470p_4 C584 100u/6.3V_3528

REV B:Modify it for EMI.--0218

13 CPPE#_EC R266 0_4 CPPE#

MODULE 'A' TV card

MODULE 'B' Wireless card

Double Stack MINI CARD

MINI-CARD

CAPACITOR on Module

REV B:Modify footprint--- 2/22

MODULE 'A' MODULE 'B' CN33

+3V_MINI R539 0_8 +3V_MINI_A +3V_MINI_B R540 0_8 +3V_MINI

RF_LED# R538 *0_4 RF_LED# A RF_LED# B R327 0_4 RF_LED# 20

USBP5+ R344 *0_4 USBP5+ C USBP5- R340 *0_4 USBP5- C USBP7+ C R541 0_4 USBP7- C R542 0_4 USBP7+ 13 USBP7- 13

MINI_SMDATA MINI_SMCLK

PCIE_TXP2 PCIE_TXN2 PCIE_RXP2 PCIE_RXN2 PCIE_RST# CLK_PCIE_TV CLK_PCIE_TV# TV_CLKREQ# PCIE_WAKE_WL_R_# R537 *0_4 WAKE_WL_A# R534 0_4

PCIE_TXP3 PCIE_TXN3 PCIE_RXP3 PCIE_RXN3 PCIE_RST# CLK_PCIE_MINI CLK_PCIE_MINI# MINI_CLKREQ# WAKE_WL_B#

+1.5V

LFRAME# R569 A_LFRAME#_R LAD3 R612 A_LAD3_R LAD2 R570 A_LAD2_R LAD1 R611 A_LAD1_R LAD0 R440 A_LAD0_R

LFRAME#_R R318 LAD3_R R313 LAD2_R R319 LAD1_R R314 LAD0_R R320 *0_4

LFRAME# 12,25 LAD3 12,25 LAD2 12,25 LAD1 12,25 LAD0 12,25

Debug

12,23,25 SERIRQ 12 LDRQ1# 12,23 PCIRST# 12 PCCLK_DEBUG

SERIRQ_R LDRQ1#_R PCIE_RST#_R LPC_CLK_DEBUG1_R

+3V_MINI R564 0_6 +3V_MINI_R

Modify it for Debug.--1017. TV use +3V C692 .1u/16V_4

RF_EN R613 *0_4 RF_EN_A RF_EN_B R614 0_4 RF_EN RF_EN 25

+5V_TV-CARD R566 0_6 +5V_TV-CARD_R

TV use +5V

For EMI PCCLK_DEBUG R567 *22_4 C695 *10P_4

SP@QUASAR-CA0404-071N21_92P

A/B MODULE Share pin

+3V for WWAN card is 2.75A

+3V R317 0_8 +3V_MINI C623 *22u/6.3V_8 C450 4.7u/6.3V_6 C453 4.7u/6.3V_6 C447 4.7u/6.3V_6 C448 4.7u/6.3V_6

+3V_MINI_B C457 C445 C454 .1u/16V_4

+3V_MINI_A C657 C653 C655 .1u/16V_4

+1.5V C455 .1u/16V_4 C456 .1u/16V_4 C444 4.7u/6.3V_6

+5V R565 0_6 +5V_TV-CARD C693 4.7u/6.3V_6 C694 .1u/16V_4

500mA, 25mil

+3VSUS Q30 *DTC144EUA R331 4.7K_4

13,21,25 PCIE_WAKE# PCIE_WAKE_WL_R_#

13,21 MSMB_DATA 13,21 MSMB_CLK

+3V R323 10K_4 Q27 2N7002 MINI_SMDATA R315 *0_4

+3V R324 10K_4 Q28 2N7002 MINI_SMCLK R316 *0_4

Quanta Computer Inc.

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	NEW&MINI&TV CARD/USB/BT/CIR	1A

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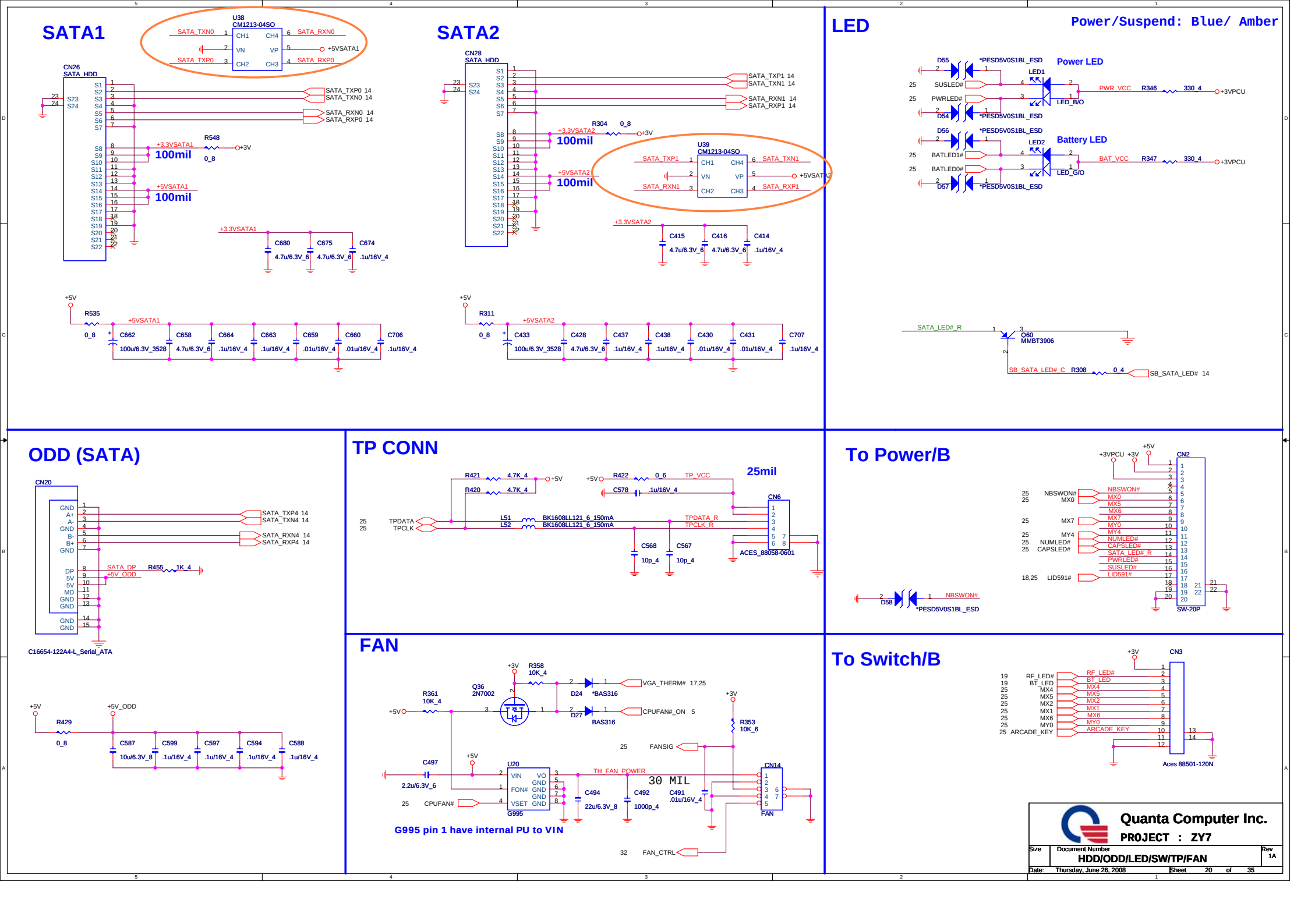
SATA1
U38
CM1213-04SO
SATA_TXN0
SATA_RXN0
SATA_TXP0
SATA_RXP0
+5VSATA1
CN26
SATA_HDD
SATA_TXP0 14
SATA_TXN0 14
SATA_RXN0 14
SATA_RXP0 14
R548
0_8
+3.3VSATA1
100mil
+3V
+5VSATA1
100mil
C680
C675
C674
4.7u/6.3V_6
4.7u/6.3V_6
.1u/16V_4
+5V
R535
0_8
C662
C658
C664
C663
C659
C660
C706
100u/6.3V_3528
4.7u/6.3V_6
.1u/16V_4
.1u/16V_4
.01u/16V_4
.01u/16V_4
.1u/16V_4
SATA2
CN28
SATA_HDD
SATA_TXP1 14
SATA_TXN1 14
SATA_RXN1 14
SATA_RXP1 14
R304
0_8
+3.3VSATA2
100mil
+3V
+5VSATA2
100mil
U39
CM1213-04SO
SATA_TXP1
SATA_TXN1
SATA_RXN1
SATA_RXP1
+5VSATA2
+3.3VSATA2
C415
C416
C414
4.7u/6.3V_6
4.7u/6.3V_6
.1u/16V_4
+5V
R311
0_8
C433
C428
C437
C438
C430
C431
C707
100u/6.3V_3528
4.7u/6.3V_6
.1u/16V_4
.1u/16V_4
.01u/16V_4
.01u/16V_4
.1u/16V_4
LED
Power/Suspend: Blue/ Amber
D55
*PESD5V0S1BL_ESD
Power LED
LED1
SUSLED#
PWRLED#
LED_B/O
PWR_VCC
R346
330_4
+3VPCU
D54
*PESD5V0S1BL_ESD
D56
*PESD5V0S1BL_ESD
Battery LED
LED2
BATLED1#
BATLED0#
LED_G/O
BAT_VCC
R347
330_4
+3VPCU
D57
*PESD5V0S1BL_ESD
SATA_LED#_R
Q60
MMBT3906
SB_SATA_LED#_C
R308
0_4
SB_SATA_LED#
ODD (SATA)
CN20
SATA_TXP4 14
SATA_TXN4 14
SATA_RXN4 14
SATA_RXP4 14
SATA_DP
+5V_ODD
R455
1K_4
C16654-122A4-L_Serial_ATA
+5V
+5V_ODD
R429
0_8
C587
C599
C597
C594
C588
10u/6.3V_8
.1u/16V_4
.1u/16V_4
.1u/16V_4
.1u/16V_4
TP CONN
25mil
R421
4.7K_4
R420
4.7K_4
+5V
R422
0_6
TP_VCC
C578
.1u/16V_4
TPDATA
TPCLK
L51
L52
BK1608LL121_6_150mA
BK1608LL121_6_150mA
TPDATA_R
TPCLK_R
C568
C567
10p_4
10p_4
CN6
ACES_88058-0601
FAN
Q36
2N7002
R358
10K_4
R361
10K_4
+3V
+5V
D24
*BAS316
D27
BAS316
VGA_THERM# 17,25
CPUFAN#_ON 5
R353
10K_6
FANSIG
C497
2.2u/6.3V_6
U20
G995
VIN
FON#
VSET
VO
GND
TH_FAN_POWER
30 MIL
C494
22u/6.3V_8
C492
1000p_4
C491
.01u/16V_4
CPUFAN#
CN14
FAN
FAN_CTRL
G995 pin 1 have internal PU to VIN
To Power/B
+3VPCU
+3V
+5V
CN2
NBSWON#
MX0
MX5
MX6
MX7
MY0
MY4
NUMLED#
CAPSLED#
SATA_LED#_R
PWRLED#
SUSLED#
LID591#
SW-20P
D58
*PESD5V0S1BL_ESD
To Switch/B
+3V
CN3
RF_LED#
BT_LED
MX4
MX5
MX2
MX1
MX6
MY0
ARCADE_KEY
Aces 88501-120N
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1A
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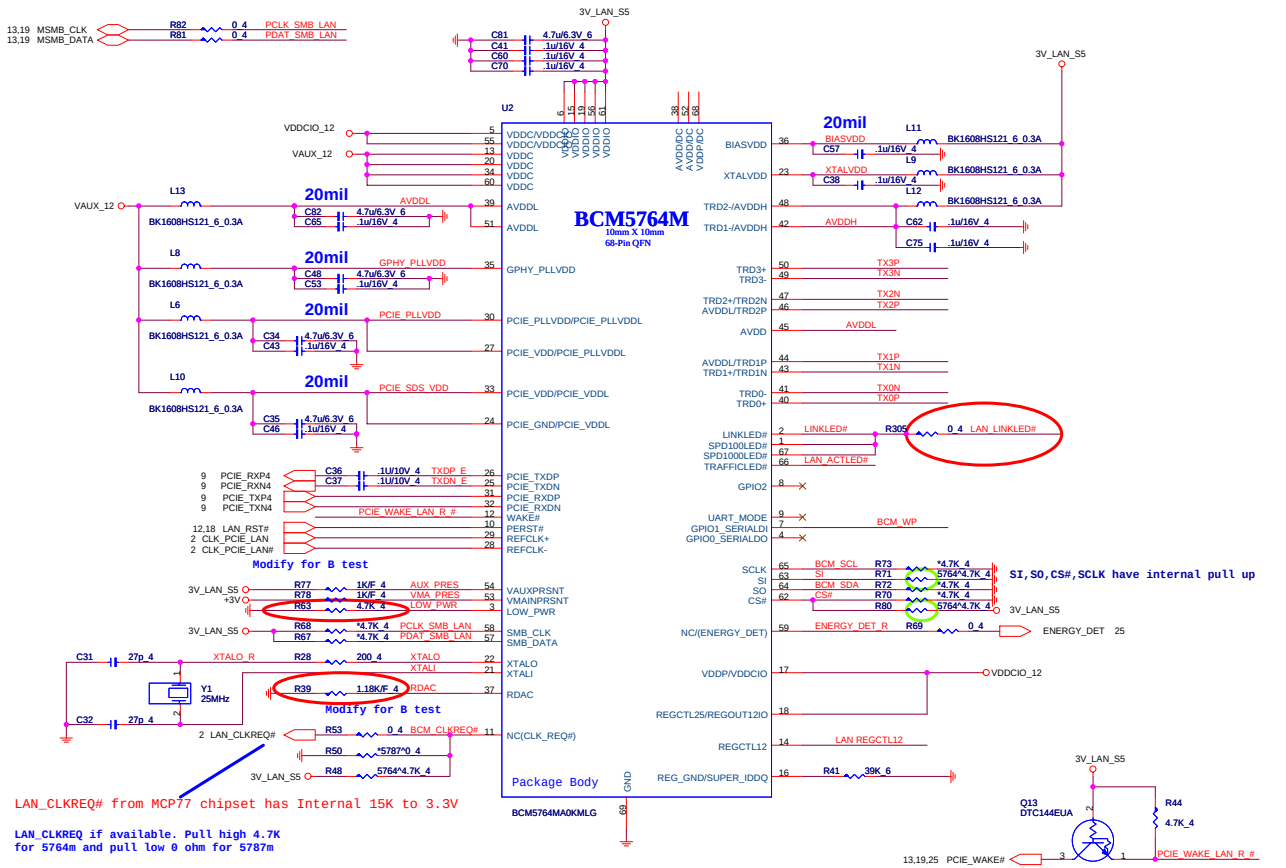
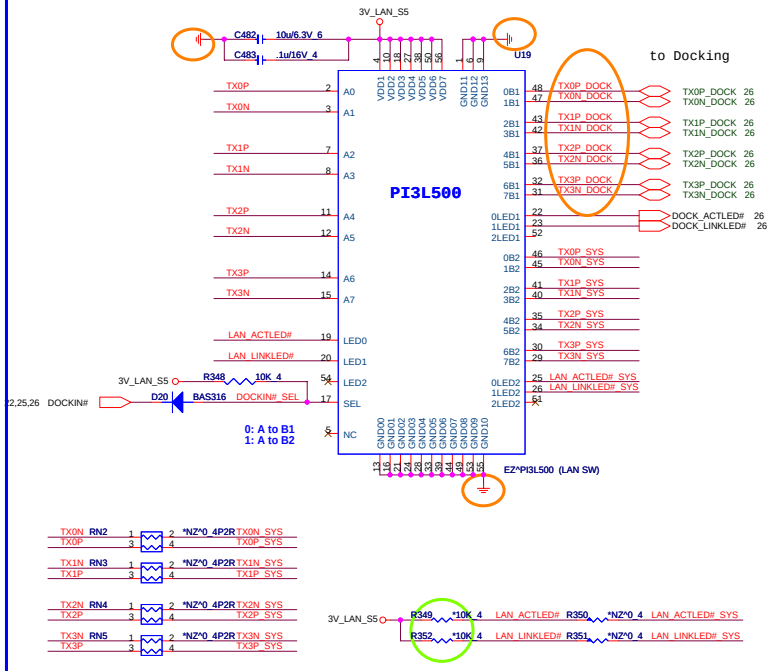
Giga LAN BCM5787M/5764M



LAN SWITCH

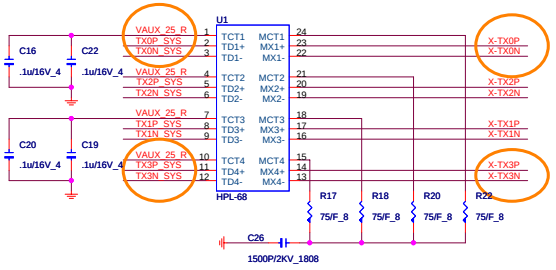


Transfomer

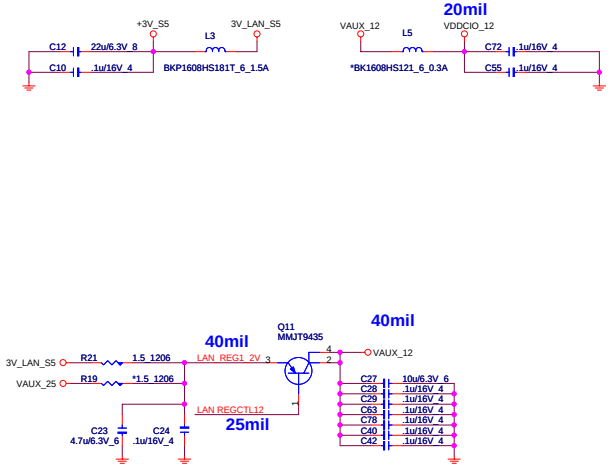
Source 1: DELTA LFE9249 DB0ZR1LAN11

Source 2: Bothand GST5009 DBKN1NLAN03

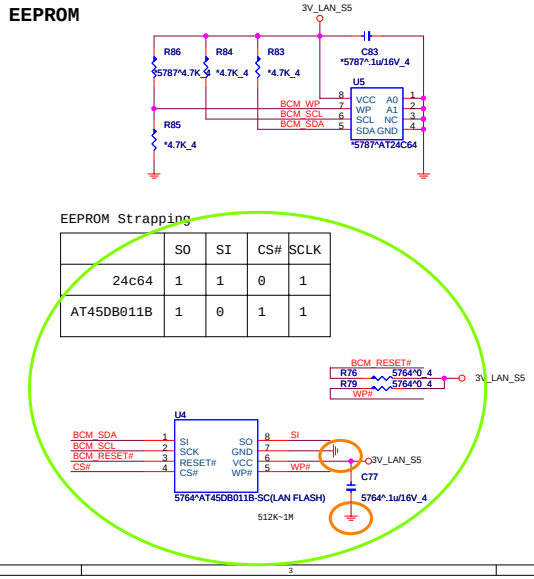
REV B: SWAP net for layout issue---0214



LAN POWER



EEPROM

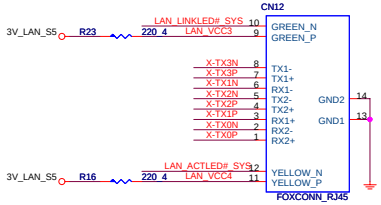


EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

RJ45 connector

Modify for C test



Quanta Computer Inc.

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	GigaLAN BCM5787M/5764M & RJ45	1A

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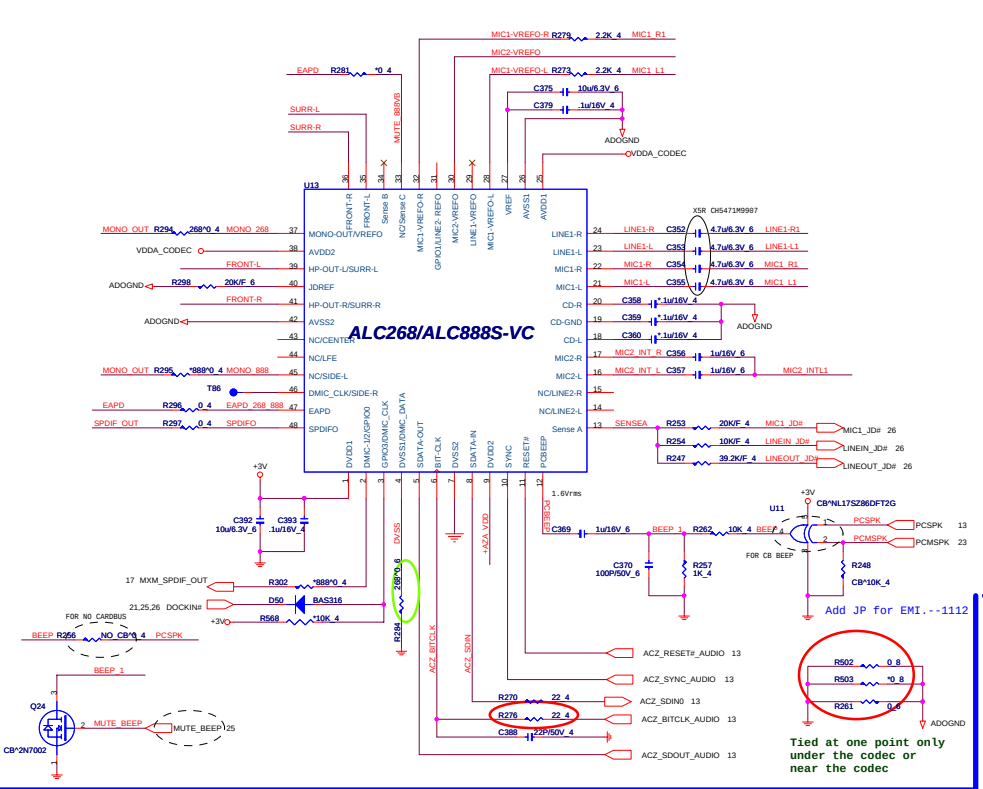
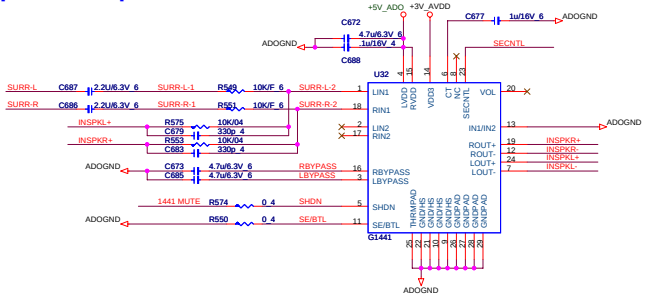
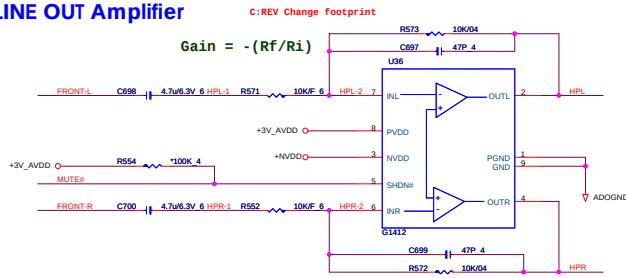
CODEC



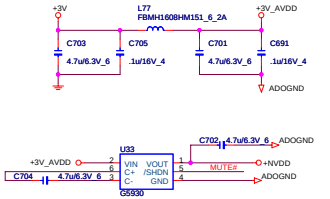
Speaker Amplifier



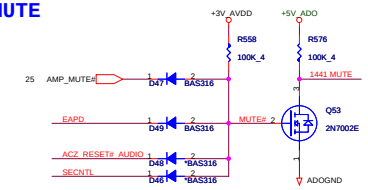
LINE OUT Amplifier



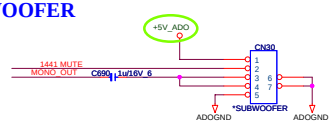
Amplifier POWER



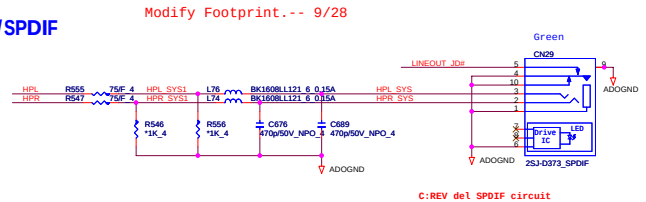
MUTE



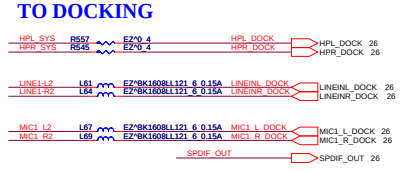
SUBWOOFER



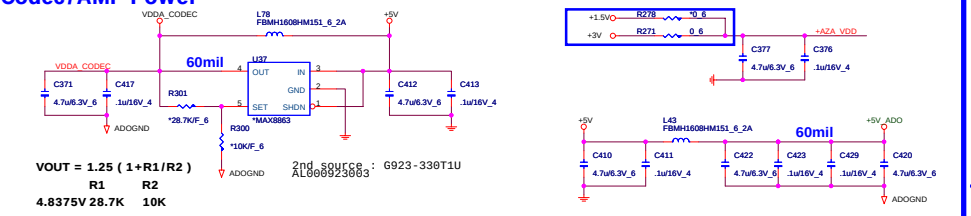
LINE OUT/SPDIF



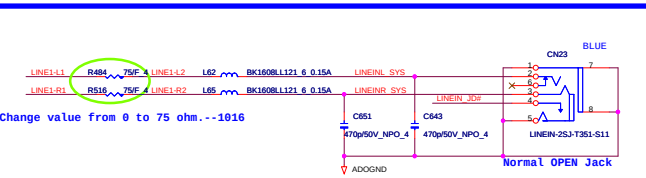
TO DOCKING



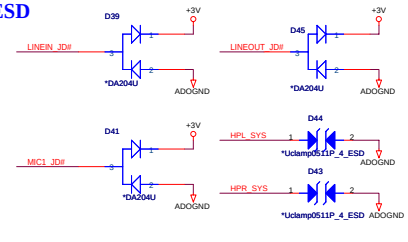
Codec/AMP Power



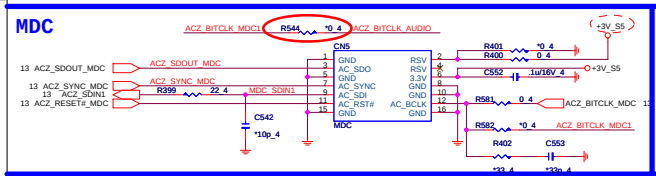
LINE IN



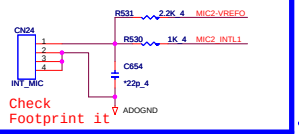
ESD



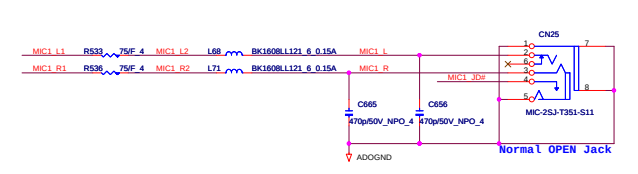
MDC



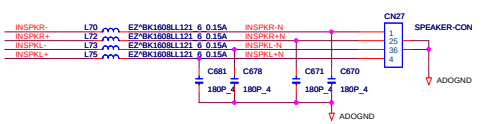
INT MIC.

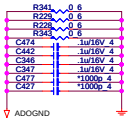


MIC



SPEAKER





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	CODEC/AMP/MDC	1A
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NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

Modify it from 150 to 100ohm.--0928

AD20 R328 100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

For EMI

PCLK_PCM — R329 *22_4 — C463 *22p_4

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

+3V — C424 4.7u/6.3V_6 — C451 .1u/16V_4 — C458 .1u/16V_4 — C439 .1u/16V_4

R321 33K/F_6 — R322 33K/F_6 — VPPD0

U16 OZ601T

CORE_VCC ×4, PCI_VCC ×3

12,16 AD[31..0] — AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

PCM_IDSEL

12 CBE3# CBE2# CBE1# CBE0#

12 PCLK_PCM

12 DEVSEL# FRAME# IRDY# TRDY# STOP# PAR

12 PERR#

12 REQ0# GNT0#

12,19 PCIRST# — R334 0_4 — PCIRST#_R
13 PCI_PME# — R330 0_4 — PCM_PME#

12,25 CLKRUN#
22 PCMSPK
12,19,25 SERIRQ
12 INTA#

VCC5#/VCCD0#/SDATA
VCC3#/VCCD1#/SCLK
VPP_PGM/VPPD0/SLATCH

VCCD0 VCCD1

CAD31 CAD30 CAD29 CAD28 CAD27 CAD26 CAD25 CAD24 CAD23 CAD22 CAD21 CAD20 CAD19 CAD18 CAD17 CAD16 CAD15 CAD14 CAD13 CAD12 CAD11 CAD10 CAD9 CAD8 CAD7 CAD6 CAD5 CAD4 CAD3 CAD2 CAD1 CAD0

R_A_CCLK

CCLK CFRAME# CIRDY# CTRDY# CDEVSEL# CSTOP# CPAR CPERR# CSERR# CREQ# CGNT# CINT# CBLOCK# CCLKRUN# CRST# R2_D2 R2_D14 R2_A18 CVS1 CVS2 CCD1# CCD2# CAUDIO CSTSCHG

CC/BE3# CC/BE2# CC/BE1# CC/BE0#

A_CFRAME# A_CIRDY# A_CTRDY# A_CDEVSEL# A_CSTOP# A_CPAR A_CPERR# A_CSERR# A_CREQ# A_CGNT# A_CINT# A_CBLOCK# A_CCLKRUN#

A_CRST# R312 47K — SKT_VCC

RST# PME#/RI_OUT# MF6 (CLKRUN#) MF4 (RI_OUT#) MF3 (SERIRQ#) MF0 (INTA#)

GND ×6 — 32 45 65 96 128

R_A_CCLK R306 33_4 A_CCLK

PCMCIA SOCKET

Check it

CN10

A_CAD0	2	GND1	1	SKTAVCC1	17 — SKT_VCC
A_CAD1	3	SKTAAD0/D3	51	SKTAVCC2	
A_CAD3	4	SKTAAD1/D4			
A_CAD5	5	SKTAD3/D5	18	SKTAVPP1	
A_CAD7	6	SKTAD5/D6	52	SKTAVPP2	
A_CC/BE0#	7	SKTAAD7/D7			
A_CAD9	8	-SKTACBE0/CE1#			
A_CAD11	9	SKTAAD9/A10			
A_CAD12	10	SKTABAD11/OE#		GND5	69
A_CAD14	11	SKTAAD12/A11		GND6	70
A_CC/BE1#	12	SKTAAD14/A9		GND7	71
A_CPAR	13	-SKTACBE1/A8		GND8	72
A_CPERR#	14	SKTAPAR/A13		GND9	73
A_CGNT#	15	-SKTAPERR/A14		GND10	74
A_CINT#	16	-SKTAGNT/WE#		GND11	75
		-SKTAINT/RDY		GND12	76
		UPPER PIN		GND13	77
A_CCLK	19	SKTAPCLK/A16		GND14	78
A_CIRDY#	20	-SKTAIRDY/A15		GND15	79
A_CC/BE2#	21	-SKTACBE2/A12		GND16	80
A_CAD18	22	SKTAAD18/A7		GND17	81
A_CAD20	23	SKTAAD20/A6		GND18	82
A_CAD21	24	SKTAAD21/A5		GND19	83
A_CAD22	25	SKTAAD22/A4		GND20	84
A_CAD23	26	SKTAAD23/A3			
A_CAD24	27	SKTAAD24/A2			
A_CAD25	28	SKTAAD25/A1			
A_CAD26	29	SKTAAD26/A0		NC	85
A_CAD27	30	SKTAAD27/D0		NC	86
A_CAD29	31	SKTAAD29/D1		NC	87
A_CRSVD/D2	32	SKTARSVD/D2		NC	88
A_CCLKRUN#	33	-SKTACLKRUN/WP			
	34	GND2			
	35	GND3			
A_CCD1#	36	-SKTACD1/CD1#			
A_CAD2	37	SKTAAD2/D11			
A_CAD4	38	SKTAD4/D12			
A_CAD6	39	SKTAAD6/D13			
A_CRSVD/D14	40	SKTARSVD/D14			
A_CAD8	41	SKTAAD8/D15			
A_CAD10	42	SKTAAD10/CE2#			
A_CVS1#	43	-SKTAVS1/VS1#			
A_CAD13	44	SKTAAD13/IORD#			
A_CAD15	45	SKTAAD15/IOWR#			
A_CAD16	46	SKTAAD16/A17			
A_CRSVD/A18	47	-SKTRSVD/A18			
A_CBLOCK#	48	-SKTALOCK/A19			
A_CSTOP#	49	-SKTASTOP/A20			
A_CDEVSEL#	50	-SKTADEVSEL/A21			
		LOWER PIN			
A_CTRDY#	53	-SKTATRDY/A22			
A_CFRAME#	54	-SKTAFRAME/A23			
A_CAD17	55	SKTAAD17/A24			
A_CAD19	56	SKTAAD19/A25			
A_CVS2#	57	-SKTAVS2/VS2#			
A_CRST#	58	-SKTARST/RESET			
A_CSERR#	59	0SKTASERR/WAIT#			
A_CREQ#	60	-SKTAREQ/INPACK#			
A_CC/BE3#	61	-SKTACBE3/REG#			
A_CAUDIO	62	SKTAAUDIO/BVD2			
A_CSTSCHG	63	-SKTASTSCHG/BVD1			
A_CAD28	64	SKTAAD28/D8			
A_CAD30	65	SKTAAD30/D9			
A_CAD31	66	SKTAAD31/D10			
A_CCD2#	67	-SKTACD2/CD2#			
	68	GND4			

PCMCIA_SOCKET

Del SKT_VCC.-0927

SKT_VCC — C472 4.7u/6.3V_6 — C471 .1u/16V_4 — C475 4.7u/6.3V_6 — C473 .1u/16V_4 — C465 4.7u/6.3V_6 — C467 .1u/16V_4

U18 OZ2210G
VCC1 +3.3 (6,5) — VCC2 +3.3 (7,8) — VCC5# +5V (3,4) — VCC3# GND (1,2)
VCCD0 VCCD1

Check Footprint

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

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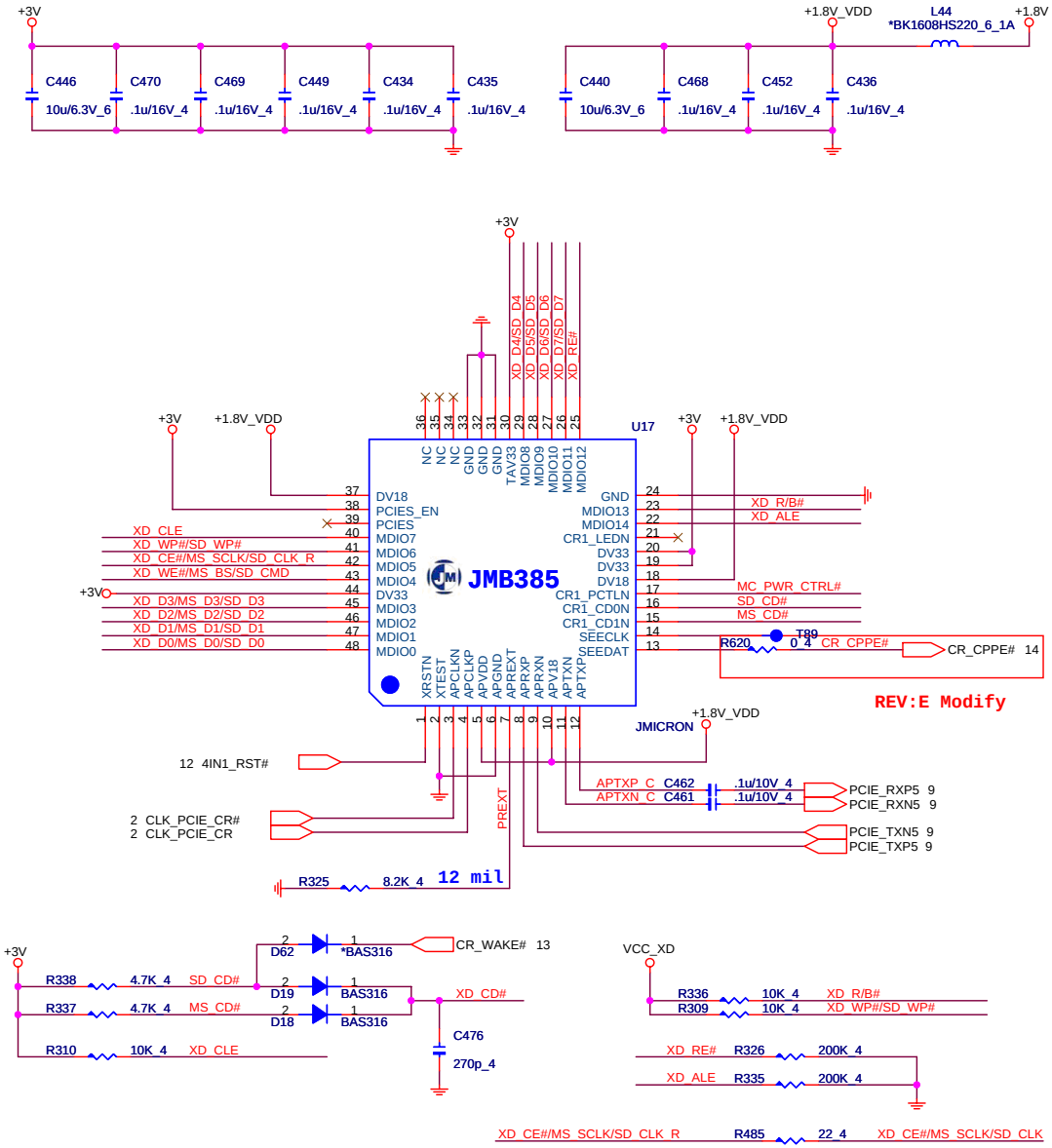
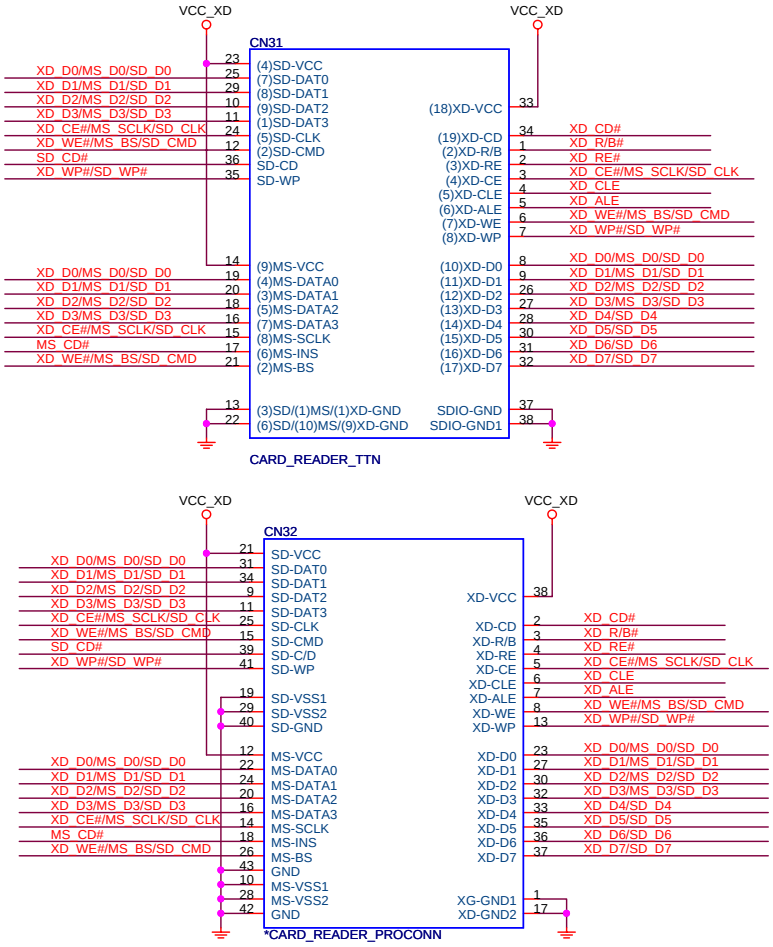
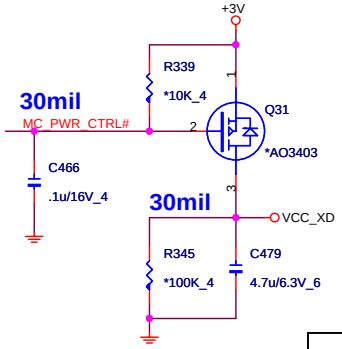
4 IN 1 CARD READER

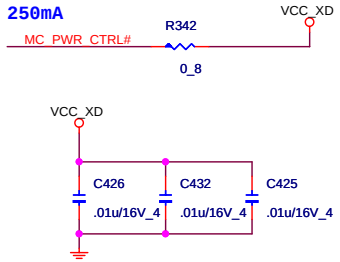




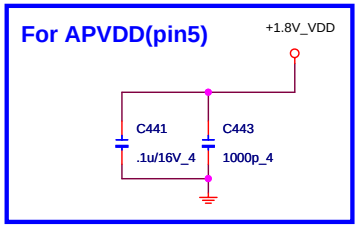
Memory Card Power Supply



Use 0805 type and over 20 mils trace width on both side



APVDD(pin5) must put C601/1000pF close to APVDD(pin5) (length must under 120mil) and trace width = 20mil, after C601, pls put one more 0.1uF for it.



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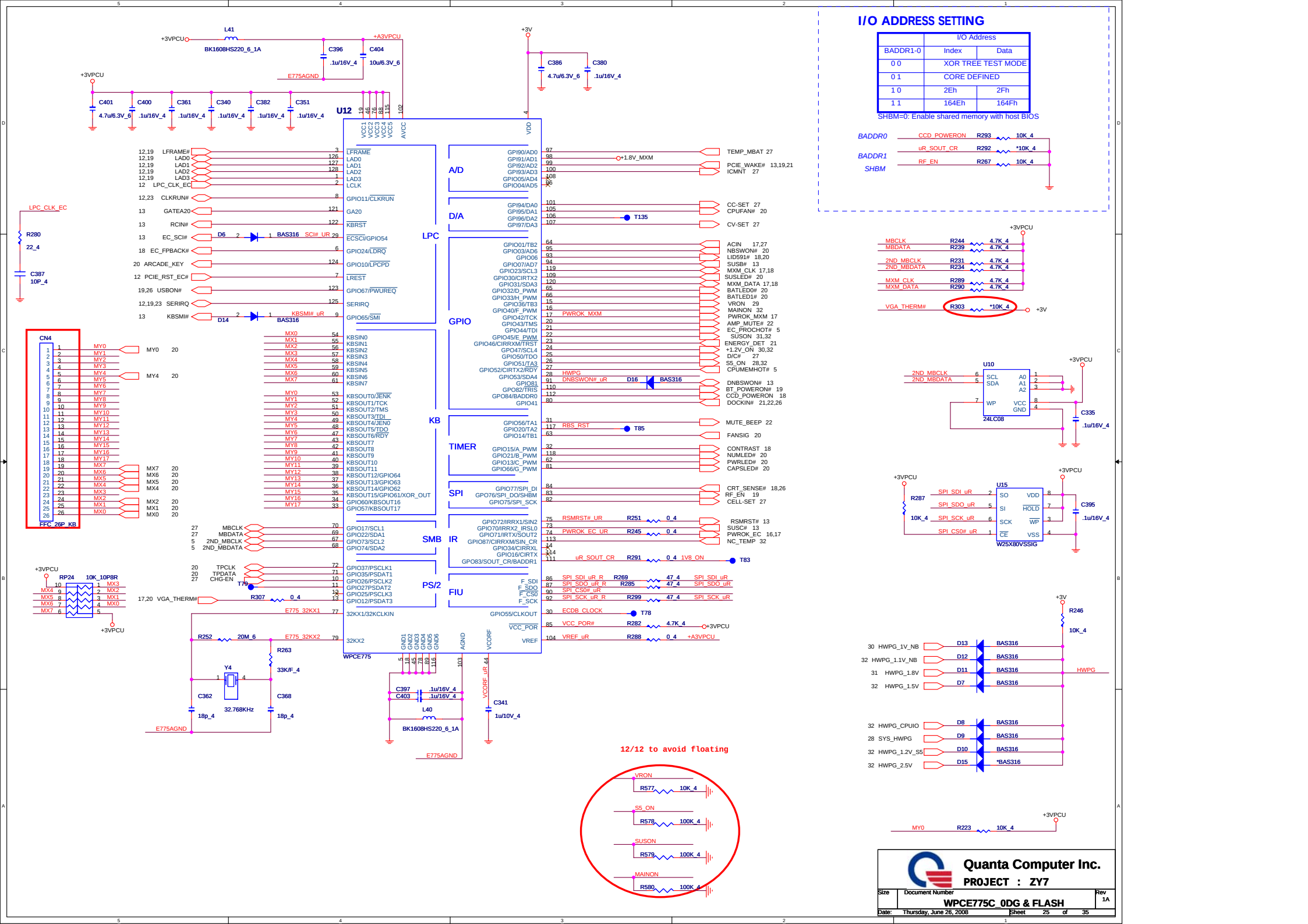
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0
BADDR1
SHBM
CCD_POWERON R293 10K_4
uR_SOUT_CR R292 *10K_4
RF_EN R267 10K_4
U12
WPCE775
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
LFRAME#
LAD0
LAD1
LAD2
LAD3
LCLK
GPIO11/CLKRUN
GA20
KBRST
ECSCI/GPIO54
GPIO24/LDRQ
GPIO10/LPCPD
LREST
GPIO67/PWUREQ
SERIRQ
GPIO65/SMI
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4/JEN0
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
GPIO60/KBSOUT16
GPIO57/KBSOUT17
GPIO17/SCL1
GPIO22/SDA1
GPIO73/SCL2
GPIO74/SDA2
GPIO37/PSCLK1
GPIO35/PSDAT1
GPIO26/PSCLK2
GPIO27/PSDAT2
GPIO25/PSCLK3
GPIO12/PSDAT3
32KX1/32KCLKIN
32KX2
GPI90/AD0
GPI91/AD1
GPI92/AD2
GPI93/AD3
GPIO05/AD4
GPIO04/AD5
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
GPIO01/TB2
GPIO03/AD6
GPIO06
GPIO07/AD7
GPIO23/SCL3
GPIO30/CIRTX2
GPIO31/SDA3
GPIO32/D_PWM
GPIO33/H_PWM
GPIO36/TB3
GPIO40/F_PWM
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45/E_PWM
GPIO46/CIRRXM/TRST
GPO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/CIRTX2/RDY
GPIO53/SDA4
GPIO81
GPO82/TRIS
GPO84/BADDR0
GPIO41
GPIO56/TA1
GPIO20/TA2
GPIO14/TB1
GPIO15/A_PWM
GPIO21/B_PWM
GPIO13/C_PWM
GPIO66/G_PWM
GPIO77/SPI_DI
GPO76/SPI_DO/SHBM
GPIO75/SPI_SCK
GPIO72/IRRX1/SIN2
GPIO70/IRRX2_IRSL0
GPIO71/IRTX/SOUT2
GPIO87/CIRRXM/SIN_CR
GPIO34/CIRRXL
GPIO16/CIRTX
GPO83/SOUT_CR/BADDR1
F_SDI
F_SDO
F_CS0
F_SCK
GPIO55/CLKOUT
VCC_POR
VREF
VDD
AVCC
VCC1
VCC2
VCC3
VCC4
VCC5
GND1
GND2
GND3
GND4
GND5
GND6
AGND
VCORF
TEMP_MBAT 27
PCIE_WAKE# 13,19,21
ICMNT 27
+1.8V_MXM
CC-SET 27
CPUFAN# 20
T135
CV-SET 27
ACIN 17,27
NBSWON# 20
LID591# 18,20
SUSB# 13
MXM_CLK 17,18
SUSLED# 20
MXM_DATA 17,18
BATLED0# 20
BATLED1# 20
VRON 29
MAINON 32
PWROK_MXM 17
AMP_MUTE# 22
EC_PROCHOT# 5
SUSON 31,32
ENERGY_DET 21
+1.2V_ON 30,32
D/C# 27
S5_ON 28,32
CPUMEMHOT# 5
PWROK_MXM
DNBSWON# uR
D16
BAS316
DNBSWON# 13
BT_POWERON# 19
CCD_POWERON 18
DOCKIN# 21,22,26
MUTE_BEEP 22
RBS_RST
T85
FANSIG 20
CONTRAST 18
NUMLED# 20
PWRLED# 20
CAPSLED# 20
CRT_SENSE# 18,26
RF_EN 19
CELL-SET 27
RSMRST# UR
R251
0_4
RSMRST# 13
SUSC# 13
PWROK_EC UR
R245
PWROK_EC 16,17
NC_TEMP 32
uR_SOUT_CR
R291
0_4 1V8_ON
T83
SPI_SDI_uR_R
R269
47_4
SPI_SDI_uR
SPI_SDO_uR_R
R285
SPI_SDO_uR
SPI_CS0#_uR
SPI_SCK_uR_R
R299
SPI_SCK_uR
ECDB_CLOCK
T78
VCC_POR#
R282
4.7K_4
+3VPCU
VREF_uR
R288
0_4
+A3VPCU
E775_32KX1
E775_32KX2
R252
20M_6
R263
33K/F_4
Y4
32.768KHz
C362
18p_4
C368
18p_4
E775AGND
C397
C403
.1u/16V_4
L40
BK1608HS220_6_1A
C341
1u/10V_4
VCORF uR 44
12/12 to avoid floating
VRON
R577
10K_4
S5_ON
R578
100K_4
SUSON
R579
100K_4
MAINON
R580
100K_4
CN4
FFC_26P_KB
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MY16
MY17
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
RP24
10K_10P8R
T79
R307
0_4
VGA_THERM#
LPC_CLK_EC
R280
22_4
C387
10P_4
D6
BAS316
SCI# uR
D14
KBSMI# uR
MBCLK
MBDATA
2ND_MBCLK
2ND_MBDATA
TPCLK
TPDATA
CHG-EN
R244
R239
R231
R234
R289
R290
R303
*10K_4
U10
24LC08
C335
.1u/16V_4
U15
W25X80VSSIG
R287
10K_4
C395
.1u/16V_4
R246
10K_4
D13
D12
D11
D7
D8
D9
D10
D15
*BAS316
HWPG
HWPG_1V_NB
HWPG_1.1V_NB
HWPG_1.8V
HWPG_1.5V
HWPG_CPUIO
SYS_HWPG
HWPG_1.2V_S5
HWPG_2.5V
MY0
R223
10K_4
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CABLE DOCK

CN13-4 EZ^CABLE DOCKING

13 USBP9+ — EZ^0_4 R26 — BUSBP9+ — 47 USB+
13 USBP9- — EZ^0_4 R30 — BUSBP9- — 48 USB-
19,25 USBON# — USBON# — 49 USB_EN#
VAUX_25 — 50 RESERVED1
18,25 CRT_SENSE# — EZ^0_4 R529 — CRT_SEN# D — 51 RESERVED2
L7 — VAUX_25_EZ — 52 LAN_PWR
*EZ^BK1608HS121_6_0.3A
LAN-PWR,500mA

21 DOCK_ACTLED# — 53 LAN_ACT
21 DOCK_LINKLED# — 54 LAN_LINK
55 GND

To LAN

21 TX0P_DOCK — 56 LAN_0
21 TX0N_DOCK — 57 LAN_0#
58 GND

21 TX1P_DOCK — 59 LAN_1
21 TX1N_DOCK — 60 LAN_1#
61 GND

21 TX3P_DOCK — 62 LAN_3
21 TX3N_DOCK — 63 LAN_3#
64 GND

GND — 69
GND — 70

CN13-3 EZ^CABLE DOCKING

+5VPCU
P3-PWR: 5V_USB,3A — 68

5V_USB, 3A

LIN_IN_DT# — 33 LINEIN_JD# 22
LIN_IN_L — 34 LINEINL_DOCK 22
LIN_IN_R — 35 LINEINR_DOCK 22

MIC_DT# — 36 MIC1_JD# 22
MIC_L — 37 MIC1_L_DOCK 22
MIC_R — 38 MIC1_R_DOCK 22

GNDA — 39 ADOGND1

DOCK_DT1# — 40 DOCKIN# 21,22,25
SPDIF — 41 SPDIF_OUT 22

GND — 42

LAN_2 — 43 TX2P_DOCK 21
LAN2# — 44 TX2N_DOCK 21

GND — 45

GND — 71
P4-PWR : 19V,5A — 67

VA_DOCK
C481 EZ^10u/25V_1206
C33 EZ^.1u/16V_4

REV C: Change to 1K --0408

CN13-2 EZ^CABLE DOCKING

P1-PWR : GND — 65
R35 EZ^1K_4 DOCKIN2# — 20 DOCK_DT2#

22 HPL_DOCK — 21 HP_L
22 HPR_DOCK — 22 HP_R
22 LINEOUT_JD# — 23 HP_DT#
ADOGND1 — 24 GNDA

DOCK_DVI_HP_A — 25 DVI_DT
18 DOCK_HDMI_DDCDATA — 26 DVI_DDCDT
18 DOCK_HDMI_DDCCLK — 27 DVI_DDCCK

18 CRT_VSYNC_DOCK — 28 VGA_VS
18 CRT_HSYNC_DOCK — 29 VGA_HS

18 CRT_DDCCLK_DOCK — 30 VGA_DDCCK
18 CRT_DDCDAT_DOCK — 31 VGA_DDCDT

+5V — 32 5V_S0

P2-GND — 66
GND — 72

TO POWER VA (19V,5A)

CN13-1 EZ^CABLE DOCKING

GND — 1
DVI_CLKP — 2 DOCK_HDMICLK 18
DVI_CLKN — 3 DOCK_HDMICLK# 18

GND — 4
DVI_TX0P — 5 DOCK_HDMITX0 18
DVI_TX0N — 6 DOCK_HDMITX0# 18

GND — 7
DVI_TX1P — 8 DOCK_HDMITX1 18
DVI_TX1N — 9 DOCK_HDMITX1# 18

GND — 10
DVI_TX2P — 11 DOCK_HDMITX2 18
DVI_TX2N — 12 DOCK_HDMITX2# 18
GND — 13

VGA_R — 14 VGA_RED_DOCK 18
GND — 15
VGA_G — 16 VGA_GRN_DOCK 18
GND — 17
VGA_B — 18 VGA_BLU_DOCK 18
GND — 19

NC — 74
NC — 73

D42 *DA204U
CRT_SEN# D — 3
+3V — 1
2

VA_DOCK
R29 *EZ^0_6
R31 *EZ^0_6
PD5
VA1
SBM1040-13-F
PD6 SW1010CPT
DCIN_S

+5V
+3V_S5
R24 EZ^10K_4
DOCK_INSERT_5V 18 To CRT
R25 EZ^10K_4
Q12 EZ^2N7002E
DOCKIN#
C30 EZ^.1u/16V_4
+3V_S5
R543 *10K_4
DOCK_IN To EC
Q58 *2N7002E
C418 *.1u/16V_4
A1A:(9/18) Refer to Acer DVR1019

CHECK +3V or +5V

EMI Solution

DOCK_ACTLED# C64 *10p_4
DOCK_LINKLED# C66 *10p_4
HPL_DOCK C56 *10p_4
HPR_DOCK C59 *10p_4
LINEINL_DOCK C45 *10p_4
LINEINR_DOCK C61 *10p_4
MIC1_L_DOCK C52 *10p_4
MIC1_R_DOCK C67 *10p_4
VGA_RED_DOCK C484 *10p_4
VGA_GRN_DOCK C485 *10p_4
VGA_BLU_DOCK C486 *10p_4
CRT_HSYNC_DOCK C68 *10p_4
CRT_VSYNC_DOCK C71 *10p_4
CRT_DDCCLK_DOCK C74 *10p_4
CRT_DDCDAT_DOCK C69 *10p_4

R43 EZ^0_4
R40 EZ^0_4
C51 EZ^.1u/16V_4
C39 EZ^.1u/16V_4
C44 EZ^.1u/16V_4
C54 EZ^.1u/16V_4
C58 *1000p_4
C47 *1000p_4
ADOGND1

+3V_S5
C383 EZ^4.7u/6.3V_6
C385 EZ^1u/10V_4
C384 EZ^.1u/16V_4

+5V
C515 EZ^4.7u/6.3V_6
C73 EZ^1u/10V_4
C76 EZ^.1u/16V_4

DOCK_DVI_HP_A R47 *10K_4
EZ^1K_4 R49
DOCK_DVI_HPD 18 R46 EZ^10K_4

REV:E Modify

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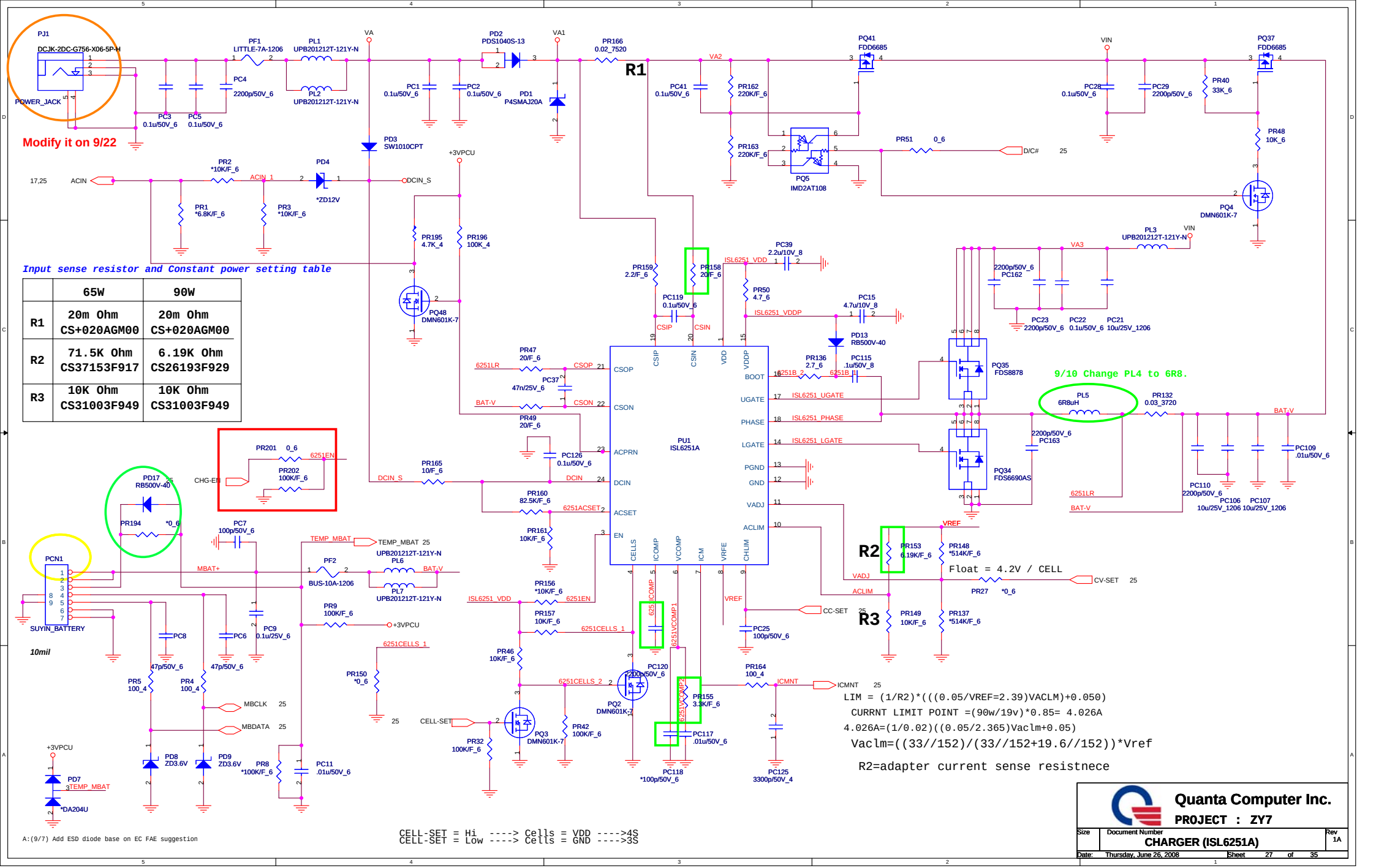
PJ1
DCJK-2DC-G756-X06-5P-H
POWER_JACK
Modify it on 9/22
PF1
LITTLE-7A-1206
PL1
UPB201212T-121Y-N
PL2
UPB201212T-121Y-N
PC4
2200p/50V_6
PC3
0.1u/50V_6
PC5
0.1u/50V_6
VA
PD2
PDS1040S-13
VA1
PR166
0.02_7520
R1
PC1
0.1u/50V_6
PC2
0.1u/50V_6
PD1
P4SMAJ20A
PD3
SW1010CPT
+3VPCU
PR2
*10K/F_6
ACIN_1
PD4
*ZD12V
DCIN_S
17,25
ACIN
PR1
*6.8K/F_6
PR3
*10K/F_6
PR195
4.7K_4
PR196
100K_4
PQ48
DMN601K-7
Input sense resistor and Constant power setting table
65W
90W
R1
20m Ohm
CS+020AGM00
20m Ohm
CS+020AGM00
R2
71.5K Ohm
CS37153F917
6.19K Ohm
CS26193F929
R3
10K Ohm
CS31003F949
10K Ohm
CS31003F949
PR201
0_6
6251EN
PR202
100K/F_6
CHG-EN
PD17
RB500V-40
PR194
*0_6
PC7
100p/50V_6
PCN1
SUYIN_BATTERY
10mil
MBAT+
TEMP_MBAT
TEMP_MBAT 25
PF2
BUS-10A-1206
PL6
UPB201212T-121Y-N
PL7
UPB201212T-121Y-N
BAT-V
PR9
100K/F_6
+3VPCU
PC8
47p/50V_6
PC6
47p/50V_6
PC9
0.1u/25V_6
PR5
100_4
PR4
100_4
MBCLK
25
MBDATA
25
PD8
ZD3.6V
PD9
ZD3.6V
PR8
*100K/F_6
PC11
.01u/50V_6
PD7
TEMP_MBAT
*DA204U
PR165
10/F_6
DCIN_S
PR160
82.5K/F_6
6251ACSET
PR161
10K/F_6
PR47
20/F_6
6251LR
PC37
47n/25V_6
BAT-V
PR49
20/F_6
PC126
0.1u/50V_6
PU1
ISL6251A
CSOP
CSON
ACPRN
DCIN
ACSET
EN
CSIP
CSIN
VDD
VDDP
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
CELLS
ICOMP
VCOMP
ICM
VREFE
CHLIM
PR119
0.1u/50V_6
PR159
2.2/F_6
PR158
20/F_6
ISL6251_VDD
PC39
2.2u/10V_8
PR50
4.7_6
ISL6251_VDDP
PC15
4.7u/10V_8
PD13
RB500V-40
PR136
2.7_6
PC115
.1u/50V_8
6251B_2
6251B_1
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PQ35
FDS8878
PQ34
FDS6690AS
9/10 Change PL4 to 6R8.
PL5
6R8uH
PR132
0.03_3720
2200p/50V_6
PC163
PC109
.01u/50V_6
PC110
2200p/50V_6
PC106
10u/25V_1206
PC107
10u/25V_1206
6251LR
BAT-V
PR156
*10K/F_6
6251EN
PR157
10K/F_6
6251CELLS_1
PR46
10K/F_6
6251CELLS_2
PR150
*0_6
25
CELL-SET
PR32
100K/F_6
PQ3
DMN601K-7
PR42
100K/F_6
PC120
2200p/50V_6
PQ2
DMN601K-7
PR155
3.3K/F_6
PC117
.01u/50V_6
PC118
*100p/50V_6
PR164
100_4
ICMNT
ICMNT 25
PC125
3300p/50V_4
VREF
PR153
6.19K/F_6
PR148
*514K/F_6
Float = 4.2V / CELL
CV-SET
25
PR27
*0_6
CC-SET
25
PC25
100p/50V_6
PR149
10K/F_6
PR137
*514K/F_6
LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece
PR51
0_6
D/C#
25
PQ5
IMD2AT108
PQ41
FDD6685
PQ37
FDD6685
PQ4
DMN601K-7
PR40
33K_6
PR48
10K_6
PC28
0.1u/50V_6
PC29
2200p/50V_6
PL3
UPB201212T-121Y-N
PC162
2200p/50V_6
PC23
2200p/50V_6
PC22
0.1u/50V_6
PC21
10u/25V_1206
A:(9/7) Add ESD diode base on EC FAE suggestion
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
Quanta Computer Inc.
PROJECT : ZY7
Size
Document Number
CHARGER (ISL6251A)
Rev
1A
Date: Thursday, June 26, 2008
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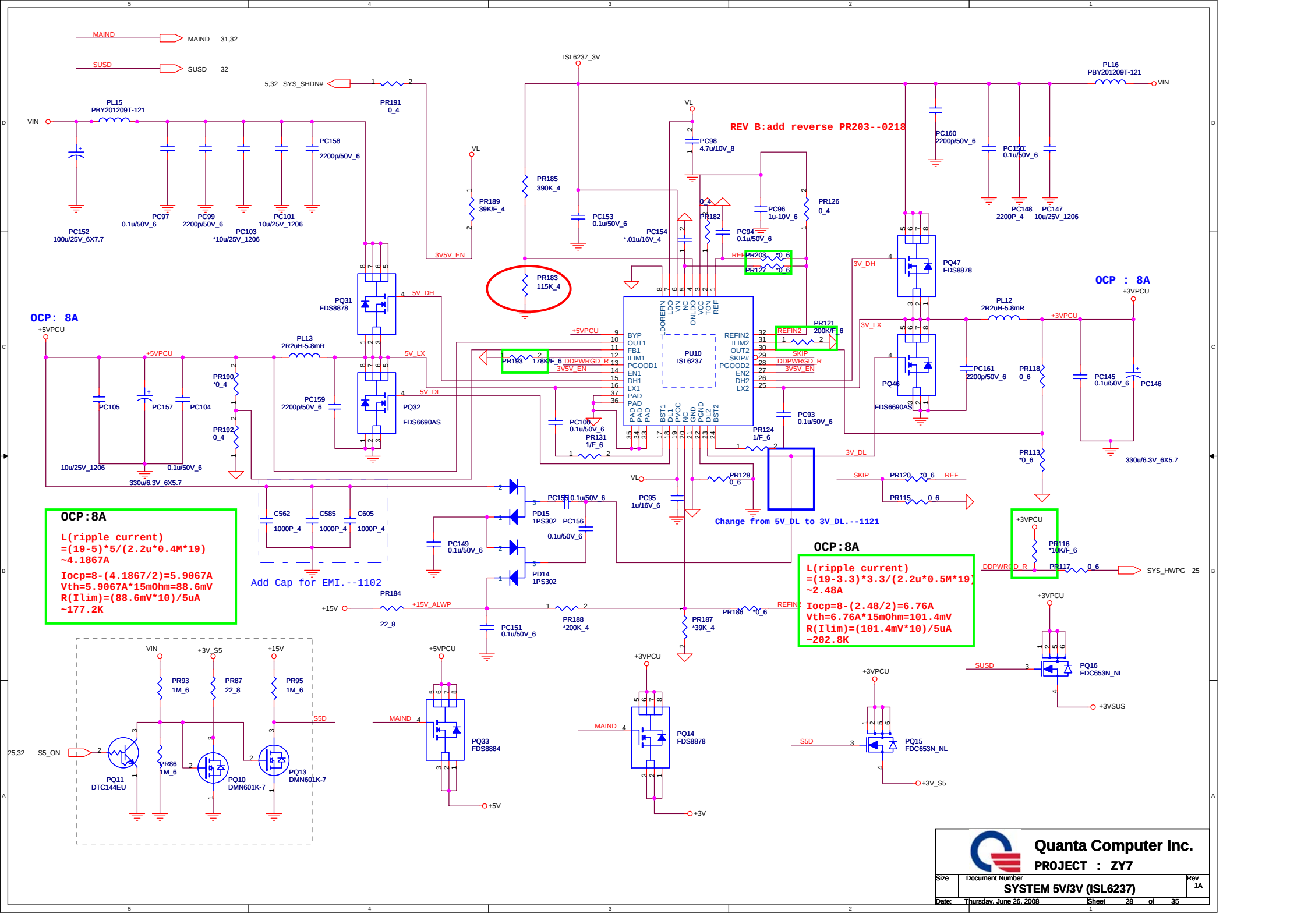
MAIND
MAIND 31,32
SUSD
SUSD 32
5,32 SYS_SHDN#
ISL6237_3V
PL16
PBY201209T-121
VIN
PL15
PBY201209T-121
PR191
0_4
PC158
2200p/50V_6
PC152
100u/25V_6X7.7
PC97
0.1u/50V_6
PC99
2200p/50V_6
PC103
*10u/25V_1206
PC101
10u/25V_1206
VL
PR189
39K/F_4
3V5V_EN
PR185
390K_4
PC153
0.1u/50V_6
PC154
*.01u/16V_4
PC98
4.7u/10V_8
PR182
0_4
PC96
1u-10V_6
PC94
0.1u/50V_6
PR126
0_4
REF
PR203 *0_6
PR127 *0_6
PR183
115K_4
REV B:add reverse PR203--0218
PC160
2200p/50V_6
PC150
0.1u/50V_6
PC148
2200P_4
PC147
10u/25V_1206
OCP: 8A
+5VPCU
PQ31
FDS8878
5V_DH
5V_LX
5V_DL
PQ32
FDS6690AS
PL13
2R2uH-5.8mR
PR190
*0_4
PR192
0_4
PC105
PC157
PC104
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PC159
2200p/50V_6
PR193
178K/F_6
DDPWRGD_R
3V5V_EN
PU10
ISL6237
PC100
0.1u/50V_6
PR131
1/F_6
PC93
0.1u/50V_6
PR124
1/F_6
3V_DL
PR121
200K/F_6
REFIN2
SKIP
3V_DH
3V_LX
PQ47
FDS8878
PQ46
FDS6690AS
PL12
2R2uH-5.8mR
PC161
2200p/50V_6
PR118
0_6
PC145
0.1u/50V_6
PC146
330u/6.3V_6X5.7
PR113
*0_6
OCP : 8A
+3VPCU
PR120 *0_6
PR115 0_6
REF
SKIP
PR128
0_6
PC95
1u/16V_6
Change from 5V_DL to 3V_DL.--1121
C562
1000P_4
C585
1000P_4
C605
1000P_4
Add Cap for EMI.--1102
PC155
0.1u/50V_6
PD15
1PS302
PC156
0.1u/50V_6
PC149
0.1u/50V_6
PD14
1PS302
PR184
22_8
+15V
+15V_ALWP
PC151
0.1u/50V_6
PR188
*200K_4
PR187
*39K_4
PR186 *0_6
REFIN2
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.1867A
Iocp=8-(4.1867/2)=5.9067A
Vth=5.9067A*15mOhm=88.6mV
R(Ilim)=(88.6mV*10)/5uA
~177.2K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.76A
Vth=6.76A*15mOhm=101.4mV
R(Ilim)=(101.4mV*10)/5uA
~202.8K
PR116
*10K/F_6
PR117
0_6
DDPWRGD_R
SYS_HWPG 25
PQ16
FDC653N_NL
SUSD
+3VSUS
PQ15
FDC653N_NL
S5D
+3V_S5
PQ33
FDS8884
MAIND
+5V
PQ14
FDS8878
+3V
VIN
+3V_S5
+15V
PR93
1M_6
PR87
22_8
PR95
1M_6
S5D
25,32 S5_ON
PR86
1M_6
PQ11
DTC144EU
PQ10
DMN601K-7
PQ13
DMN601K-7
Quanta Computer Inc.
PROJECT : ZY7
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SYSTEM 5V/3V (ISL6237)
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

add it.--1023

Pin 49 is GND Pin

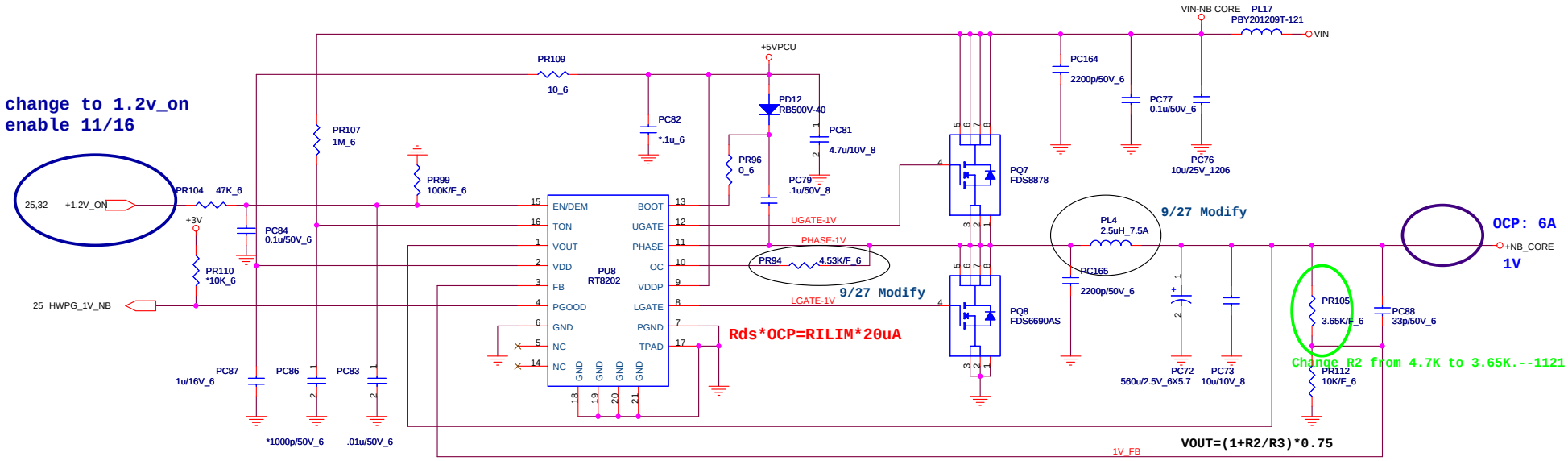
REV B:Add PC172,PC173 for ISL request --0226

Close to CPU socket

Parallel

Close to CPU socket

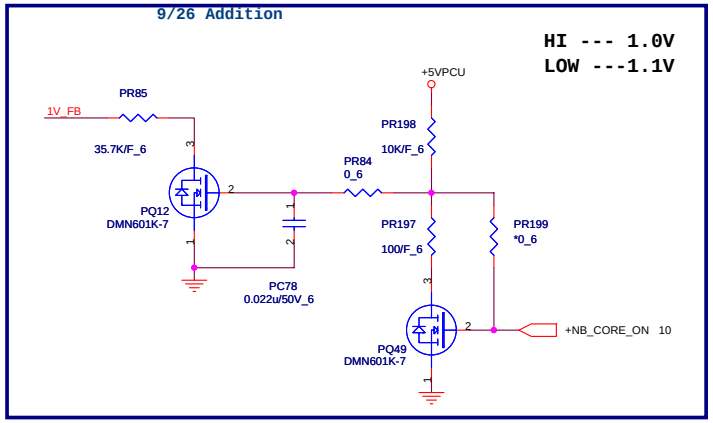
Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: AMD Gfiffin (ISL6265) | Rev 1A
Date: Thursday, June 26, 2008 | Sheet 29 of 35



TON=3.85p*RTON*Vout/(Vin-0.5)

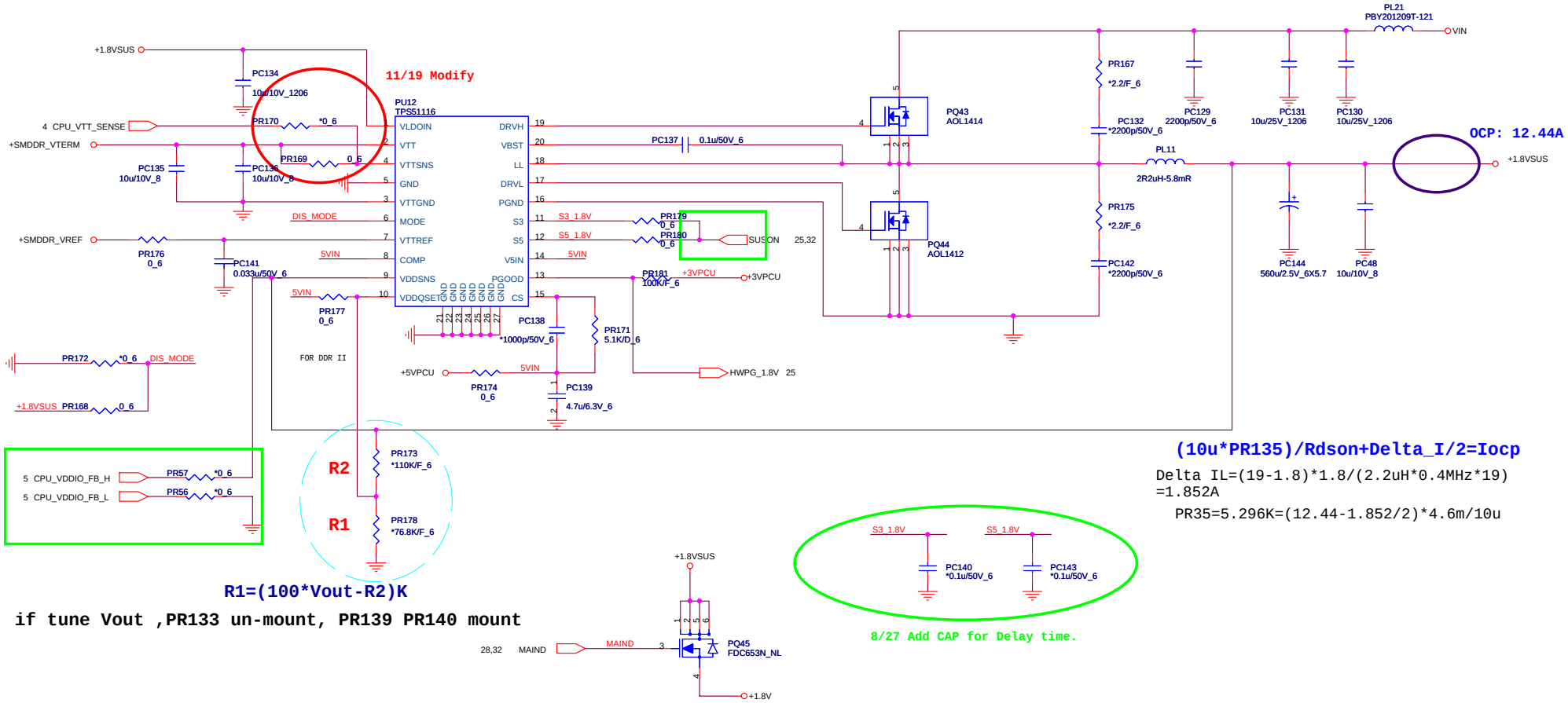
Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm



Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	NB_CORE(RT8202)	1A
Date: Thursday, June 26, 2008	Sheet 30 of 35	



(10u*PR135)/Rdson+Delta_I/2=Iocp

Delta IL=(19-1.8)*1.8/(2.2uH*0.4MHz*19)
=1.852A

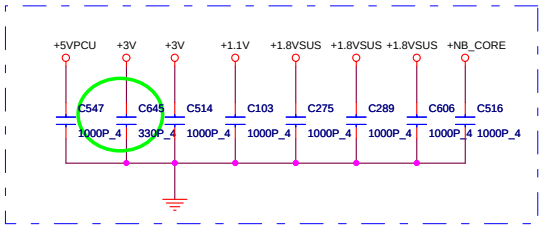
PR35=5.296K=(12.44-1.852/2)*4.6m/10u

R1=(100*Vout-R2)K

if tune Vout ,PR133 un-mount, PR139 PR140 mount

8/27 Add CAP for Delay time.

C REV: change to 330PF for EMI request



Add Cap for EMI.--1112

Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: DDR 1.8V(TPS51116)	Rev 1A
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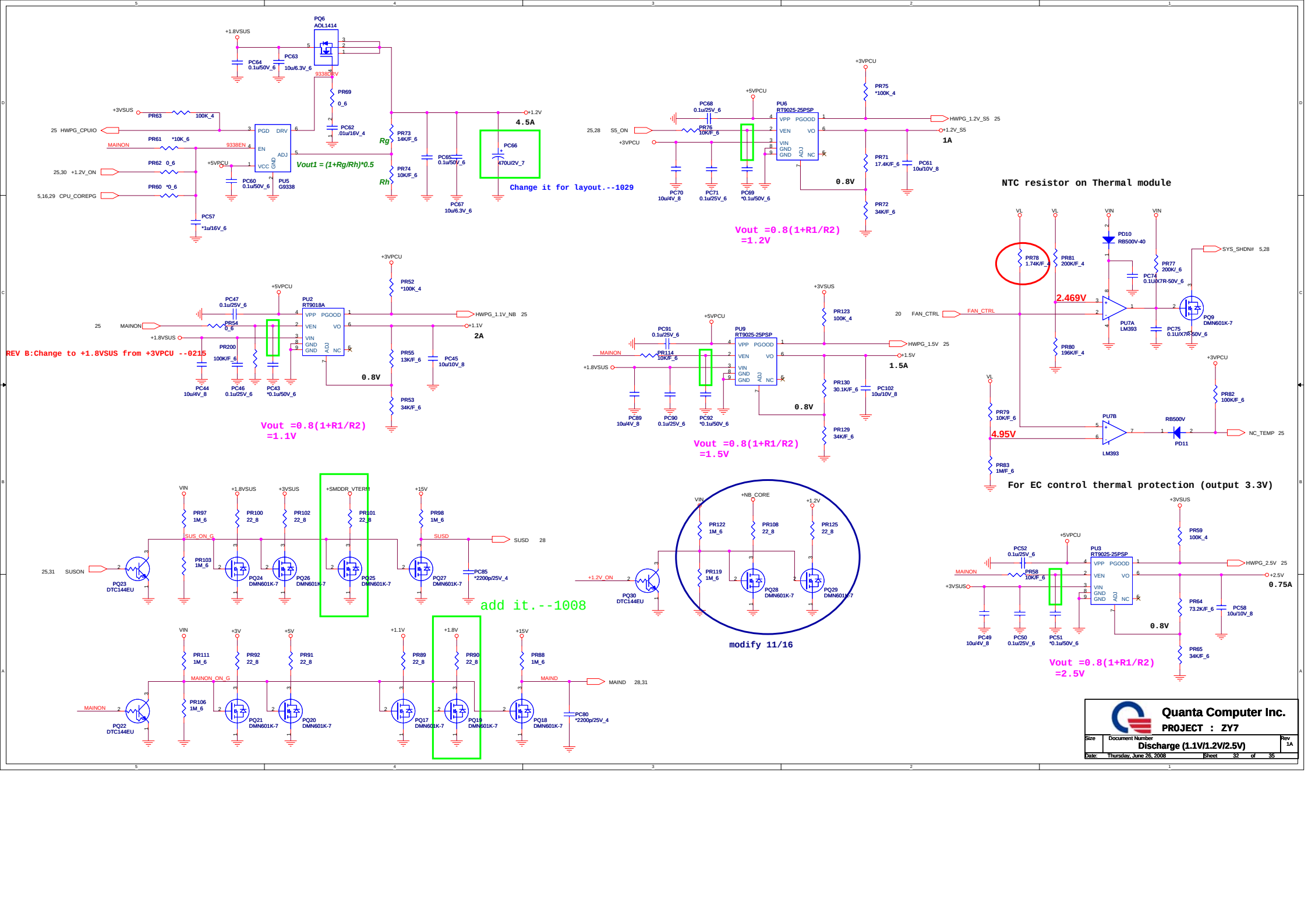
PQ6 AOL1414
+1.8VSUS
PC64 0.1u/50V_6
PC63 10u/6.3V_6
9338DEN
PR69 0_6
+3VSUS
PR63 100K_4
25 HWPG_CPUIO
MAINON
PR61 *10K_6
9338EN
PR62 0_6
25,30 +1.2V_ON
+5VPCU
PR60 *0_6
5,16,29 CPU_COREPG
PC57 *1u/16V_6
PC62 .01u/16V_4
PR73 14K/F_6
Rg
PR74 10K/F_6
Rh
PC65 0.1u/50V_6
PC67 10u/6.3V_6
PC66 470U/2V_7
+1.2V
4.5A
PU5 G9338
PGD DRV EN ADJ VCC GND
Vout1 = (1+Rg/Rh)*0.5
Change it for layout.--1029
+3VPCU
PR75 *100K_4
+5VPCU
PC68 0.1u/25V_6
25,28 S5_ON
PR76 10K/F_6
PU6 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
HWPG_1.2V_S5 25
+1.2V_S5
1A
PR71 17.4K/F_6
PC61 10u/10V_8
0.8V
PR72 34K/F_6
PC70 10u/4V_8
PC71 0.1u/25V_6
PC69 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=1.2V
NTC resistor on Thermal module
+3VPCU
PR52 *100K_4
+5VPCU
PC47 0.1u/25V_6
PU2 RT9018A
VPP PGOOD VEN VO VIN GND GND ADJ NC
HWPG_1.1V_NB 25
25 MAINON
PR54 0_6
+1.8VSUS
+1.1V
2A
REV B:Change to +1.8VSUS from +3VPCU --0215
PR200 100K/F_6
PR55 13K/F_6
PC45 10u/10V_8
0.8V
PR53 34K/F_6
PC44 10u/4V_8
PC46 0.1u/25V_6
PC43 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=1.1V
+3VSUS
PR123 100K_4
20 FAN_CTRL
PC91 0.1u/25V_6
PU9 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
HWPG_1.5V 25
MAINON
PR114 10K/F_6
+1.8VSUS
+1.5V
1.5A
0.8V
PR130 30.1K/F_6
PC102 10u/10V_8
PR129 34K/F_6
PC89 10u/4V_8
PC90 0.1u/25V_6
PC92 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=1.5V
VL
VIN
PR78 1.74K/F_4
PR81 200K/F_4
PD10 RB500V-40
PR77 200K/_6
SYS_SHDN# 5,28
PC74 0.1U/X7R-50V_6
2.469V
PU7A LM393
PC75 0.1U/X7R-50V_6
PQ9 DMN601K-7
PR80 196K/F_4
FAN_CTRL
+3VPCU
PR82 100K/F_6
PR79 10K/F_6
PU7B
RB500V
4.95V
NC_TEMP 25
LM393
PD11
PR83 1M/F_6
For EC control thermal protection (output 3.3V)
VIN
+1.8VSUS
+3VSUS
+SMDDR_VTERM
+15V
PR97 1M_6
PR100 22_8
PR102 22_8
PR101 22_8
PR98 1M_6
SUS_ON_G
SUSD
SUSD 28
25,31 SUSON
PR103 1M_6
PQ23 DTC144EU
PQ24 DMN601K-7
PQ26 DMN601K-7
PQ25 DMN601K-7
PQ27 DMN601K-7
PC85 *2200p/25V_4
add it.--1008
+1.2V_ON
PQ30 DTC144EU
+NB_CORE
+1.2V
PR122 1M_6
PR108 22_8
PR125 22_8
PR119 1M_6
PQ28 DMN601K-7
PQ29 DMN601K-7
modify 11/16
+3VSUS
PR59 100K_4
+5VPCU
PC52 0.1u/25V_6
PU3 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
HWPG_2.5V 25
MAINON
PR58 10K/F_6
+3VSUS
+2.5V
0.75A
PR64 73.2K/F_6
PC58 10u/10V_8
0.8V
PC49 10u/4V_8
PC50 0.1u/25V_6
PC51 *0.1u/50V_6
PR65 34K/F_6
Vout =0.8(1+R1/R2)
=2.5V
VIN
+3V
+5V
+1.1V
+1.8V
+15V
PR111 1M_6
PR92 22_8
PR91 22_8
PR89 22_8
PR90 22_8
PR88 1M_6
MAINON_ON_G
MAIND
MAIND 28,31
MAINON
PR106 1M_6
PQ22 DTC144EU
PQ21 DMN601K-7
PQ20 DMN601K-7
PQ17 DMN601K-7
PQ19 DMN601K-7
PQ18 DMN601K-7
PC80 *2200p/25V_4
Quanta Computer Inc.
PROJECT : ZY7
Size
Document Number
Discharge (1.1V/1.2V/2.5V)
Rev 1A
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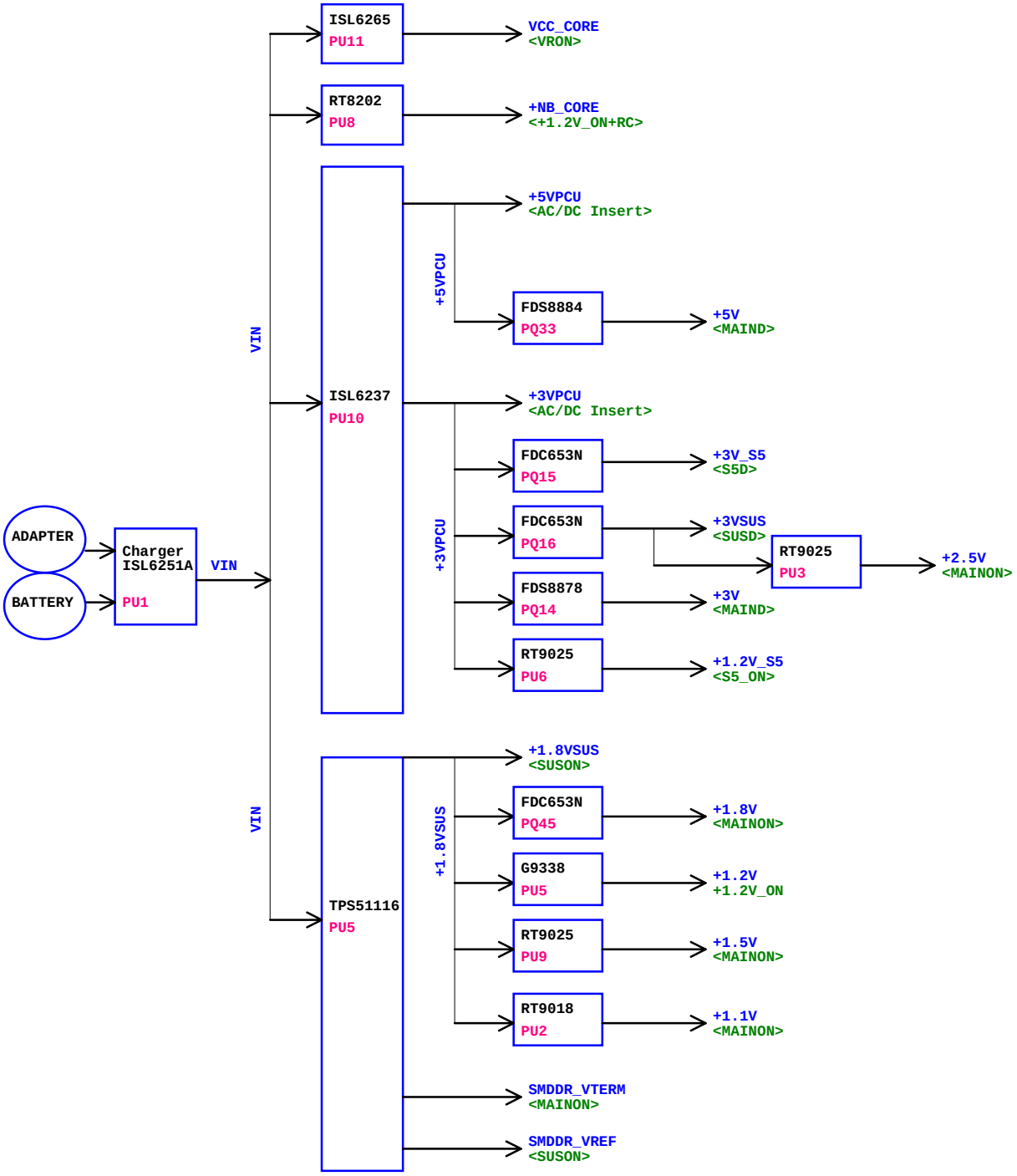

Quanta Computer Inc.
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Size	Document Number	Rev
	Power Tree	1A

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CHANGE LIST

Model	REV	CHANGE LIST	MODEL	ZY7 FROM	ZY7 To
ZY7 MB	1A	1A First release--0107		X	1A
	2B	Page 02 change C350 from unstuff to 22P for EMI request--0215 Page 03 Add HOLE39 for ME request--0215 Page 06 Del C193, C203, C178 and C184,C185 for ISL6265 request--0226 Page 29 PC172,PC173 for ISL6265 request--0226 Page 09 Add HDMI CAP circuit for layout request --0216 page 10 Add C601,C646,C647,C648 100PF for EMI request--0201 Page 10 Change R149 value from 150ohm to 140 ohm following AMD change---0214 Page 10 Change +3V_AVDD_NB PU from +3V_S5 to +3V follow AMD CRB suggest.--0201 Page 16 Add C641 1N Capacitor to Smoothing NB_PWRGD_IN ---0202 Page 16 Change U7,R179 unstuff,PR183 stuff,follow A1-2chip .--0202 Page 17 Del MXM_POWEREN circuit follow AMD request--0214 Page 18 Change R393 value from 150ohm to 140 ohm following AMD change---0214 Page 19 Add L79,L80 for EMI request--0218 Page 19 add reseve D34,D35,D37,D38 for ESD request--0218 Page 21 SWAP TX0P/N with TX3P/N net for LAN layout issue--0214 Page 21 change R39 Value from 1.24K to 1.2K and sutff R63 for LAN issue--0215 Page 22 del VR button function follow Spec--0218 Page 28 add reverse PR203 ---0218 page 32 PU2 Power source change to +1.8VSUS from +3VPCU--0128		1A	2A
	2C	page 18 add R617,R616,R618,R619 for HDMI vendor suggest--0331 page 21 SWAP CN12 LAN_LINKLED#_SYS and LAN_ACTLED#_SYS net for LAN LED issue---0331 page 22 change u36 footprint---0331 page 22 del SPDF circuit, C684, R561,Q52 cancel, U34 cancel----0331 page 10 unstuff Q50 and R452,stuff R459 follow AMD suggest---0402 page 19 add R198 and R207(reserve) for FP S3 issue---0408 Page 31 change C645 from 1000P to 330P for EMI issue---0408 Page 16 add C684, C696 330PF for EMI issue---0408 Page 12 add C178 10PF for EMI issue ---0408 Page 26 change R35 to 1K for Docking AC issue---0408 Page 18 unstuff R3, Q1,Q4,Q5, Add and stuff D17, D21---0410		2A	2B
	2D			2B	3A

DOC NO.	PROJECT MODEL :	ZY7	APPROVED BY:		DATE:	2008/01/07
	PART NUMBER:		DRAWING BY:		REVISON:	3A

Title	<Title>		
Size: Custom	Document Number: <Doc>		Rev: <RevCode>
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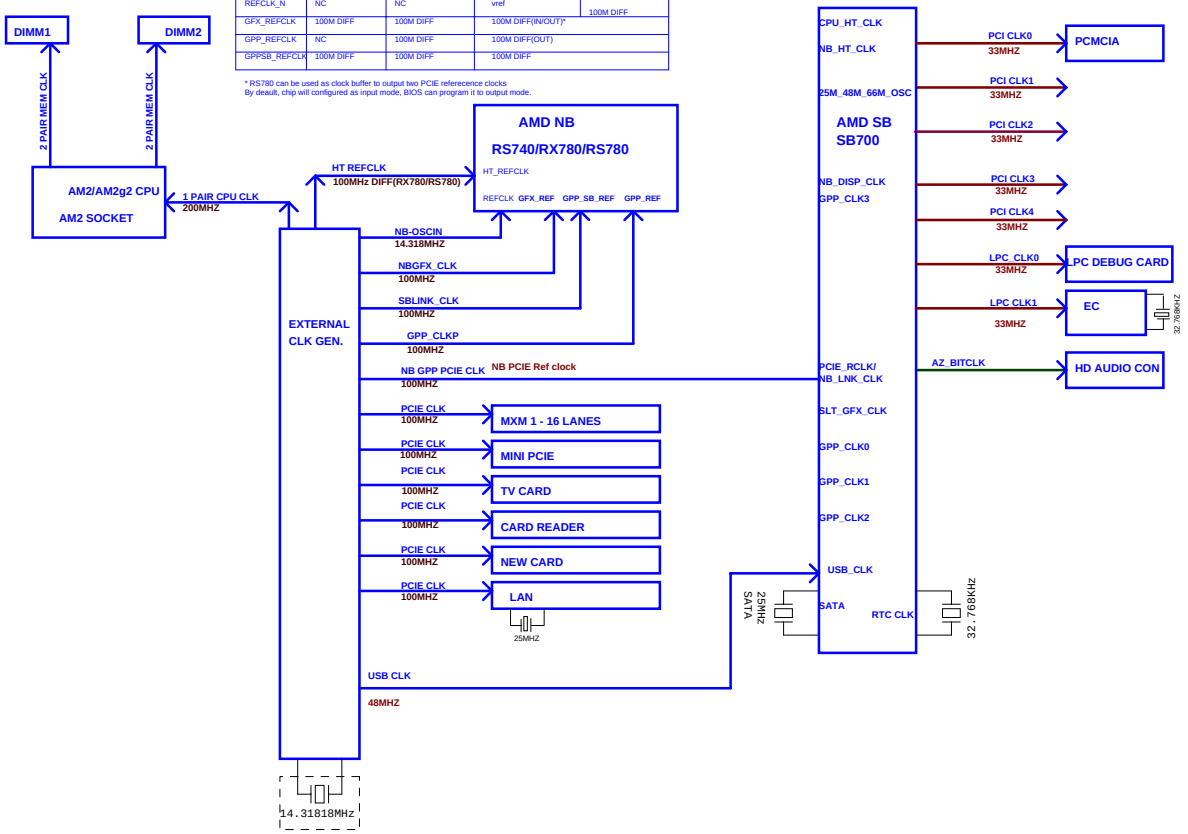
NB CLOCK INPUT TABLE

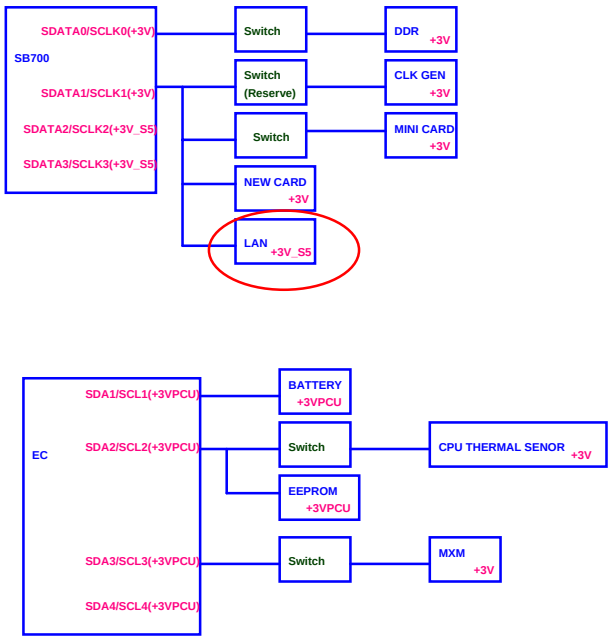
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refereence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

Clock distribution



SMBUS Table



Quanta Computer Inc.
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	Clock/SMBUS	A

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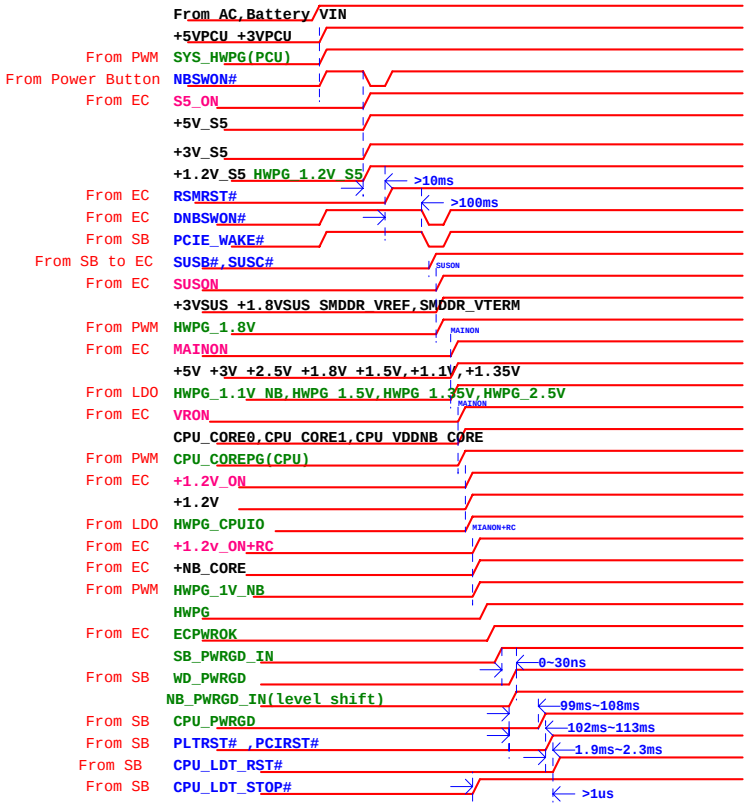
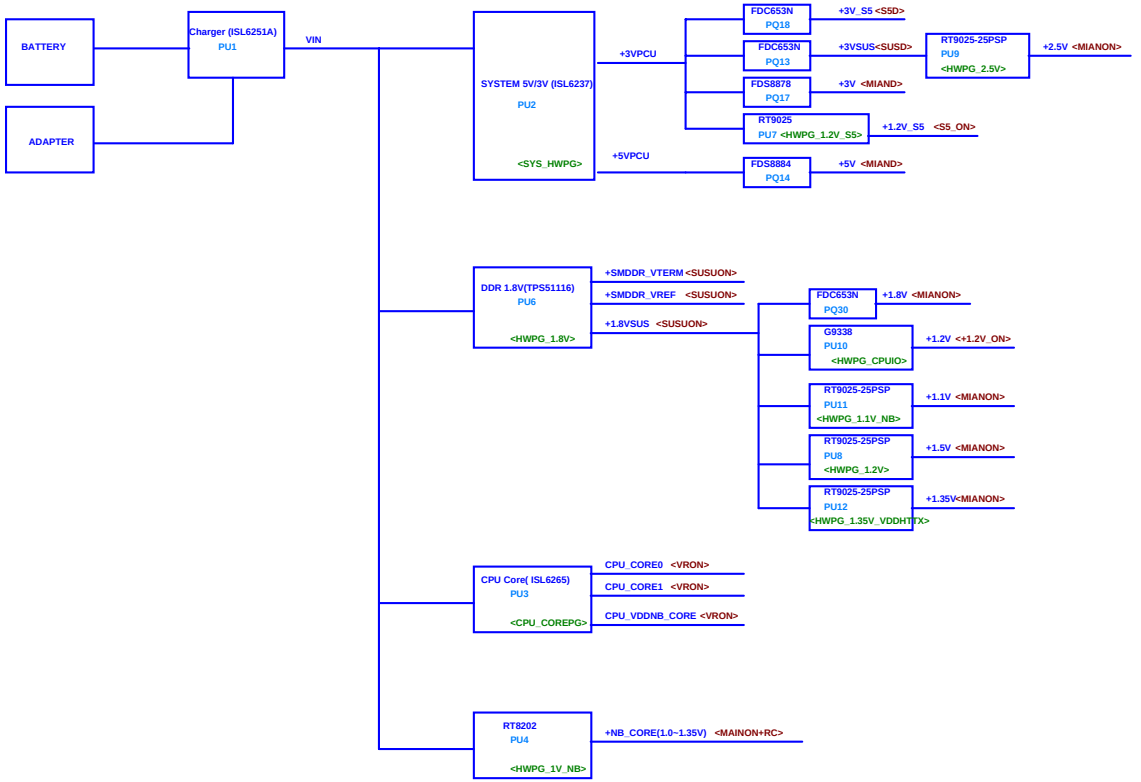
ZY7 Power On Sequence



Power State / Voltage Rail Activity Summary

SYSTEM STATE	SLEEP STATE	PROCESSOR STATE	Description		RTC	ALWAYS	S5	SUS	RUN
G0	S0	C0	RUNNING		ON	ON	ON	ON	ON
G0	S0	C0	RUNNING	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1		HALT	ON	ON	ON	ON	ON
G0	S0	C2		Stop grant,caches snoopable	ON	ON	ON	ON	ON
G0	S0	C1E/C3		Stop grant, no LDTSTOP,not expected,cache snoops	ON	ON	ON	ON	ON
G0	S0	C1E/C3		Stop grant with LDTSTOP, cache not snoopable	ON	ON	ON	ON	ON
G1	S1	OFF	SLEEPING	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF		Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF		Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	SOFT OFF		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	POWER BUTTON ONLY		ON	ON	OFF	OFF	OFF
G3		OFF	MECHANICAL OFF		ON	OFF	OFF	OFF	OFF



POWER	Distribution
VCC_CORE	CPU
+5VPCU	FINGERPRINT
+3VPCU	CIR,EC,SW/B,SUSLED,PWR LED,BAT LED,SPI FLASH
+1.1V	RS780
+NB_CORE	RS780
+5V	CRT,HDMI,DOCK,PCMCIA,AUDIO,HDD,ODD,FAN,TP,TV CARD,SB700,MXM
+3V	CPU,CLK GEN,SB700,RS780,MXM,DDR,DOCK,EC,CARD READER,PCMCIA,CODEC,LAN,HDD,NEW CARD,MINI CARD,LCD,CM2009,HDMI,CAMERA,CODEC,HEADPHONE,AMP
+3V_S5	DOCK,MDC,LAN,NEW CARD
+3VSUS	SUSLED,BT
+2.5V	CPU,MXM
+1.2V_S5	SB700
+1.8VSUS	CPU,SB700
+1.8V	CARD READER,RS780,SB700
+1.2V	SB600 , RS780 , CPU , CLK GEN
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+1.5V	NEW CARD,MINI CARD
+5V_S5	

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