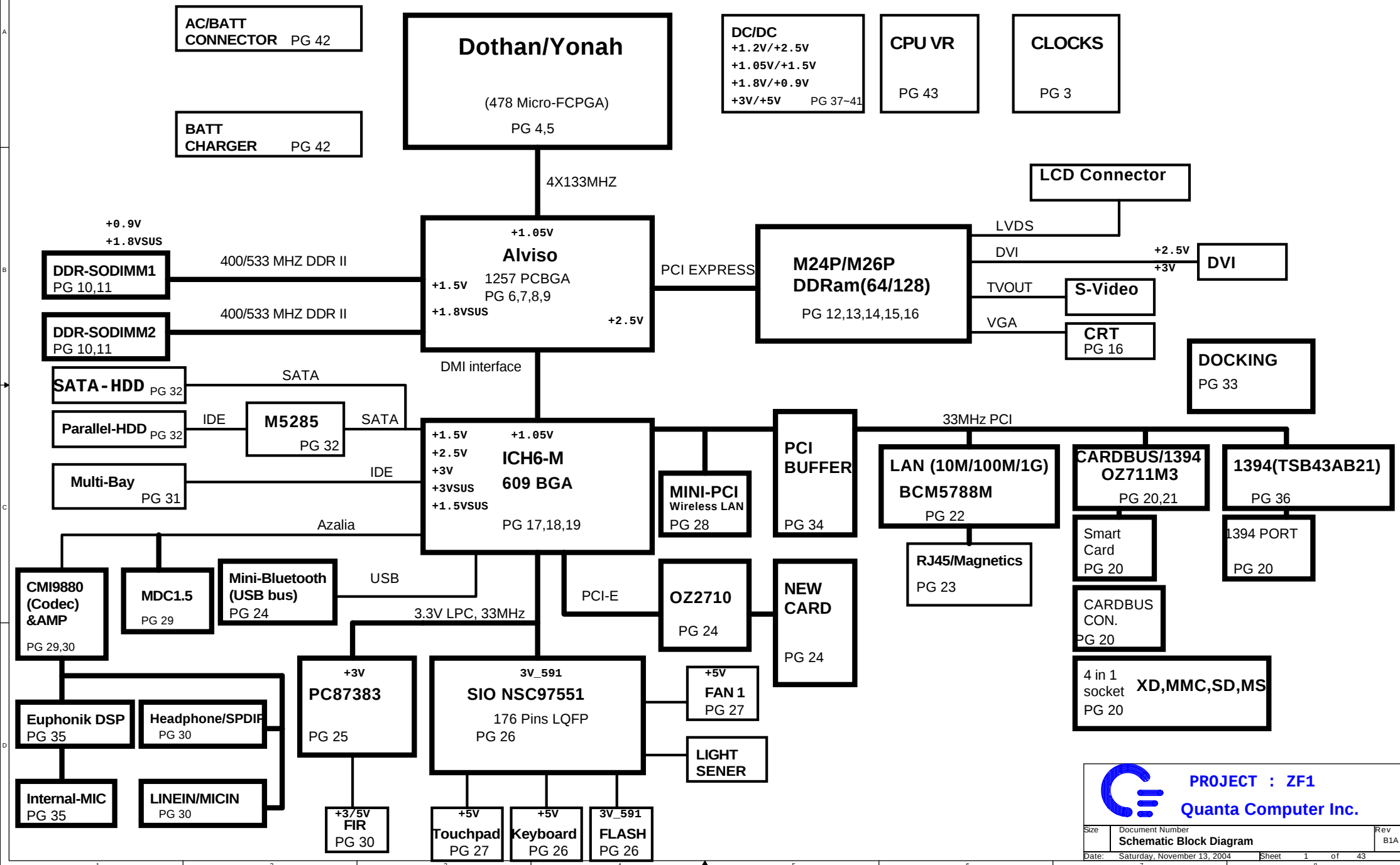


ZF1



PROJECT : ZF1
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Check again

Change History

Voltage Rails		ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT		X	X	X	X	
3V 591		X	X	X	X	
5VPCU		X	X	X	X	
+3V S5		X	X	X	X	S5 ON
3V LAN		X	X	X	X	
+1.5V S5		X	X	X	X	S5 ON
+1.8VSUS		X	X			SUS ON
+3VSUS		X	X			SUSD
+5VSUS		X	X			SUSD
SMDDR VTERM	DDR Termination voltage	X	X			MAINON
SMDDR VREF		X				MAINON
VGA PCIE 1.2V		X				MAINON
VCC CORE	Core voltage for Processor	X				VR ON
+VCCP	1.05V rail for Processor I/O	X				MAINON
+1.5V		X				MAINON
+1.8V		X				MAIND
+2.5V		X				MAIND
+3V		X				MAIND
+5V						MAIND
+12V		X				MAINON
+3VRUN		X				PCI Switch Power ON
+5VRUN		X				PCI Switch Power ON

5/28
1.System DVI DET function move in EZ port , So,Del Q47,R557
2.Addition AND gate for DOCKING Power Good AND DockingIN Singal combine Circuit
3.Addition Power led circuit for system
4.Change D34 AND D35 + -
5.Addition LID Switch and LID connector
6.Addition RC Delay for PCIE1.2V
7.Change EC Three GPIO port same to ZL2
5/31
1.Change C145 PCB Footprint to 3528
2.Combine USB and bluetooth connector to 19pin connector 87212-1900
3.Change PCBFootprint 88216-1200 to 88213-1200
4.Change USB connector bypass C to 0805 10u
5.Adujst 80pin connector 3 singal
6/1
1.Update power all circuit for GND name
2.Addition OR to PRST
3.Change IDE RST
6/2
1.Change ICH-6 USB Port
2.Del CDR,CDL,CDGND Singal and DEL prevent CDR,CDL,CDGND noise circuit.
6/4
1.U49,U50, Form 3VRUN change to +3V AND CHANGE MINPCI connector to PCI BUS,And addition PCI SWRST # AND PCI SWRST1#
2.Change BT POWER NAME
3.Change VOIP AGND
6/7
1.Change VOIP AGND TO AGND2 for Layout

External PCI Devices

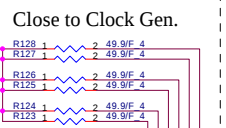
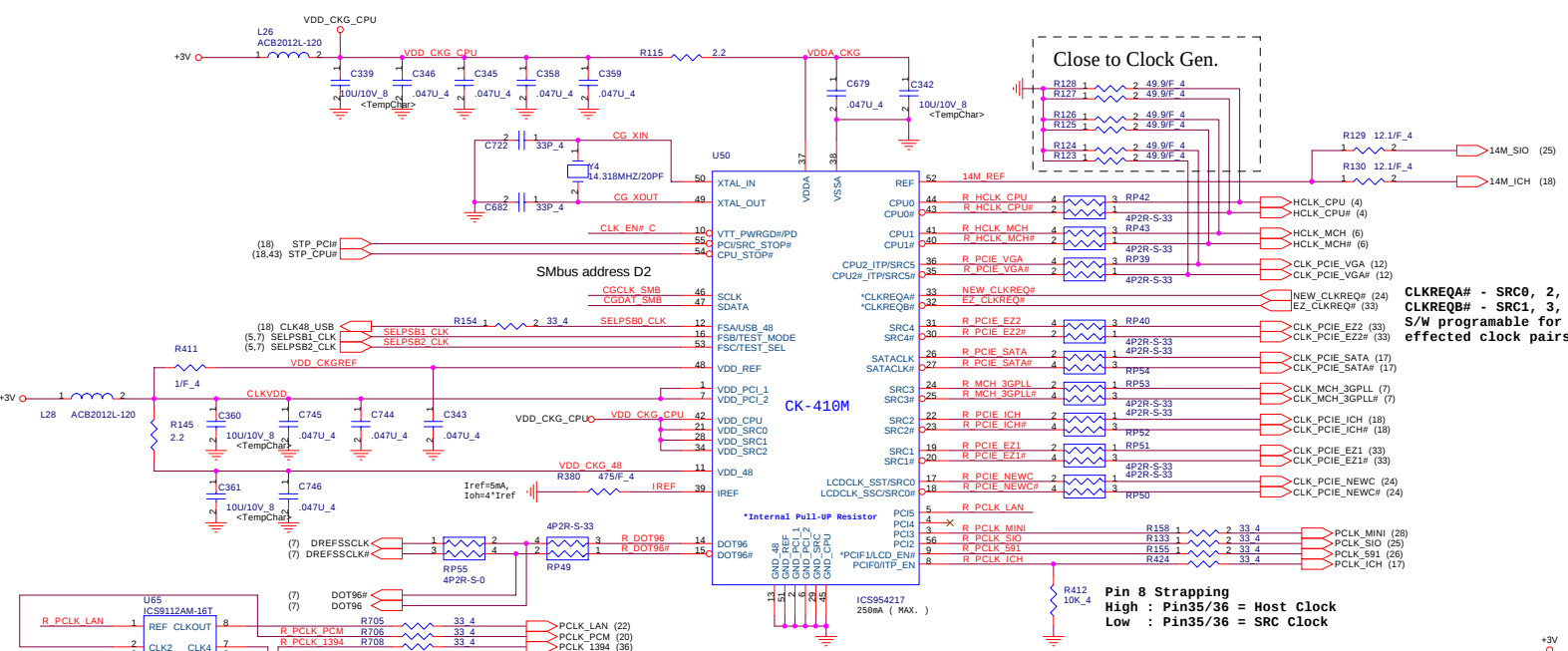
Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+Smart Card	AD25	1	PIRQC/B
Mini-PCI	AD19	2	PIRQB/D
LAN	AD22	0	PIRQA
1394	AD23	3	PIRQD

EC SM Bus1 address

Device
Smart Battery
THERMAL SENSOR
LIGHT SENER
VOIP FLASH ROM

ICH6-M SM Bus address

Device
SODIMM 1010 000X b
Clock Gen 1101 001x b

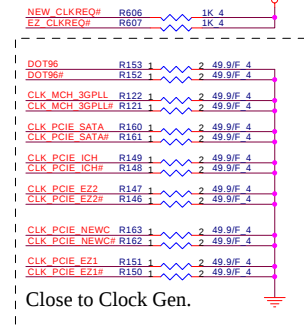
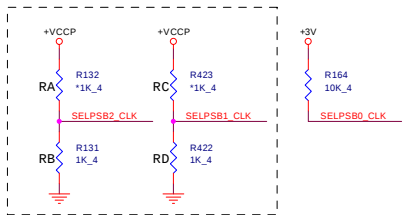


CLKREQA# - SRC0, 2, SATA
 CLKREQB# - SRC1, 3, 4
 S/W programmable for
 effected clock pairs

Pin 8 Strapping
 High : Pin35/36 = Host Clock
 Low : Pin35/36 = SRC Clock

Resistor Stuff Table

	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X



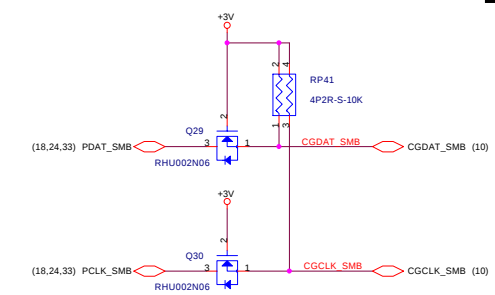
Close to Clock Gen.

Clock Gen. Frequency Selection Table

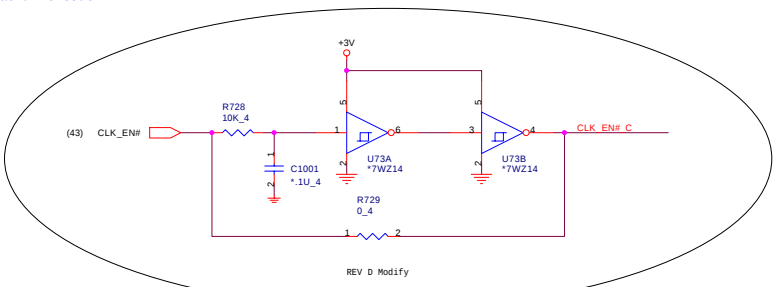
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN BSEL Output Value

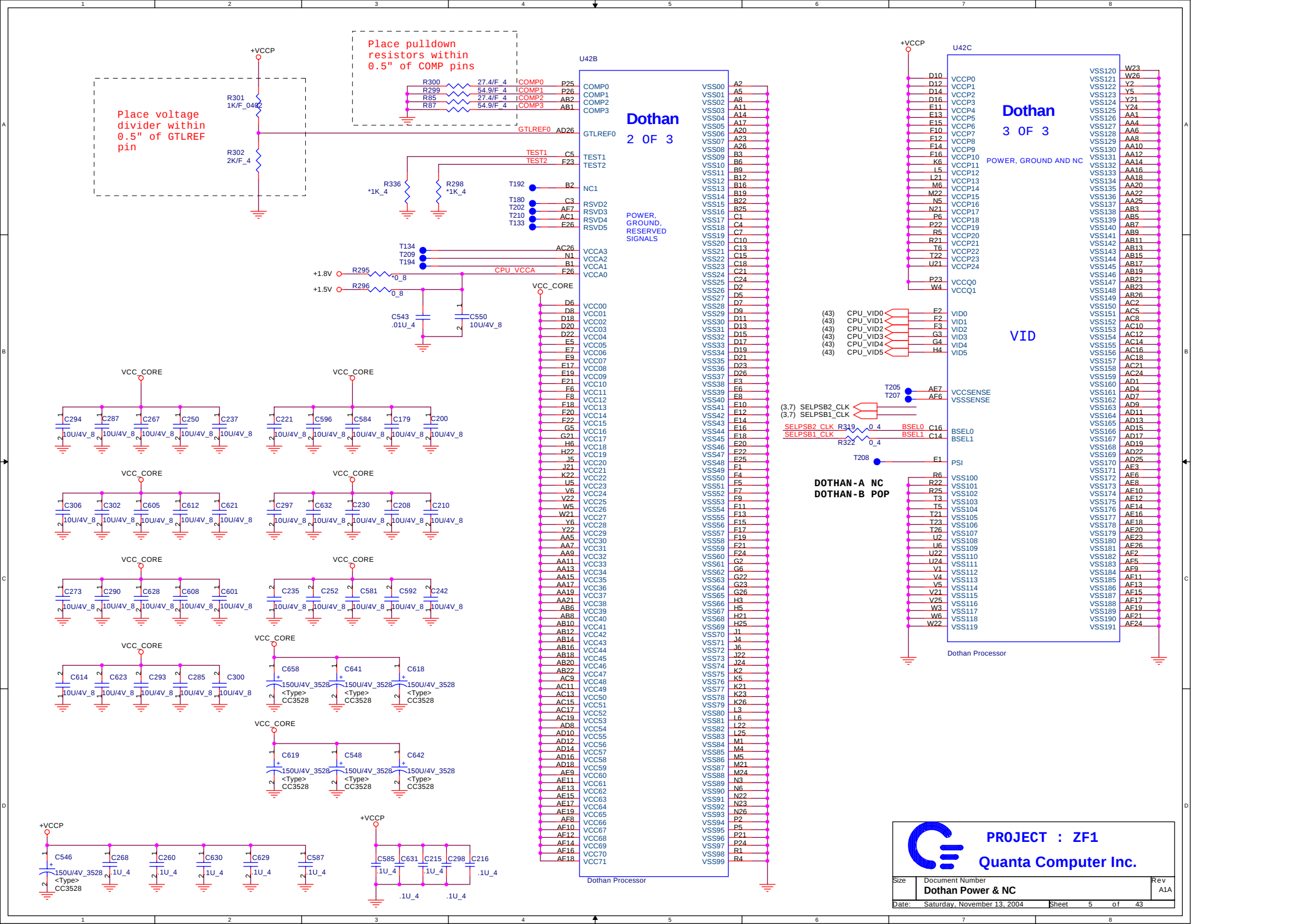
FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

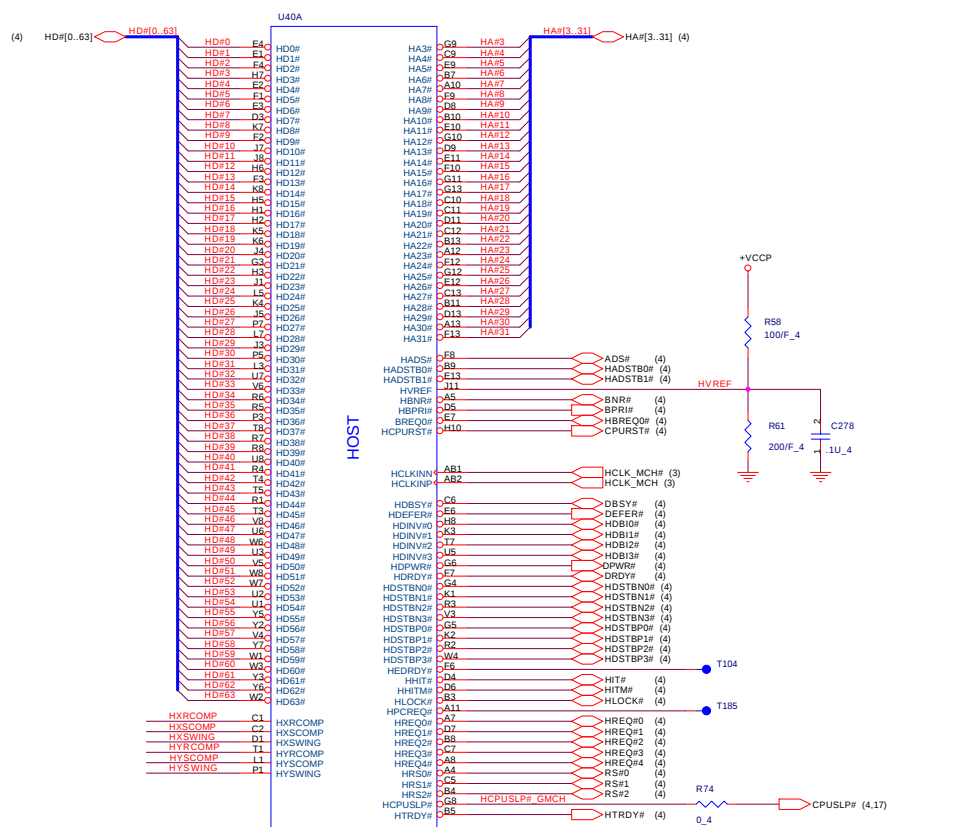
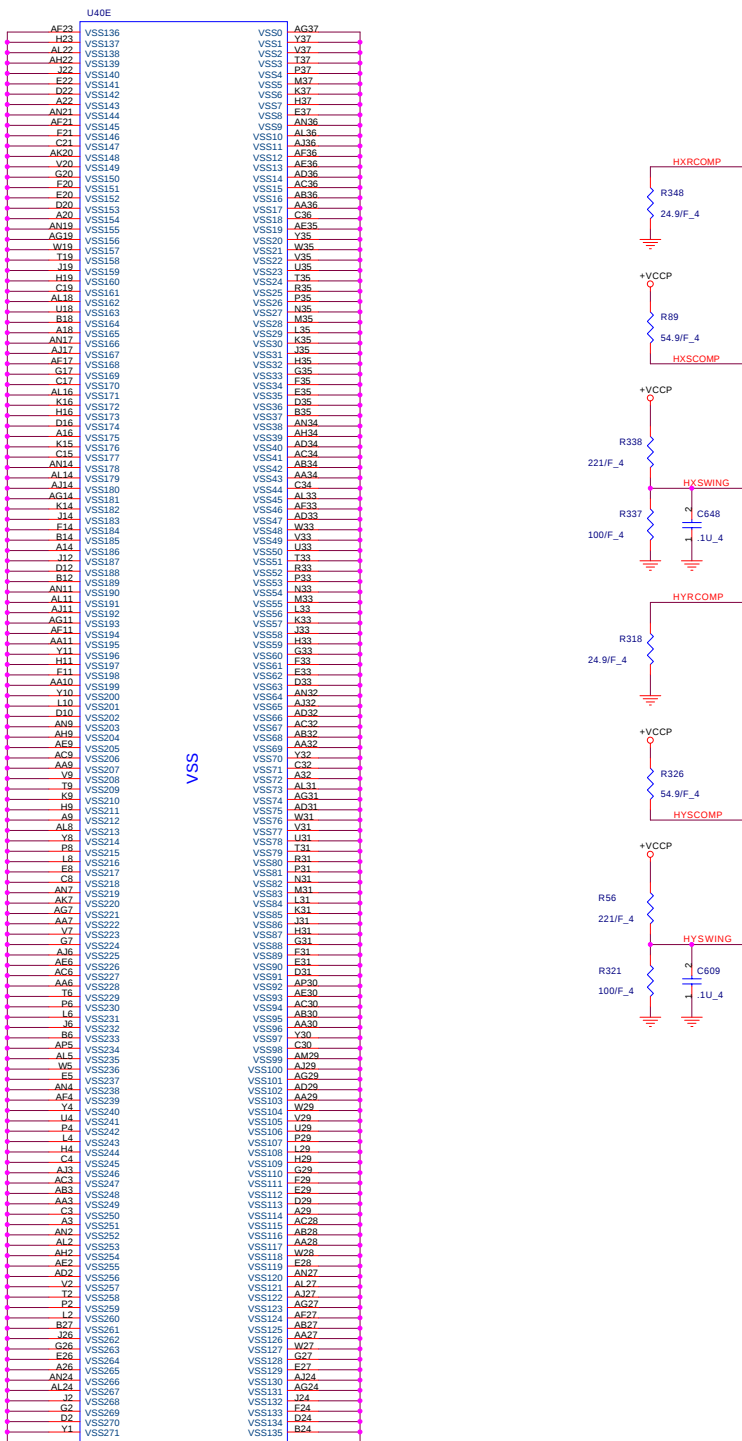


These are for backdrive issue

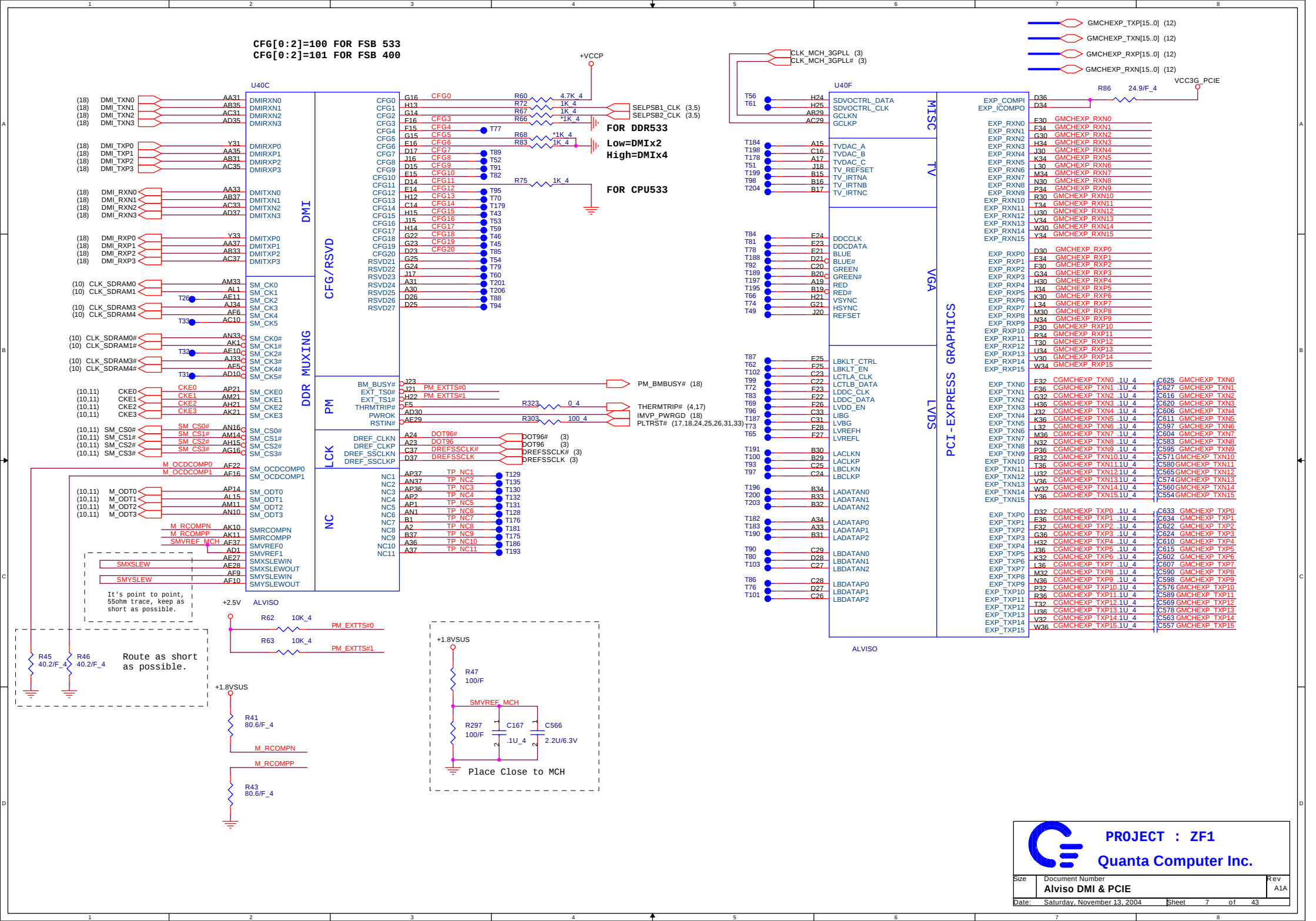


REV D Modify





DO NOT INSTALL FOR DOTHAN-A AND INSTALL FOR DOTHAN-B



(10) R_A_MD[0..63]



ALVISO

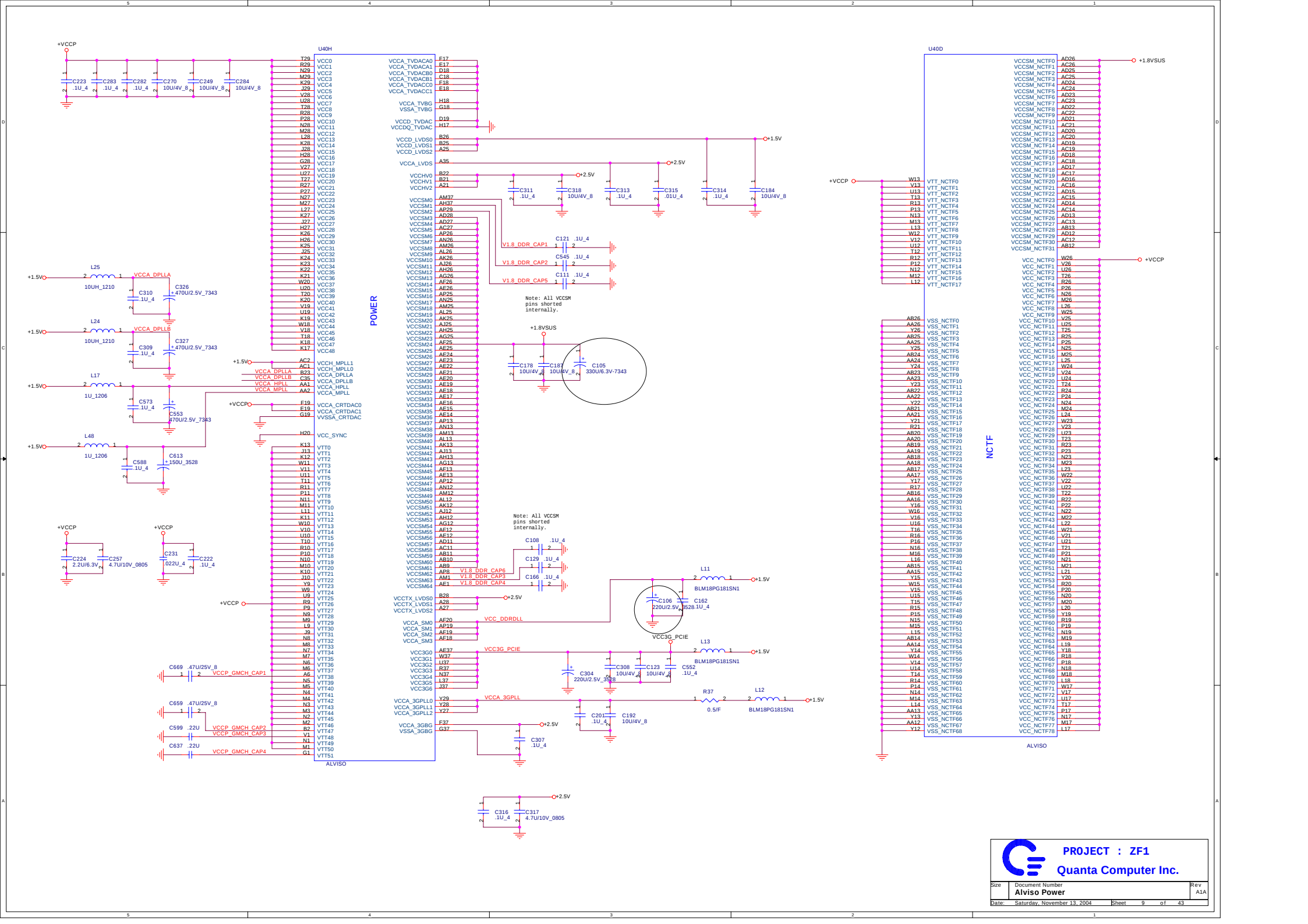
(10) R_B_MD[0..63]

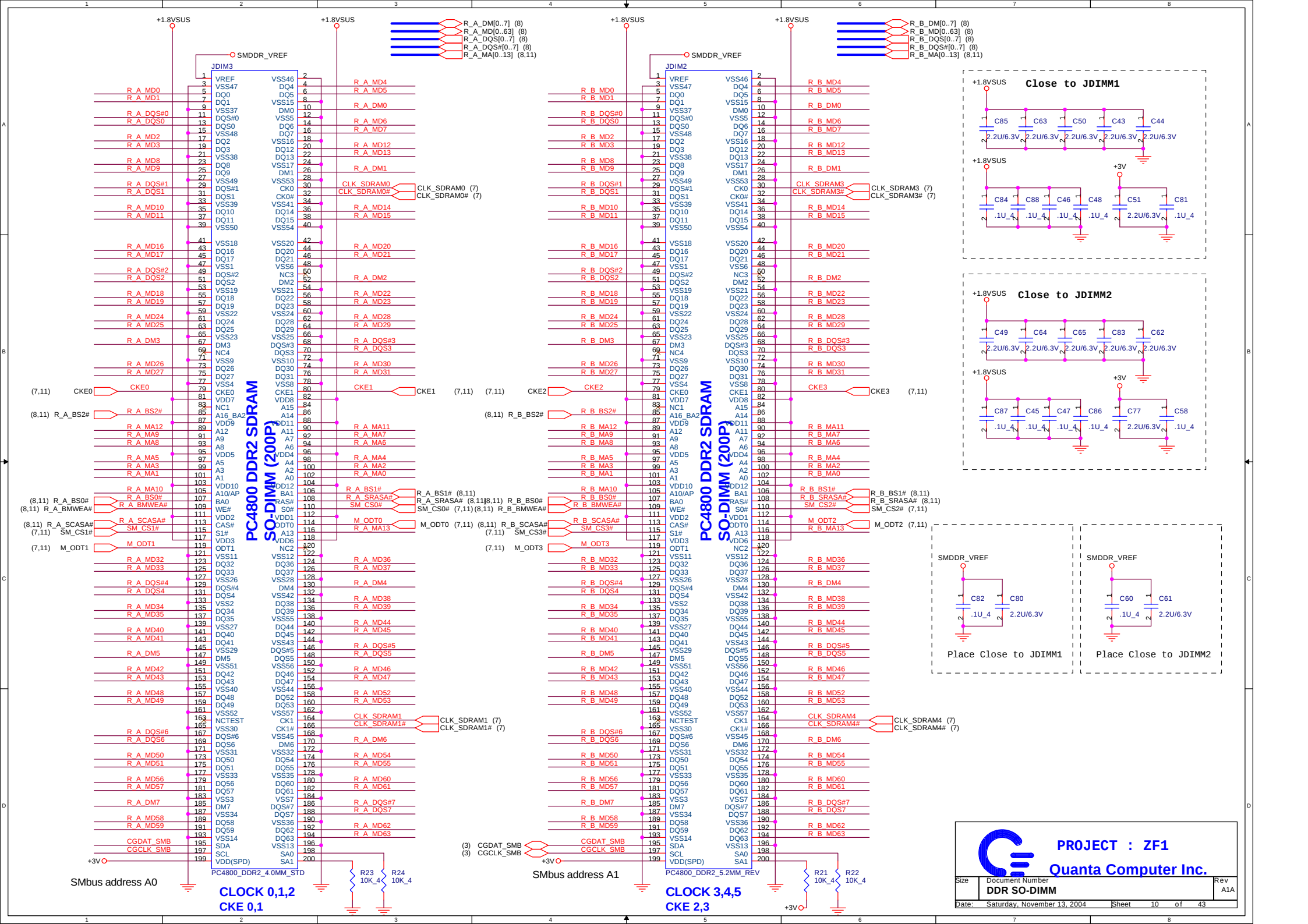


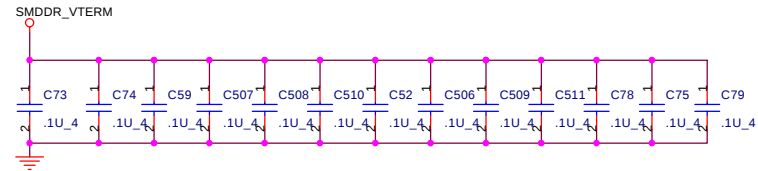
ALVISO



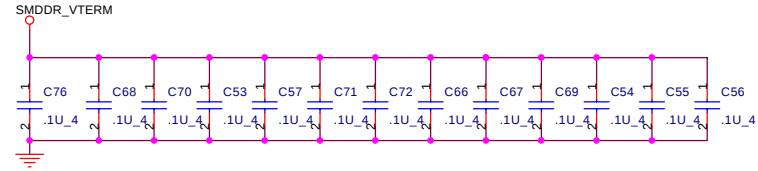
PROJECT : ZF1
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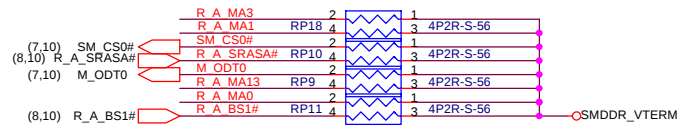
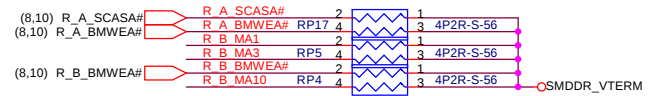
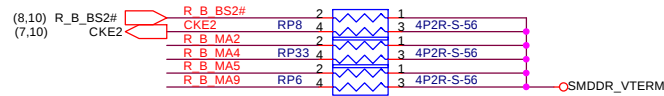
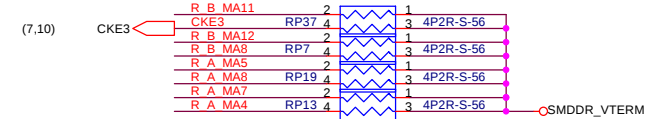
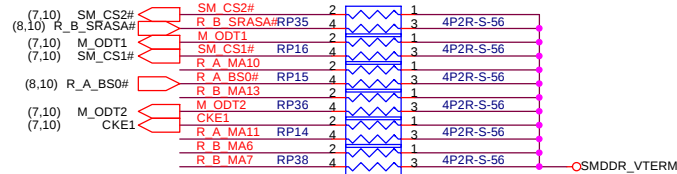
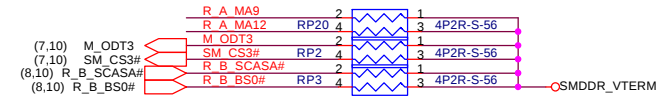
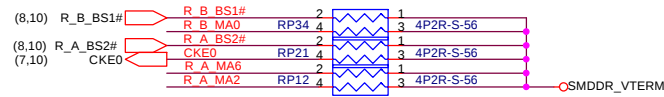
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

R_A_MA[0..13] (8,10)

R_B_MA[0..13] (8,10)

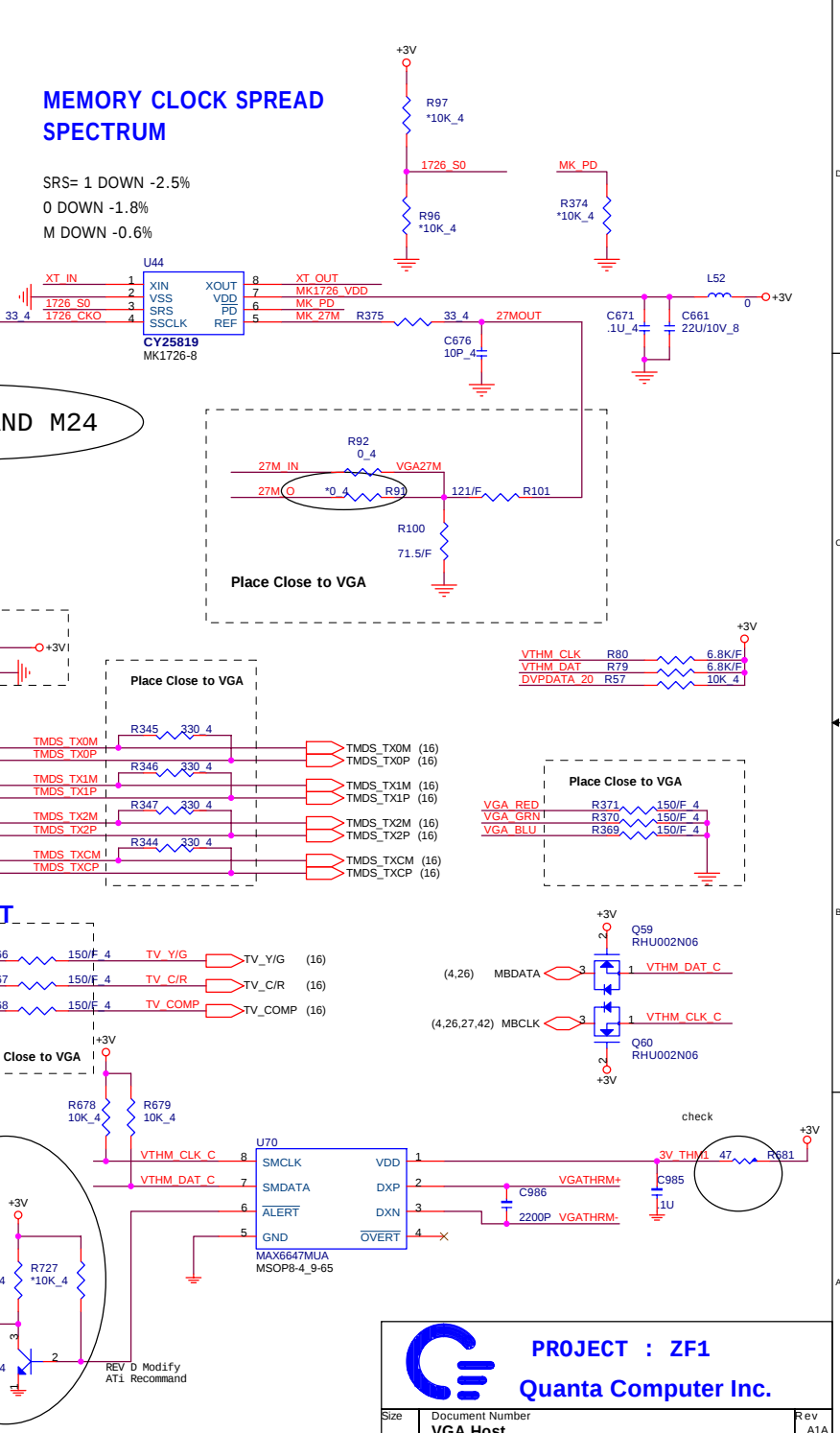
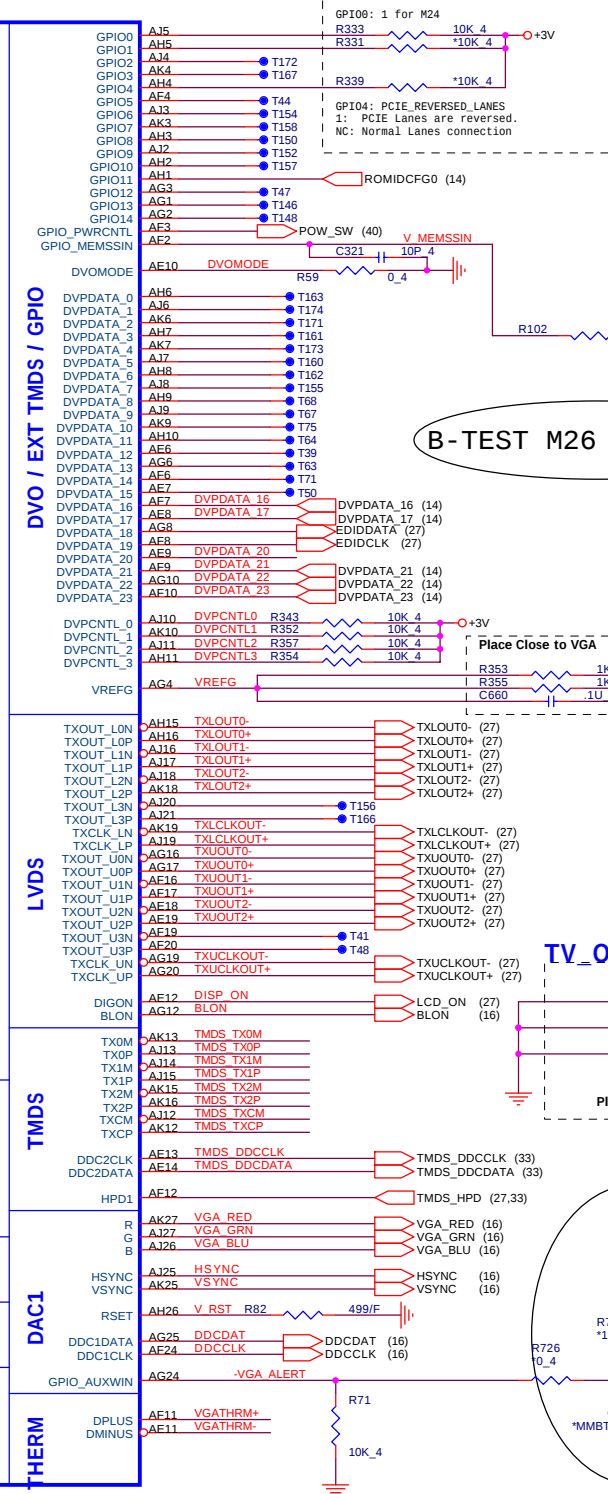
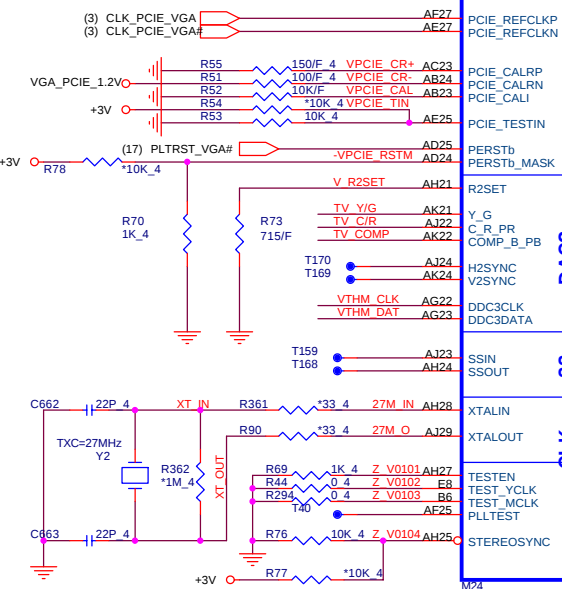
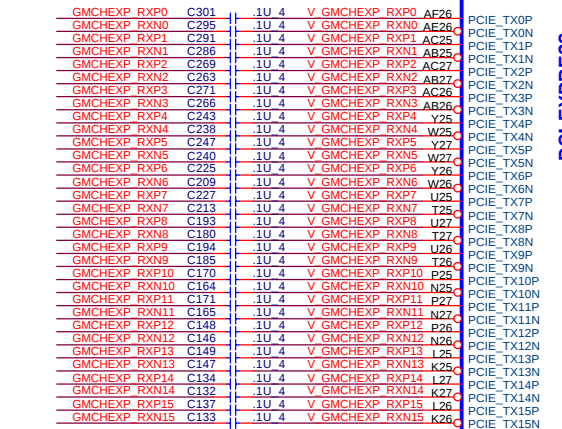


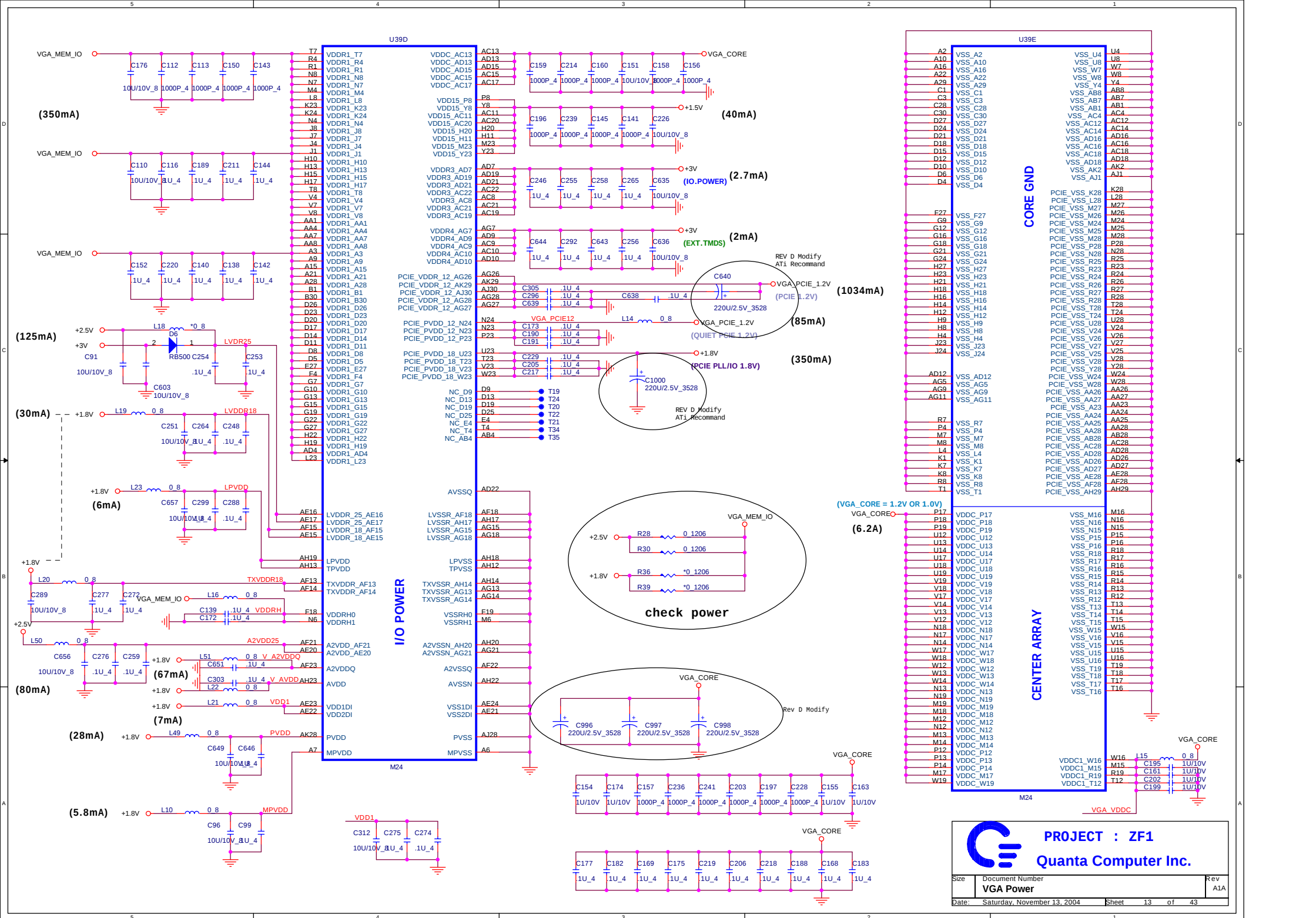


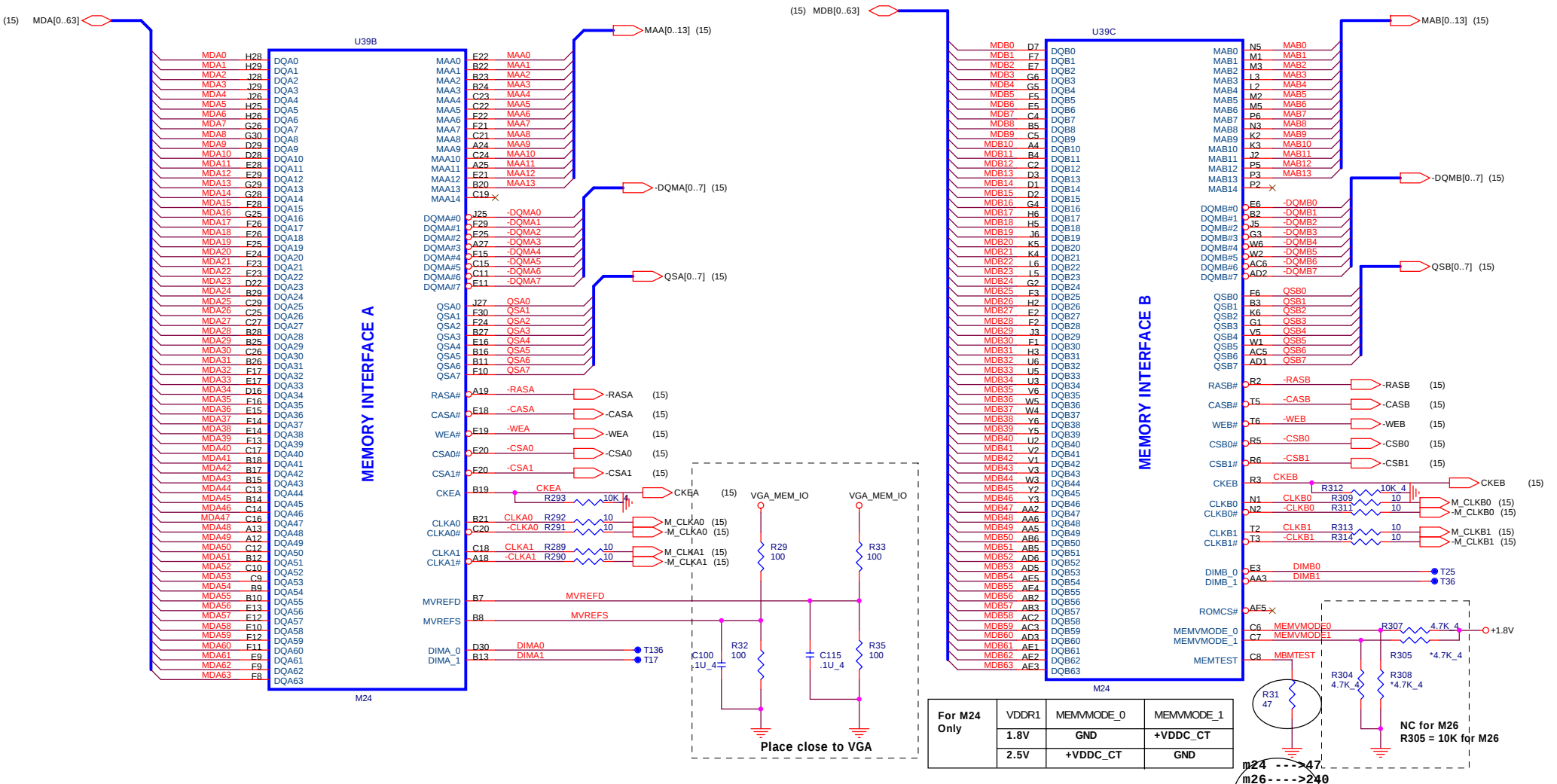
PROJECT : ZF1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR Res. ARRAY	A1A
Date:	Saturday, November 13, 2004	Sheet 11 of 43

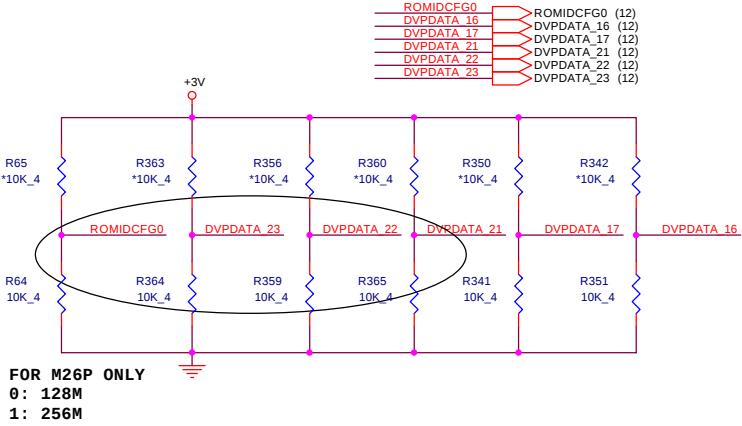






STRAPS PIN

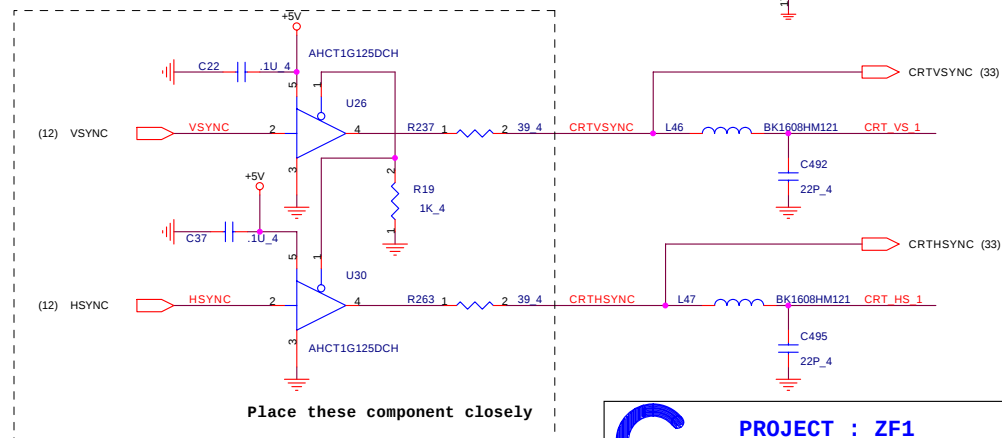
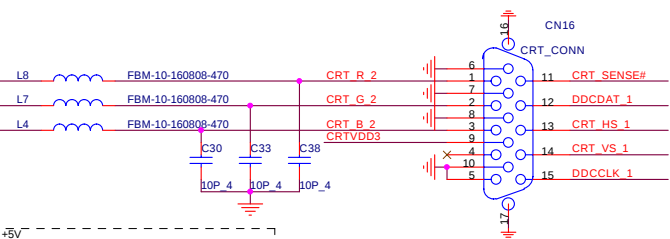
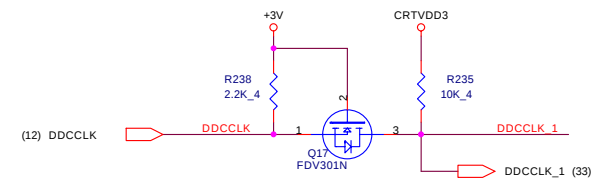
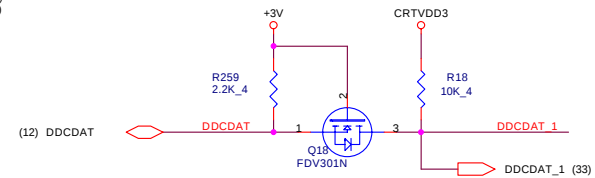
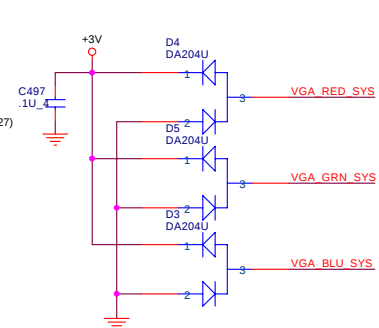
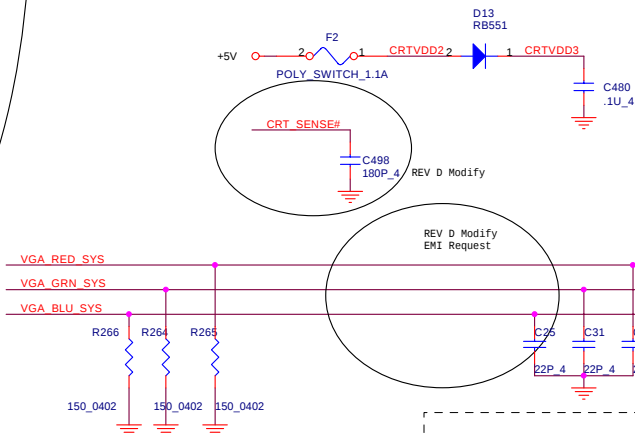
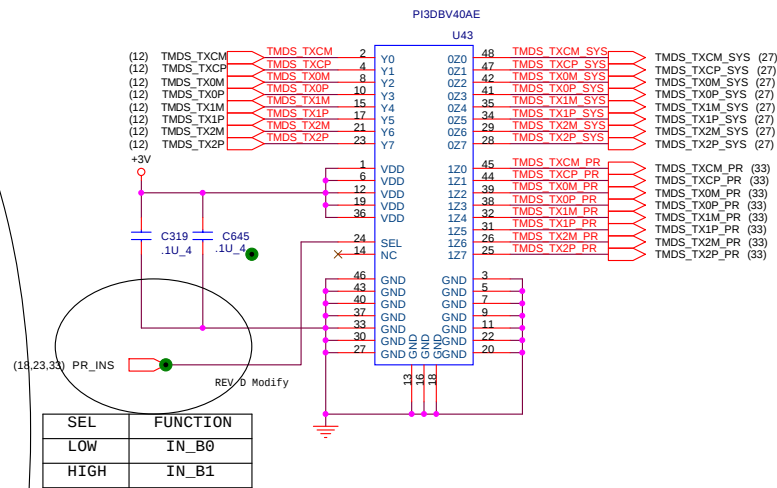
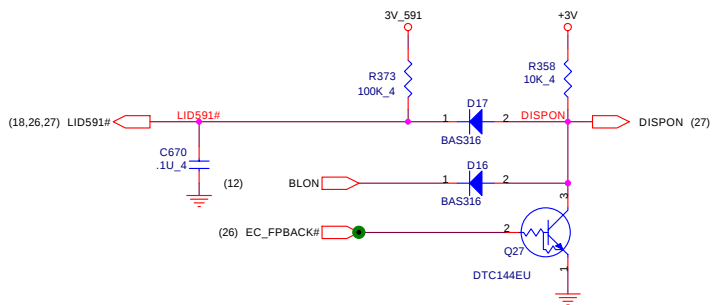
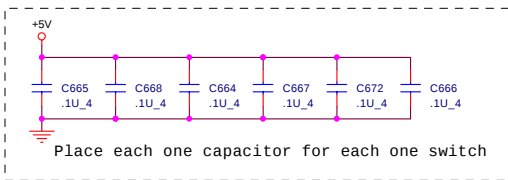
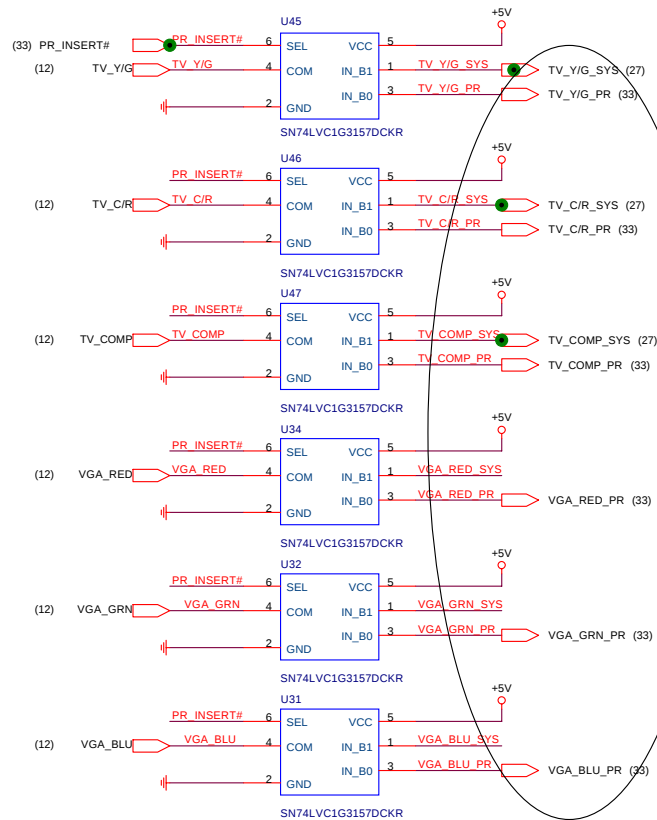
GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21~23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

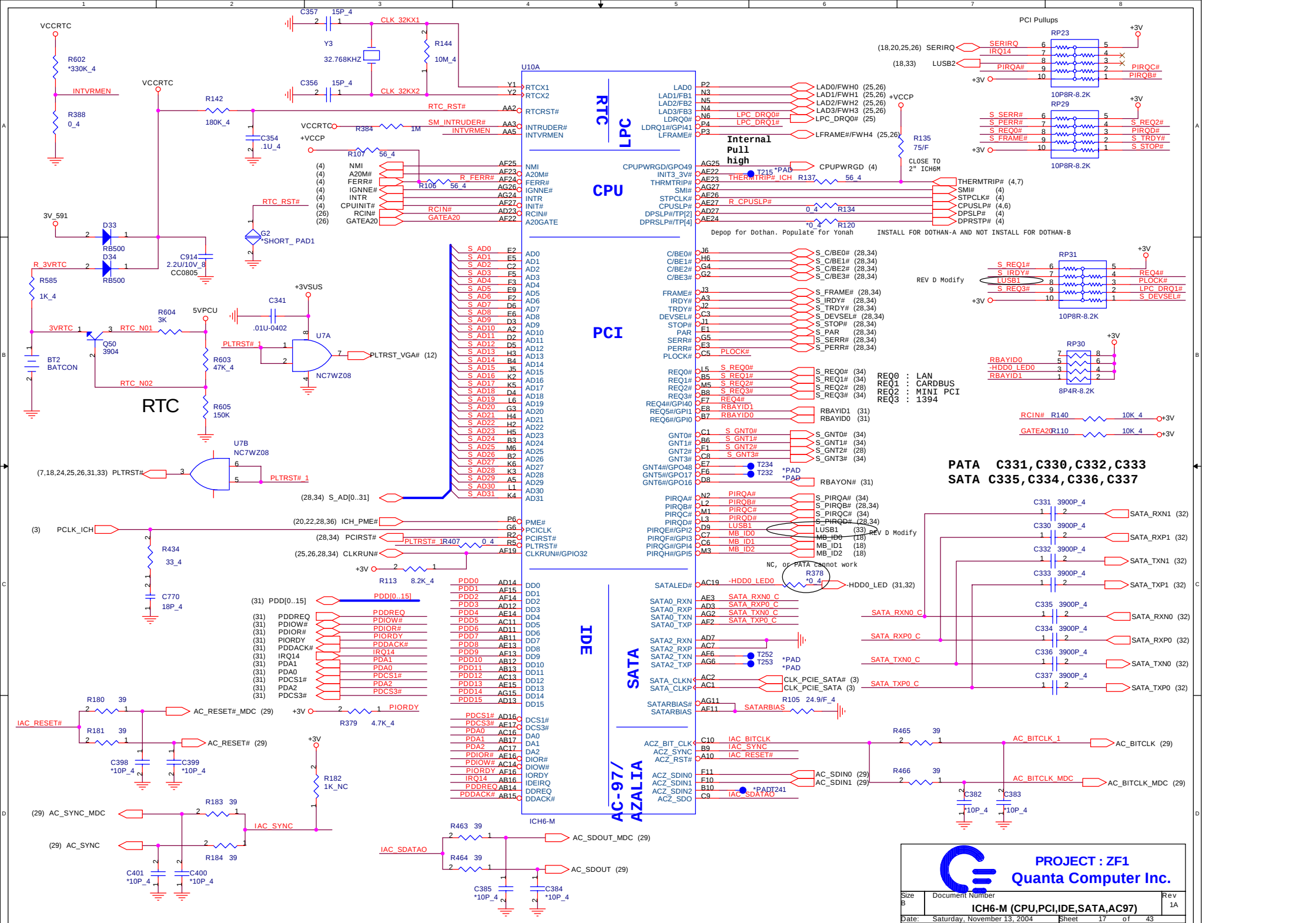


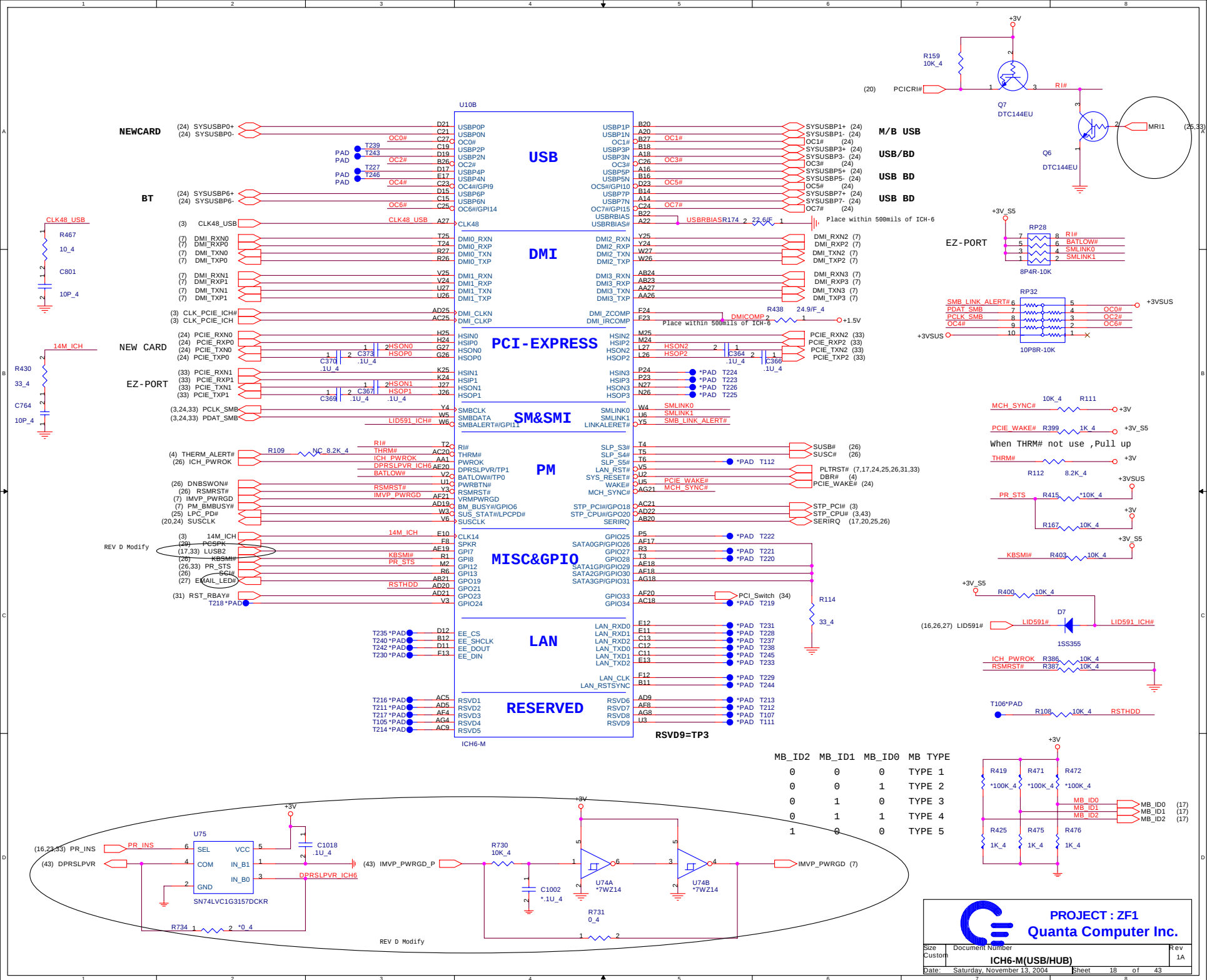


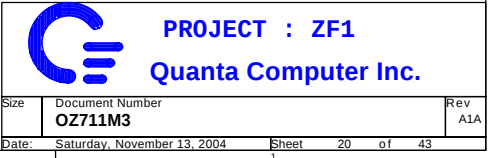
PROJECT : ZF1
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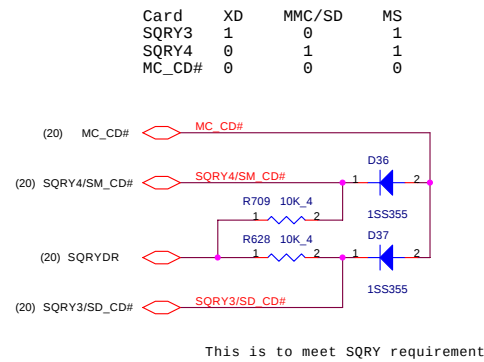
Size	Document Number	Rev
	VGA MEM & Strapping	A1A
Date:	Saturday, November 13, 2004	Sheet 14 of 43



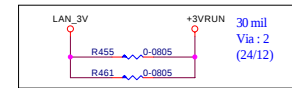




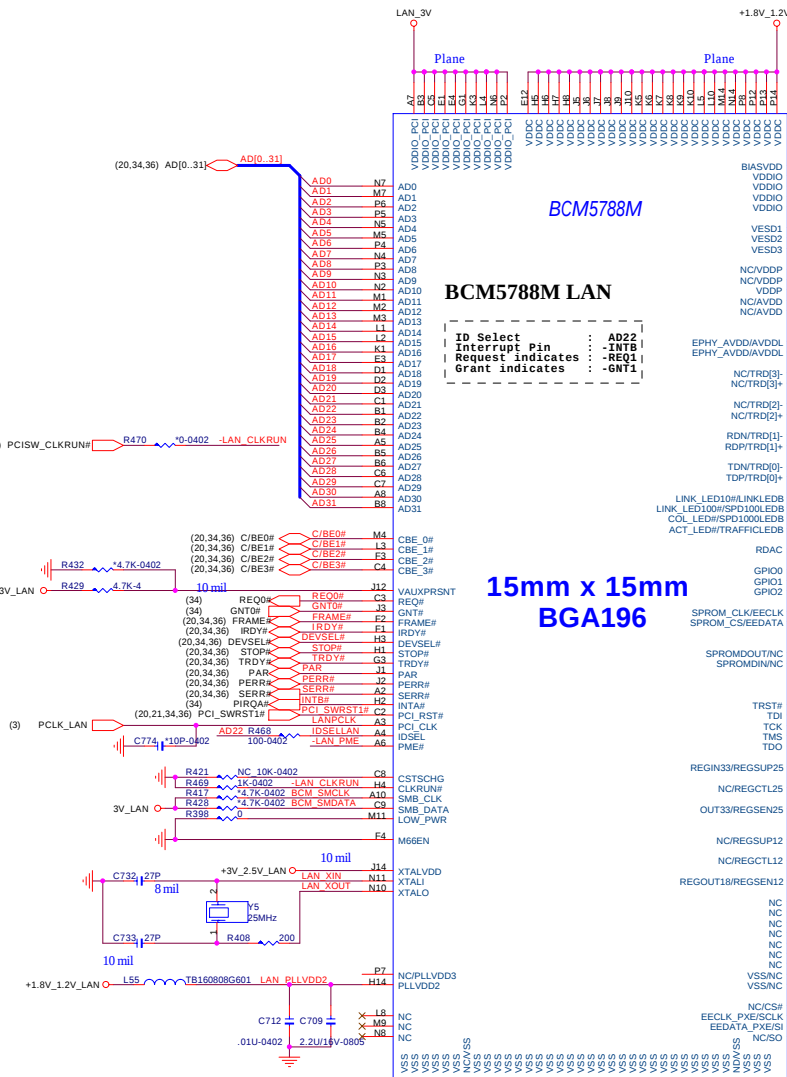


[illegible]

Sheet 21 of 43



FOR 5788M(61GA) USE

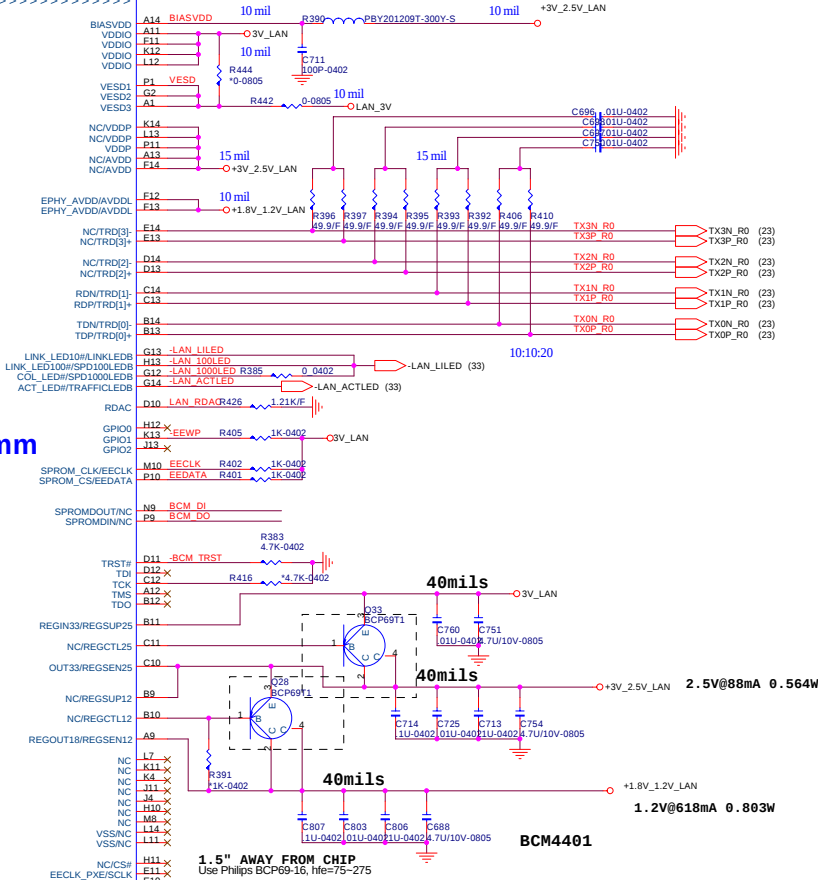


BCM5788M

BCM5788M LAN

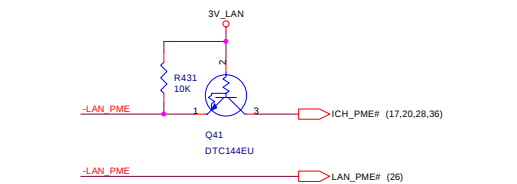
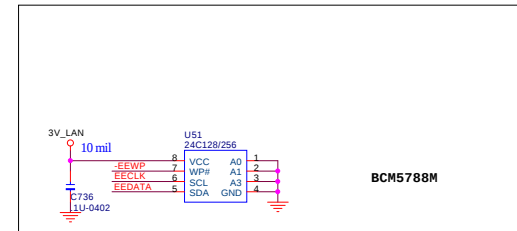
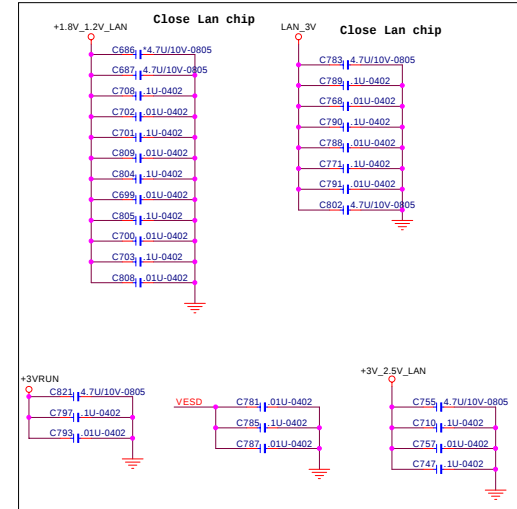
ID Select
Interrupt Pin
Request indicates
Grant indicates

15mm x 15mm
BGA196



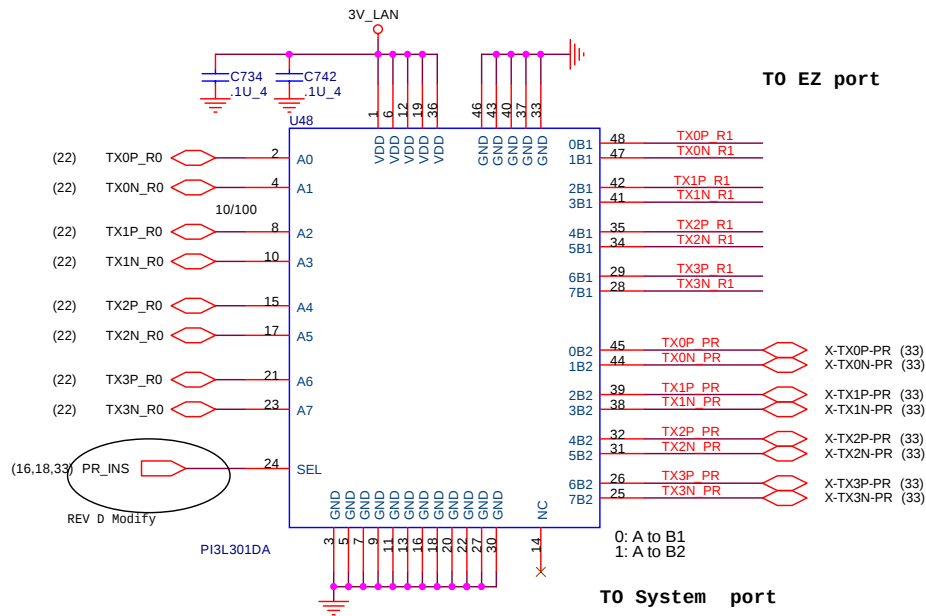
Voltage Rail 4401 5702 5705M
VDDIO_PCI 3V_S5 +3V +3V
+3V_2.5V_LAN 3.3V 2.5V 2.5V
+1.8V_1.2V_LAN 1.8V 1.2V 1.2V

BCM4401 DNS Q16, Q17, U26 R327, R329 R331, R332, U55
BCM5788M U55, R331, R332 Q16, Q17, U26



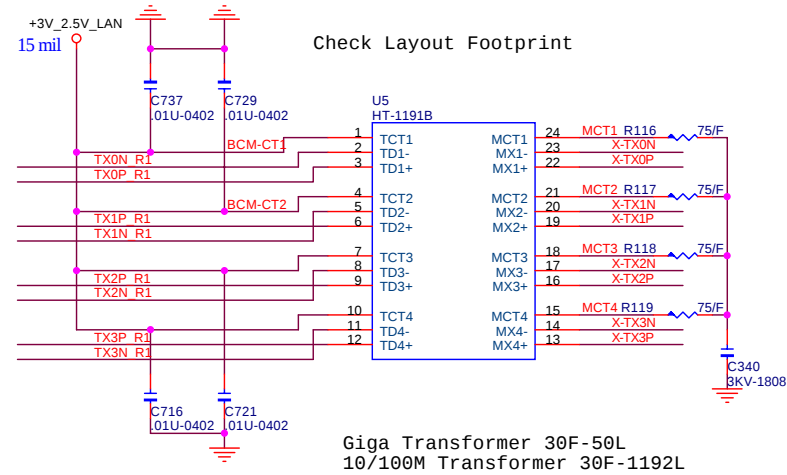
PROJECT : ZF1
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Lan Switch



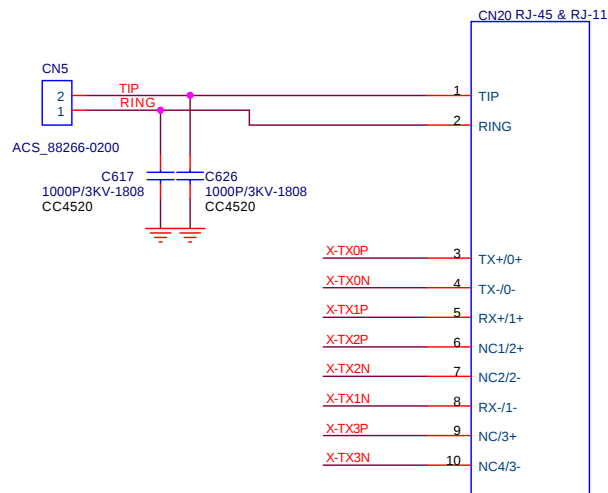
10/100/1000 M TRANSFORMER

Check Layout Footprint



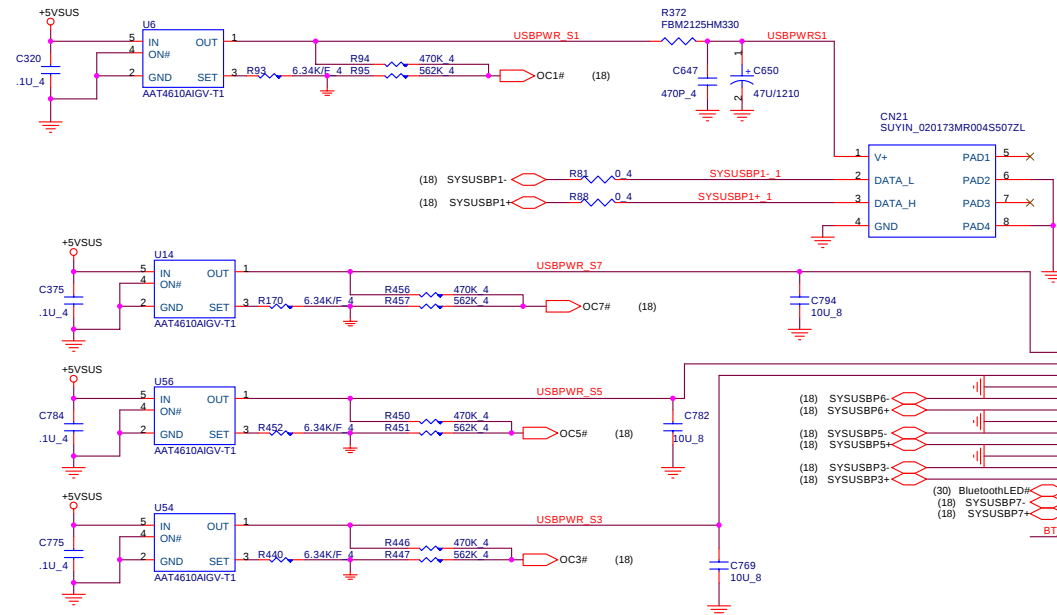
LAN and RJ11 Jack

Check Layout Footprint

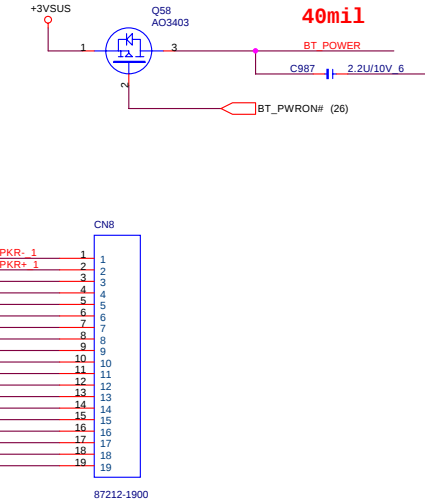


PROJECT : ZF1
Quanta Computer Inc.

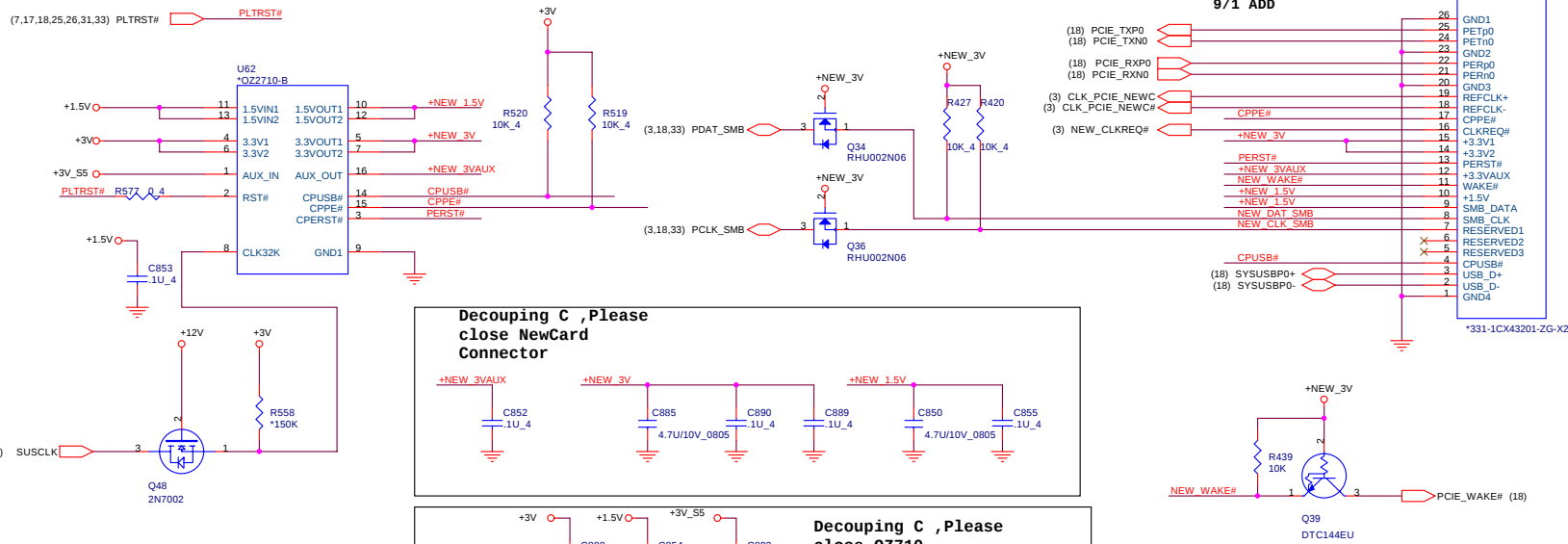
USB Connector and USB board



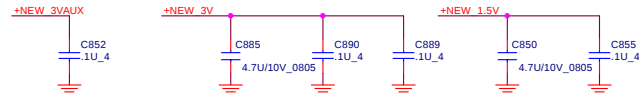
Bluetooth AND USB Connector



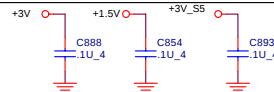
NewCard

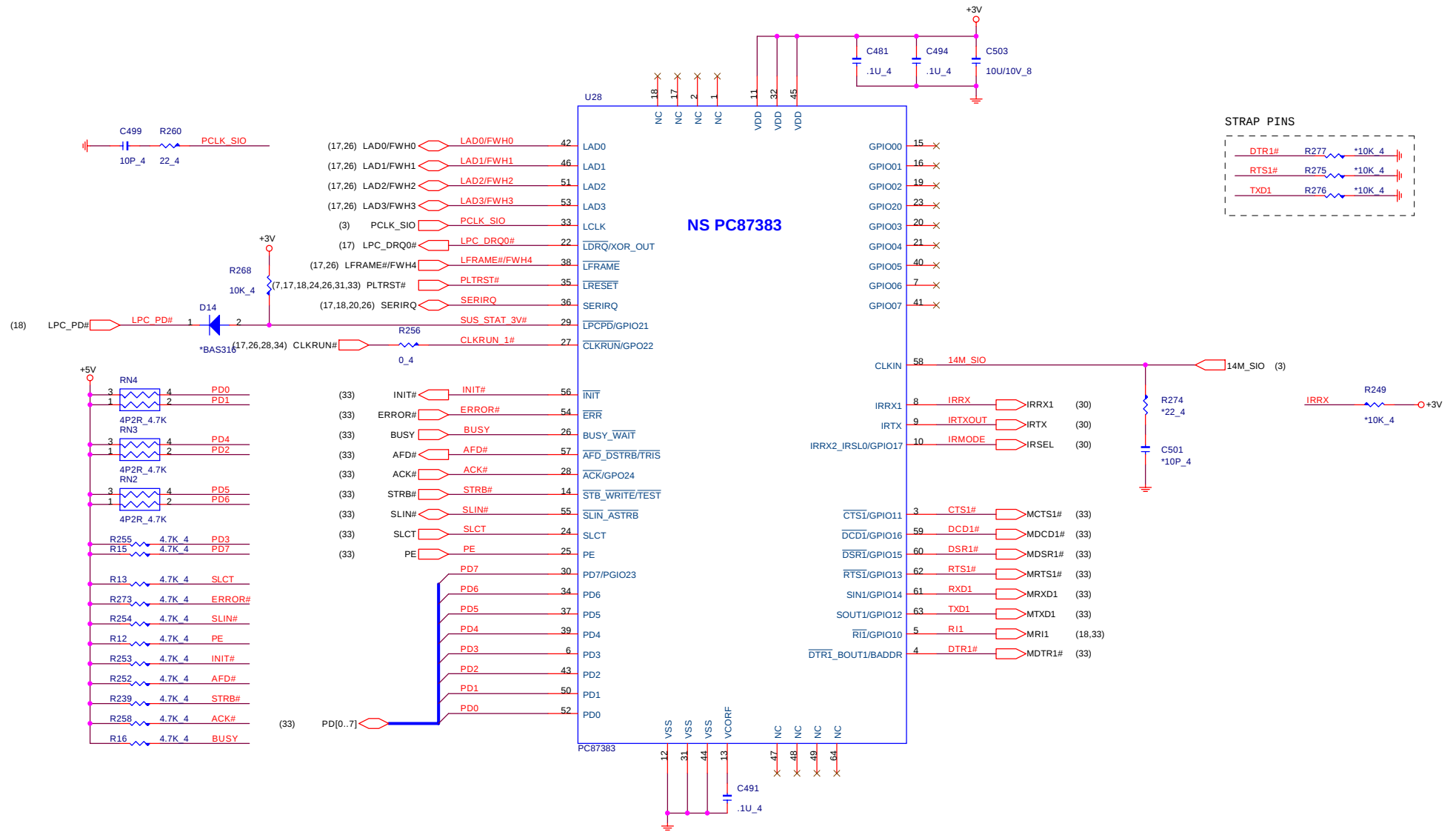


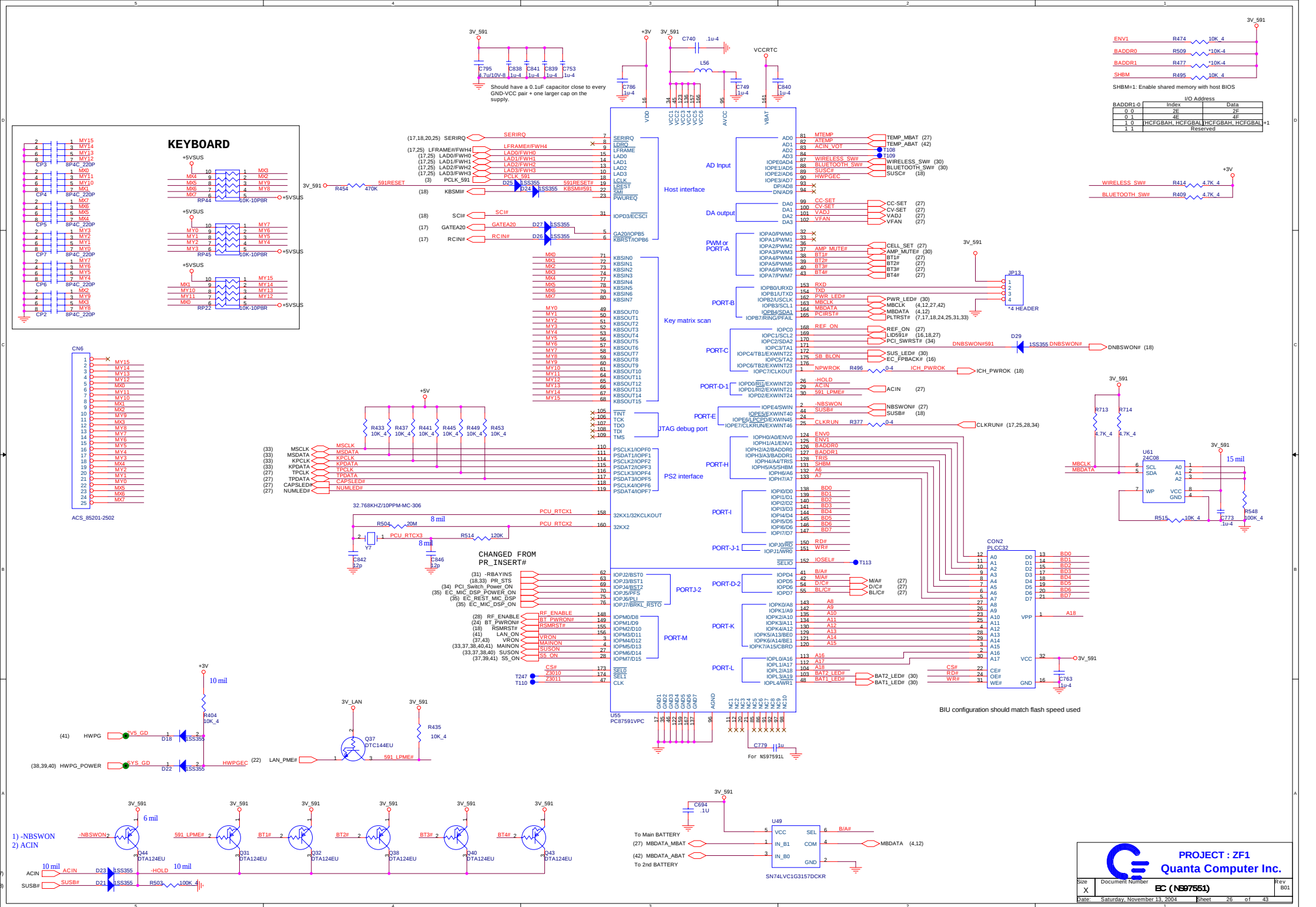
Decoupling C ,Please
close NewCard
Connector



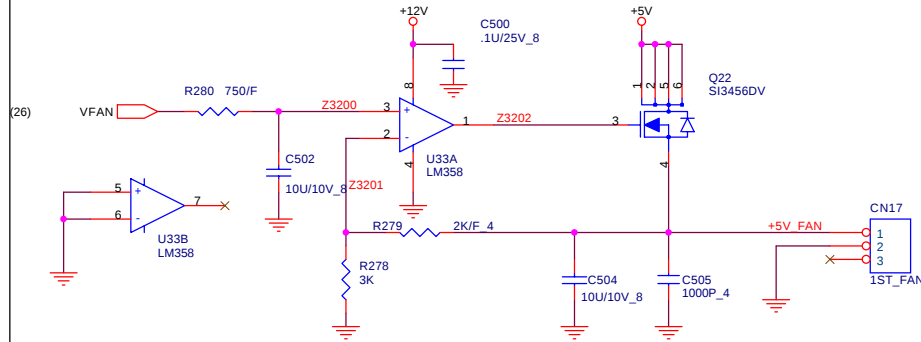
Decoupling C ,Please
close 02710



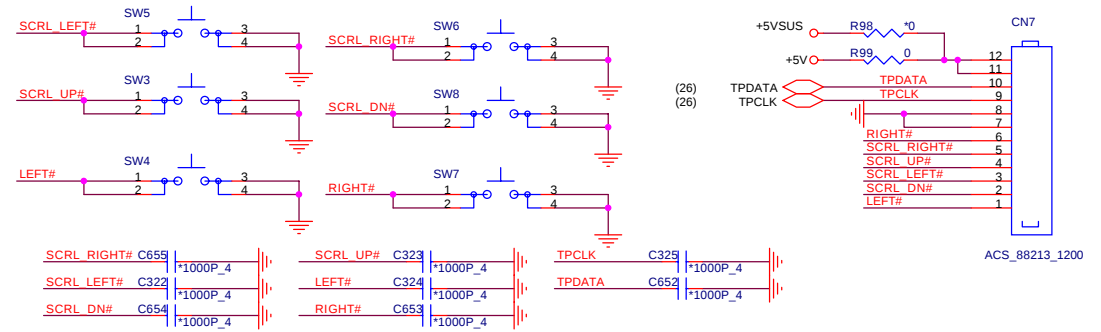




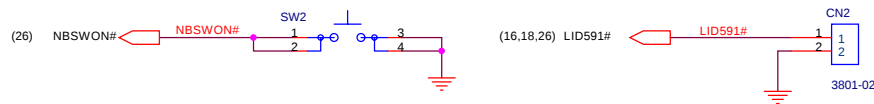
1st FAN OUT CONNECTOR



TouchPad Switch and T/P Module Connector

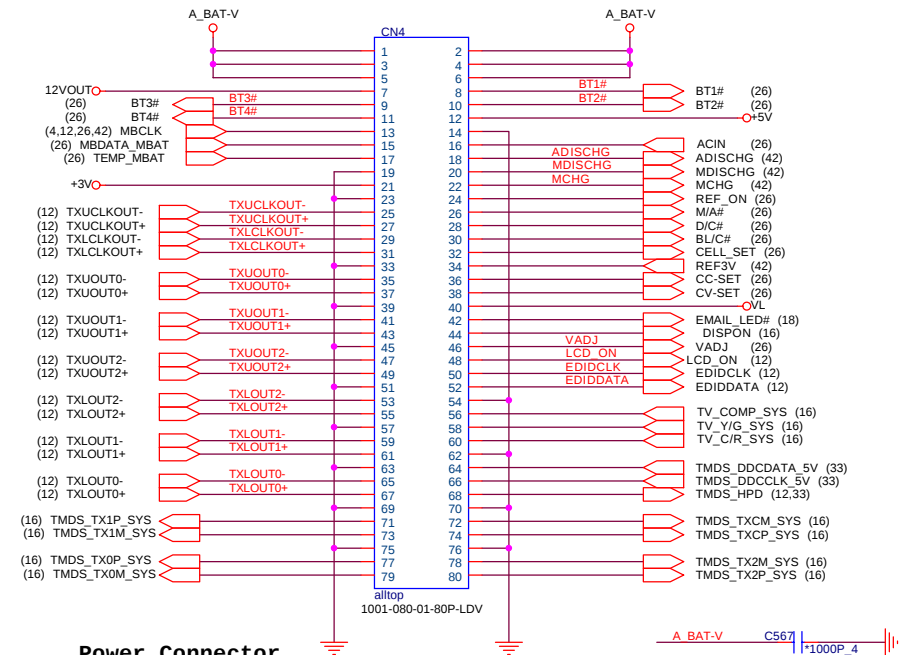
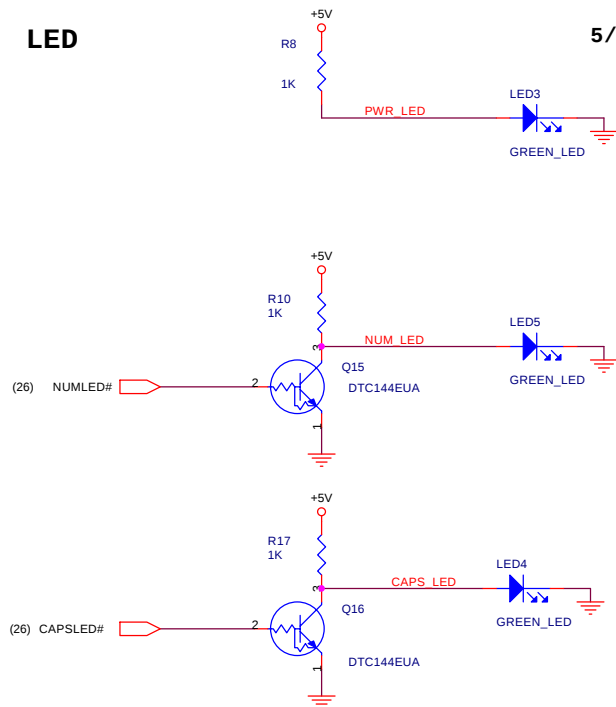


Power Switch

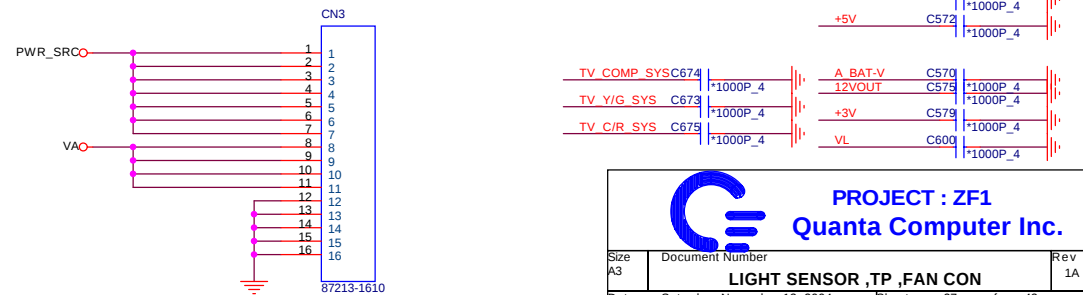


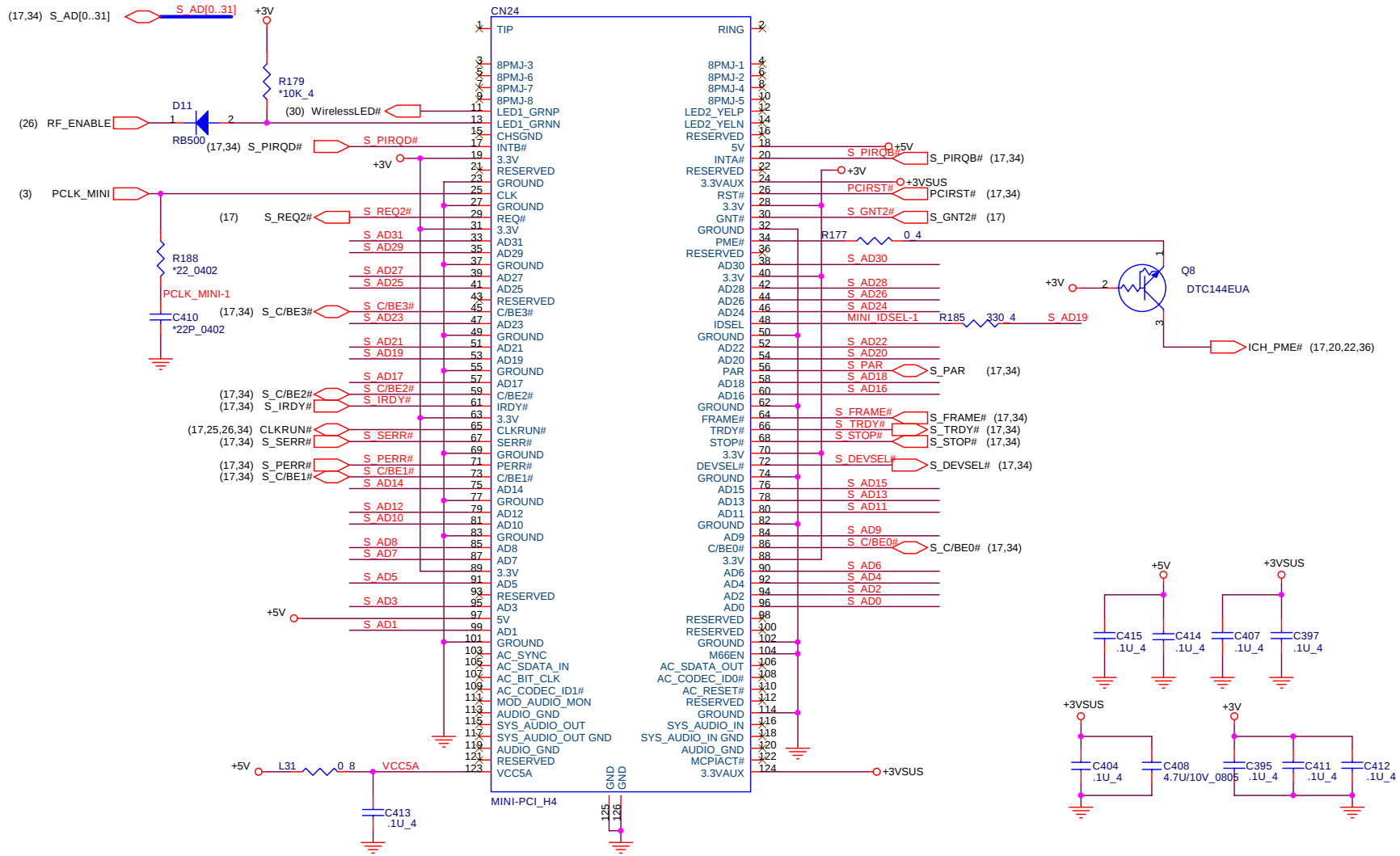
LED

5/28 ADD

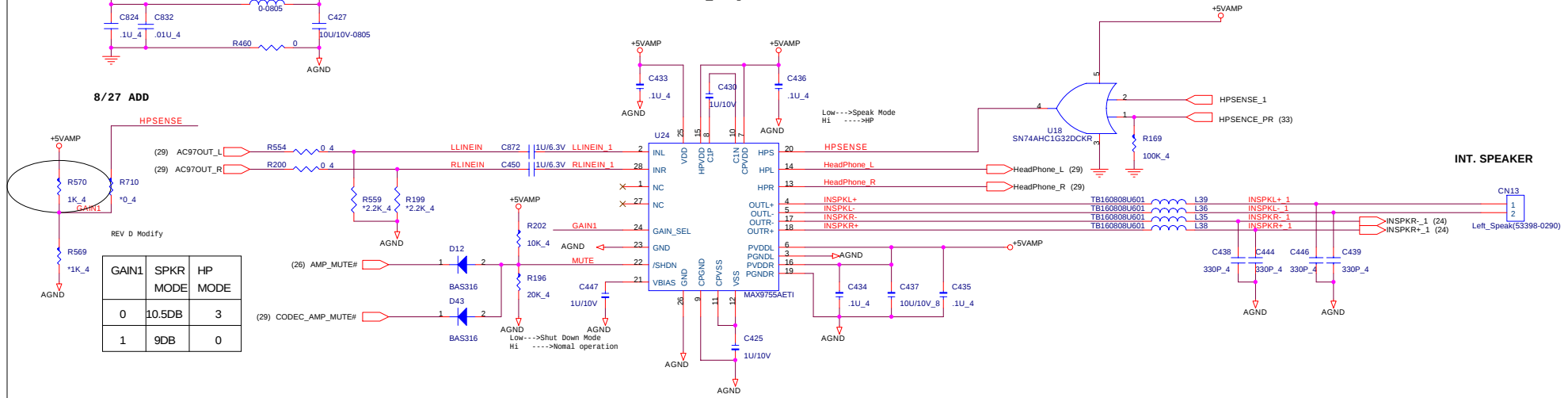


Power Connector

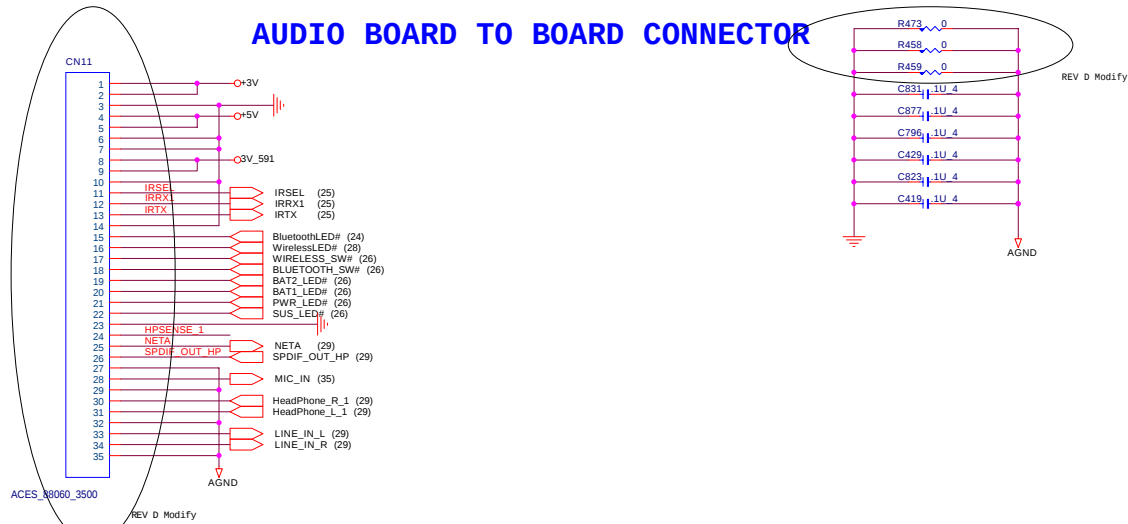




Audio amplifier



AUDIO BOARD TO BOARD CONNECTOR



[illegible]

9/1 A/D

IDE_LED

D40 CH501H-40

R7 1K

+3V

R72 4.7K

Q3 DTC144EUA

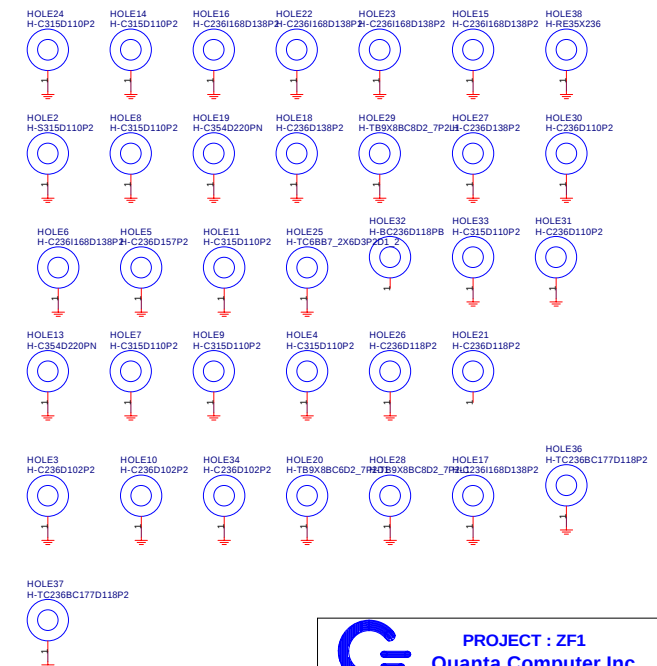
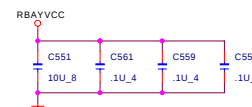
IDE_LED

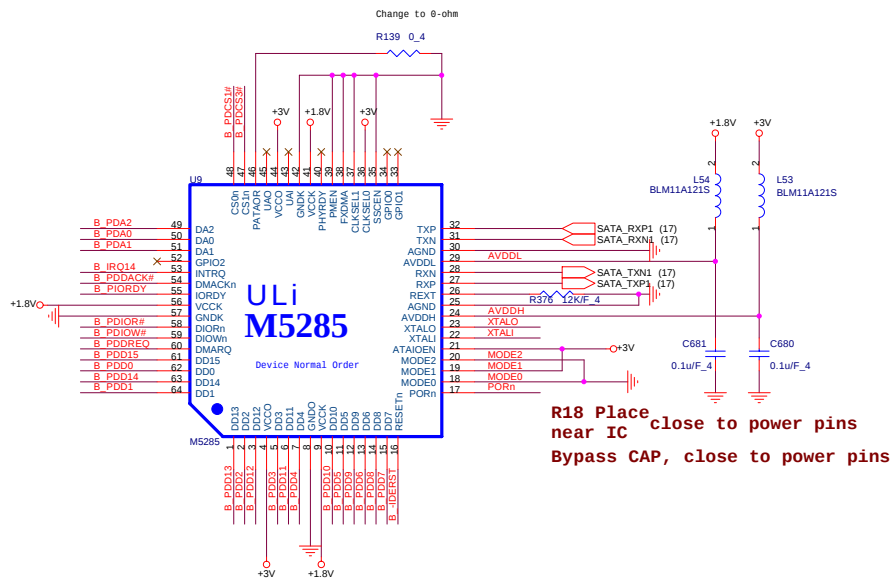
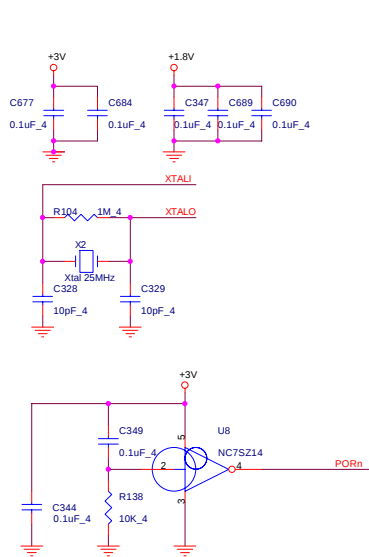
Orange_LED

DEL DE10 X2 AND A/D

[illegible]

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD



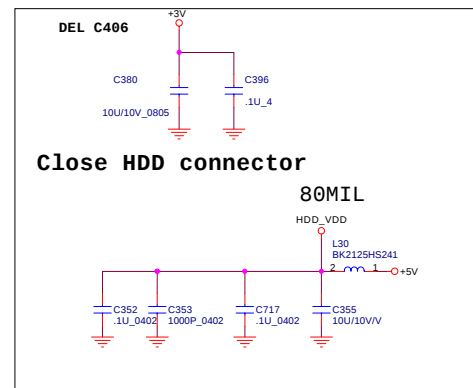
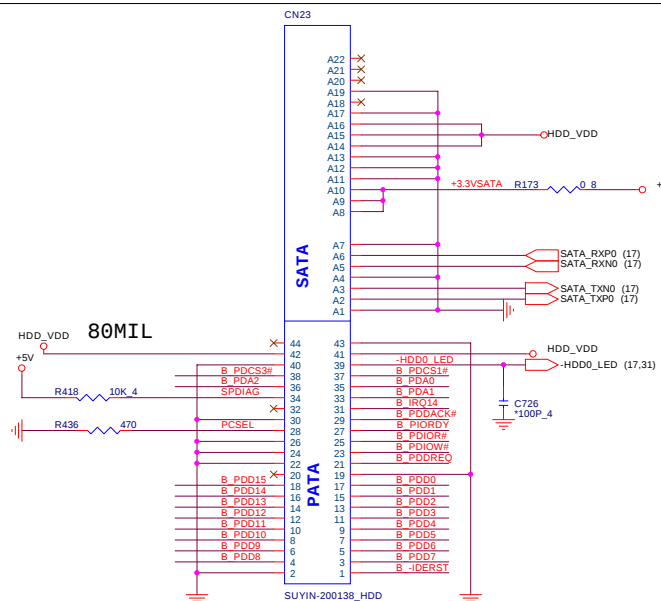
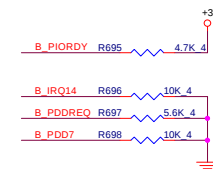


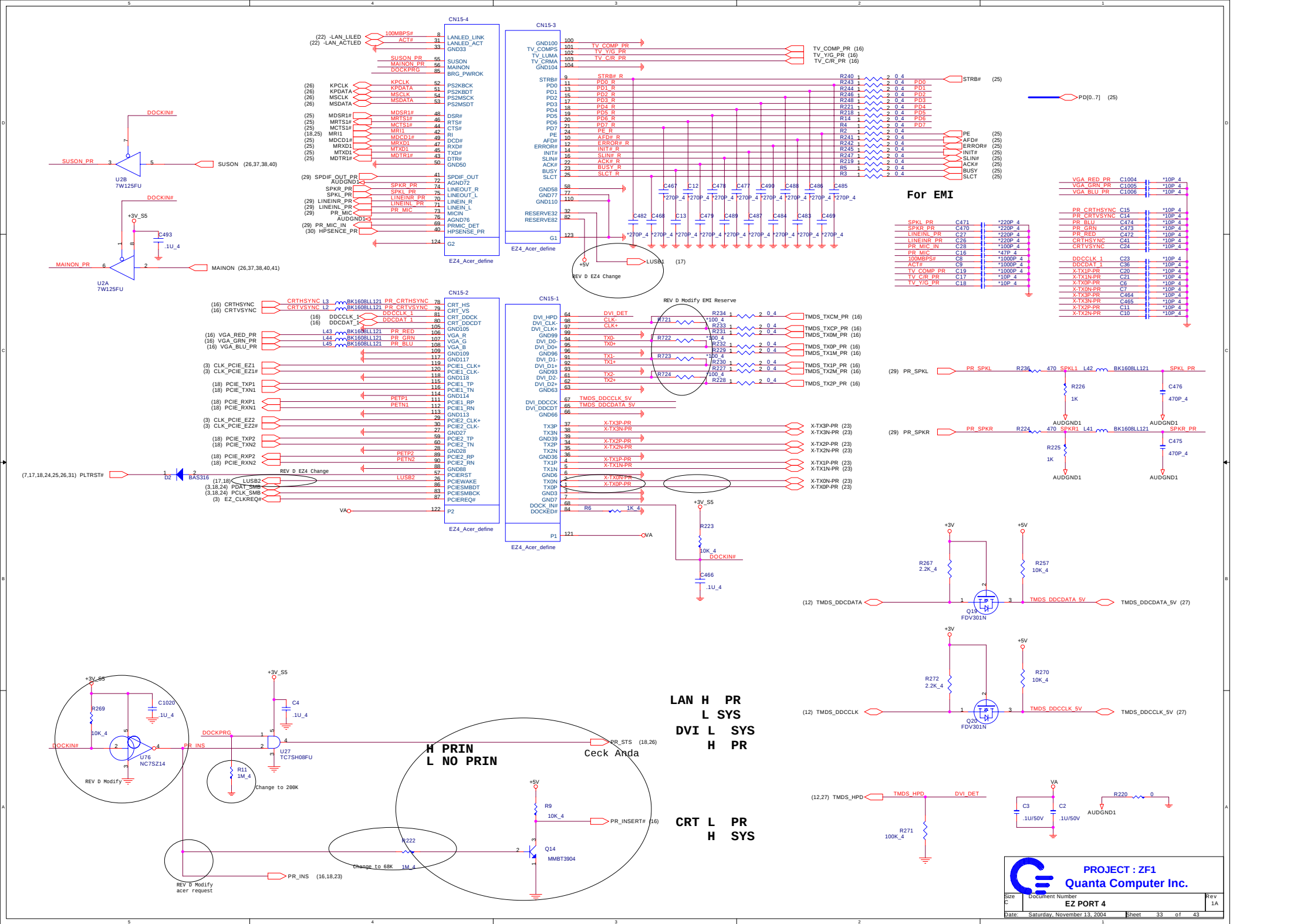
Operation Mode

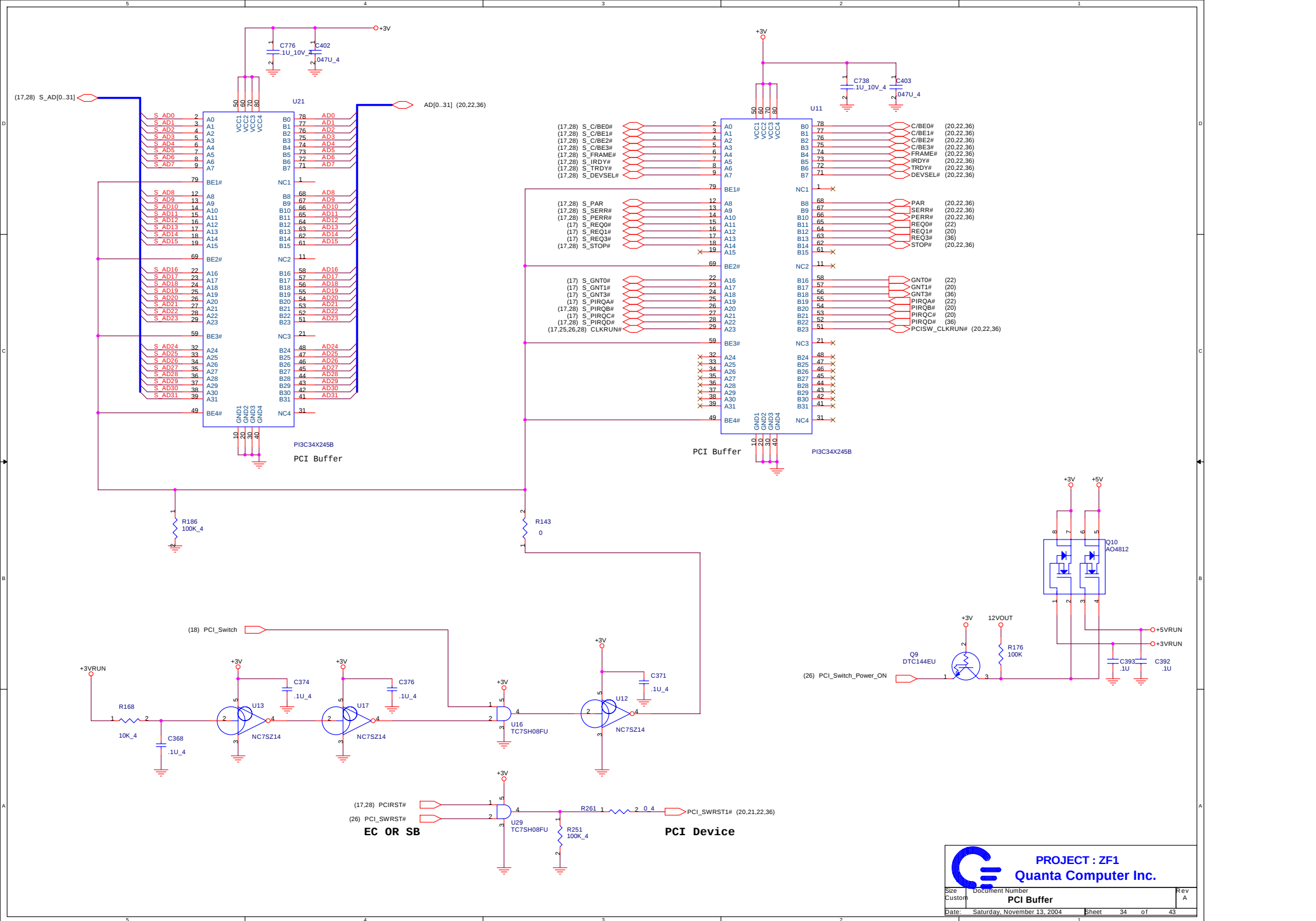
MODE[2..0]	Device mode
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVE

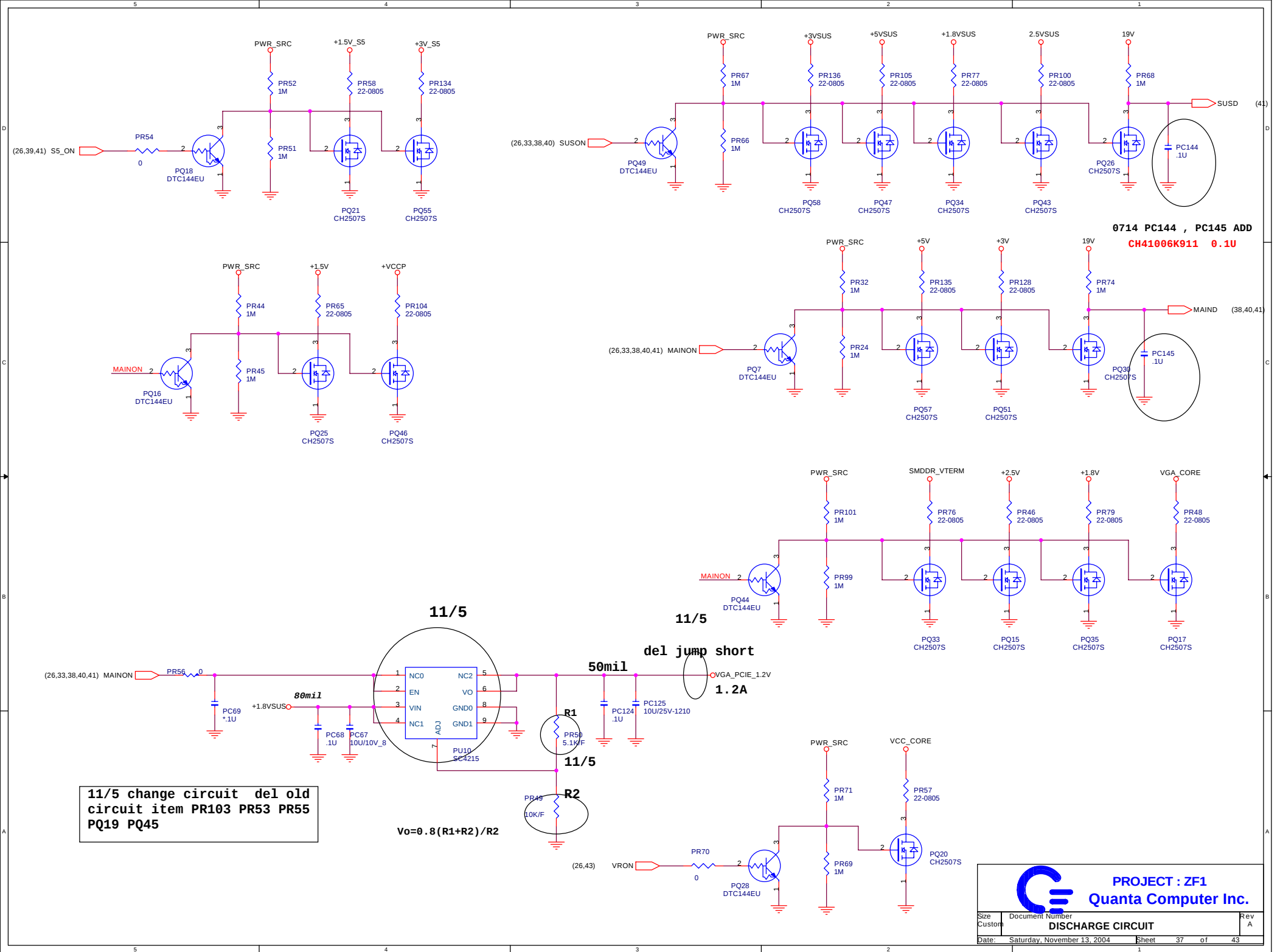
Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHz
0 1	25 MHz







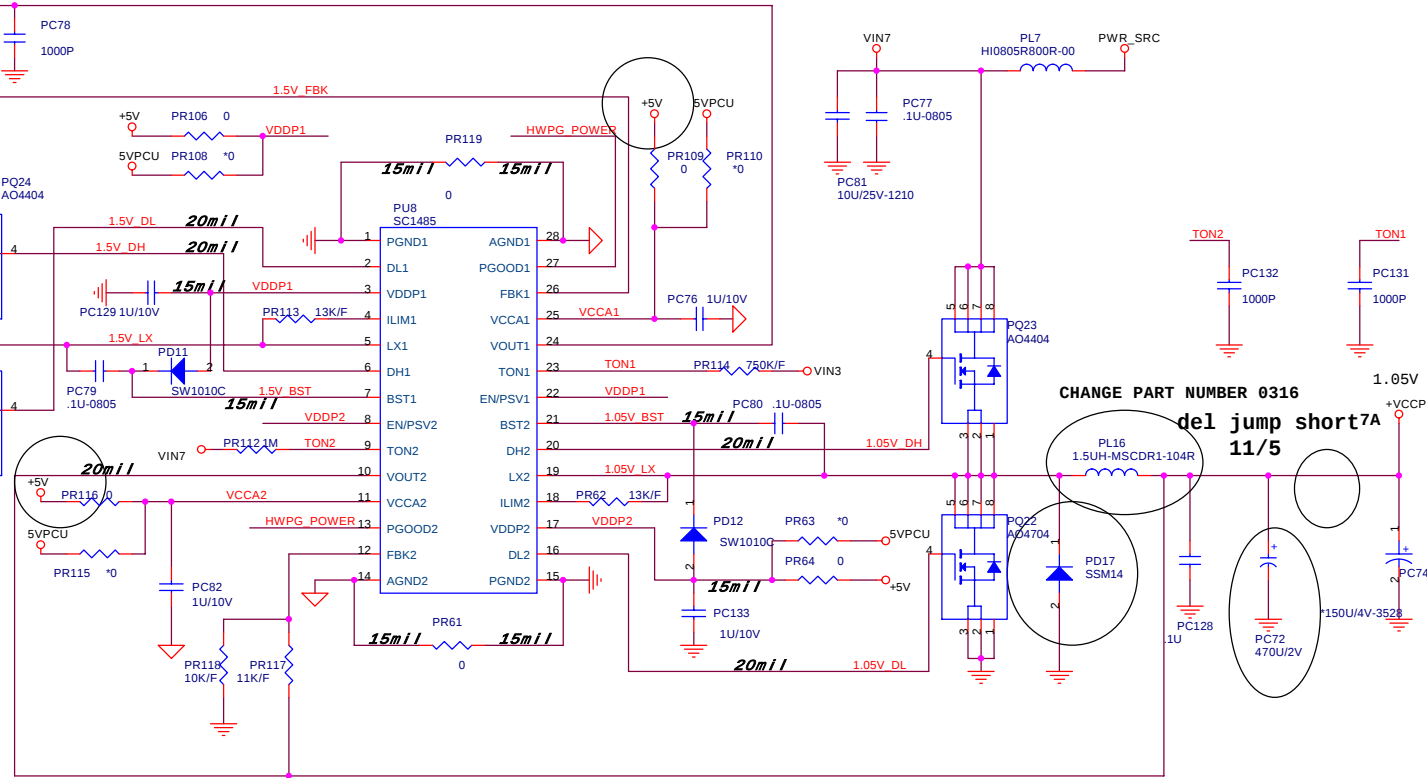


del jump short
11/5

$I_{LOAD} * R_{DS(on)} = 10 * R_{ILM1}$
 $A04704 R_{DS(on)} 4.5V = 0.013 \text{ ohm}$
 $10 * 0.013 = 0.00001 * R_{ILM1}$
 $R_{ILM1} = 13K$

0714 PD13 change from
 NC to BC000014Z01 SSM14
 0713 PC75 change from
 CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

(26,38,40) HWPG_POWER

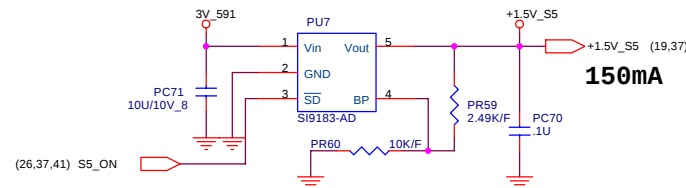


$I_{LOAD} * R_{DS(on)} = 10 * R_{ILM}$

$A04704 R_{DS(on)} 4.5V = 0.013 \text{ ohm}$
 $10 * 0.013 = 0.00001 * R_{ILM}$
 $R_{ILM} = 13K$

0714 PD817change from
 NC to BC000014Z01 SSM14

0713 PC72 change from
 CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343



$$L / RL(DCR) = Cqe * Rqe$$

$$3R3 \text{ DCR} = 0.0043$$

$$3.3u / 0.0043 = 0.1u * Rqe$$

$$Rqe = 7.68K$$

0714 PR37 change from
CS21823F902 1.82K/F to CS27683F909 7.68K/F

0714 PL13 change from
CV-15A0MZ05 1R5 to CV-33E0MZ01 3R3

0714 PQ11 change from
BAM44040012 A04404 to BAM60300Z11 FDD6030L

0714 PQ37 change from
BAM47040005 A04704 to BAM66880Z01 FDD6688

$$L / RL(DCR) = Cqe * Rqe$$

$$3R8 \text{ DCR} = 0.0130$$

$$3.8u / 0.0130 = 0.1u * Rqe$$

$$Rqe = 2.94K$$

del jump short
11/5

1.2V/1.0V
VGA_CORE
12A

0714 PC118 change from
NC to CH747RY8800 470u/2.5V-7343

0713 PC57 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

0714 PD8 change from
NC to BC000014Z01 SSM14

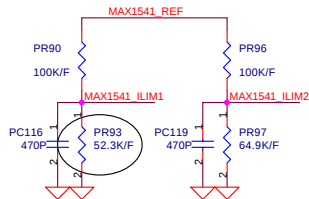
$$I \text{ LOAD} * DCR * 10 = ILIM$$

$$3R3 \text{ DCR} = 0.0043$$

$$16 * 0.0043 * 10 = 0.688V (ILIM1)$$

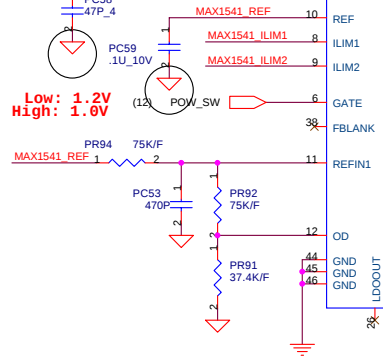
$$1R5 \text{ DCR} = 0.0081$$

$$6 * 0.0130 * 10 = 0.78V (ILIM2)$$



0714 PR93 change from

CS34993F908 49.9K/F to CS35233F908 52.3K/F



Low: 1.2V
High: 1.0V



0714 PR137 ADD
CS01003F902 10
0714 PC146 ADD
CH41006K911 0.1u

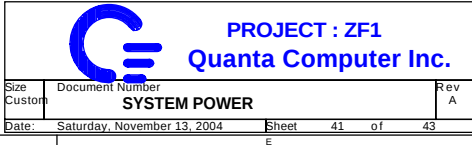
del jump short
11/5

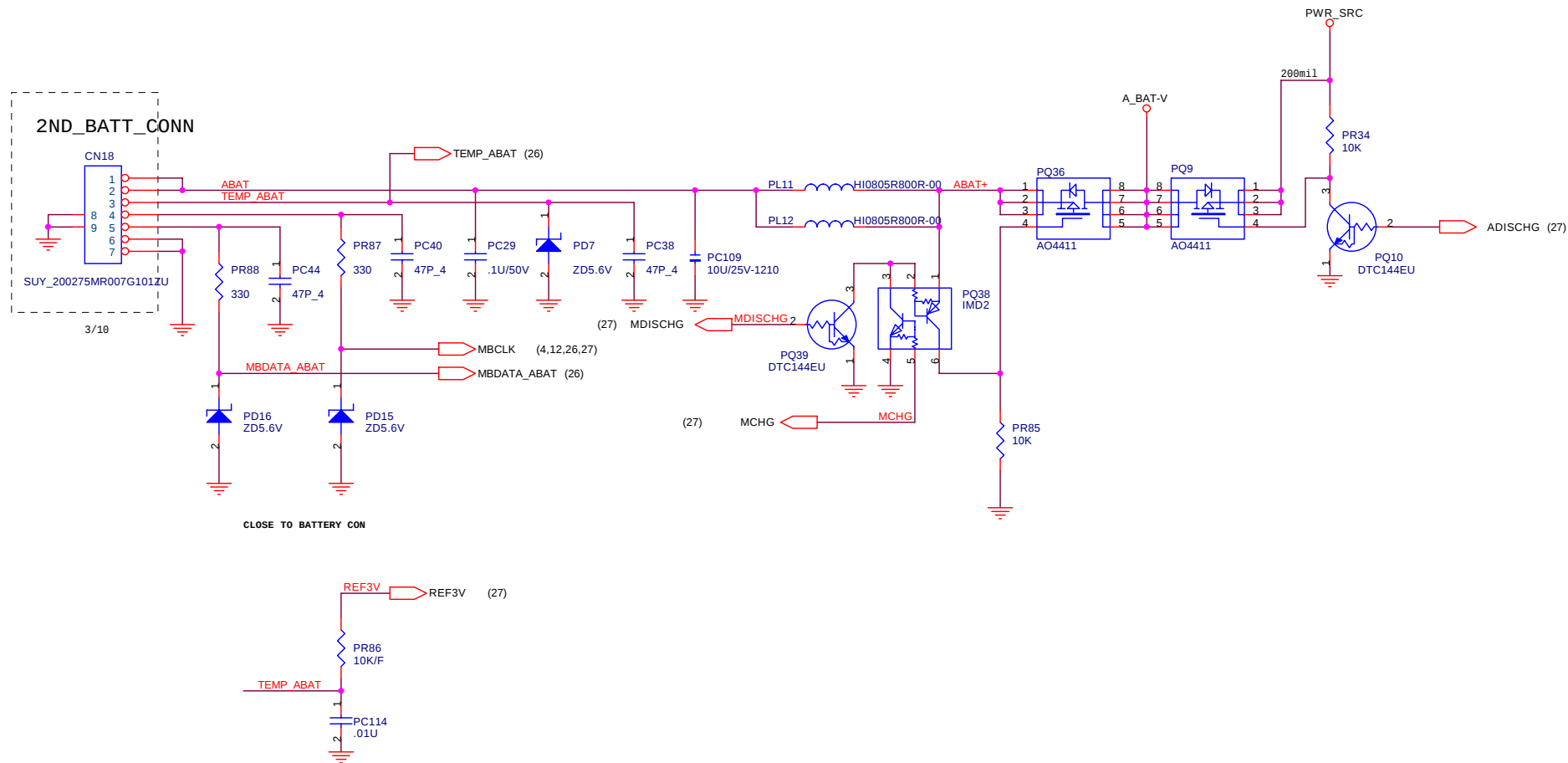
4A



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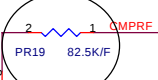




0714 PR19 change from

CS34223F901 42.2K/F to CS38253F909 82.5K/F

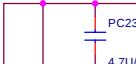
value provided
2.67% offset;
old value was
for old 4.62%
offset.



BG waveforms
improved. may
delete from
future
revision.

0714 PR27 change from

CS-33304JA09 3.3 to CS00004JA07 0



CHANGE CHOCK 0316

2mR-7520 PR102

PC37 10U/25V-1210

PC39 10U/25V-1210

PC35 10U/25V-1210

PC33 *10U/25V-1210

PC43 1U-0805

PC31 1U-0805

PC32 2200P

PC48 1U-0805

PC35 10U/25V-1210

PC33 *10U/25V-1210

PC122 470U/2.5V-7343

PC66 470U/2.5V-7343

PC123 470U/2.5V-7343

PC64 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

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PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

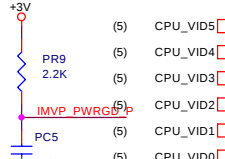
PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

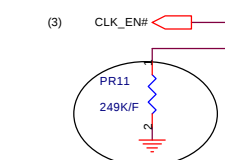
PC123 470U/2.5V-7343

PC123 470U/2.5V-7343

PC123 470U/2.5V-7343



Set up for
constant-ripple
mode. was
constant-frequency
mode



20 mil Trace list for layout

Added filter for PBOOT

PR11 249K/F

PR17 *30.1K/F

PR13 36.5K/F

PR20 33.2K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

PR23 54.9K/F

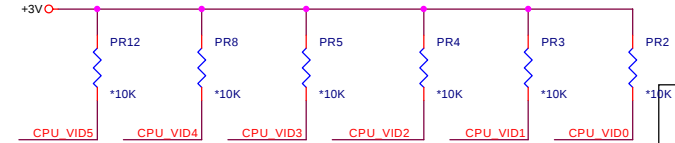
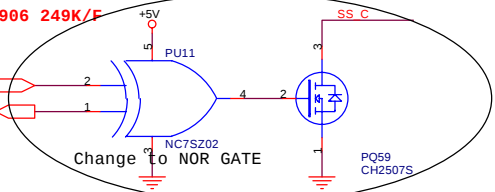
V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	V
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	1	0	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

10 mil Trace list for layout

SC1476
pin 4 pin
5 pin 7
pin 25
pin 30



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