Brook_BH_ULT
Schematics Document

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Title: ***Cover Page***		
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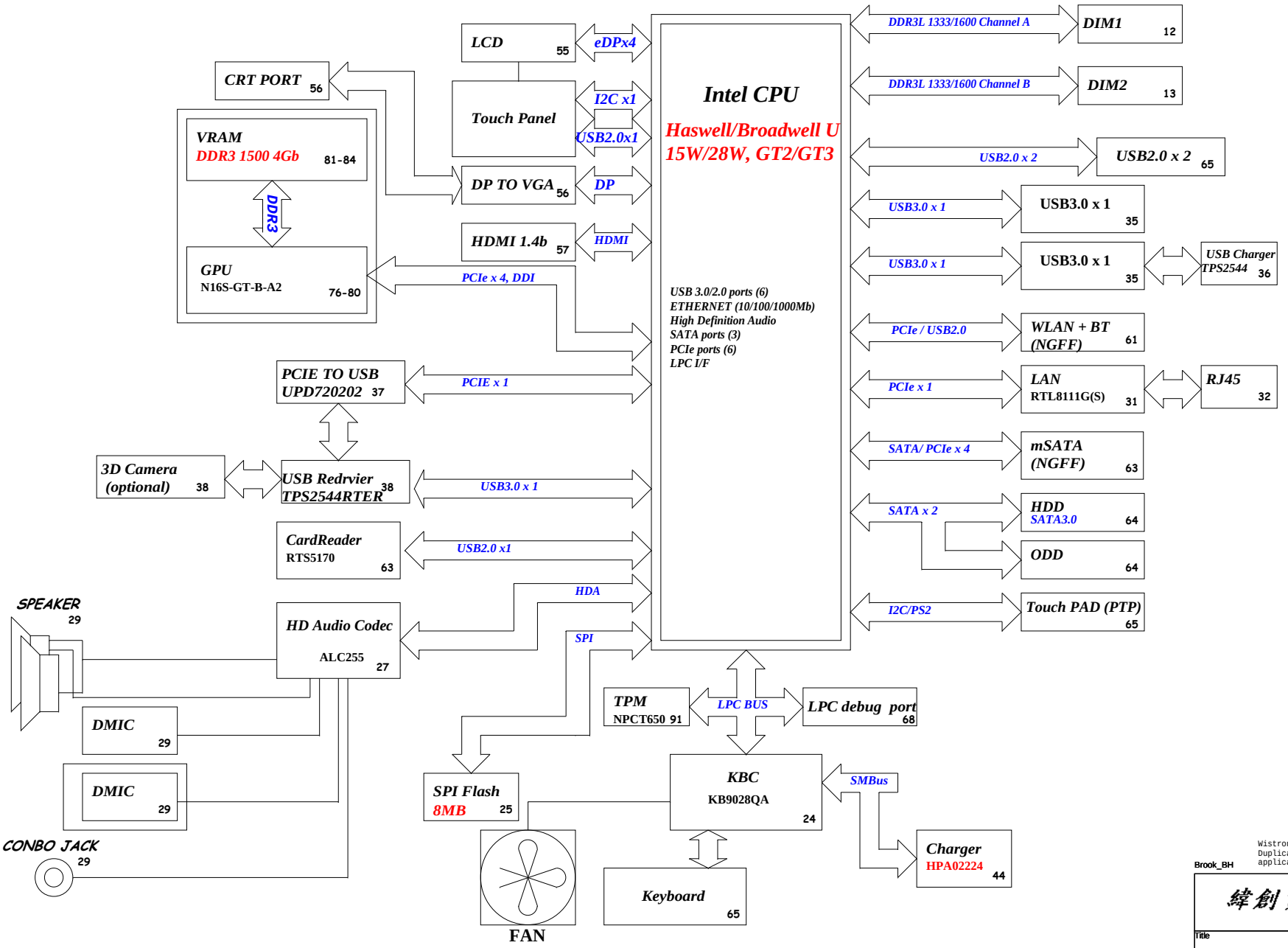
BROOK ULT Board Block Diagram

Project code : 4PD04X010001
PCB P/N : 14276
Revision : -1M



CHARGER HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT6575B	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC RT6575B	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51716	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8231	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM LDO S13390D15	51
INPUTS	OUTPUTS
3D3V_S5	1D3V_S5

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Title: Block Diagram

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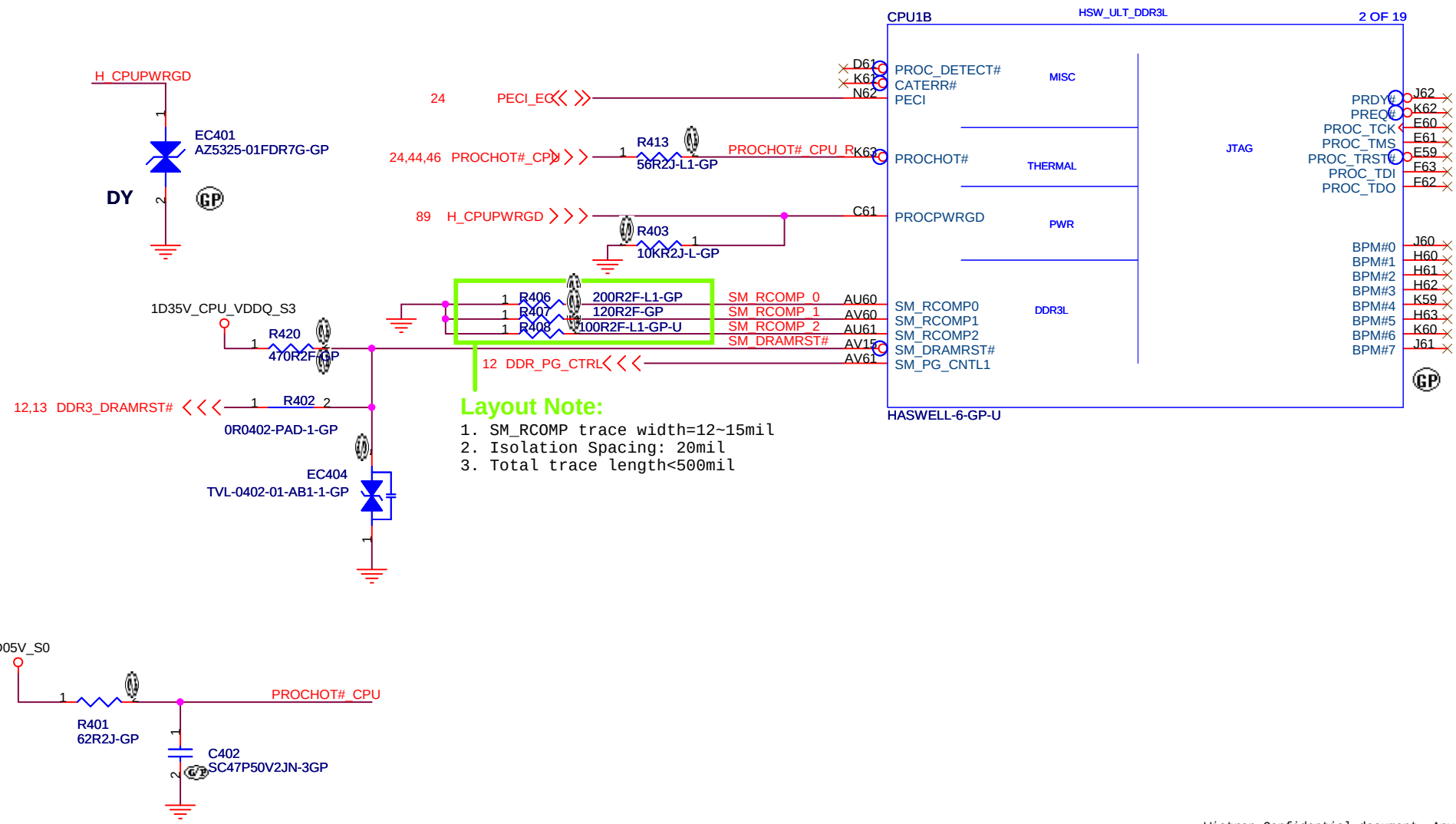

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Title
CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A4	Brook_BH	-1M

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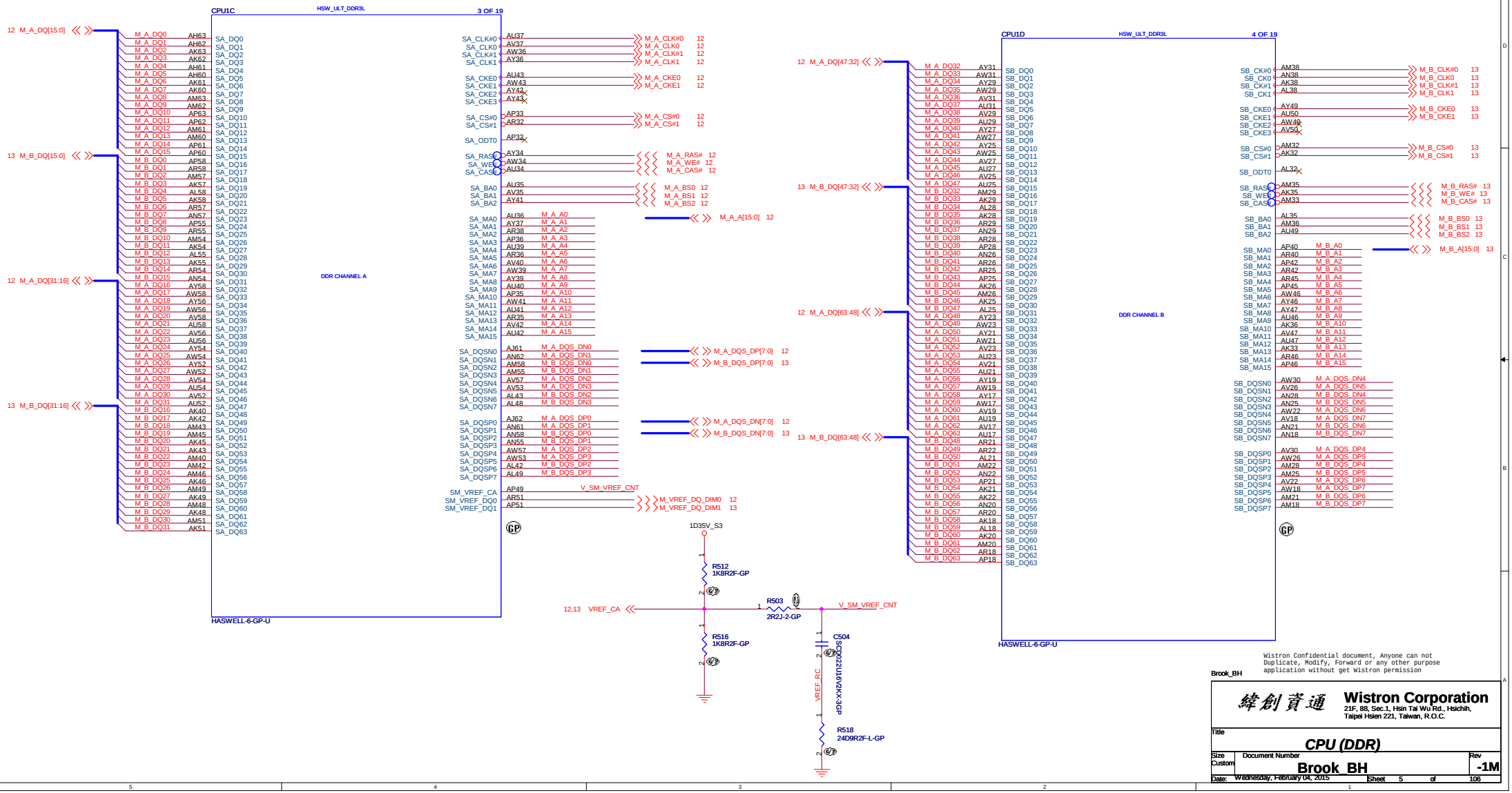
SSID = CPU



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Title: **CPU (DDR)**

Size	Document Number	Rev
Custom	Brook_BH	-1M

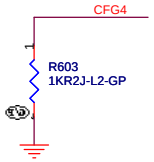
Date: Wednesday, February 04, 2015 Sheet 5 of 106

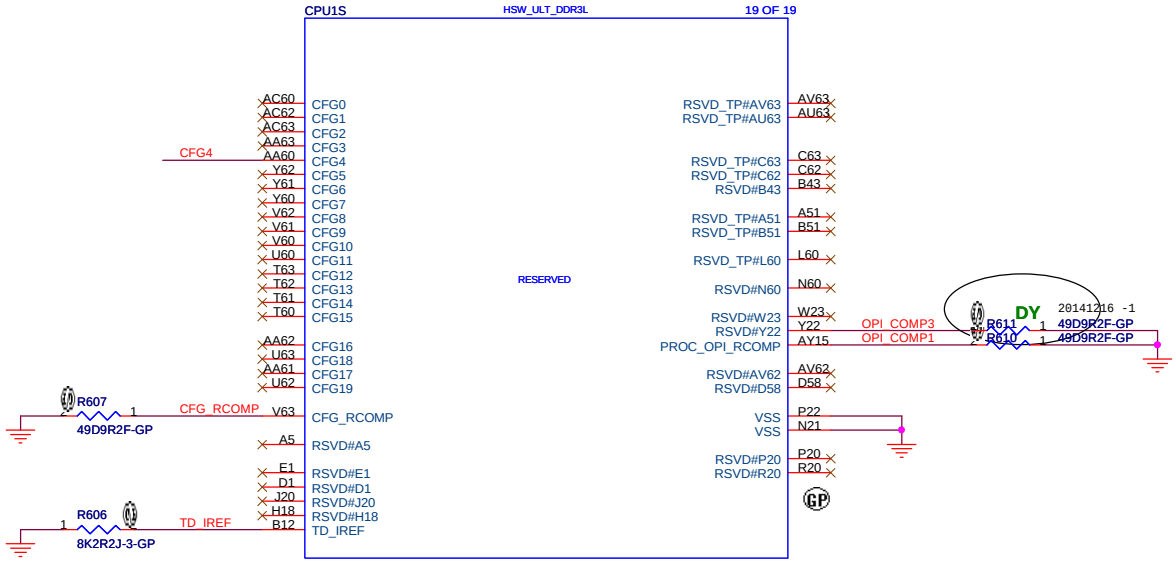
SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✔
CFG[19:0]		Please refer to the *Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)* .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable
	0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

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Title: **CPU (CFG)**

Size	Document Number	Rev
Custom	Brook_BH	-1M

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SSID = CPU

1D35V_S3 1D35V_CPU_VDDQ_S3

PG701 PG702 PG703 PG704 PG705 PG706 GAP-CLOSE-PWR

1D05V_S0

Close to CPU

130R2F-1-GP R703 VIDSOUT_CPU

75R2F-2-GP R704 VIDALERT#_CPU

R701 close to CPU

RN701 SRN100J-L-GP VSS_SENSE VCC_SENSE

1V_CPU_CORE

RN702 SRN10KJ-L-GP

40,48,51 1D05V_S0_PWRGD

26,40,46 IMVP_PWRGD

VCCST_GD_CPU IMVP_PWRGD_R

ET701 TVL-0402-01-AB1-1-GP ET702 TVL-0402-01-AB1-1-GP

R707 5K1R2-GP R708 5K1R2-GP

C703,C715 close to CPU

PIN AC22 AE22 AE23

C703 SC22U6D3V5MX-L3-GP

DY C715 SC1U10V2KX-L1-GP

1D35V_CPU_VDDQ_S3

1V_CPU_CORE

1V_VCOMP_OUT

1D05V_S0

CPU1L HSW_ULT_DDR3L 12 OF 19

HSW ULT POWER

RSVD#L59 RSVD#J58

VDDQ x10 VCC

RSVD#N58 RSVD#AC58

VCC_SENSE RSVD#AB23 VCCIO_OUT VCCIOA_OUT RSVD#AD23 RSVD#AA23 RSVD#AE59

46 VCC_SENSE VCC_SENSE

46 VIDALERT#_CPU VIDSCK_CPU 46 VIDSOUT_CPU VCCST_GD_CPU 46 H_VR_EN

R705 43R2J-GR VIDALERT#_CPU_R

IMVP_PWRGD_R

R706 150R2F-4-L-GP PWR_DEBUG

Follow Intel CRB

VIDALERT# VIDSCLK VIDSOUT VCCST_PWRGD VR_EN VR_READY

PWR_DEBUG# VSS RSVD_TP#P60 RSVD_TP#P61 RSVD_TP#N59 RSVD_TP#N61 RSVD#T59 RSVD#AD60 RSVD#AD59 RSVD#AA59 RSVD#AE60 RSVD#AC59 RSVD#AG58 RSVD#U59 RSVD#V59

VCCST x3

VCC x7

VCC x10

HASWELL-6-GP-U

1V_CPU_CORE

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Title: CPU (VCC_CORE)

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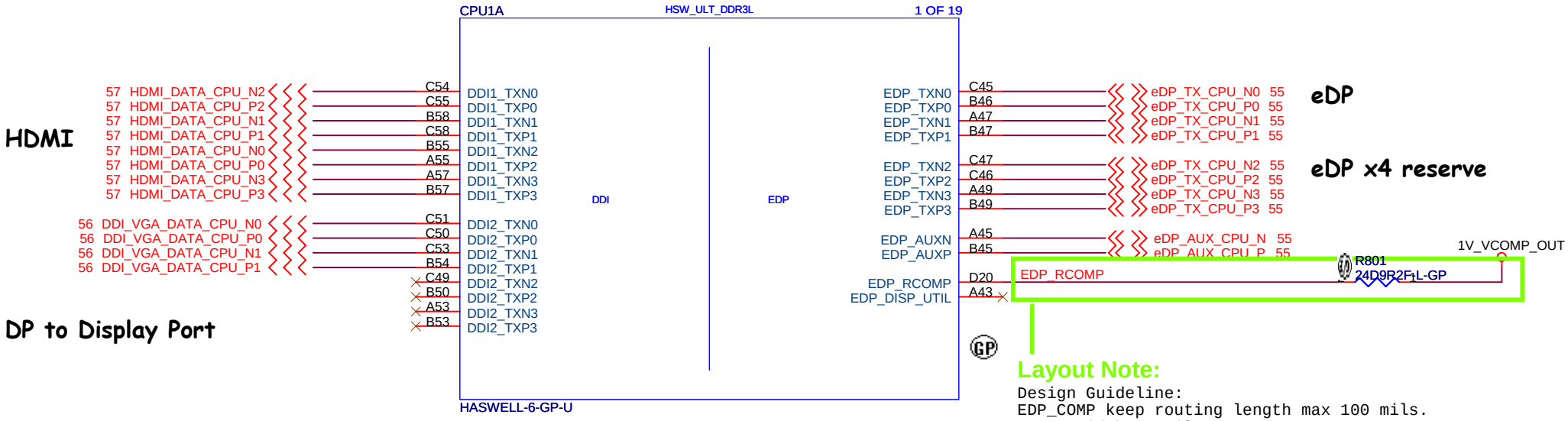
SSID = CPU



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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Title: ***CPU (DDI/EDP)***

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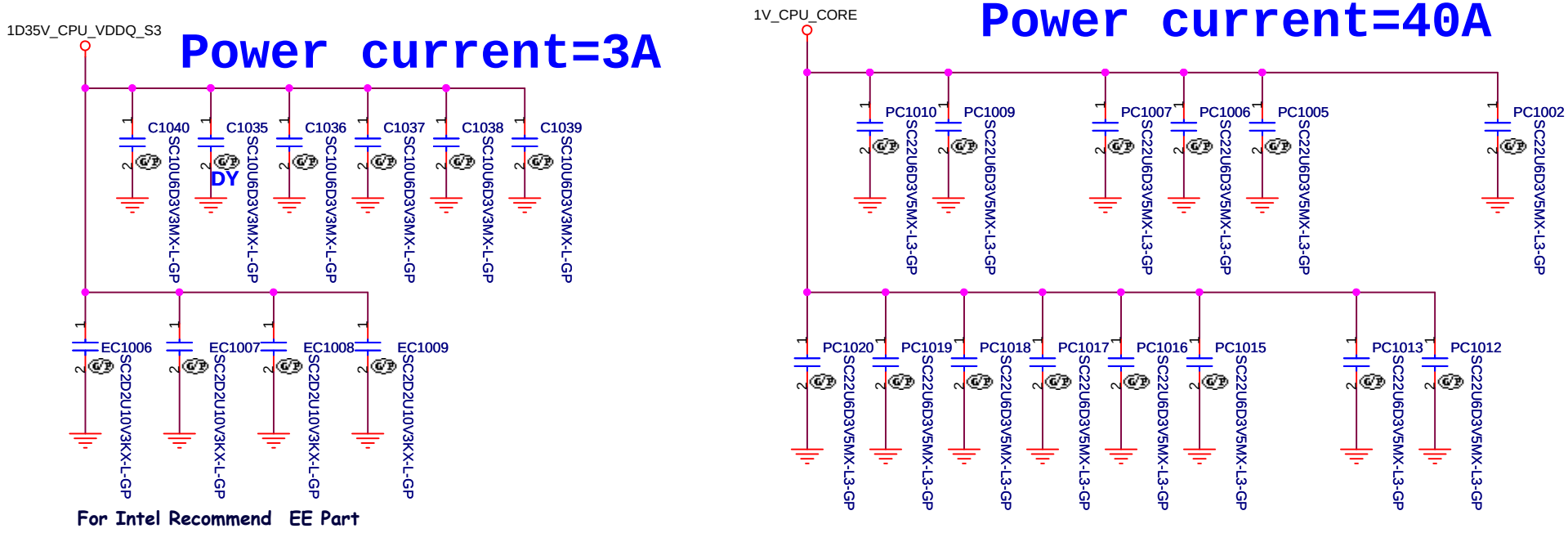

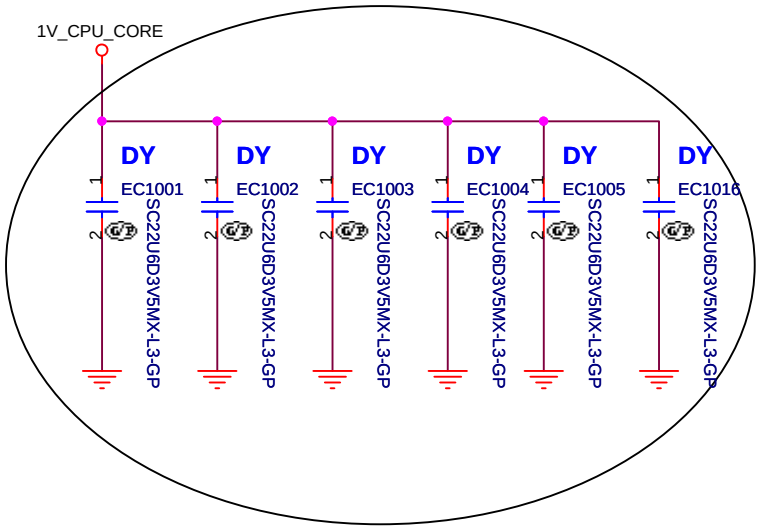

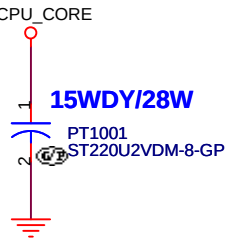

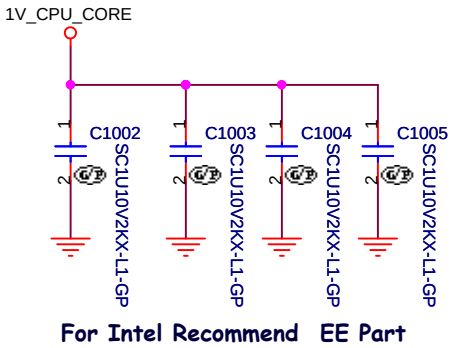

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Title: CPU (Power CAP1)

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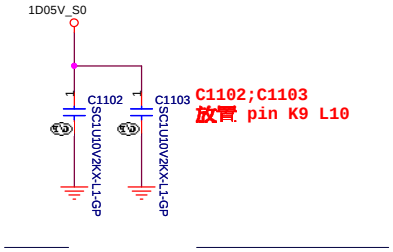
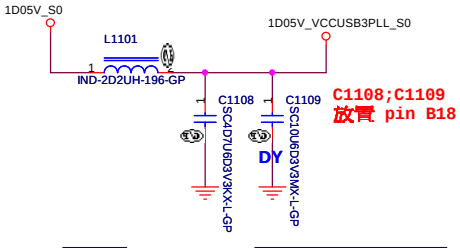
擺放電容的位置請參考 Page 21,每個位置如下

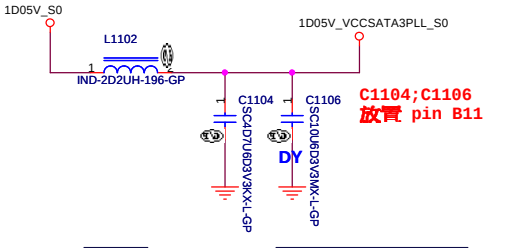
MAX: 3.074A



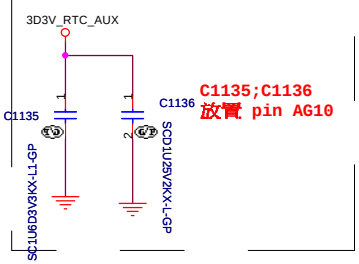
C1102;C1103
放置 pin K9 L10



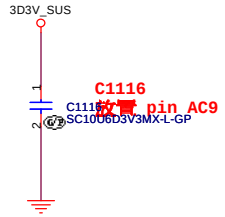
C1108;C1109
放置 pin B18



C1104;C1106
放置 pin B11

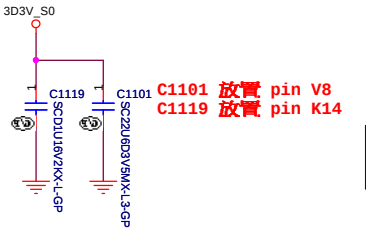


C1135;C1136
放置 pin AG10

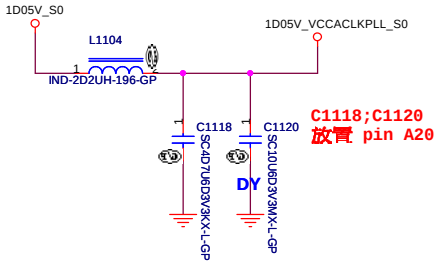


C1116
放置 pin AC9

MAX: 0.285A

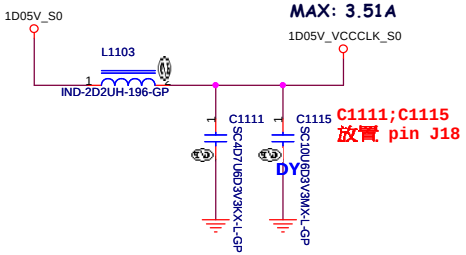


C1101 放置 pin V8
C1119 放置 pin K14

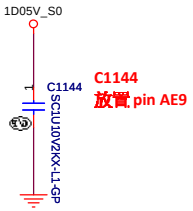


C1118;C1120
放置 pin A20

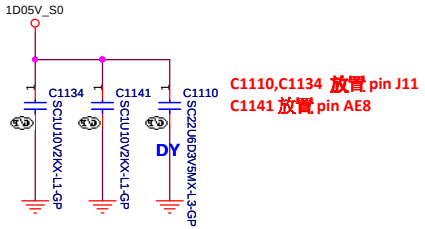
MAX: 3.51A



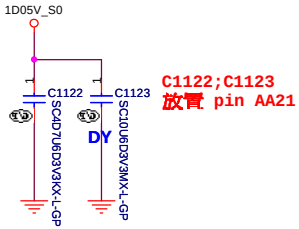
C1111;C1115
放置 pin J18



C1144
放置 pin AE9



C1110,C1134 放置 pin J11
C1141 放置 pin AE8



C1122;C1123
放置 pin AA21

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Title: CPU (Power CAP2)

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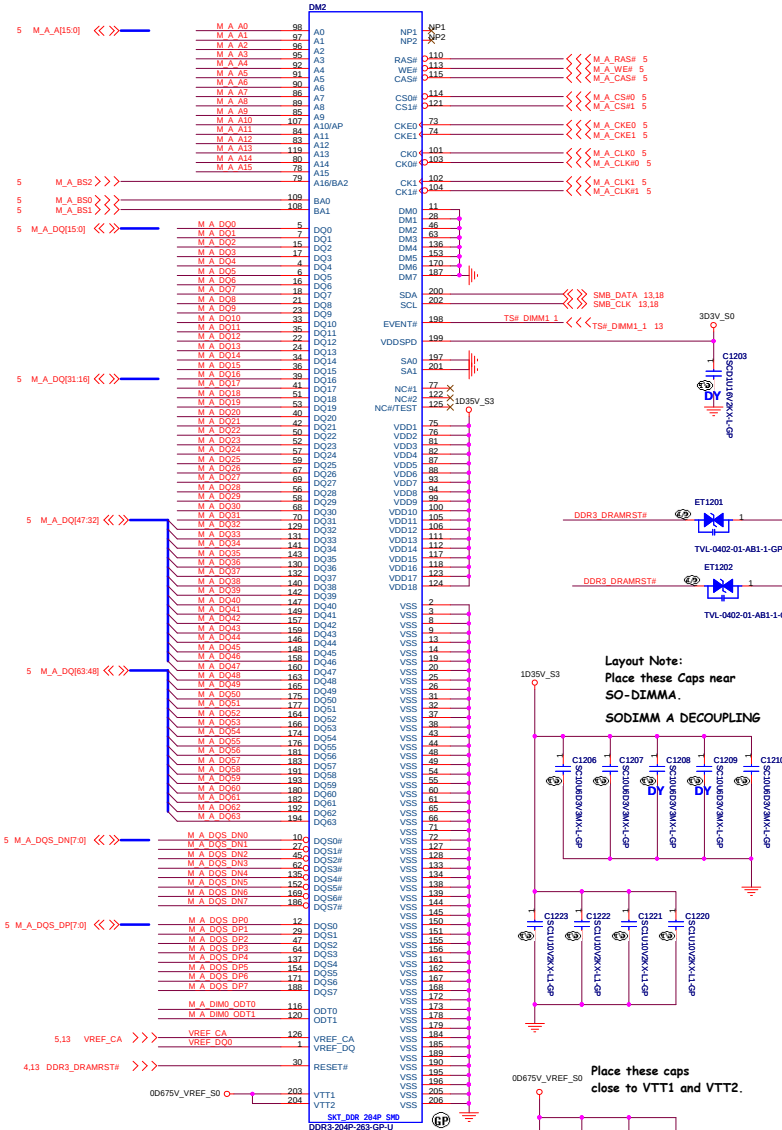
SSID = MEMORY

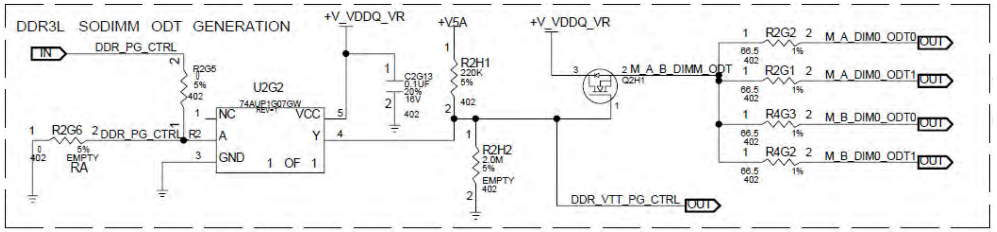


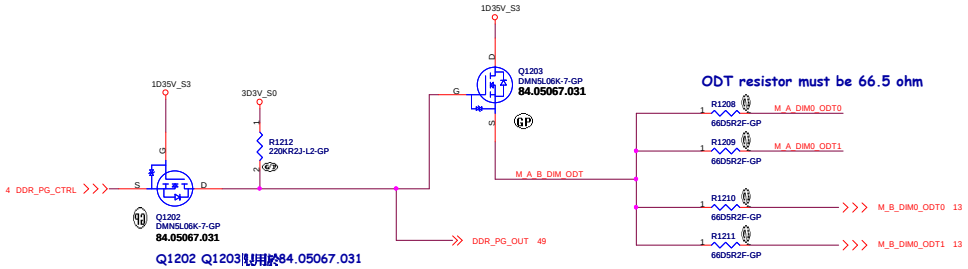
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

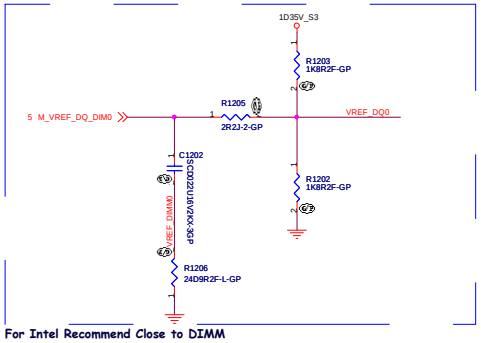
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

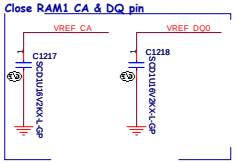
SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.









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Title: ***DDR3-SODIMM1***

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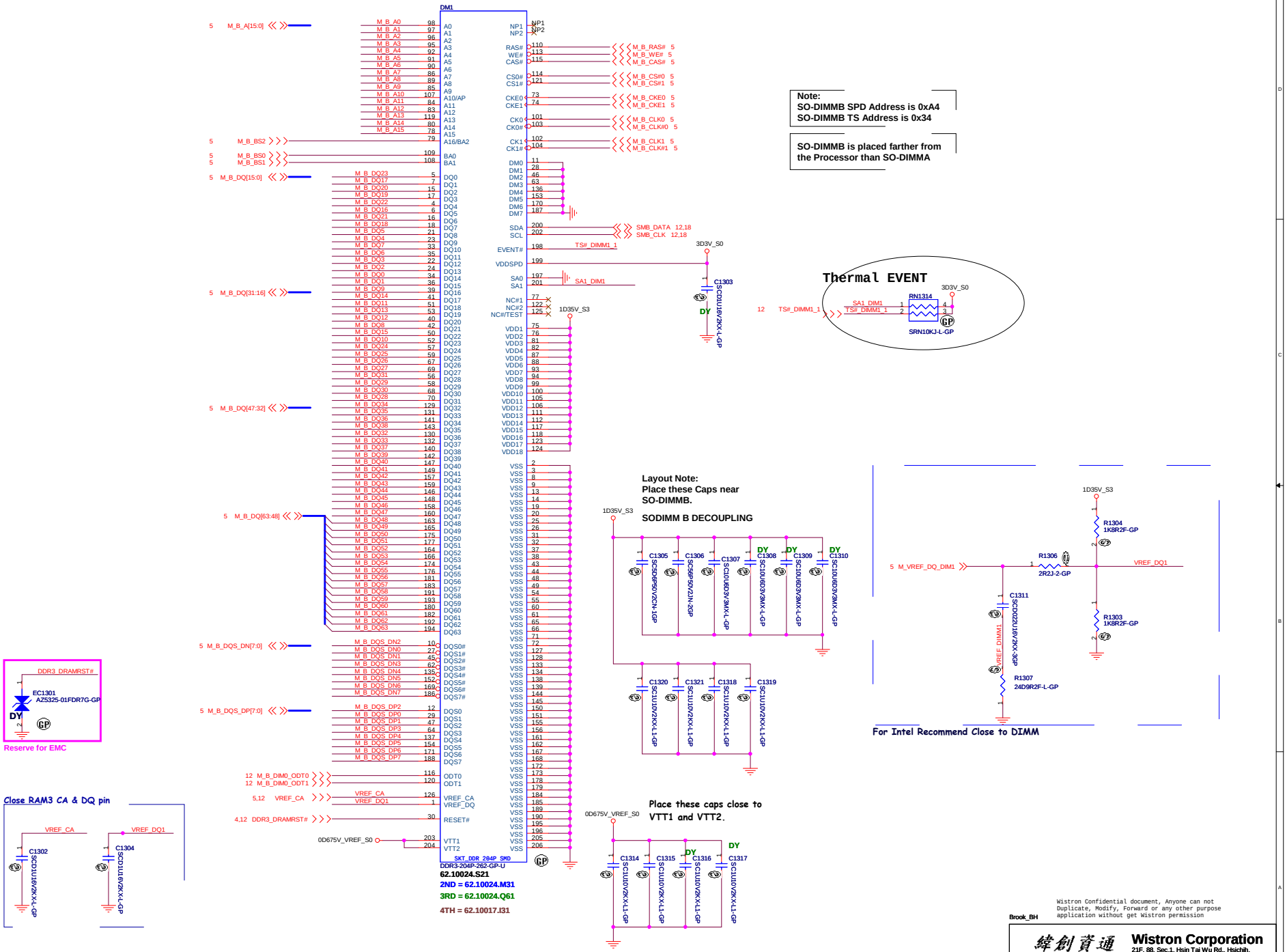
SSID = MEMORY



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Title: DDR3-SODIMM2

Size: Custom | Document Number: Brook_BH | Rev: -1M

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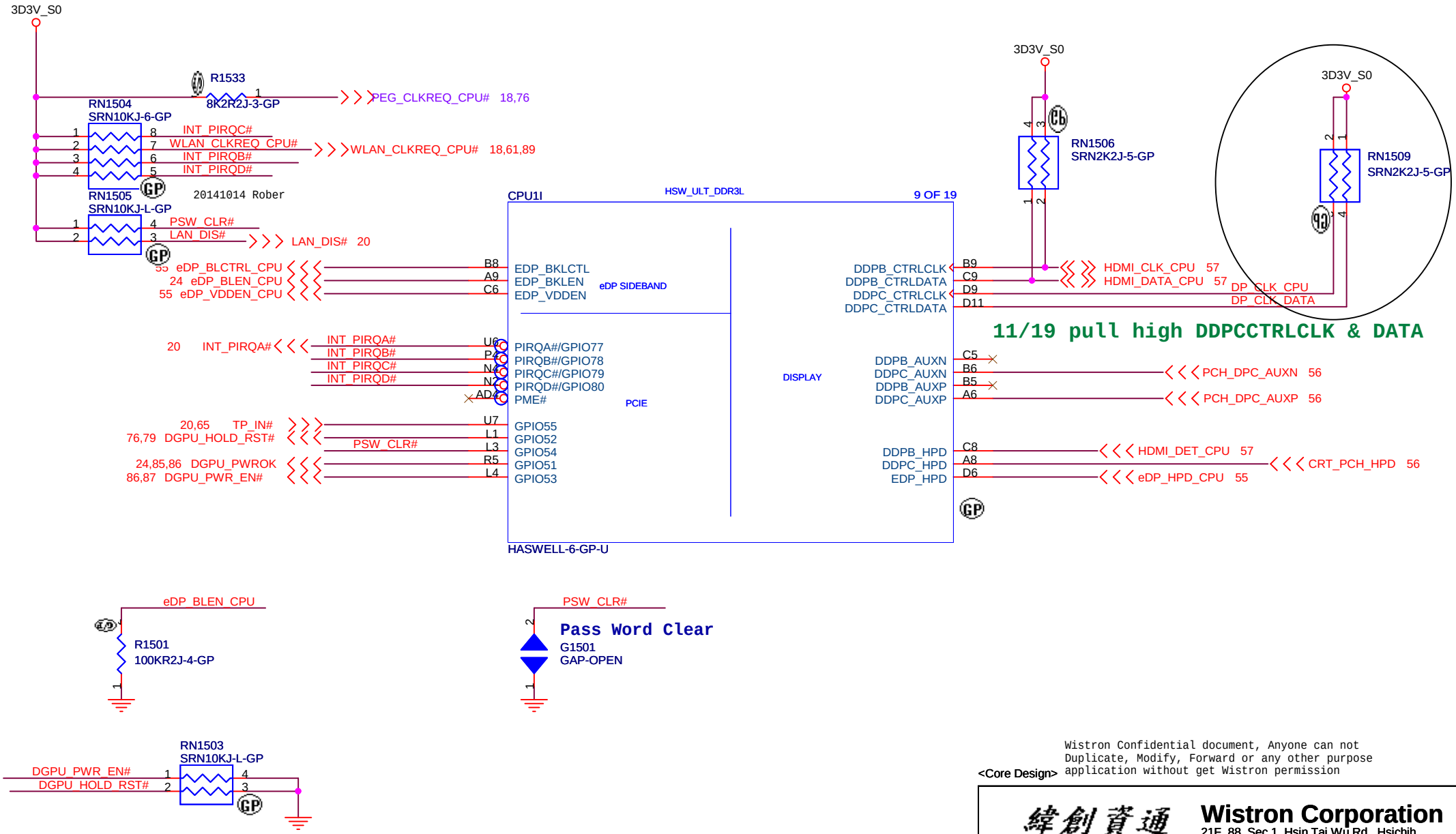

<Core Design>

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Title	***CPU(EDP SIDEBAND/GPIO/DDI)***	
Size A4	Document Number **Brook_BH**	Rev **-1M**
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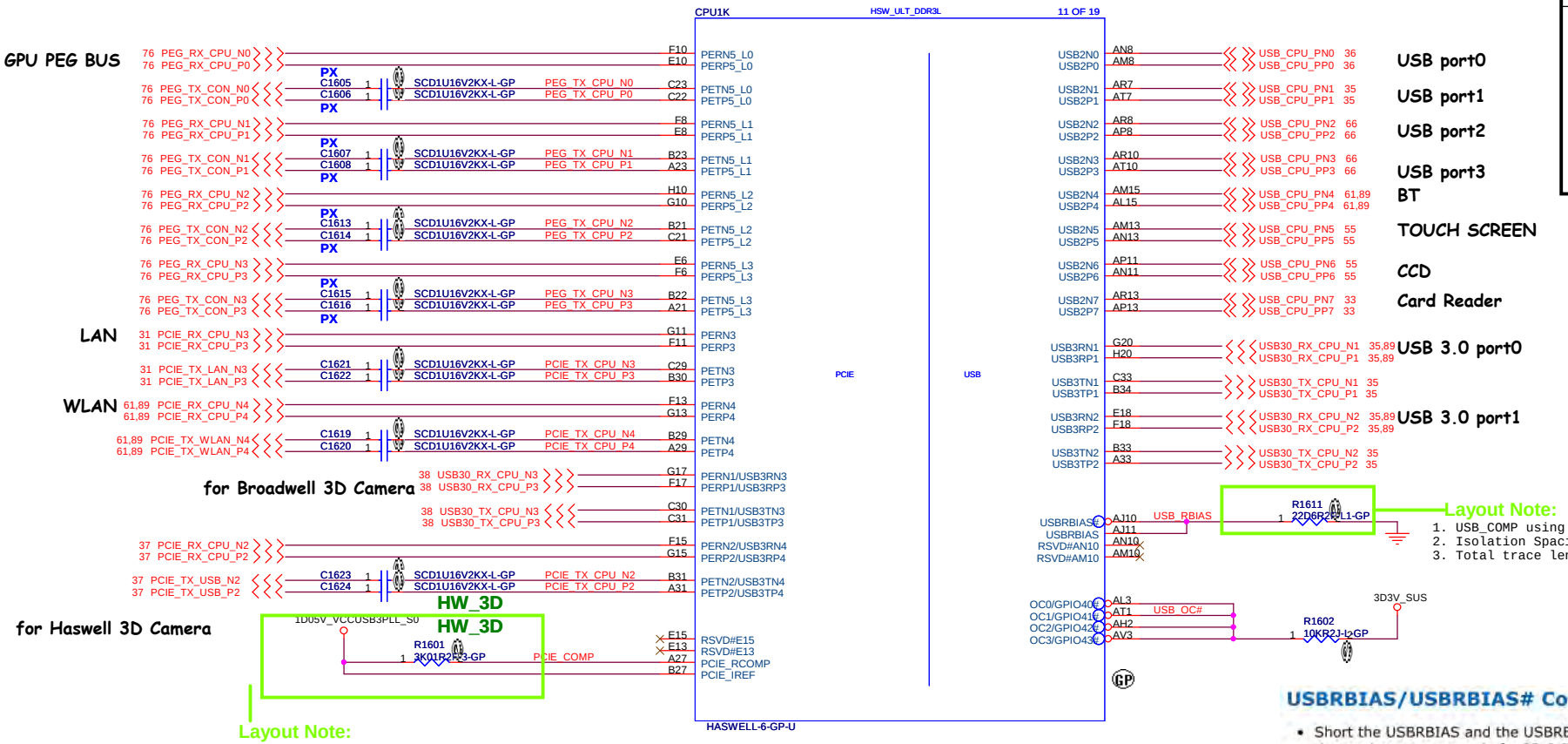

USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port2
3	USB3.0 Port3
4	BT
5	TOUCH SCREEN
6	CCD
7	Card Reader

USB port0
USB port1
USB port2
USB port3
BT
TOUCH SCREEN
CCD
Card Reader
USB 3.0 port0
USB 3.0 port1

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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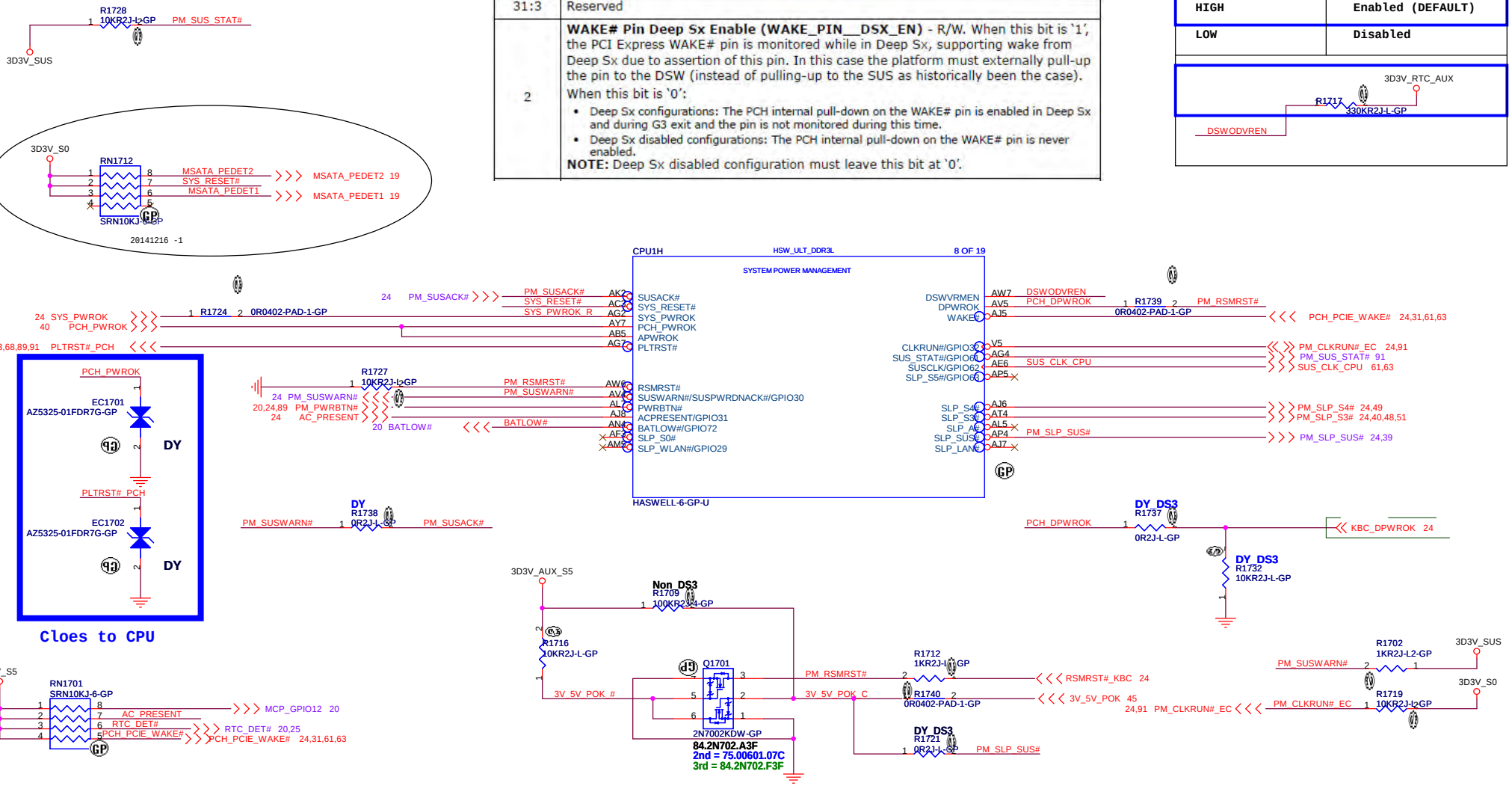
Title: **CPU (PCI/USB)**

Size: A3 | Document Number: **Brook_BH** | Rev: **-1M**

Date: Wednesday, February 04, 2015 | Sheet 16 of 106

Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



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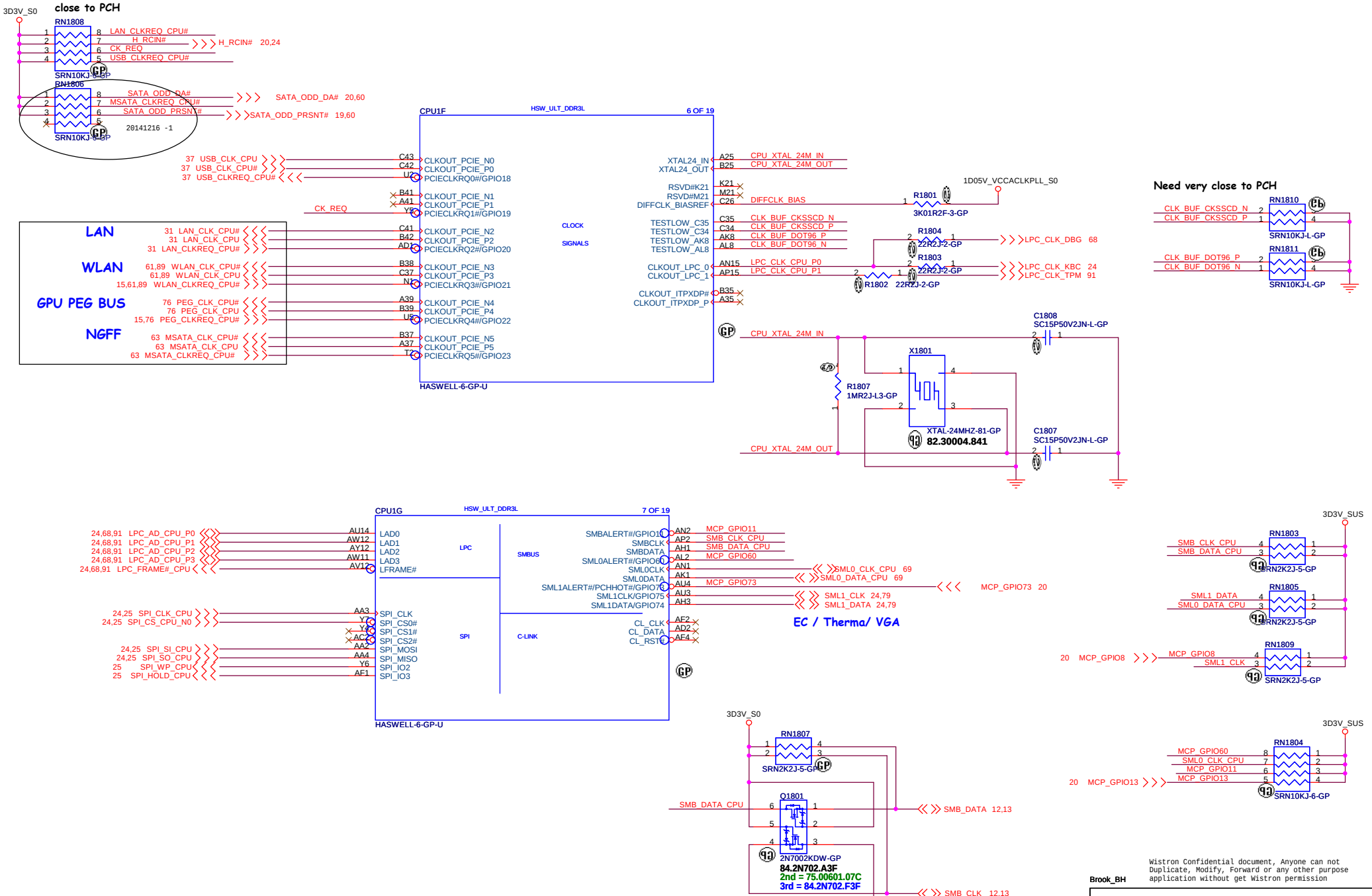
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DMI/FDI/PM)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 17 of 106



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PCI-E/SMBUS/CLOCK/CL)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 18 of 106

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

3D3V_RTC_AUX
R1928 20KR2F-L3-GP
R1927 20KR2F-L3-GP
C1903 SC1U6D3V3KX-L1-GP
EC1902 AZ5325-01F7G-GP DY
EC1901 AZ5325-01FDR7G-GP DY
C1904 SC1U6D3V3KX-L1-GP
Cloes to CPU
RTC Reset
G1901 GAP-OPEN

3D3V_RTC_AUX
R1904 1M1R2J-GP
R1905 330KR2F-L-GP
CPU_XTAL_32K_X1
CPU_XTAL_32K_X2
SM_INTRUDER#
PCH_INTVRMEN
SRTC_RST#
RTC_RST#

CPU1E HSW_ULT_DDR3L 5 OF 19
RTCX1 AW5
RTCX2 AY5
INTRUDER# AU6
INTVRMEN AV7
SRTCRST# AV8
RTCRST# AU7
RTC

HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_RST#_CPU
27 HDA_SDIN0_CPU
24 ME_UNLOCK
R1908 1KR2J-L2-GP
HDA_SDOUT_CPU
HDA_BCLK/I2S0_SCLK AW8
HDA_SYNC/I2S0_SFRM AV11
HDA_RST#/I2S_MCLK# AU9
HDA_SDI0/I2S0_RXD AY10
HDA_SDI1/I2S1_RXD AU12
HDA_SDO/I2S0_TXD AU11
HDA_DOCK_EN#/I2S1_TXD# AW10
HDA_DOCK_RST#/I2S1_SFRM# AV12
I2S1_SCLK AY8
AUDIO

PCH_TRST# AU62
PCH_TCK AE62
PCH_TDI AD61
PCH_TDO AE61
PCH_TMS AD62
RSVD#AL11 AL11
RSVD#AC4 AC4
JTAGX AE63
RSVD#AV2 AV2
JTAG

SATA_RN0/PERN6_L3 J5
SATA_RP0/PERP6_L3 H5
SATA_TN0/PETN6_L3 B15
SATA_TP0/PETP6_L3 A15
SATA_RX_CPU_N0 60
SATA_RX_CPU_P0 60
SATA_TX_CPU_N0 60
SATA_TX_CPU_P0 60
SATA HDD

SATA_RN1/PERN6_L2 J8
SATA_RP1/PERP6_L2 H8
SATA_TN1/PETN6_L2 A17
SATA_TP1/PETP6_L2 B17
SATA_RX_CPU_N1 60
SATA_RX_CPU_P1 60
SATA_TX_CPU_N1 60
SATA_TX_CPU_P1 60
SATA ODD

SATA_RN2/PERN6_L1 J6
SATA_RP2/PERP6_L1 H6
SATA_TN2/PETN6_L1 B14
SATA_TP2/PETP6_L1 C15
PCIE_RX_CPU_N6 63
PCIE_RX_CPU_P6 63
PCIE_TX_CPU_N6 63
PCIE_TX_CPU_P6 63

SATA_RN3/PERN6_L0 F5
SATA_RP3/PERP6_L0 E5
SATA_TN3/PETN6_L0 C17
SATA_TP3/PETP6_L0 D17
SATA_RX_CPU_N3 63
SATA_RX_CPU_P3 63
SATA_TX_CPU_N3 63
SATA_TX_CPU_P3 63
NGFF SSD

SATA0GP/GPIO34 V1 MCP_GPIO34
SATA1GP/GPIO35 U1
SATA2GP/GPIO36 V6 MSATA_PEDET1
SATA3GP/GPIO37 AC1 MSATA_PEDET2
SATA_ODD_PRSNT# 18,60
MSATA_PEDET1 17
MSATA_PEDET2 17
1D05V_VCCSATA3PLL_S0
SATA_IREF A12
RSVD#L11 L11
RSVD#K10 K10
SATA_RCOMP C12
SATALED# U3
R1926 3K01R2F-3-GP
SATA

3D3V_S0
R1932 10KR2J-L-GP MCP_GPIO34
R1929 10KR2J-L-GP INT_SERIRQ 20,24,91

CPU_XTAL_32K_X1
R1901 10MR2J-L-GP
CPU_XTAL_32K_X2
X1901 XTAL-32D768KHZ-64-GP
82.30001.661
2nd = 82.30001.B21
C1901 SC5P50V2CN-2GP
C1902 SC5P50V2CN-2GP

27 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
RN1901 SRN33J-5-GP-U
HDA_SDOUT_CPU
HDA_SYNC_CPU

27 HDA_RST#_CODEC
27 HDA_BITCLK_CODEC
RN1903 SRN33J-5-GP-U
HDA_RST#_CPU
HDA_BITCLK_CPU

For AFR

RTC_RST#
Q1903 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

24 RTCRST_ON
RTC_RST#_R
R1918 100KR2J-4-GP
R1921 2K2R2J-L1-GP

M.2 auto detection
Q1902 2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C
Baseline
63 MSATA_PEDET
MSATA_PEDET2
MSATA_PEDET1
MSATA_PEDET 63

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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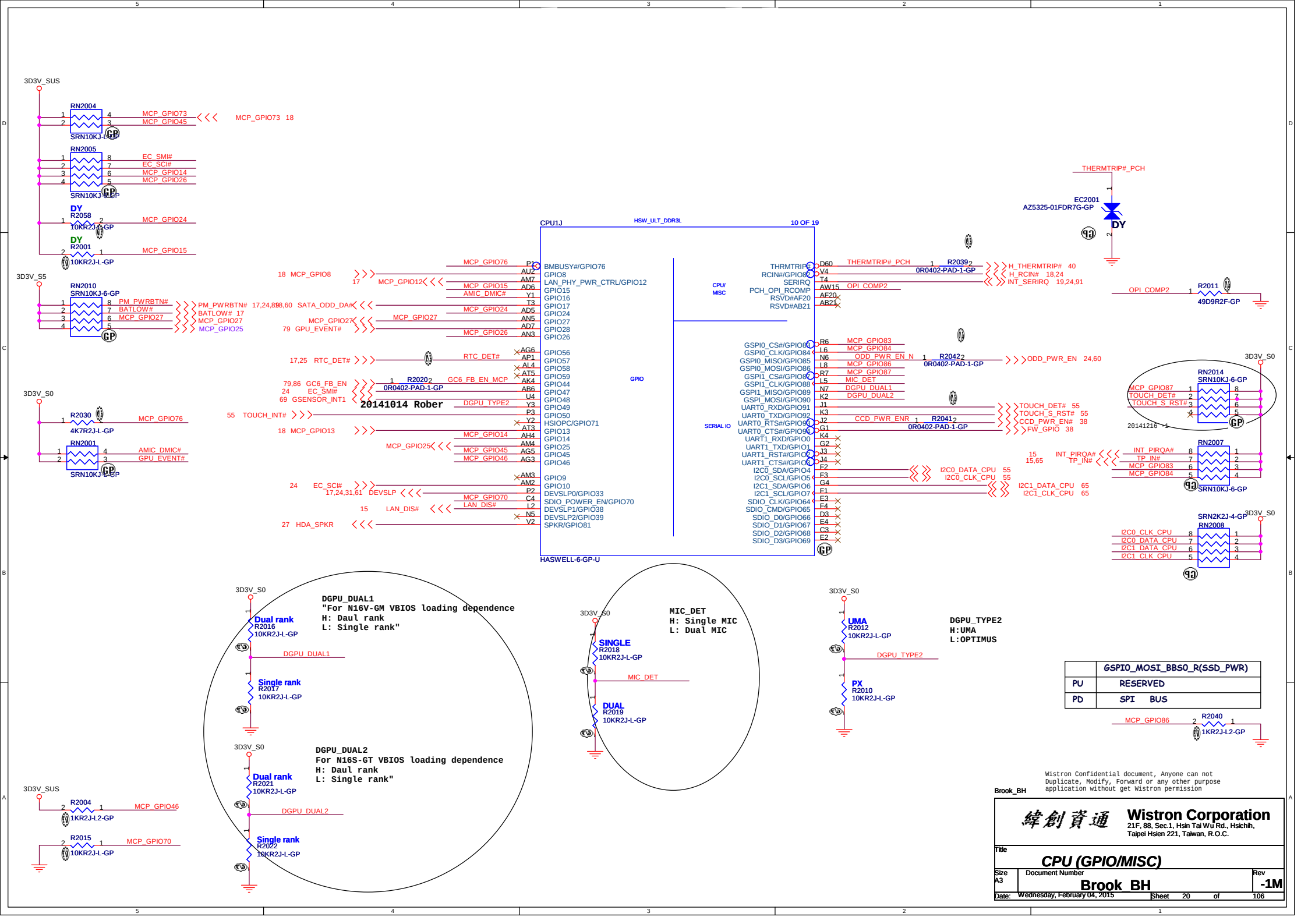
Title: CPU (RTC/LPC/SATA/HDA)
Size: Custom | Document Number: Brook_BH | Rev: -1M
Date: Wednesday, February 04, 2015 | Sheet 19 of 106


3D3V_SUS
RN2004
MCP_GPIO73
MCP_GPIO45
SRN10KJ-L-GP
RN2005
EC_SMI#
EC_SCI#
MCP_GPIO14
MCP_GPIO26
DY
R2058
10KR2J-L-GP
MCP_GPIO24
R2001
MCP_GPIO15
3D3V_S5
RN2010
SRN10KJ-6-GP
PM_PWRBTN#
BATLOW#
MCP_GPIO27
MCP_GPIO25
3D3V_S0
R2030
4K7R2J-L-GP
MCP_GPIO76
RN2001
AMIC_DMIC#
GPU_EVENT#
CPU1J
HSW_ULT_DDR3L
10 OF 19
BMBUSY#/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81
GPIO
CPU MISC
THRMTRIP#
RCIN#/GPIO80
SERIRQ
PCH_OPI_RCOMP
RSVD#AF20
RSVD#AB21
SERIAL IO
GSPI0_CS#/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85
GSPI0_MOSI/GPIO86
GSPI1_CS#/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS#/GPIO93
UART0_CTS#/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST#/GPIO2
UART1_CTS#/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
HASWELL-6-GP-U
THERMTRIP#_PCH
EC2001
AZ5325-01FDR7G-GP
R2039
0R0402-PAD-1-GP
H_THERMTRIP# 40
H_RCIN# 18,24
INT_SERIRQ 19,24,91
OPI_COMP2
R2011
49D9R2F-GP
R2042
ODD_PWR_EN 24,60
R2041
TOUCH_DET# 55
TOUCH_S_RST# 55
CCD_PWR_EN# 38
FW_GPIO 38
I2C0_DATA_CPU 55
I2C0_CLK_CPU 55
I2C1_DATA_CPU 65
I2C1_CLK_CPU 65
RN2014
SRN10KJ-6-GP
RN2007
SRN10KJ-6-GP
SRN2K2J-4-GP
RN2008
R2020
GC6_FB_EN_MCP
20141014 Rober
DGPU_TYPE2
RTC_DET#
TOUCH_INT#
EC_SCI#
DEVSLP
LAN_DIS#
HDA_SPKR
DGPU_DUAL1
"For N16V-GM VBIOS loading dependence
H: Daul rank
L: Single rank"
Dual rank
R2016
10KR2J-L-GP
Single rank
R2017
10KR2J-L-GP
DGPU_DUAL2
For N16S-GT VBIOS loading dependence
H: Daul rank
L: Single rank"
R2021
10KR2J-L-GP
R2022
10KR2J-L-GP
MIC_DET
H: Single MIC
L: Dual MIC
SINGLE
R2018
10KR2J-L-GP
DUAL
R2019
10KR2J-L-GP
DGPU_TYPE2
H:UMA
L:OPTIMUS
UMA
R2012
10KR2J-L-GP
PX
R2010
10KR2J-L-GP
GSPIO_MOSI_BBSO_R(SSD_PWR)
PU
RESERVED
PD
SPI BUS
R2040
1KR2J-L2-GP
R2004
1KR2J-L2-GP
MCP_GPIO46
R2015
10KR2J-L-GP
MCP_GPIO70
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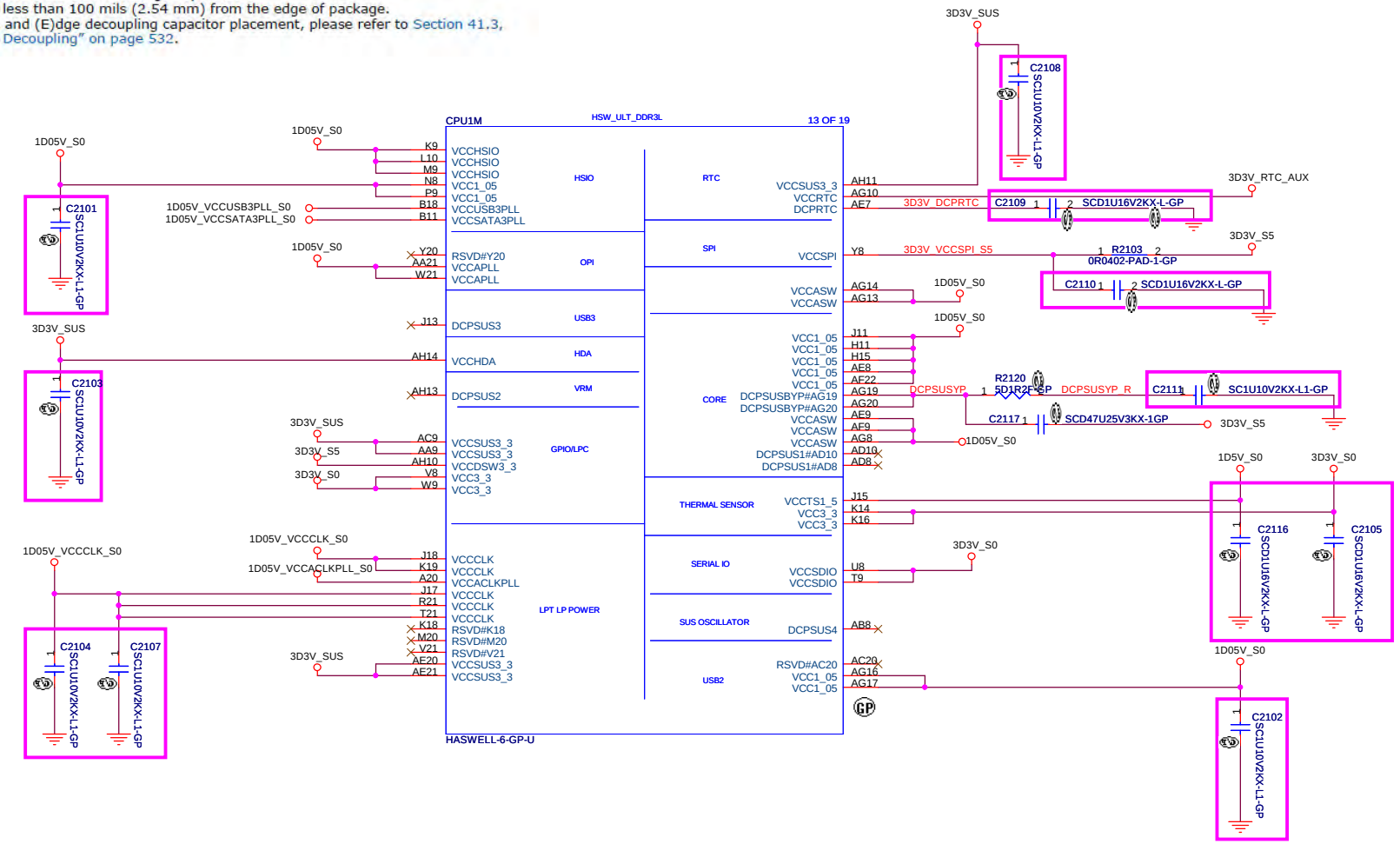
Title
CPU (GPIO/MISC)
Size A3
Document Number
Brook_BH
Rev -1M
Date: Wednesday, February 04, 2015
Sheet 20 of 106

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



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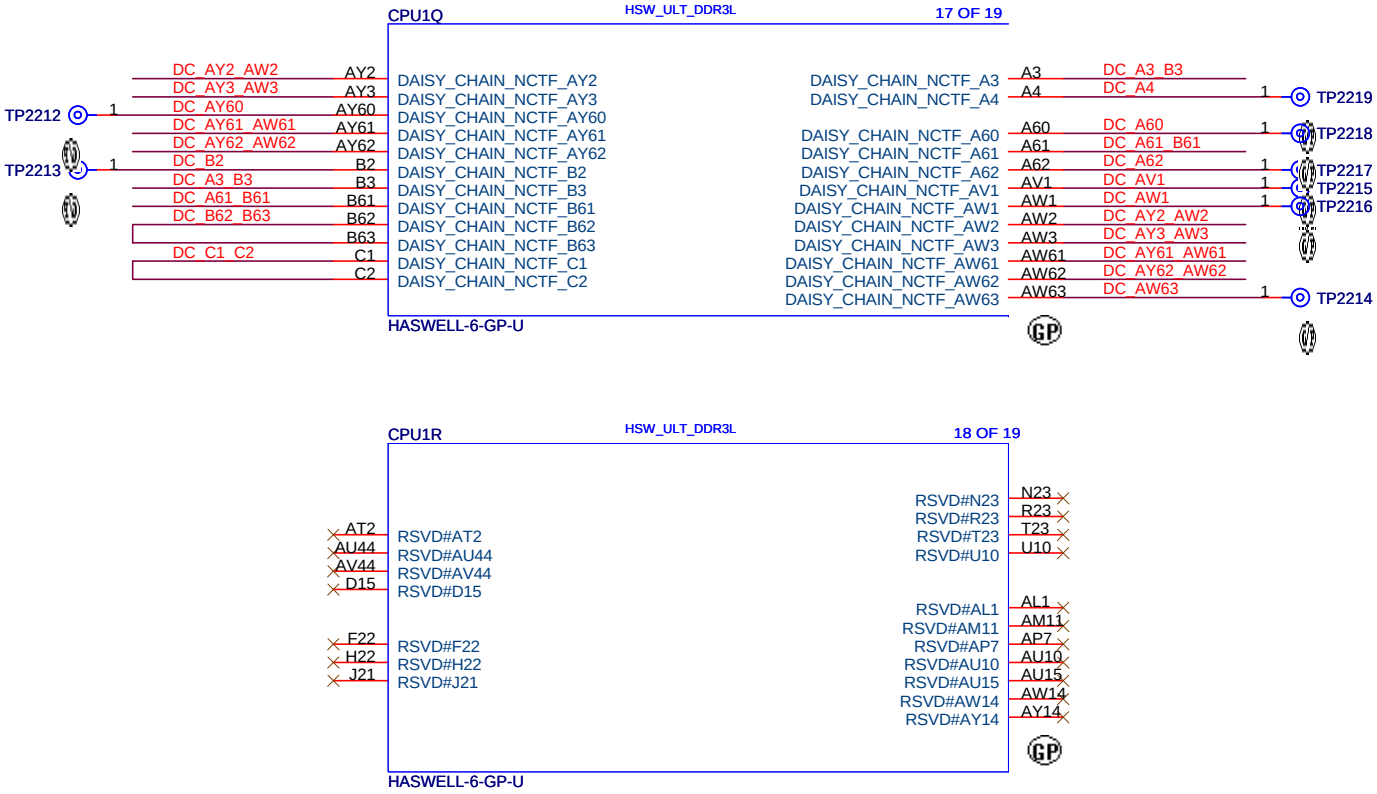
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 21 of 106



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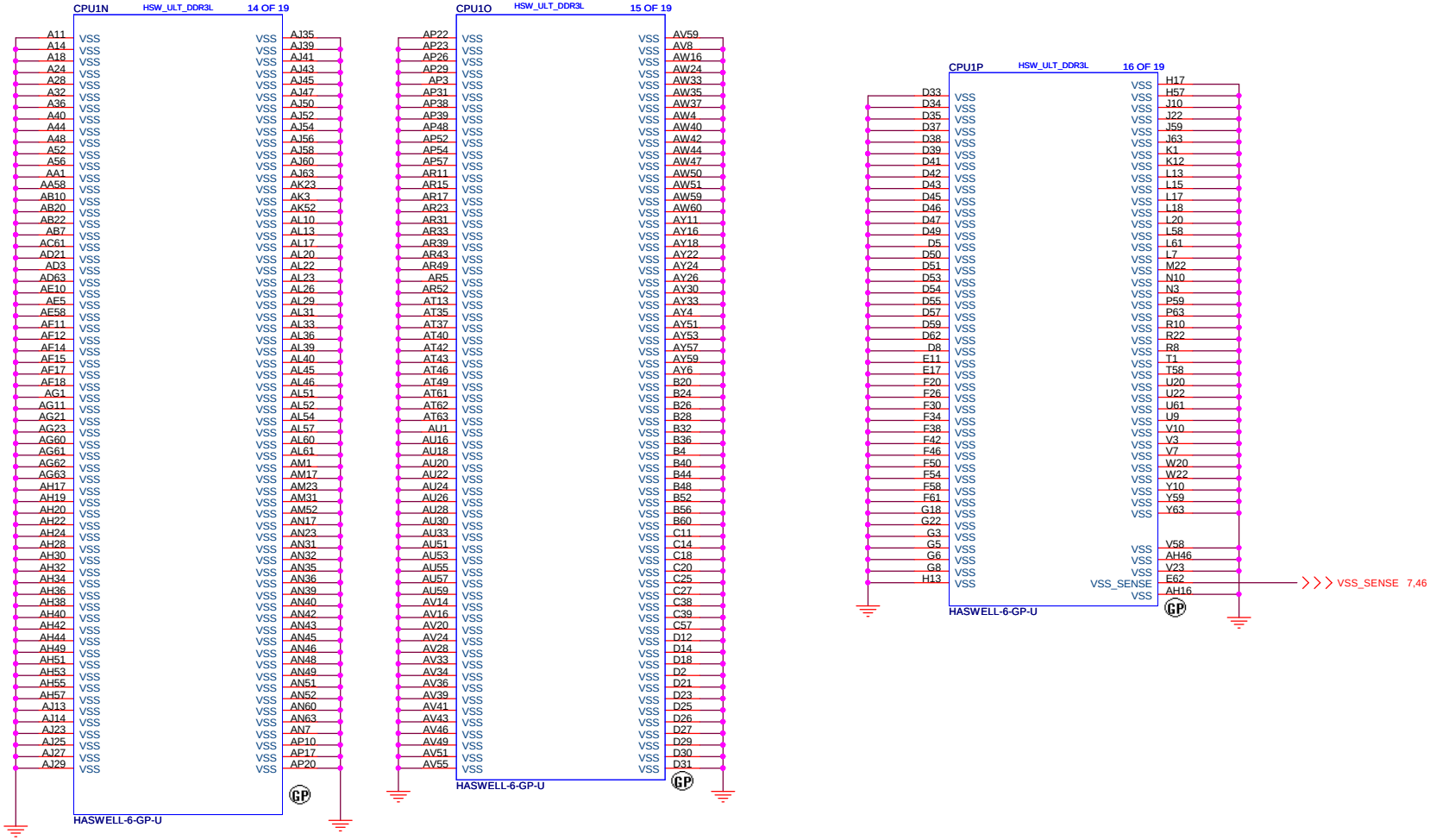
Title: ***CPU (RSVD)***

Size	Document Number	Rev
Custom	Brook_BH	-1M
Date: Wednesday, February 04, 2015	Sheet 22 of 106	



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 23 of 106

SSID = KBC

Close to the EC

11/18 RN7904 to RN2404

VCC_LPC(Pin9)

OPMODE (Pin70)

< ---CPU/GPU

< ---BATTER /CHARGER

< ---Touch Pad

20141014 Rober

Rober change 11/17

GPIO0 High Active

2ND = 84.T3906.E11

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Brook_H_UMA/Brook_SL_UMA	100.0 K	10.0 K	3.000 V
Brook_H_DIS/Brook_SL_DIS	100.0 K	20.0 K	2.750 V
Brook_B_UMA	100.0 K	33.0 K	2.481 V
Brook_B_DIS	100.0 K	47.0 K	2.245 V
Reserved for project use	100.0 K	64.9 K	2.001 V
Reserved for project use	100.0 K	76.8 K	1.867 V
Reserved for project use	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
33W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.818 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

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Title: KBC_KB9038

Size: A2 | Document Number: Brook_BH | Rev: -1M

Date: Thursday, February 12, 2015 | Sheet 24 of 106

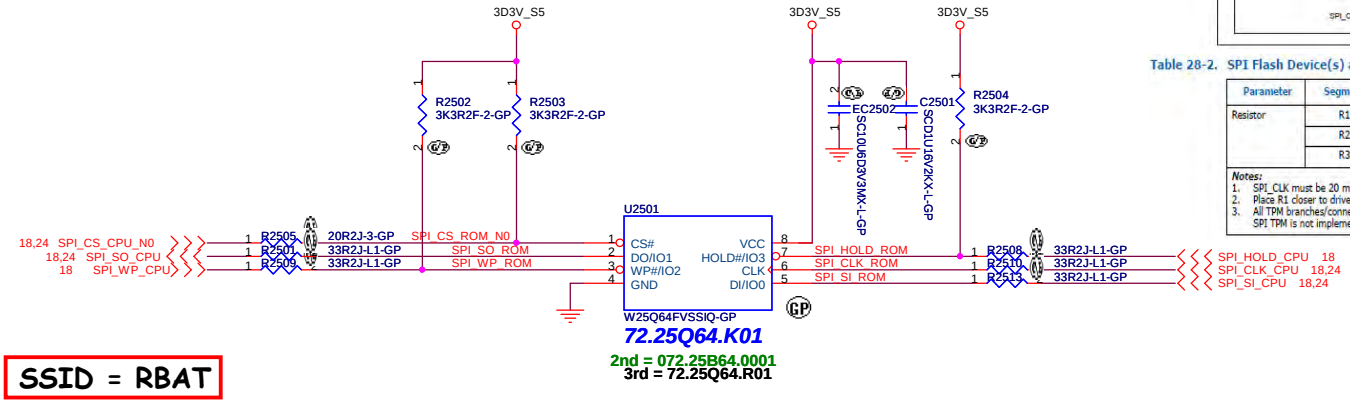
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)
1ST= 072.02564.0001(AMIC A25LQ64M)
2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
72.25647.00A (MXIC MX25L6473EM2I)



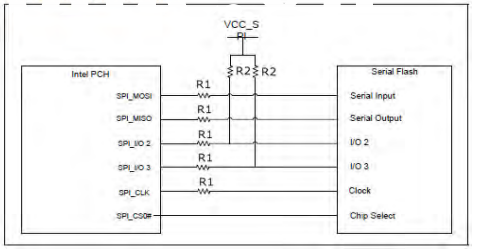
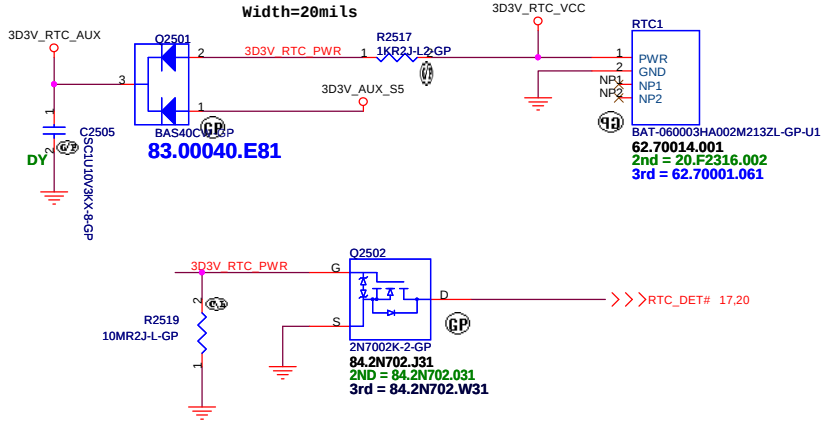


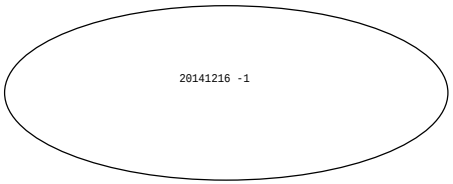
Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

Notes:
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC if SPI TPM is not implemented.

SSID = RBAT





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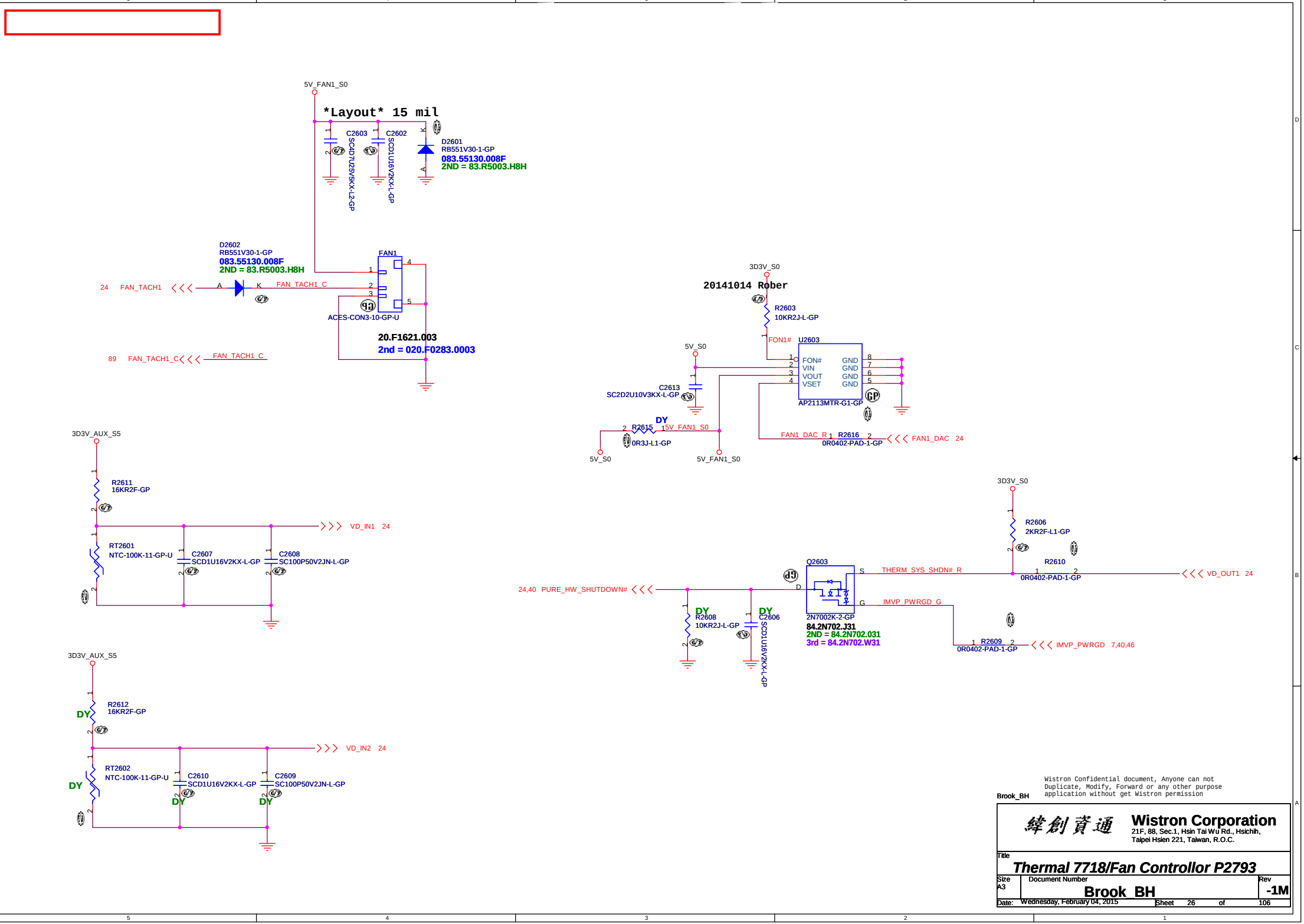
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 25 of 106



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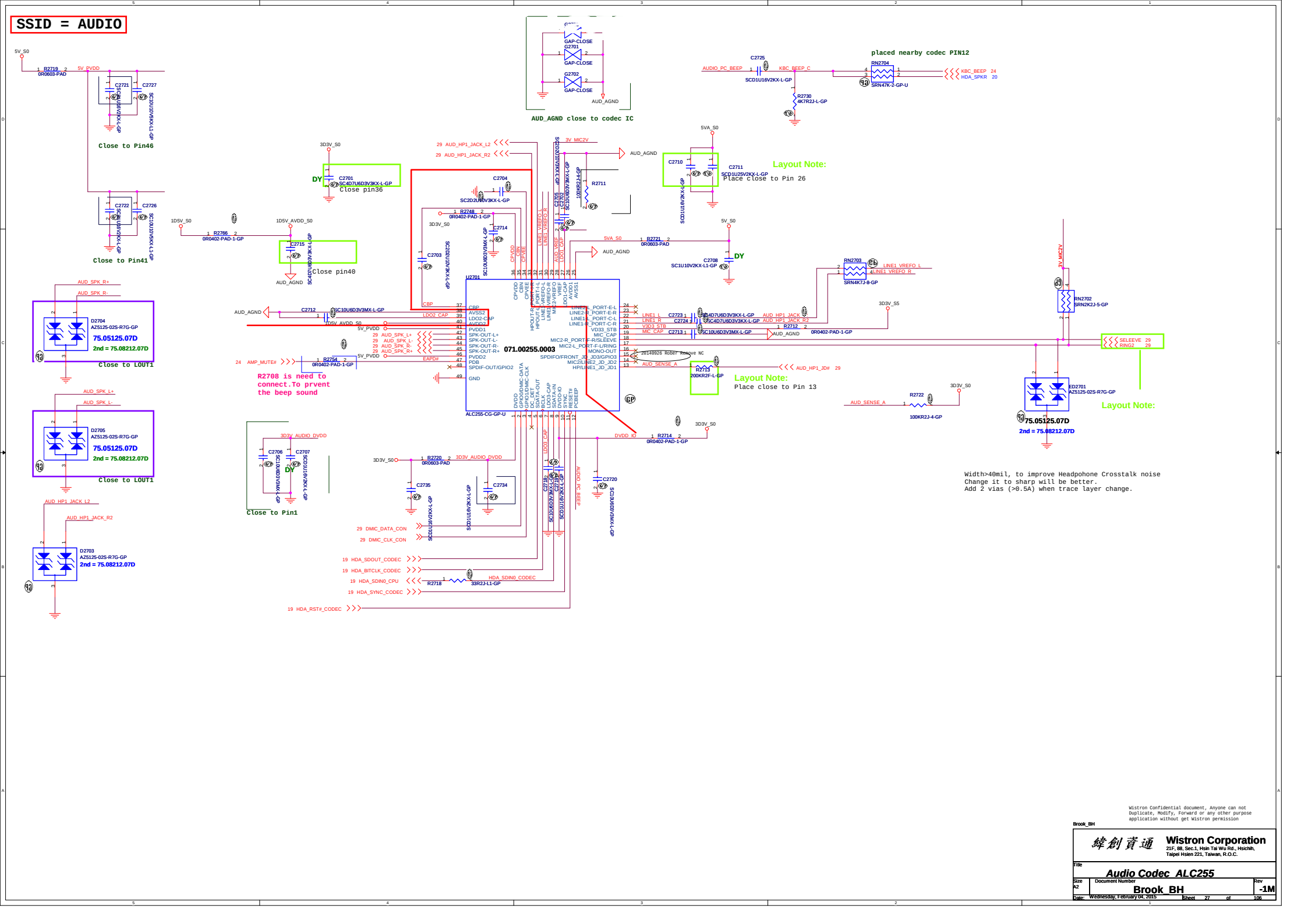
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal 7718/Fan Controllor P2793***

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 26 of 106

SSID = AUDIO



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC255**

Size	Document Number	Rev
A2	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 27 of 106

SSID = AUDIO

Speaker

27 AUD_SPK_L-
27 AUD_SPK_L+
27 AUD_SPK_R-
27 AUD_SPK_R+

EL2914 1 BLM15PX121SN1D-GP
EL2915 1 BLM15PX121SN1D-GP
EL2916 1 BLM15PX121SN1D-GP
EL2917 1 BLM15PX121SN1D-GP

AUD_SPK1_L- _CON
AUD_SPK1_L+ _CON
AUD_SPK1_R- _CON
AUD_SPK1_R+ _CON

SPK*
20.F1621.004
2nd = 020.F0155.0004

EC2901 1 SC1KP50V2KX-L-1-GP
EC2902 1 SC1KP50V2KX-L-1-GP
EC2915 1 SC1KP50V2KX-L-1-GP
EC2920 1 SC1KP50V2KX-L-1-GP

ES-CON4-17-GP-U1

AUD_SPK1_L-_CON 89
AUD_SPK1_L+_CON 89
AUD_SPK1_R-_CON 89
AUD_SPK1_R+_CON 89

AFTP TESTPOINT

Layout Note:
Trace width=40mil

Combo Jack

R2910 1 2 0R0402-PAD-1-GP
AUD_HP1_JD#_R
Q2901
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
AUD_HP1_JD# 27
C2902
R2901 100KR2J-4-GP
SC10U6D3V3MX-L-GP
AUD_AGND

3D3V_S0
R2905 10KR2J-L-GP
AUD_HP1_JD#_TYPE
R2906 0R0402-PAD-1-GP
AUD_AGND
0527_SB

27 RING2
27 AUD_HP1_JACK_L2
27 AUD_HP1_JACK_R2
27 SELEEVE

R2920 1 0R0402-PAD-1-GP
ER2913 1 33D4R3F-GP
20141216 -1
ER2912 1 33D4R3F-GP
R2921 1 0R0402-PAD-1-GP

RING2_R
AUD_HP1_JACK_L1
AUD_HP1_JD#_TYPE
AUD_HP1_JD#_R
AUD_HP1_JACK_R1
SELEEVE_R
MS

AUD1
Audio(IP/NK comb)
AUDIO-JK506-GP-U

EC2923 1 2 SC22P50V2JN-L-GP
EC2921 1 SC22P50V2JN-L-GP
EC2922 1 SC22P50V2JN-L-GP
EC2912 1 SC22P50V2JN-L-GP
EC2913 1 SC22P50V2JN-L-GP
EC2914 1 SC22P50V2JN-L-GP
AUD_AGND

022.10002.0951

AUD_HP1_JD#_R 89
AUD_HP1_JACK_R1 89
AUD_HP1_JACK_L1 89
RING2_R 89
SELEEVE_R 89
AUD_HP1_JD#_TYPE 89

AFTP TESTPOINT

DUAL
SINGLE
R2917 1 0R2J-L-GP
R2916 1 0R2J-L-GP
20141216 -1
DUAL/SINGAL
DMIC_DATA_R

MIC2
ENHANCE
CS
GND
VDD
DATA
CLK
DMIC_DATA_CON_R
DMIC_CLK_CON_R
3D3V_S0
MICROPHONE-105-GP-U
082.40011.0001

MIC1
DUAL
DMIC_DATA_R1
DMIC_CLK_CON_R1
MICROPHONE-105-GP-U
082.40011.0001

DMIC_CLK_CON_R
DMIC_DATA_CON_R
DMIC_CLK_CON_R1
R2909 1 2 0R0402-PAD-1-GP DMIC_CLK_CON 27
R2911 1 2 0R0402-PAD-1-GP DMIC_DATA_CON 27
0R2J-L-GP
R2912 DMIC_CLK_CON
DY DY DY
DUAL
EC2903 EC2904 EC2905
SC4D7P50V2BN-GP

DMIC_DATA_R
SINGLE
R2919 0R2J-L-GP

DMIC_DATA_R1
0R2J-L-GP
R2913 DMIC_DATA_R
DY
EC2906
SC4D7P50V2BN-GP
DUAL

DUAL MIC=082.40011.0001
SINGALE MIC=082.40011.0011
Single MIC 2nd=082.40002.0031

CLK_CON_MIC3
DATA_CON_MIC3
DY DY
EC2908 EC2907
SC4D7P50V2BN-GP

MIC3
3D3V_S0
CLK_CON_MIC3
DATA_CON_MIC3
R2914 1 2 0R0402-PAD-1-GP DMIC_CLK_CON 27
R2915 1 2 0R0402-PAD-1-GP DMIC_DATA_CON 27
PTWO-CON4-9-GP-U1
DY

11/30 SB

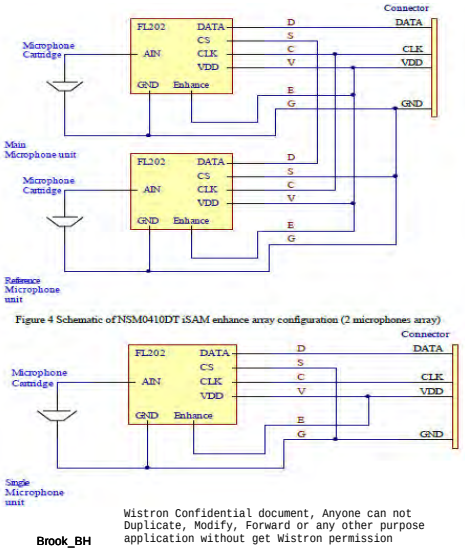
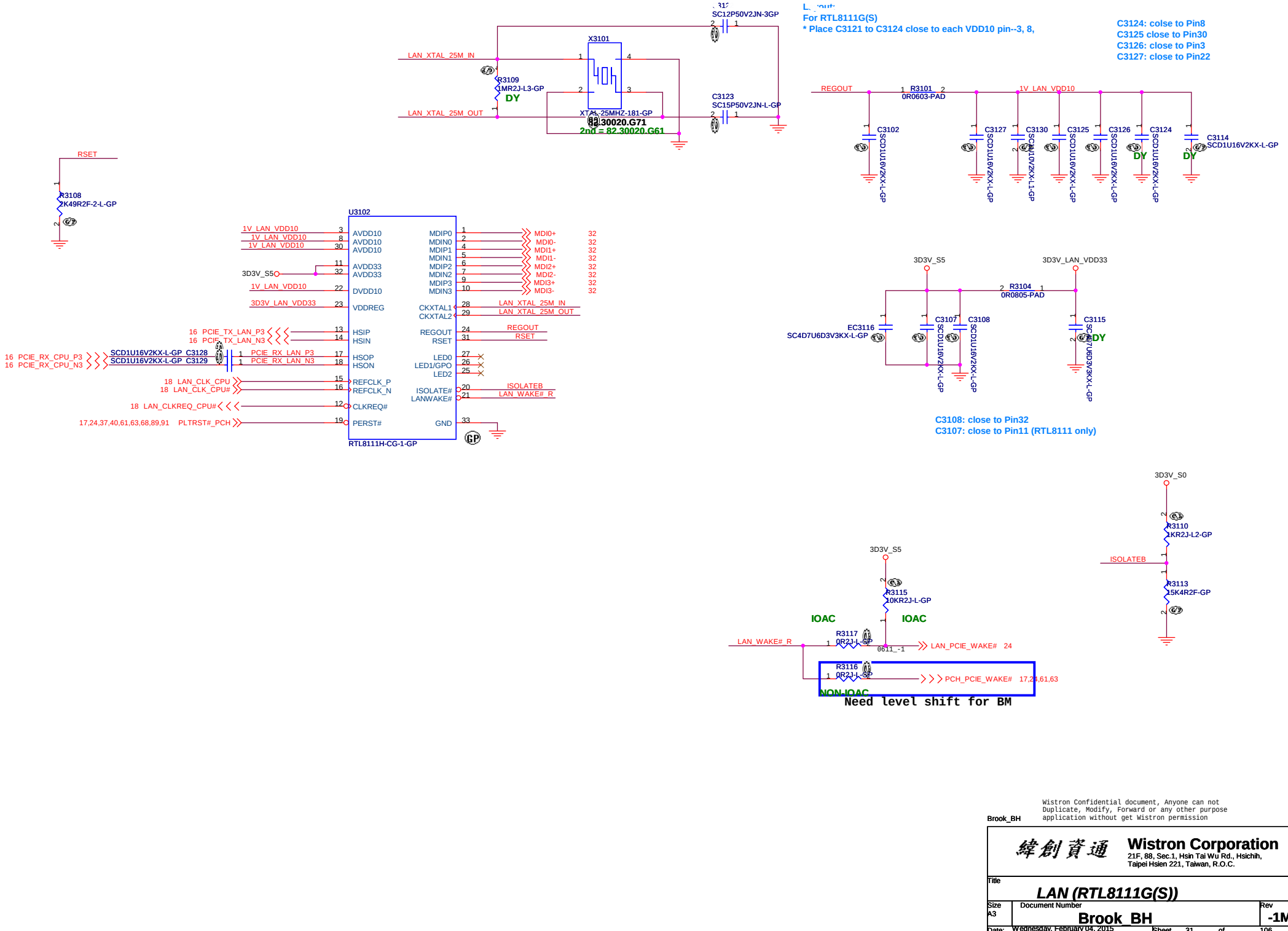


Figure 4 Schematic of NSM0410DT iSAM enhance array configuration (2 microphones array)

Brook_BH

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack
Size: A3
Document Number: Brook BH
Rev: -1M
Date: Thursday, February 12, 2015
Sheet 29 of 106



Brook_BH

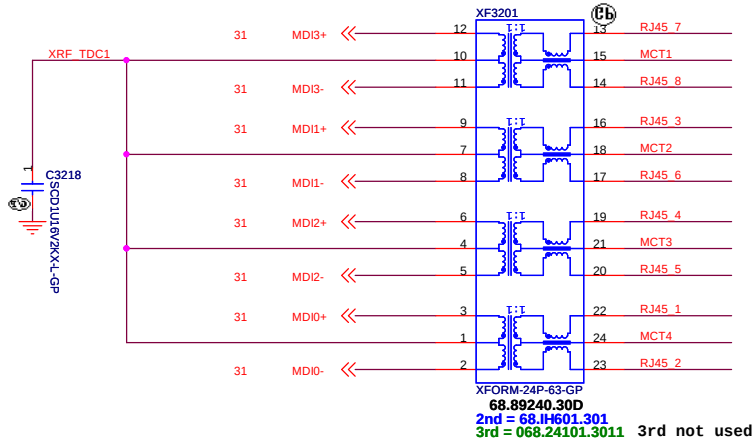
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN (RTL8111G(S))**

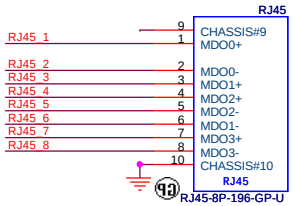
Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 31 of 106

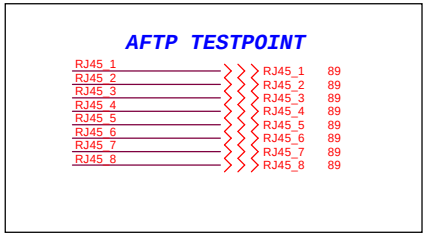
SSID = LAN

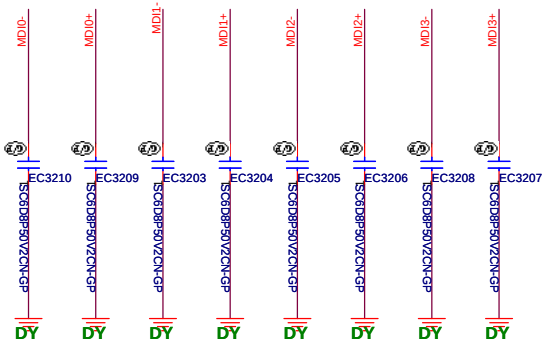


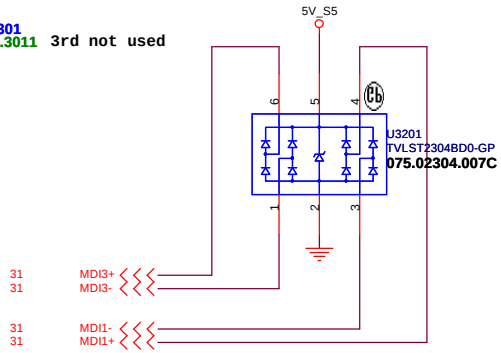
3rd not used

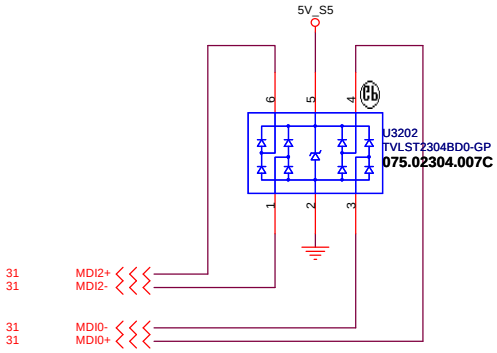


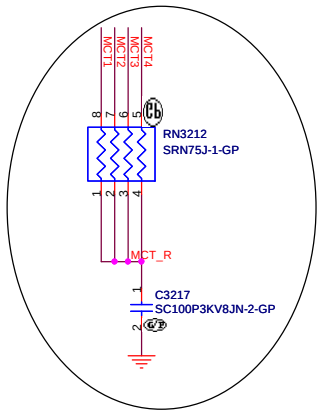
022.10001.00F1
2nd = 022.10001.0F21











12/23 修改家電下鄉 PD

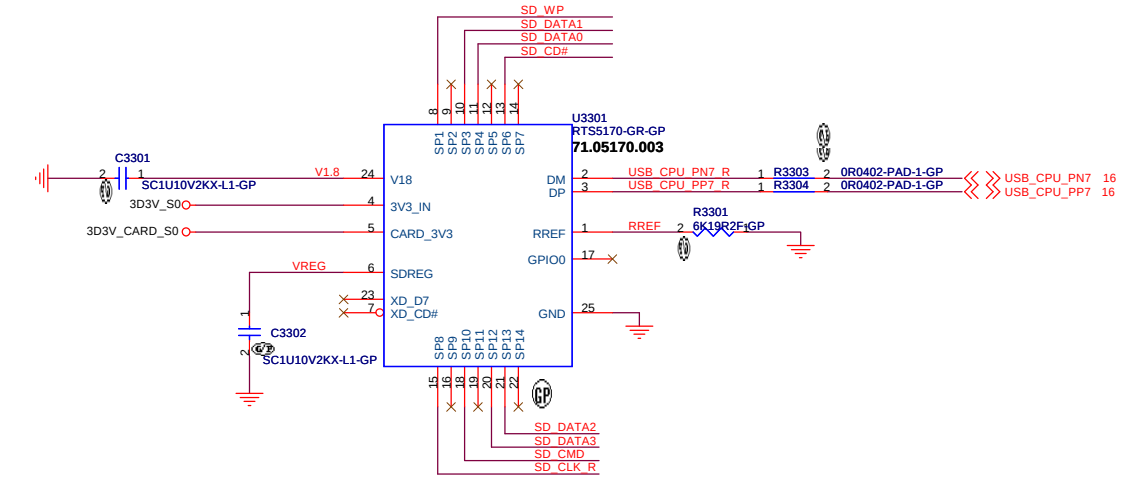
Brook_BH

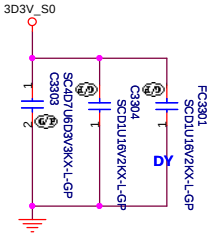
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

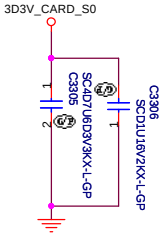
Title: (LAN+VGA) CONNECTOR

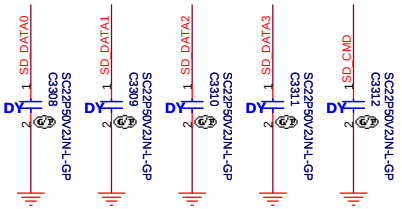
Size	Document Number	Rev
A3	Brook_BH	-1M

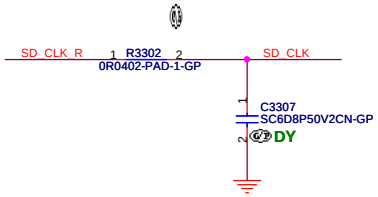
Date: Wednesday, February 04, 2015 Sheet 32 of 106

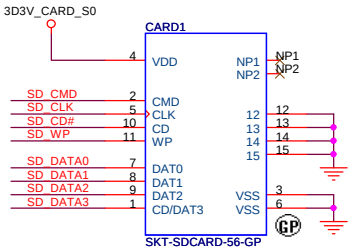


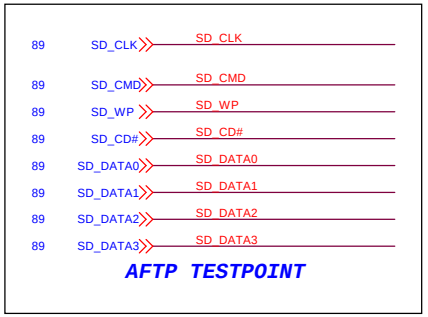












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緯創資通 **Wistron Corporation**
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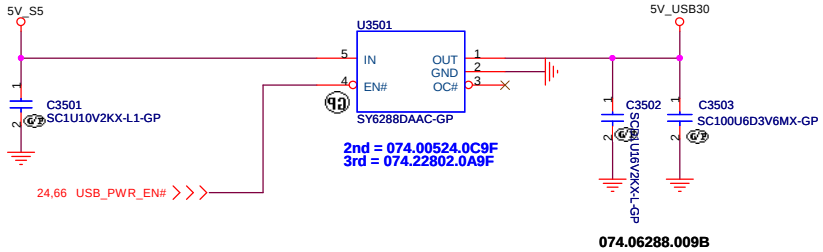
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader CONN (Reserved)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 33 of 106

Low Active 2A



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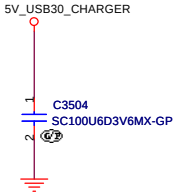
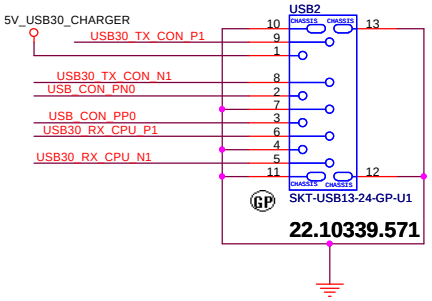
074.06288.009B



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

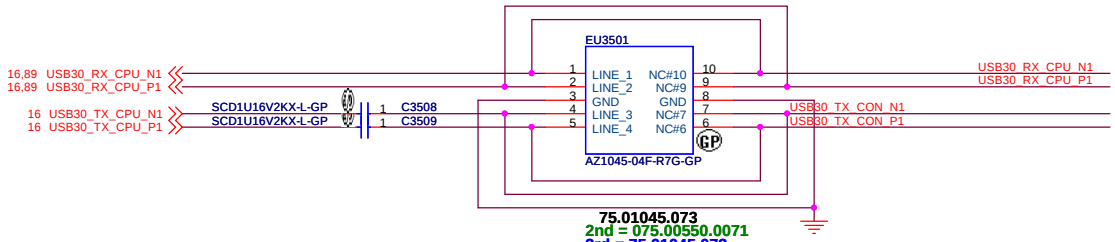
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001



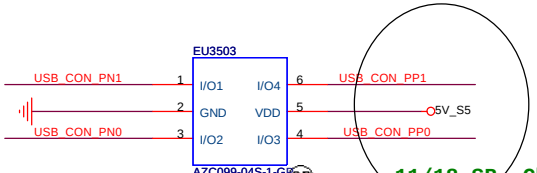
22.10339.571

AFTP TESTPOINT

USB30_TX_CON_P1	USB30_TX_CON_P1 89
USB30_TX_CON_N1	USB30_TX_CON_N1 89
USB_CON_PN0	USB_CON_PN0 89
USB_CON_PP0	USB_CON_PP0 89
USB30_RX_CPU_P1	USB30_RX_CPU_P1 16,89
USB30_RX_CPU_N1	USB30_RX_CPU_N1 16,89
USB30_TX_CON_P2	USB30_TX_CON_P2 89
USB30_TX_CON_N2	USB30_TX_CON_N2 89
USB_CON_PN1	USB_CON_PN1 89
USB_CON_PP1	USB_CON_PP1 89
USB30_RX_CPU_P2	USB30_RX_CPU_P2 16,89
USB30_RX_CPU_N2	USB30_RX_CPU_N2 16,89

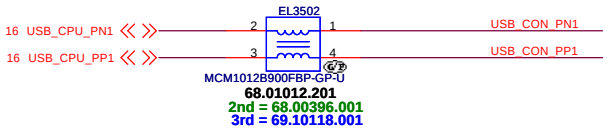


75.01045.073
2nd = 075.00550.0071
3rd = 75.01045.073

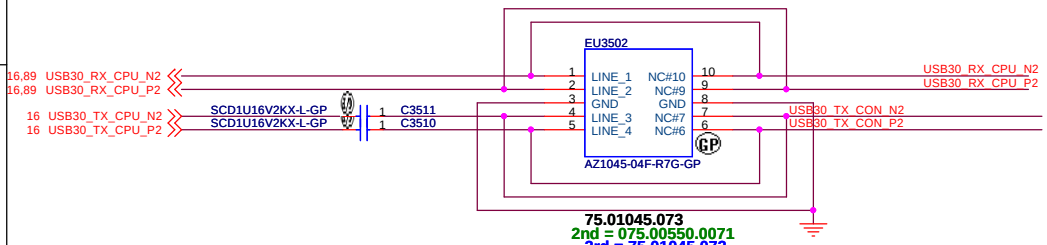


75.09904.07C
2nd = 75.00005.C7C
3rd = 075.01256.007C

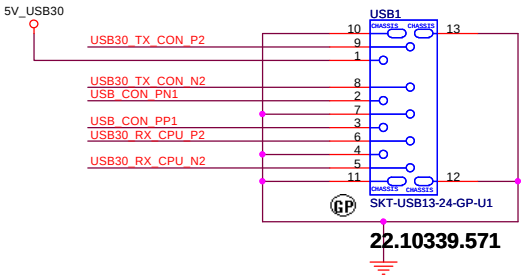
11/18 SB Change to 5V_S5



68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001



75.01045.073
2nd = 075.00550.0071
3rd = 75.01045.073



22.10339.571

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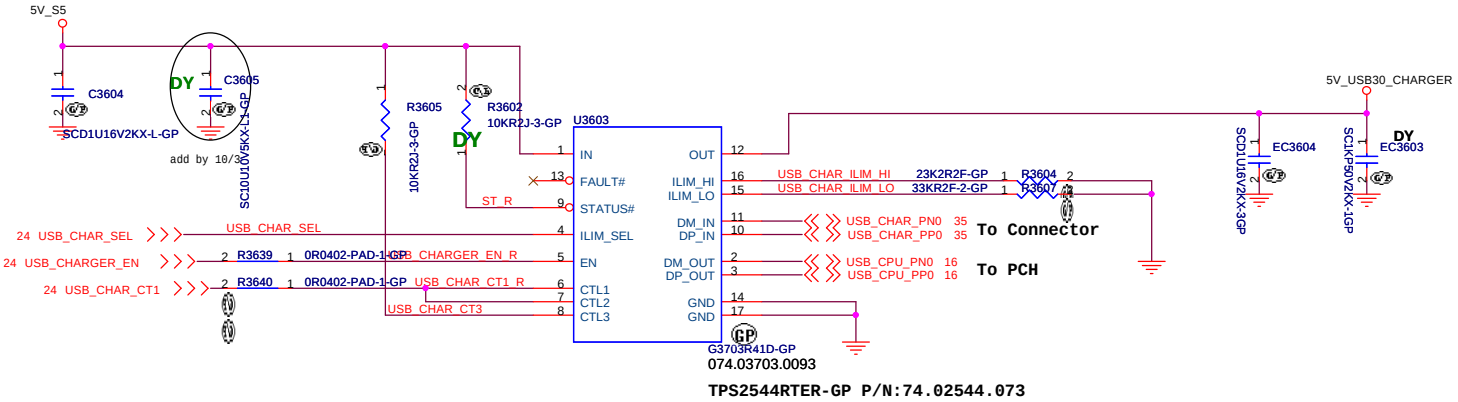
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB_3.0**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Tuesday, February 10, 2015 Sheet 35 of 106



074.03703.0093

TPS2544RTER-GP P/N:74.02544.073

20150115 -1

	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A ~ 2.4 A).

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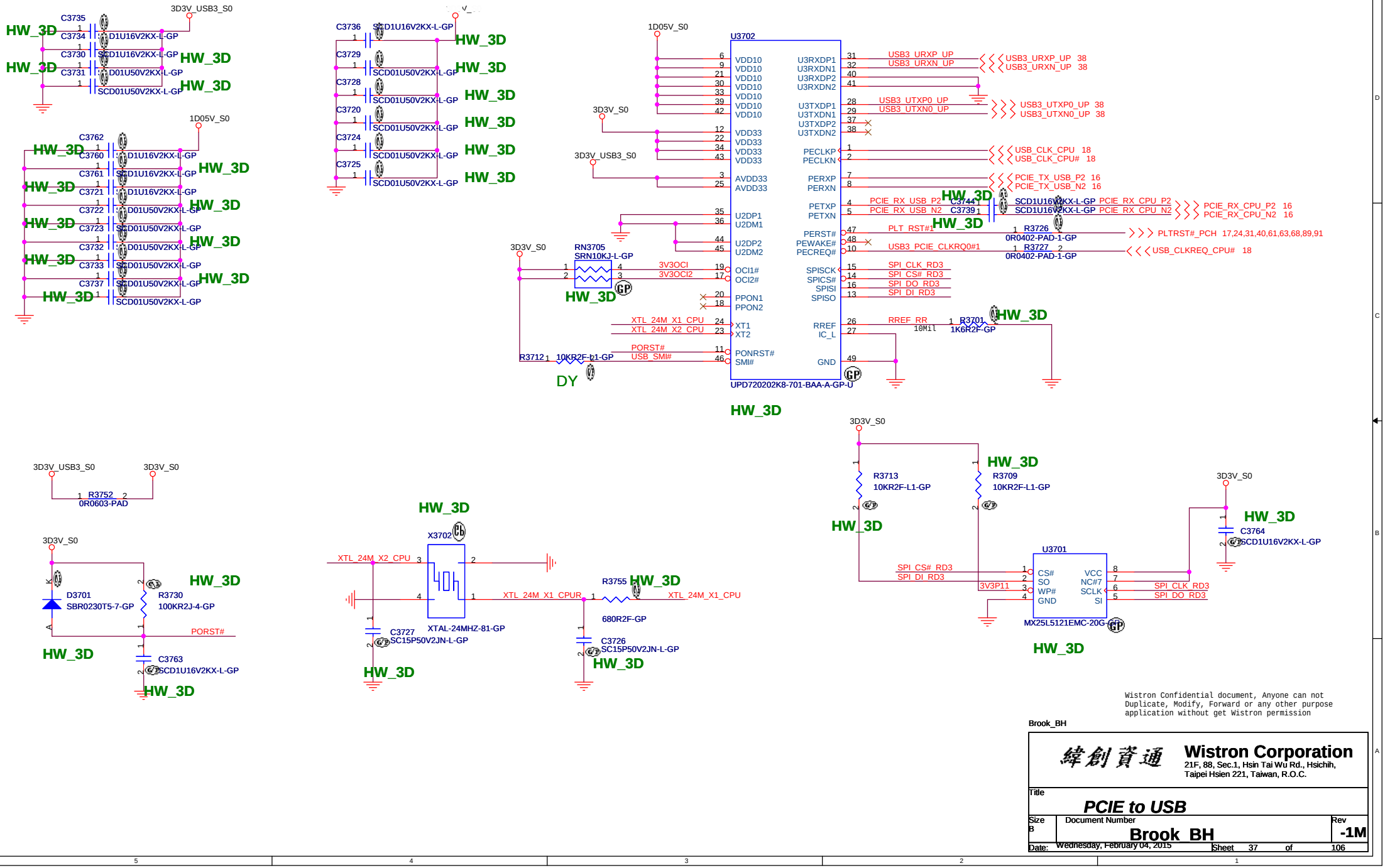
Title: **USB Charger**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 36 of 106



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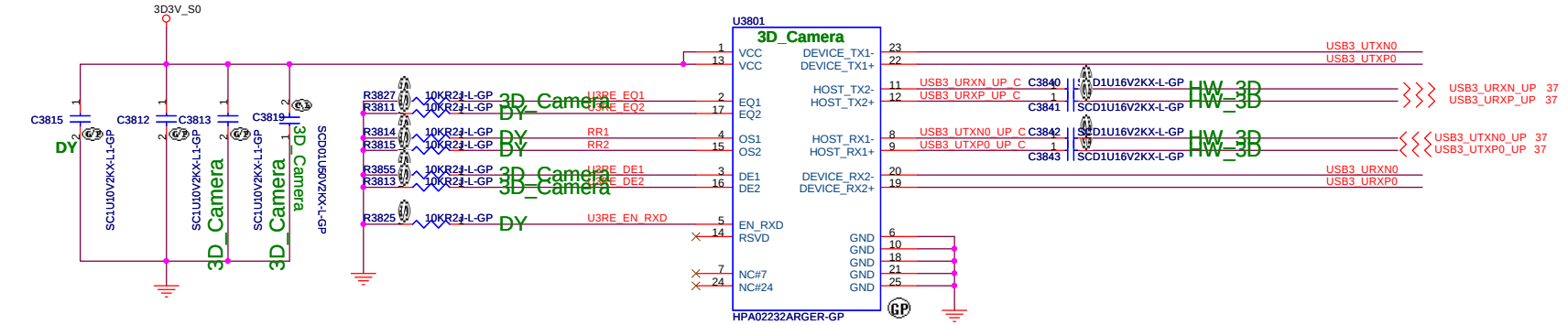
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

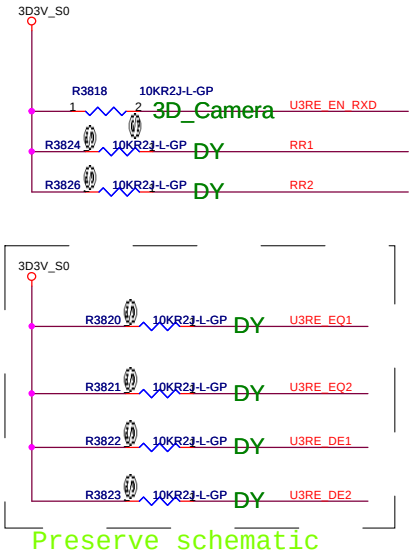
Title: PCIE to USB

Size	Document Number	Rev
B	Brook_BH	-1M

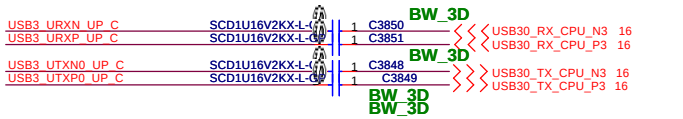
Date: Wednesday, February 04, 2015 Sheet 37 of 106

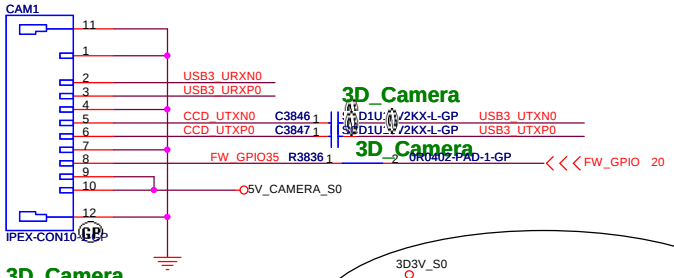


20141013 Rober



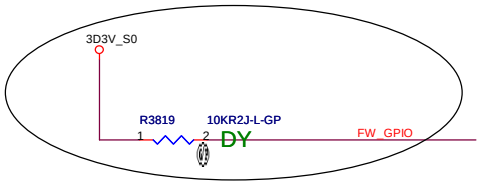
for Broadwell 3D Camera



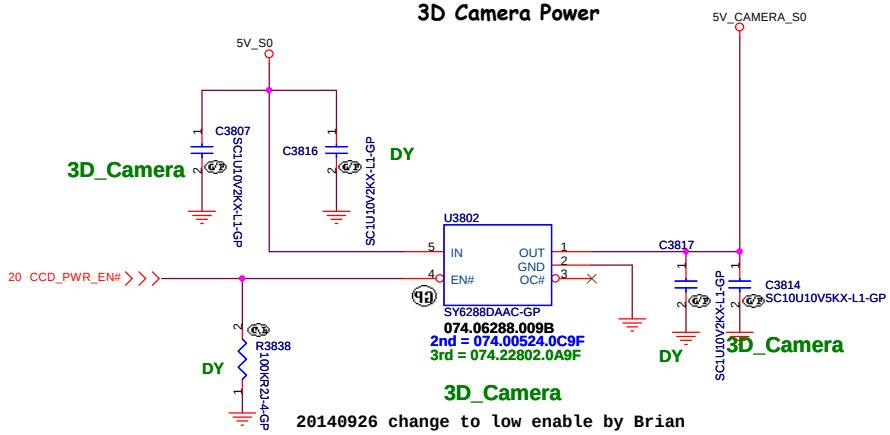


3D_Camera

20.K0329.010



3D Camera Power



20140926 change to low enable by Brian

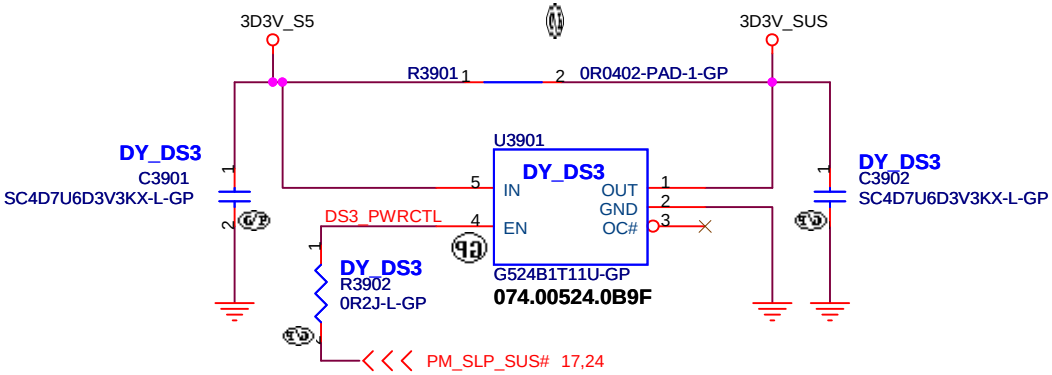
Brook_BH

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Redriver

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 38 of 106



Brook_BH

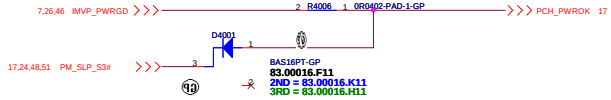
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DS3***

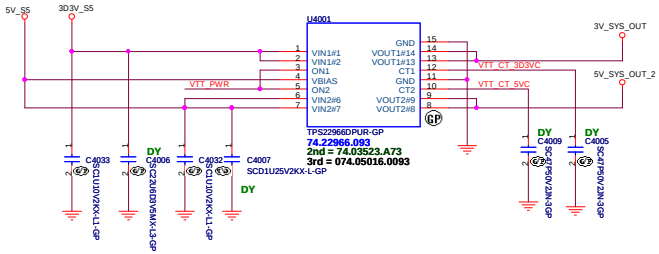
Size	Document Number	Rev
A4	**Brook_BH**	**-1M**

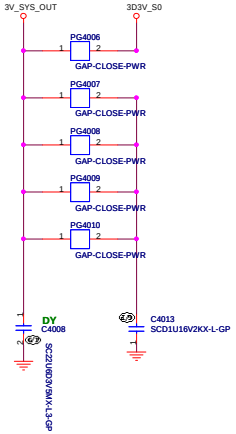
Date: Wednesday, February 04, 2015 Sheet 39 of 106

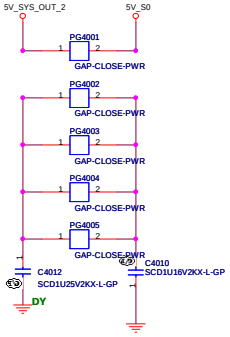
Power Sequence



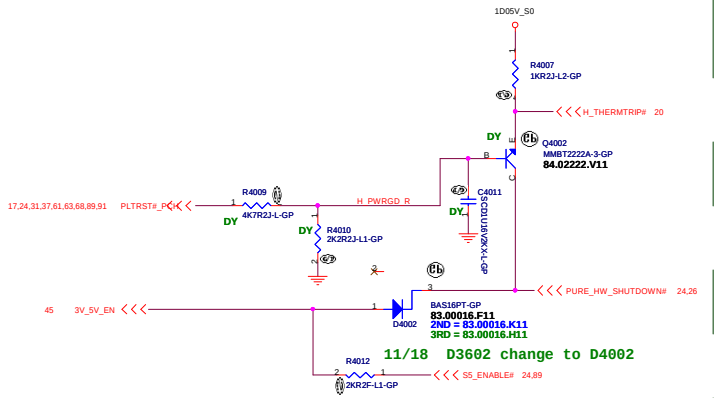
ANNIE Run Power

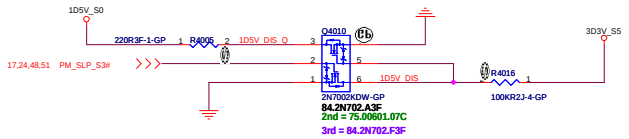






Discharge circuit





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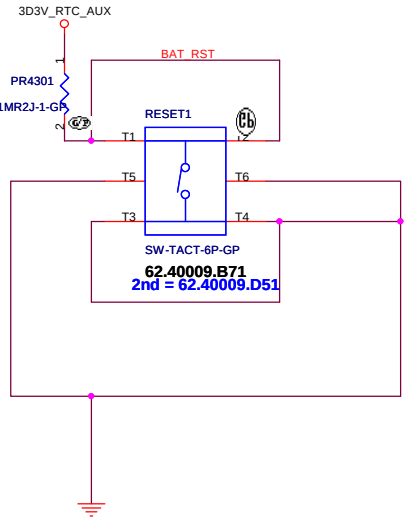
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Connected Standby1**

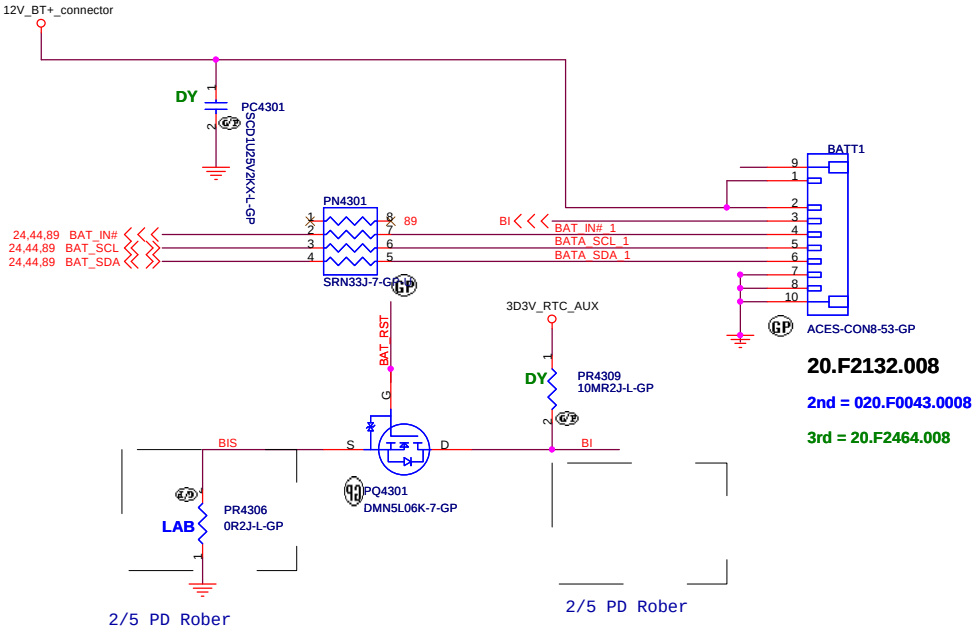
Size: A2 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 40 of 106

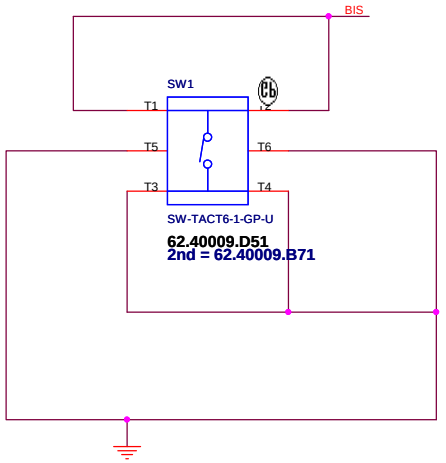
Battery Reset



Battery Connector

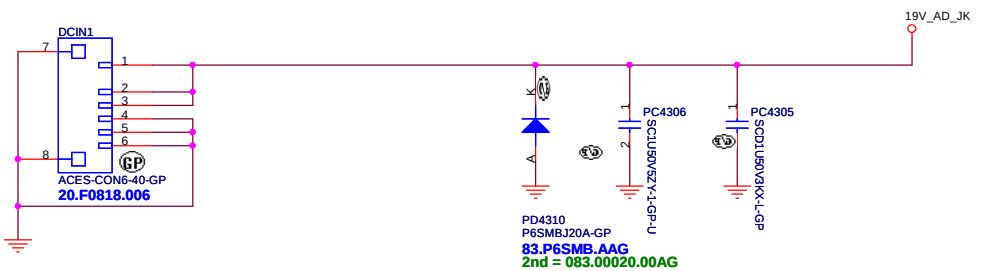


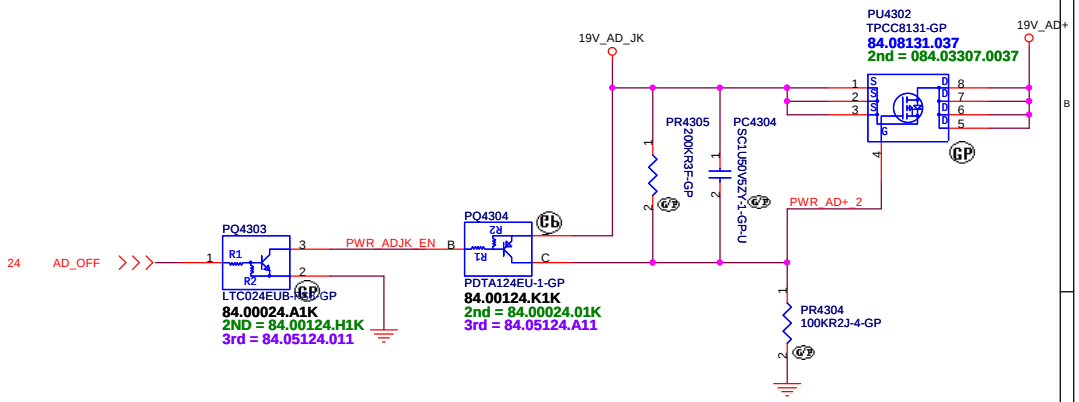
Battery Insert



ANNIE solution

Adaptor in to generate DCBATOUT





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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK&BATT CONN***		
Size: A3	Document Number: **Brook_BH**	Rev: **-1M**
Date: Thursday, February 05, 2015	Sheet 43 of 106	

SSID = Charger

	45W	90W
PR4404	20m(64.R0205.7FL)	10m(64.R0105.7FL)
PR4407	60.4K(64.60425.6DL)	60.4K(64.60425.6DL)
PR4401	100K(64.10035.L3L)	100K(64.10035.L3L)

adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407

Add PR4838/PR4437
2011.0817

Deglicth Time Setting
125K -> Deglitch time : 5us
375K -> Deglitch time : 15us

CYNTEC, 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Charger Current=1.4~3.6A

PU4404/PU4405 change to SIS412

Battery OCP	R3	R4
6 Cell (3S2P)	7A	105K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	13.2V	90.9K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

Wistron Corporation
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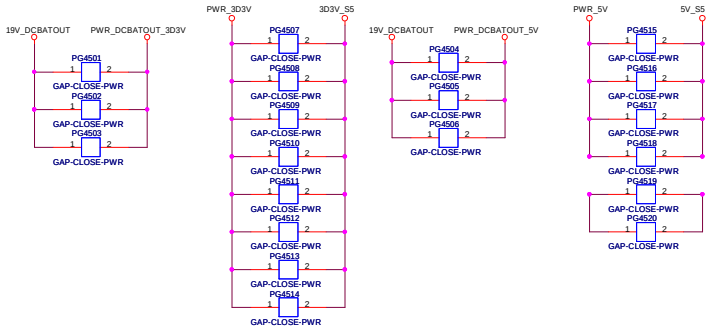
Title: CHARGER_HPA02224
Size: Custom | Document Number: Brook_BH | Rev: -1M
Date: Wednesday, February 06, 2013 | Sheet 44 of 105

SSID = PWR.Plane.Regulator_3p3v5v



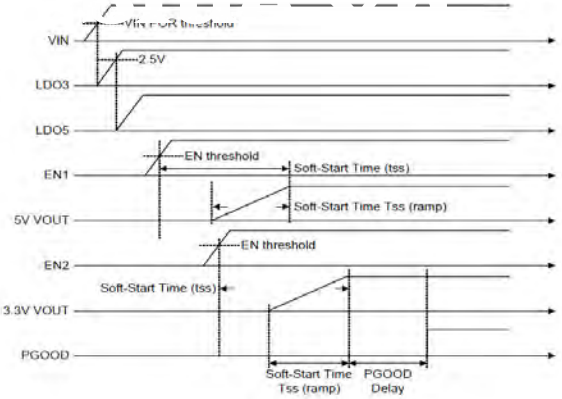
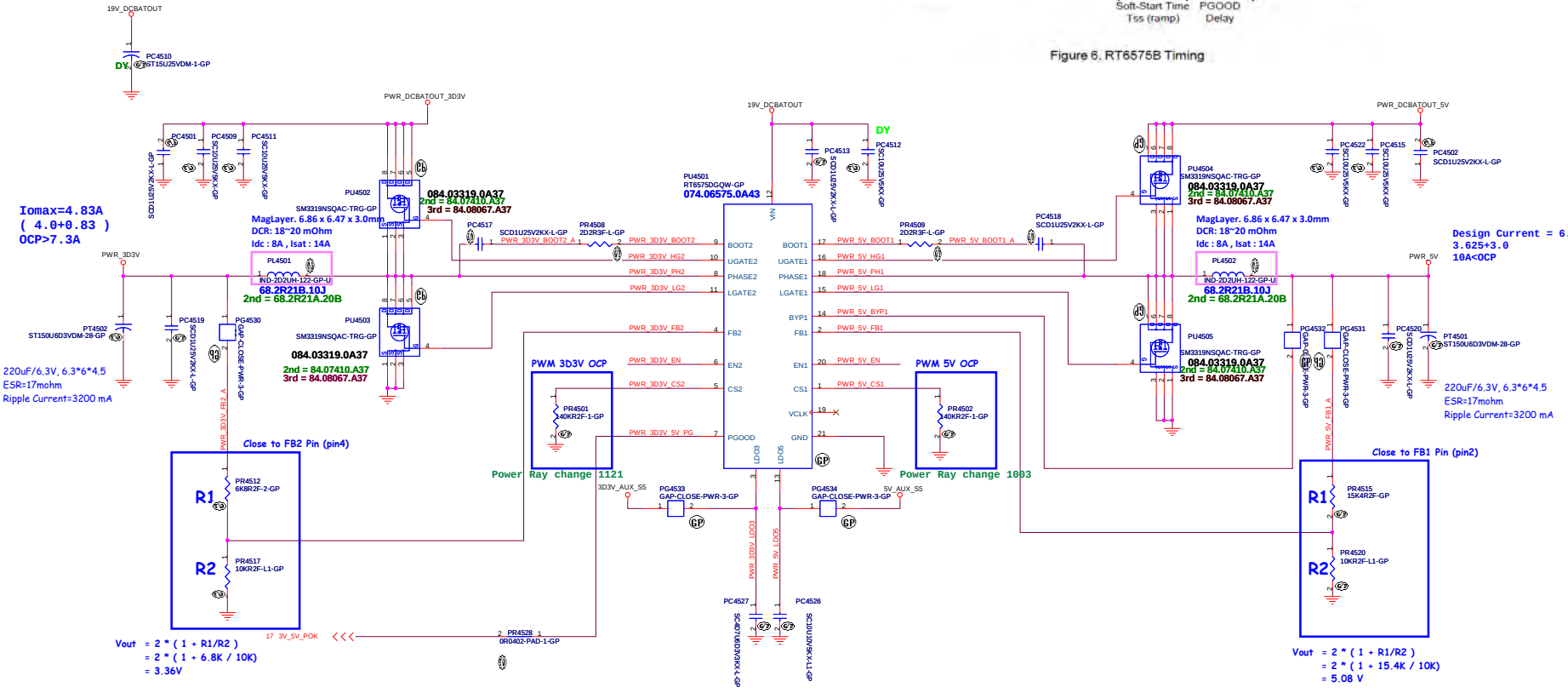
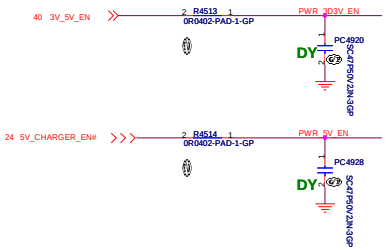


Figure 6. RT6575B Timing



11/18 R4913 and R4914 need to change R4513and R4514



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

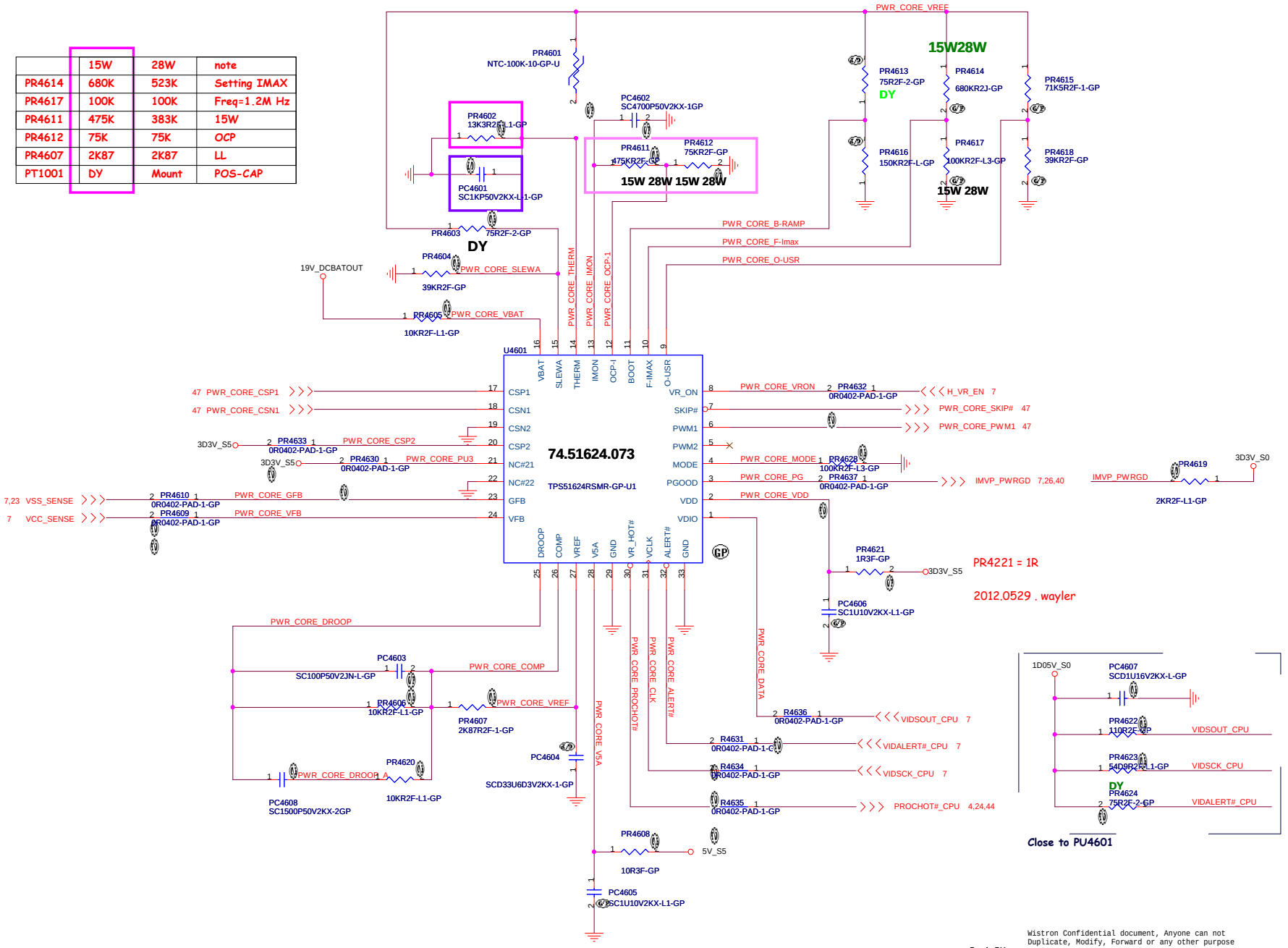
Title: *TPS51225_5V/3D3V*

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 45 of 106

SSID = CPU.Regulator

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCP
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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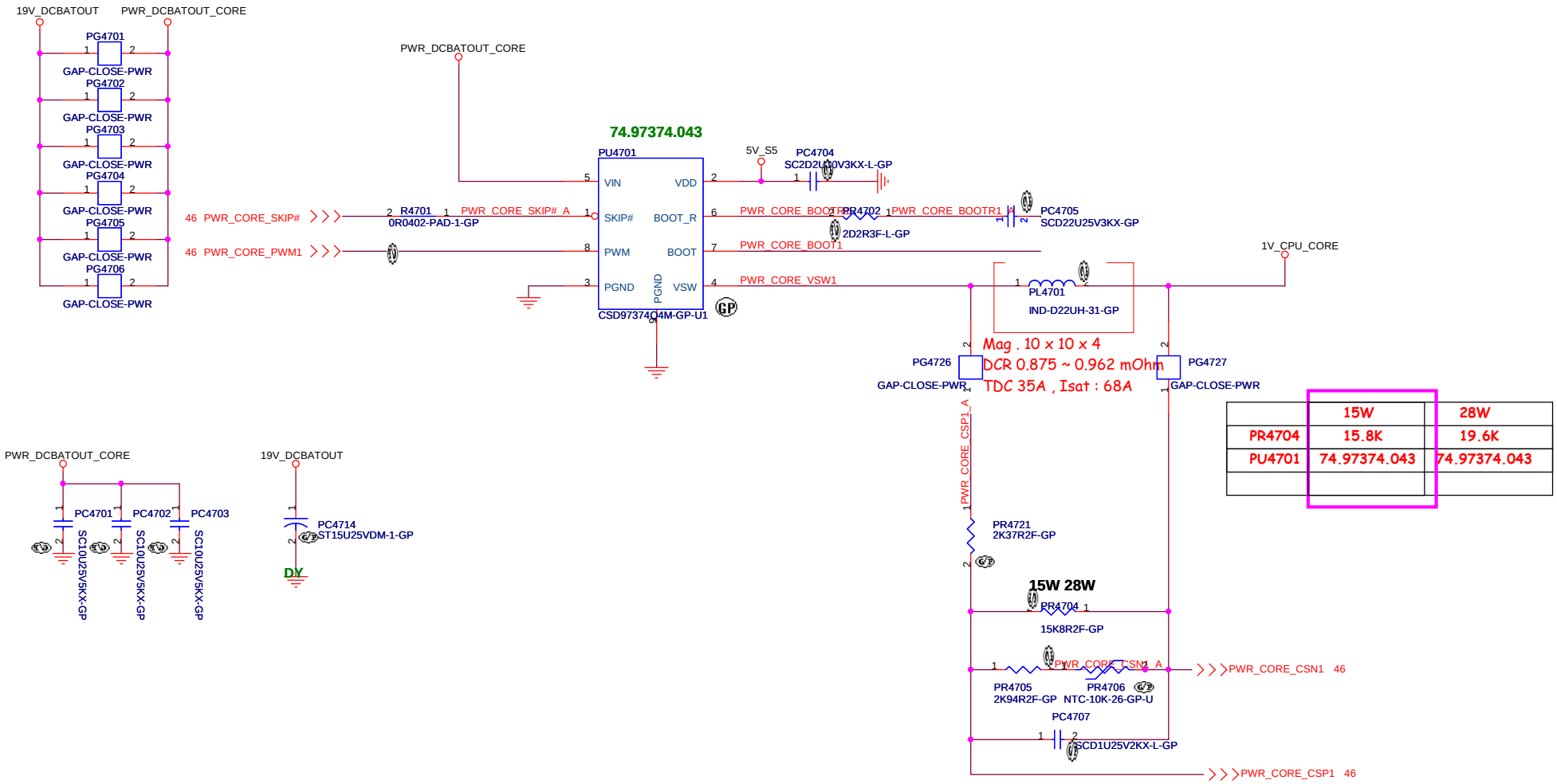
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51624 CPUCORE(1/2)**

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 46 of 106



	15W	28W
PR4704	15.8K	19.6K
PU4701	74.97374.043	74.97374.043

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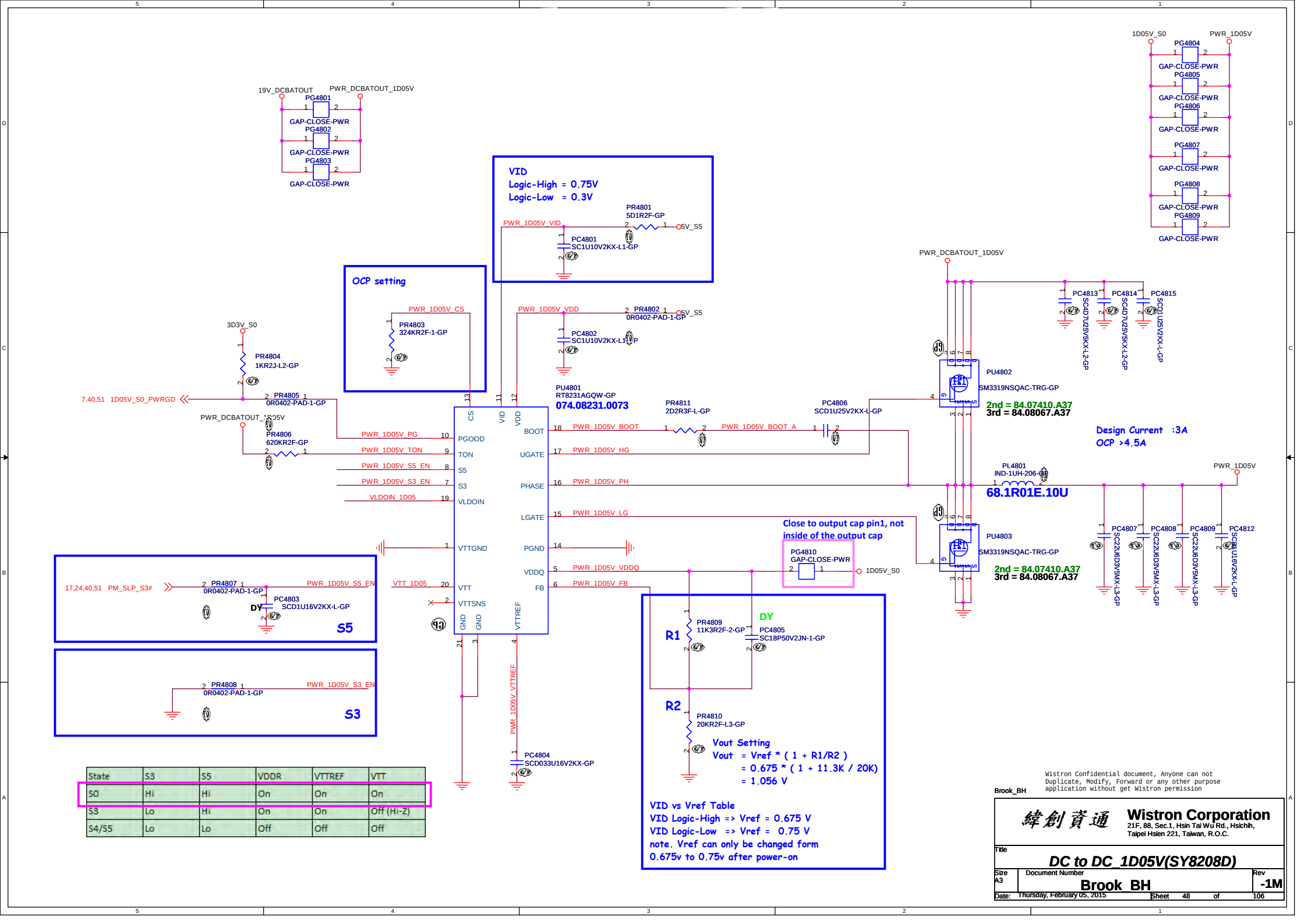
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51624_CPUCORE(2/2)***

Size	Document Number	Rev
B	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 47 of 106



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Brook_BH

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Taipei Hsien 221, Taiwan, R.O.C.

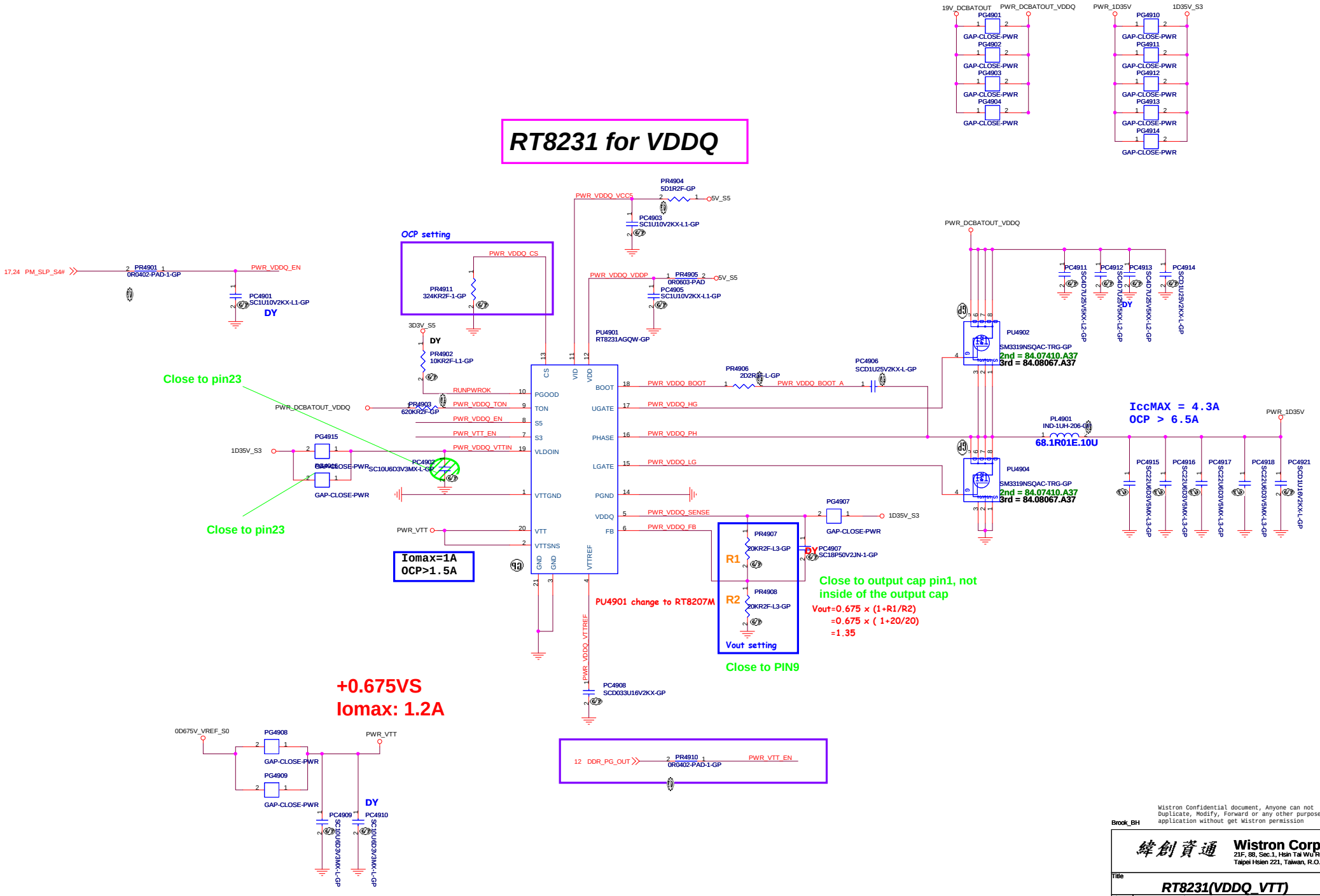
Title: **DC to DC_1D05V(SY8208D)**

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Thursday, February 05, 2015 Sheet 48 of 106

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8231 for VDDQ



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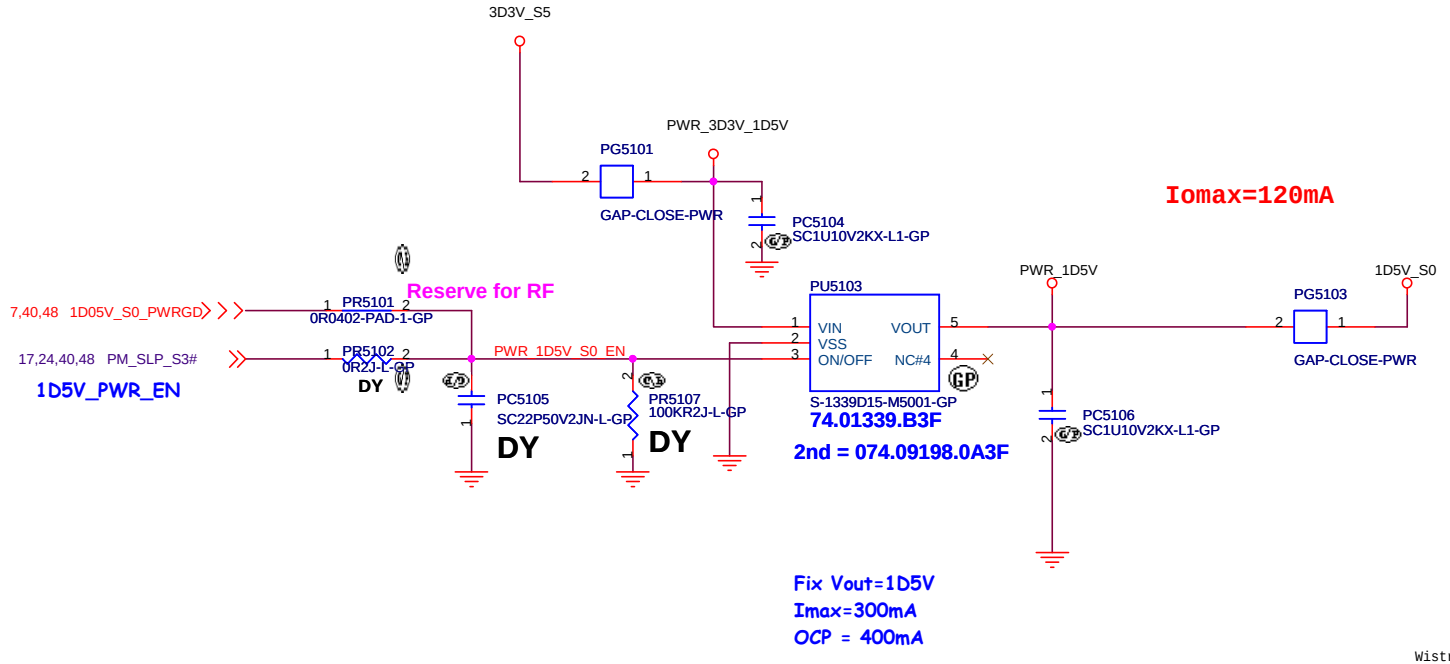
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231(VDDQ_VTT)

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 49 of 106

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



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Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D5V_S0 SYW232*

Size	Document Number	Rev
Custom	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 51 of 106

Main Func = LCD

Pin count		
1	Display	EDP 4Lans+CCD
2		GND
3		eDP_AUX_CON_P
4		eDP_AUX_CON_N
5		GND
6		eDP_TX_CON_P0
7		eDP_TX_CON_N0
8		GND
9		eDP_TX_CON_P1
10		eDP_TX_CON_N1
11		GND
12		eDP_TX_CON_P2
13		eDP_TX_CON_N2
14		GND
15		eDP_TX_CON_P3
16		eDP_TX_CON_N3
17		eDP_HPD_CON
18		LCDVDD(3V)
19		LCDVDD(3V)
20		LCDVDD(3V)
21		LCDVDD(3V)
22	Touch	TOUCH_DET#
23		TOUCH_GND/ TOUCH_RST
24		TOUCH_EN/ TOUCH_INT
25		Touch_PWR(3V/5V)
26		USB_PN6/ SCL
27		USB_PP6/ SDA
28	CCD	3D3V_CAMERA_S0
29		USB_CAMERA_P
30		USB_CAMERA_N
31	GND	GND
32		GND
33		GND
34		GND
35		
36		
37	DCBATOUT	DCBATOUT_LCD
38		DCBATOUT_LCD
39		DCBATOUT_LCD
40		DCBATOUT_LCD

LCD1

STAR-CONN1-GP

eDP_AUX_CON_P — C5501 SCD1U16V2KX-L-GP — eDP_AUX_CPU_P 8
eDP_AUX_CON_N — C5505 SCD1U16V2KX-L-GP — eDP_AUX_CPU_N 8
eDP_TX_CON_P0 — C5506 SCD1U16V2KX-L-GP — eDP_TX_CPU_P0 8
eDP_TX_CON_N0 — C5507 SCD1U16V2KX-L-GP — eDP_TX_CPU_N0 8
eDP_TX_CON_P1 — C5517 SCD1U16V2KX-L-GP — eDP_TX_CPU_P1 8
eDP_TX_CON_N1 — C5518 SCD1U16V2KX-L-GP — eDP_TX_CPU_N1 8
eDP_TX_CON_P2 — C5519 SCD1U16V2KX-L-GP — eDP_TX_CPU_P2 8
eDP_TX_CON_N2 — C5520 SCD1U16V2KX-L-GP — eDP_TX_CPU_N2 8
eDP_TX_CON_P3 — C5521 SCD1U16V2KX-L-GP — eDP_TX_CPU_P3 8
eDP_TX_CON_N3 — C5522 SCD1U16V2KX-L-GP — eDP_TX_CPU_N3 8
eDP_HPD_CON
3D3V_LCDVDD_PWR — R5501 0R0805-PAD — 3D3V_LCDVDD_S0

TOUCH_DETR# — R5524 33R2J-L1-GP — TOUCH_DET# 20
TOUCH_S_RST#_R — R5523 33R2J-L1-GP — TOUCH_S_RST# 20
TOUCH_INTR# — R5522 33R2J-L1-GP — TOUCH_INT# 20
TS_S0 — R5526 0R2J-L-GP — TS_USB
TS_I2C — R5515 33R2J-L1-GP

TS_USB_CON_N
TS_USB_CON_P
USB_CON_PP6
USB_CON_PN6
3D3V_CAMERA_S0
eDP_BLEN_CON — R5520 33R2J-L1-GP — eDP_BLCTRL_CPU 15
eDP_BLCTRL_CON
19V_DCBATOUT_LCD

20.K0809.040
2nd = 20.K0678.040

20140926 Rober

Inverter Power

19V_DCBATOUT_LCD — C5502 SC4D7U25V5KX-L2-GP
19V_DCBATOUT — F5501 POLYSW-1D1A24V-GP-U 69.50007.A31 2nd = 69.50007.A41 — C5504 SCD1U25V2KX-L-GP

eDP_BLEN_CON — RN5513 SRN1KJ-7-GP — BLON_OUT 24
eDP_HPD_CON — eDP_HPD_CPU 15
eDP_HPD_CON — RN5514 SRN100KJ-7-GP
eDP_BLEN_CON
20141216 -1

TS_I2C

R5523 0R2J-L-GP — I2C0_DATA_CPU 20
R5524 0R2J-L-GP — I2C0_CLK_CPU 20

TS_I2C — TS_USB
TS_USB_CON_P — USB_CPU_PP5 16
TS_USB_CON_N — USB_CPU_PN5 16
EL5503
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

USB_CON_PP6 — EL5504 — USB_CPU_PP6 16
USB_CON_PN6 — USB_CPU_PN6 16
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

USB_CON_PP6 — USB_CON_PP6 89
USB_CON_PN6 — USB_CON_PN6 89
TS_USB_CON_N — TS_USB_CON_N 89
TS_USB_CON_P — TS_USB_CON_P 89
3D3V_CAMERA_S0 — 3D3V_CAMERA_S0 89
TOUCH_DETR# — TOUCH_DETR# 89
TOUCH_S_RST#_R — TOUCH_S_RST#_R 89
TS_S0 — TS_S0 89
eDP_TX_CON_P3 — eDP_TX_CON_P3 89
eDP_TX_CON_N3 — eDP_TX_CON_N3 89
eDP_TX_CON_P2 — eDP_TX_CON_P2 89
eDP_TX_CON_N2 — eDP_TX_CON_N2 89
eDP_AUX_CON_P — eDP_AUX_CON_P 89
eDP_AUX_CON_N — eDP_AUX_CON_N 89
eDP_TX_CON_P0 — eDP_TX_CON_P0 89
eDP_TX_CON_N0 — eDP_TX_CON_N0 89
3D3V_LCDVDD_PWR — 3D3V_LCDVDD_PWR 89
eDP_TX_CON_P1 — eDP_TX_CON_P1 89
eDP_TX_CON_N1 — eDP_TX_CON_N1 89
TOUCH_INTR# — TOUCH_INTR# 89
eDP_HPD_CON 89
eDP_BLEN_CON 89
eDP_BLCTRL_CON 89

AFTP TESTPOINT

T-COM Power

3D3V_LCDVDD_S0 — C5511 SC4D7U6D3V3KX-L-GP — C5508 SCD1U16V2KX-L-GP — DY C5509 SC1U10V2KX-L-GP
3D3V_S0 — C5512 SC4D7U6D3V3KX-L-GP
U5501 RT9724GB-GP
74.09724.09F
2ND = 74.03514.07F
15 eDP_VDDEN_CPU — R5509 100KR2J-4-GP
Layout 40 mil

USB_CON_PP6 — EU5504 — USB_CON_PP6
USB_CON_PN6
TS_USB_CON_N
TS_USB_CON_P
5V_S0
AZC099-04S-1-GP
75.09904.07C
2nd = 75.00005.C7C
3rd = 075.01256.007C

Camera Power

3D3V_S0 — F5510 POLYSW-1D1A6V-9-GP-U 69.48001.081 2ND = 69.50011.081 — 3D3V_CAMERA_S0
C5513 SC10U10V5KX-L-GP
C5514 SCD1U16V2KX-L-GP

Touch panel Power

TS_S0
3D3V_S0 — R5744 0R3J-L-GP — DY
5V_S0 — R5745 0R3J-L-GP — TS
C5515 SC10U10V5KX-L1-GP — C5516 SCD1U16V2KX-L-GP — TS
20141216 -1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A3 | Document Number: Brook_BH | Rev: -1M
Date: Thursday, February 12, 2015 | Sheet 55 of 106

SSID = Display

VGA RTD2168

Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

3D3V_S0 — R5611 4K7R2J-L-GP — LDO_EN

C5603 SCD1U16V2KX-L-GP — 1D2V_VCCK_S0

20141013 Rober

close to pin25

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

close to pin24

3D3V_AVCC_S0 — L5604 PBY100505T-600Y-N-GP — 3D3V_S0

C5618 SC10U10V5KX-L-GP, C5616 SCD1U16V2KX-L-GP

C5620 SCD1U16V2KX-L-GP

close to pin5

3D3V_DAC_S0 — L5605 PBY100505T-600Y-N-GP

C5619 SC10U10V5KX-L-GP, C5617 SCD1U16V2KX-L-GP

C5621 SCD1U16V2KX-L-GP

close to pin9

close to pin20

R5617 100KR2J-4-GP

CRT_RED — L5601 BLM18BB220SN-GP — CRT_RED_CON

C5604 SC10P50V2JN-L1-GP, C5605 SC10P50V2JN-L1-GP

CRT_GREEN — L5602 BLM18BB220SN-GP — CRT_GREEN_CON

C5606 SC10P50V2JN-L1-GP, C5607 SC10P50V2JN-L1-GP

CRT_BLUE — L5603 BLM18BB220SN-GP — CRT_BLUE_CON

C5608 SC10P50V2JN-L1-GP, C5609 SC10P50V2JN-L1-GP

RN5610 SRN150J-1-GP, RN5611 SRN150J-1-GP

those compoent need to close

L5601~3 change to 68.00084.B61

U5601 RTD2168-CGT-GP

3D3V_AVCC_S0	24	AVCC_33	
1D2V_VCCK_S0	25	AVCC_12	
3D3V_S0	5	DVCC_33	
	20	DVCC_33	
1D2V_VCCK_S0	19	VCCK_12	
3D3V_DAC_S0	9	VDD_DAC_33	
LDO_EN	21	LDO_EN	
DP_AUX_CON_P	26	AUX_P	
DP_AUX_CON_N	27	AUX_N	
DDI_VGA_DATA_C_P0	29	LANE0P	
DDI_VGA_DATA_C_N0	30	LANE0N	
DDI_VGA_DATA_C_P1	31	LANE1P	
DDI_VGA_DATA_C_N1	32	LANE1N	
	17	XI/CKIN	
	18	XO	
RRX	28	RRX	
	1	HPD	CRT_HPD
	2	SMB_SCL	SMB_SCL
	3	SMB_SDA	SMB_SDA
	4	VGA_SCL	CRT_DDCCLK_CON
	6	VGA_SDA	CRT_DDCDATA_CON
	7	VSYNC	CRT_VSYNC
	8	HSYNC	CRT_HSYNC
	15	RED_P	CRT_RED
	16	RED_N	
	12	GREEN_P	CRT_GREEN
	13	GREEN_N	
	10	BLUE_P	CRT_BLUE
	11	BLUE_N	
	22	POL1_SDA	POL1_SDA
	23	POL2_SCL	POL1_SCL
	14	GND_DAC	
	33	GND	

RN5612 SRN4K7J-8-GP — 20141216 -1

15 PCH_DPC_AUXP, 15 PCH_DPC_AUXN — C5615, C5614 SCD1U16V2KX-L-GP

8 DDI_VGA_DATA_CPU_P0, 8 DDI_VGA_DATA_CPU_N0 — C5613, C5612 SCD1U16V2KX-L-GP

8 DDI_VGA_DATA_CPU_P1, 8 DDI_VGA_DATA_CPU_N1 — C5611, C5610 SCD1U16V2KX-L-GP

20140926 Rober

R5610 12KR2F-L-GP

20141013 Rober

5V_CRT_S0 — 5V_HDMI_S0

D5601 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

RN5601 SRN2K2J-5-GP

CRT_DDCDATA_CON, CRT_DDCCLK_CON

C5622 SCD1U16V2KX-L-GP — 1D2V_VCCK_S0

C5622 SC2D2U10V3KX-L-GP

close to pin19

CRT_VSYNC — R5605 36R2F-1-GP — CRT_VSYNC_CON

C5601 SC10P50V2JN-L1-GP

CRT_HSYNC — R5606 36R2F-1-GP — CRT_HSYNC_CON

C5602 SC10P50V2JN-L1-GP

CRT_DDCDATA_CON 89
CRT_DDCCLK_CON 89
CRT_RED_CON 89
CRT_GREEN_CON 89
CRT_BLUE_CON 89
CRT_VSYNC_CON 89
CRT_HSYNC_CON 89

AFTP TESTPOINT

5V_CRT_S0 — C5632 SCD1U16V2KX-L-GP

CRT1 D-SUB-15-155-GP-U

	9	VCC_CRT	
		NC#4	4
		NC#11	11
CRT_DDCDATA_CON	12	DDCDATA_ID1	
CRT_DDCCLK_CON	15	DDCCLK_ID3	
CRT_RED_CON	1	CRT_RED	
CRT_GREEN_CON	2	CRT_GREEN	
CRT_BLUE_CON	3	CRT_BLUE	
CRT_VSYNC_CON	14	VSYNC	
CRT_HSYNC_CON	13	HSYNC	
		GND	5
		GND	6
		GND	7
		GND	8
		GND	10
		GND	16
		GND	17

20.20984.015

2nd = 20.20938.015

Mode Configure Table(Power On Latch)

3D3V_S0 — R5613 4K7R2J-L-GP (DY) — POL1_SDA — R5614 4K7R2J-L-GP

3D3V_S0 — R5615 4K7R2J-L-GP — POL1_SCL — R5616 4K7R2J-L-GP (DY)

POL2_SCL(PIN23) \ POL1_SDA(PIN22)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for systemdesign.
Reserve 4.7K resistor pull high/low for mode selection
ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode: PIN22 pull high, PIN23 pull low
EEPROM Mode: PIN22 pull high, PIN23 pull high

EEPROM MODE

3D3V_S0 — U5602 CAT24C128YI-GT3-GP (DY)

A0, A1, A2, GND, VCC, WP, SCL, SDA — POL1_SCL, POL1_SDA

VEDOR CHECK

In EEPROM mode,an additional EEPROM is needed. EEPROM should configure with following conditions. 1- EEPROM with a size of 16K-Byte
ROM or EEPROM mode: connect to PCH SMBUS
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

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Title: VGA RTD2168

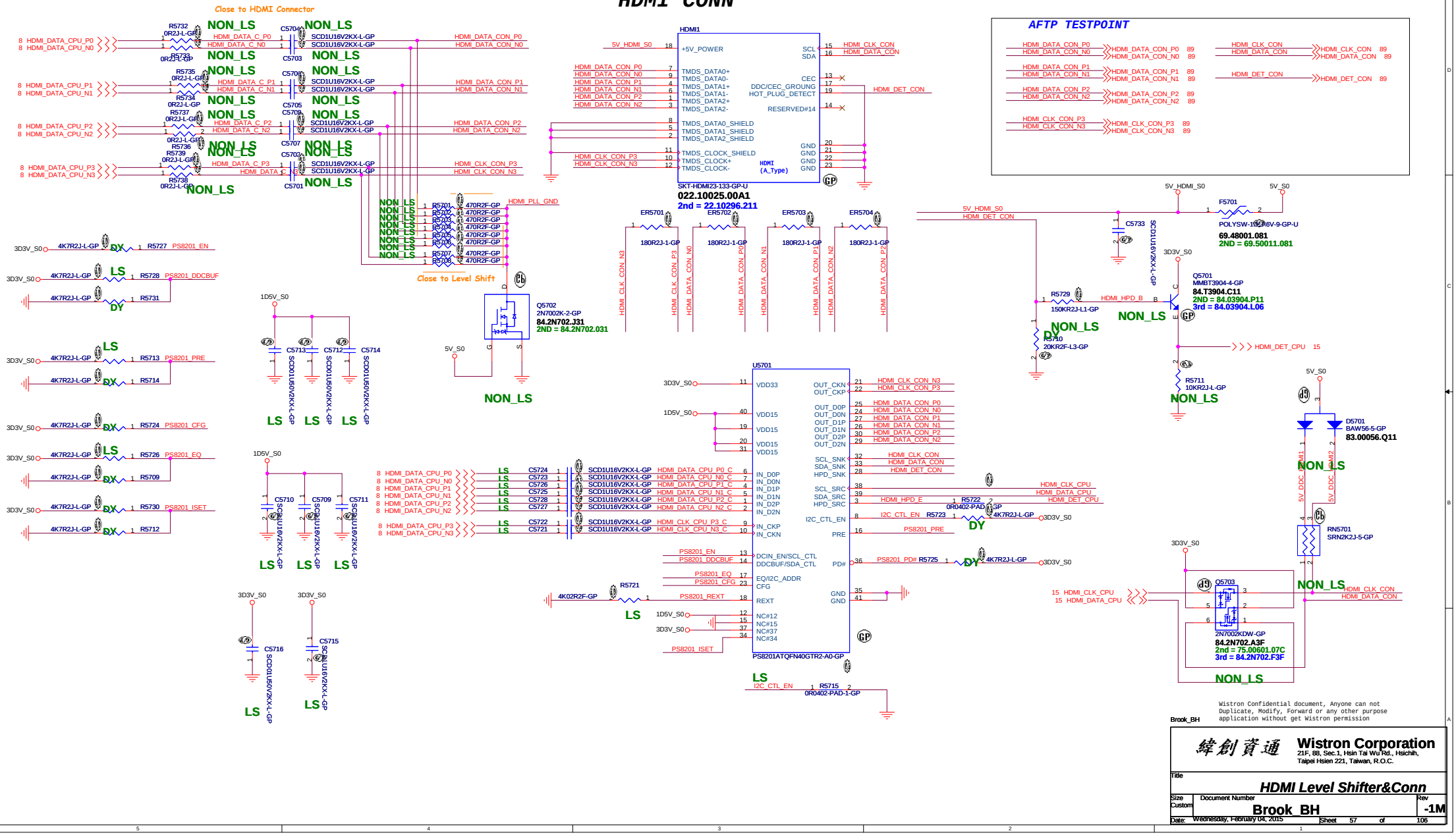
Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Thursday, February 12, 2015 | Sheet 56 of 106

SSID = VIDEO

HDMI Level Shifter & CONN

HDMI CONN



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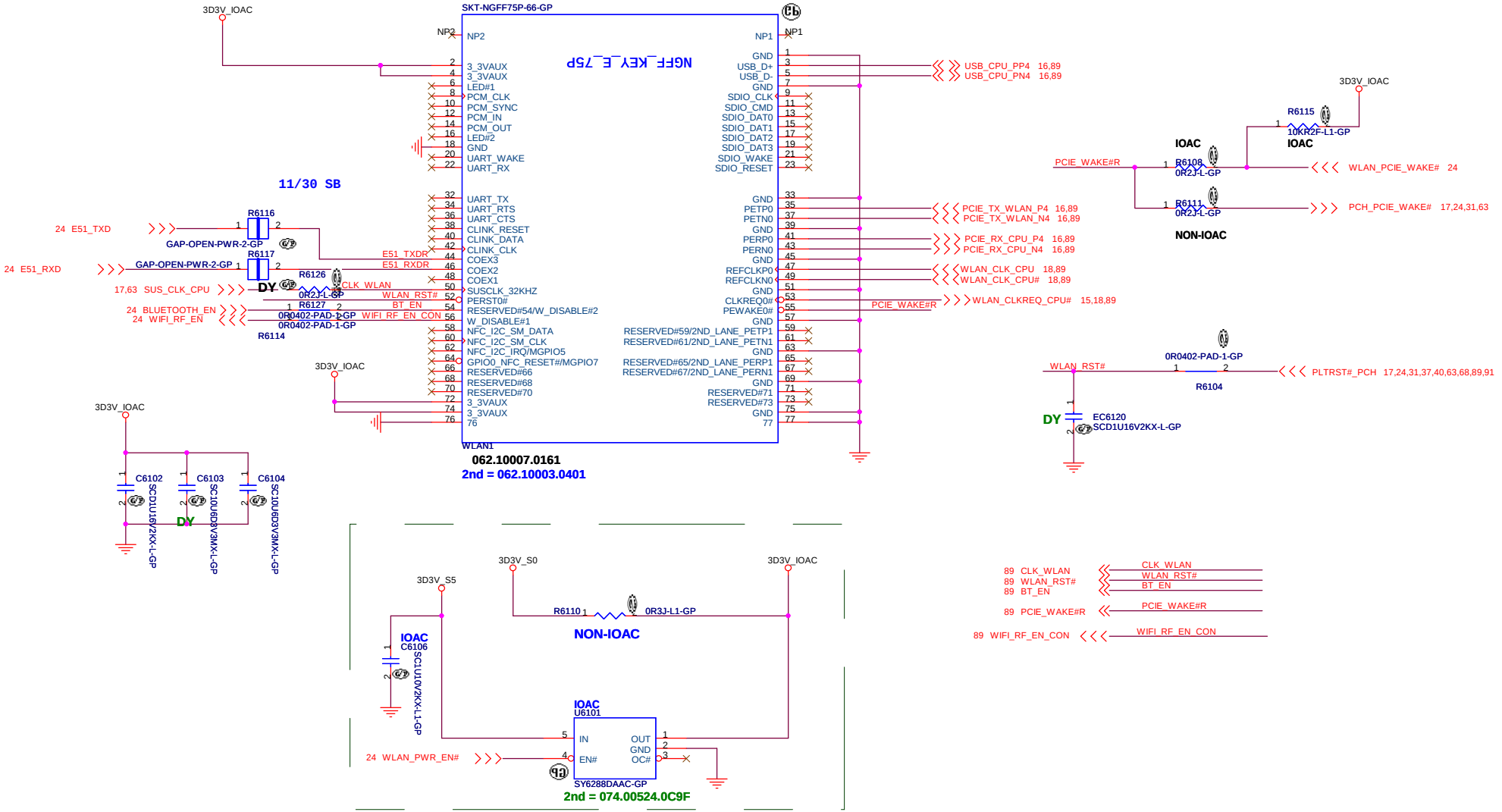
Title	HDMI Level Shifter&Conn	
Size: Custom	Document Number: Brook_BH	Rev: -1M
Date: Wednesday, February 04, 2015	Sheet 57 of 106	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

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Title: Mini Card WLAN

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 11, 2015 Sheet 61 of 106

SSID = mSATA

Mini Card Connector(mSATA)

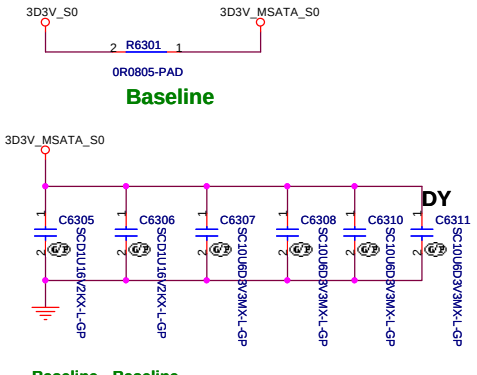
17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

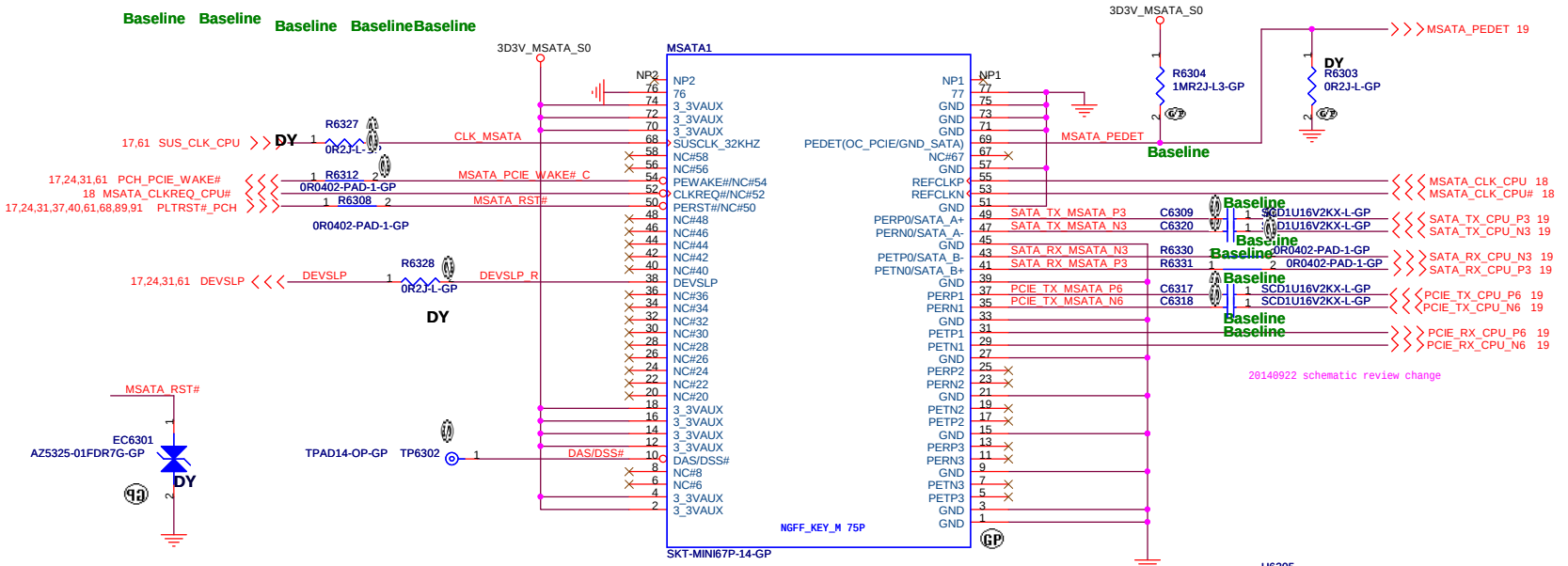
The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

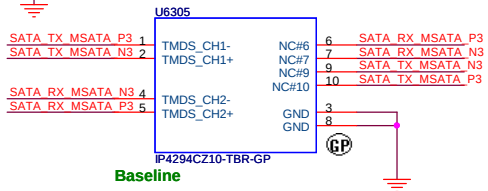
Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.







2/5 PD Rober Part number change with EU3501

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

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Title: **MSATA Conn**

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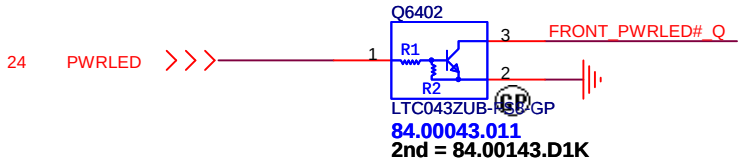
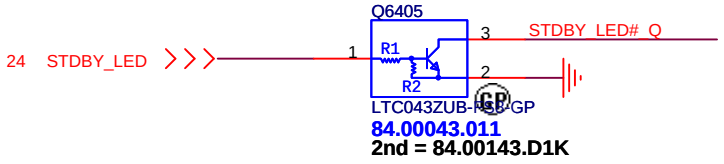
Date: Thursday, February 12, 2015 | Sheet 63 of 106

SSID = User.Interface

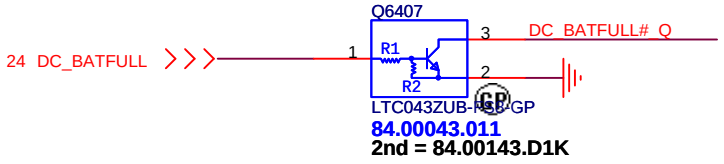
Power Button_LED



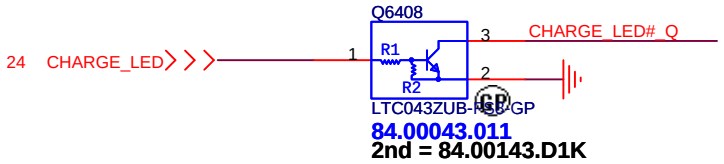
Power STDBY_LED

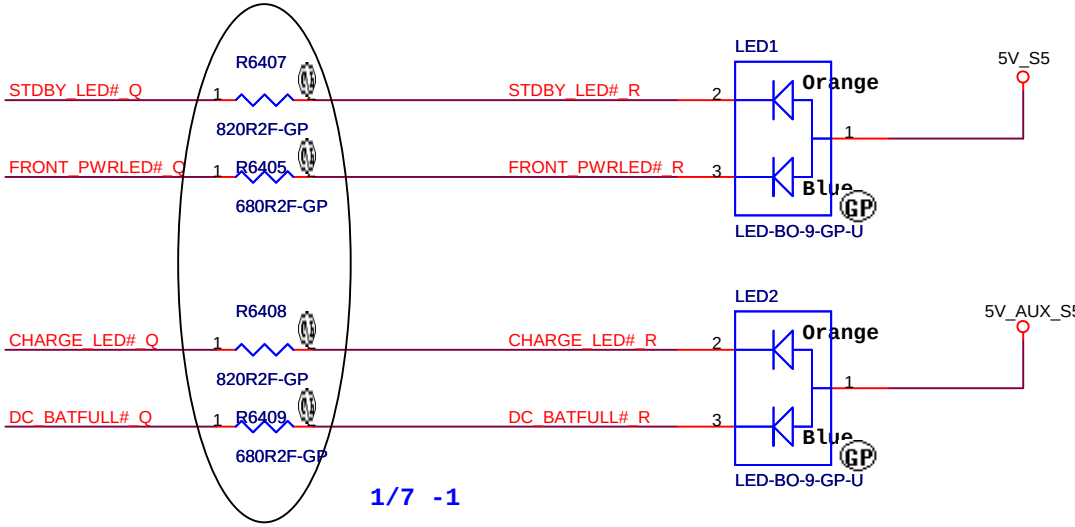


Battery LED2(DC_BATFULL)

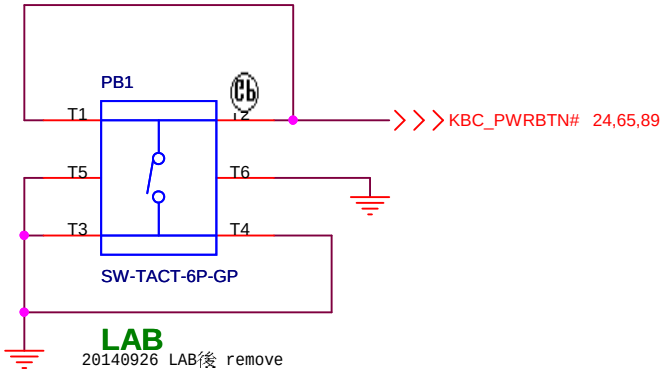


Battery LED1(CHARGE)





Power Button



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Title: *LED Bard/Powe Button*

Size	Document Number	Rev
A4	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 64 of 106

Internal Touch Pad

I2C Addr. = 0X2C (Synaptics)

Pin Number	Pin Name	Description
1	VDD	Power Supply Voltage
2	PS2_CLK	PS/2 Clock
3	PS2_DAT	PS/2 Data
4	GND	Ground
5	I2C_DATA	I²C Data
6	I2C_CLK	I²C Clock
7	ATTN	Attention
8	SENSOR OFF	Sensor Off

3D3V_TP_S3 — R6506 100KR2J-4-GP — Q6502 — 3D3V_S0 — TP_IN# — TP_IN#_R — 2N7002K-2-GP

2nd = 84.2N702.031

3rd = 84.2N702.W31

24 EC_TP_IN# — R6512 0R0402-PAD-1-GP

3D3V_TP_S3 — RN6503 SRN4K7J-8-GP — RN6502 SRN33J-5-GP-U

24 EC_TPCLK — 24 EC_TPDATA — EC_TP_CLK_C — EC_TP_DATA_C

I2C1_DATA_TP — I2C1_CLK_TP — TP_IN#_R — TP_LID_CLOSE#

24 FUN_OFF# — R6524 0R0402-PAD-1-GP

TPAD1 ACES-CON8-40-GP

20.K0667.008

2nd = 20.K0665.008

3D3V_TP_S3 — 3D3V_S0 — RN6505 SRN2K2J-5-GP — Q6503 2N7002K-2-GP

20 I2C1_CLK_CPU — I2C1_CLK_TP — EC6503 DY SCD1U16V2KX-L-GP

20 I2C1_DATA_CPU — I2C1_DATA_TP — EC6505 DY SCD1U16V2KX-L-GP

84.2N702.A3F

2nd = 75.00601.07C

3rd = 84.2N702.F3F

11/18 Chang 180 degree

3D3V_S5 — C6509 SC4D7U6D3V3KX-L-GP

3D3V_TP_S3 — C6504 SC4D7U6D3V3KX-L-GP

U6502 SY6288DAAC-GP — IN — EN# — OUT — GND — OC#

TPAD_PWRCTL — R6505 0R0402-PAD-1-GP

074.06288.009B

2nd = 074.00524.0C9F

3rd = 074.22802.0A9F

PTP_PWR_EN# 24

3D3V_S5 — 20141216 -1 — DY — R6507 100KR2J-4-GP — TPAD_PWRCTL

89 EC_TP_CLK_C — EC_TP_CLK_C

89 EC_TP_DATA_C — EC_TP_DATA_C

89 I2C1_DATA_TP — I2C1_DATA_TP

89 I2C1_CLK_TP — I2C1_CLK_TP

89 TP_IN#_R — TP_IN#_R

89 TP_LID_CLOSE# — TP_LID_CLOSE#

Internal KeyBoard Connector

KB1 ACES-CON28-9-GP — 020.K0130.0028

KROW0 KROW1 KROW2 KROW3 KROW4 KROW5 KROW6 KROW7 KROW8 KROW9 KROW10 KROW11 KROW12 KROW13 KROW14 KROW15 KROW16 KROW17

KCOL0 KCOL1 KCOL2 KCOL3 KCOL4 KCOL5 KCOL6 KCOL7

24,64,89 KBC_PWRBTN#

KROW[0..17] 24,89

KCOL[0..7] 24,89

P1-VCC — PWR — P2-GND

VIEW FROM TOP SIDE

PIN NUMBER

28 CARBON UP 1

C08 C07 C06 C05 C04 C03 C02 C01

R01 R02 R03 R04 R05 R06 R07 R08 R09 R10 R11 R12 R13 R14 R15 R16 R17 R18

PTWO-CON4-9-GP-U1 — KB_BL — KB_BL_DET_R — KB_LED_PWM_D — KB_BL1

R6504 100KR2J-4-GP — KB_BL

R6502 200KR2F-L-GP — KB_BL

5V_S0 — KB_BL_DET 24 — C6501 DY SCD1U16V2KX-L-GP

20.K0382.004

2nd = 20.K0465.004

3rd = 20.K0422.004

KB_BL

Q6501 2N7002K-2-GP

84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31

24 KB_BL_PWM — C6502 SCD1U16V2KX-L-GP DY

VCC Pin 1 — NC Pin 2 — VCC Pin 3 — GND Pin 4

KB_BL_DET_R — KB_BL_DET_R 89

KB_LED_PWM_D — KB_LED_PWM_D 89

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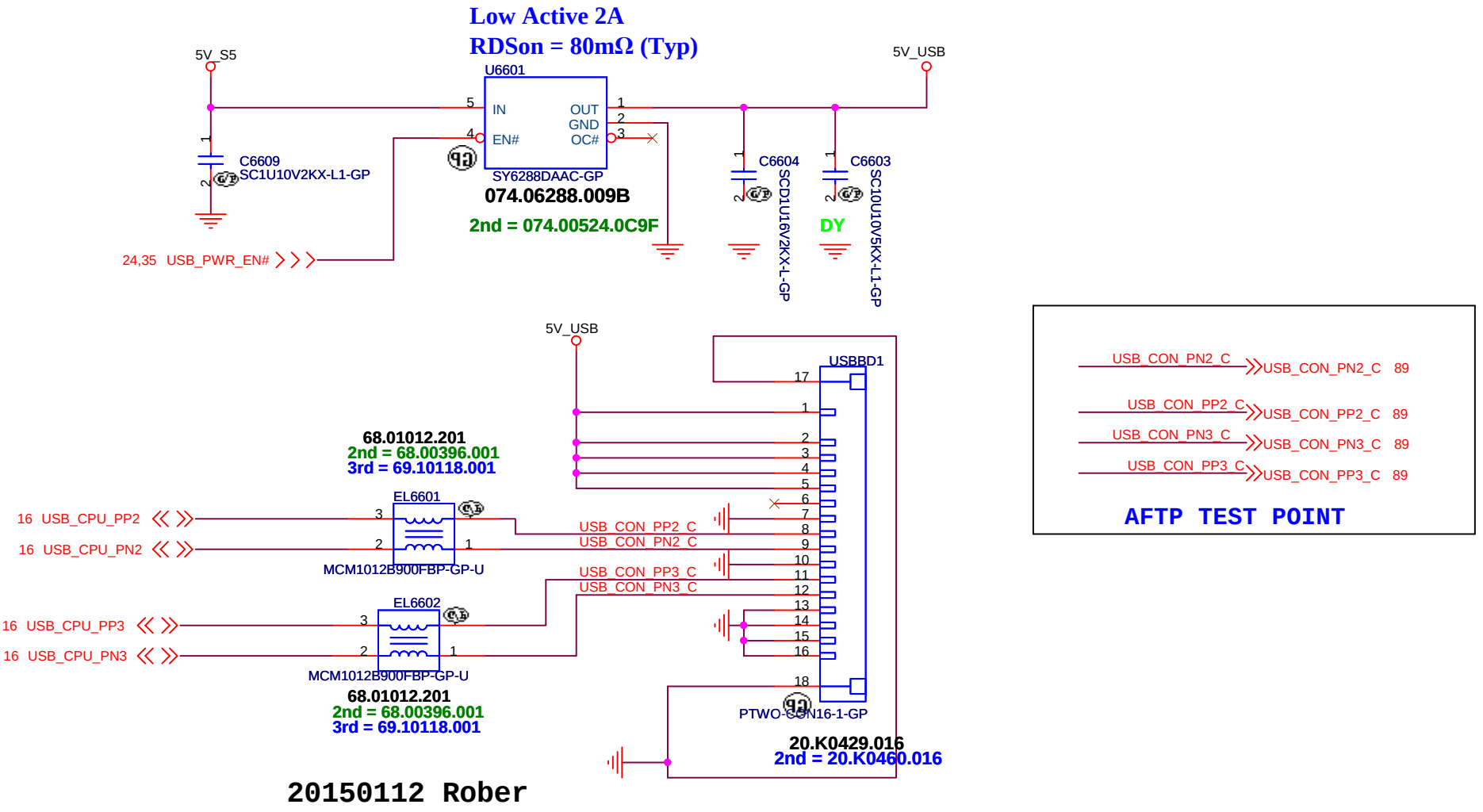
Title: Key Board/Touch Pad

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 65 of 106



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Title: ***IO Board***

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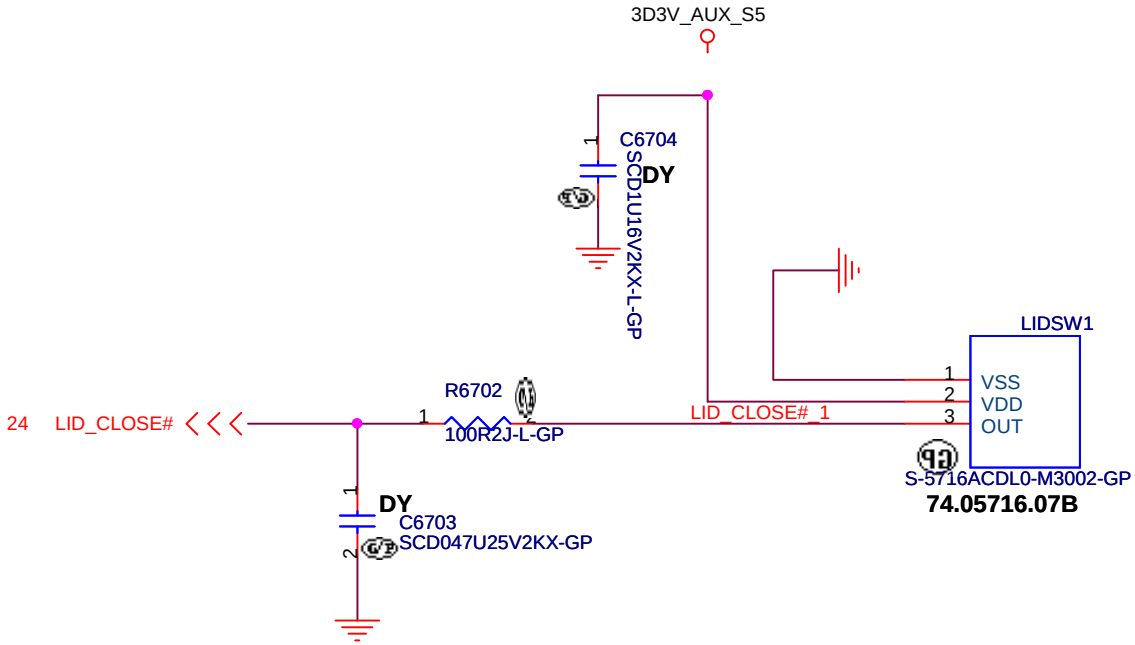

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Title

Hall Sensor

Size	Document Number	Rev
Custom	Brook_BH	-1M
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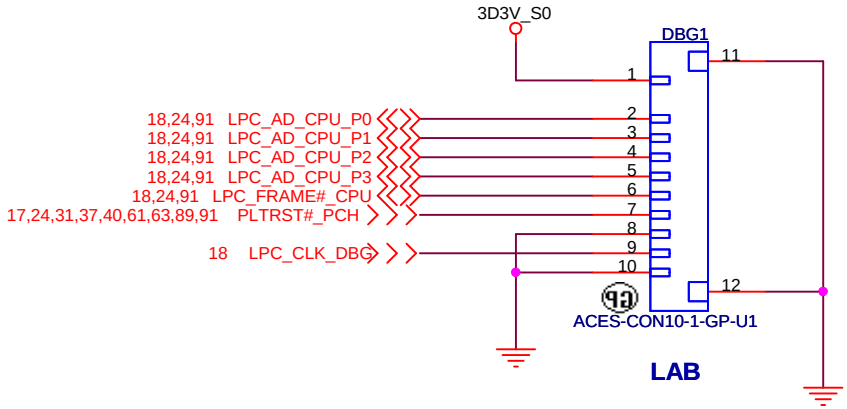

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Title: ***Dubug connector***

Size	Document Number	Rev
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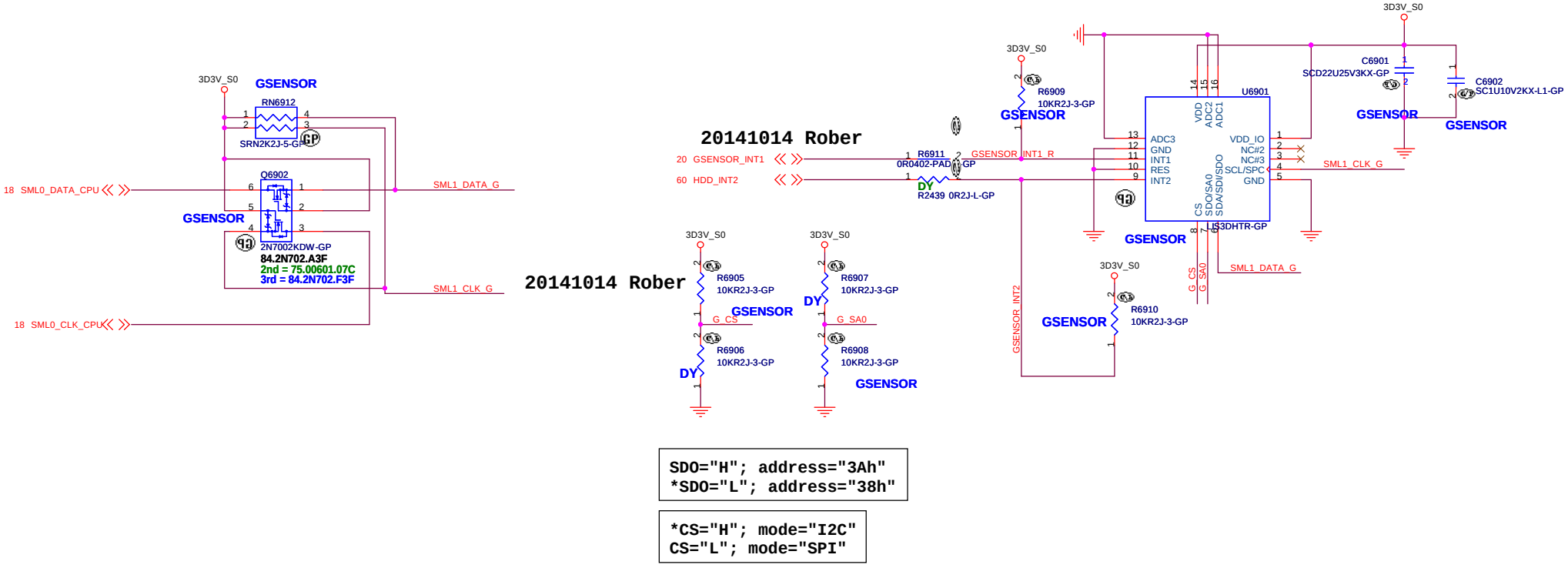
Date: Wednesday, February 04, 2015 Sheet 68 of 106

SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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Title: G-SENSOR

Size: A3 | Document Number: Brook_BH | Rev: -1M

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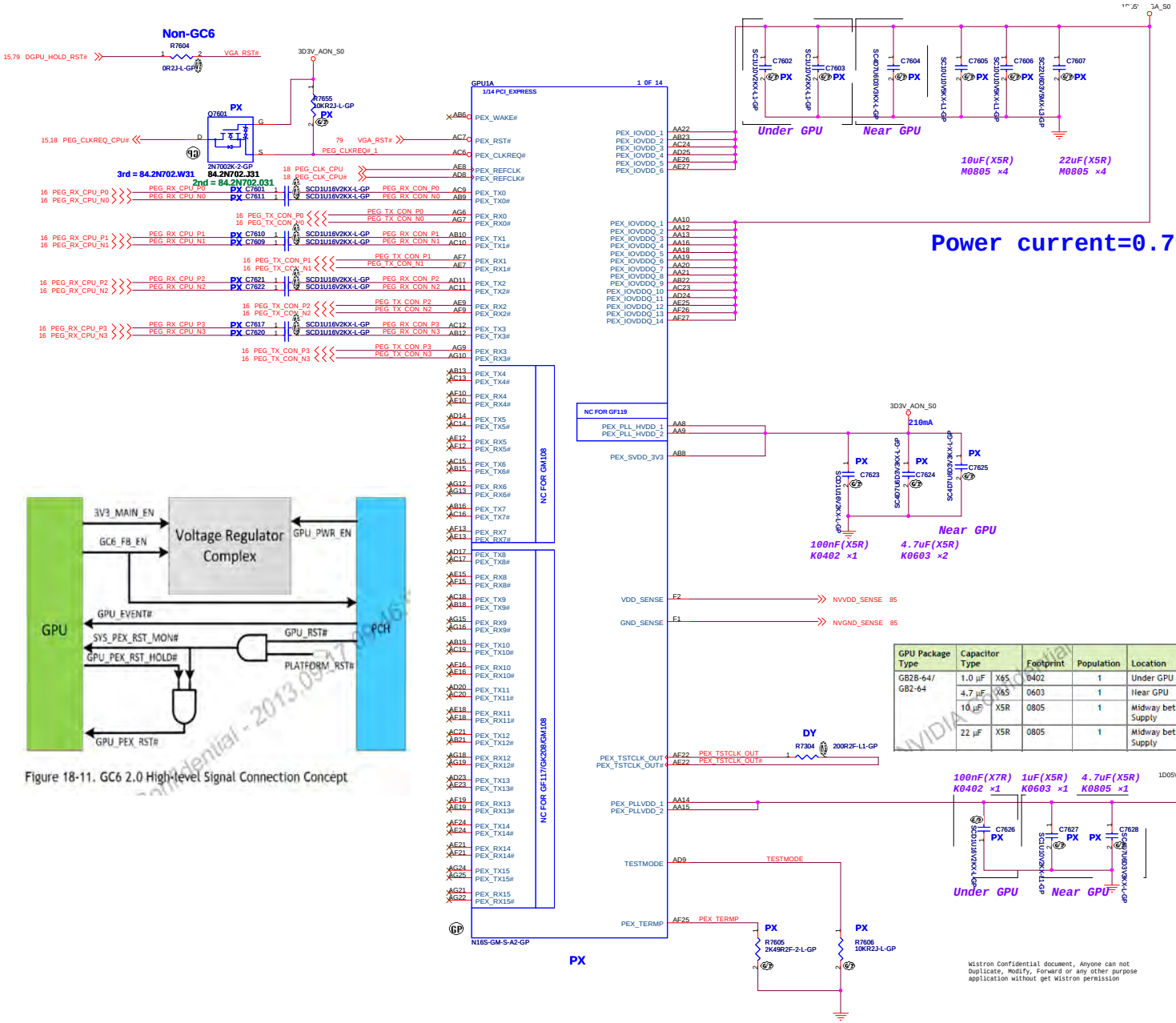

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3B-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

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Title: GPU (PEG)

Size: A2 | Document Number: Brook_BH | Rev: -1M

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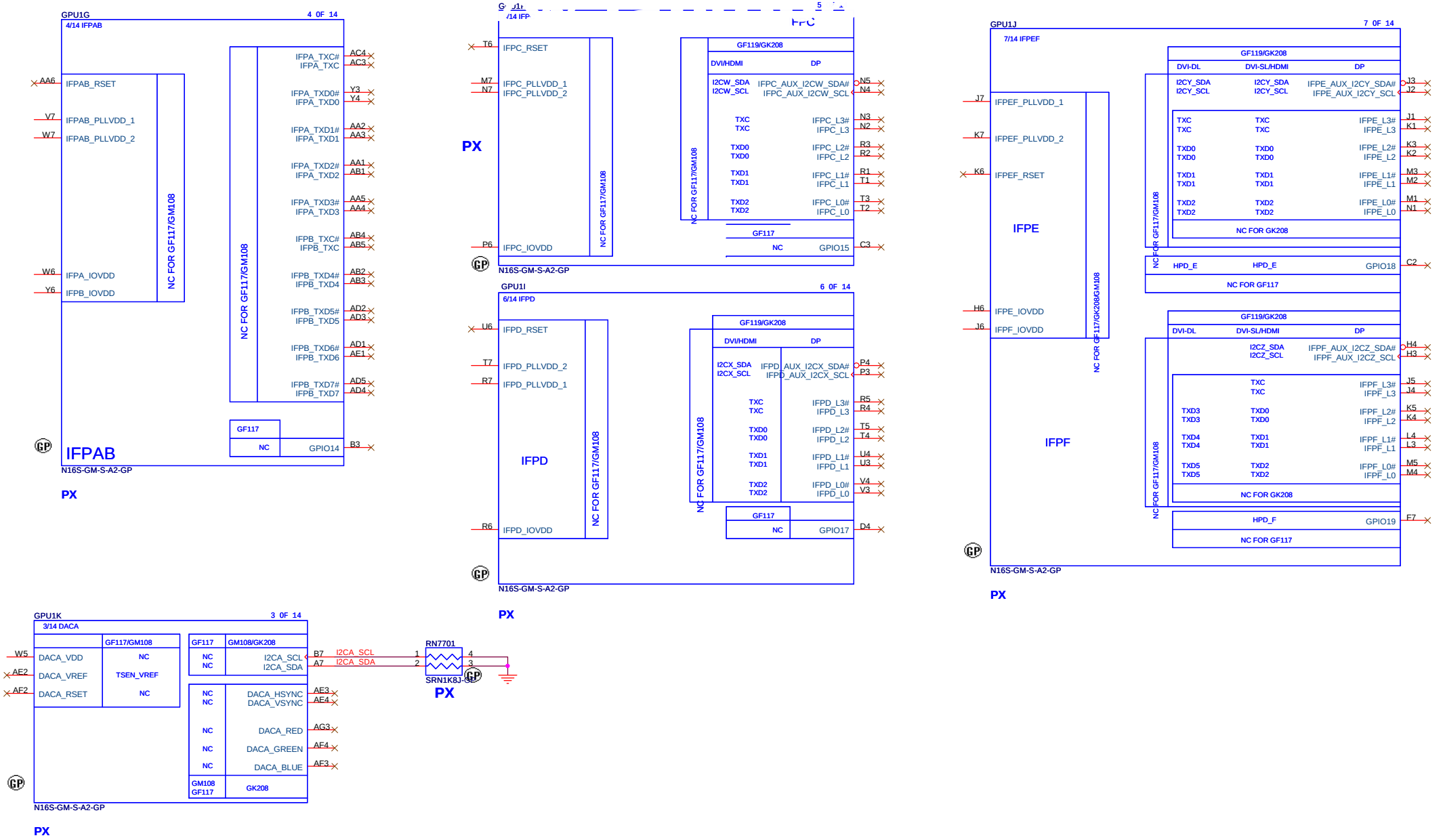

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Title: **GPU (DIGITALOUT)**

Size	Document Number	Rev
A3	Brook_BH	-1M

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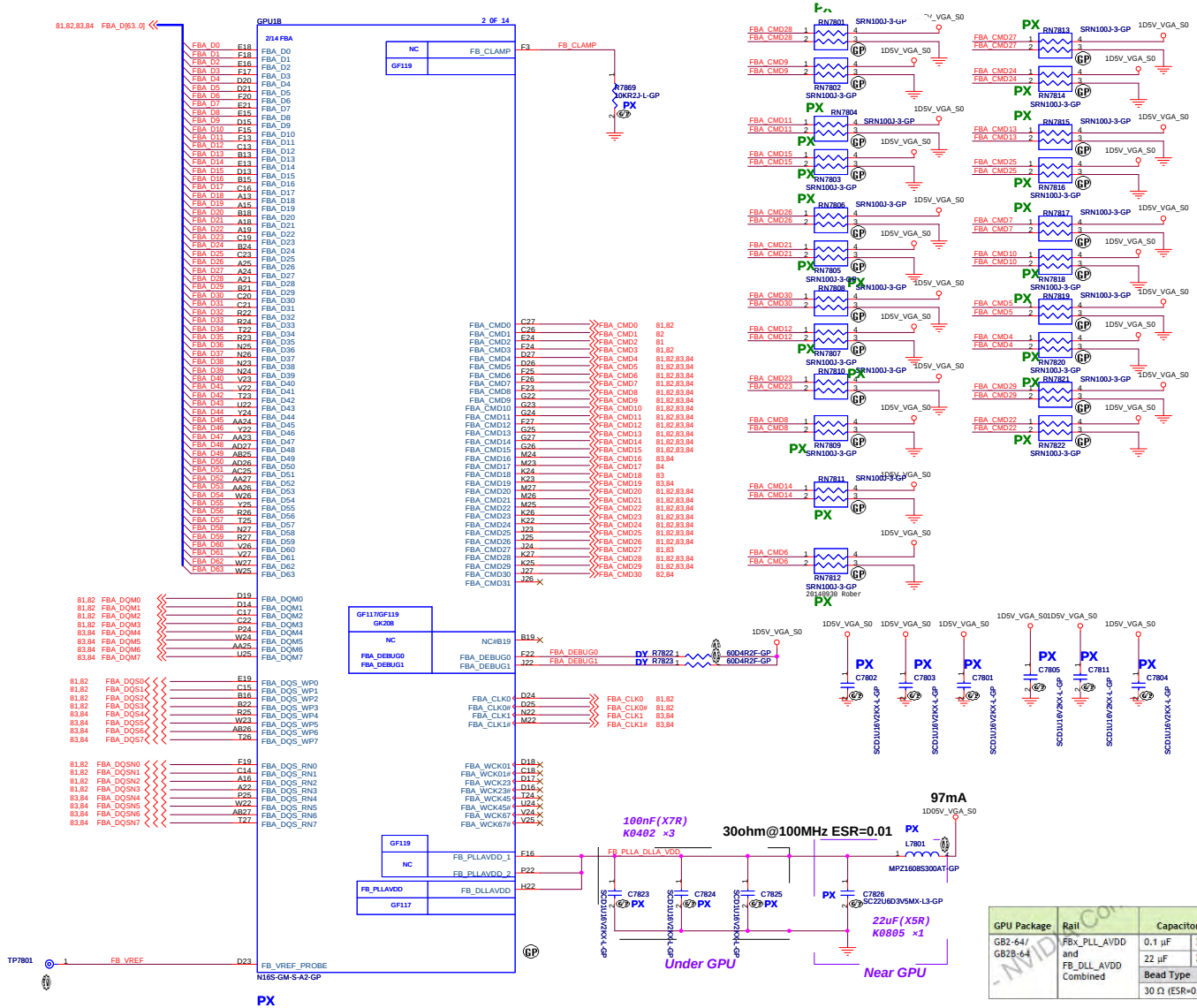


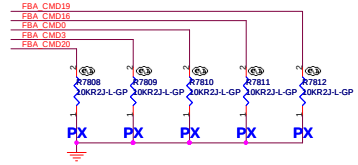
Table 6-4. Mode E Command Mapping

N16x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30		BA2	BA2	
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				
FBx_CMD34	DBG0[2]			
FBx_CMD35	DBG1[2]			

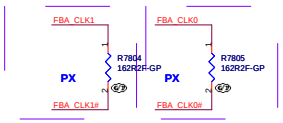
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Memory ODTx, CKEx and RST Termination



FBCLK Termination placed near each VRAM at board edge side



CHECK N16 Design guide P.98 Table 6-7

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Title: **GPU (VRAM I/F)**

Size: A2 | Document Number: **Brook_BH** | Rev: **-1M**

Date: Wednesday, February 04, 2015 | Sheet 78 of 106

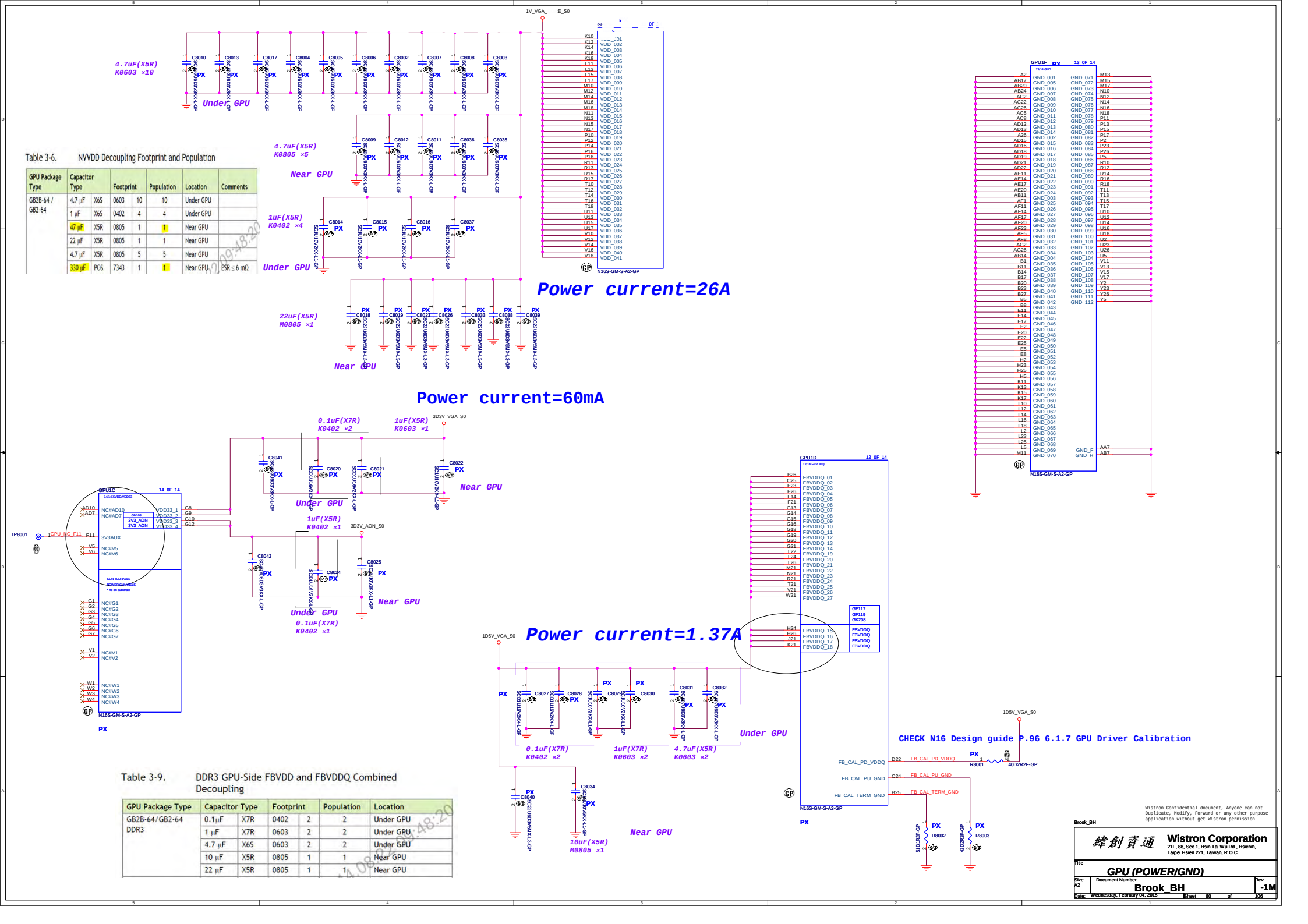

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint	Population		Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

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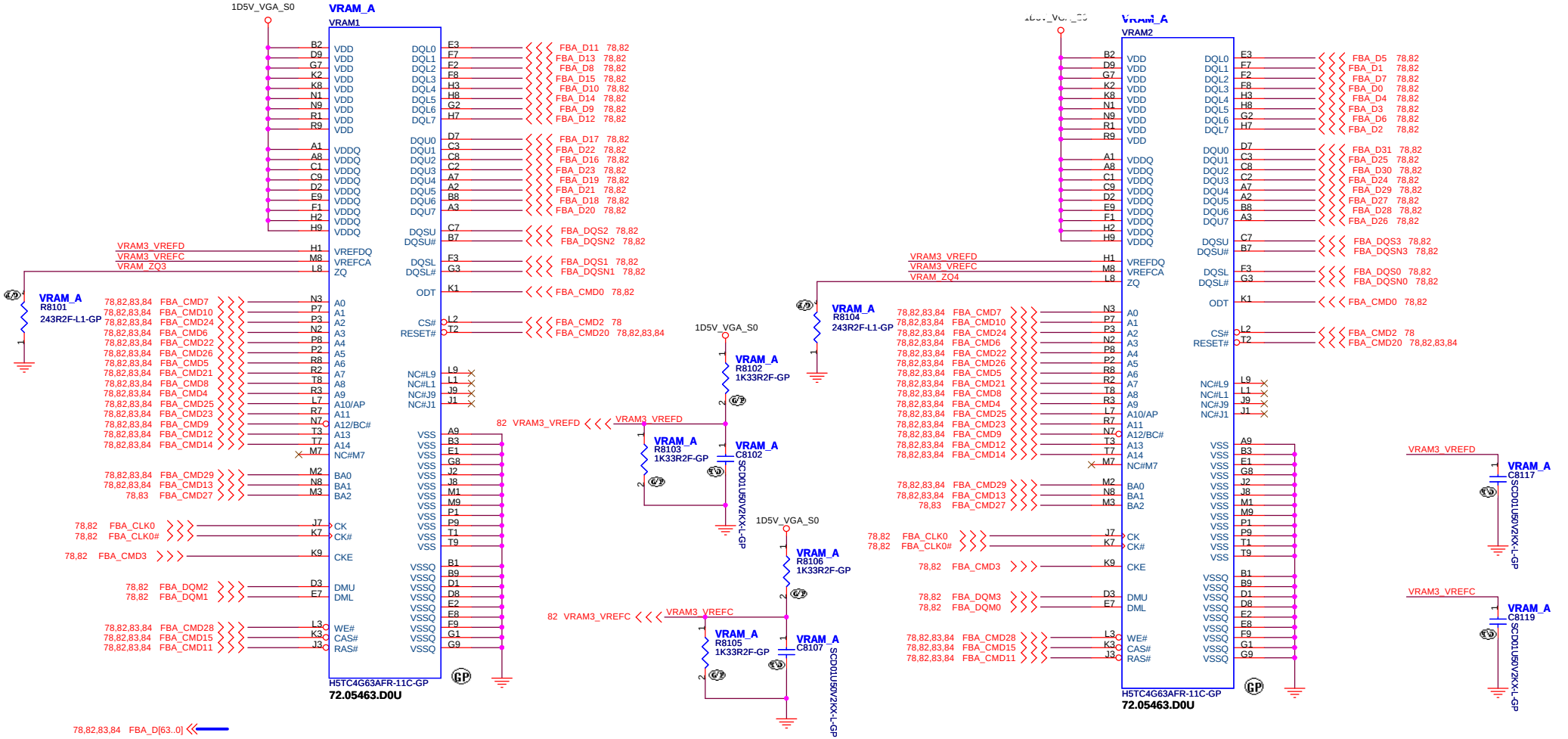
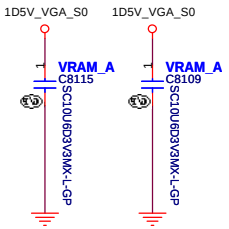
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (POWER/GND)

Size: A2 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 80 of 106





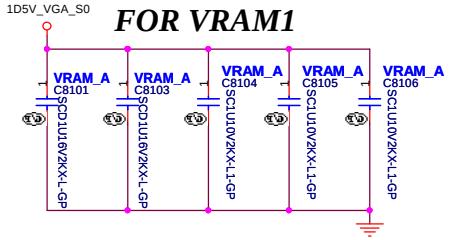
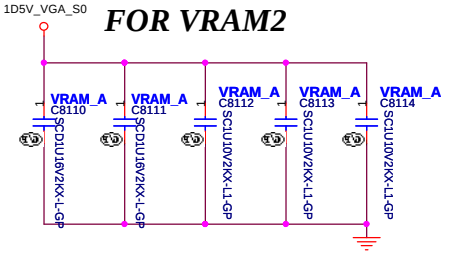
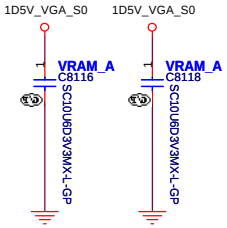


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combinod					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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Title: GPU-VRA1,2 (1/4)

Size: Custom | Document Number: Brook_BH | Rev: -1M

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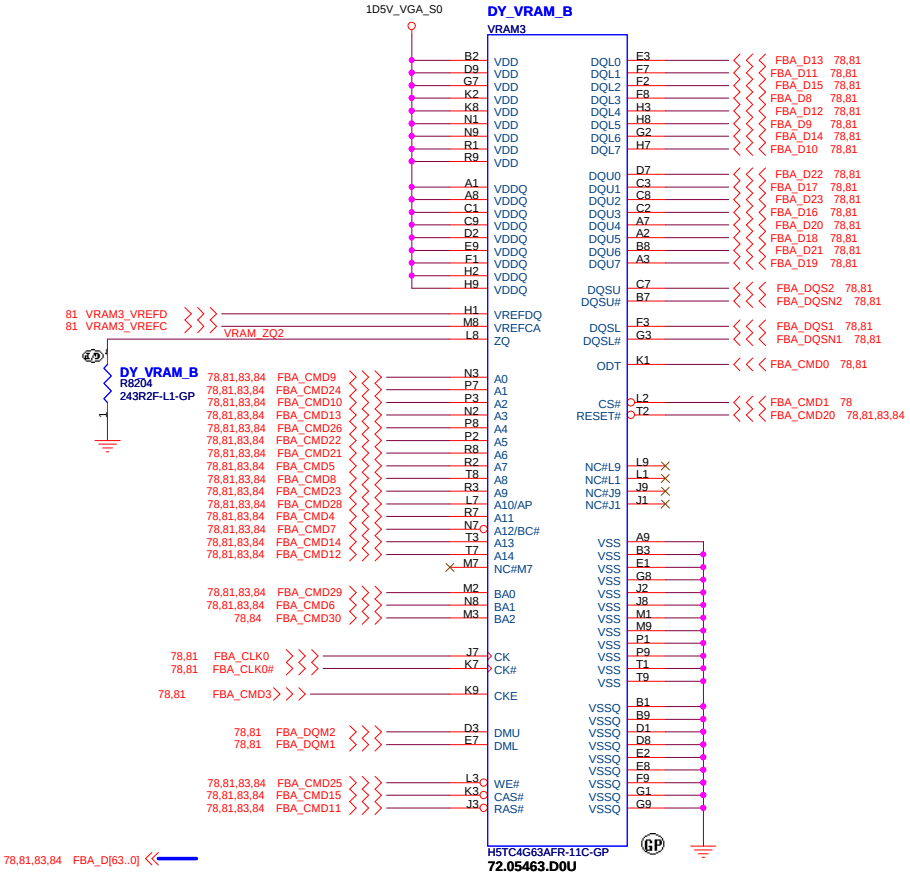
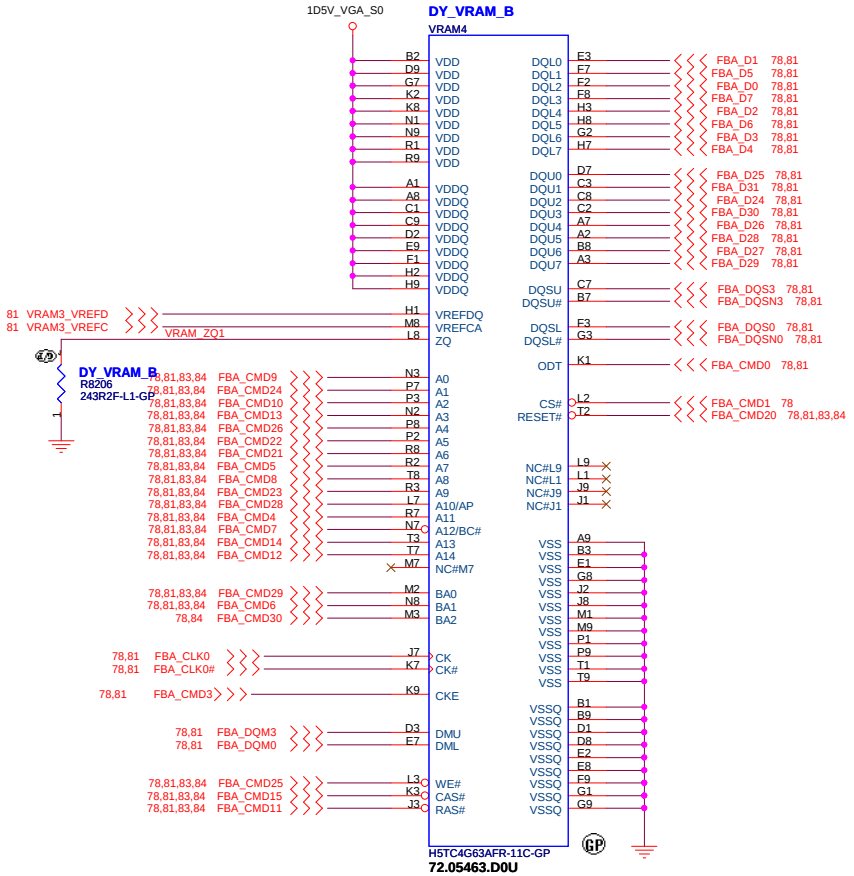
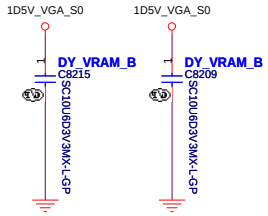
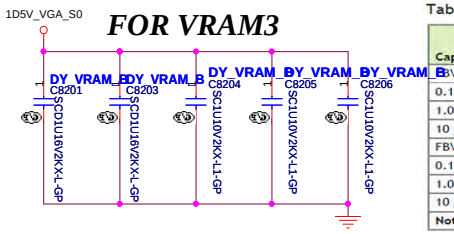






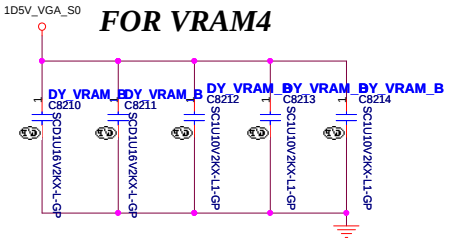


FOR VRAM3

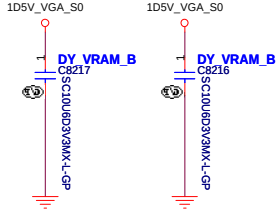
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



FOR VRAM4



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/4)**

Size: Custom | Document Number: **Brook_BH** | Rev: **-1M**

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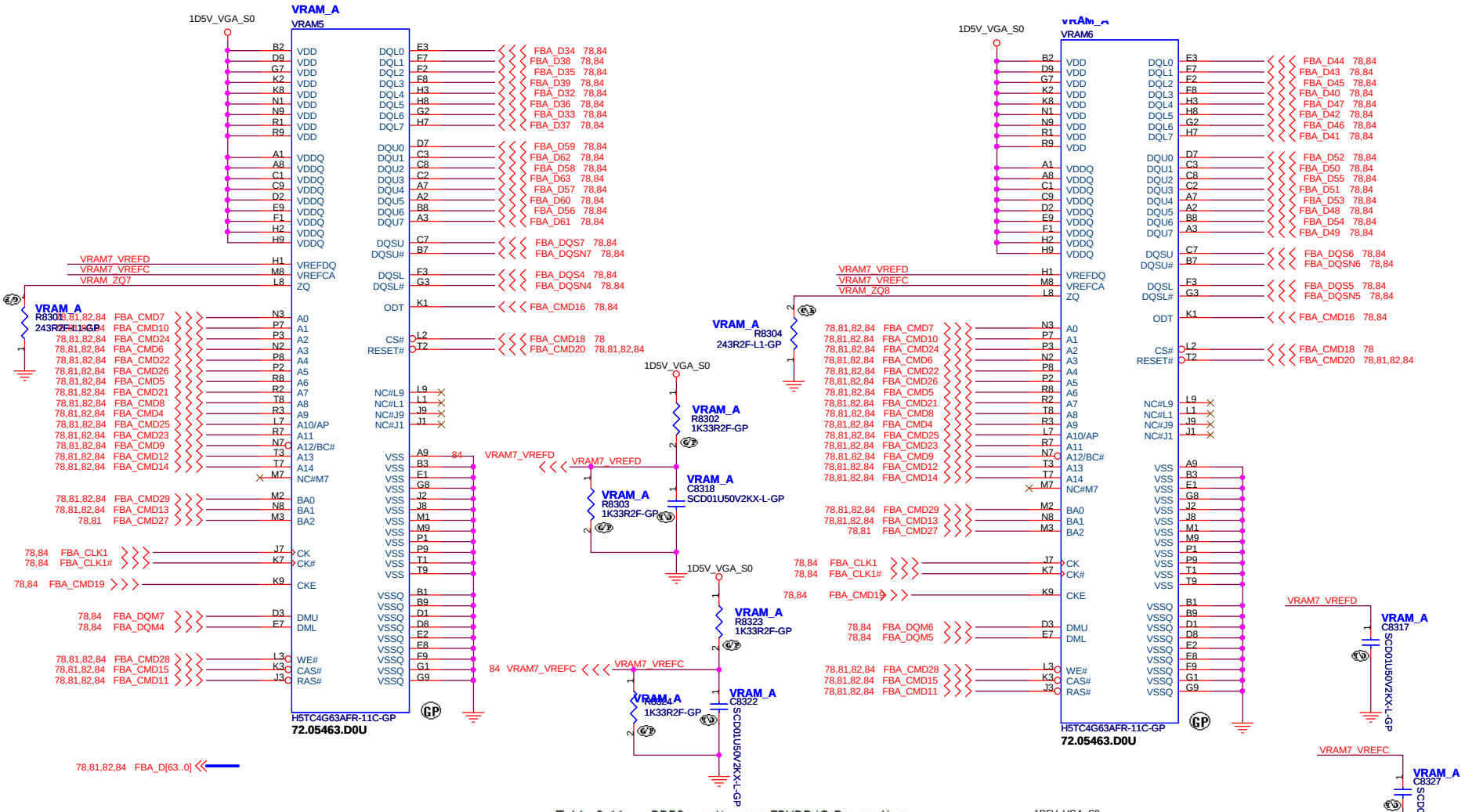


FOR VRAM5

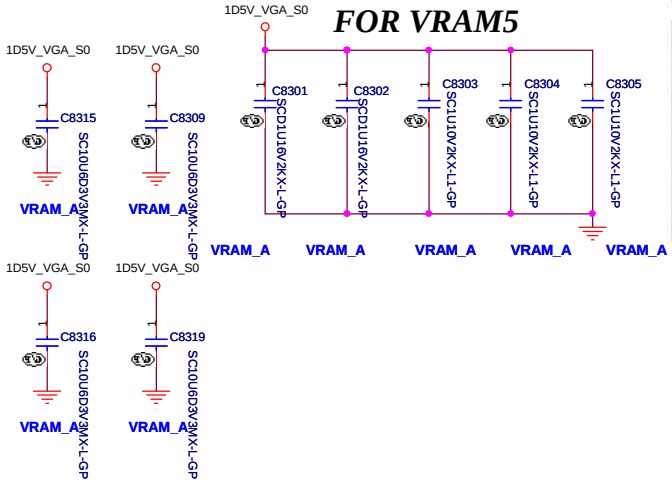
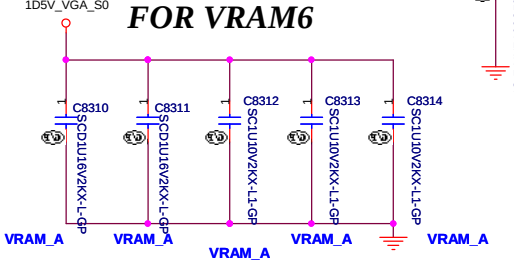


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

FOR VRAM6



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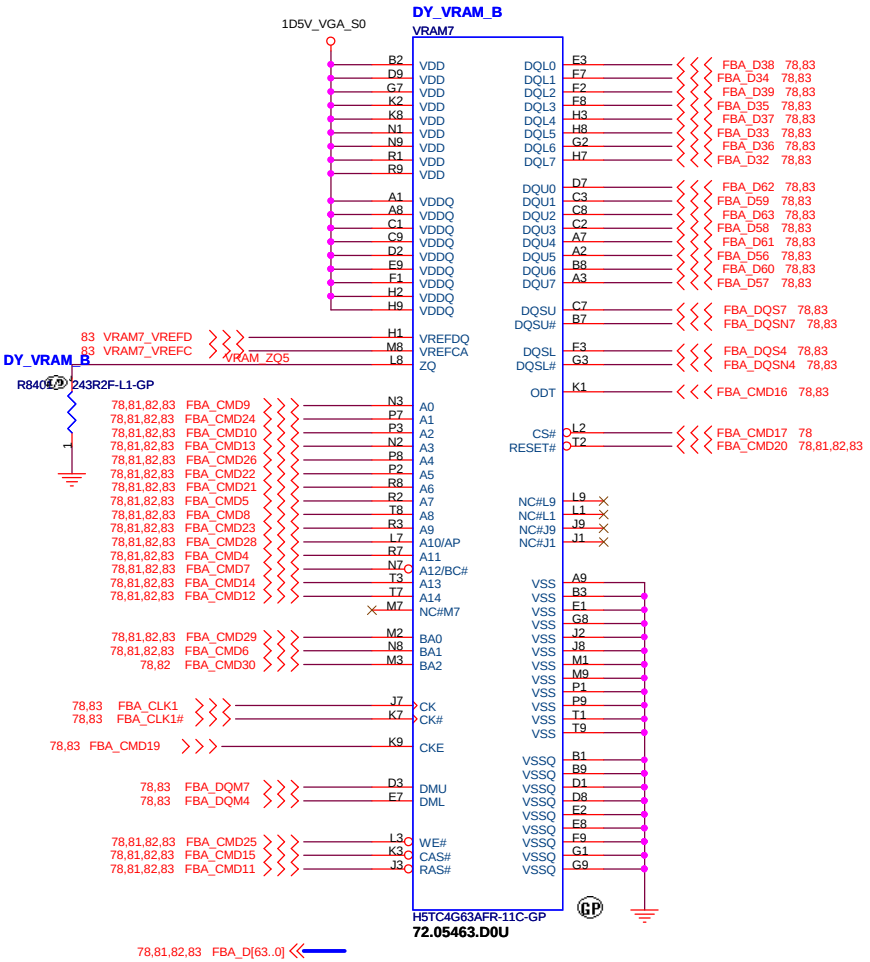
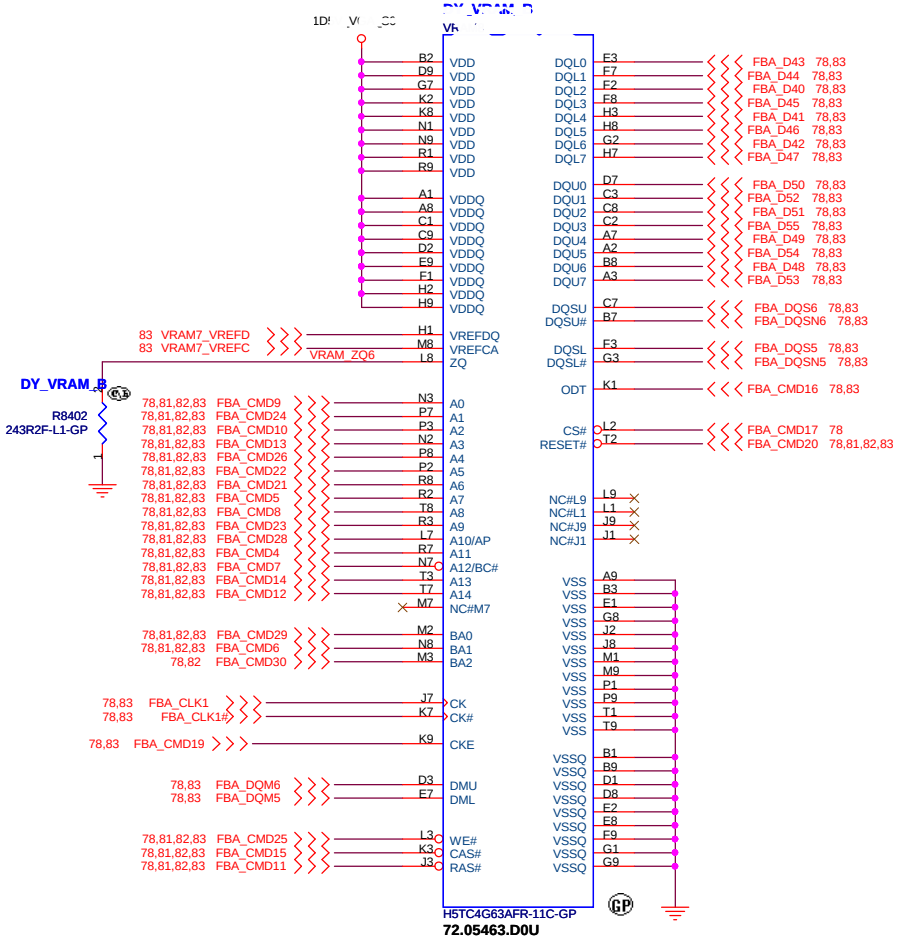
Taipei Hsien 221, Taiwan, R.O.C.

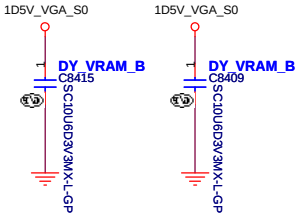
Title: GPU-VRAM7,8 (4/4)

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 83 of 106







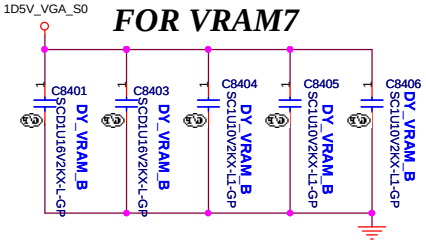
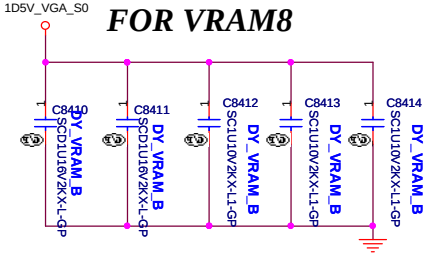
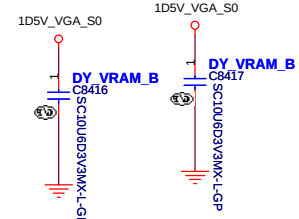


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

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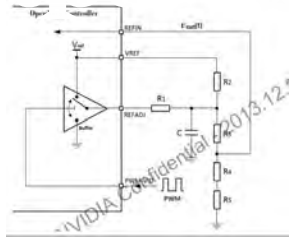
PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.45	1.15
Vboot	V	0.875	0.8	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6



19V_DCBATOUT
PWR_DCBATOUT_VGA_CORE
PG8501 GAP-CLOSE-PWR
PG8502 GAP-CLOSE-PWR
PG8503 GAP-CLOSE-PWR
PG8504 GAP-CLOSE-PWR
PG8505 GAP-CLOSE-PWR
PG8506 GAP-CLOSE-PWR
PG8507 GAP-CLOSE-PWR
PG8508 GAP-CLOSE-PWR

19V_DCBATOUT
DY PC8514 ST15U25VDM-1-GP
5V_S0
PR8523 2D2R3F-L-GP PX
VGA_PVCC
PC8507 SCD1U16V2KX-L-GP PX
PC8502 SCD1U25V2KX-L-GP PX
PWR_VGA_CORE_TON_1
PR8502 2D2R3F-L-GP PX
PR8501 499KR2F-1-GP PX
PWR_DCBATOUT_VGA_CORE

PU8501 RT8812AGQW-GP 74.08812.073

PWR_VGA_CORE_TON	9 TON	UGATE1 2	PWR_VGA_CORE_UGATE1
15,24,86 DGPU_PWROK	13 PGOOD	BOOT1 1	PWR_VGA_CORE_BOOT1
PWR_VGA_CORE_EN	3 EN	PHASE1 20	PWR_VGA_CORE_PHASE1
79 VGA_CORE_PSI	4 PSI	LGATE1 19	PWR_VGA_CORE_LGATE1
79 VGA_CORE_VID	5 VID	UGATE2 14	PWR_VGA_CORE_UGATE2_R
PWR_VGA_CORE_VREF	8 VREF	BOOT2 15	PWR_VGA_CORE_BOOT2
PWR_VGA_CORE_REFIN	7 REFIN	PHASE2 16	PWR_VGA_CORE_PHASE2
PWR_VGA_CORE_REFADJ	6 REFADJ	LGATE2 17	PWR_VGA_CORE_LGATE2
PWR_VGA_CORE_SS	11 SS	VSNS 12	PWR_VGA_CORE_VSNS
	21 GND	RGND 10	PWR_VGA_CORE_RGND

PR8518 0R3J-L1-GP PX
PC8511 SCD1U25V2KX-L-GP PX
PR8510 0R3J-L1-GP PX
OCP setting
PR8524 9K31R2F-GP PX
PR8519 0R3J-L1-GP PX
PR8511 0R3J-L1-GP PX
PC8506 SCD1U25V2KX-L-GP PX
PR8507 0R0402-PAD-1-GP
DY PC8503 SC1KP50V2KX-L-1-GP
DY PC8501 SCD1U16V2KX-L-GP
PR8506 20KR2F-L3-GP PX
PR8522 20KR2F-L3-GP PX
PR8508 2KR2F-L1-GP PX
DY PC8505 SC1KP50V2KX-L-1-GP
PC8523 SC2700P50V2KX-1-GP PX
PR8509 18KR2F-GP PX
DY PC8504 SCD01U50V2KX-L-GP

PU8503 PU8504 FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00920.037
2nd = 084.07321.0037
PX 3rd = 84.08S36.037
DY 3rd = 84.08S36.037

PWR_DCBATOUT_VGA_CORE
PX PC8508 SC10U25V5KX-GP
PX PC8509 SC10U25V5KX-GP
PX PC8520 SCD1U25V2KX-L-GP

Mag. 7.5 X 6.7 X 4.0 mm
DCR: 1 mohm
Idc : 45A , Isat : 27A
1V_VGA_CORE_S0
PL8501 IND-D24UH-2-GP PX
68.R2410.101
2nd = 68.R2410.20A

Design Current
= 26A
OCP> 39A

PU8505 PU8506 FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00920.037
2nd = 084.07321.0037
PX 3rd = 84.08S36.037
DY 3rd = 84.08S36.037

PWR_DCBATOUT_VGA_CORE
PX PC8512 SC10U25V5KX-GP
PX PC8513 SC10U25V5KX-GP
PX PC8521 SCD1U25V2KX-L-GP

Mag. 7.5 X 6.7 X 4.0 mm
DCR: 1 mohm
Idc : 45A , Isat : 27A
PL8502 IND-D24UH-2-GP PX
68.R2410.101
2nd = 68.R2410.20A

1V_VGA_CORE_S0
77.53371.18L
2nd = 79.3371V.6CL
PT8507 PT8508 SE330U2D5VM-8-GP PX

PC8519 SC47P50V2JN-3GP
DY PC8522 SC47P50V2JN-3GP
DY PC8517 SC47P50V2JN-3GP
PR8521 0R0402-PAD-1-GP NVVDD_SENSE 76
PR8520 0R0402-PAD-1-GP NVGND_SENSE 76

3D3V_VGA_CORE
20141216 -1
PX RN8512 N10KJ-L-GP
DGPU_PWROK
PWR_VGA_CORE_EN PWR_VGA_CORE_EN 87
86 DGPU_PWR_EN
DY PR8560 0R3J-L1-GP
DGPU_PWR_EN_D1
PC8525 SCD1U25V2KX-L-GP PX
DY PD8501 BAW56-5-GP

1V_VGA_CORE_S0
RN8515 SRN100J-GP
PWR_VGA_CORE_VSNS
PWR_VGA_CORE_RGND
20141216 -1
PX

Brook_BL

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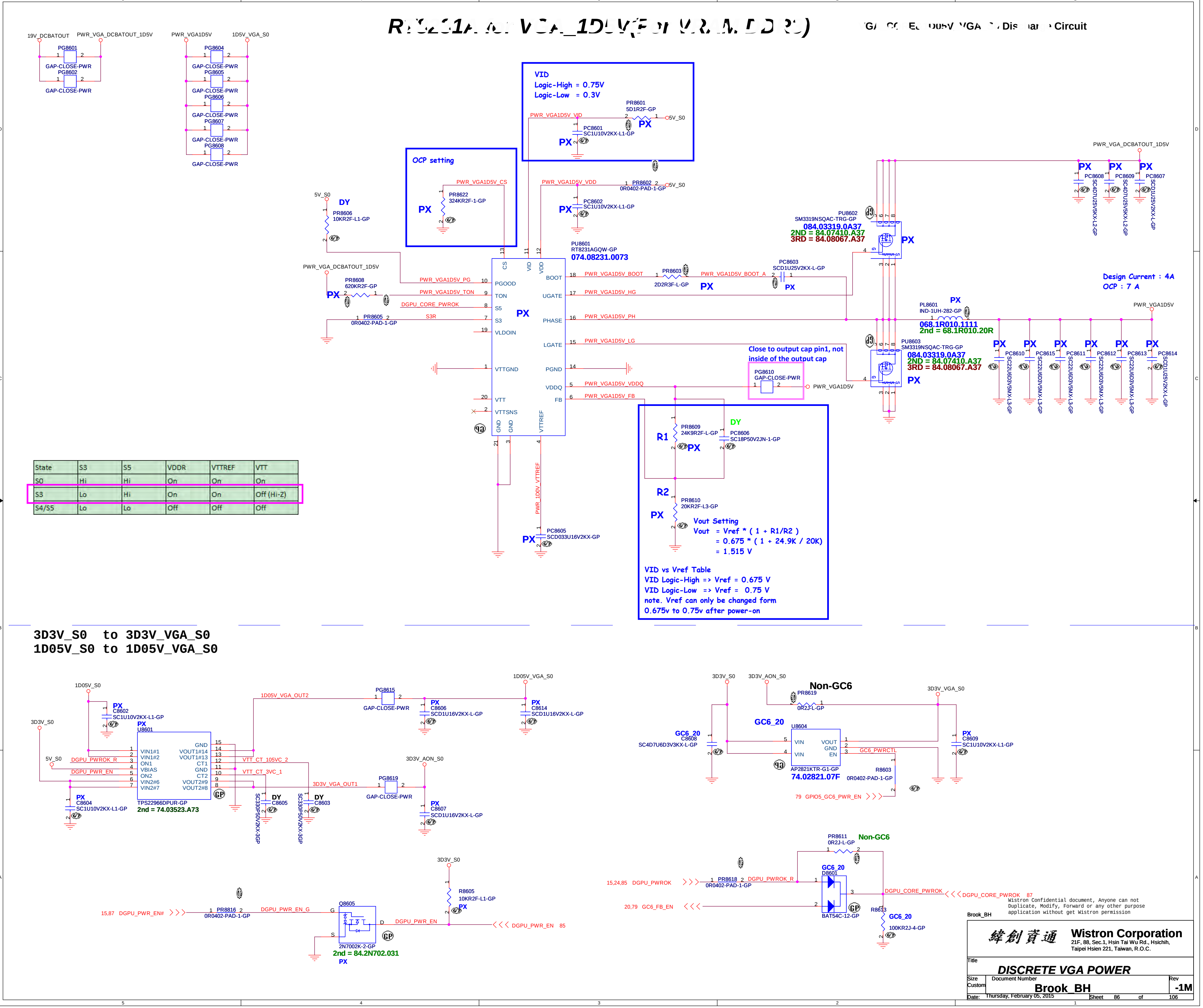
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8812A_VGA_CORE
Size: Custom | Document Number: Brook_BL | Rev: -1M
Date: Wednesday, February 04, 2015 | Sheet 85 of 106

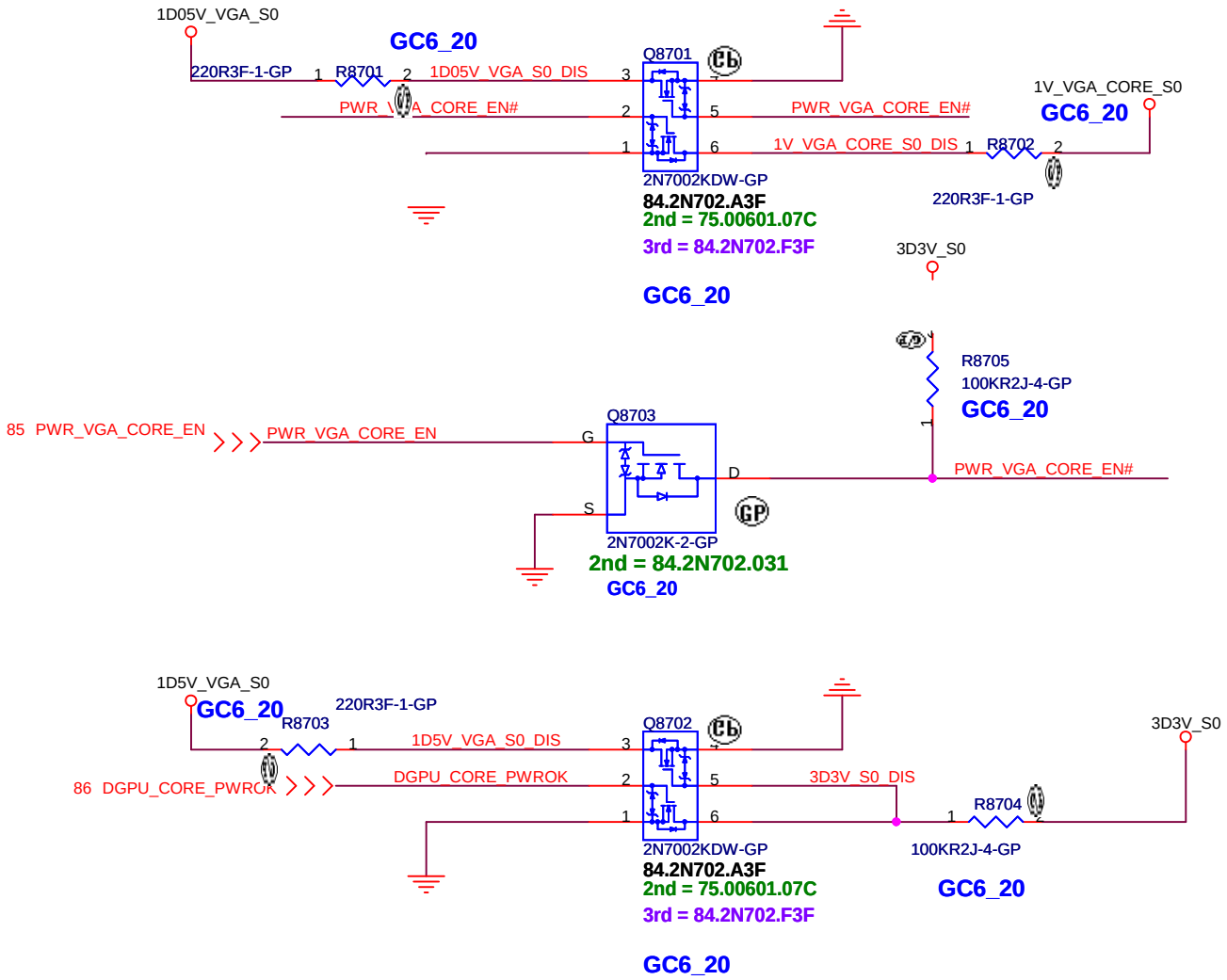


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Document Number: Brook_BH   Rev: -1M



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Title
DISCHARGE

Size	Document Number	Rev
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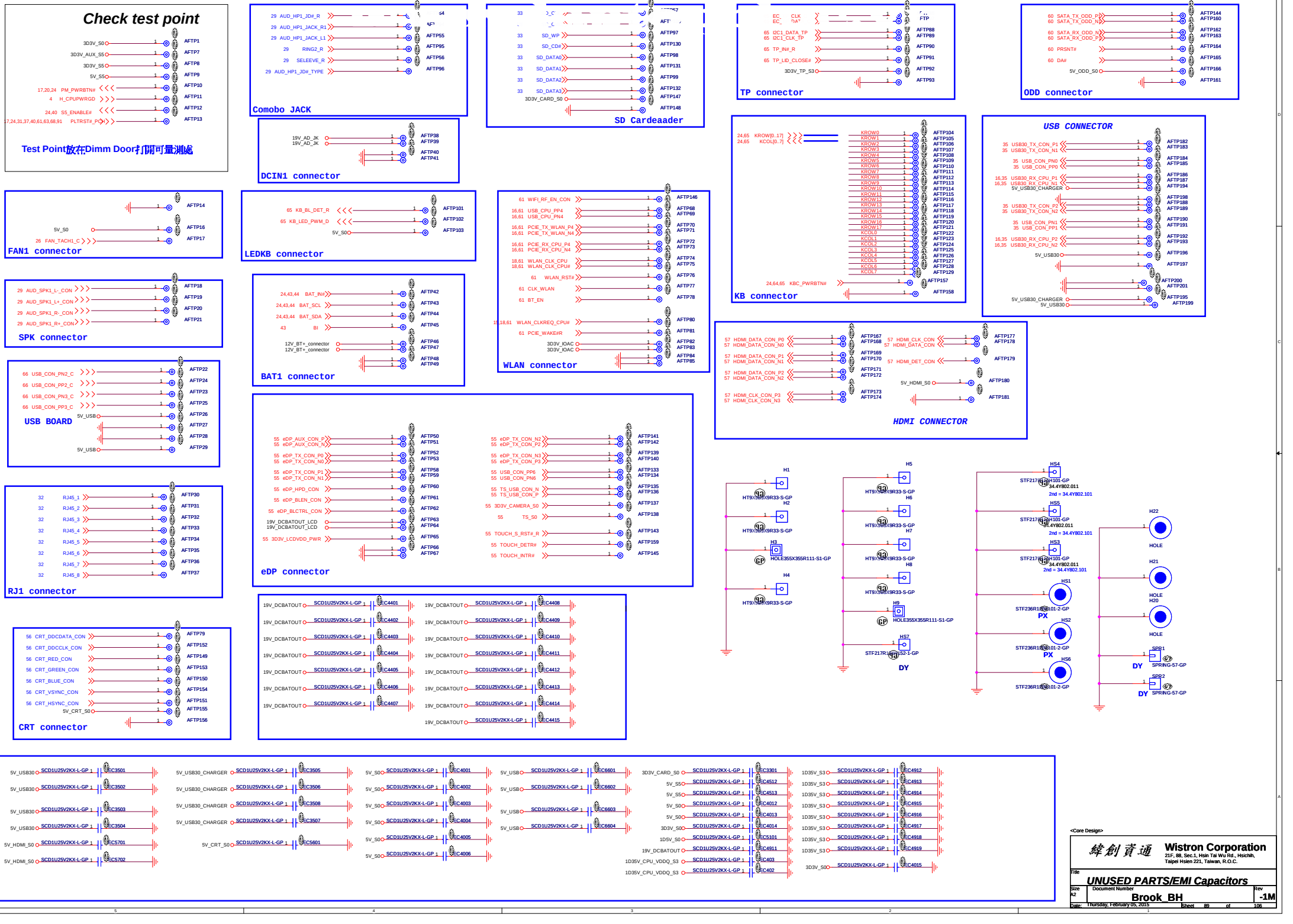
Check test point
3D3V_S0 AFTP1
3D3V_AUX_S5 AFTP7
3D3V_S5 AFTP8
5V_S5 AFTP9
17,20,24 PM_PWRBTN# AFTP10
4 H_CPUPWRGD AFTP11
24,40 S5_ENABLE# AFTP12
17,24,31,37,40,61,63,68,91 PLTRST#_P AFTP13
Test Point放在Dimm Door打開可量測處
Comobo JACK
29 AUD_HP1_JD#_R
29 AUD_HP1_JACK_R1
29 AUD_HP1_JACK_L1
29 RING2_R
29 SELEEVE_R
29 AUD_HP1_JD#_TYPE
AFTP55
AFTP95
AFTP56
AFTP96
SD Cardeaader
33 SD_WP AFTP97
33 SD_CD# AFTP130
33 SD_DATA0 AFTP98
33 SD_DATA1 AFTP131
33 SD_DATA2 AFTP99
33 SD_DATA3 AFTP132
3D3V_CARD_S0 AFTP147
AFTP148
TP connector
EC_CLK
EC_DAT
FTP
65 I2C1_DATA_TP AFTP88
65 I2C1_CLK_TP AFTP89
65 TP_INT_R AFTP90
65 TP_LID_CLOSE# AFTP91
3D3V_TP_S3 AFTP92
AFTP93
ODD connector
60 SATA_TX_ODD_P AFTP144
60 SATA_TX_ODD_N AFTP160
60 SATA_RX_ODD_N AFTP162
60 SATA_RX_ODD_P AFTP163
60 PRSNT# AFTP164
60 DA# AFTP165
5V_ODD_S0 AFTP166
AFTP161
DCIN1 connector
19V_AD_JK AFTP38
19V_AD_JK AFTP39
AFTP40
AFTP41
FAN1 connector
AFTP14
5V_S0 AFTP16
26 FAN_TACH1_C AFTP17
LEDKB connector
65 KB_BL_DET_R AFTP101
65 KB_LED_PWM_D AFTP102
5V_S0 AFTP103
KB connector
24,65 KROW[0..17]
24,65 KCOL[0..7]
KROW0 AFTP104
KROW1 AFTP105
KROW2 AFTP106
KROW3 AFTP107
KROW4 AFTP108
KROW5 AFTP109
KROW6 AFTP110
KROW7 AFTP111
KROW8 AFTP112
KROW9 AFTP113
KROW10 AFTP114
KROW11 AFTP115
KROW12 AFTP116
KROW13 AFTP117
KROW14 AFTP118
KROW15 AFTP119
KROW16 AFTP120
KROW17 AFTP121
KCOL0 AFTP122
KCOL1 AFTP123
KCOL2 AFTP124
KCOL3 AFTP125
KCOL4 AFTP126
KCOL5 AFTP127
KCOL6 AFTP128
KCOL7 AFTP129
24,64,65 KBC_PWRBTN# AFTP157
AFTP158
USB CONNECTOR
35 USB30_TX_CON_P1 AFTP182
35 USB30_TX_CON_N1 AFTP183
35 USB_CON_PN0 AFTP184
35 USB_CON_PP0 AFTP185
16,35 USB30_RX_CPU_P1 AFTP186
16,35 USB30_RX_CPU_N1 AFTP187
5V_USB30_CHARGER AFTP194
AFTP198
35 USB30_TX_CON_P2 AFTP188
35 USB30_TX_CON_N2 AFTP189
35 USB_CON_PN1 AFTP190
35 USB_CON_PP1 AFTP191
16,35 USB30_RX_CPU_P2 AFTP192
16,35 USB30_RX_CPU_N2 AFTP193
5V_USB30 AFTP196
AFTP197
AFTP200
AFTP201
5V_USB30_CHARGER AFTP195
5V_USB30 AFTP199
SPK connector
29 AUD_SPK1_L-_CON AFTP18
29 AUD_SPK1_L+_CON AFTP19
29 AUD_SPK1_R-_CON AFTP20
29 AUD_SPK1_R+_CON AFTP21
BAT1 connector
24,43,44 BAT_IN# AFTP42
24,43,44 BAT_SCL AFTP43
24,43,44 BAT_SDA AFTP44
43 BI AFTP45
12V_BT+_connector AFTP46
12V_BT+_connector AFTP47
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16,61 USB_CPU_PN4 AFTP69
16,61 PCIE_TX_WLAN_P4 AFTP70
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18,61 WLAN_CLK_CPU AFTP74
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61 WLAN_RST# AFTP76
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57 HDMI_DATA_CON_N0 AFTP168
57 HDMI_DATA_CON_P1 AFTP169
57 HDMI_DATA_CON_N1 AFTP170
57 HDMI_DATA_CON_P2 AFTP171
57 HDMI_DATA_CON_N2 AFTP172
57 HDMI_CLK_CON_P3 AFTP173
57 HDMI_CLK_CON_N3 AFTP174
57 HDMI_CLK_CON AFTP177
57 HDMI_DATA_CON AFTP178
57 HDMI_DET_CON AFTP179
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eDP connector
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55 eDP_TX_CON_N3 AFTP139
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32 RJ45_6 AFTP35
32 RJ45_7 AFTP36
32 RJ45_8 AFTP37
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56 CRT_DDCCLK_CON AFTP152
56 CRT_RED_CON AFTP149
56 CRT_GREEN_CON AFTP153
56 CRT_BLUE_CON AFTP150
56 CRT_VSYNC_CON AFTP154
56 CRT_HSYNC_CON AFTP151
5V_CRT_S0 AFTP155
AFTP156
19V_DCBATOUT SCD1U25V2KX-L-GP 1 EC4401
EC4402
EC4403
EC4404
EC4405
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EC4415
5V_USB30 SCD1U25V2KX-L-GP 1 EC3501
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EC3503
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5V_HDMI_S0 EC5701
EC5702
5V_USB30_CHARGER EC3505
EC3506
EC3508
EC3507
5V_CRT_S0 EC5601
5V_S0 EC4001
EC4002
EC4003
EC4004
EC4005
EC4006
5V_USB EC6601
EC6602
EC6603
EC6604
3D3V_CARD_S0 EC3301
5V_S5 EC4512
EC4513
5V_S0 EC4012
EC4013
3D3V_S0 EC4014
1D5V_S0 EC5101
19V_DCBATOUT EC4911
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EC402
1D3V_S3 EC4912
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EC4914
EC4915
EC4916
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EC4918
EC4919
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H1
HT9X355X9R33-S-GP
H2
H3
HOLE355X355R111-S1-GP
H4
H5
H6
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H9
HS7
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DY
HS4
STF217R4H101-GP
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HS5
HS3
HS1
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Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
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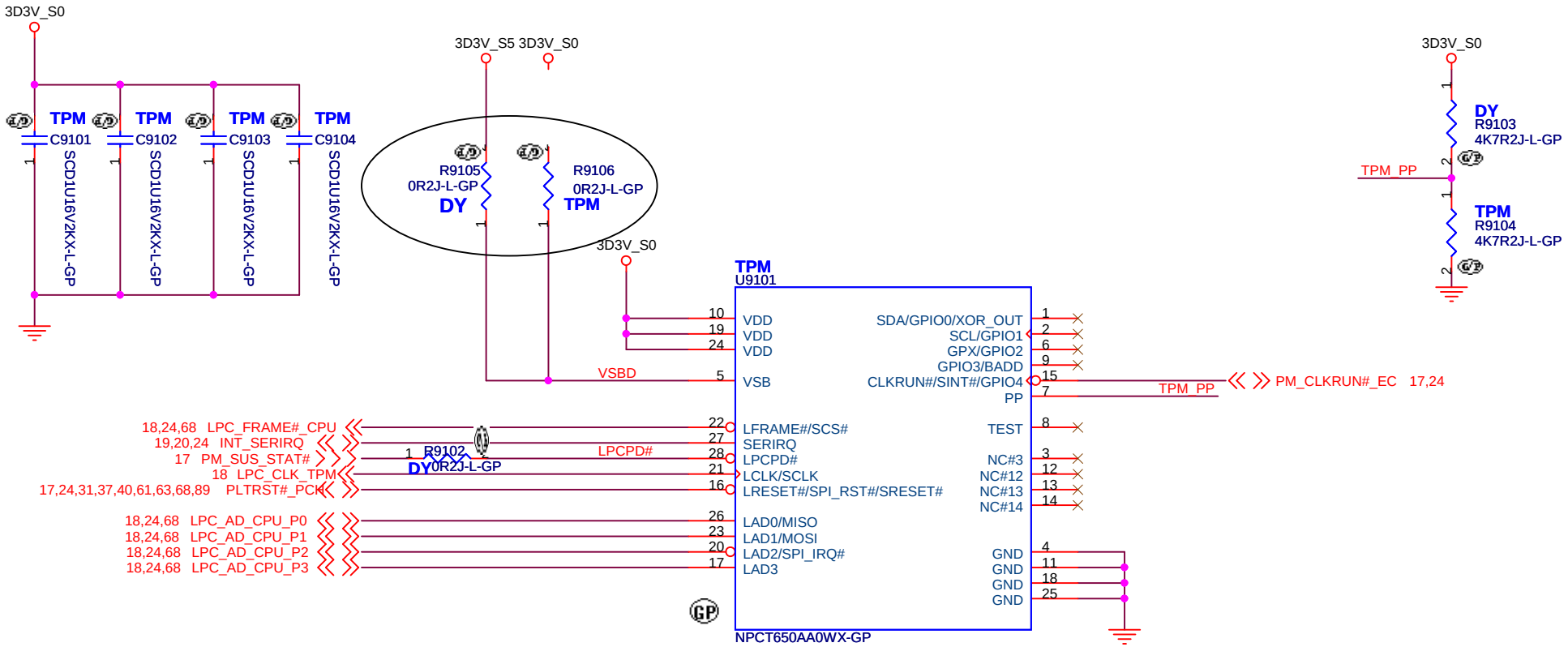

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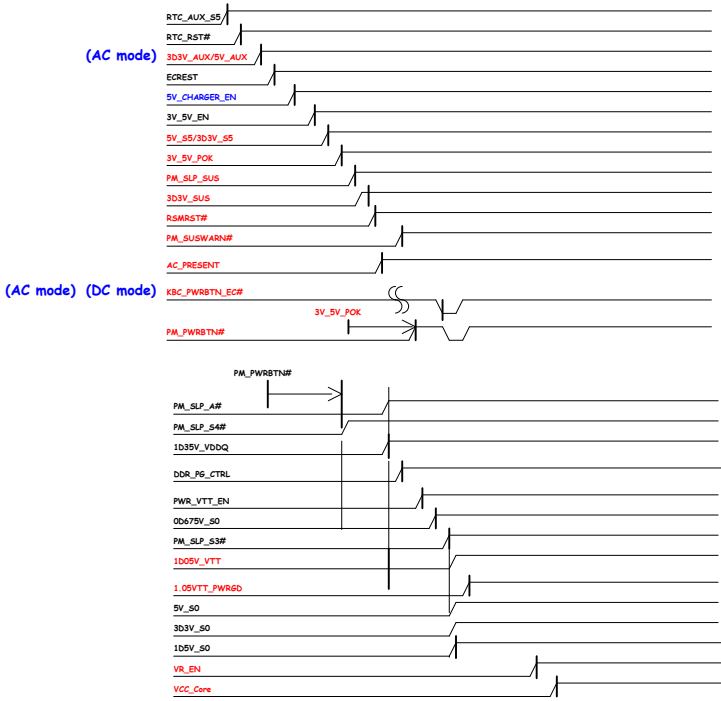
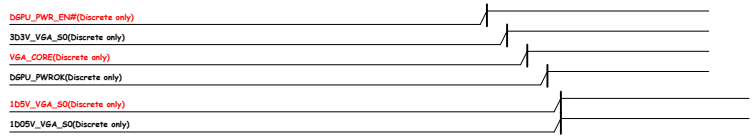
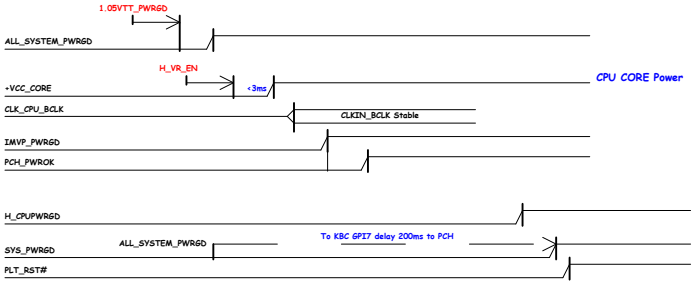
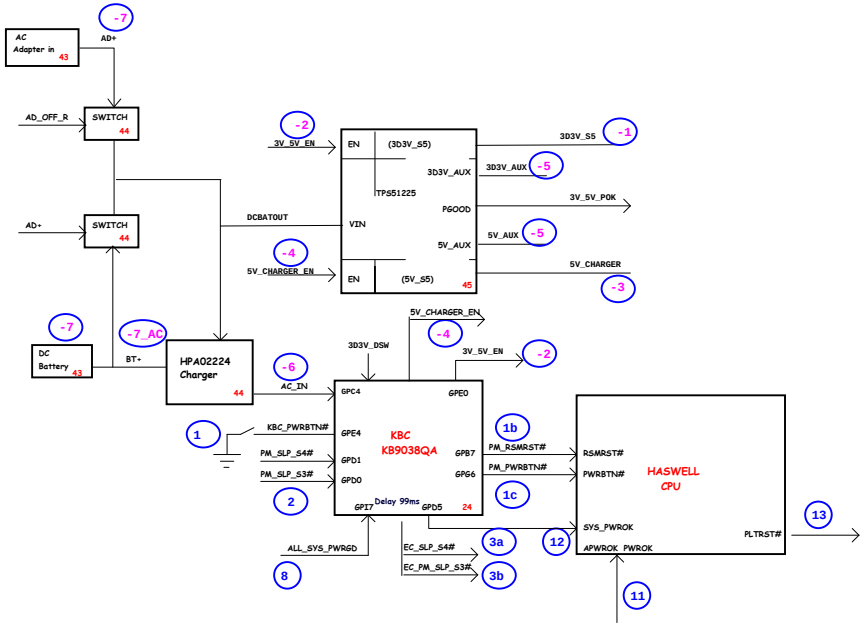
Intel-Power Up Sequence

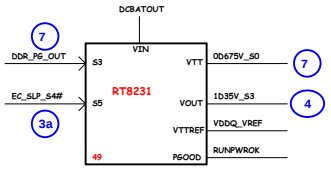


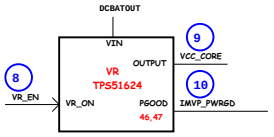


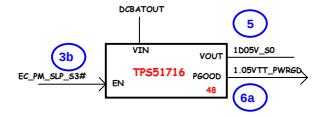


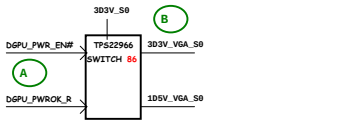
HASWELL POWER UP SEQUENCE DIAGRAM

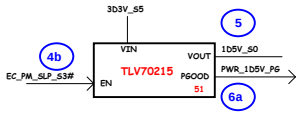


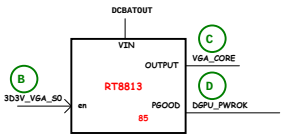


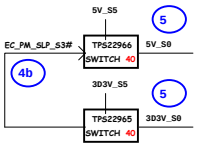


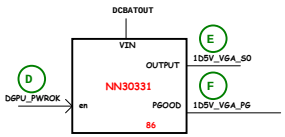












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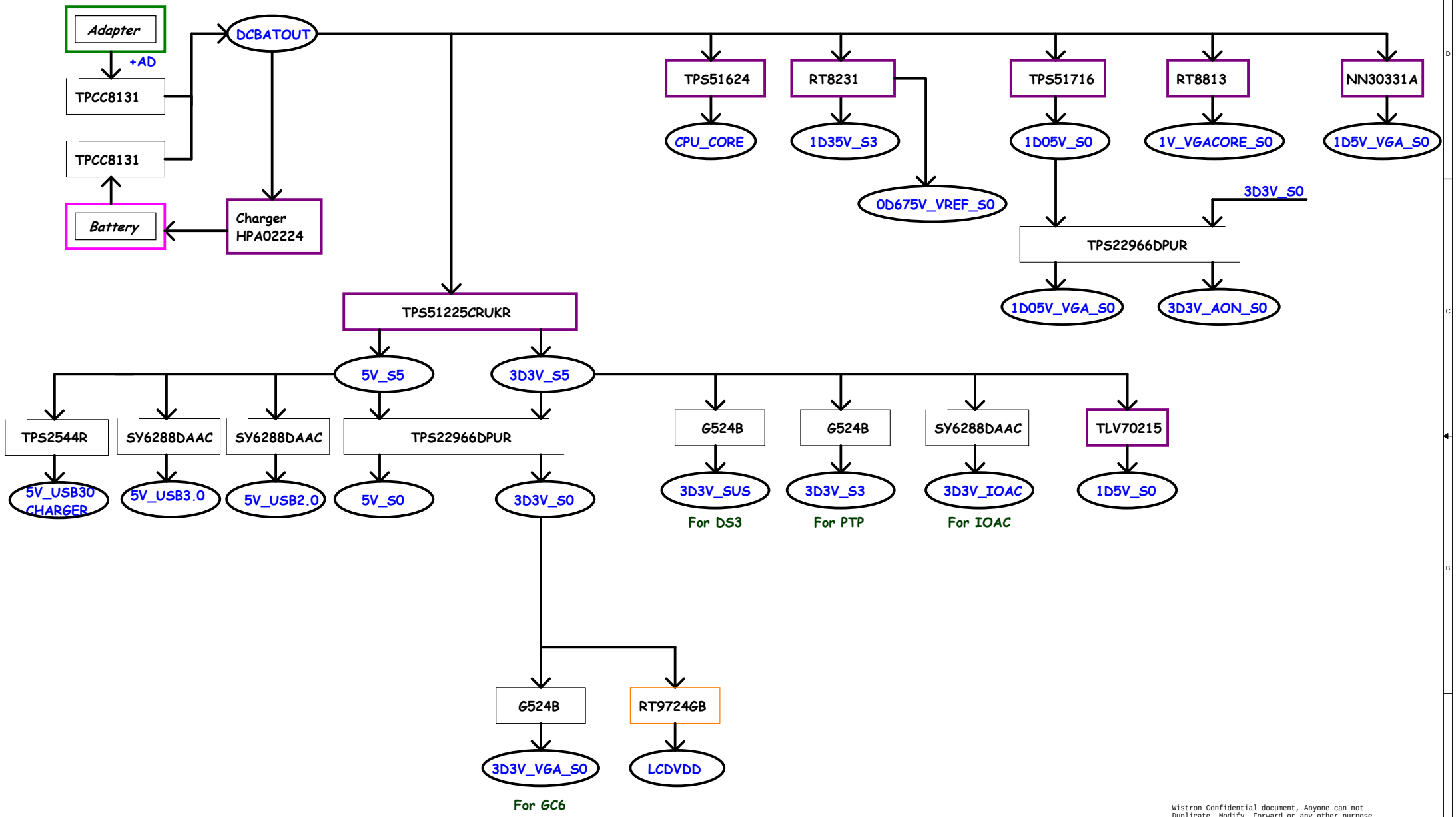

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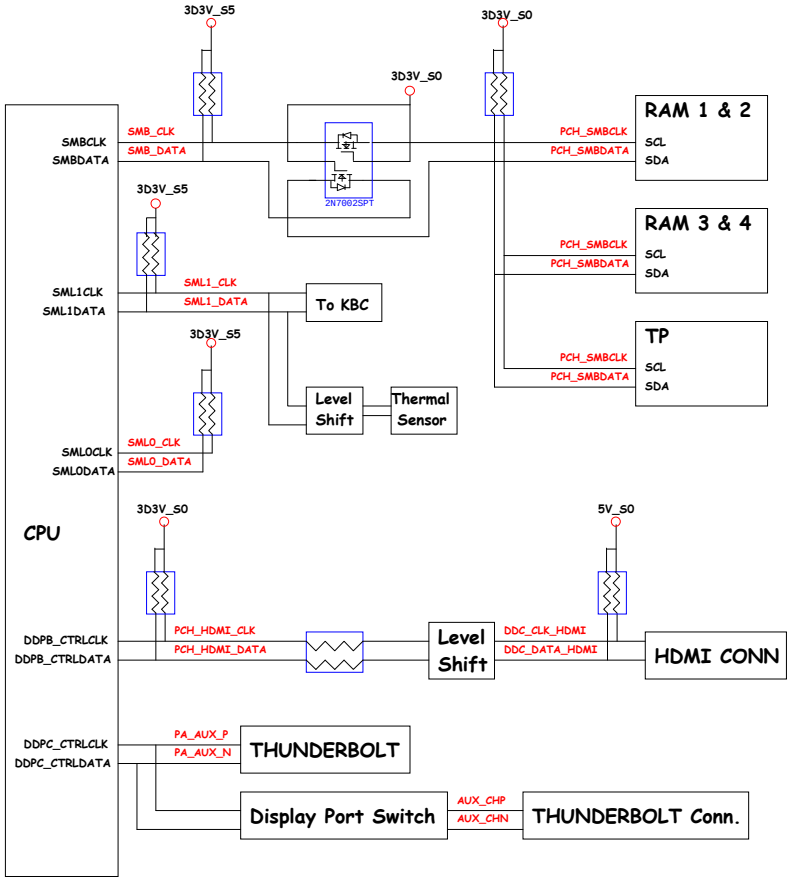
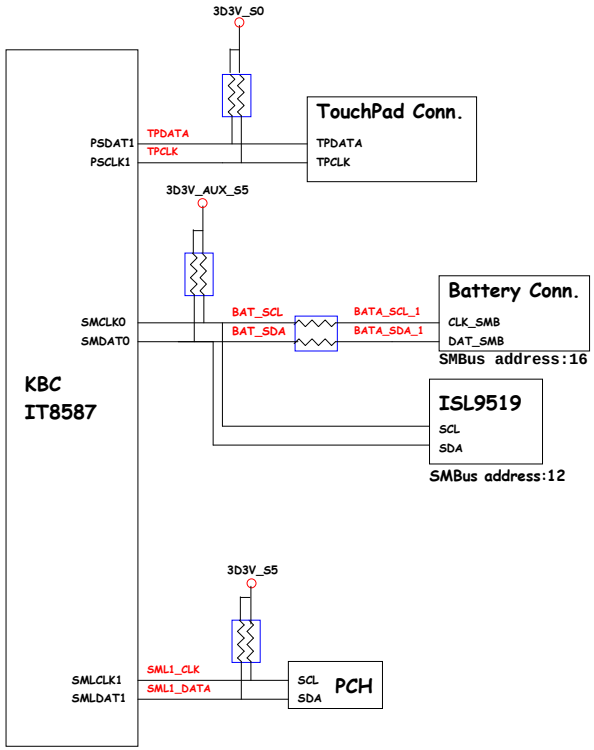
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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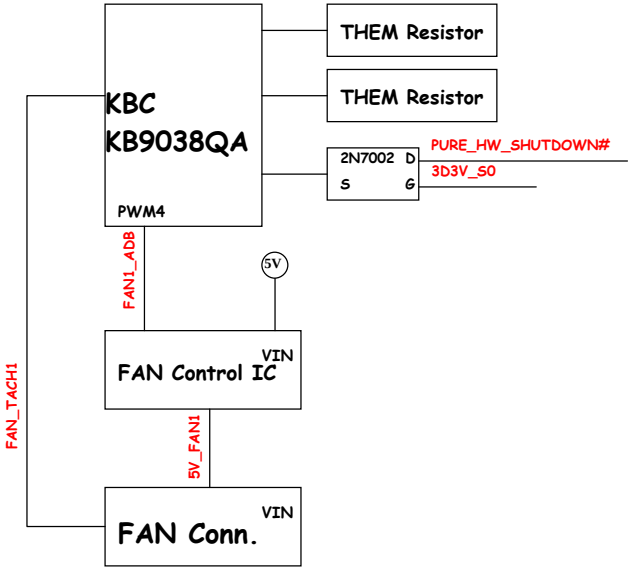
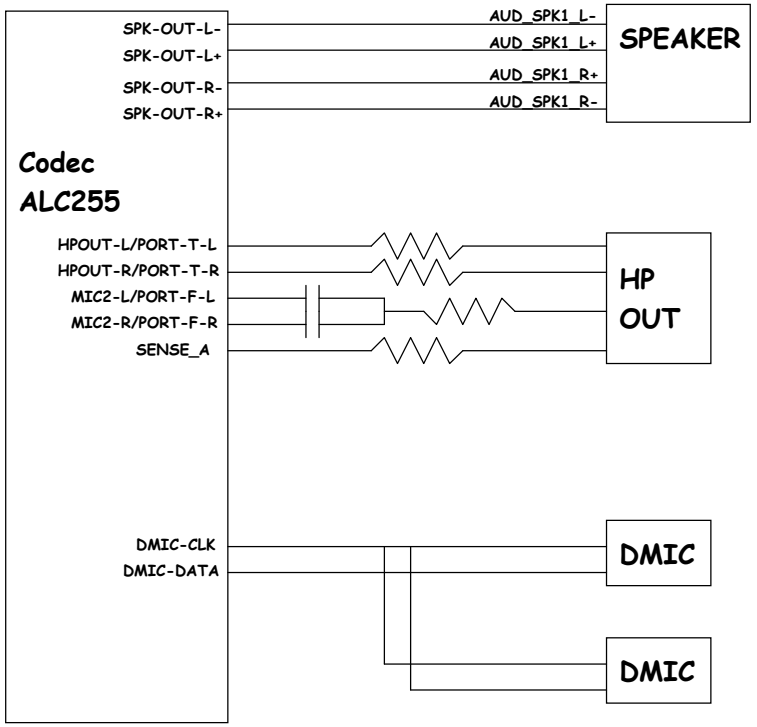
Thermal Block Diagram



Audio Block Diagram



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