

Compal Confidential

FH50P MB Schematics Document

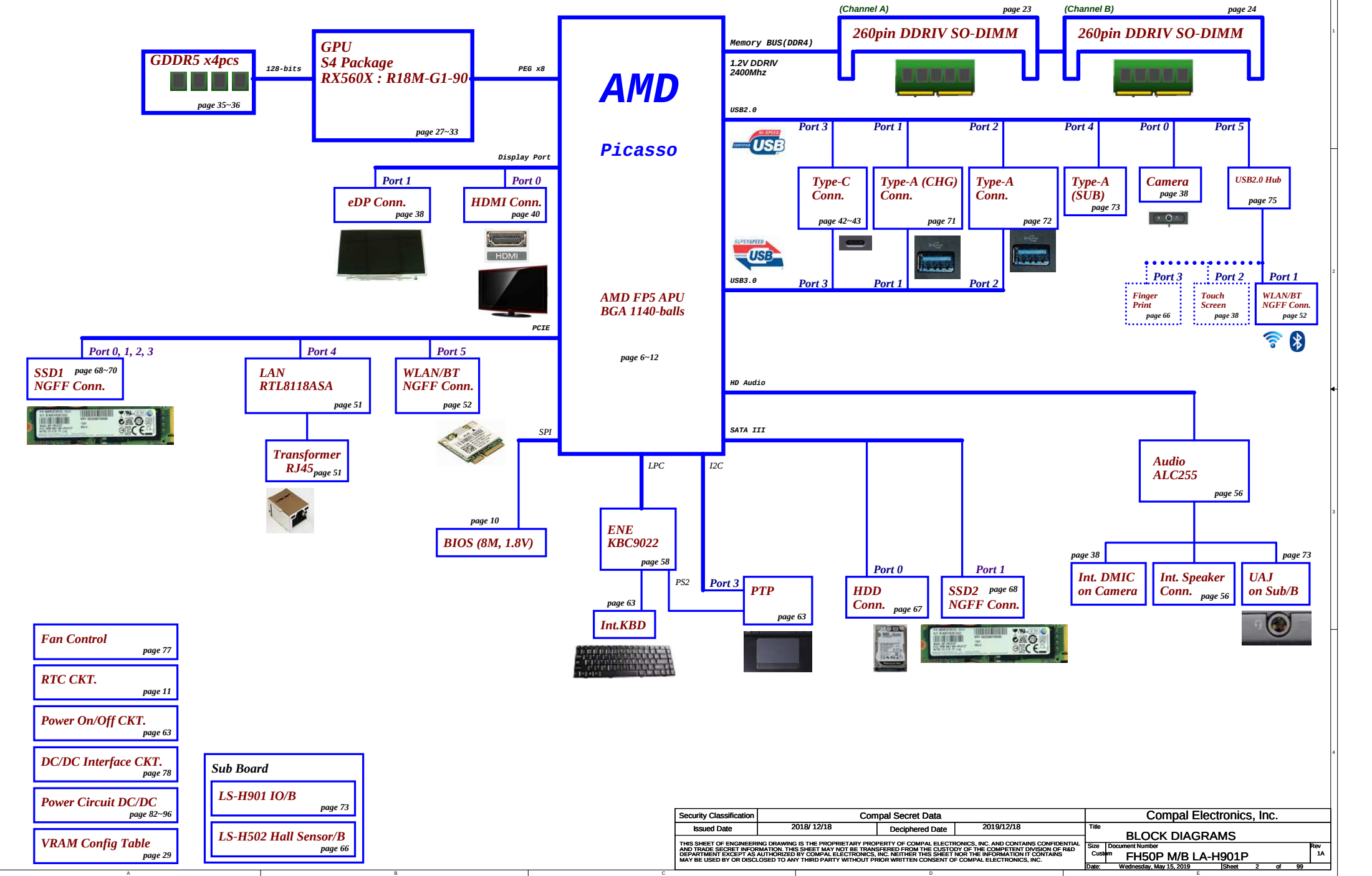
AMD Picasso Platform

AMD R18M-G1-90

LA-H901P REV:1A

2019-05-13

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Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)				
I2C Port 2 (+3VS)				
SBMUS Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TSI)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h
	Thermal Sensor (Remote1 GPU) (Remote2 APU)		1001 1010b 9Ah	1001 1011b 9Bh
SMBus Port 3 (+3VALW)	LED driver		1100 0000b C0h	1100 0001b C1h

Board ID	PCB Revision
0	EVT
1	PVT
2	MP
9	With RGB BL

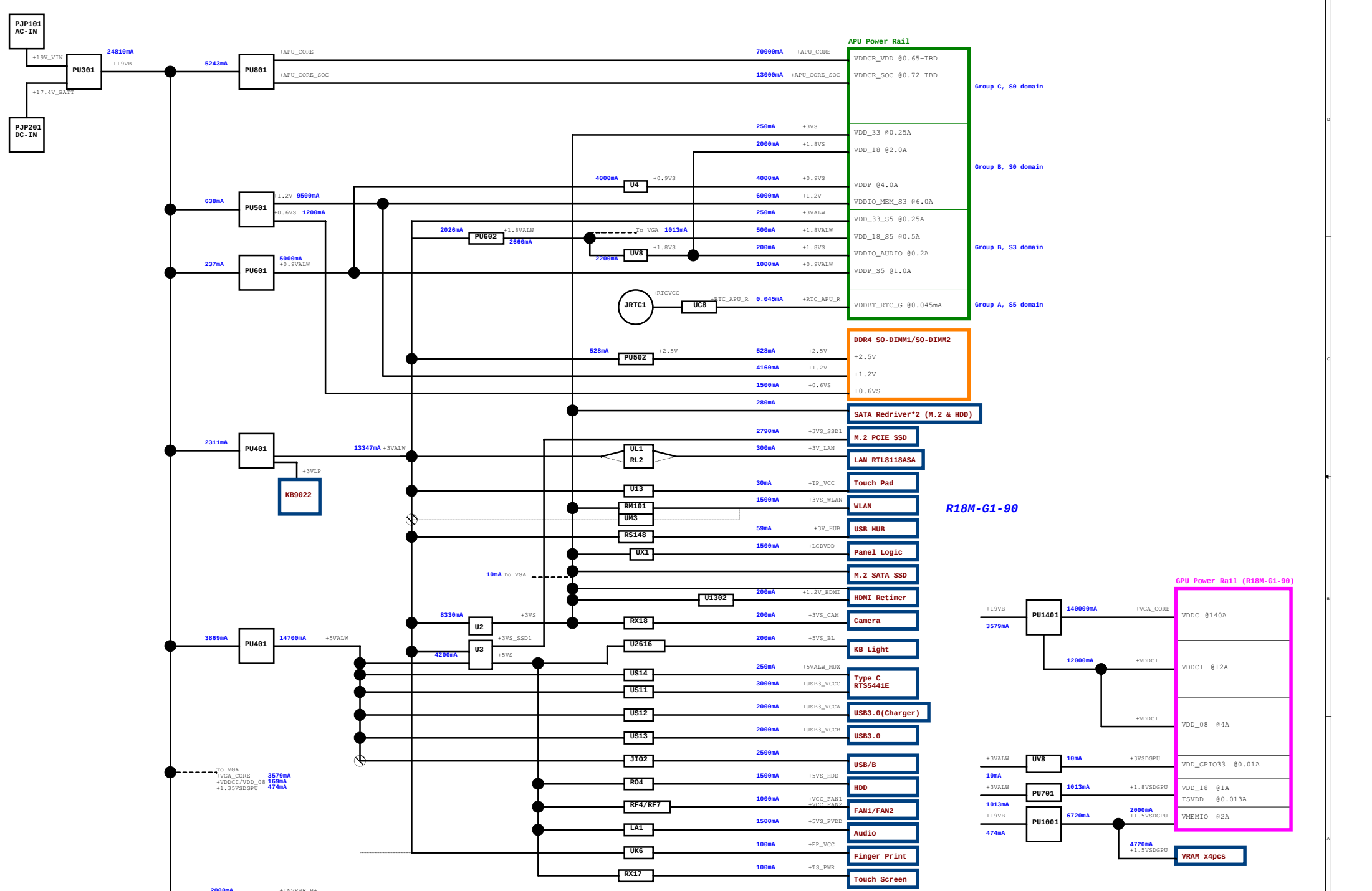
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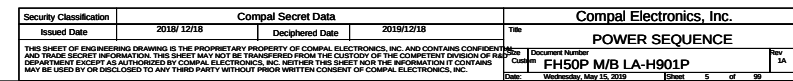
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

Group	Signal	Value	Initial State	Transition	Final State
G-A	+RTCBATT		Low	High	High
	EC_ON		Low	High	High
	+5VALW		Low	High	High
G-B	3V_EN		Low	High	High
	+3VALW		Low	High	High
	0_9_1_8VALW_PWREN		Low	High	High
	+1.8VALW/+0.9VALW		Low	High	High
G-C	SYSON		Low	High	High
	+1.2V/+2.5V		Low	High	High
	SUSP#		Low	High	High
	+5VS/+3VS/+1.8VS/+0.6VS		Low	High	High
	0_9VS_PWR_EN#		Low	High	High
	+0.9VS		Low	High	High
G-D	VR_ON		Low	High	High
	+APU_CORE		Low	High	High
	+APU_CORE_SOC		Low	High	High

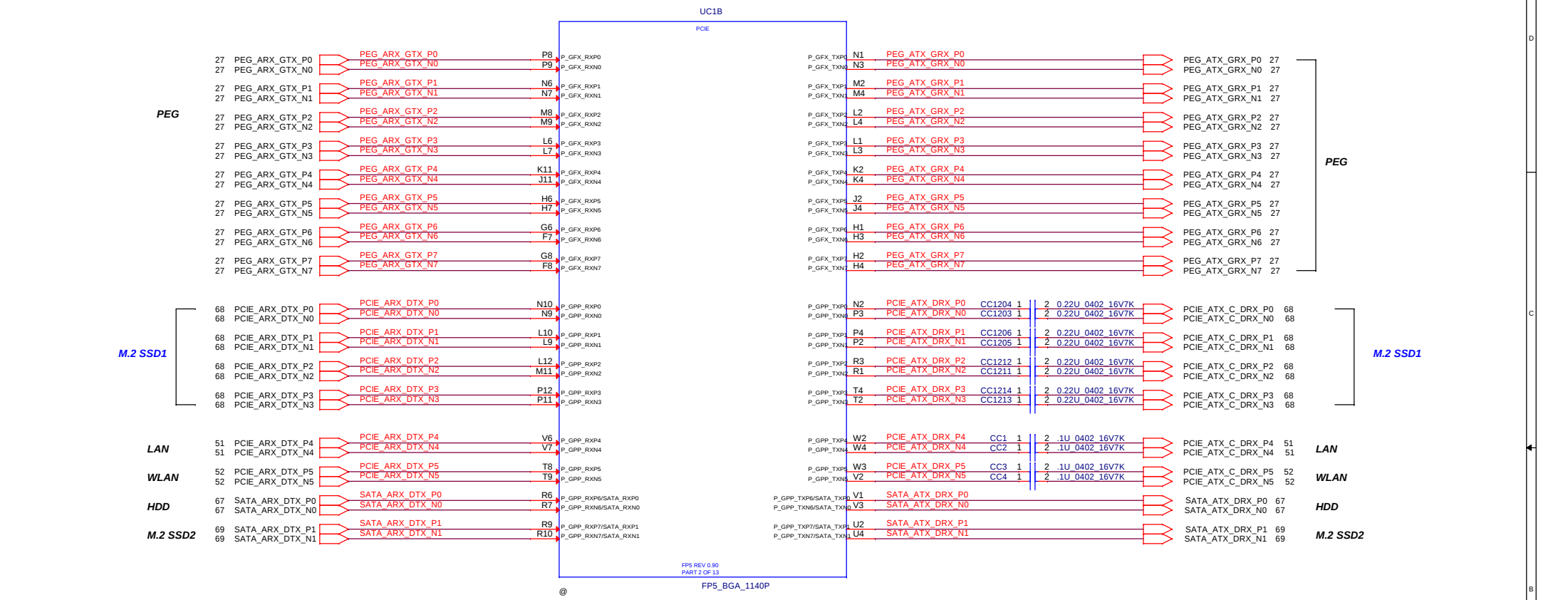
Signal	Timing Diagram
PE_GPT01/VGA_ON +3VSDGPU +1.8VSDGPU	
VGA_ON_B +VDDCI +VGA_CORE	
DGPU_PWRGOOD +1.5VSDGPU	
PE_GPT00	

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Main Func = CPU



APU PN Table

APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN	Compal PN
Picasso	UC1 R5APUQC@	UC1 R7APUQC@	UC1 R5APU@	UC1 R7APU@		
	S IC RYZEN5 YM3500C4T4MFG 2.1G BGA APU SA0000CCR20	S IC RYZEN7 YM3700C4T4MFG 2.3G BGA APU SA0000C7640	S IC RYZEN5 YM3500C4T4MFG 2.1G APU ABO! SA0000CCR60	S IC RYZEN7 YM3700C4T4MFG 2.3G APU ABO! SA0000C7680		

PCB Number

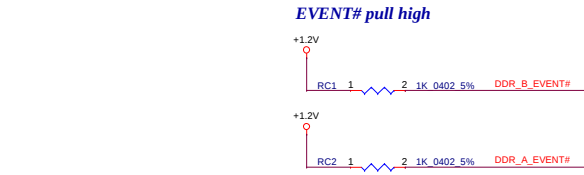
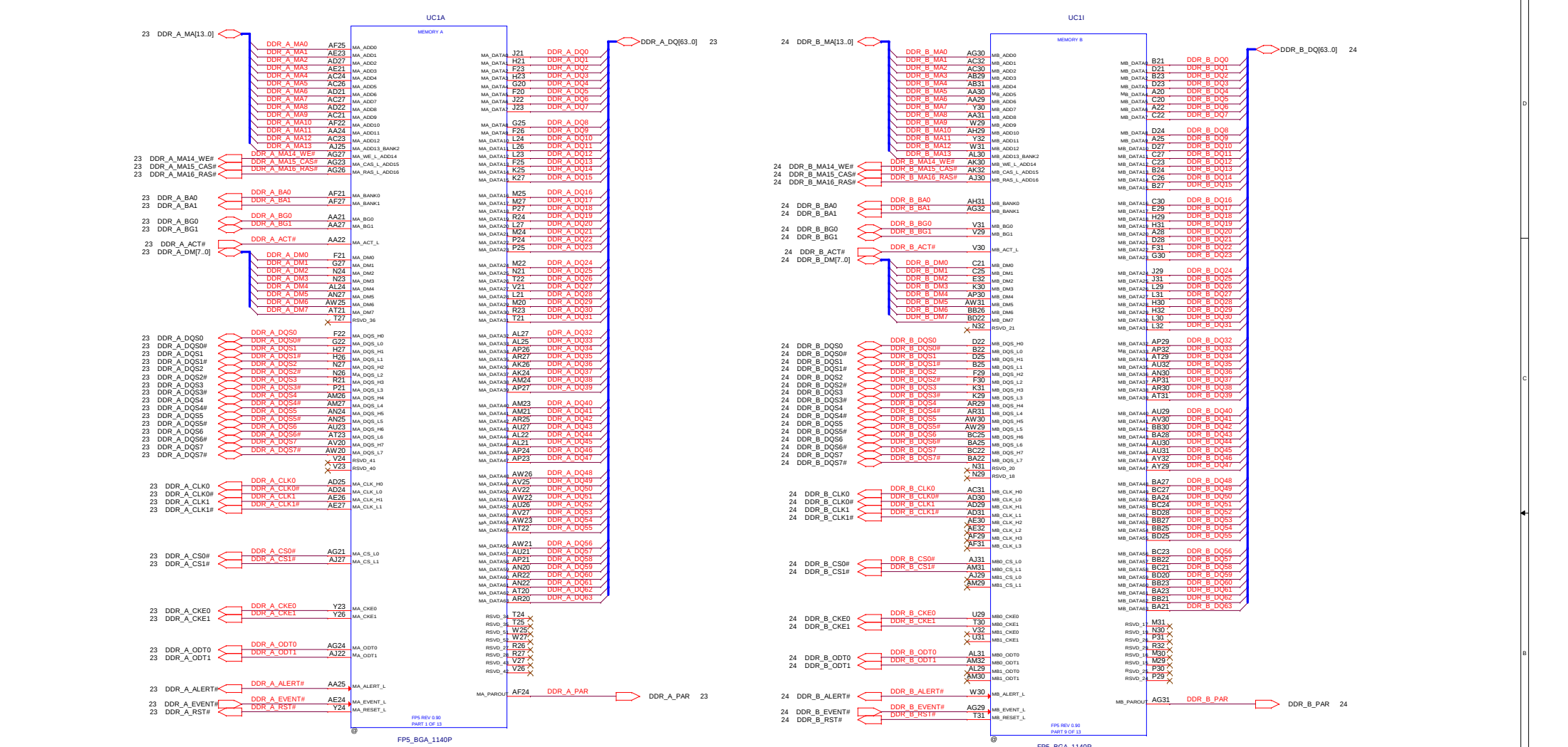
ZZZ EVT@
PCB 2QE LA-H901P REV0 M8 2
DA8001JM000

ZZZ PVT@
PCB FH50P LA-H901P LS-H901P/H502P
DAZ2QE00100
PCB: DAZ2QE00100, DA8001JM010 REV: 1.0/1.0/1.0

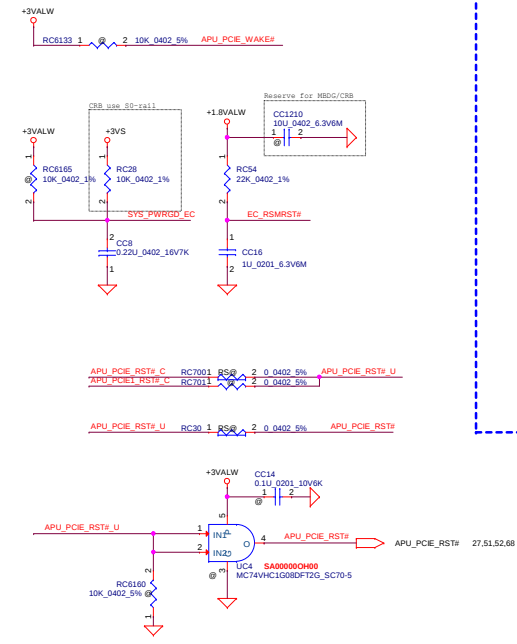
ZZZ MP@
PCB FH50P LA-H901P LS-H901P/H502P
DAZ2QE00101
PCB: DAZ2QE00101, DA8001JM01A REV: 1.A/1.0/1.0

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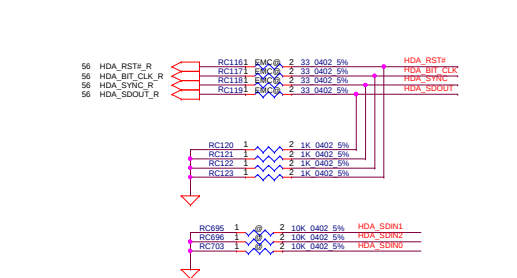
Main Func = CPU



ACPI

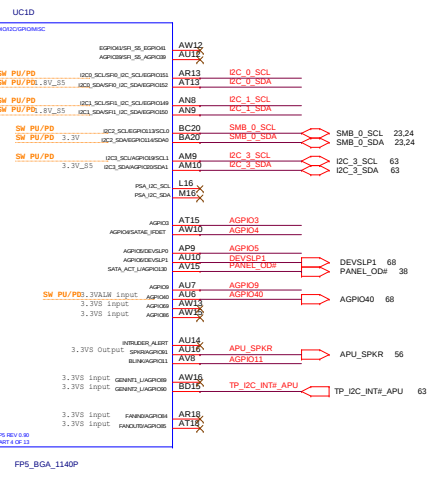
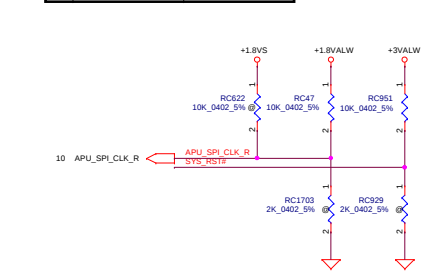


HDA



Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 48MHZ CRYSTAL CLOCK (Default)	NORMAL RESET MODE (Default)
L	USE 160MHZ PCIE CLOCK AS REFERENCE CLOCK	SHORT RESET MODE

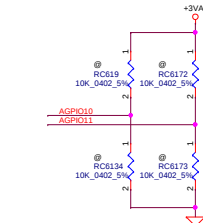
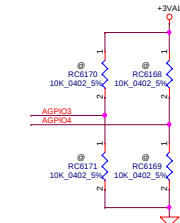
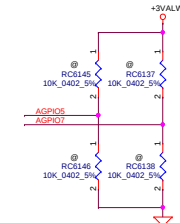


GPIO Table

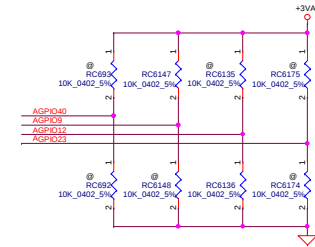
AGPIO5	AGPIO7

AGPIO3	AGPIO4

AGPIO10	AGPIO11

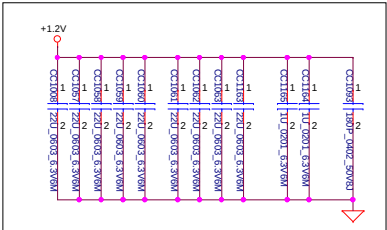


	AGPIO40	AGPIO9	AGPIO12	AGPIO23
H	RSV	DIS Type1	RSV	RSV
L	RSV	RSV	DMIC x2	RSV

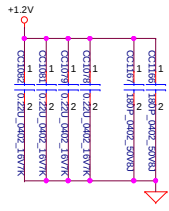


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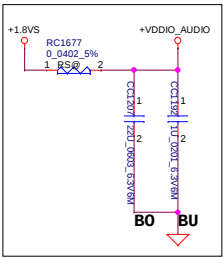
```
+APU_CORE_SOC Cap
place at Power Side
```



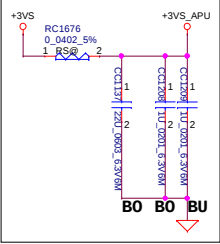
All BU (on bottom side under SOC)



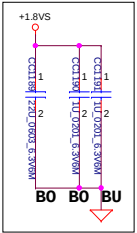
ACROSS VDDIO AND VSS SPLIT



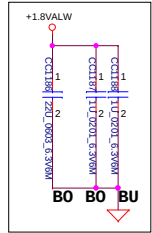
SCL/MB
1 *22
1*1uF



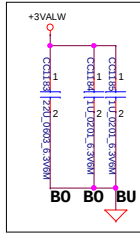
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



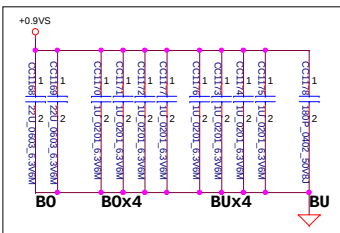
+1.3



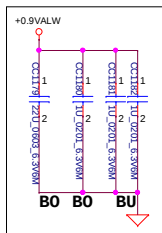
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



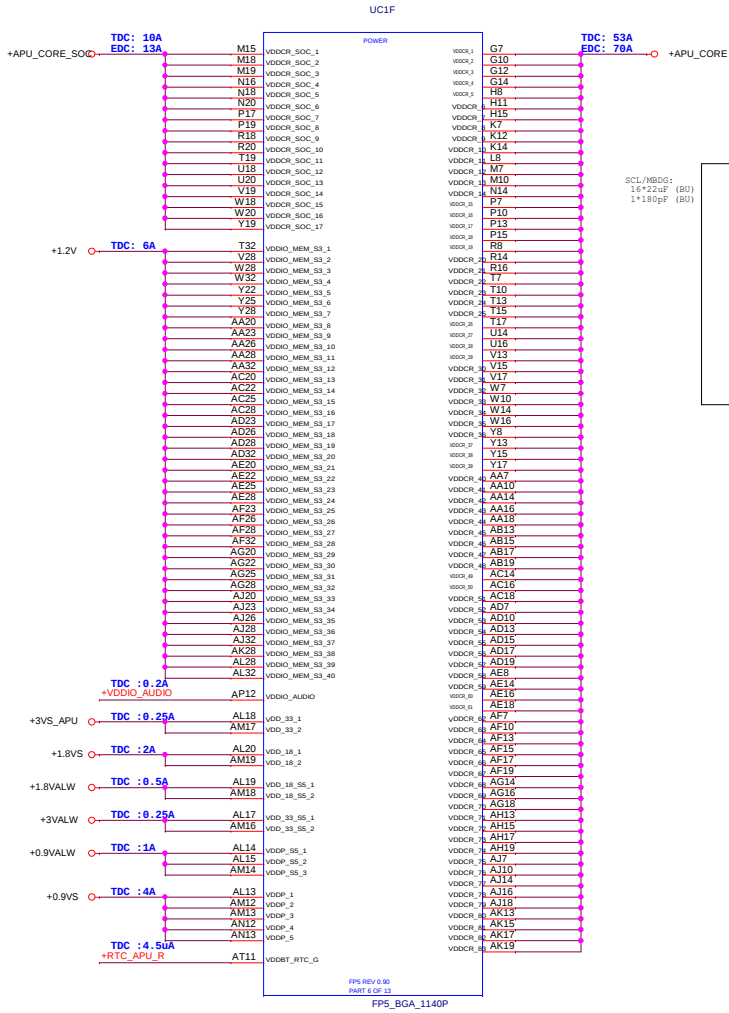
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



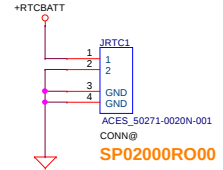
SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)



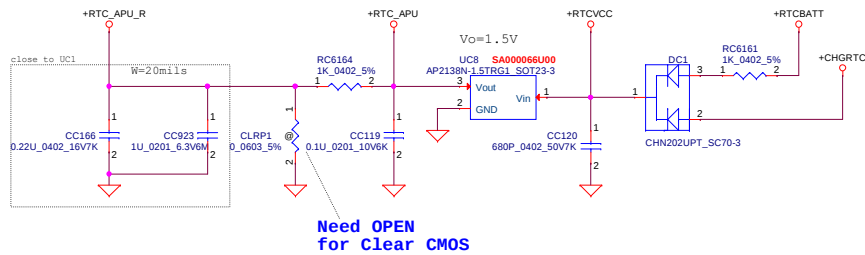
SCL/MBDG:
1 *22uF (B0)
3*1uF (B0x1+BUx2)



```
+APU_CORE Cap place at Power Side
```



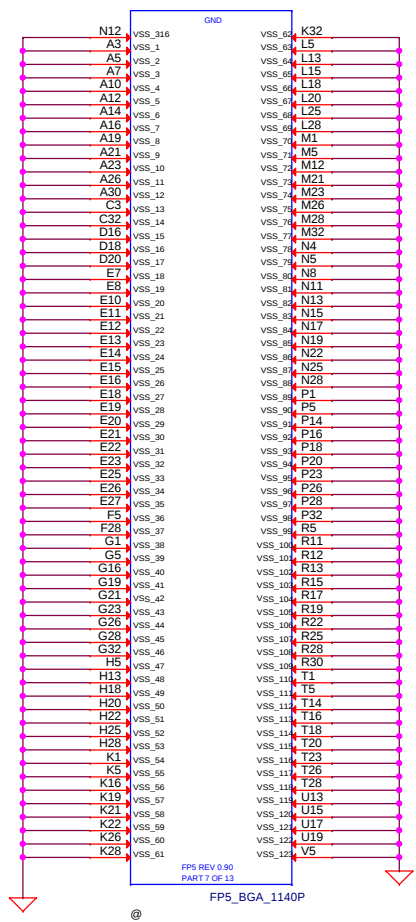
RTC OF APU



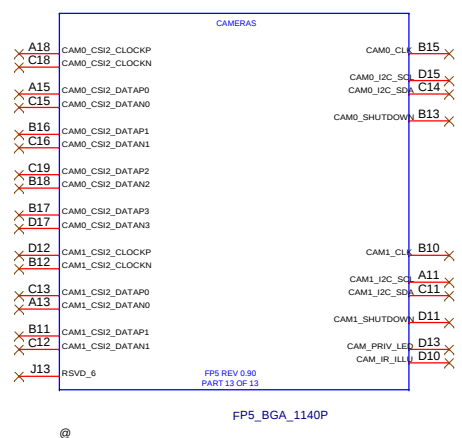
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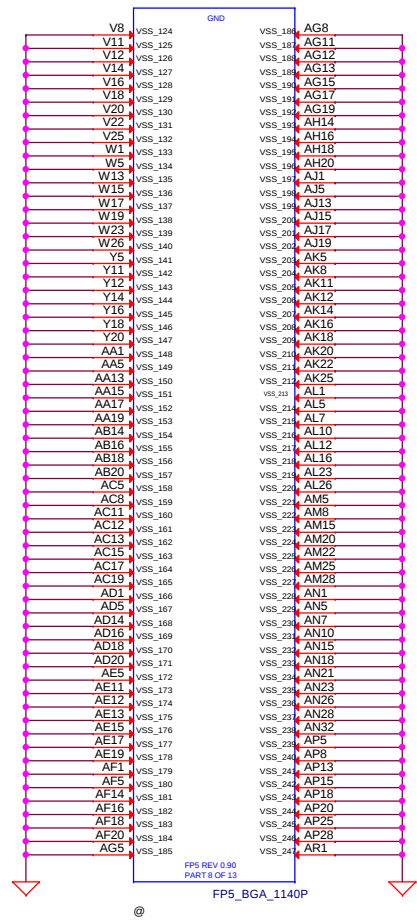
UC1G



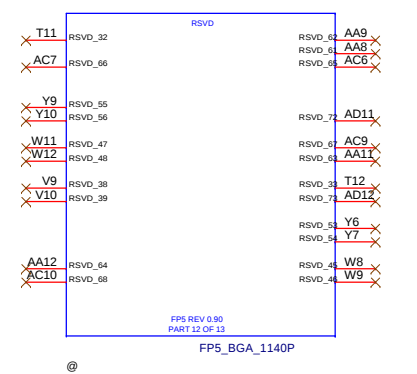
UC1M



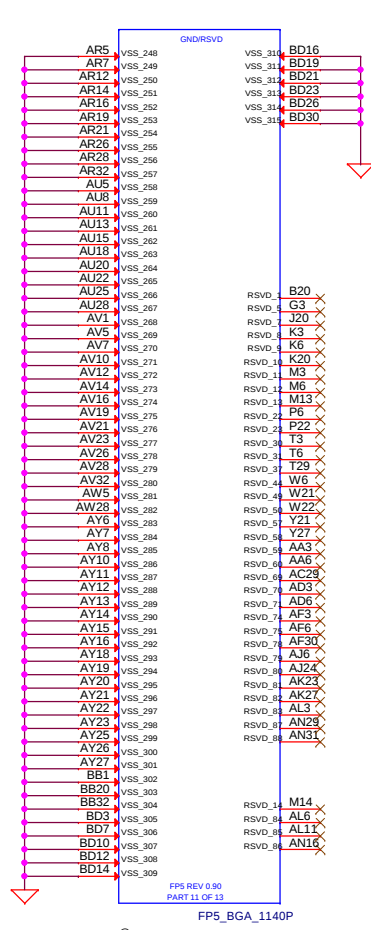
UC1H



UC1L



UC1K



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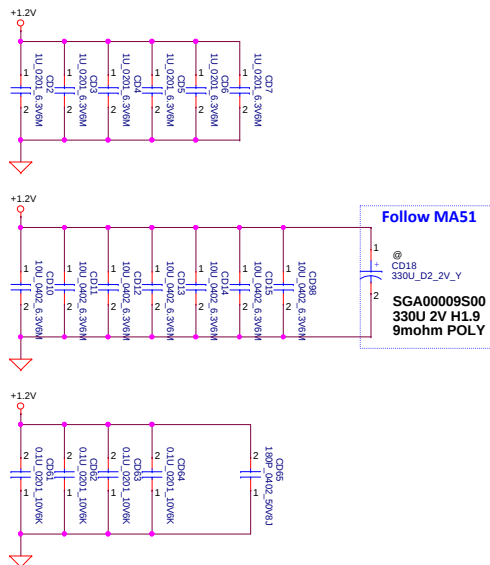
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2-3A to 1 DIMMs/channel

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

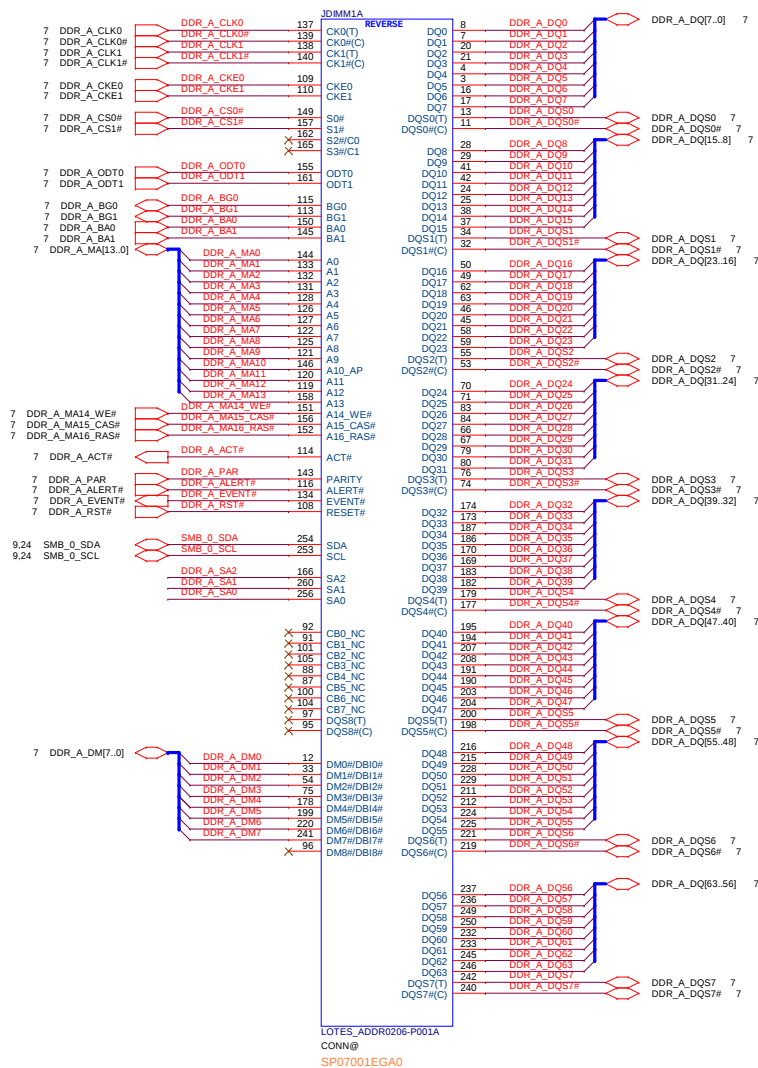
DDR4 support Even Parity check in DRAMs.

CRB use 0.1uF x12 (6 pop, 6 unpop), 180pF x1, 100uF x2



CD26
1u0201_6.3V6M

+3VS



Follow CRB design

15mil

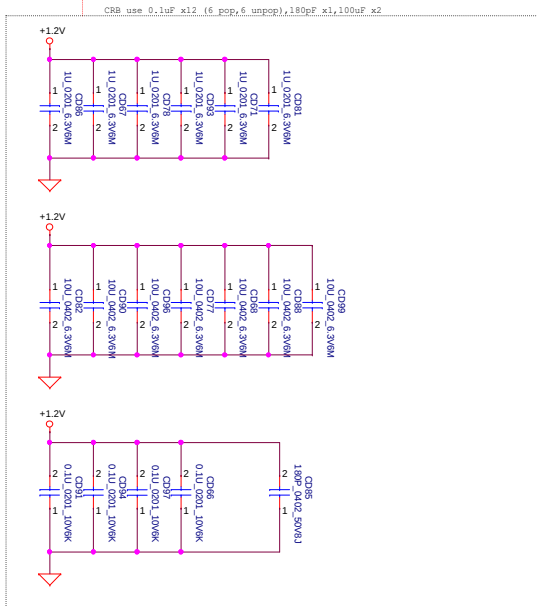
Place near to SO-DIMM connector.

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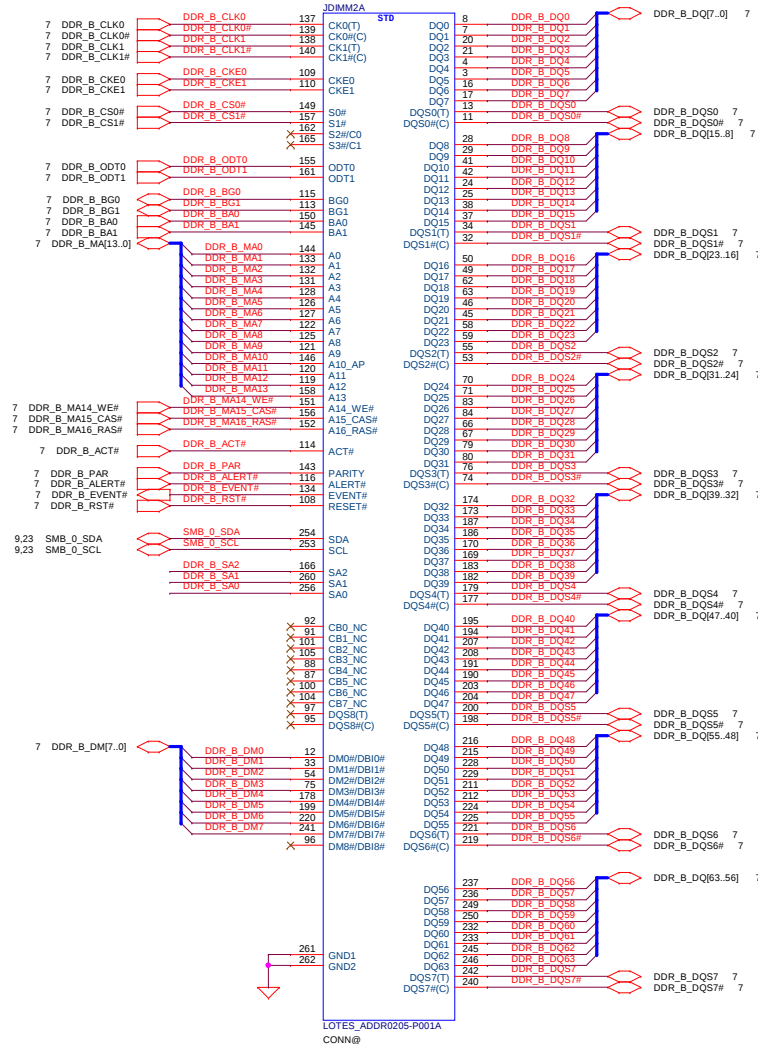
2-3A to 1 DIMMs/channel

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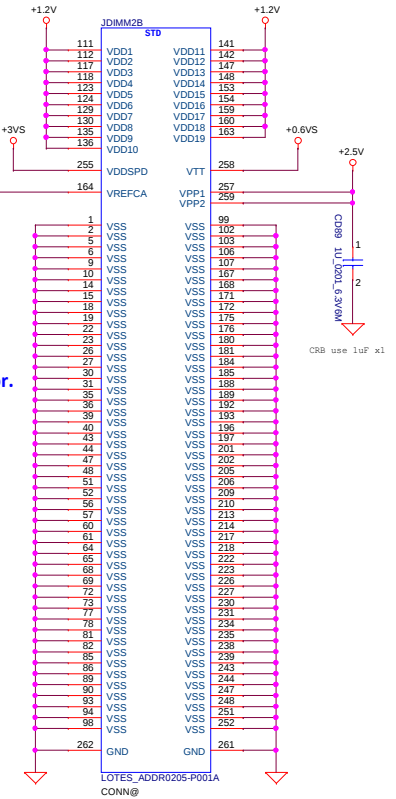
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



A circuit diagram showing a 1uF capacitor connected between a +3VS voltage source and ground. The capacitor is labeled '1u 0.01 6.3V/M' and 'CD95'. The ground symbol is a red triangle pointing downwards.



Place near to SO-DIMM connector.



CRB use 4.7uF x1, 0.1uF x1



The diagram shows a CRB circuit with four CD74 buffers. The inputs of the buffers are connected to a common rail, and the outputs are connected to a common rail. The circuit is powered by +0.6VS. It features four 1uF 0.001 6.3VW capacitors (CD72) and four 10k 0.02 6.3VW capacitors (CD70). The circuit is designed to buffer the common rail signal.

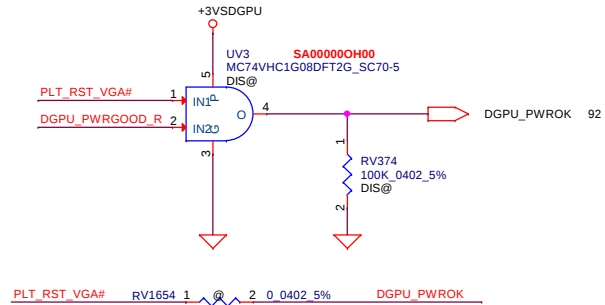
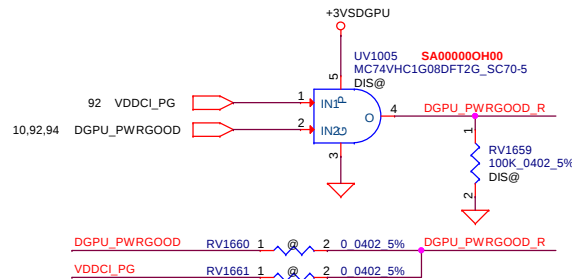
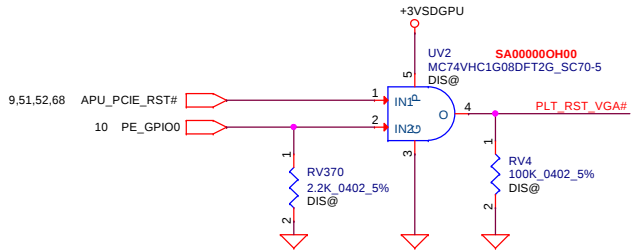
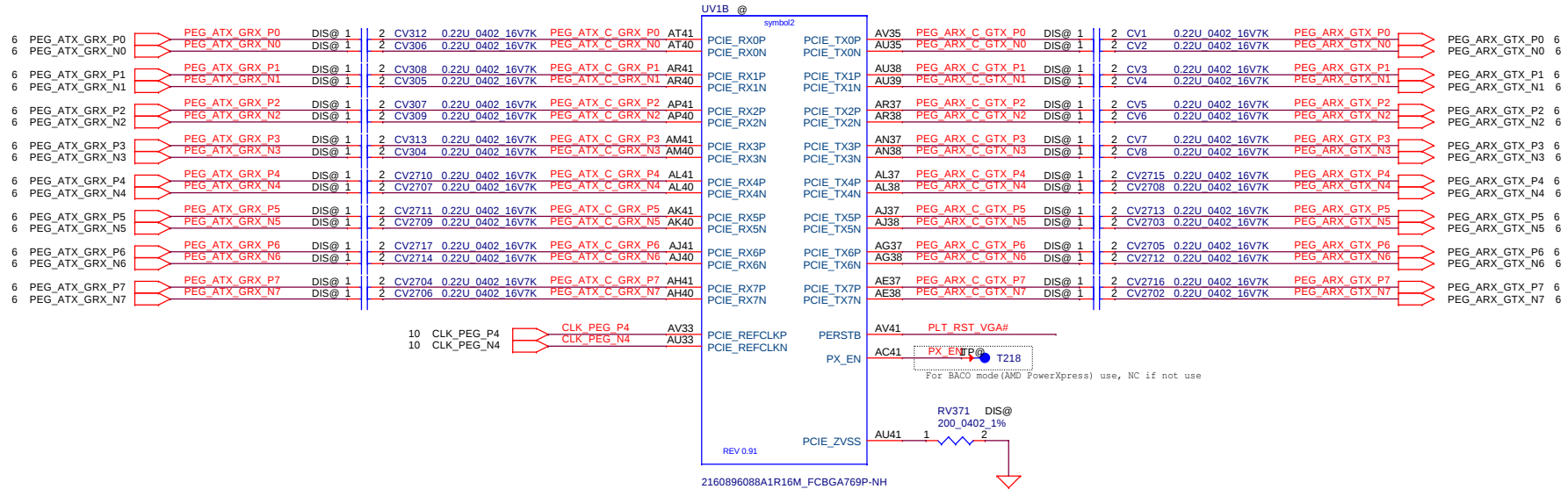
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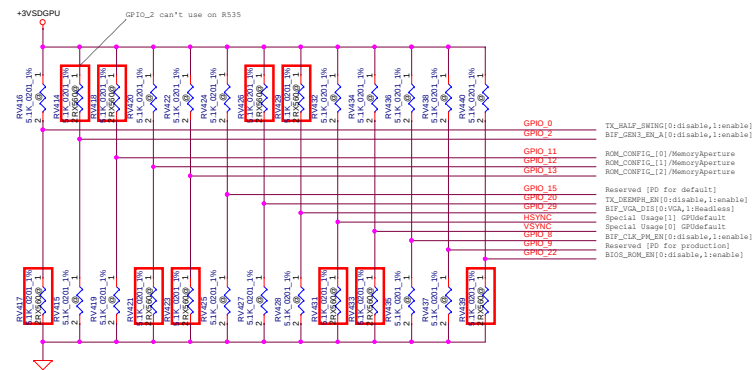
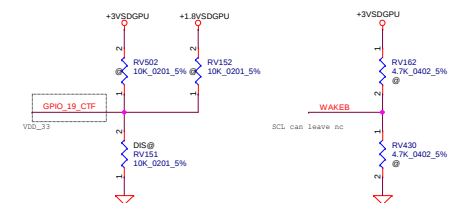
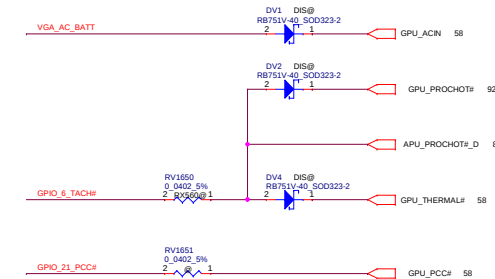
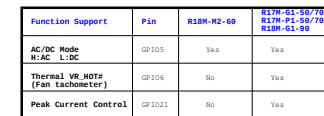
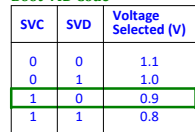
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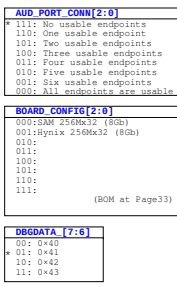
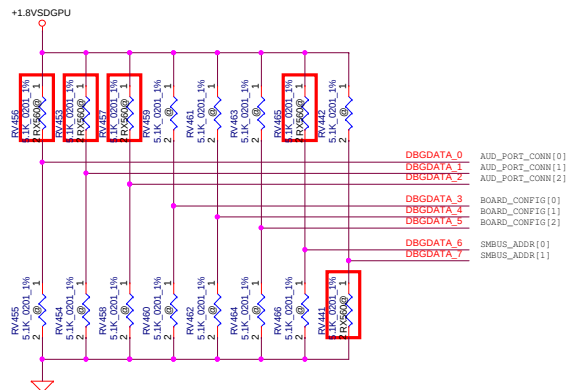
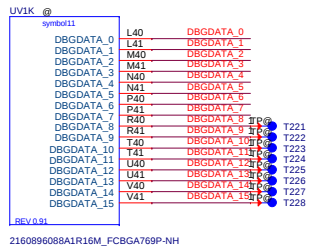
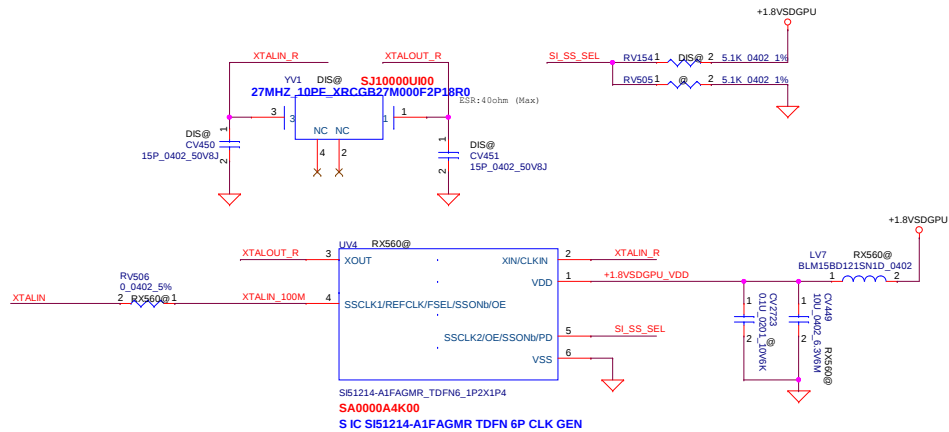
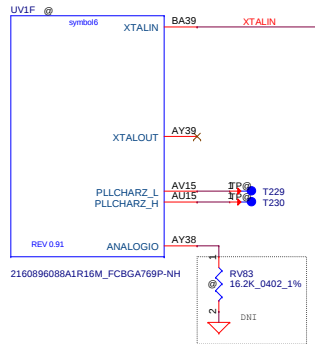
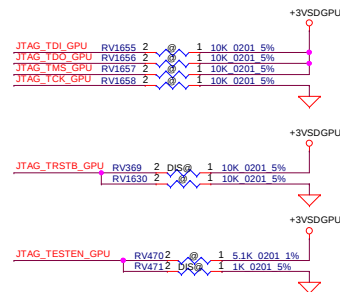
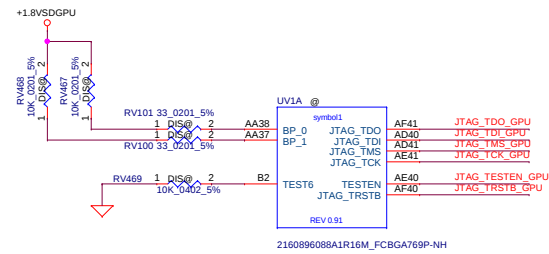


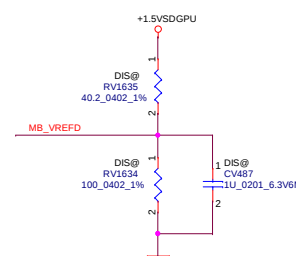
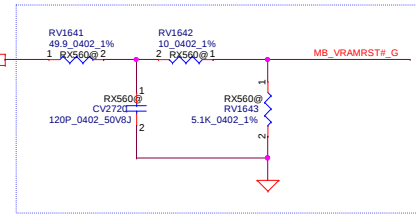
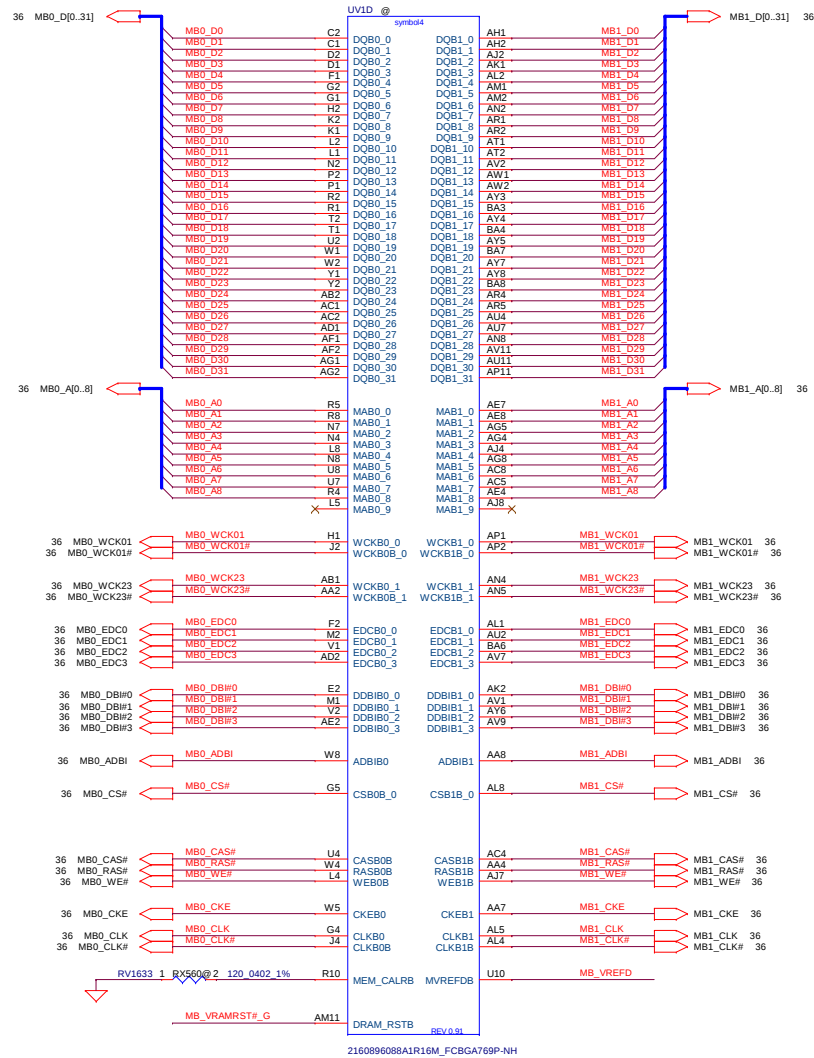
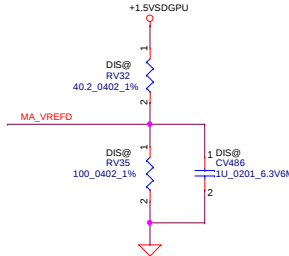
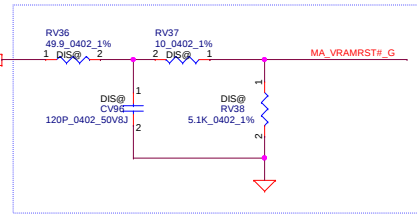
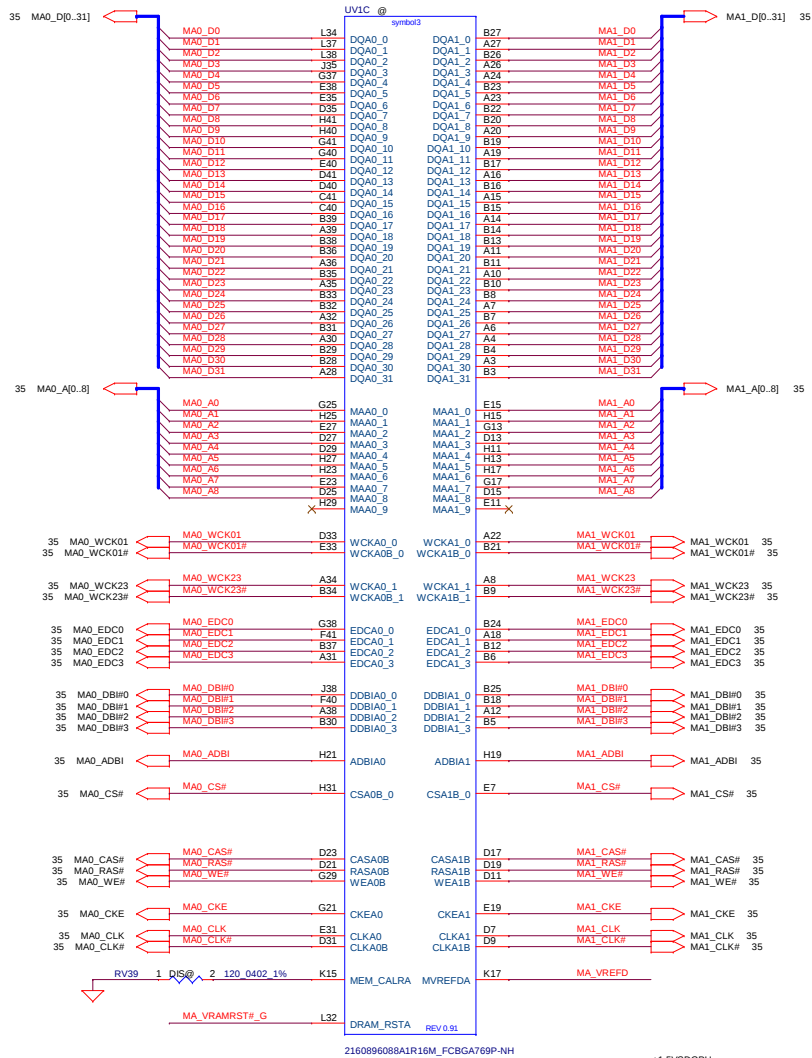
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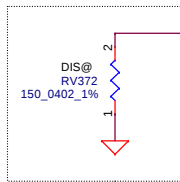
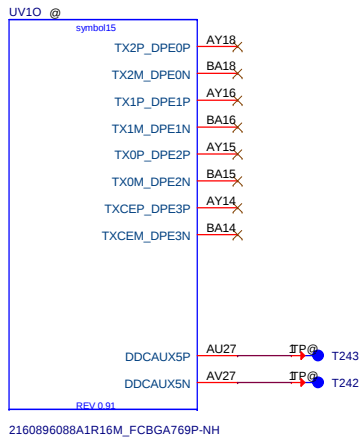
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

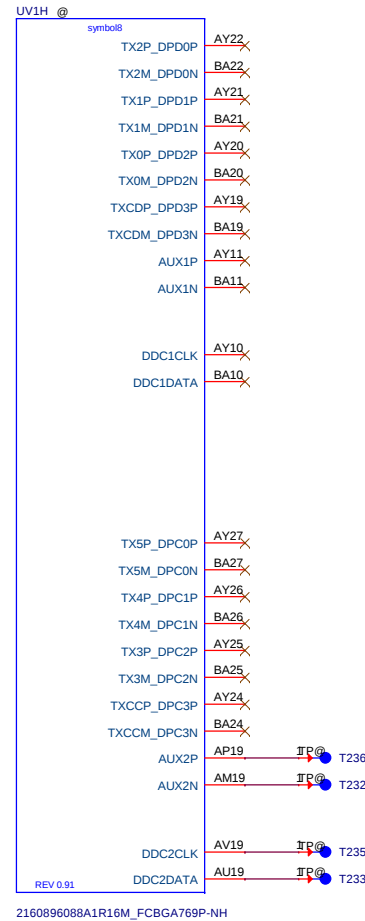
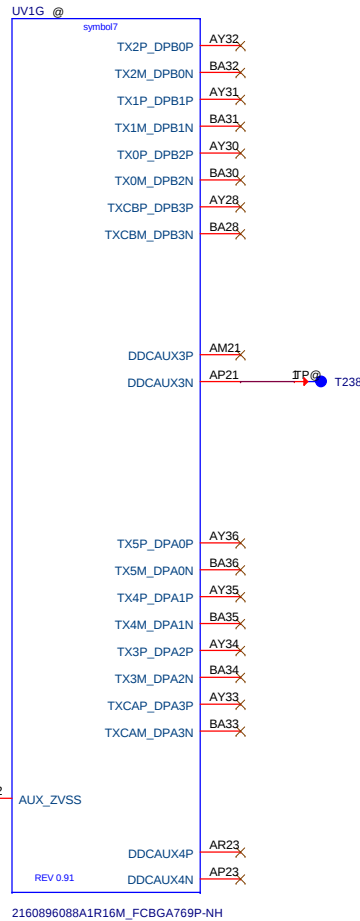




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Data Book: need config even if not use display function



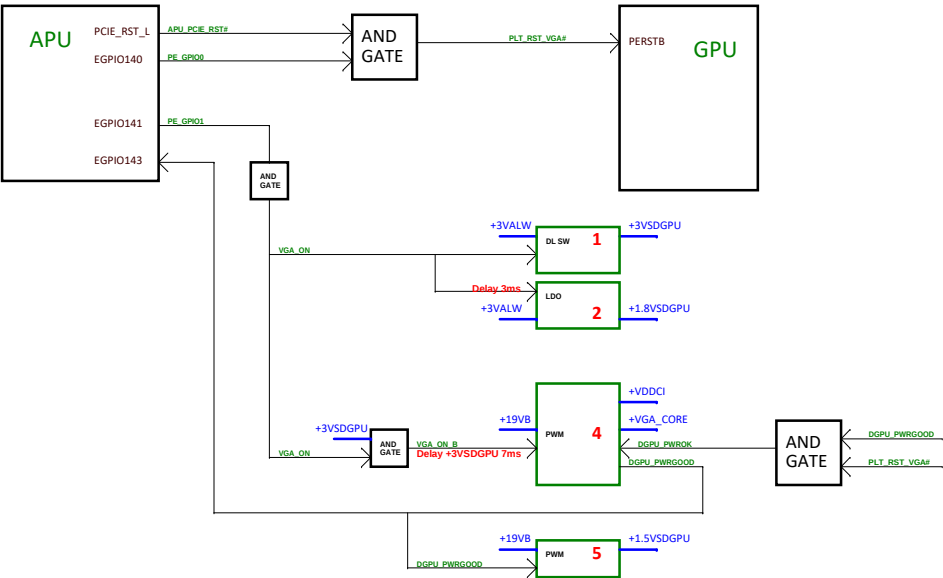
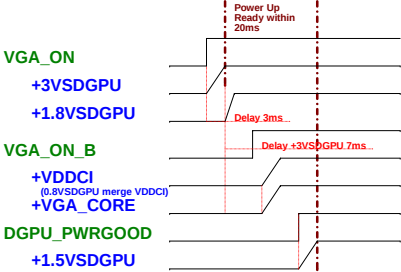
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5.3 Power-up/down Sequence

"R17M-G1-50 / R17M-G1-70 / R18M-G1-90" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

R18M-G1-90



For AMD R18M-G1-90 VRAM Device ID: 67EF/C0

Memory ID/Vendor/Size	Memory PN R3(ABOI)	BOARD_CONFIG[2:0]	DBGDATA_3 (H: RV463, L: RV464) DBGDATA_2 (H: RV464, L: RV462) DBGDATA_1 (H: RV459, L: RV460)
000 (8Gb) SAMSUNG 256M x32	UV1001 X78_S4G@ UV1002 X78_S4G@ UV1003 X78_S4G@ UV1004 X78_S4G@ S IC D5 256M32 K4G80325FB-HC25 FBGA ABOI SA00009TA10	RV464 X78_S4G@ RV462 X78_S4G@ RV460 X78_S4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900	
001 (8Gb) HYNIX 256M x32	UV1001 X78_H4G@ UV1002 X78_H4G@ UV1003 X78_H4G@ UV1004 X78_H4G@ S IC D5 256M32 H5GC8H24AJR-R2C BGA ABOI SA0000C1700	RV464 X78_H4G@ RV462 X78_H4G@ RV459 X78_H4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900	
010 SAMSUNG 128M x32			
011 HYNIX 128M x32			
100 MICRON 256M x32			

AMD GPU PN

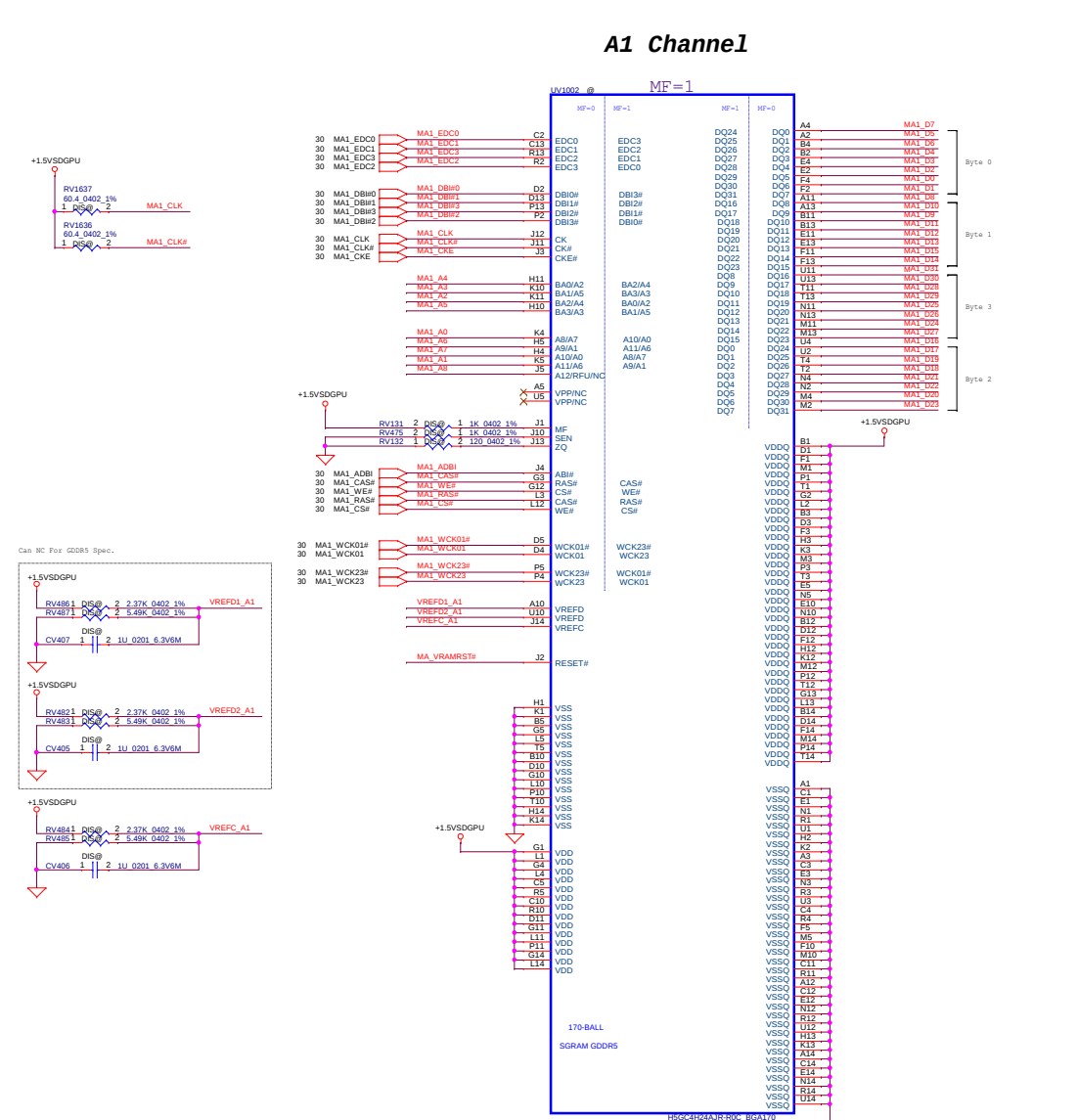
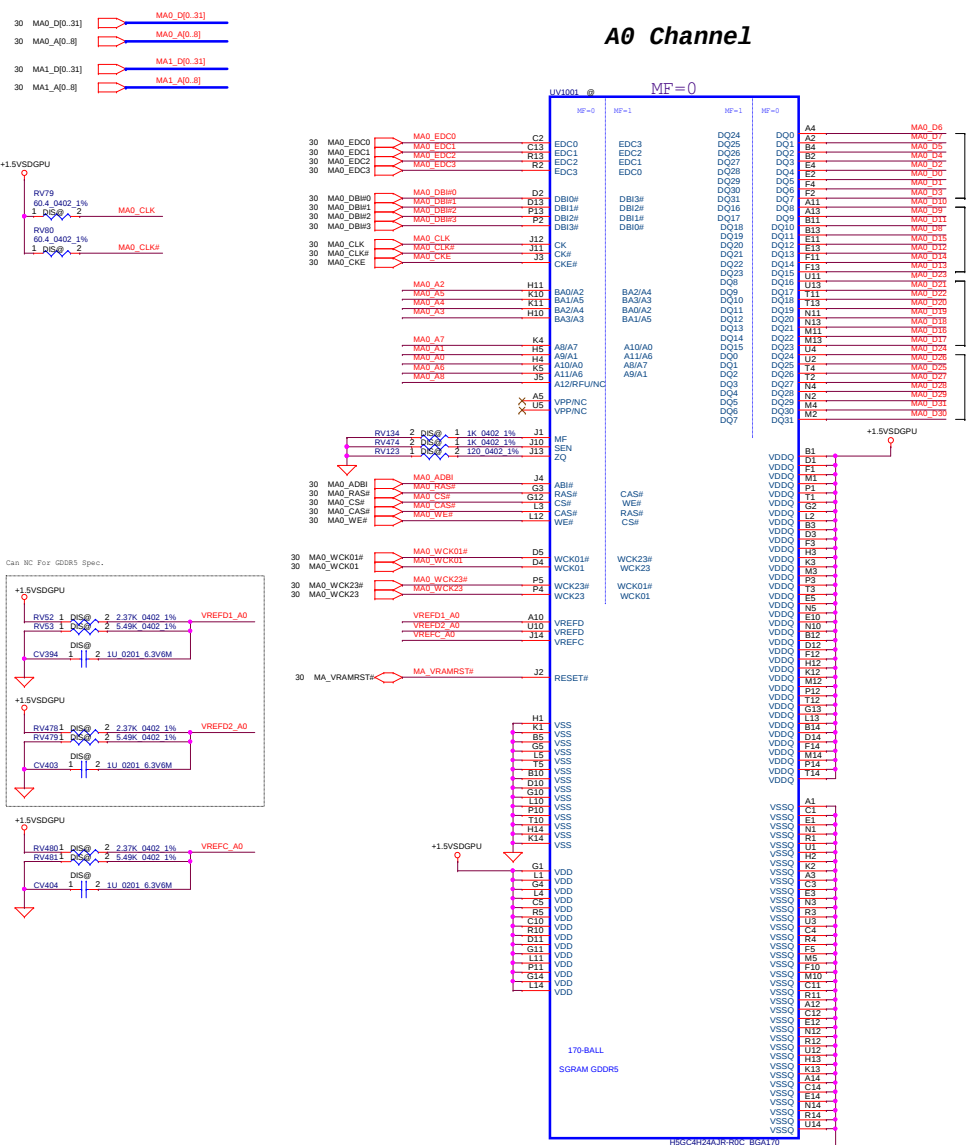
R18M-G1-90 PN R1(ROH)
UV1 RX560@
S IC 215-0908004 A1 R18M-G1-90 ABOI SA0000BFF10

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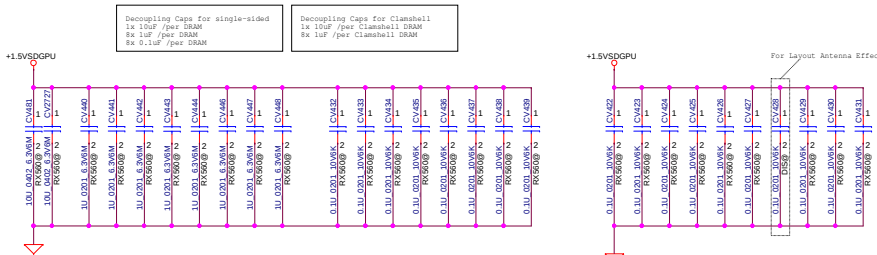
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A0 Channel1

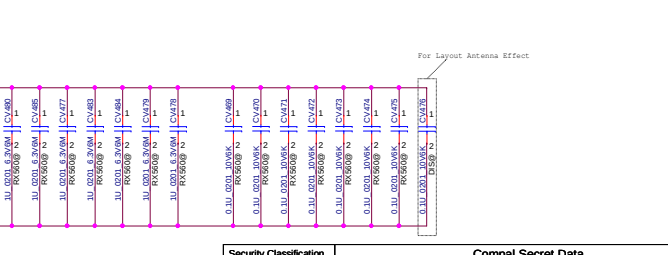
A1 Channel1



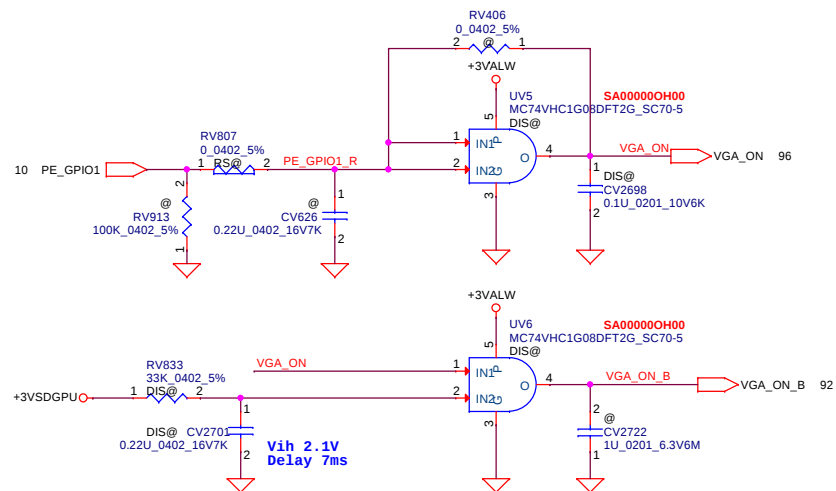
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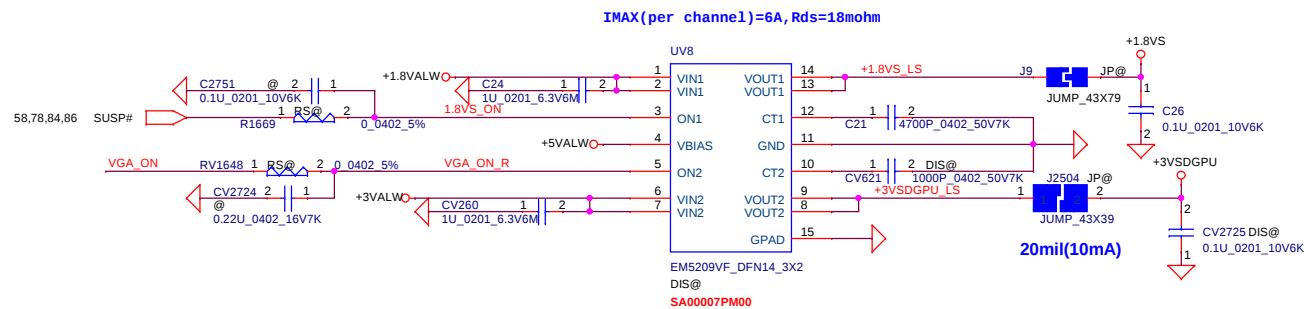
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				Revision	1A



+3VALW TO +3VSDGPU



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LCD POWER CIRCUIT

3V5S

100nF 6.3V5M C22

1 2

5 4

UX1

IN OUT

1 2

W=60mV

100nF 6.3V5M C21

1 2

ENVDD

8

ENVDD

10k R2

EN

OC

SOT23-5

SY6288C20AAC

SA000079400

Vih=1.5

100nF 6.3V5M C23

1 2

4.7U 0402 6.3V5M

1 2

0.1U 0201 10V5K C24

1 2

60mV

LCDVDD

LED PANEL Conn.

W=60mils

JEDP1

Pin Connections:

- 8 INVTPWM → INVTPWM
- 58 BKOFF# → BKOFF#
- 8 EDP_HPD → EDP_HPD
- +LCDVDD → +LCDVDD
- PANEL_OD#_R → PANEL_OD#_R
- EDP_AUXN_C → EDP_AUXN_C
- EDP_AUXP_C → EDP_AUXP_C
- EDP_TXP0_C → EDP_TXP0_C
- EDP_TXN0_C → EDP_TXN0_C
- EDP_TXP1_C → EDP_TXP1_C
- EDP_TXN1_C → EDP_TXN1_C
- EDP_TXP2_C → EDP_TXP2_C
- EDP_TXN2_C → EDP_TXN2_C
- EDP_TXP3_C → EDP_TXP3_C
- EDP_TXN3_C → EDP_TXN3_C
- +TS_PWR → +TS_PWR
- 58 TS_EN → TS_EN
- +3VS_CAM → +3VS_CAM
- 56 DMIC_CLK_R → DMIC_CLK_R
- 56 DMIC_DATA_R → DMIC_DATA_R

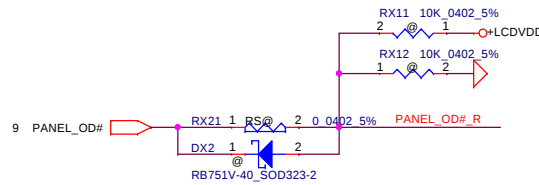
Ground Connections:

- 41 GND
- 42 GND
- 43 GND
- 44 GND
- 45 GND
- 46 GND

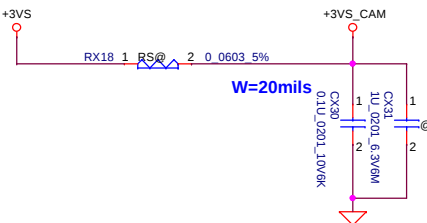
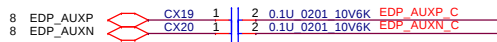
ACES_50203-04001-002

CONN@

SP010014B10



+5VS +3VS +TS_PWR
 RX16 1 @ 2 0 0603 5%
 RX17 1 @ 2 0 0603 5%



10 USB20_P0

10 USB20_N0

RX19 1 2 15 0402 1%

CX32 1 2 470P 0402 50V8J

RX20 1 2 15 0402 1%

CX33 1 2 470P 0402 50V8J

USB20_P0_RC

USB20_N0_RC

LX2

USB20_P0_L

USB20_N0_L

DLM0NSN900HY2D_4P

EMC@

SMO70005U00

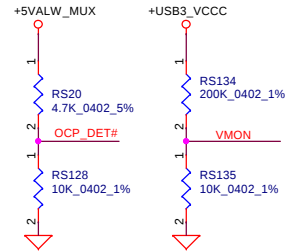
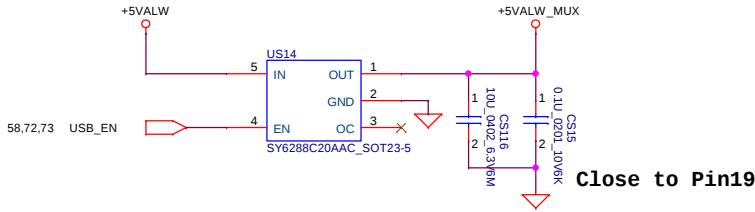
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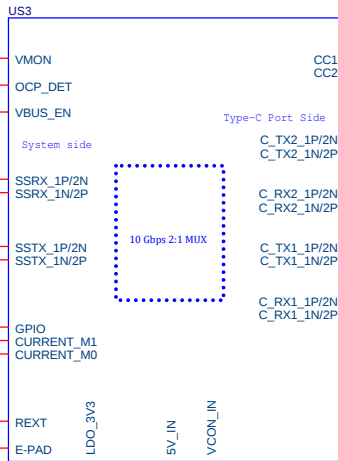
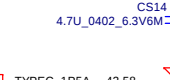
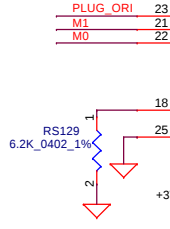
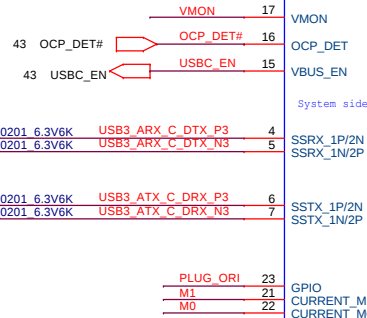
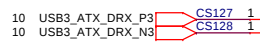
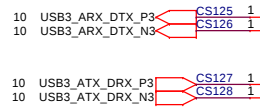
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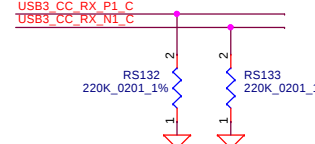
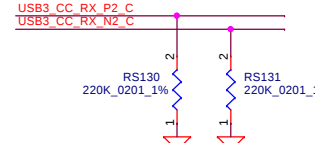
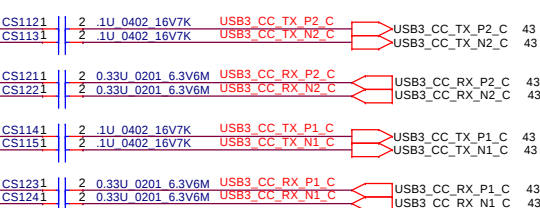


USB3.0 (Port 3)



10 Gbps 2:1 MUX

Close to Pin13

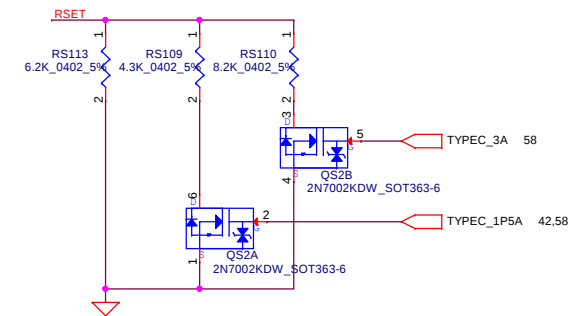
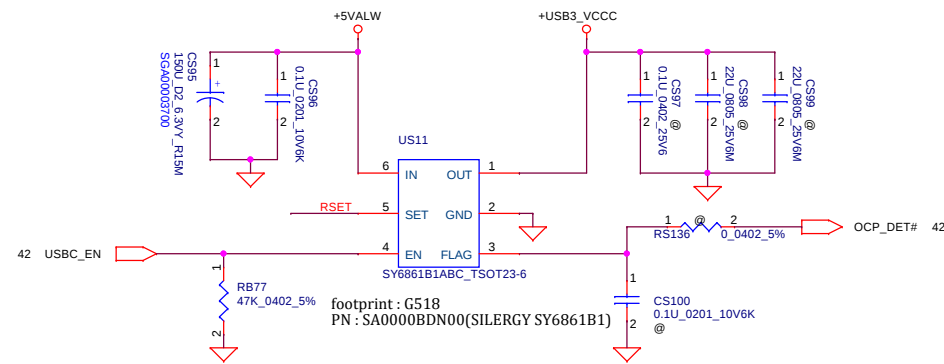


5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

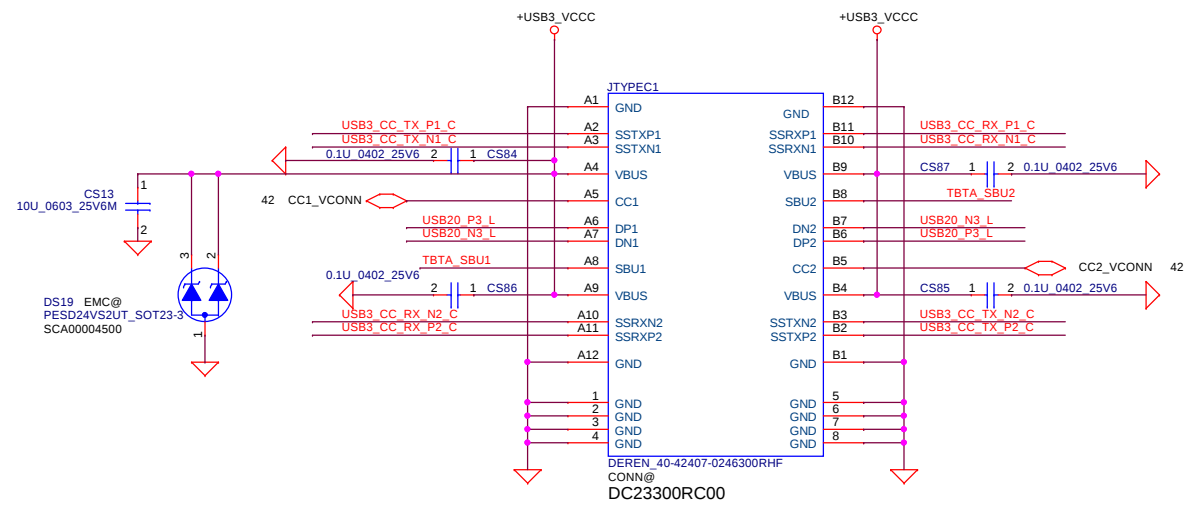
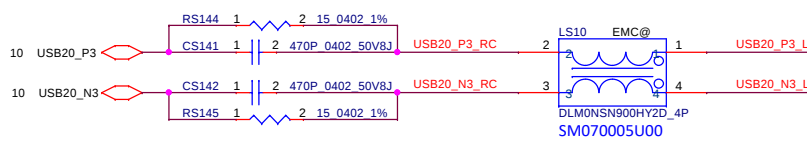
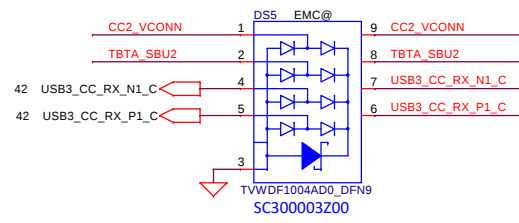
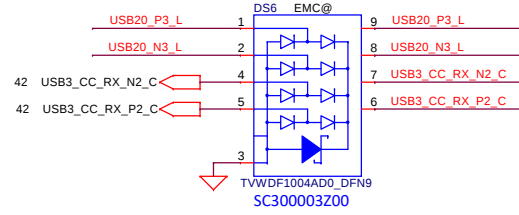
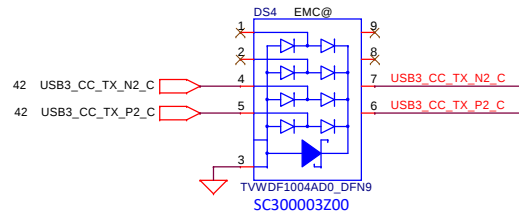
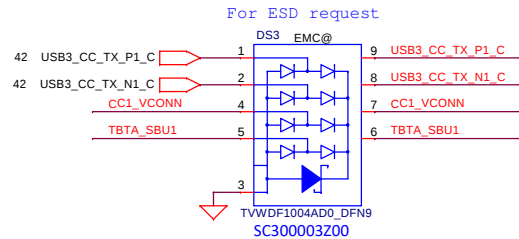
RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

confirm realtek hand-shake

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SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20mil trace width.

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								Size		Document Number				Rev	
								Custom		FH50P M/B LA-H901P				1A	
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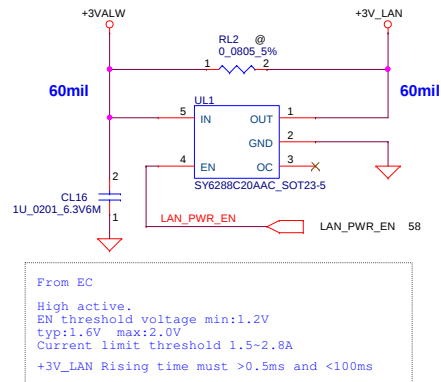
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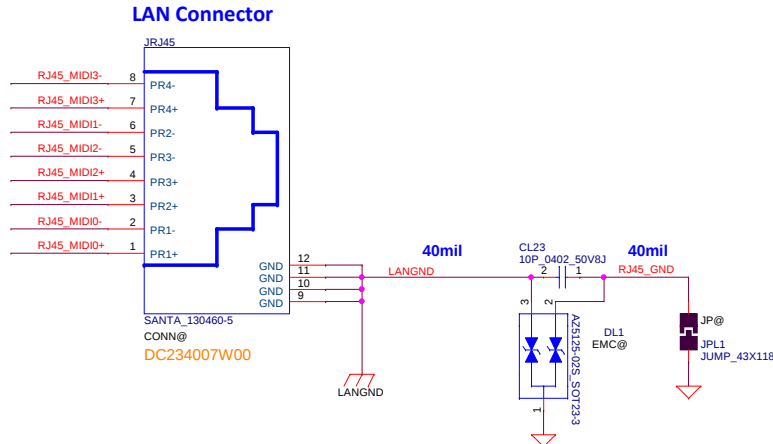
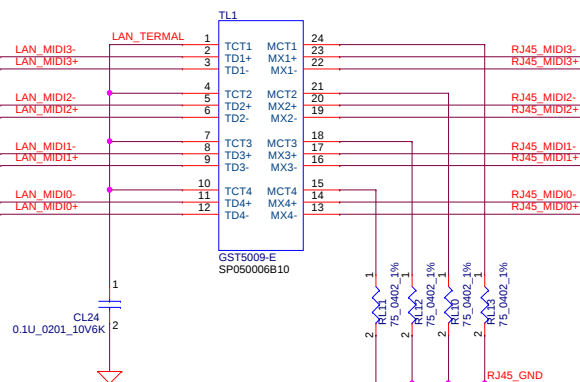
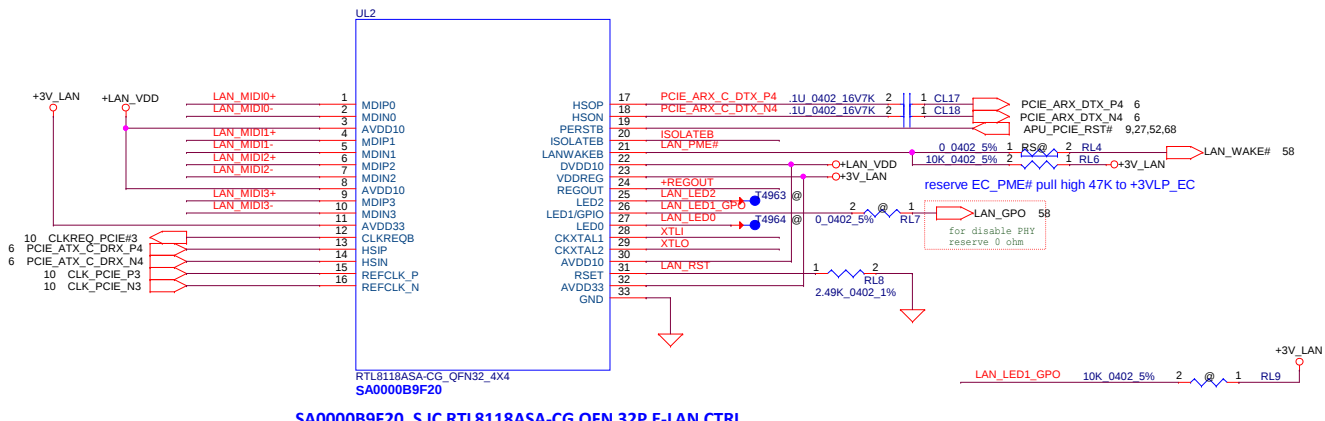
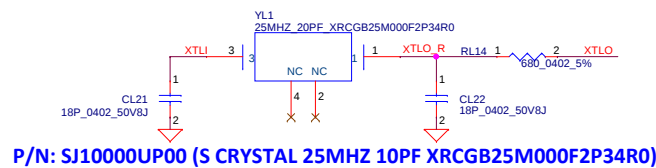
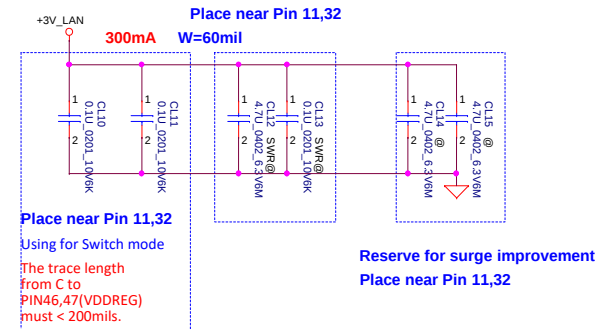
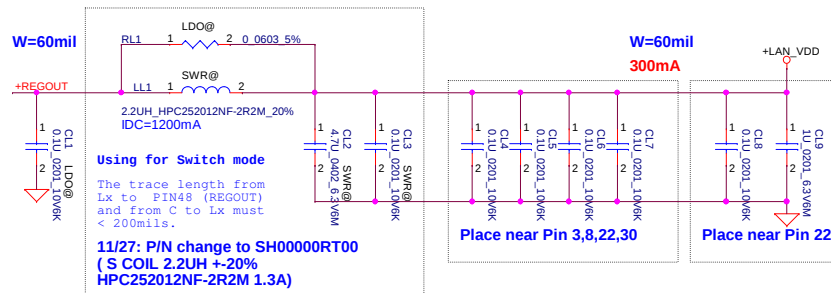
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+3V_LAN Rising time (10%-90%) must >0.5mS and <100mS

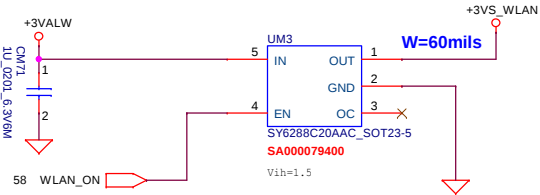
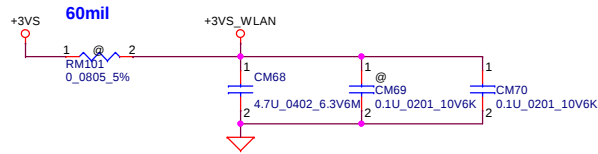


RTL8111H LDO mode
RTL8118ASA SWR mode



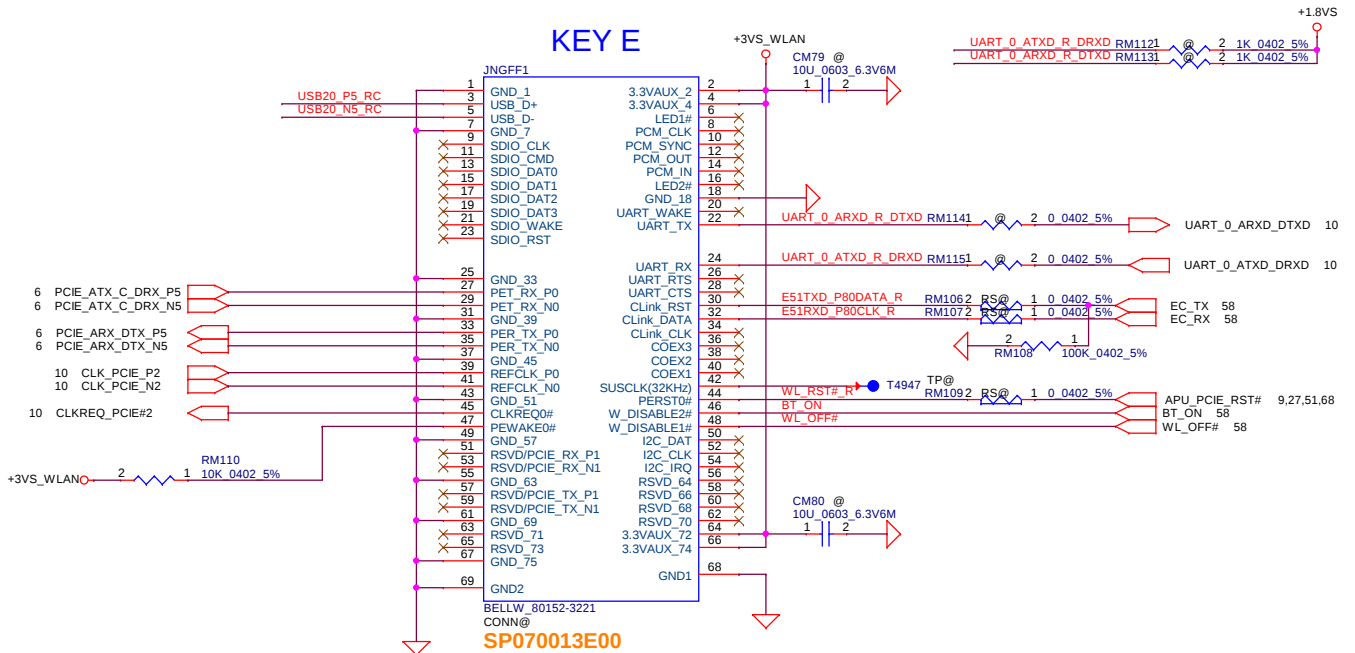
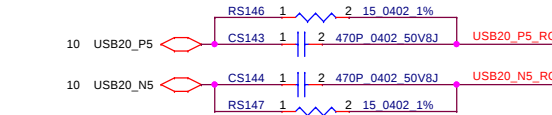
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Wireless LAN



NGFF WL+BT (KEY E)

74	1.3v	GND	75
72	1.8v	RESERVED/REFCLKN1	73
70	UM_Power_SNK/GPIO/PWAVE1#	RESERVED/REFCLKP1	71
68	UM_Power_SNK/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O)(0.3V)	GND	61
60	QCC CLK (I/O)(0.3V)	Reserved/PETn1	61
58	QCC DATA (I/O)(0.3V)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(0.3V)	GND	57
54	Reserved_W_DISABLE#2 (O)(0.3V)	PWAVE#n (O)(0.3V)	55
52	PERST0N (O)(0.3V)	CLKREQ#n (O)(0.3V)	53
50	SUSCn(32MHz) (O)(0.3V)	GND	51
48	CODE1 (I/O)(1.8V)	REFCLKN0	49
46	CODE2(O)(0.1.8V)	REFCLKP0	47
44	CODE3(O)(0.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0.1.8V)	PETn0	37
34	UART CTS (I/O)(1.8V)	PETp0	35
32	UARTTx (O)(0.1.8V)	GND	33
	UART Rx (I/O)(1.8V)	SDIO_RESET# (O)(0.1.8V)	23
22	UART Rx (I/O)(1.8V)	SDIO_Wake# (I)(0.1.8V)	21
20	UART Wake# (I/O)(3.3V)	SDIO DAT#(O)(0.1.8V)	19
18	GND	SDIO DAT#(I/O)(0.1.8V)	17
16	LED2# (I)(I/O)	SDIO DAT#(O)(0.1.8V)	17
14	PCM_OUT/IS_SD_OUT (O)(0.1.8V)	SDIO DAT#(I)(O)(0.1.8V)	15
12	PCM_IN/IS_SD_IN (I/O)(0.1.8V)	SDIO DAT#(O)(0.1.8V)	13
10	PCM_SYNC/IS WS (O)(0.1.8V)	SDIO CMD#(O)(0.1.8V)	11
8	PCM_CLK/IS SCK (O)(0.1.8V)	SDIO CLK#(O)(0.1.8V)	9
6	LED1# (I)(I/O)	GND	7
4	1.8V	USB_D+	5
2	1.8V	USB_D-	3
	1.8V	GND	1



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				Date:	Wednesday, May 15, 2019
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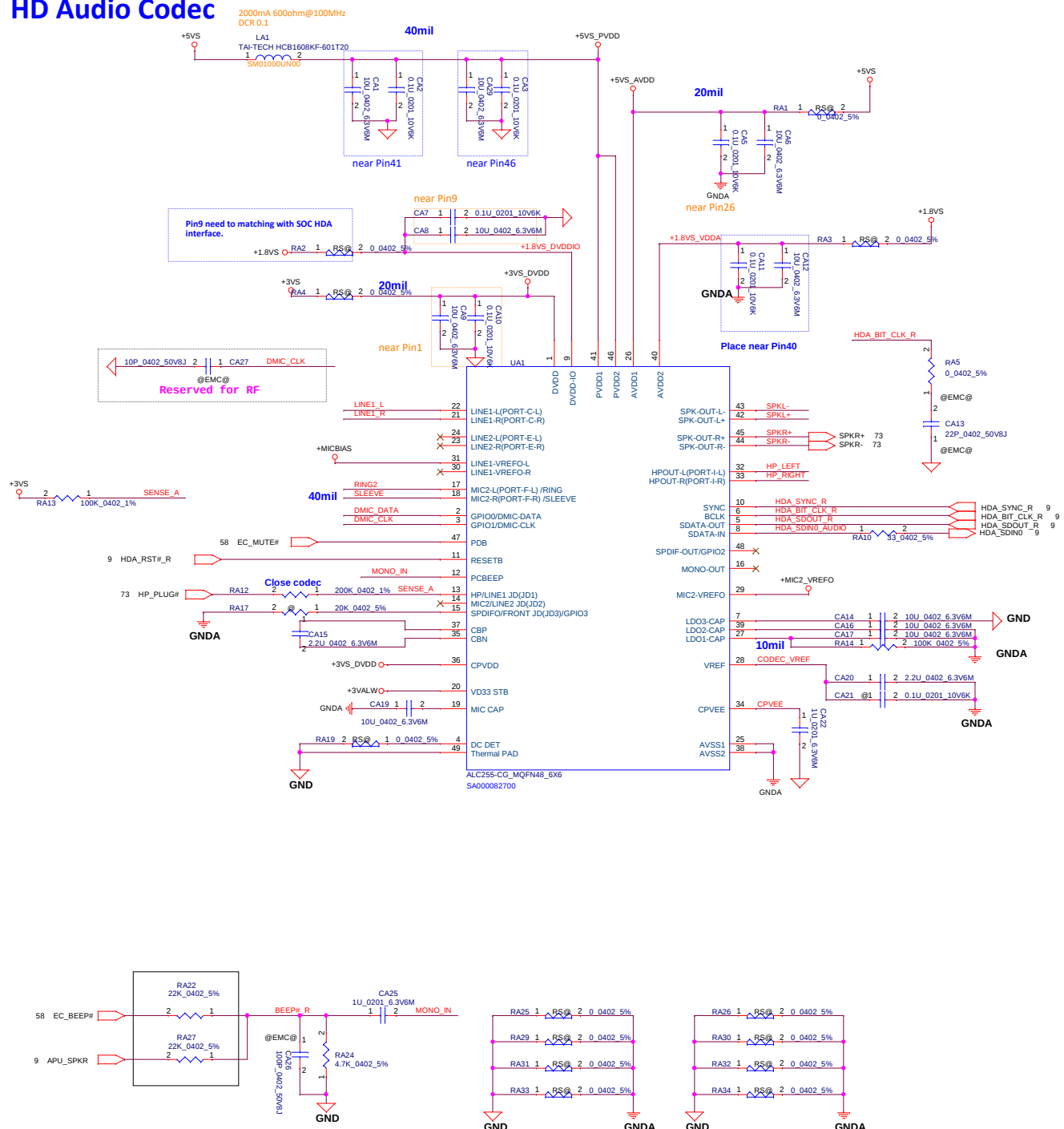
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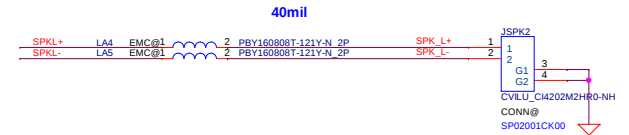
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HD Audio Codec

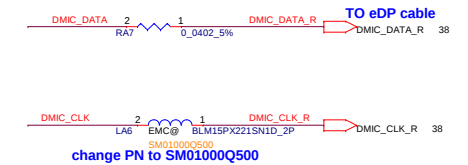


Int. Speaker Conn.

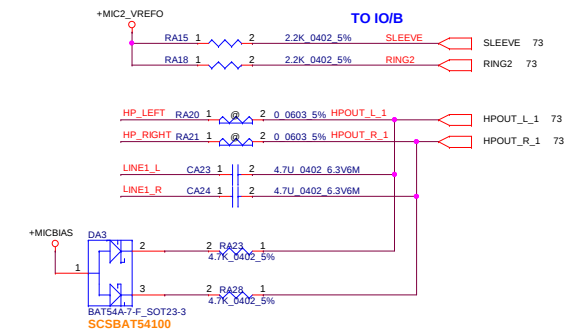


Digital MIC

MIC BOM upload by Audio Team



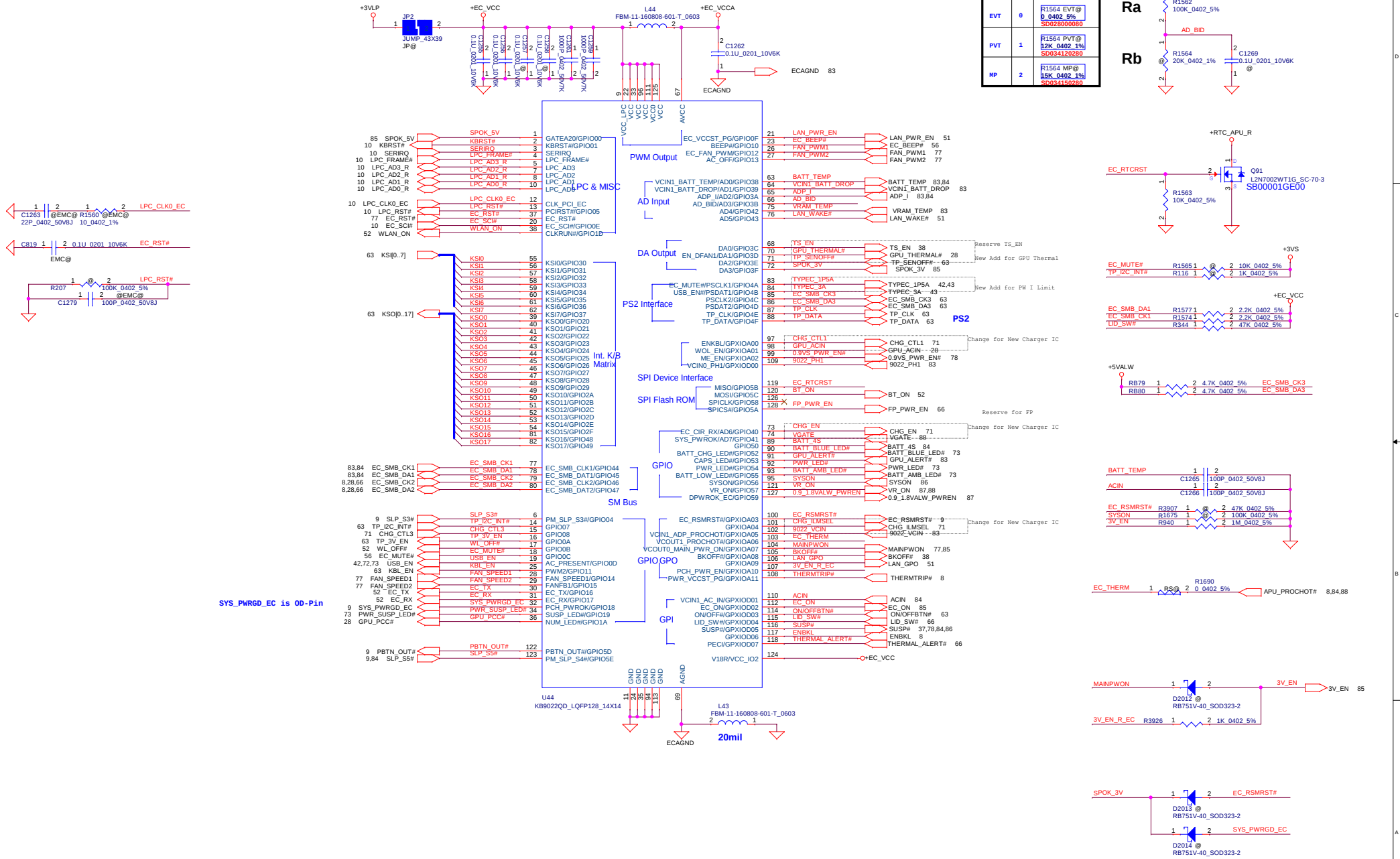
Headphone Out



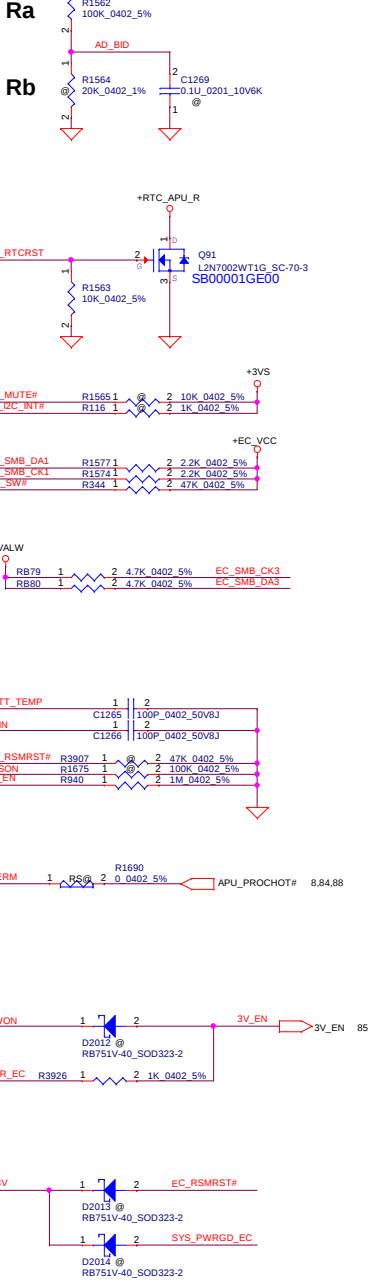
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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	HD Audio Codec ALC255	
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Board ID / Rb			
EVT	0	R1564 EVT@	SD028000080
PVT	1	R1564 PVT@	R2K 0402 1% SD034120280
MP	2	R1564 MP@	18K 0402 1% SD034150280

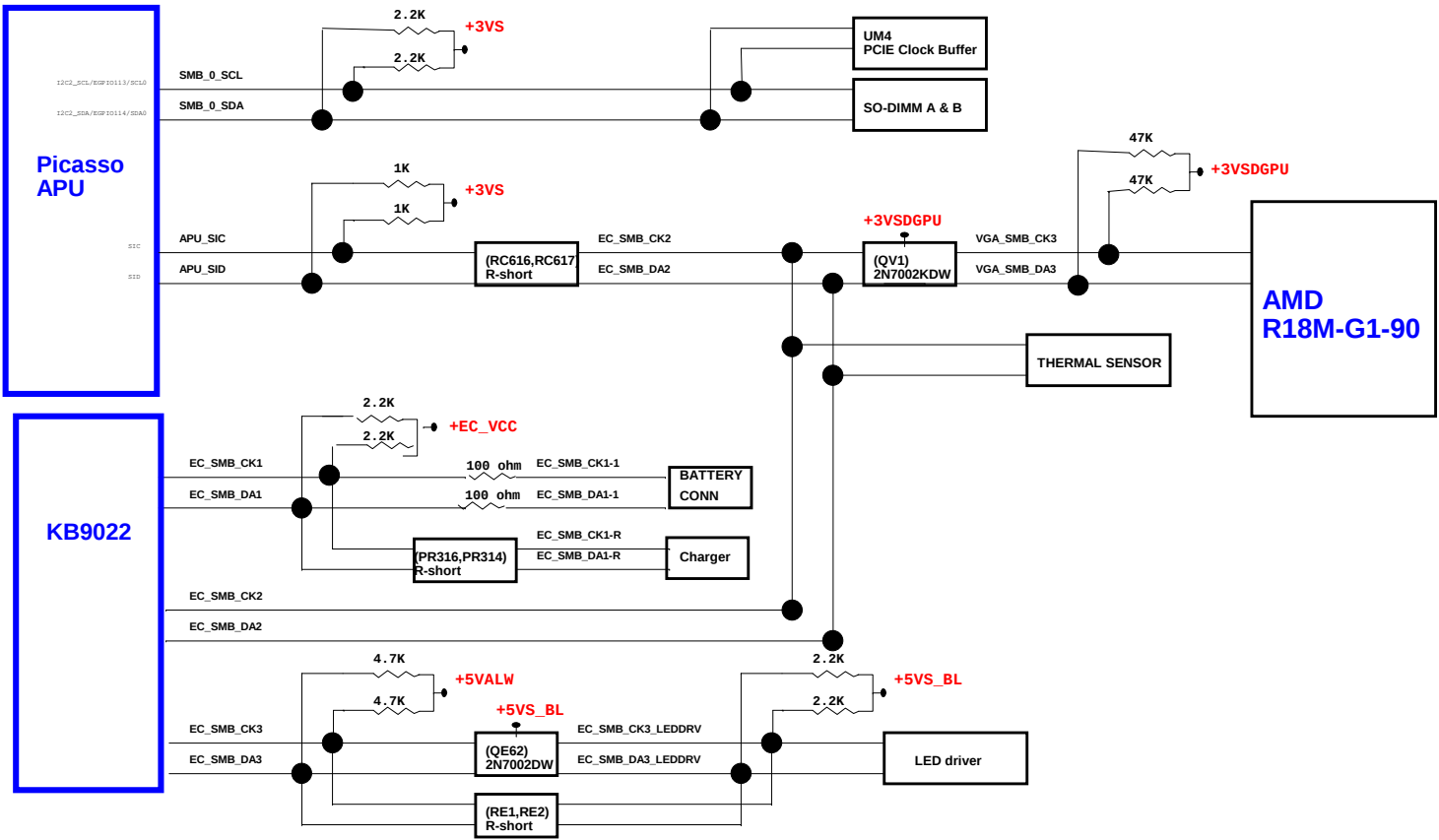


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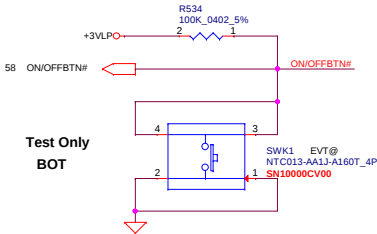
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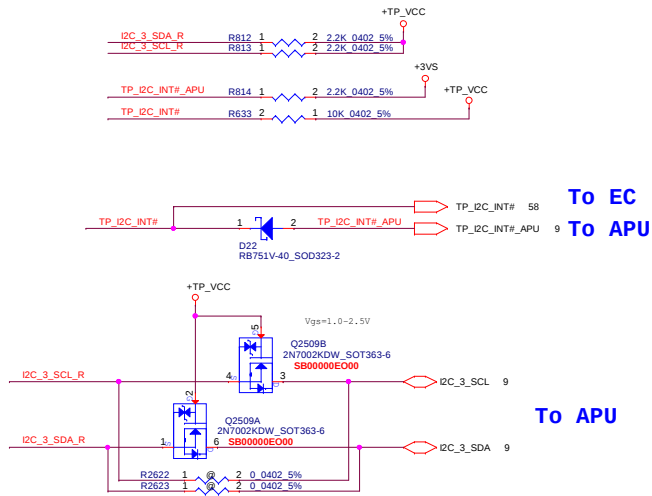
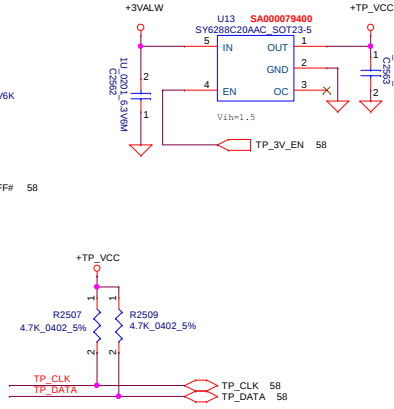
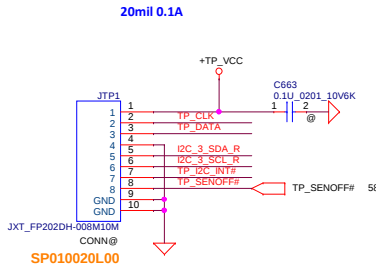
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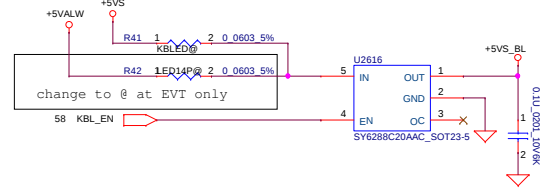
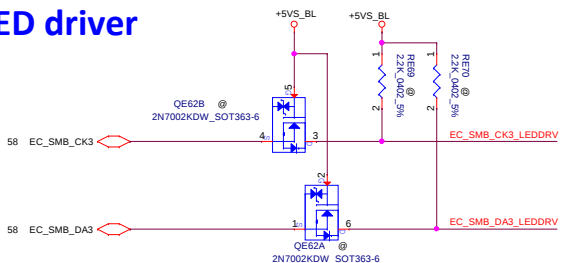
ON/OFF BTN



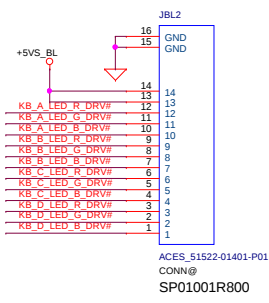
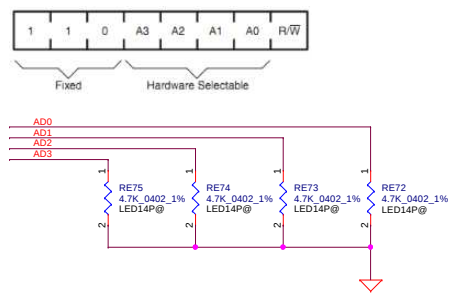
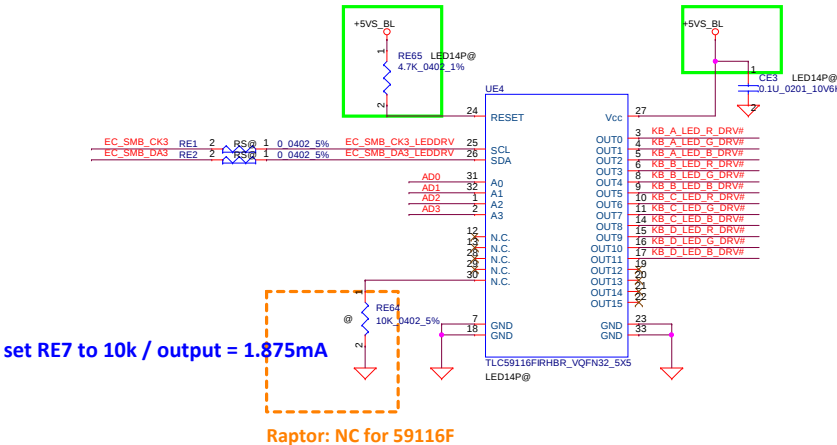
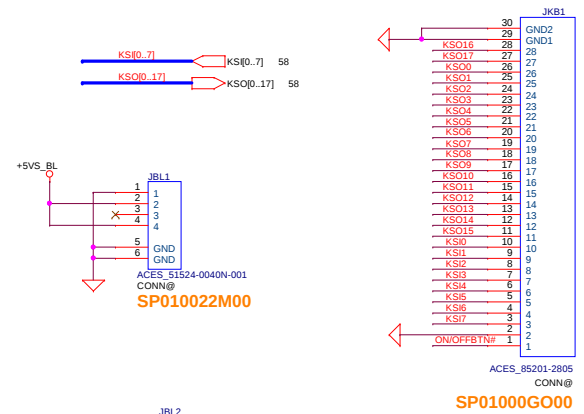
TP/B Conn.



LED driver



KB Conn. / Backlight



KB Conn.
KB BackLight

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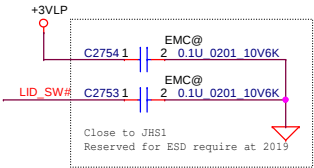
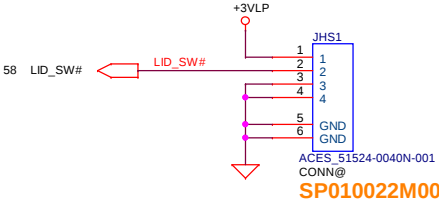
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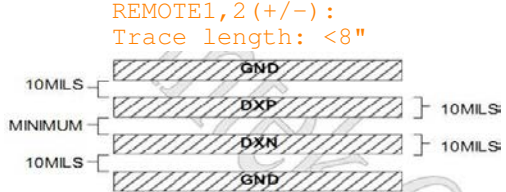
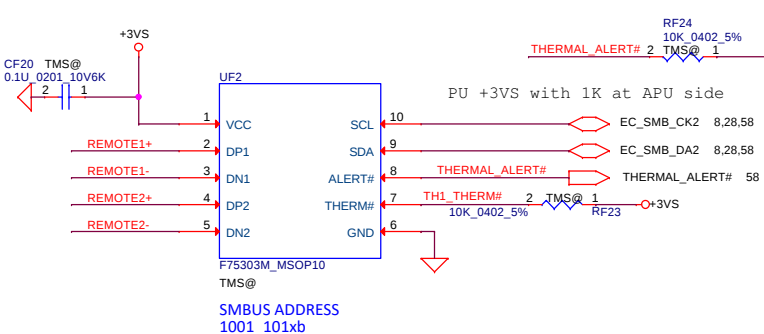
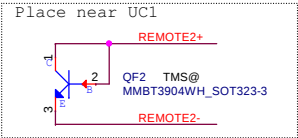
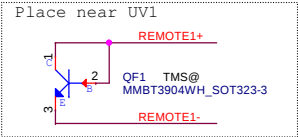
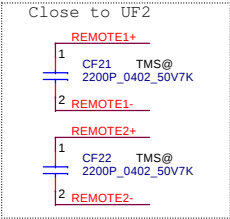
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To Hall sensor/B

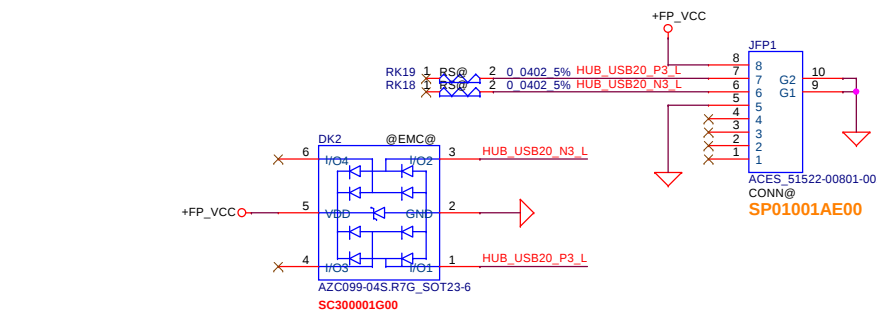
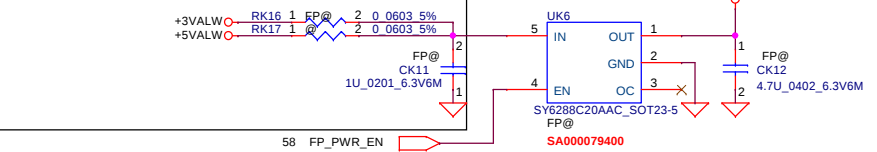


THERMAL SENSOR



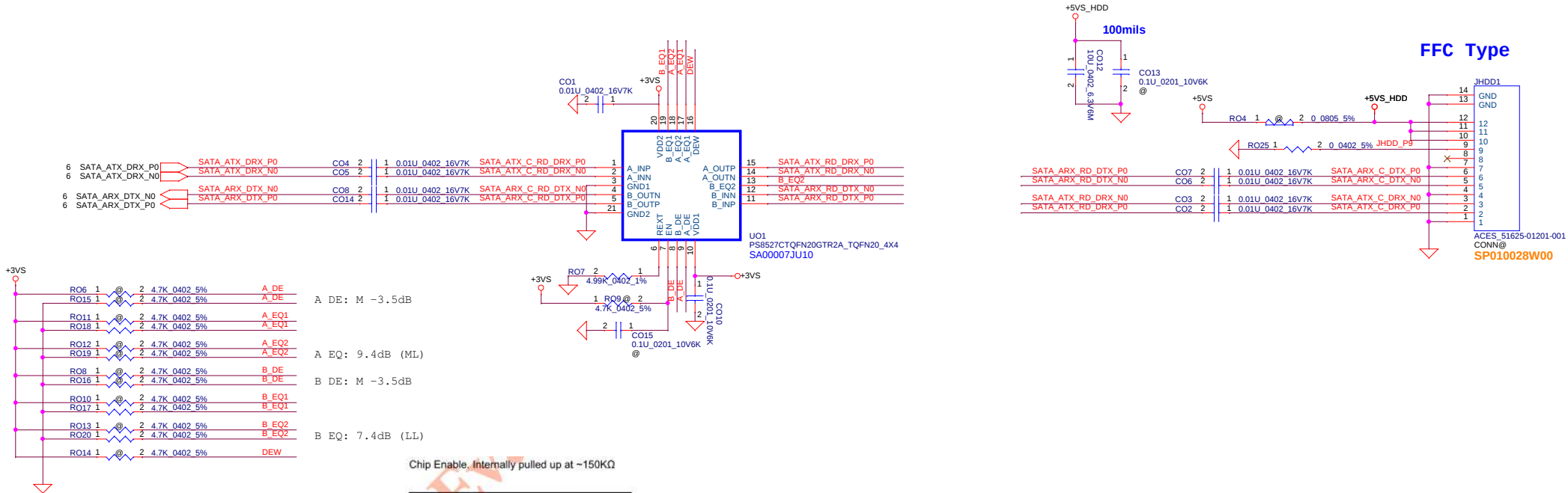
Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

SATA Re-Driver and cable HDD Conn.



Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

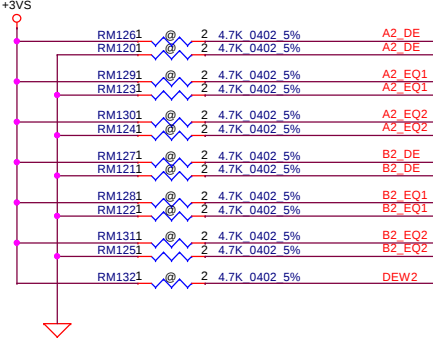
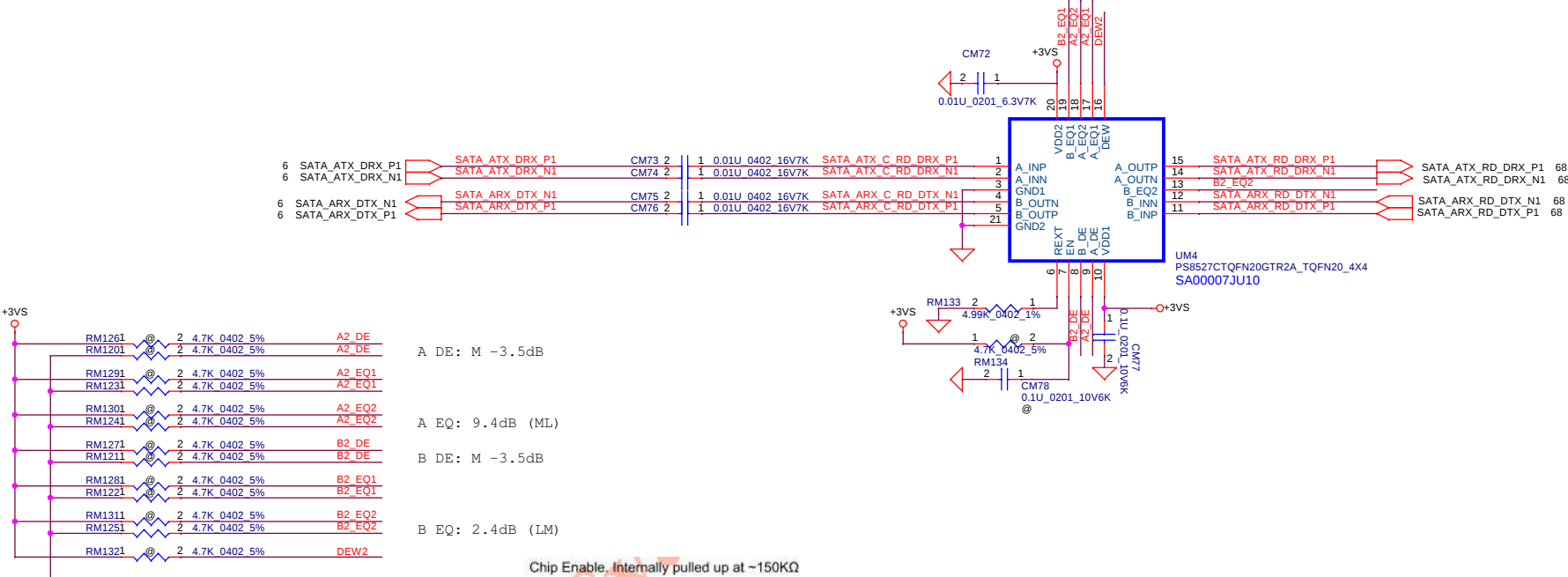
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

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SATA Re-Driver for M.2 Connector



Chip Enable, internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

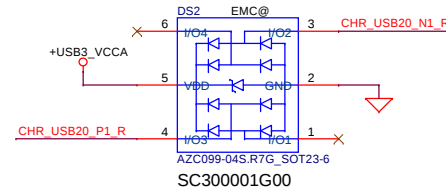
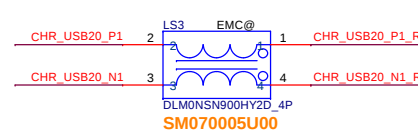
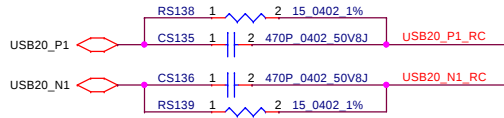
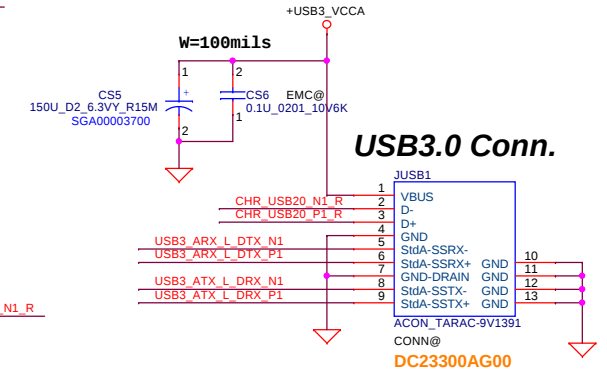
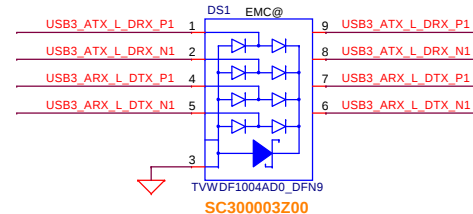
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

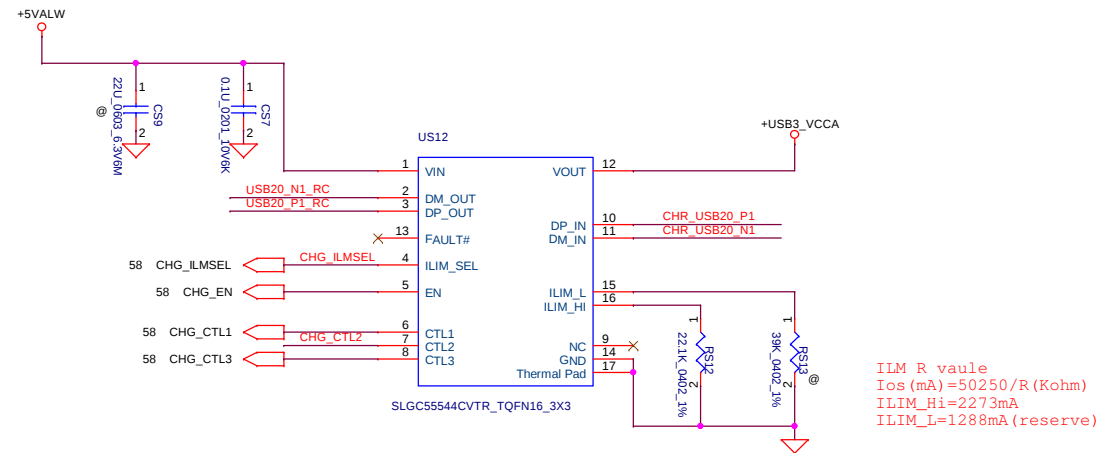
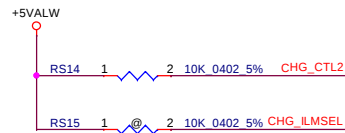
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USB3.0



USB Host Charger

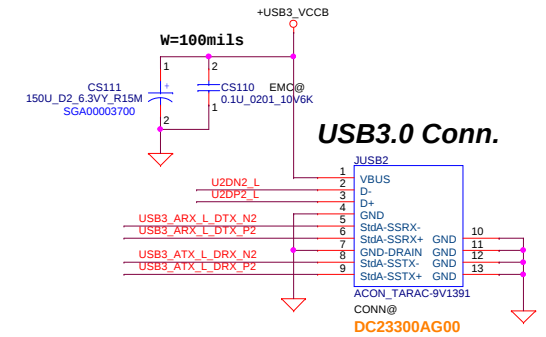
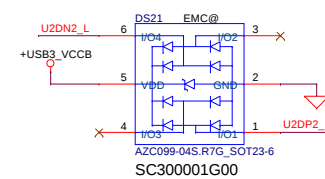
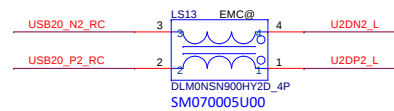
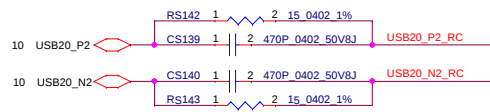
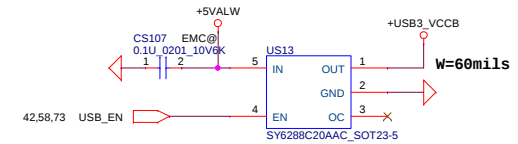
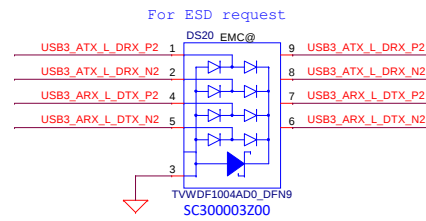


USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

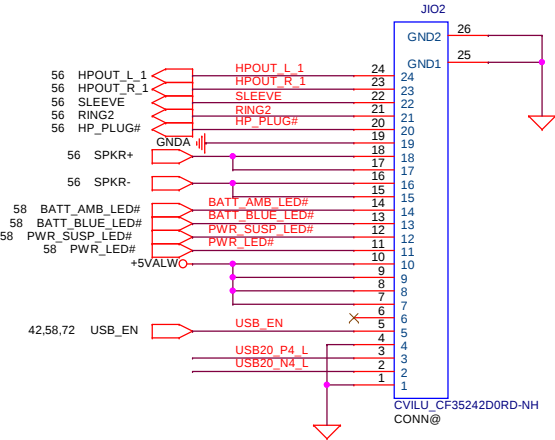
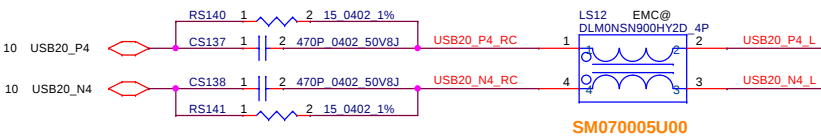
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Issued Date		2018/ 12/18		Deciphered Date		2019/12/18		Title							
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								Size		Document Number				Rev	
								Custom		FH50P M/B LA-H901P				1A	
								Date:		Wednesday, May 15, 2019		Sheet		71 of 99	

USB3.0



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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	USB3.0 Conn
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				FH50P M/B LA-H901P Date: Wednesday, May 15, 2019 Sheet 72 of 99	

IO/B CONN



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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	IO/B Interface
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				Date:	Wednesday, May 15, 2019
				Sheet	74 of 99
				Rev	1A
				FH50P M/B LA-H901P	

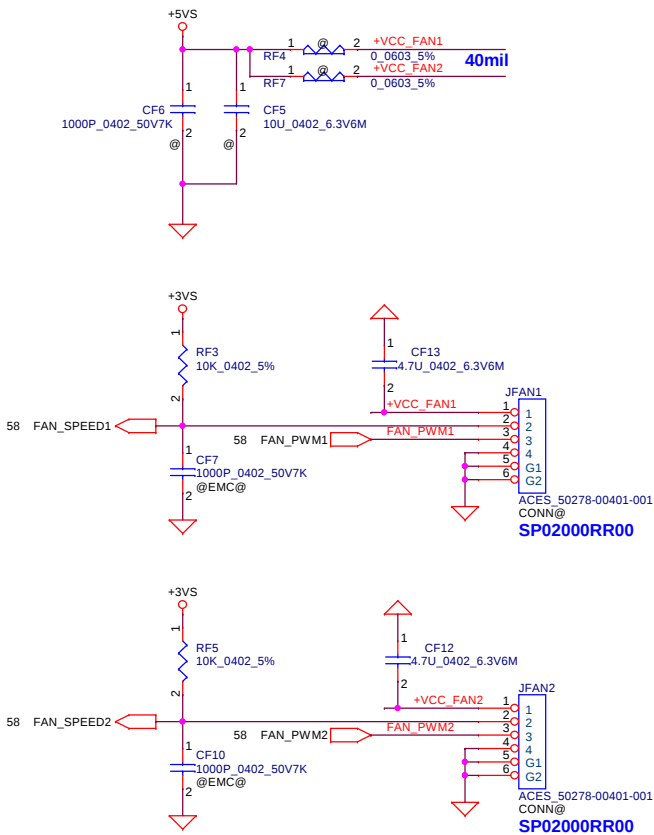
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				Date	Wednesday, May 15, 2019
				Sheet	75 of 99
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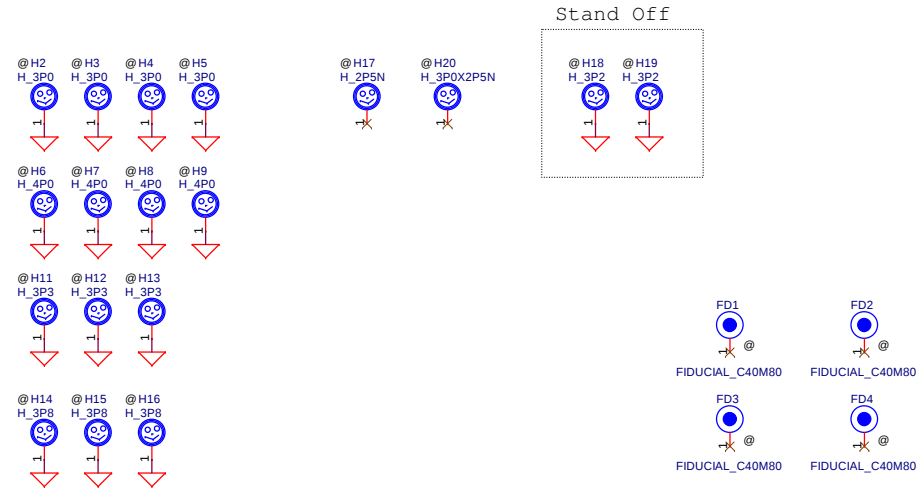
Reserve Page

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				Date	Wednesday, May 15, 2019
				Sheet	76 of 99
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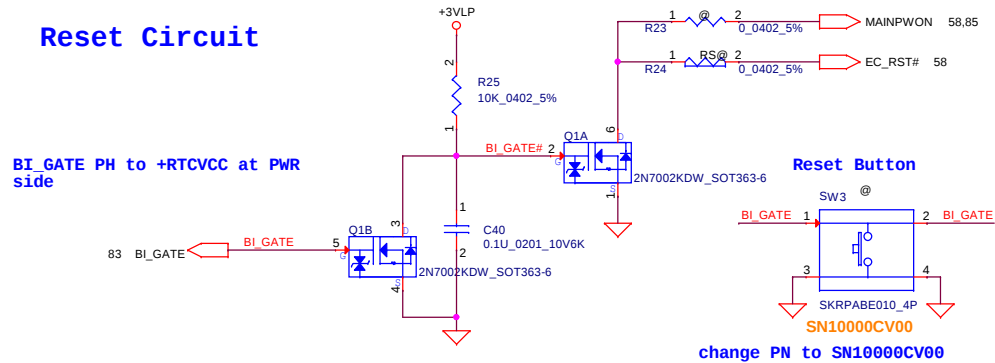
FAN Conn



Screw Hole



Reset Circuit



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				Size	Document Number	Rev
				Custom	FH50P M/B LA-H901P	1A
				Date:	Wednesday, May 15, 2019	Sheet 77 of 99

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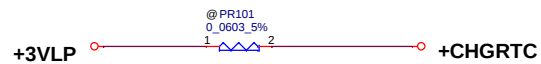
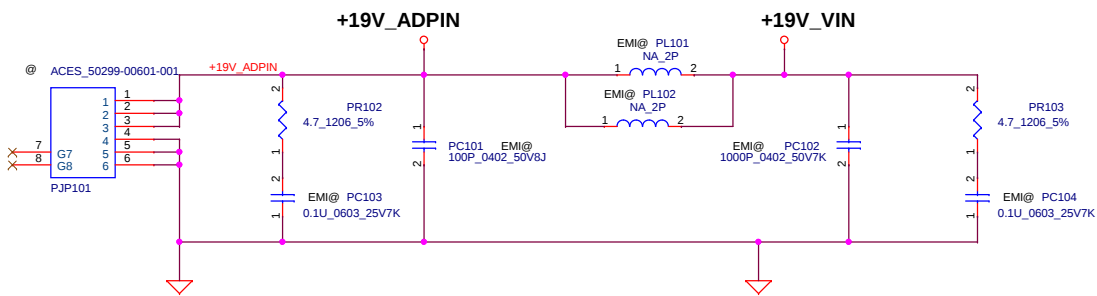
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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	Reserve Page
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				Date:	Wednesday, May 15, 2019
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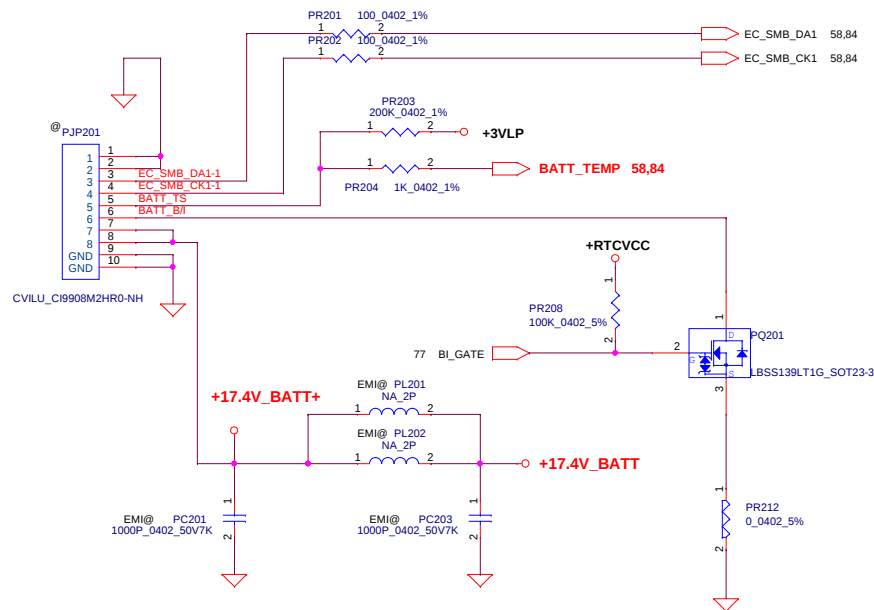
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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	Reserve Page
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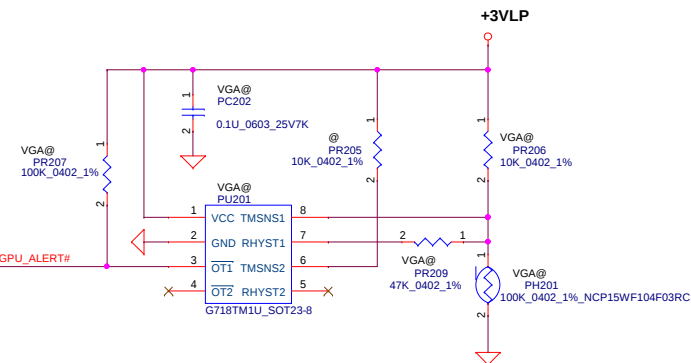
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58 GPU_ALERT#

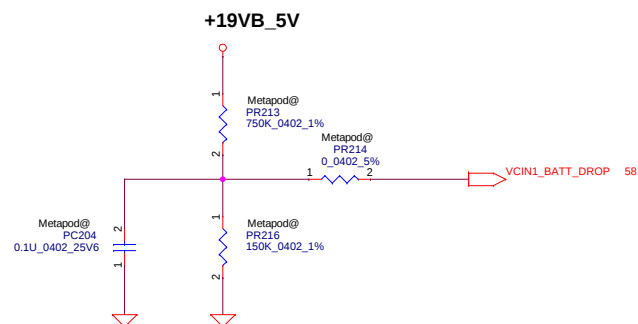


For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

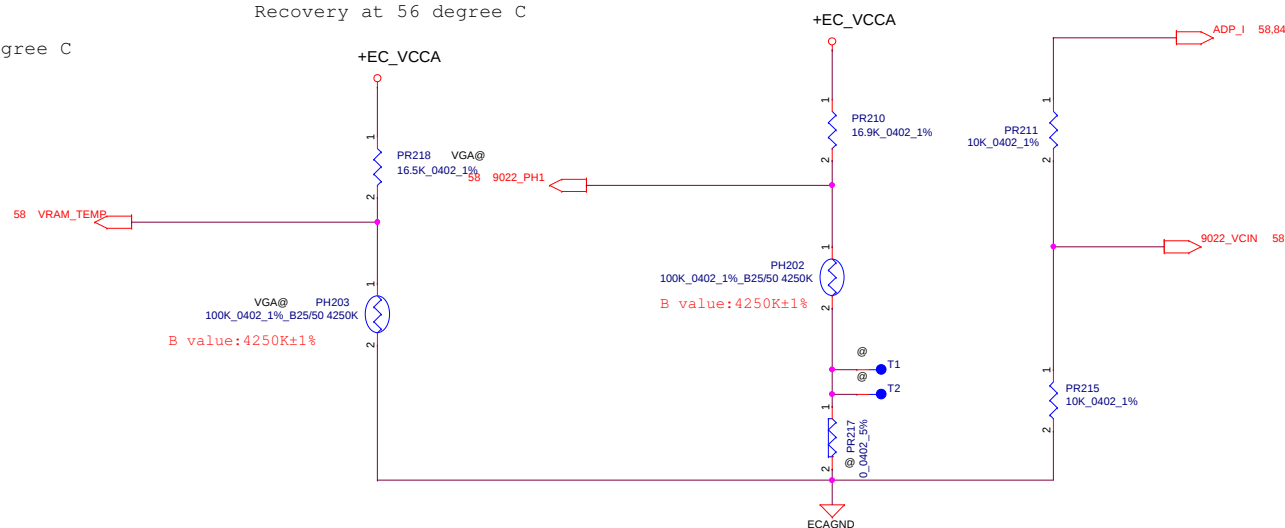
For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

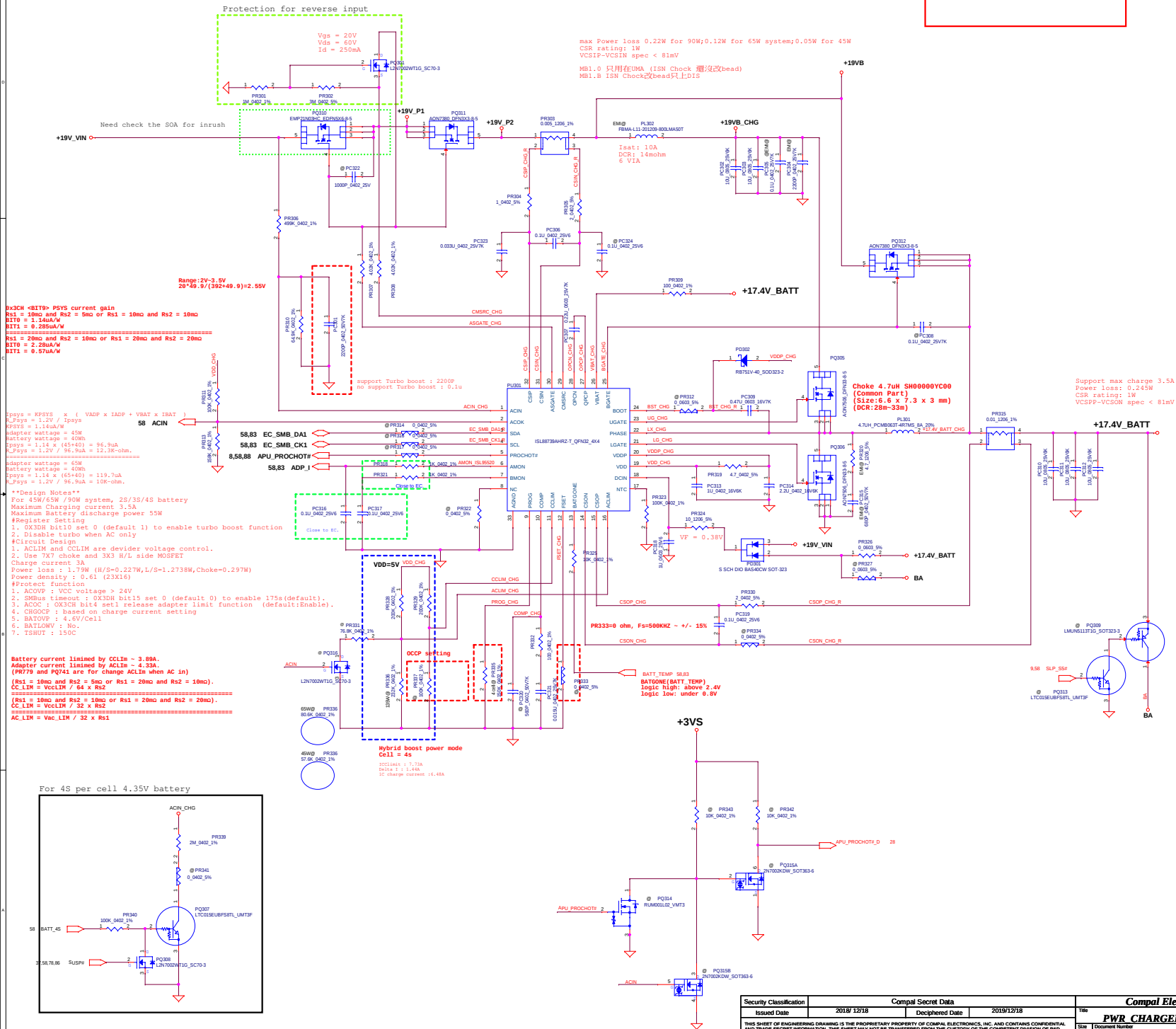
Reserve for 2-cell design



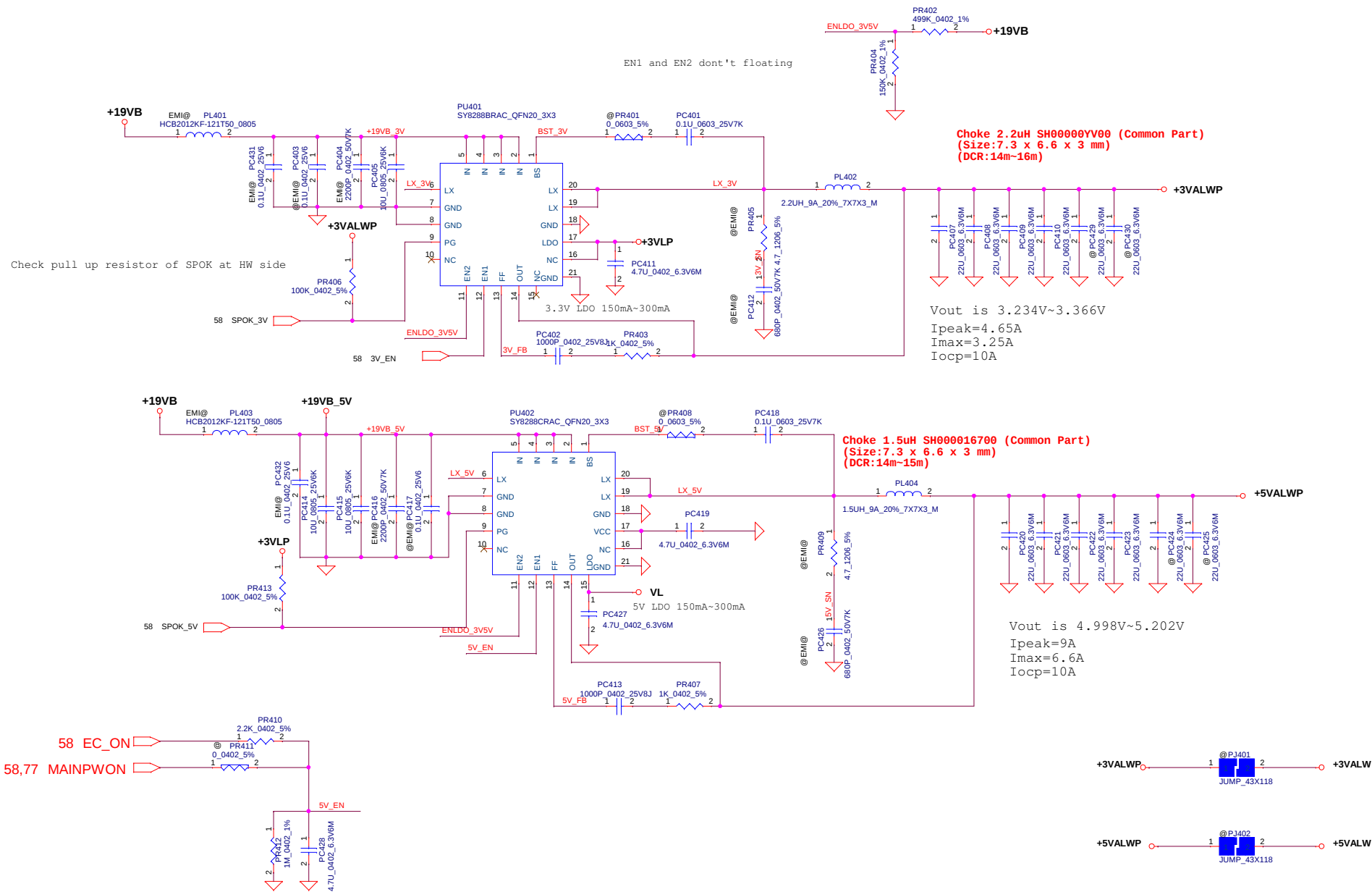
PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C



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										Date:	Wednesday	May 15, 2019	Sheet

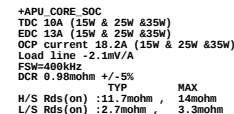


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BT8880C CZ35W V2B.mdd for SW portion



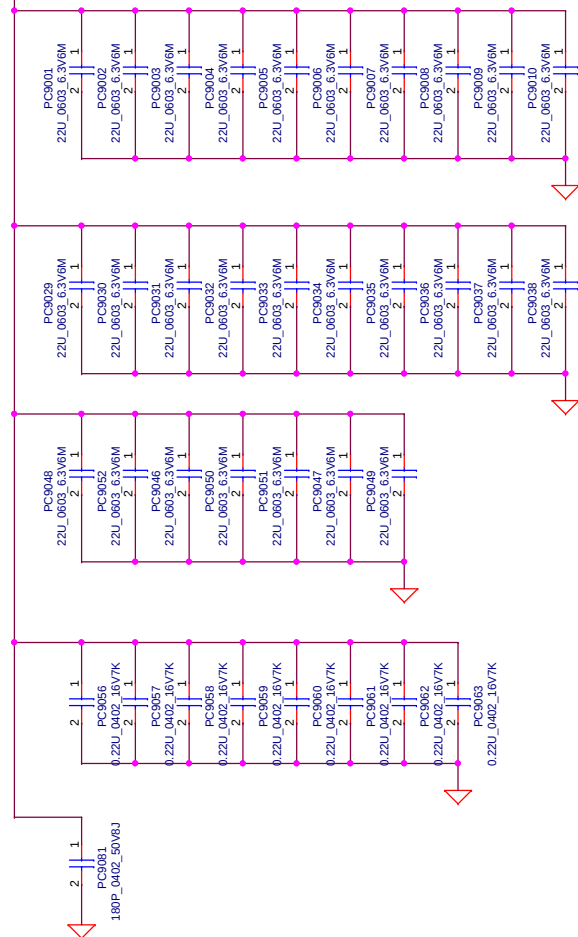
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			New 1A	

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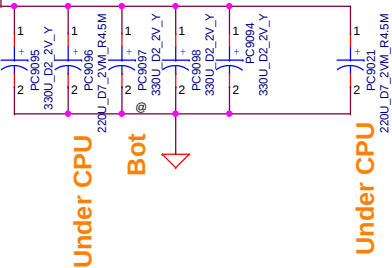
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+APU_CORE

+APU_CORE



+APU_CORE



Under CPU

Bot

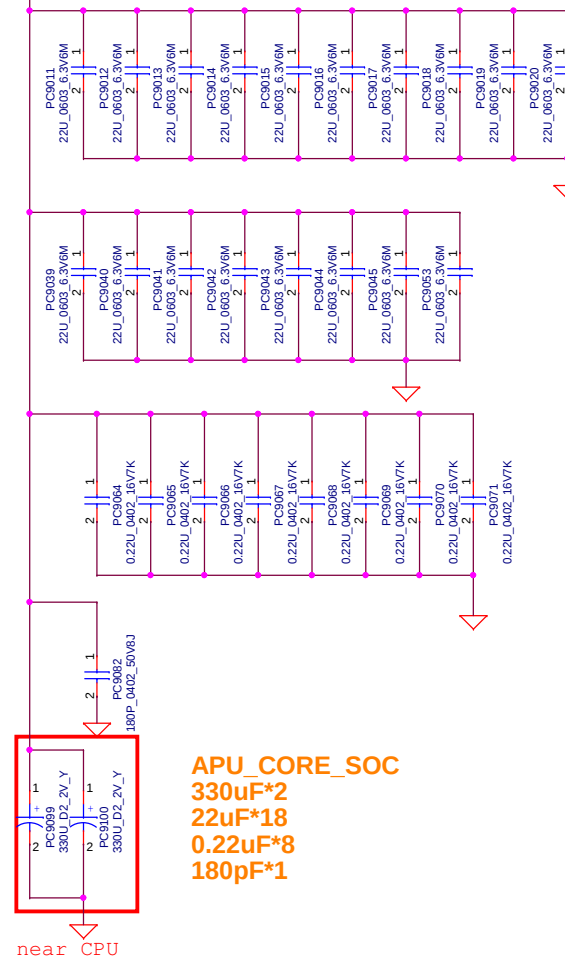
Under CPU

330u is common part SGA00009S00

APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

+APU_CORE_SOC

+APU_CORE_SOC



near CPU

330u is common part SGA00009S00

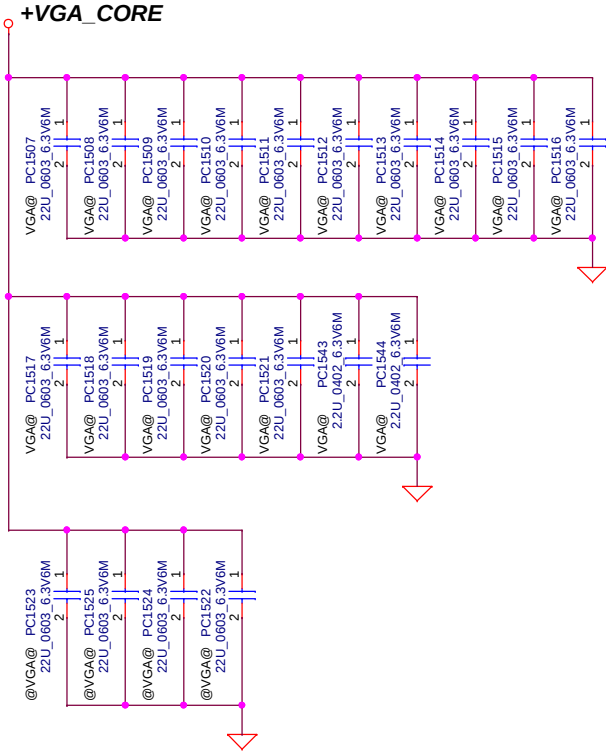
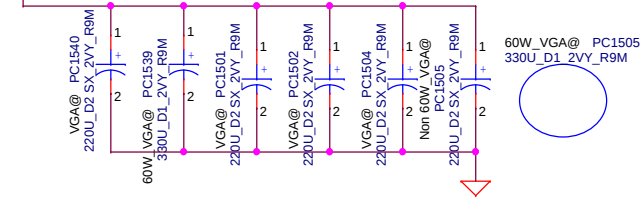
APU_CORE_SOC
330uF*2
22uF*18
0.22uF*8
180pF*1

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Size	Document Number	Rev			1A
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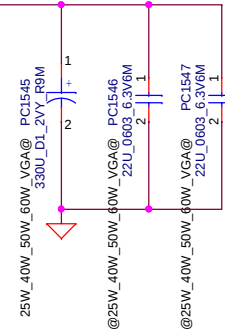


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+VGA_CORE

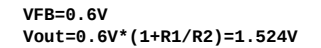


+VDDCI



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				Document Number	1A
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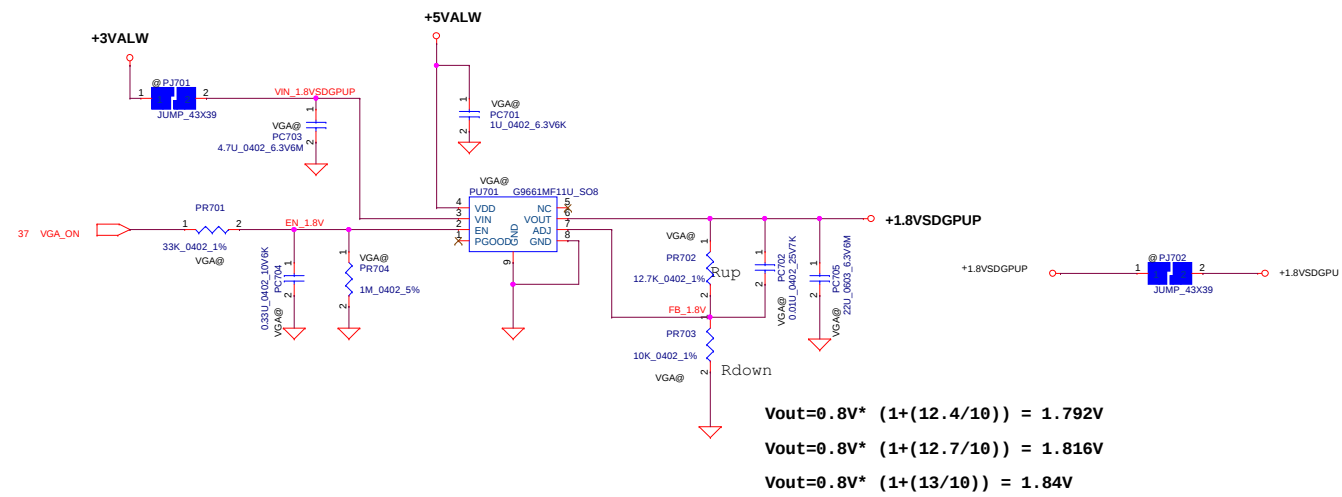
Module model information
SY8208D_V1.mdd



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	POWER Module design Change	0.1		PQ310: EMB04N03H_SB00001C500 -> _EMP21N03HC_SB00001LC00 PC313: 1U_0402_10V6K_SE00000QL10 -> _1U 16V K X5R 0402_SE00000OU00 PC314: 1U_0402_10V6K_SE00000QL10 -> _2.2U 16V K X5R 0402_SE000013780	2019/03/22	A
02	Design Update	CPU_CORE transient and load line test	0.1		PC830: 270P_0402_50V7K_SE074271K80 -> _330P_0402_50V7K_SE074331K80 PR831: 97.6K_0402_1%_SD034976280 -> _110K_0402_1%_SD034110380 Pr806: 34.8K_0402_1%_SD034348280 -> _52.3K_0402_1%_SD034523280 PC9097: 330U_D2_2V_Y_SGA00009S00 -> _Unpop	2019/03/22	A
03							
04	Design Update	reduce part count	0.1		PR212: 0_0402_5%_SD028000080 -> _R-SHORT PR333: 0_0402_5%_SD028000080 -> _R-SHORT PR314: 0_0402_5%_SD028000080 -> _R-SHORT PR316: 0_0402_5%_SD028000080 -> _R-SHORT PR317: 0_0402_5%_SD028000080 -> _R-SHORT	2019/03/22	A
05	Design Update	reduce part count	0.1		Del colay PJ1401 PJ1402 PJ1403	2019/03/22	A
06	Design Update	prochot 調整	0.3		PR304:change R-SHORT SD028000080 0_0402_5% -> SD028100B80 1_0402_5% PC323: add NA -> SE000006O00 0.033U_0402_25V7K PC324: add NA ->@ SE00000G880 0.1U_0402_25V6 PR211: change SD034200280 20K_0402_1% -> SD034100280 10K_0402_1% PR310: change SD034665280 66.5K_0402_1% -> SD034649280 64.9K_0402_1%	2019/04/26	C
07	Design Update	EMI 需求	0.3		PR1437,PR1419,PR1402,PR1463: unpop ->SD001470B804.7_1206_5% PC1442,PC1426,PC1408,PC1467: unpop ->SE074681K80680P_0402_50V7K	2019/05/07	C
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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Issued Date		Deciphered Date		Title	
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