BAD50 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

D12G

緯創資通 Wistron Corporation
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Title: Cover Page		
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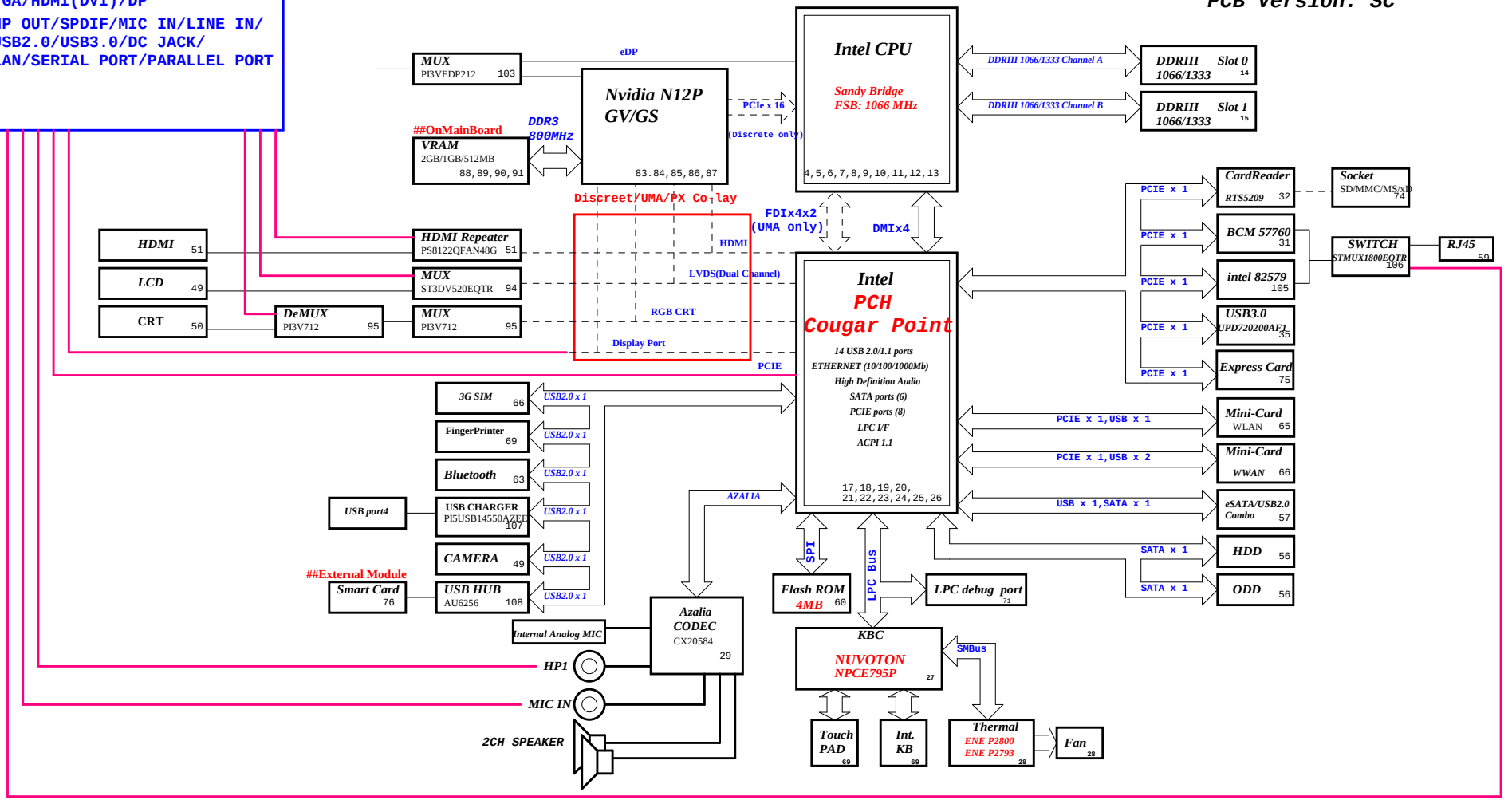
BAD50-HR Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4NM01.001
Project Name: BAD50_HR
PCB No: 10309
PCB Version: SC

Buttom Docking

VGA/HDMI(DVI)/DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



SYSTEM DC/DC TPS5146 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

CPU DC/DC VT1317SFCX 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8237AGQW 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8239CGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT1317SFCX 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208AGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8015AGQW 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC	
INPUTS	OUTPUTS

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: **Block Diagram**

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA Pair	SATA Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

CPU1A
SANDY

1 0F 9

SANDY

DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP

19 DMI_TXN[3:0]
DMI_TXN0 B27 DMI_RX#0
DMI_TXN1 B25 DMI_RX#1
DMI_TXN2 A25 DMI_RX#2
DMI_TXN3 B24 DMI_RX#3

19 DMI_TXP[3:0]
DMI_TXP0 B28 DMI_RX0
DMI_TXP1 B26 DMI_RX1
DMI_TXP2 A24 DMI_RX2
DMI_TXP3 B23 DMI_RX3

19 DMI_RXN[3:0]
DMI_RXN0 G21 DMI_TX#0
DMI_RXN1 E22 DMI_TX#1
DMI_RXN2 F21 DMI_TX#2
DMI_RXN3 D21 DMI_TX#3

19 DMI_RXP[3:0]
DMI_RXP0 G22 DMI_TX0
DMI_RXP1 D22 DMI_TX1
DMI_RXP2 F20 DMI_TX2
DMI_RXP3 C21 DMI_TX3

19 FDI_TXN[7:0]
FDI_TXN0 A21 FDI0_TX#0
FDI_TXN1 H19 FDI0_TX#1
FDI_TXN2 E19 FDI0_TX#2
FDI_TXN3 F18 FDI0_TX#3
FDI_TXN4 B21 FDI1_TX#0
FDI_TXN5 C20 FDI1_TX#1
FDI_TXN6 D18 FDI1_TX#2
FDI_TXN7 E17 FDI1_TX#3

19 FDI_TXP[7:0]
FDI_TXP0 A22 FDI0_TX0
FDI_TXP1 G19 FDI0_TX1
FDI_TXP2 E20 FDI0_TX2
FDI_TXP3 G18 FDI0_TX3
FDI_TXP4 B20 FDI1_TX0
FDI_TXP5 C19 FDI1_TX1
FDI_TXP6 D19 FDI1_TX2
FDI_TXP7 F17 FDI1_TX3

19 FDI_FSYNC0 J18 FDI0_FSYNC
19 FDI_FSYNC1 J17 FDI1_FSYNC
19 FDI_INT H20 FDI_INT
19 FDI_LSYNC0 J19 FDI0_LSYNC
19 FDI_LSYNC1 H17 FDI1_LSYNC

1D05V_VTT
R402 1 24D9R2F-L-GP DP_COMP A18 EDP_COMPIO
R403 1 10KR2J-3-GP eDP_HPD A17 EDP_ICOMPO
B16 EDP_HPD

103 eDP_AUXP_CPU C15 EDP_AUX
103 eDP_AUXN_CPU D15 EDP_AUX#

103 eDP_TXP0_CPU C17 EDP_TX0
103 eDP_TXP1_CPU F16 EDP_TX1
C16 EDP_TX2
G15 EDP_TX3

103 eDP_TXN0_CPU C18 EDP_TX#0
103 eDP_TXN1_CPU E16 EDP_TX#1
D16 EDP_TX#2
F15 EDP_TX#3

PEG_ICOMPI J22 PEG_IRCOMP_R R401 1 24D9R2F-L-GP 1D05V_VTT
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RXN[0..15] 83
PEG_RX#0 K33 PEG_RXN15
PEG_RX#1 M35 PEG_RXN14
PEG_RX#2 L34 PEG_RXN13
PEG_RX#3 J35 PEG_RXN12
PEG_RX#4 J32 PEG_RXN11
PEG_RX#5 H34 PEG_RXN10
PEG_RX#6 H31 PEG_RXN9
PEG_RX#7 G33 PEG_RXN8
PEG_RX#8 G30 PEG_RXN7
PEG_RX#9 F35 PEG_RXN6
PEG_RX#10 E34 PEG_RXN5
PEG_RX#11 E32 PEG_RXN4
PEG_RX#12 D33 PEG_RXN3
PEG_RX#13 D31 PEG_RXN2
PEG_RX#14 B33 PEG_RXN1
PEG_RX#15 C32 PEG_RXN0

PEG_RXP[0..15] 83
PEG_RX0 J33 PEG_RXP15
PEG_RX1 L35 PEG_RXP14
PEG_RX2 K34 PEG_RXP13
PEG_RX3 H35 PEG_RXP12
PEG_RX4 H32 PEG_RXP11
PEG_RX5 G34 PEG_RXP10
PEG_RX6 G31 PEG_RXP9
PEG_RX7 F33 PEG_RXP8
PEG_RX8 F30 PEG_RXP7
PEG_RX9 E35 PEG_RXP6
PEG_RX10 E33 PEG_RXP5
PEG_RX11 E32 PEG_RXP4
PEG_RX12 D34 PEG_RXP3
PEG_RX13 E31 PEG_RXP2
PEG_RX14 C33 PEG_RXP1
PEG_RX15 B32 PEG_RXP0

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

PEG_TXN[0..15] 83
PEG_TX#0 M29 PEG_C_TXN15 C401 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN15
PEG_TX#1 M32 PEG_C_TXN14 C402 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN14
PEG_TX#2 M31 PEG_C_TXN13 C403 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN13
PEG_TX#3 L32 PEG_C_TXN12 C404 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN12
PEG_TX#4 L29 PEG_C_TXN11 C405 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN11
PEG_TX#5 K31 PEG_C_TXN10 C406 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN10
PEG_TX#6 K28 PEG_C_TXN9 C407 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN9
PEG_TX#7 J30 PEG_C_TXN8 C408 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN8
PEG_TX#8 J28 PEG_C_TXN7 C409 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN7
PEG_TX#9 H29 PEG_C_TXN6 C410 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN6
PEG_TX#10 G27 PEG_C_TXN5 C411 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN5
PEG_TX#11 F29 PEG_C_TXN4 C412 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN4
PEG_TX#12 F27 PEG_C_TXN3 C413 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN3
PEG_TX#13 D28 PEG_C_TXN2 C414 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN2
PEG_TX#14 F26 PEG_C_TXN1 C415 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN1
PEG_TX#15 E25 PEG_C_TXN0 C416 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXN0

PEG_TXP[0..15] 83
PEG_TX0 M28 PEG_C_TXP15 C417 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP15
PEG_TX1 M33 PEG_C_TXP14 C418 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP14
PEG_TX2 M30 PEG_C_TXP13 C419 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP13
PEG_TX3 L31 PEG_C_TXP12 C420 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP12
PEG_TX4 L28 PEG_C_TXP11 C421 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP11
PEG_TX5 K30 PEG_C_TXP10 C422 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP10
PEG_TX6 K27 PEG_C_TXP9 C423 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP9
PEG_TX7 J29 PEG_C_TXP8 C424 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP8
PEG_TX8 J27 PEG_C_TXP7 C425 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP7
PEG_TX9 H28 PEG_C_TXP6 C426 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP6
PEG_TX10 G28 PEG_C_TXP5 C427 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP5
PEG_TX11 E28 PEG_C_TXP4 C428 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP4
PEG_TX12 F28 PEG_C_TXP3 C429 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP3
PEG_TX13 D27 PEG_C_TXP2 C430 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP2
PEG_TX14 E26 PEG_C_TXP1 C431 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP1
PEG_TX15 D25 PEG_C_TXP0 C432 DIS_PX_Muxless SCD22U10V2KX-1GP PEG_TXP0

全改MUX

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

103 eDP_HPD_R
Do Not Stuff
R408 UMA_EDP
Do Not Stuff
Q401 UMA_EDP
Do Not Stuff
eDP_HPD

2ND = 84.2N702.031

Stuff to disable internal graphics function for power saving.

FDI_LSYNC0
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC1
FDI_INT
R404 Do Not Stuff DIS
RN401 Do Not Stuff DIS

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Title: CPU (PCIE/DMI/FDI)
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SSID = CPU

CPU1B
SANDY

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MISC
- 18 H_SNB_IVB# → C26 SNB_IVB#
- JE40 modify AN34 SKTOCC#

THERMAL
- JE40 modify AL33 CATERR#
- 22,27 H_PECI AN33 PECI
- 27,42 H_PROCHOT# → R513 1 56R2J-4-GP H_PROCHOT# R AL32 PROCHOT#
- 22,36 H_THERMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
- 19 H_PM_SYNC AM34 PM_SYNC
- 22,36,97 H_CPUPWRGD → R503 1 10KR2J-3-GP 2 AP33 UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD → R505 1 DX Do Not Stuff V8 SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# AR33 RESET#

CLOCKS
- BCLK A28 CLK_EXP_P 20
- BCLK# A27 CLK_EXP_N 20
- DPLL_REF_SSCLK A16 CLK_DP_P_R → CLK_DP_P_R 20
- DPLL_REF_SSCLK# A15 CLK_DP_N_R → CLK_DP_N_R 20

DDR3 MISC
- SM_DRAMRST# R8 R502 1 4K99R2F-L-GP SM_DRAMRST# 37
- SM_RCOMP0 AK1 SM_RCOMP_0 R506 1 140R2F-GP
- SM_RCOMP1 A5 SM_RCOMP_1 R507 1 25D5R2F-GP
- SM_RCOMP2 A4 SM_RCOMP_2 R508 1 200R2F-L-GP

JTAG & BPM
- PRDY# AP29
- PREQ# AP27
- JE40 modify
- TCK AR26
- TMS AR27
- TRST# AP30 XDP_TRST#
- TDI AR28
- TDO AP26 XDP_TDO
- DBR# AL35 XDP_DBRESET#
- BPM#0 AT28
- BPM#1 AR29
- BPM#2 AR30
- BPM#3 AT30
- BPM#4 AP32
- BPM#5 AR31
- BPM#6 AT31
- BPM#7 AR32
- JE40 modify

1D05V_VTT
R501 62R2J-GP 1
H_PROCHOT#
C502 SC47P50V2JN-3GP 2
C502:
47pf@CRB
43pf@CEKLT

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CLK_DP_N_R 2
CLK_DP_P_R 1
RN502 DIS Do Not Stuff
1D05V_VTT

1D05V_VTT
RN501 SRN51J-GP
XDP_TDO 2
XDP_TRST# 1
4

3D3V_S0
RN503 SRN1K5J-1-GP
XDP_DBRESET# 1
35,36,65,66,71,75,82,83,97,105,108 PLT_RST# 2
3
4
8
7
6
5
BUF_CPU_RST#

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Title: CPU (THERMAL/CLOCK/PM)

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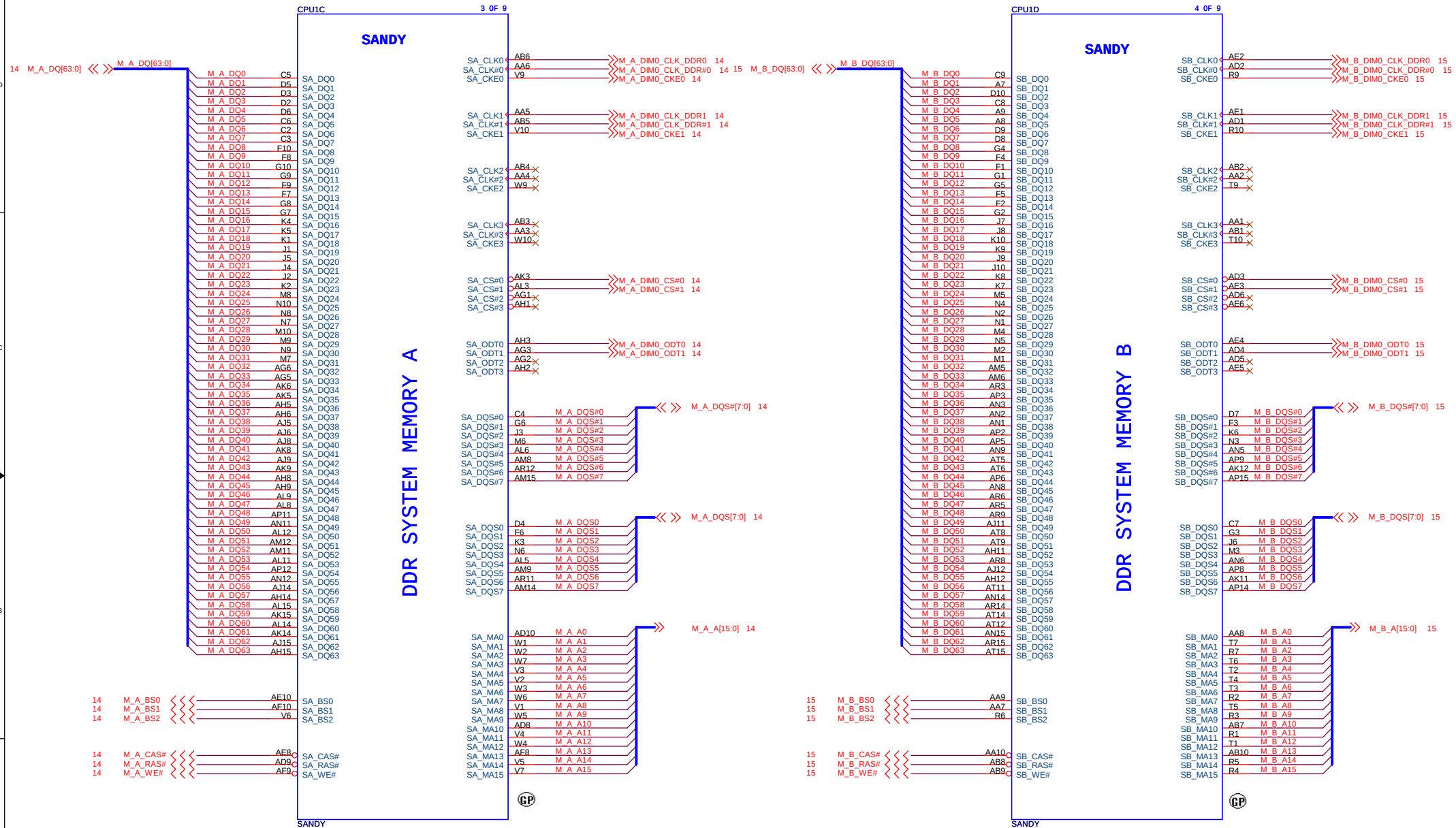
SSID = CPU



D12G

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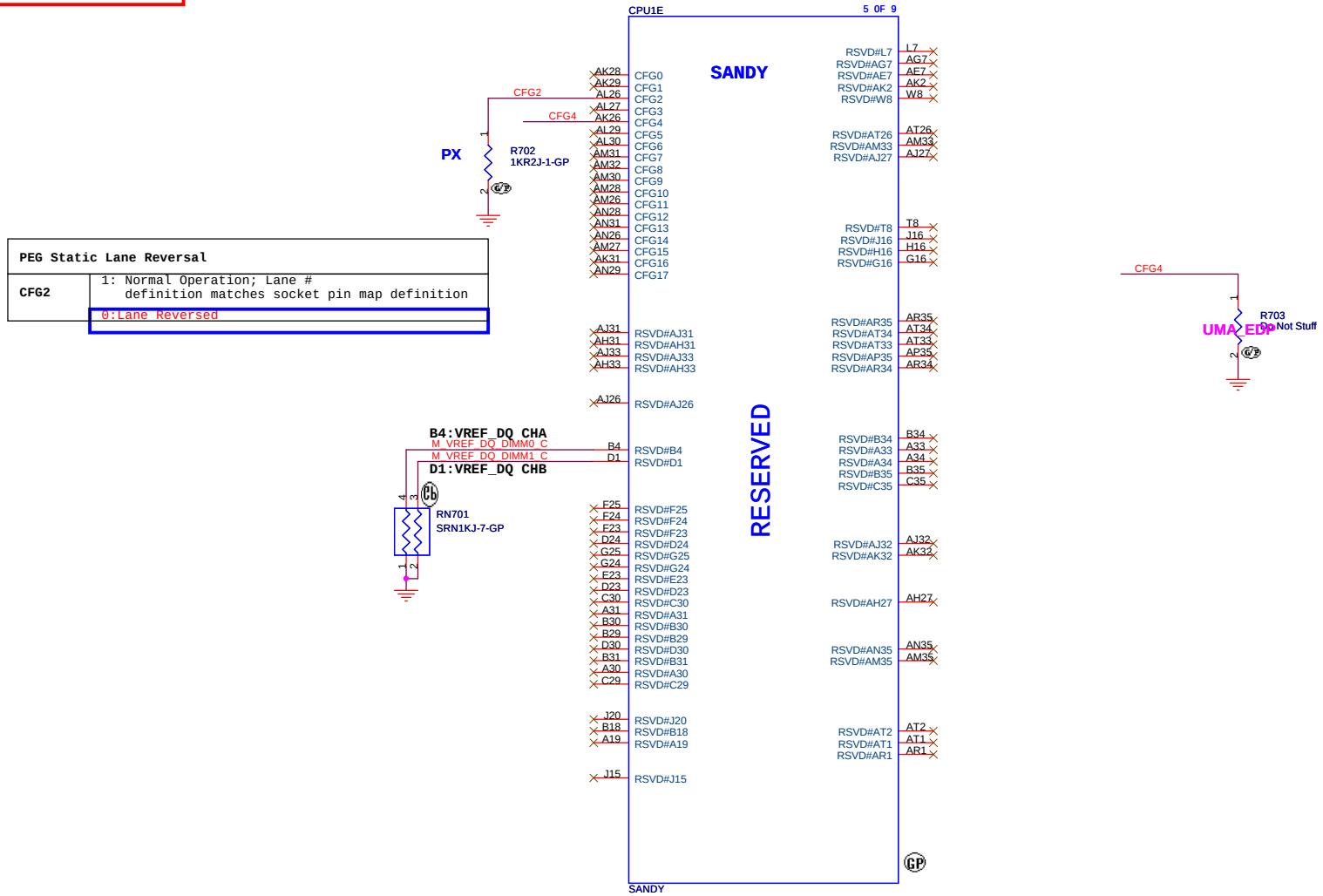
Title	***CPU (DDR)***
Size A3	Document Number **BA40-HR** Rev **SD**
Date: Thursday, April 07, 2011	Sheet 6 of 109

SSID = CPU



D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

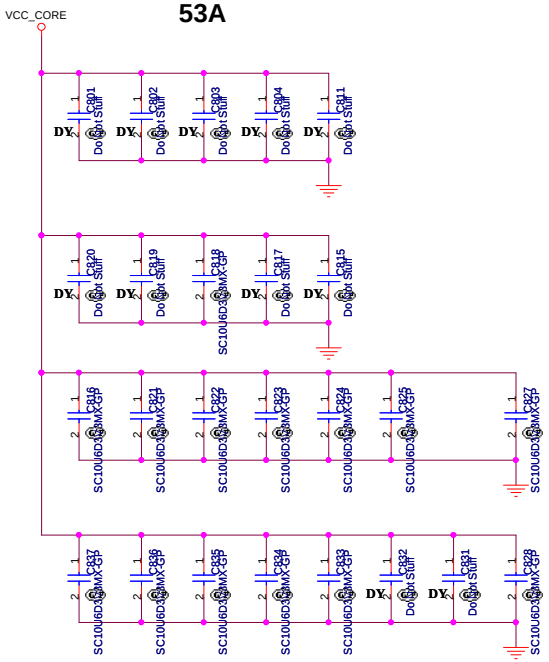
Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 7 of 109

SSID = CPU

PROCESSOR CORE POWER

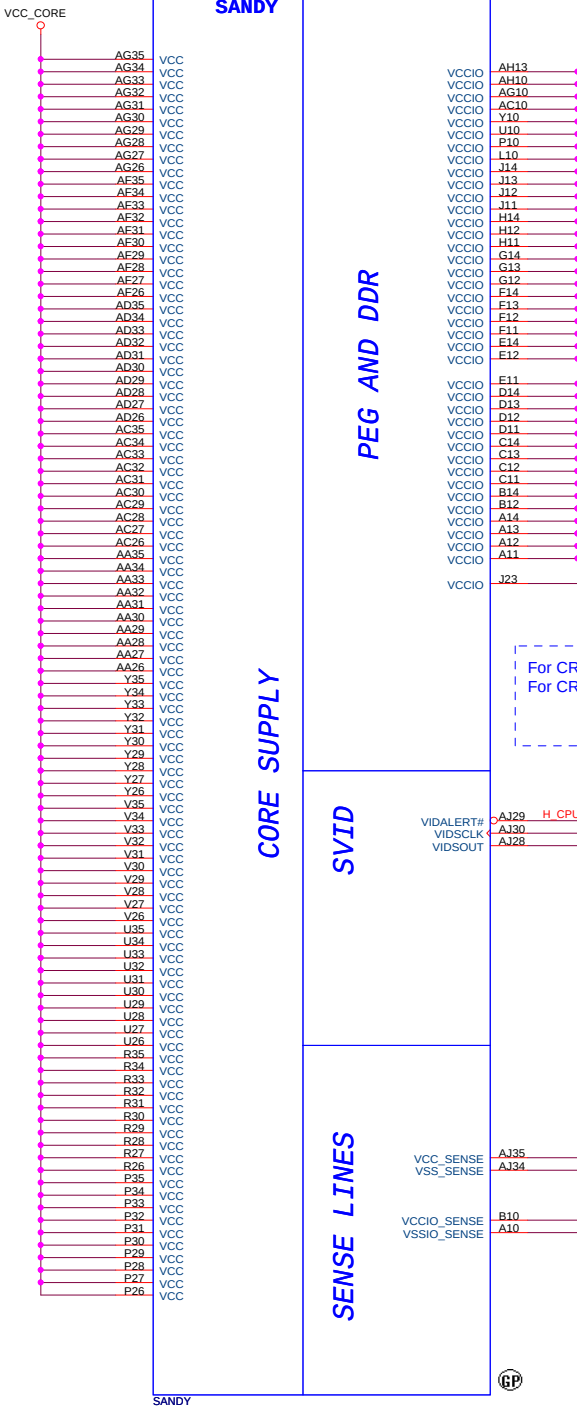
53A



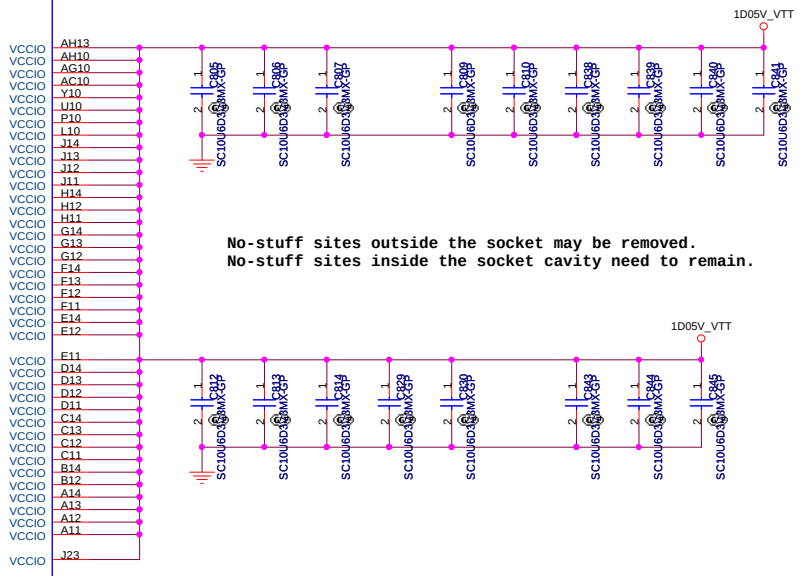
VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

POWER

CPU1F — SANDY — 6 OF 9

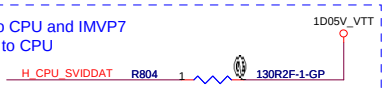


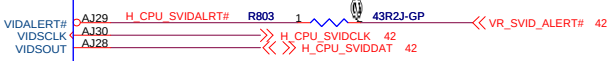
VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

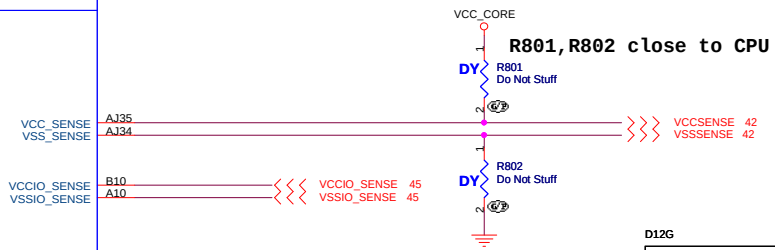


No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU







D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 8 of 109

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G 7 OF 9

SANDY

SENSE LINES
VAXG_SENSE AK35 → VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS
VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

SA RAIL
VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

1.8V RAIL
VCCPLL: B6, A6, A2

MISC
VCCSA_SENSE H23 → VCCUSA_SENSE
FC_C22 C22, C24 → H_FC_C22
VCCSA_VID1 → VCCSA_SEL 48

GRAPHICS
VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

+VCC_GFXCORE
R906 DY Do Not Stuff
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 DY Do Not Stuff

PROCESSOR VAXG: 24A

+VCC_GFXCORE
C901 DY Do Not Stuff
C902 SC10U6D3MX-L-GP
C903 SC10U6D3MX-L-GP
C904 SC10U6D3MX-L-GP
C905 SC10U6D3MX-L-GP
C906 DY Do Not Stuff
C907 DY Do Not Stuff
C908 SC10U6D3MX-L-GP
C918 DY Do Not Stuff
C919 SC10U6D3MX-L-GP
C920 SC10U6D3MX-L-GP
C921 SC10U6D3MX-L-GP
UMA_PX_Muxless

PROCESSOR VDDQ: 10A

1D5V_S0
C909 DY Do Not Stuff
C910 SC10U6D3MX-L-GP
C911 SC10U6D3MX-L-GP
C912 SC10U6D3MX-L-GP
C913 SC10U6D3MX-L-GP
C914 DY Do Not Stuff

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

PROCESSOR VCCSA: 6A

0D85V_S0
C916 DY Do Not Stuff
C915 SC10U6D3MX-L-GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 10R2J-2-GP
R902 need be close to pin H23.
TP901 Do Not Stuff

+VCC_GFXCORE
R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0
PROCESSOR VCCPLL: 1.2A
C322 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

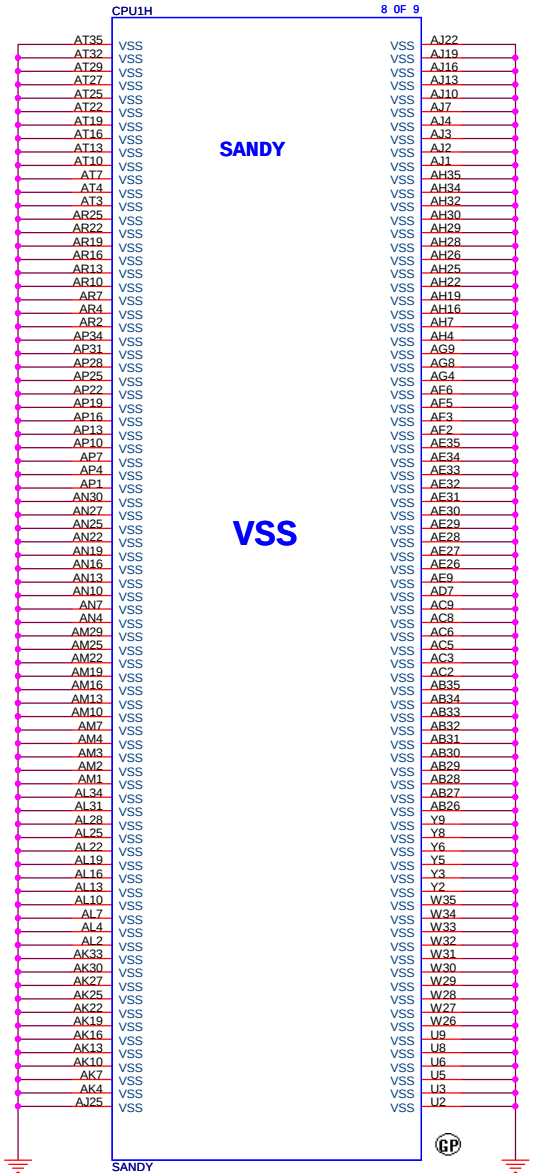
RN901 SRN1KJ-7-GP

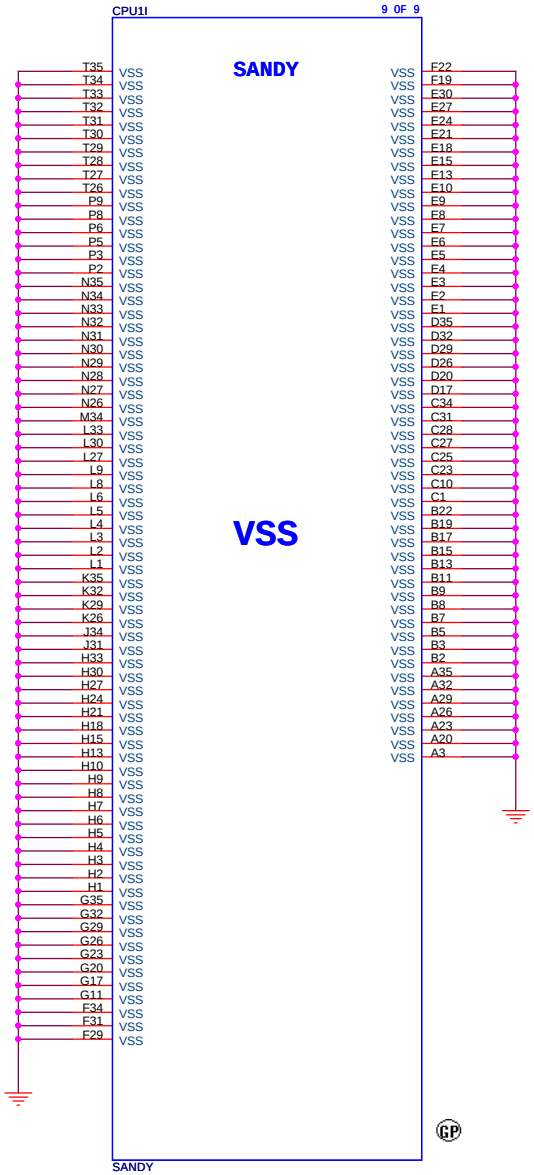
D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 9 of 109

SSID = CPU





D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 10 of 109

JE40 delete XDP function

D12G

緯創資通 **Wistron Corporation**
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Title: ***XDP***

Size	Document Number	Rev
A3	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 11 of 109

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 12 of 109

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D12G

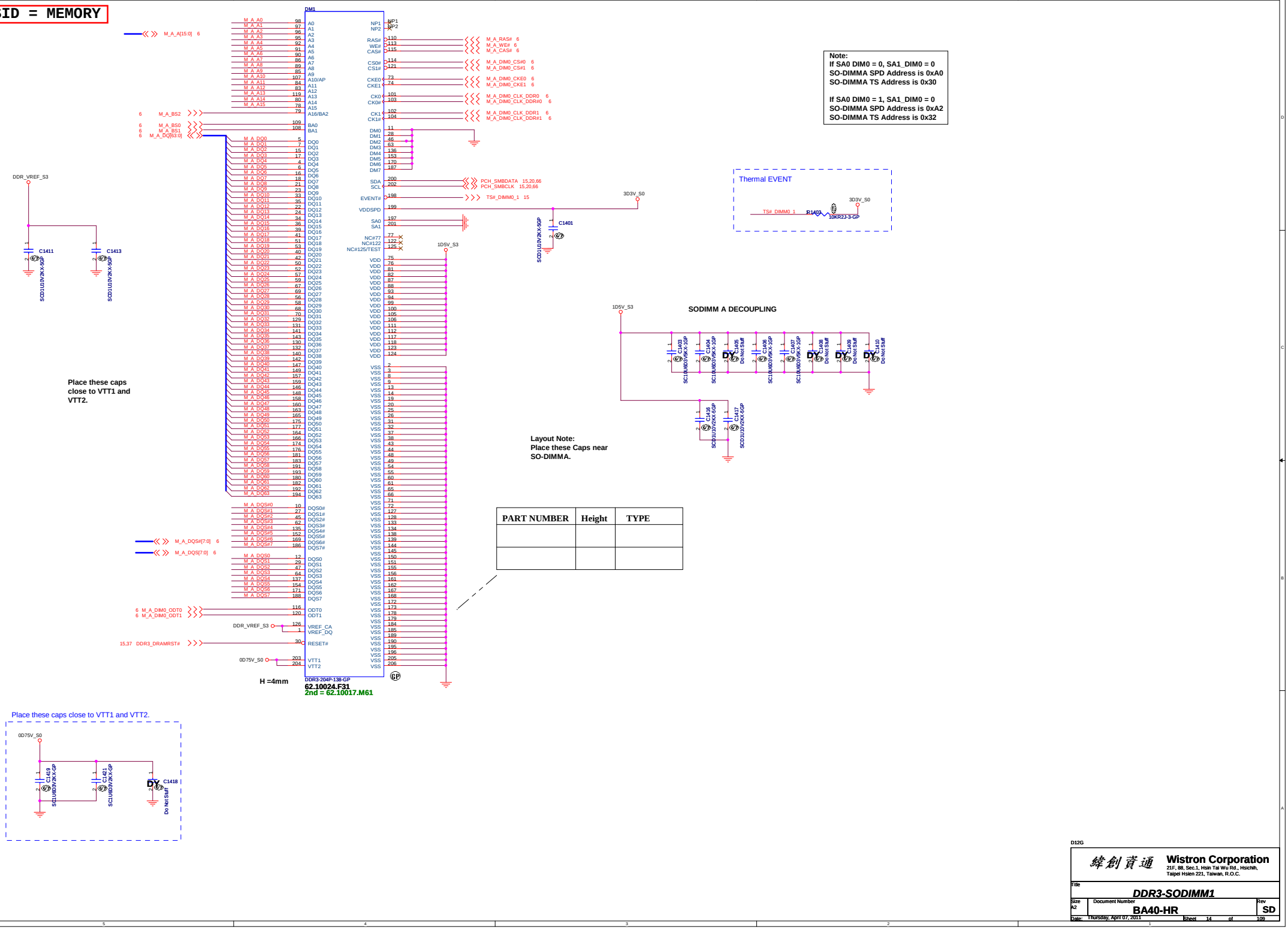
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 13 of 109

SSID = MEMORY



PART NUMBER	Height	TYPE

D12G

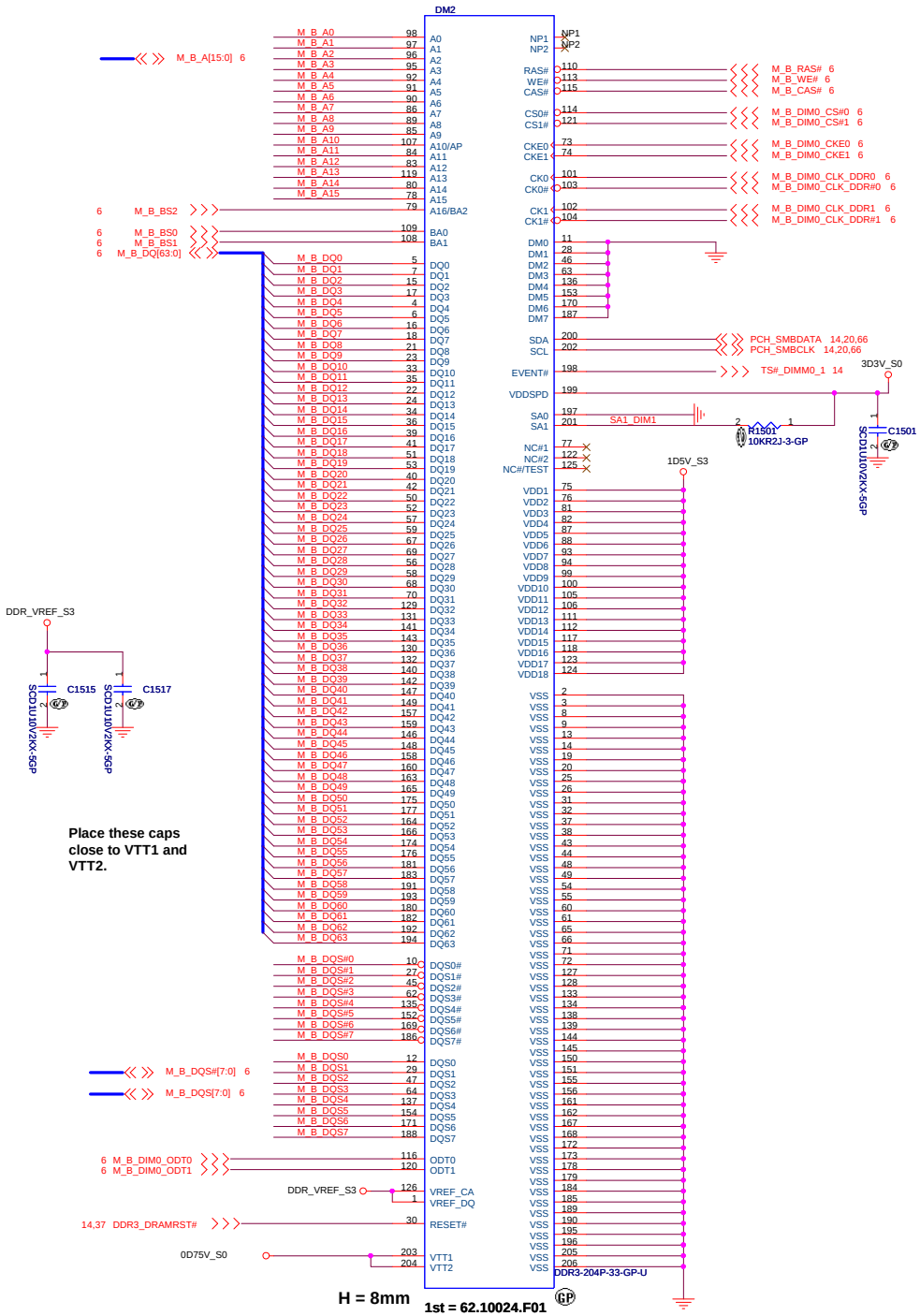
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size: A2 | Document Number: **BA40-HR** | Rev: **SD**

Date: Thursday, April 07, 2011 | Sheet 14 of 109

SSID = MEMORY



DDR_VREF_S3

C1515 SCD1U10V2KX-5GP

C1517 SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

H = 8mm

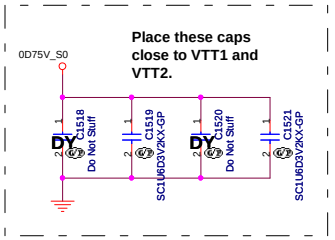
1st = 62.10024.F01

2nd = 62.10017.M71

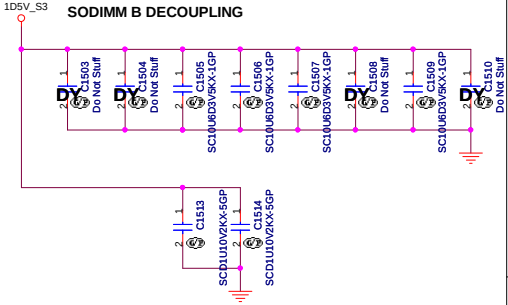
Due to strange symbol of 62.10024.F01,
we use 62.10017.M31 symbol. (62.10017.M31 was deleted by connector list)

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Place these caps close to VTT1 and VTT2.



Layout Note:
Place these Caps near SO-DIMMB.

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 15 of 109

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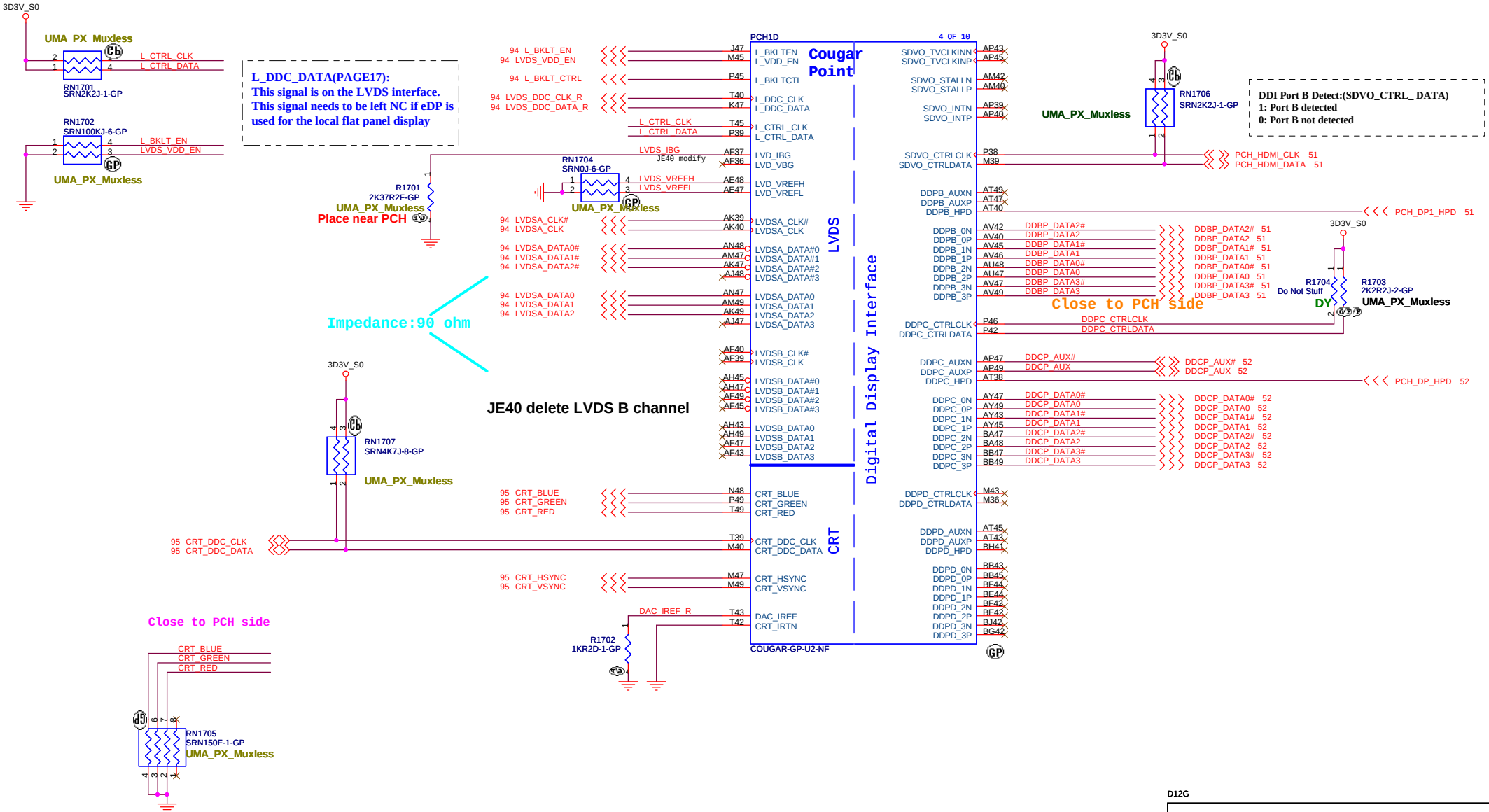
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 16 of 109



D12G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (LVDS/CRT/DDI)	
Size: A3	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 17 of 109	

SSID = PCH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE 1 R1809 1KR2J-1-GP H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

RN1801 SRN8K2J-2-GP-U
INT_PIRQH# 1
INT_PIRQB# 2
INT_PIRQF# 3
INT_PIRQA# 4
3D3V_S0 5
10 3D3V_S0
9 INT_PIRQD#
8 INT_PIRQE#
7 INT_PIRQC#
6 USB30_SMI#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803 SRN10K-5-GP
DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4

PCH1E 5 OF 10
Cougar Point
RSVD
NVRAM
PCI
USB
COUGAR-GP-U2-NF

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	3G Card
1	USB port1(SATA Combo),on M/B
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	Dock
6	X
7	X
8	USB port4 on S/B(usb charger)
9	USB port 2 on S/B
10	USB port 3 (only when 3.0 not support)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

3D3V_S0
R1814 8K2R2J-3-GP
INT_PIRQA# K40 PIRQA#
INT_PIRQB# K38 PIRQB#
INT_PIRQC# H38 PIRQC#
INT_PIRQD# G38 PIRQD#
83 DGPU_HOLD_RST# C46 REQ1#/GPIO50
94,95,103 DGPU_SELECT# C44 REQ2#/GPIO52
93 DGPU_PWR_EN# E40 REQ3#/GPIO54
94 DGPU_PWM_SELECT# D47 GNT1#/GPIO51
F42 GNT2#/GPIO53
F46 GNT3#/GPIO55
R1813 Do Not Stuff
56 SATA_ODD_DA# G42 PIRQE#/GPIO2
35 USB30_SMI# G40 PIRQF#/GPIO3
C42 PIRQG#/GPIO4
D44 PIRQH#/GPIO5
K10 PME#
5,27,31,32,35,36,65,66,71,75,82,83,97,105,108 PLT_RST# C6 PLTRST#
71 CLK_PCI_LPC R1804 22R2J-2-GP CLK_PCI_LPC_R H49 CLKOUT_PCI0
20 CLK_PCI_FB R1805 22R2J-2-GP CLK_PCI_FB_R H43 CLKOUT_PCI1
27,82 CLK_PCI_KBC R1806 22R2J-2-GP CLK_PCI_KBC_R J48 CLKOUT_PCI2
K42 CLKOUT_PCI3
H40 CLKOUT_PCI4

EC1803 EC1802 EC1801 DY Do Not Stuff
EMI request 20101109

-1_0303

USBP0N C24 USB_PN0 66
USBP0P A24 USB_PP0 66
USBP1N C25 USB_PN1 57
USBP1P B25 USB_PP1 57
USBP2N C26 USB_PN2 69
USBP2P A26 USB_PP2 69
USBP3N K28 USB_PN3 63
USBP3P H28 USB_PP3 63
USBP4N E28 USB_PN4 66
USBP4P D28 USB_PP4 66
USBP5N C28 USB_PN5 104
USBP5P A28 USB_PP5 104
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
USBP8N L30 USB_PN8 107
USBP8P K30 USB_PP8 107
USBP9N G30 USB_PN9 82
USBP9P E30 USB_PP9 82
USBP10N C30 USB_PN10 82
USBP10P A30 USB_PP10 82
USBP11N L32 USB_PN11 65
USBP11P K32 USB_PP11 65
USBP12N G32 USB_PN12 49
USBP12P E32 USB_PP12 49
USBP13N C32 USB_PN13 108
USBP13P A32 USB_PP13 108
USBRBIAS# C33 USB_RBIAS R1811 22D6R2F-L1-GP
USBRBIAS B33
3D3V_S5
R1820 10KR2J-3-GP
OC0#/GPIO59 A14
OC1#/GPIO40 K20
OC2#/GPIO41 B17
OC3#/GPIO42 C16
OC4#/GPIO43 L16
OC5#/GPIO9 A16
OC6#/GPIO10 D14
OC7#/GPIO14 C14

-1_0317

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

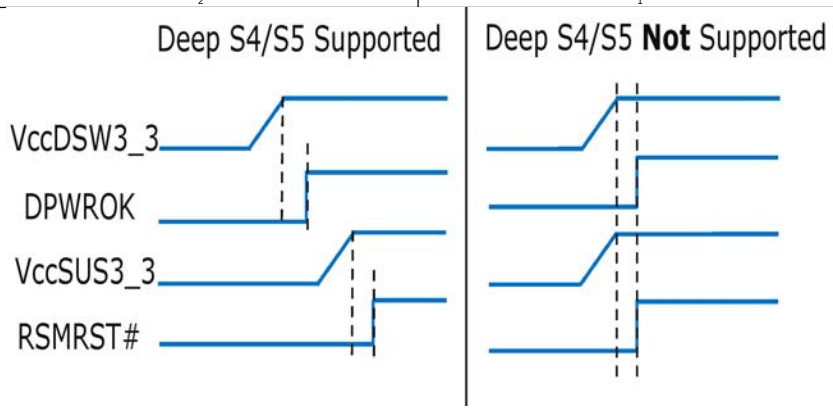
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 18 of 109

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10 — Cougar Point — COUGAR-GP-U2-NF

DMI: DMI0RXN BC24, DMI1RXN BE20, DMI2RXN BG18, DMI3RXN BG20; DMI0RXP BE24, DMI1RXP BC20, DMI2RXP BJ18, DMI3RXP BJ20; DMI0TXN AW24, DMI1TXN AW20, DMI2TXN BB18, DMI3TXN AV18; DMI0TXP AY24, DMI1TXP AY20, DMI2TXP AY18, DMI3TXP AU18

FDI: FDI_RXN0 BJ14, FDI_RXN1 AY14, FDI_RXN2 BE14, FDI_RXN3 BH13, FDI_RXN4 BC12, FDI_RXN5 BJ12, FDI_RXN6 BG10, FDI_RXN7 BG9; FDI_RXP0 BG14, FDI_RXP1 BB14, FDI_RXP2 BF14, FDI_RXP3 BG13, FDI_RXP4 BE12, FDI_RXP5 BG12, FDI_RXP6 BJ10, FDI_RXP7 BH9; FDI_INT AW16; FDI_FSYNC0 AV12; FDI_FSYNC1 BC10; FDI_LSYNC0 AV14; FDI_LSYNC1 BB10

1D05V_VTT
R1901 1 49D9R2F-GP DMI_COMP_R — DMI_ZCOMP BJ24
R1902 1 750R2F-GP RBIAS_CPY — DMI_IRCOMP BG25; DMI2RBIAS BH21

R1926 Do Not Stuff DY
R1904 100KR2J-1-GP
SYS_PWROK — PWROK
0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.

JE40 modify SUS_PWR_ACK — SUSACK# C12
3D3V_S0 — R1905 10KR2J-3-GP — SYS_RESET# K3
36 SYS_PWROK — SYS_PWROK P12
R1924 Do Not Stuff
27,42 S0_PWR_GOOD — PWROK L22
R1930 Non iAMT
36 PM_MPWROK — R1929 Do Not Stuff — APWROK L10
5,37 PM_DRAM_PWRGD — iAMT — DRAMPWROK B13
PM_RSMRST# — RSMRST# C21
27 SUS_PWR_ACK — SUSWARN#/SUSPWRDNACK/GPIO30 K16
27,97 PM_PWRBTN# — PWRBTN# E20
27 AC_PRESENT — ACPRESENT/GPIO31 H20
BATLOW# — BATLOW#/GPIO72 E10
PM_RI# — RI# A10

System Power Management

DSWVRMEN — A18 DSWODVREN
DPWROK — E22 PCH_DPWROK
R1910 Do Not Stuff
DY
R1911 Do Not Stuff
PM_RSMRST# — RTC_AUX_S5
WAKE# — B9 PCIE_WAKE# 31,35,65,66,75
CLKRUN#/GPIO32 — N3 PM_CLKRUN# 27
SUS_STAT#/GPIO61 — G8
SUSCLK/GPIO62 — N14 PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 — D10 PM_SLP_S5# — AFTP14
SLP_S4# — H4 PM_SLP_S4# 27,46
SLP_S3# — F4 PM_SLP_S3# 27,29,36,37,47,75,92
R1928 DY Do Not Stuff
SLP_A# — G10 SLP_A# — R1927 Do Not Stuff — PM_SLP_A# 27,36
iAMT
SLP_SUS# — G16
PMSYNCH — AP14 H_PM_SYNC 5
SLP_LAN#/GPIO29 — K14 — R1931 Do Not Stuff — PM_SLP_LAN# 27,36,45
iAMT

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 330KR2J-L1-GP
DSWODVREN — R1918 DY Do Not Stuff

R1919 8K2R2J-3-GP
3D3V_S0
PM_CLKRUN#

3D3V_S5
RN1901 SRN10KJ-6-GP
BATLOW#
PM_RI#
AC_PRESENT
SUS_PWR_ACK
R1922 Non iAMT 10KR2J-3-GP PM_SLP_LAN#
R1921 10KR2J-3-GP PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
3V_5V_POK_#
PM_RSMRST# — R1912 1KR2J-1-GP — RSMRST#_KBC 27
Q1901 2N7002KDW-GP
3V_5V_POK 41
84.2N702.A3F
2nd = 84.DM601.03F

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP — PM_RSMRST#

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

D12G

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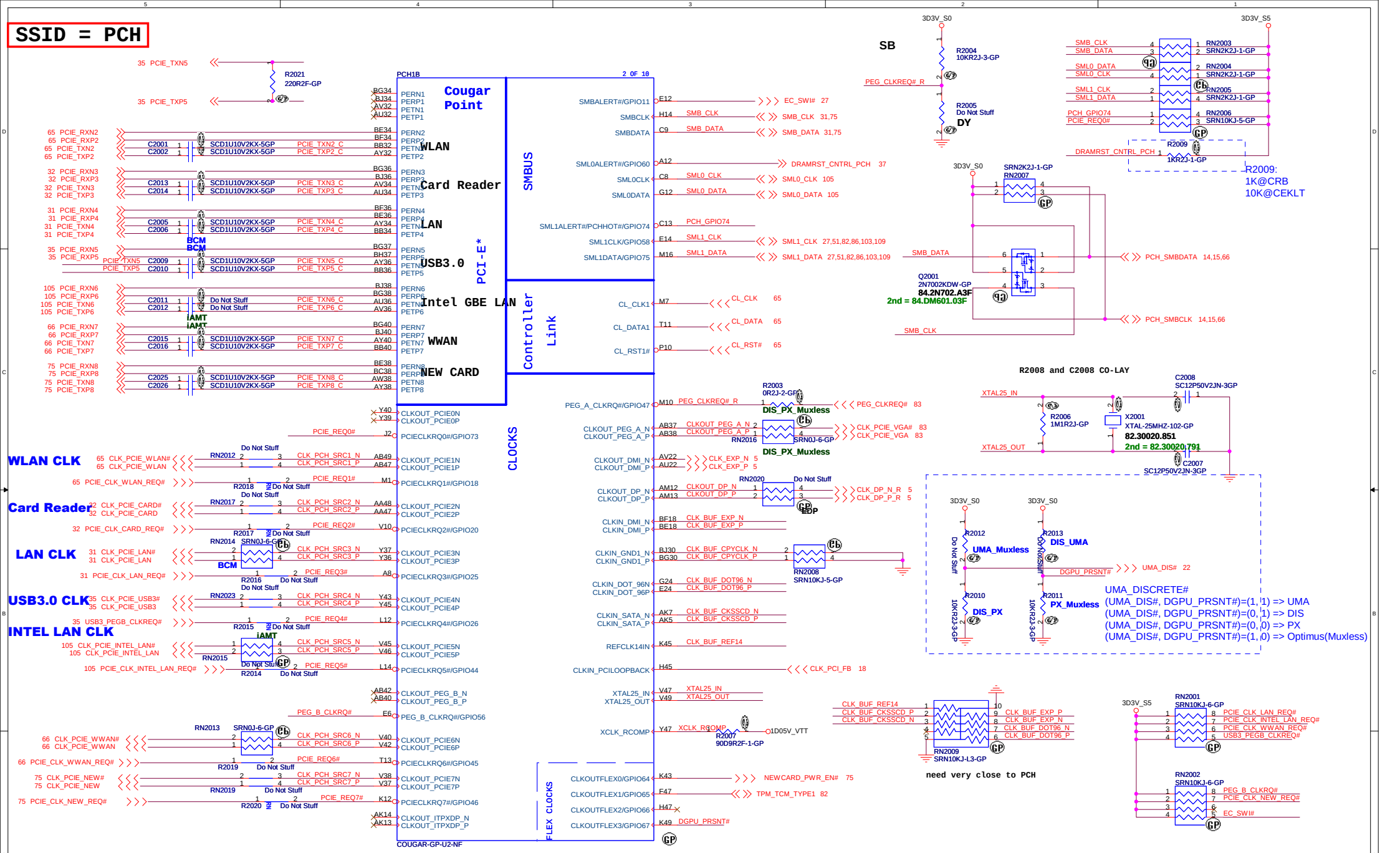
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 19 of 109

SSID = PCH



D12G

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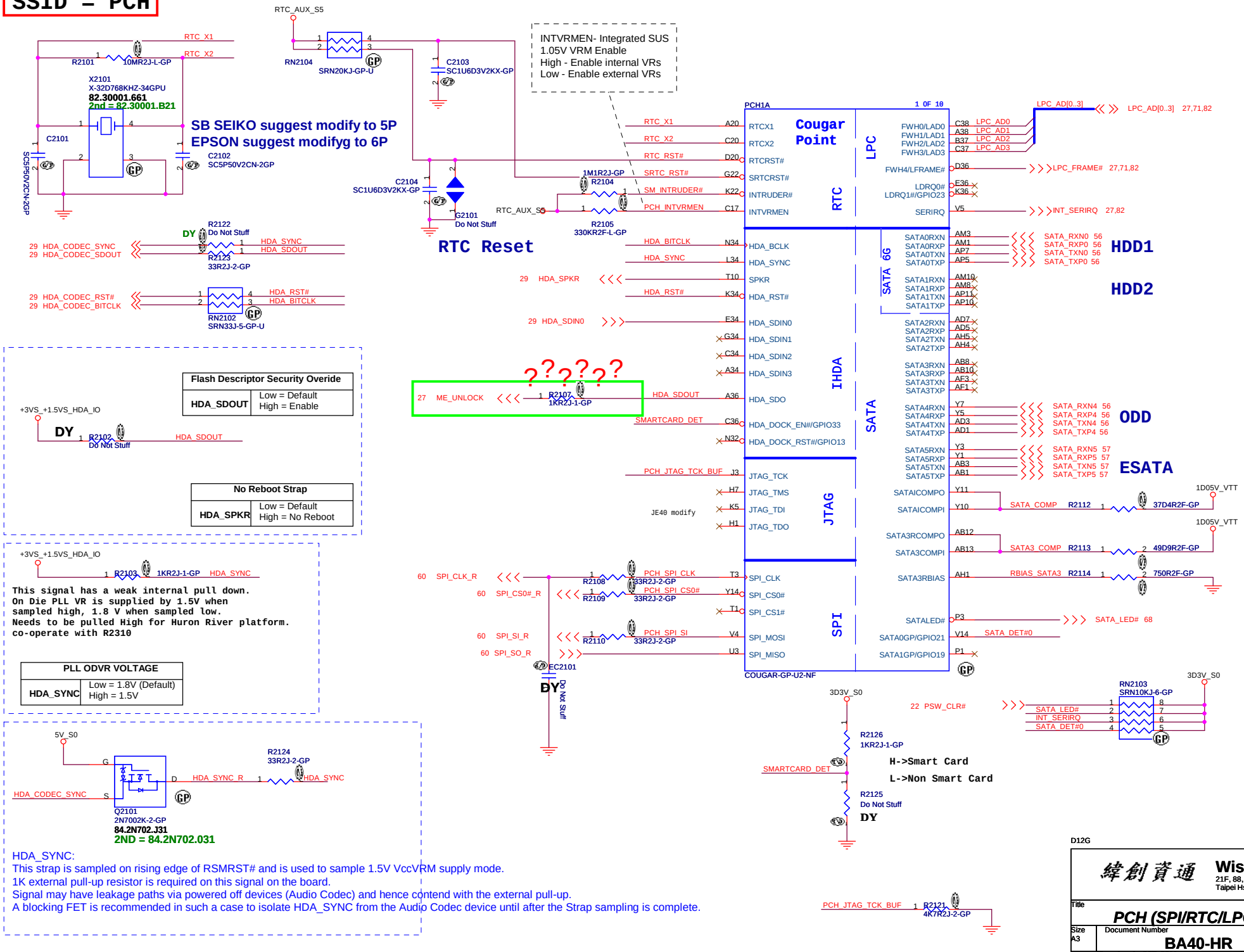
Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 20 of 109

SSID = PCH



D12G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 21 of 109

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

PassWord Clear

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

VRAM Frequency
PCH_GPIO22=1 : 800MHZ
PCH_GPIO22=0 : 900MHZ

VRAM Size

D12G

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Title: PCH (GPIO/CPU)
Size: A3 | Document Number: BA40-HR | Rev: SD
Date: Thursday, April 07, 2011 | Sheet 22 of 109

SSID = PCH 6A

POWER

PCH1G — Cougar Point — 7 OF 10 — COUGAR-GP-U2-NF

VCC CORE

1D05V_VTT — 1.3A — (1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP
C2302 SC1U6D3V2KX-GP
C2303 SC1U6D3V2KX-GP
C2304 SC1U6D3V2KX-GP

AA23 AC23 AD21 AD23 AF21 AF23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 — VCCCORE

CRT

VCCADAC — U48 +VCCA_DAC_1_2

(0.1uF/0.01uF x1) (10uF x1_0603)

C2313 SCD01U16V2KX-3GP
C2314 SCD01U16V2KX-5GP DY
C2315 Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

R2315 0R5J-5 UMA_PX_Muxless

3D3V_DAC_S0

VSSADAC — U47

LVDS

VCCALVDS — AK36 +3VS_VCCA_LVDS

0.001A

R2304 0R3J-0-U-GP UMA_PX_Muxless

3D3V_S0

VSSALVDS — AK37

R2303 Do Not Stuff DIS

U2301 for ANNIE flicker issue
R2312 for don't flicker solution

VCCTX_LVDS — AM37 AM38 AP36 AP37 — +1.8VS_VCCTX_LVDS

0.06A

R2309 Do Not Stuff DIS
C2316 SCD01U16V2KX-3GP
C2317 SCD01U16V2KX-3GP
C2318 Do Not Stuff DY

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

R2305 0R5J-5 UMA_PX_Muxless

1D8V_S0

(0.01uF x2) (22uF x1)

3.3V CRT LDO

U2301 G9091-330T11U-GP 74.09091.J3F

5V_S0 — C2311 SC1U10V2KX-1GP

VIN GND EN VOUT NC#4

UMA_PX_Muxless
2nd = 74.70233.031 UMA_PX_Muxless

3D3V_DAC_S0 — C2312 SC1U6D3V2KX-GP — C2327 SC1U6D3V3MX-GP

SB add C2327

UMA_PX_Muxless

HVCMOS

JE40 modify 07/16

1D05V_VTT — AN19 — VCCIO

1D05V_VTT — 2.925A(Total current of VCCIO)

BJ22 — VCCAPLLEXP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 — VCCIO

DY C2306 Do Not Stuff
C2307 SC1U6D3V2KX-GP
C2308 SC1U6D3V2KX-GP
C2309 SC1U6D3V2KX-GP

(1uF x4)

VCC3_3 — V33 V34

(0.1uFx1)

3D3V_S0

C2319 SCD1U10V2KX-5GP

DMI

VCCVRM — AT16 — VCCVRM

1D05V_VTT

VCCDMI — AT20 — JE40 modify

(1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI — AB36

0.266A (Totally VCC3_3 current)

3D3V_S0

(0.1uF x1)

C2310 SCD1U10V2KX-5GP

BH29 — VCC3_3

0.02A

L2303 0R3J-0-U-GP

1D05V_VTT

(1uFx1) (10uFx1)

C2321 SCD1U10V2KX-5GP
C2325 Do Not Stuff DY

NAND / SPI

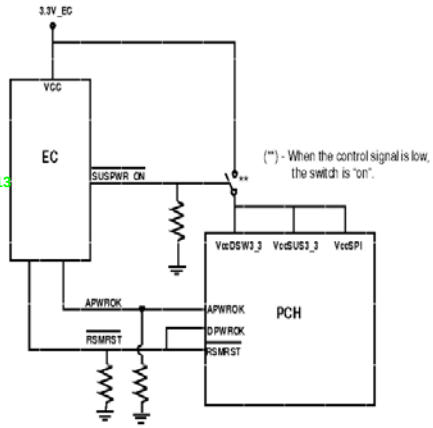
VccDFTERM — AG16 AG17 AJ16 AJ17

1D8V_S0

0.19A JE40 modify

C2326 SCD1U10V2KX-5GP
C2322 SCD1U10V2KX-5GP

Refer to NPCE795 shared SPI flash architecture



VCCVRM — R2316 0R3J-0-U-GP — 1D5V_S0
1D8V_S0 — R2317 DY Do Not Stuff

VCCVRM — AP16 — VCCVRM

0.159A(Totally current of VCCVRM)

BG6 — VCCAFDIPLL

0806 check VCCAFDIPLL

1D05V_VTT — AP17 — VCCIO

1D05V_VTT — AU20 — VCCDMI

0.042A (Totally current of VCCDMI)

FDI

VCCSPI — V1

0.02A (1uFx1)

3D3V_S5

C2323 SC1U6D3V2KX-GP

SB 公板suggest delete 3D3V_S0, R2313
SPI only support 3D3V_S5

The same BIOS SPI ROM power

D12G

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Title: PCH (POWER1)

Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 23 of 109

SSID = PCH

POWER

PCH1J — Cougar Point — 10 OF 10

Clock and Miscellaneous

- TP17 Do Not Stuff — AD49 VCCACLK
- 3D3V_S5 — 0.002A — T16 VCCDSW3_3 — (0.1uFx1)
- V12 DCPSUSBYP — (10uFx1) (1uFx1)
- 3D3V_S0 — C2402 SC1U10V2KX-1GP — T38 VCC3_3
- TP19 Do Not Stuff — BH23 VCCAPLLDMI2
- 1D05V_VTT — (10uFx1) — AL29 VCCIO
- AL24 DCPSUS
- 1D05V_M — 1.01A (Total current of VCCASW) — AA19 AA21 AA24 AA26 AA27 AA29 AA31 AC26 AC27 AC29 AC31 AD29 AD31 W21 W23 W24 W26 W29 W31 W33 VCCASW
- C2403 C2404 C2406 C2407 C2408 — SC1U6D3V2KX-GP / SC1U6D3V5KX-1GP — DY Do Not Stuff — (22uFx2_0603) (1uFx3)
- +VCCRTCEXT — C2411 SCD1U10V2KX-5GP (0.1uFx1) — N16 DCPRTC
- 0.16A (Totally current of VCCVRM) — VCCVRM — Y49 VCCVRM
- +1.05VS_VCCA_A_DPL — BD47 VCCADPLLA
- +1.05VS_VCCA_B_DPL — BF47 VCCADPLLB
- JE40 modify 07/16 — 1D05V_VTT — C2412 SC1U6D3V2KX-GP JE40 modify (1uFx1) — AF17 VCCIO
- 1D05V_VTT (1uFx1) — 0.055A — C2414 SC1U6D3V2KX-GP — AF33 AF34 AG34 VCCDIFFCLKN
- 1D05V_VTT — C2413 SC1U6D3V2KX-GP JE40 modify (1uFx1) — 0.095A — AG33 VCCSSC
- +VCCSST (0.1uFx1) — C2415 SCD1U10V2KX-5GP — V16 DCPSST
- 1D05V_M — R2416 DY Do Not Stuff — T17 V19 DCPSUS
- C2421 DY Do Not Stuff
- 1D05V_VTT — (0.1uFx2) (4.7uFx1_0603) — C2417 SC4D7U6D3V3KX-GP — C2418 SCD1U10V2KX-5GP — DY C2419 Do Not Stuff — BJ8 V_PROC_IO — A22 VCCRTC
- RTC_AUX_S5 — 6uA — (0.1uFx2) (1uFx1) — DY C2420 Do Not Stuff
- COUGAR-GP-U2-NF

USB

- 0.097A (Totally current of VCCSUS3_3) — N26 P26 P28 T27 T29 VCCIO
- 1D05V_VTT — (1uFx1) — C2423 SC1U6D3V2KX-GP
- 3D3V_S5 — (0.1uFx1) — C2424 SCD1U10V2KX-5GP — T23 T24 V23 V24 P24 VCCSUS3_3
- 3D3V_S5 — (0.1uFx1) — C2425 SCD1U10V2KX-5GP — T26 VCCIO
- 1D05V_VTT
- 0.001A — +5VA_PCH_VCC5REFSUS — M26 V5REF_SUS
- TP21 Do Not Stuff — AN23 DCPSUS
- 3D3V_S5 — JE40 modify — AN24 VCCSUS3_3

PCI/GPIO/LPC

- +5VS_PCH_VCC5REF — 0.001A — P34 V5REF
- 3D3V_S5 — JE40 modify (1uFx1) — C2428 SC1U6D3V2KX-GP — JE40 modify 07/16 — N20 N22 P20 P22 VCCSUS3_3
- 3D3V_S0 — (0.1uFx2) — C2430 SCD1U10V2KX-5GP — C2431 SCD1U10V2KX-5GP — AA16 W16 T34 VCC3_3
- 3D3V_S0 — (0.1uFx1) — C2429 SCD1U10V2KX-5GP — AJ2 VCC3_3
- 1D05V_VTT — (1uFx1) — C2432 SCD1U10V2KX-5GP — AF13 AH13 AH14 AF14 VCCIO
- TP27 Do Not Stuff — AK1 VCCAPLLSATA
- AF11 VCCVRM — VCCVRM

SATA

- AC16 AC17 AD17 VCCIO
- 1D05V_VTT — JE40 modify (1uFx1) — C2435 SC1U6D3V2KX-GP — JE40 modify 07/16
- 1D05V_M — T21 V21 T19 VCCASW
- +3VS_+1.5VS_HDA_IO — 0.01A — (0.1uFx1) — C2433 SCD1U10V2KX-5GP — P32 VCCSUSHDA

MISC

CPU

RTC

HDA

- 1D05V_VTT — 0.08A (1uFx1) (220uFx1) — IND-10UH-218-GP L2402 — 68.10050.10Y 2nd = 68.10090.10B — +1.05VS_VCCA_A_DPL — C2409 SC1U6D3V2KX-GP
- 0.08A (1uFx1) (220uFx1) — IND-10UH-218-GP L2403 — 68.10050.10Y 2nd = 68.10090.10B — +1.05VS_VCCA_B_DPL — C2410 SC1U6D3V2KX-GP

- 3D3V_S5 — D2401 CH751H-40-1-GP -1_0302 83.R0304.D8F 2nd = 83.R2004.B8F — R2408 10R2J-2-GP (0.1uFx1) — C2426 SCD1U10V2KX-5GP — 5V_S5
- 3D3V_S0 — DY D2402 Do Not Stuff Do Not Stuff 2nd = 83.R2004.B8F — R2407 10R2J-2-GP (1uFx1) — C2427 SC1U10V2KX-1GP — 5V_S0
- R2414 Do Not Stuff — DY — R2402 Do Not Stuff DY — 3D3V_S5 — 1D5V_S5
- 3D3V_S5 — U2401 G9091-150T11U-GP (VIN GND EN VOUT NC#4) — C2436 SC1U10V3Y-6GP — C2416 SC1U10V3Y-6GP — C2405 SC10U6D3V5KX-1GP — 1D5V_S5
- +3VS_+1.5VS_HDA_IO — R2409 DY Do Not Stuff — R2415 DY Do Not Stuff — R2413 0R3J-0-U-GP — 3D3V_S5 — 1D5V_S0 — 1D5V_S5

D12G

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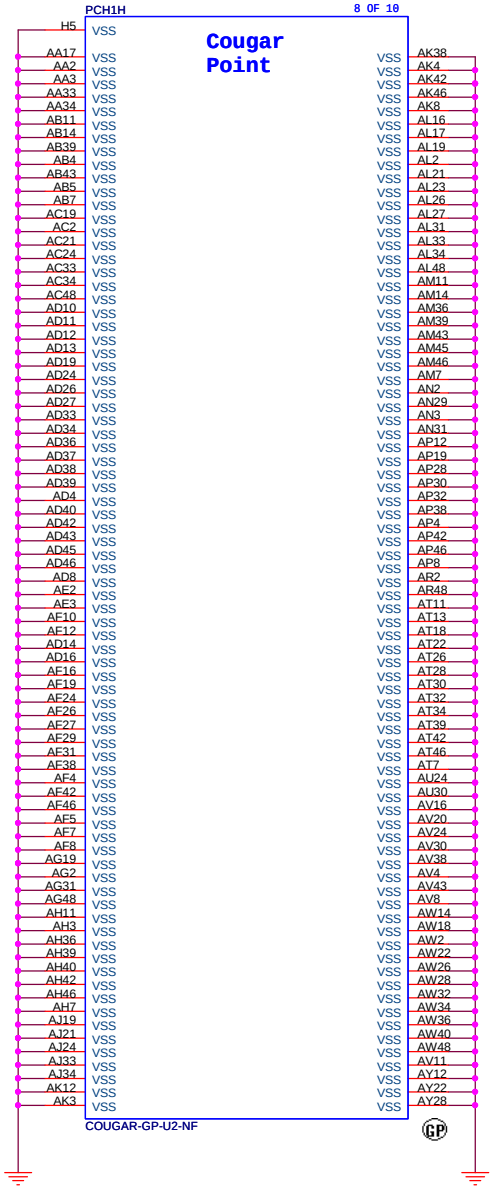
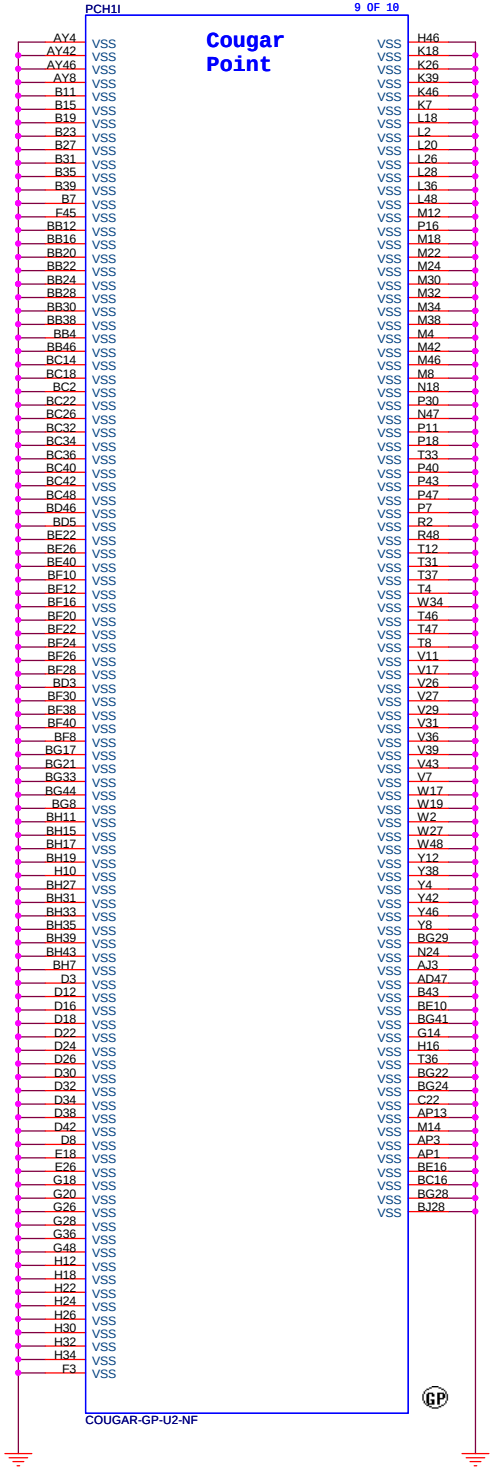
Title: PCH (POWER2)

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 24 of 109

SSID = PCH





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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 25 of 109

D12G

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Title

Clock(colay)

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 26 of 109

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

SB modify R2756 stuff, R2760 change DY

JE40 delete USB Charger function

JE40 VGA_THRM

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1

0604 Modify:
Add Pull down 100k ohm at F_SDI for Power consumption concern.

EC_GPIO47 High Active

2ND = 84.2N702.031

2nd = 84.03906.F11

Prevent BIOS data loss

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

NCT5606Y-0 (Addr: 0x32

NCT5606Y-0 (Addr: 0x30

EC_GPIO standard PH/PL

TP

BATTERY / CHARGER

PCH / EDP

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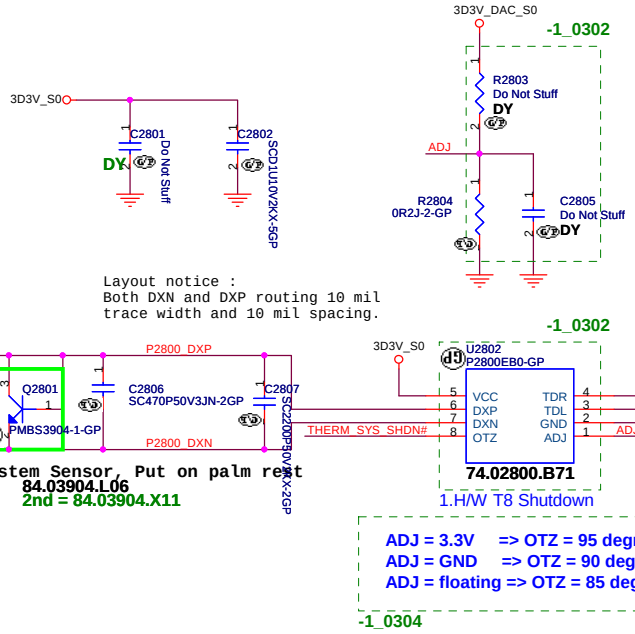
Title: KBC Nuvoton NPCE795

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 27 of 109

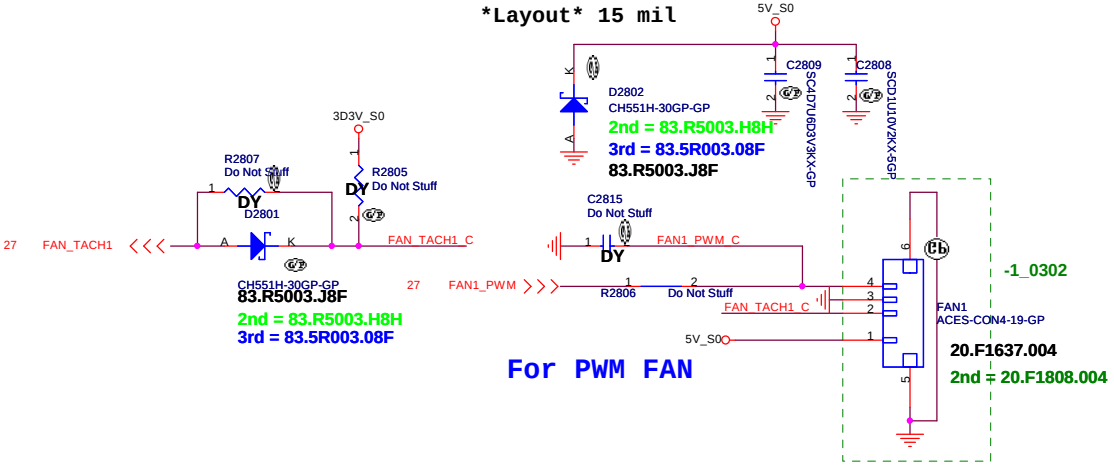
SSID = Thermal

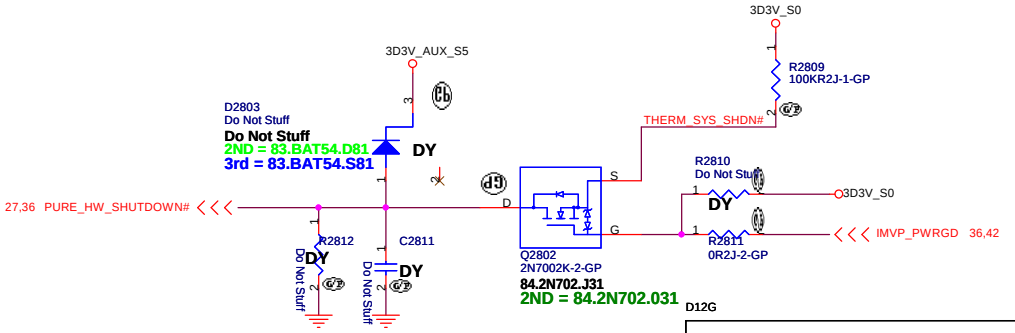
Thermal sensor P2800



Fan controller P2793

Layout 15 mil





D12G

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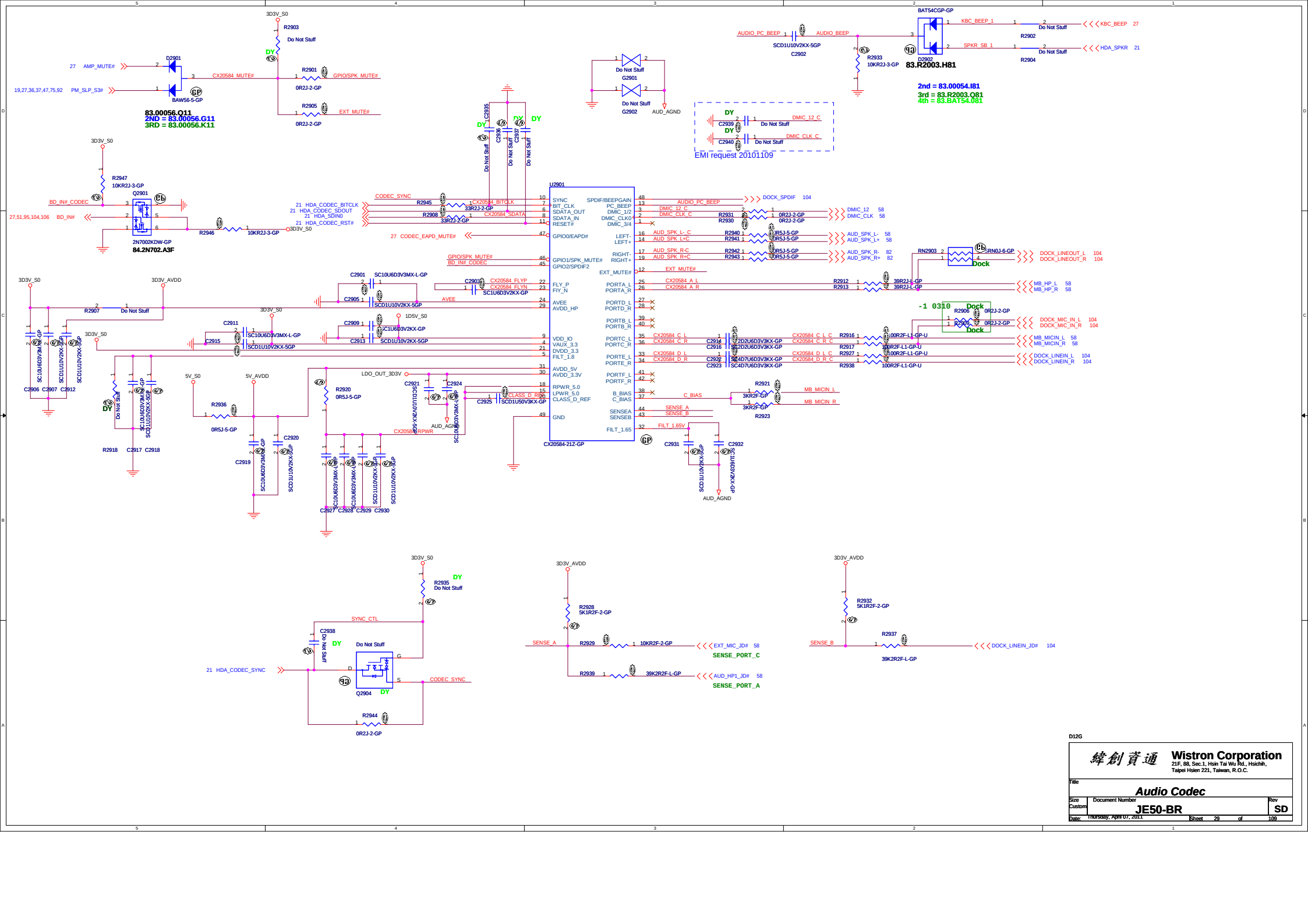
Title: Thermal P2800/Fan Controllor P2793

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 28 of 109

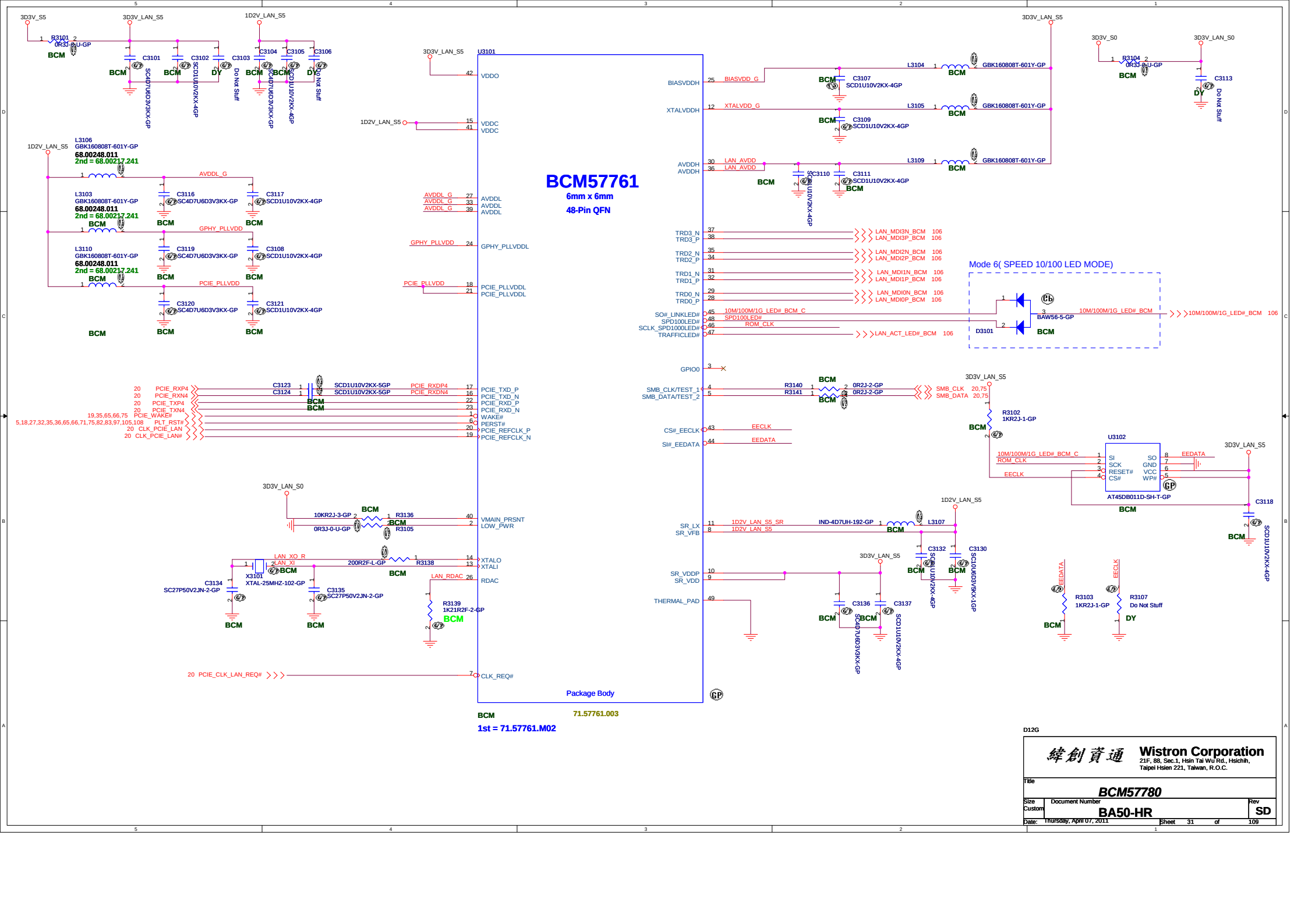

U2901
CX20584-21Z-GP
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
GPIO0/EAPD#
GPIO1/SPK_MUTE#
GPIO2/SPDIF2
EXT_MUTE#
FLY_P
FLY_N
AVEE
AVDD_HP
VDD_IO
VAUX_3.3
DVDD_3.3
FILT_1.8
AVDD_5V
AVDD_3.3V
RPWR_5.0
LPWR_5.0
CLASS_D_REF
GND
SPDIF/BEEPGAIN
PC_BEEP
DMIC_1/2
DMIC_CLK0
DMIC_3/4
LEFT-
LEFT+
RIGHT-
RIGHT+
PORTA_L
PORTA_R
PORTD_L
PORTD_R
PORTB_L
PORTB_R
PORTC_L
PORTC_R
PORTE_L
PORTE_R
PORTF_L
PORTF_R
B_BIAS
C_BIAS
SENSEA
SENSEB
FILT_1.65
EMI request 20101109
83.00056.Q11
2ND = 83.00056.G11
3RD = 83.00056.K11
84.2N702.A3F
83.R2003.H81
2nd = 83.00054.I81
3rd = 83.R2003.Q81
4th = 83.BAT54.081
-1 0310
Dock
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec
Size
Custom
Document Number
JE50-BR
Rev
SD
Date: Thursday, April 07, 2011
Sheet 29 of 109

AUDIO OP AMPLIFIER

JE40 delete AMP function

D12G

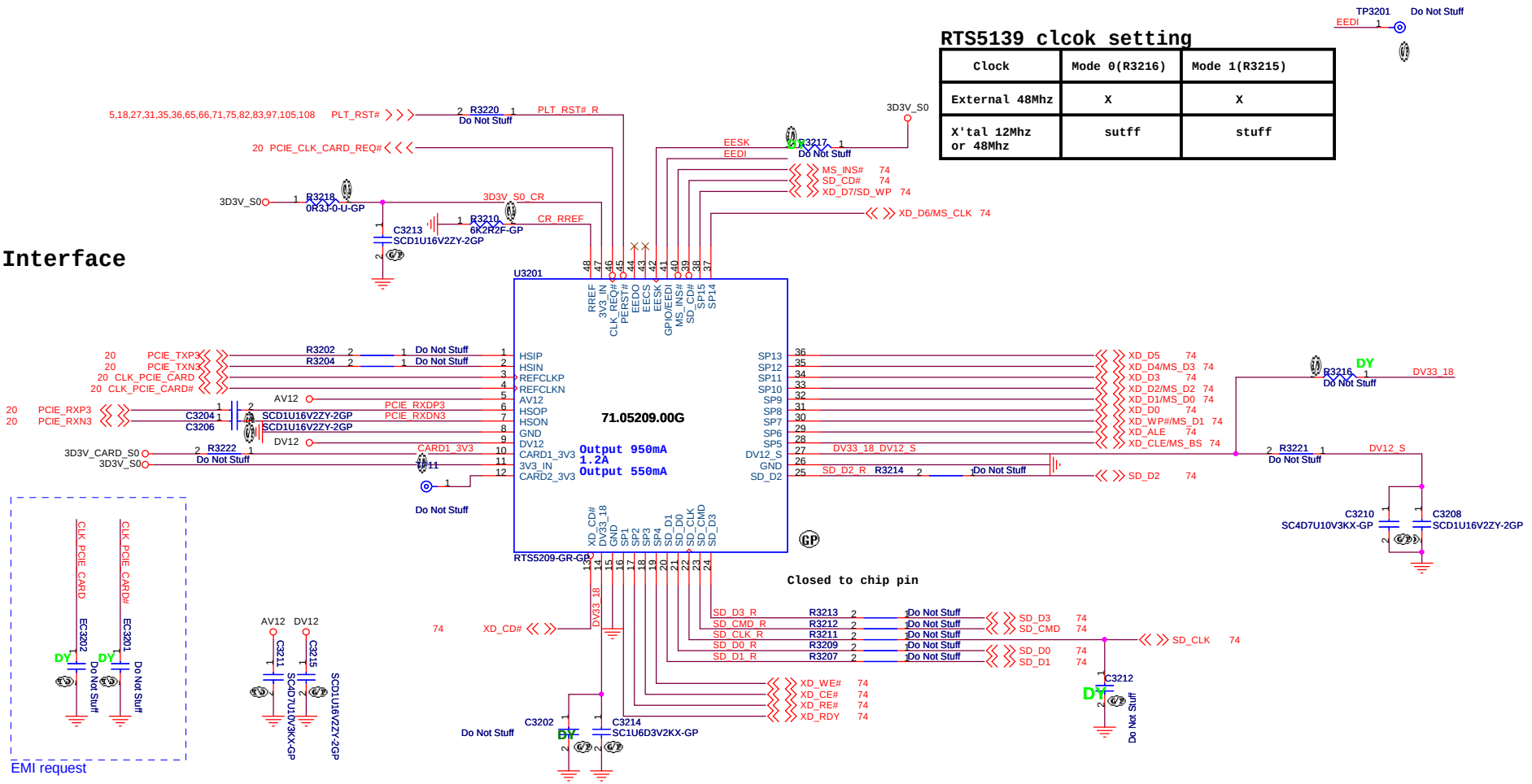
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Audio AMP***	
Size A4	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 30 of 109	


BCM57761
6mm x 6mm
48-Pin QFN
U3101
Package Body
71.57761.003
1st = 71.57761.M02
Mode 6(SPEED 10/100 LED MODE)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size
Custom
Document Number
BA50-HR
Rev
SD
Date: Thursday, April 07, 2011
Sheet 31 of 109

RTS5209==>PCI-E Interface

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	sutff	stuff



D12G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RTS5209(CARD READER)	
Size A3	Document Number BAD50-HR	Rev SD
Date: Thursday, April 07, 2011	Sheet 32 of 109	

(Blanking)

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 33 of 109

D12G

緯創資通 **Wistron Corporation**

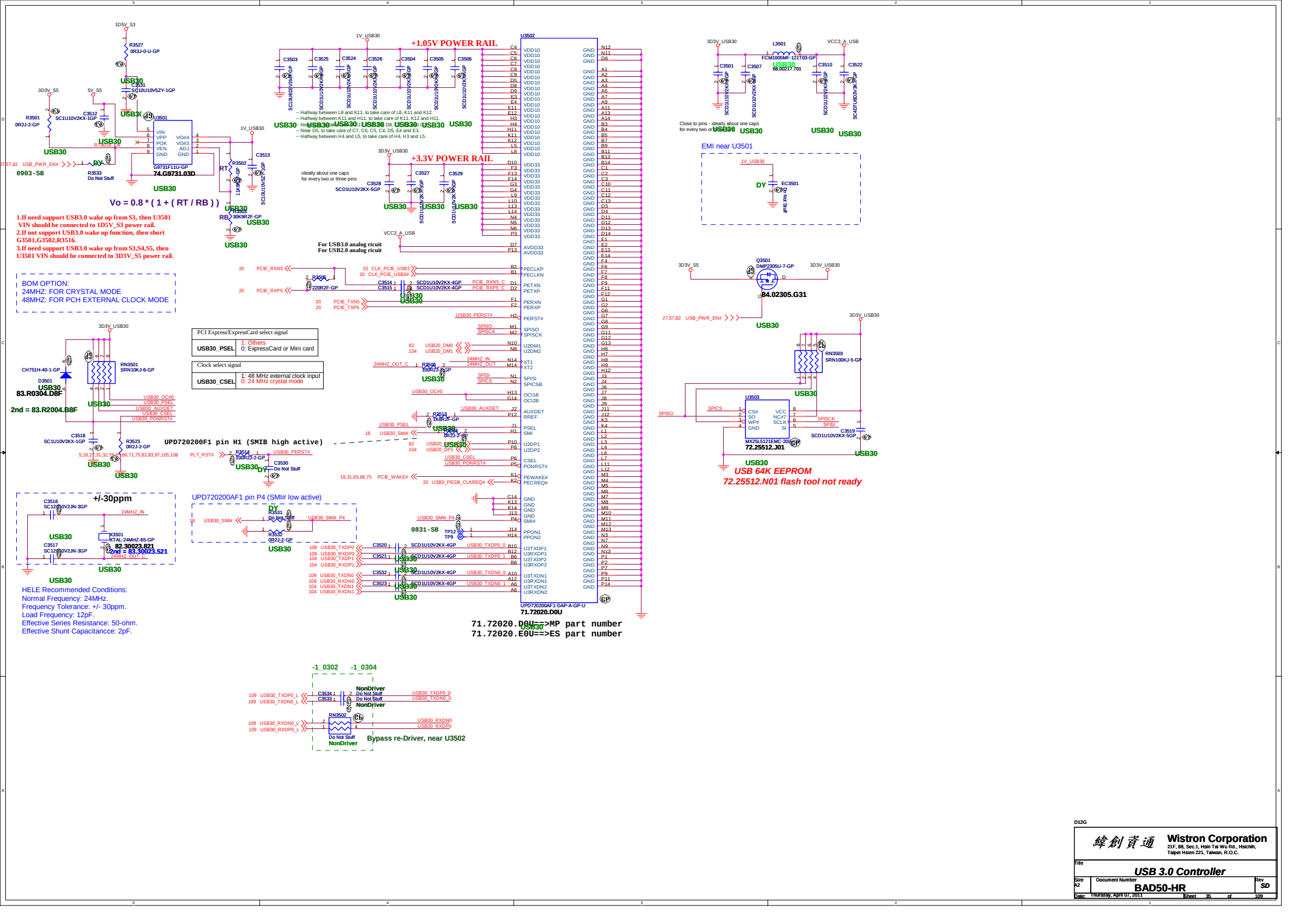
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

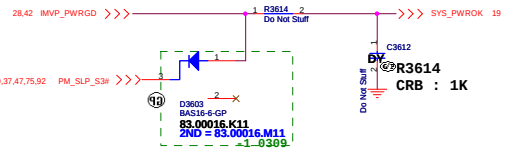
Reserved

Size	Document Number	Rev
A3	**BA40-HR**	**SD**

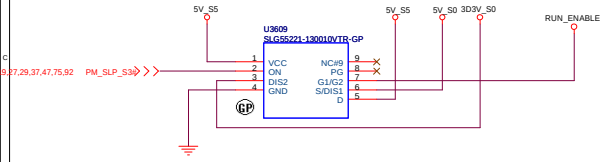
Date: Thursday, April 07, 2011 Sheet 34 of 109

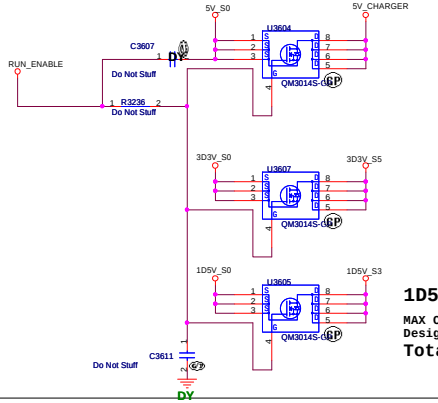

+1.05V POWER RAIL
+3.3V POWER RAIL
Vo = 0.8 * (1 + (RT / RB))
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 1D5V_S3 power rail.
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.
BOM OPTION:
24MHZ: FOR CRYSTAL MODE
48MHZ: FOR PCH EXTERNAL CLOCK MODE
PCI Express/ExpressCard select signal
USB30_PSEL
1: Others
0: ExpressCard or Mini card
Clock select signal
USB30_CSEL
1: 48 MHz external clock input
0: 24 MHz crystal mode
UPD720200F1 pin H1 (SMIB high active)
UPD720200AF1 pin P4 (SMI# low active)
+/-30ppm
HELE Recommended Conditions:
Normal Frequency: 24MHz.
Frequency Tolerance: +/- 30ppm.
Load Frequency: 12pF.
Effective Series Resistance: 50-ohm.
Effective Shunt Capacitancce: 2pF.
EMI near U3501
USB 64K EEPROM
72.25512.N01 flash tool not ready
71.72020.D0U==>MP part number
71.72020.E0U==>ES part number
Bypass re-Driver, near U3502
Close to pins - ideally about one caps for every two or
ideally about one caps for every two or three pins
For USB3.0 analog ricuit
For USB2.0 analog ricuit
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
USB 3.0 Controller
BAD50-HR
Thursday, April 07, 2011

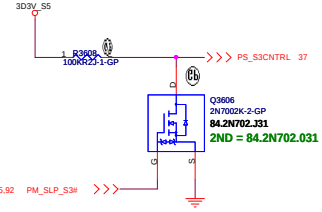
Power Sequence



ANNIE Run Power

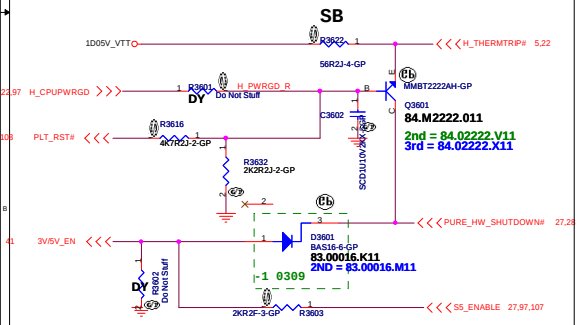


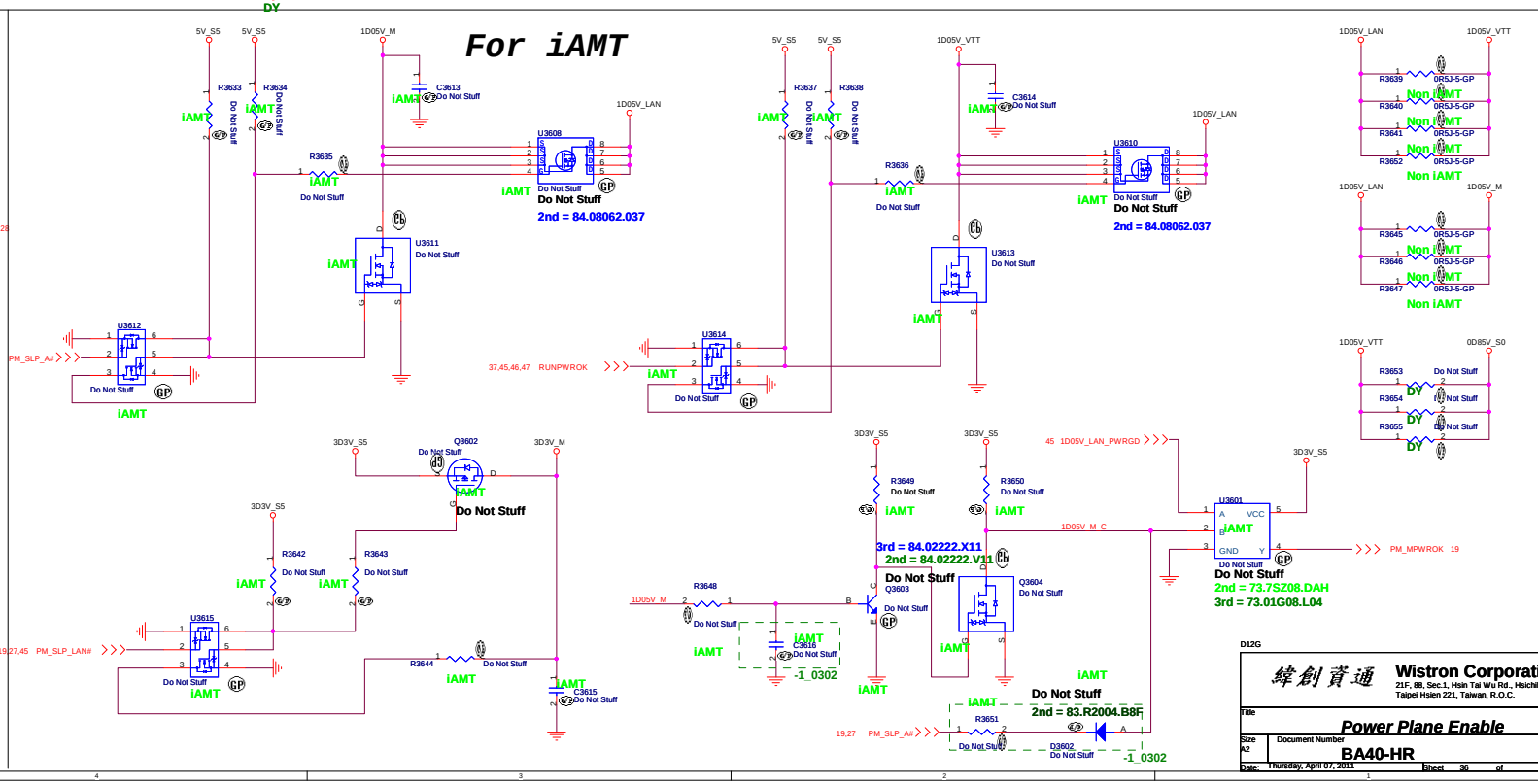




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A





D12G

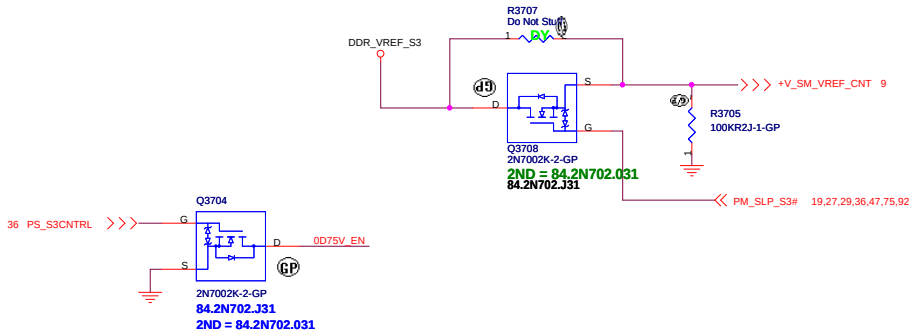
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

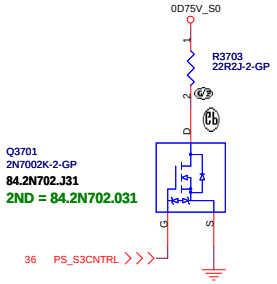
Size	Document Number	Rev
A2	BA40-HR	SD

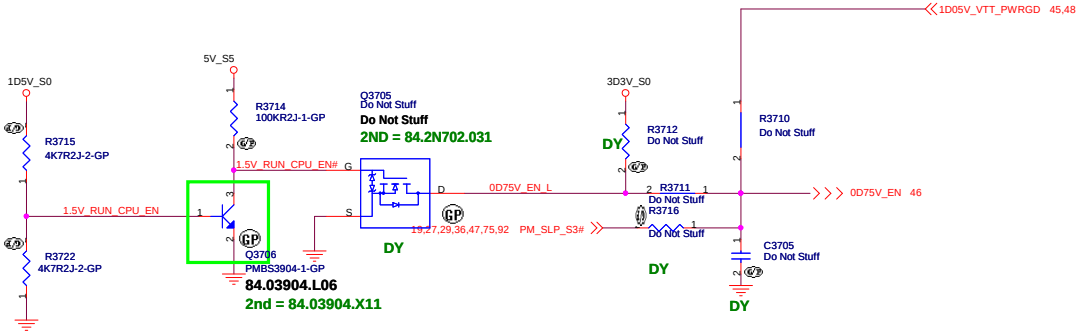
Date: Thursday, April 07, 2011 Sheet 36 of 109

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

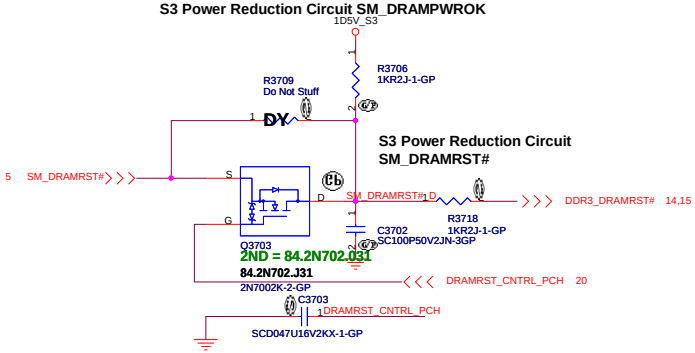


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

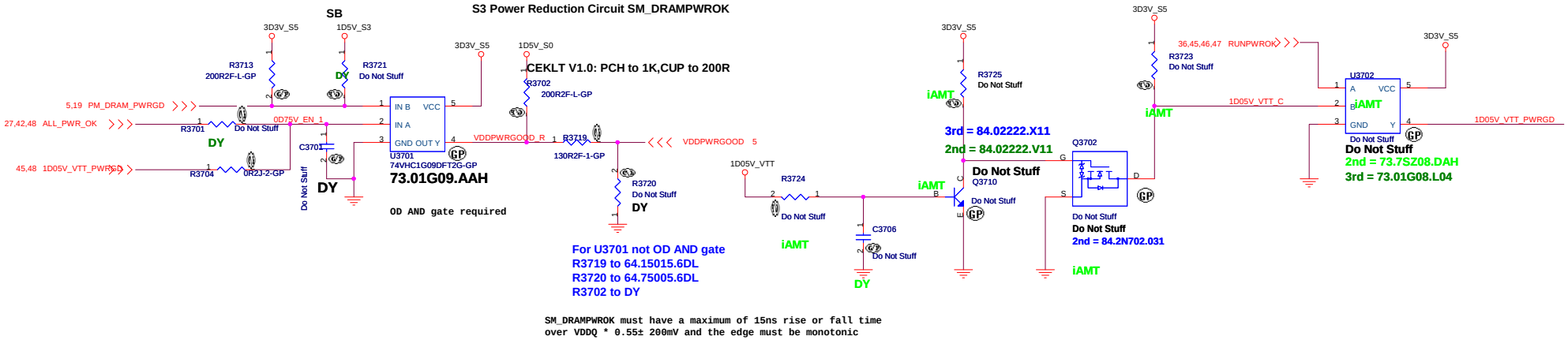




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

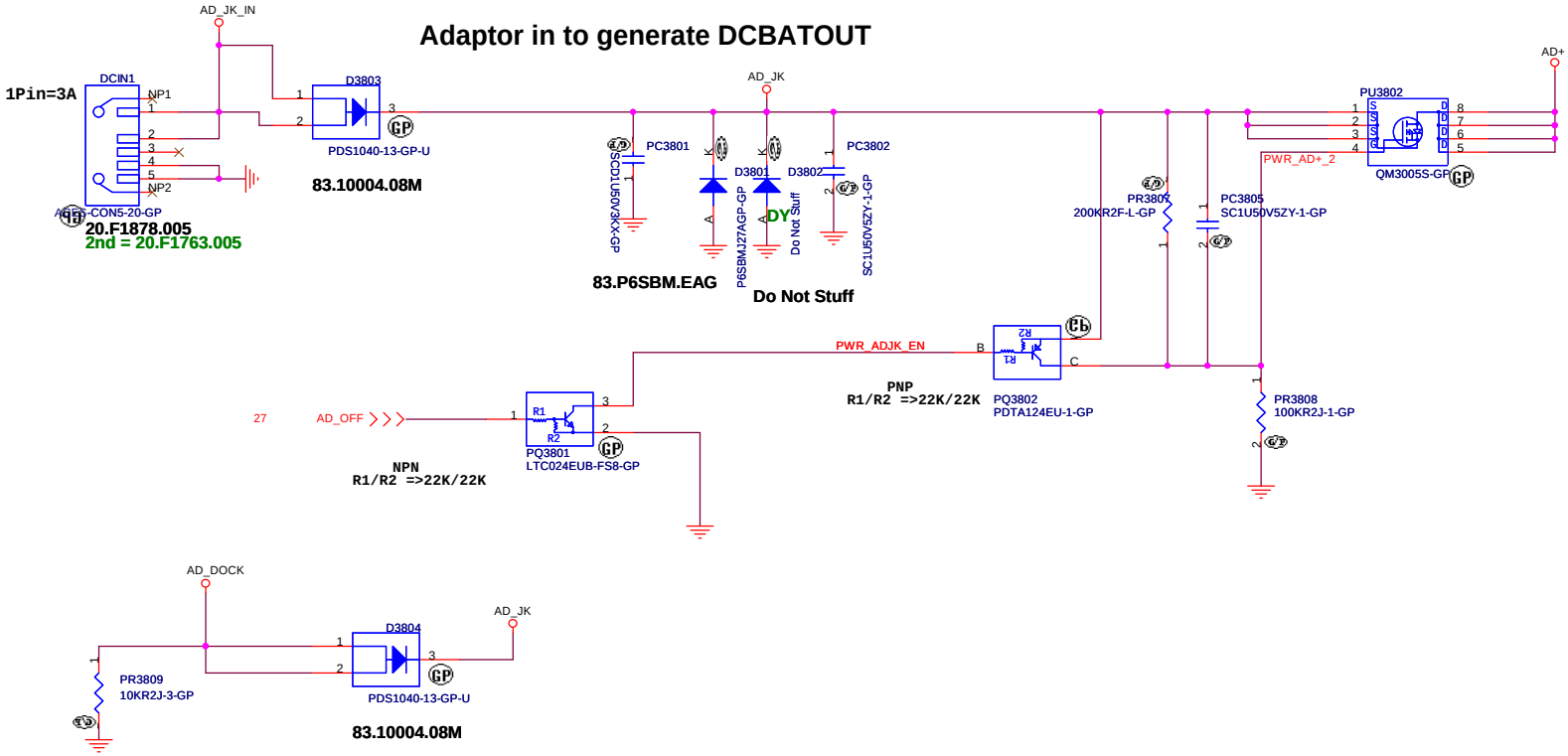


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADAPTER		
Size: Custom	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 37 of 109	

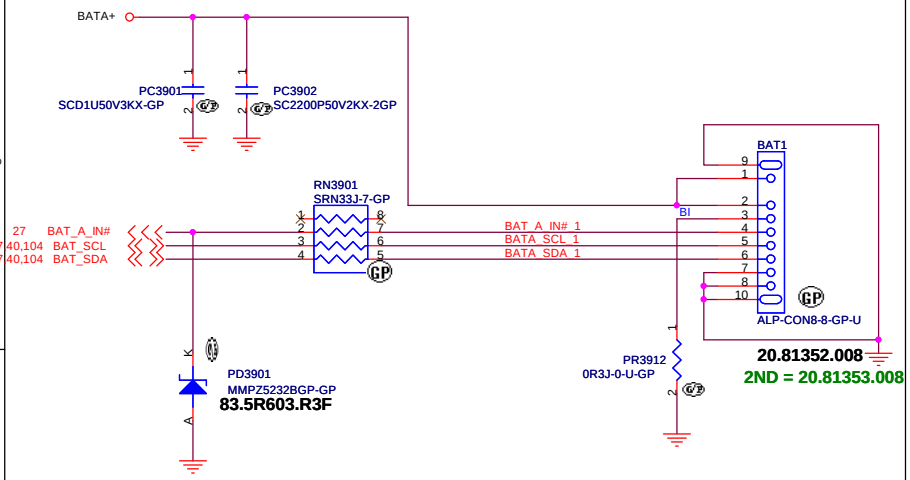
ANNIE solution



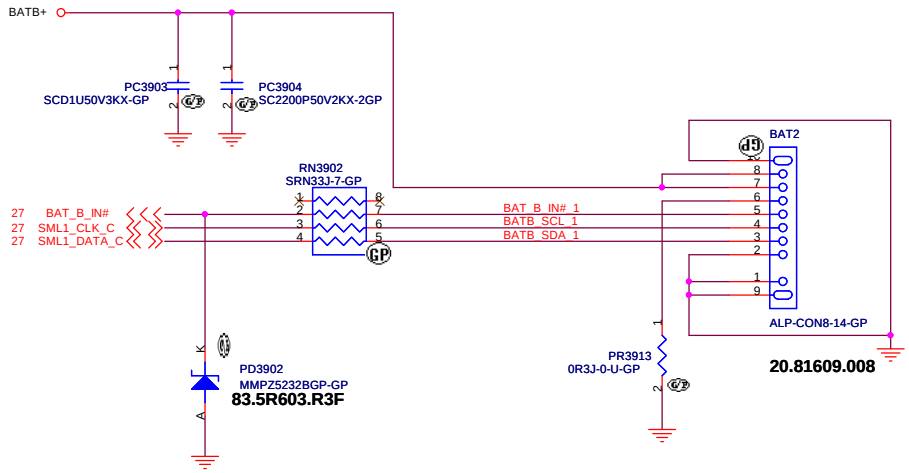
D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: A3	Document Number: BA40/50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 38 of 109	

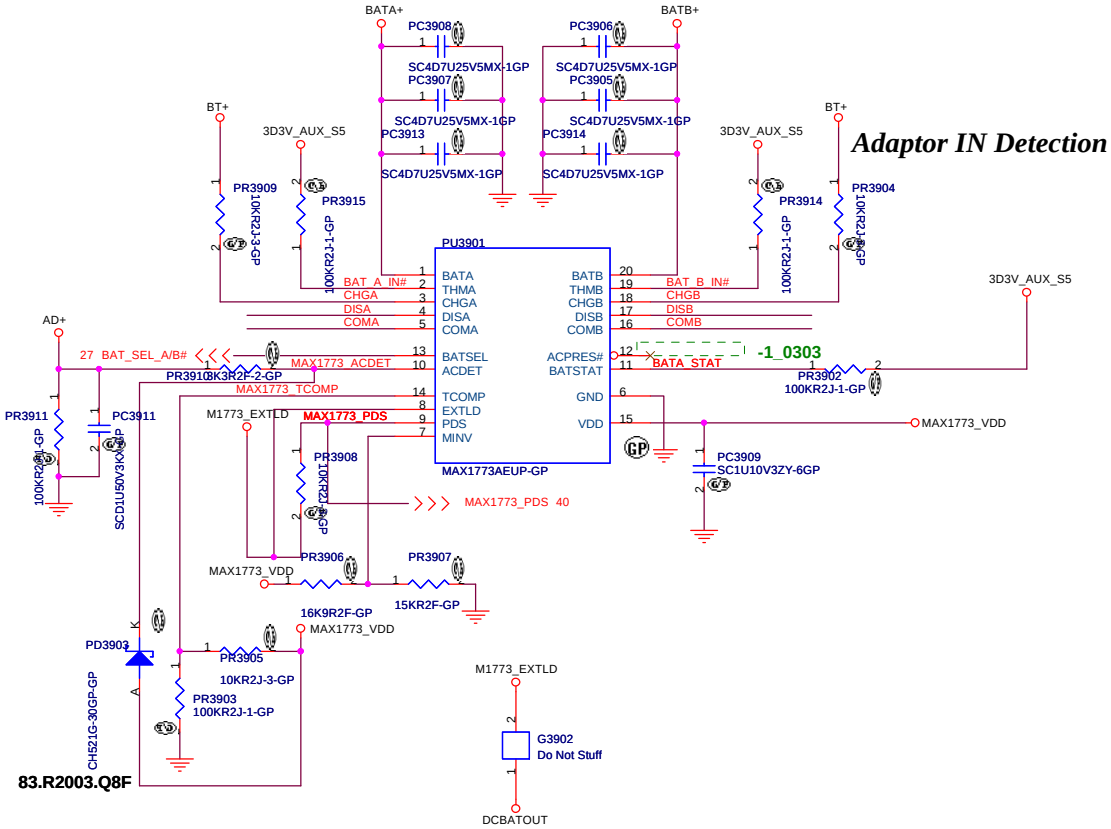
MAIN BATTERY CONNECTOR



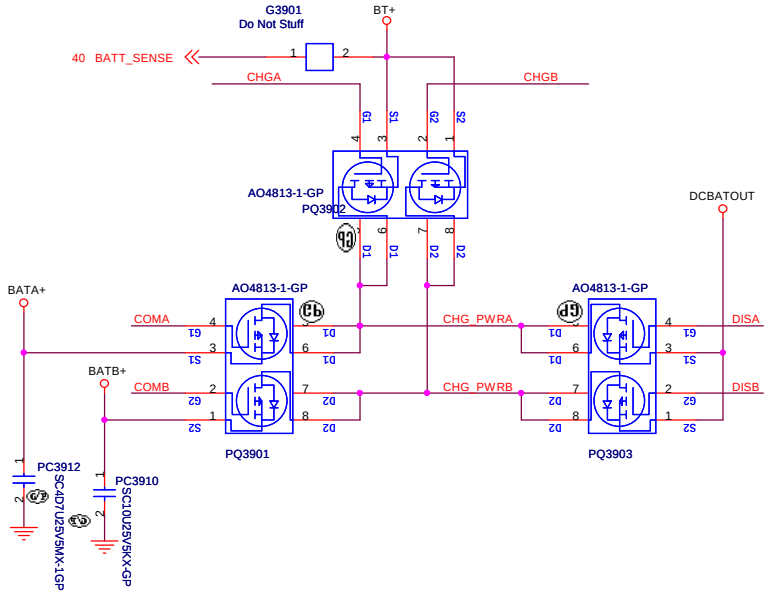
2nd BATTERY CONNECTOR



BATTERY SWITCH



Adaptor IN Detection



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT_CONN**

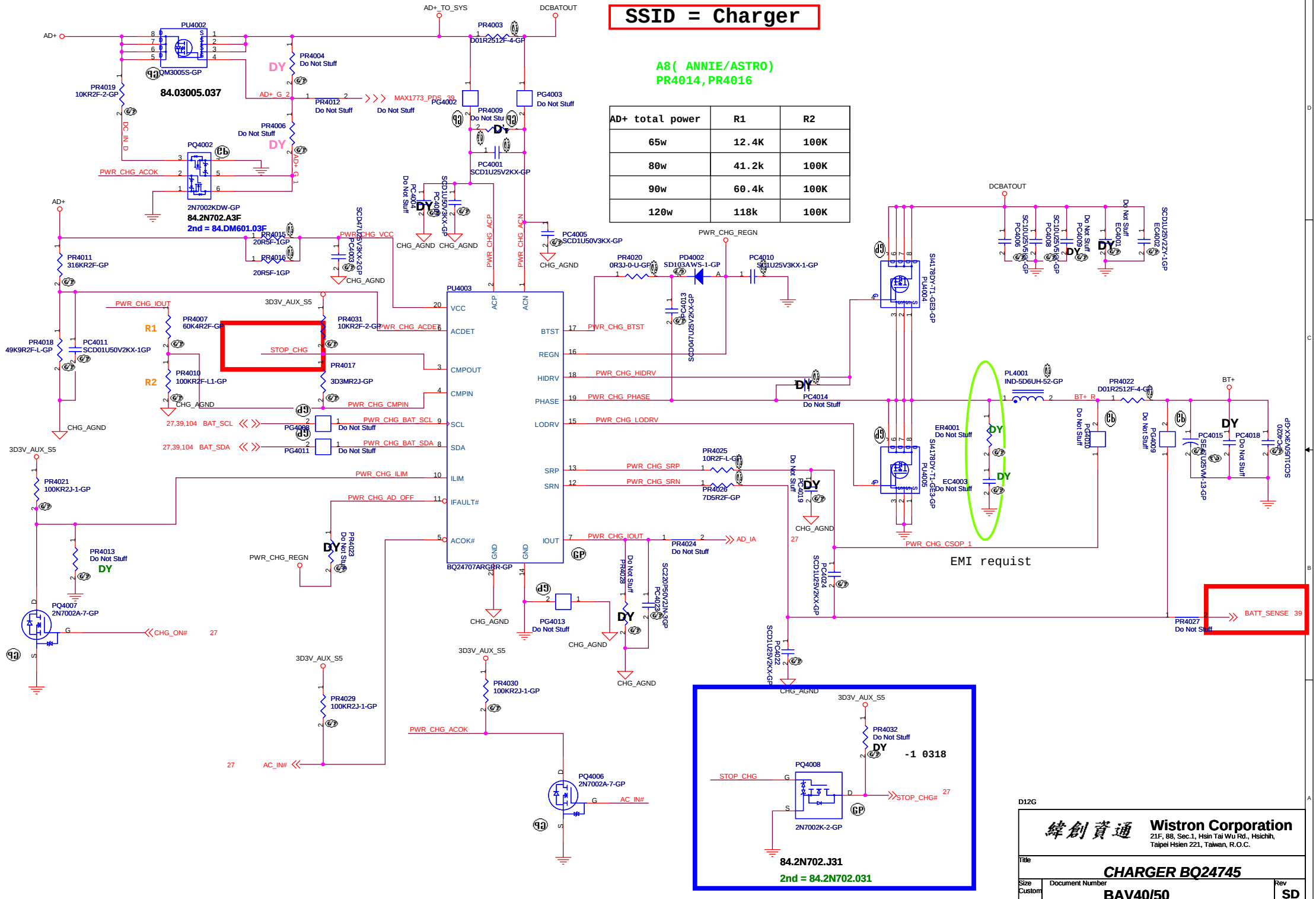
Size	Document Number	Rev
A3	BA40/50-HR	SD

Date: Thursday, April 07, 2011 Sheet 39 of 109

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size	Document Number	Rev
Custom	BAV40/50	SD

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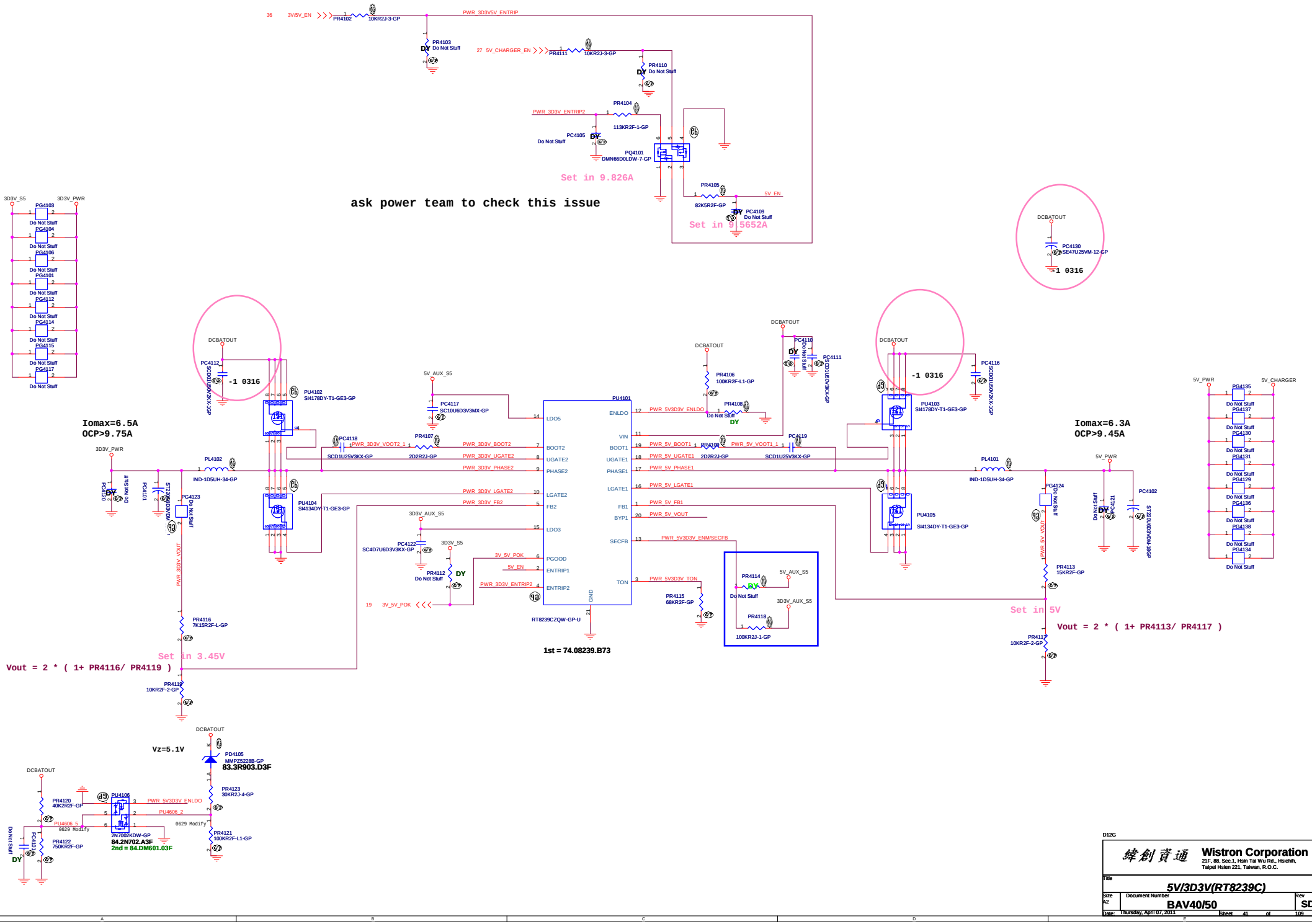
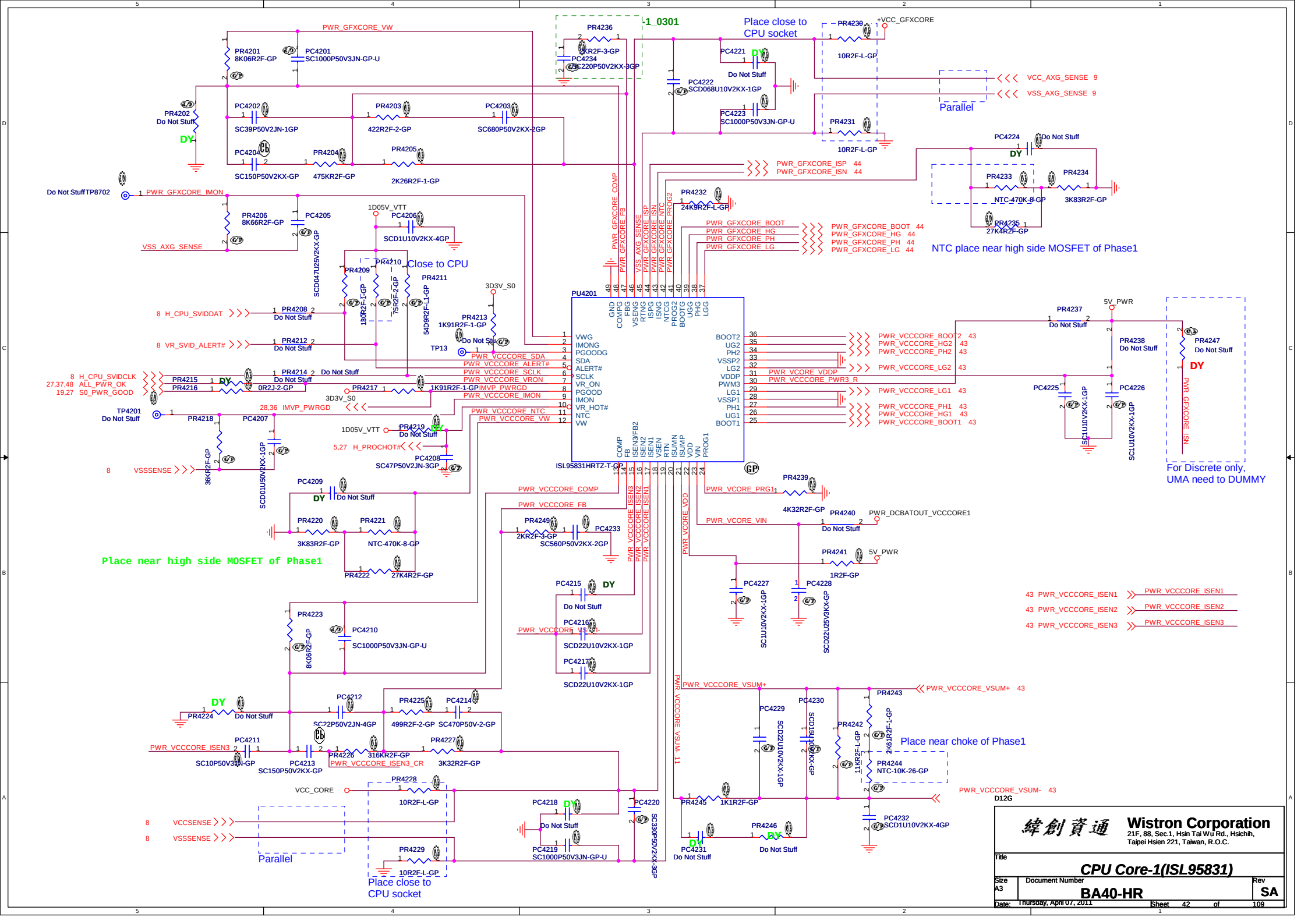

ask power team to check this issue
Set in 9.826A
Set in 3.5652A
Iomax=6.5A
OCP>9.75A
Iomax=6.3A
OCP>9.45A
Set in 3.45V
Vout = 2 * (1+ PR4116/ PR4119)
Set in 5V
Vout = 2 * (1+ PR4113/ PR4117)
Vz=5.1V
1st = 74.08239.B73
2nd = 84.DM601.03F
84.2N702.A3F
83.3R903.D3F
RT8239CZQW-GP-U
Wistron Corporation
5V/3D3V(RT8239C)
BAV40/50
Thursday, April 07, 2011


1_0301
Place close to CPU socket
Parallel
NTC place near high side MOSFET of Phase1
Close to CPU
Place near high side MOSFET of Phase1
Place near choke of Phase1
Place close to CPU socket
Parallel
For Discrete only, UMA need to DUMMY
PU4201
ISL95831HRTZ-T-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU Core-1(ISL95831)
BA40-HR
Rev SA
Thursday, April 07, 2011
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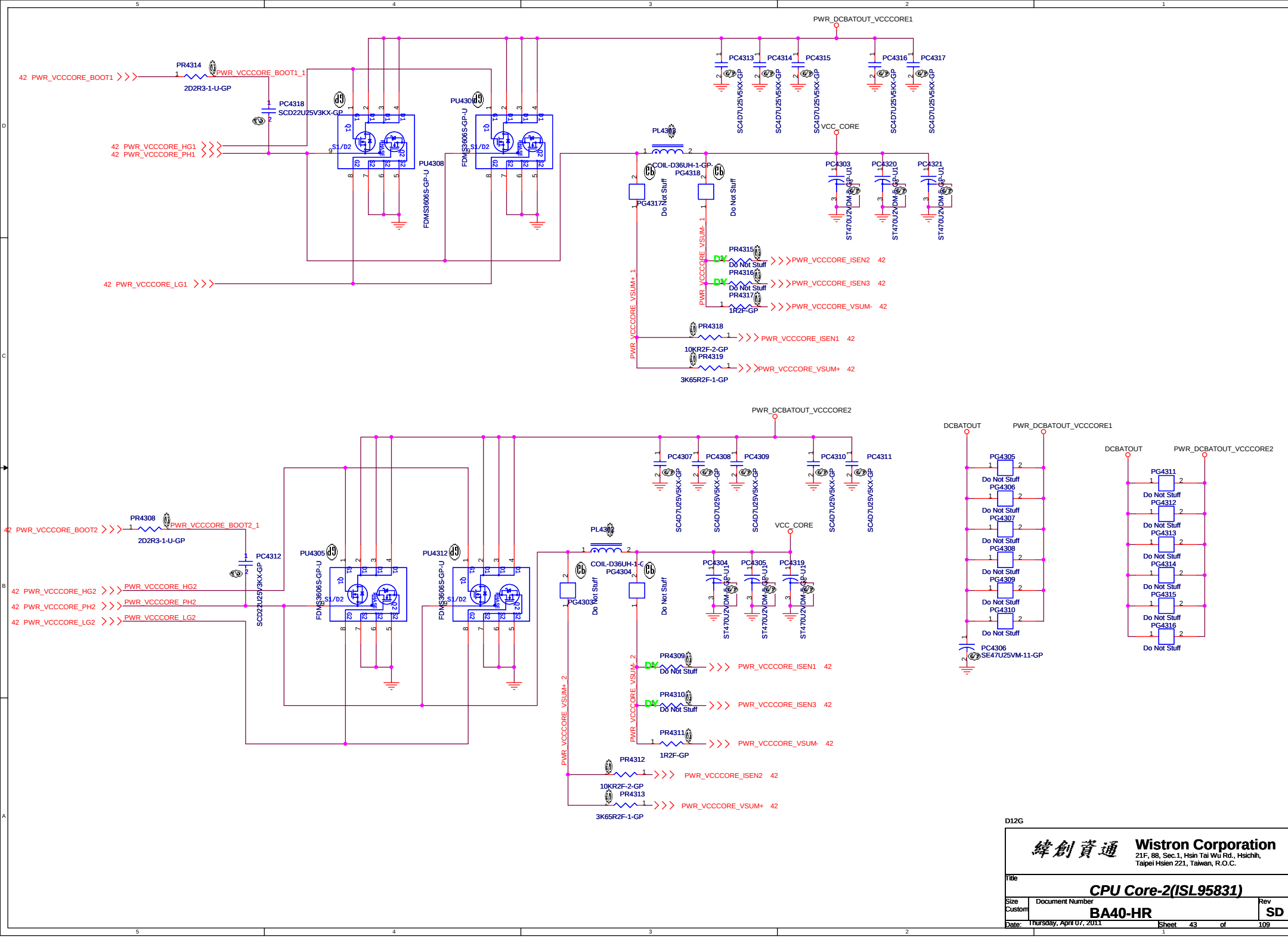


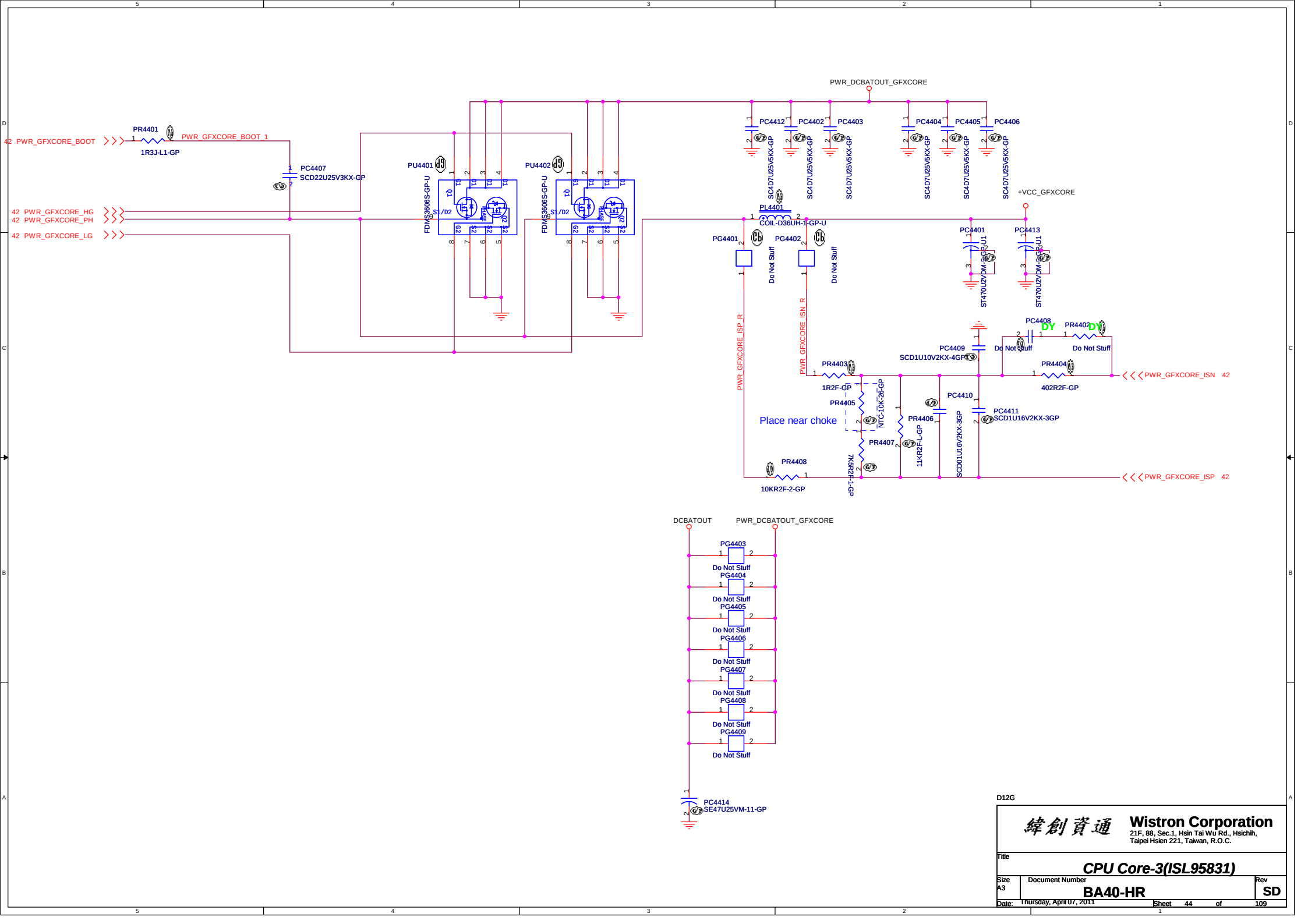
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Core-2(ISL95831)***

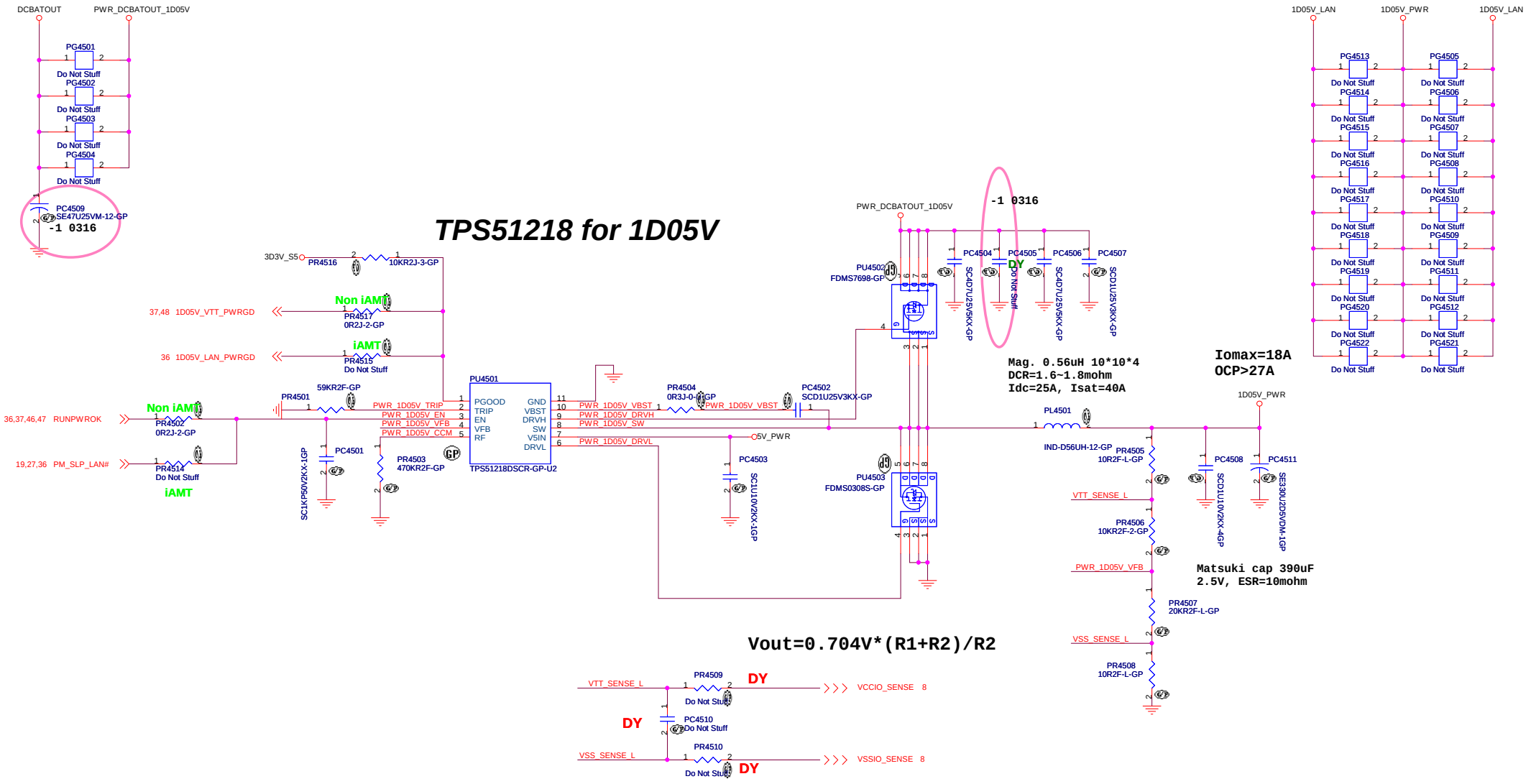
Size	Document Number	Rev
Custom	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 43 of 109



D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU Core-3(ISL95831)		
Size: A3	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 44 of 109	



D12G

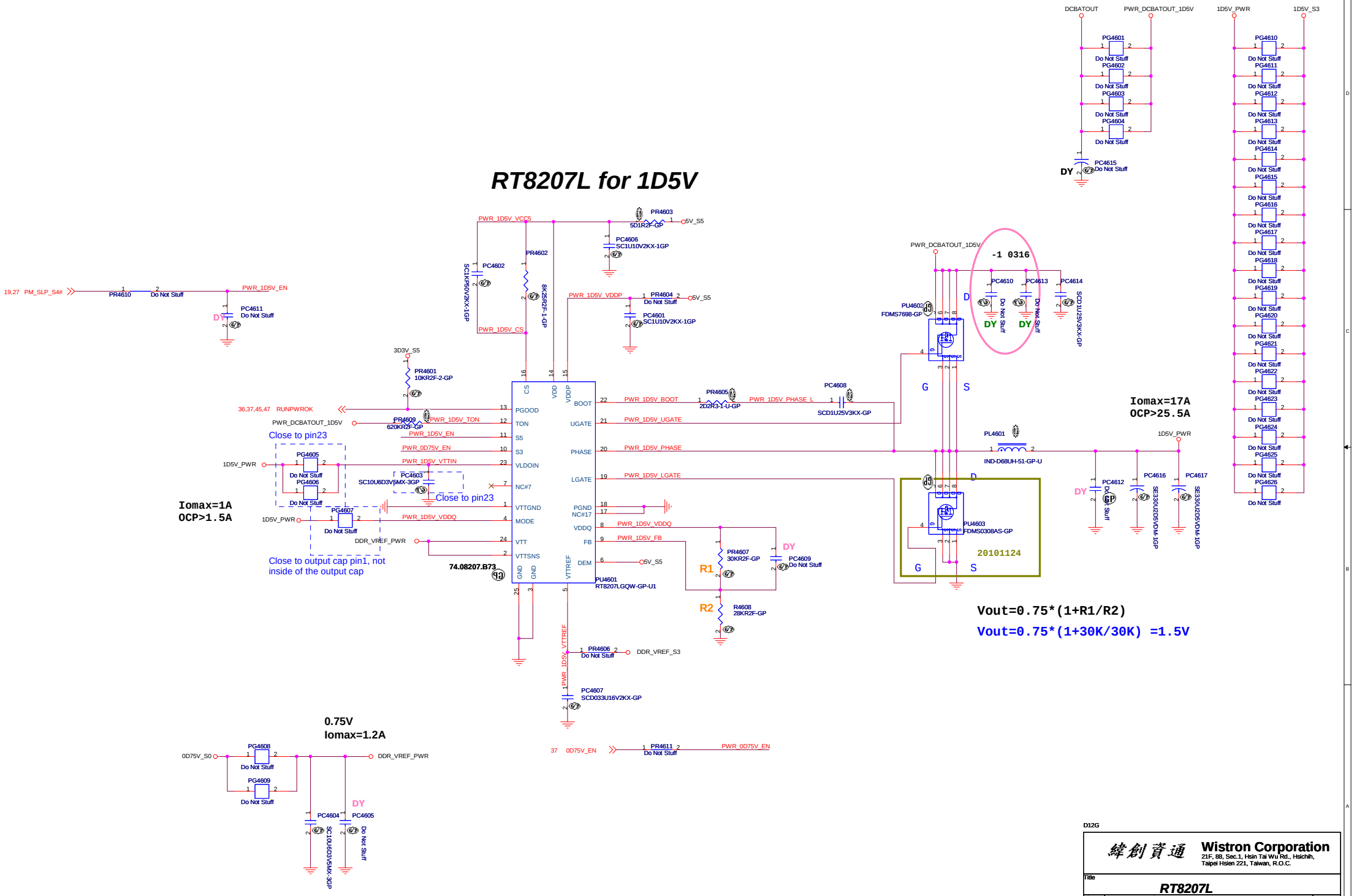
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D05V(TPS51218D)

Size	Document Number	Rev
Custom	BA40/50-HR	SD

Date: Thursday, April 07, 2011 Sheet 45 of 109

RT8207L for 1D5V

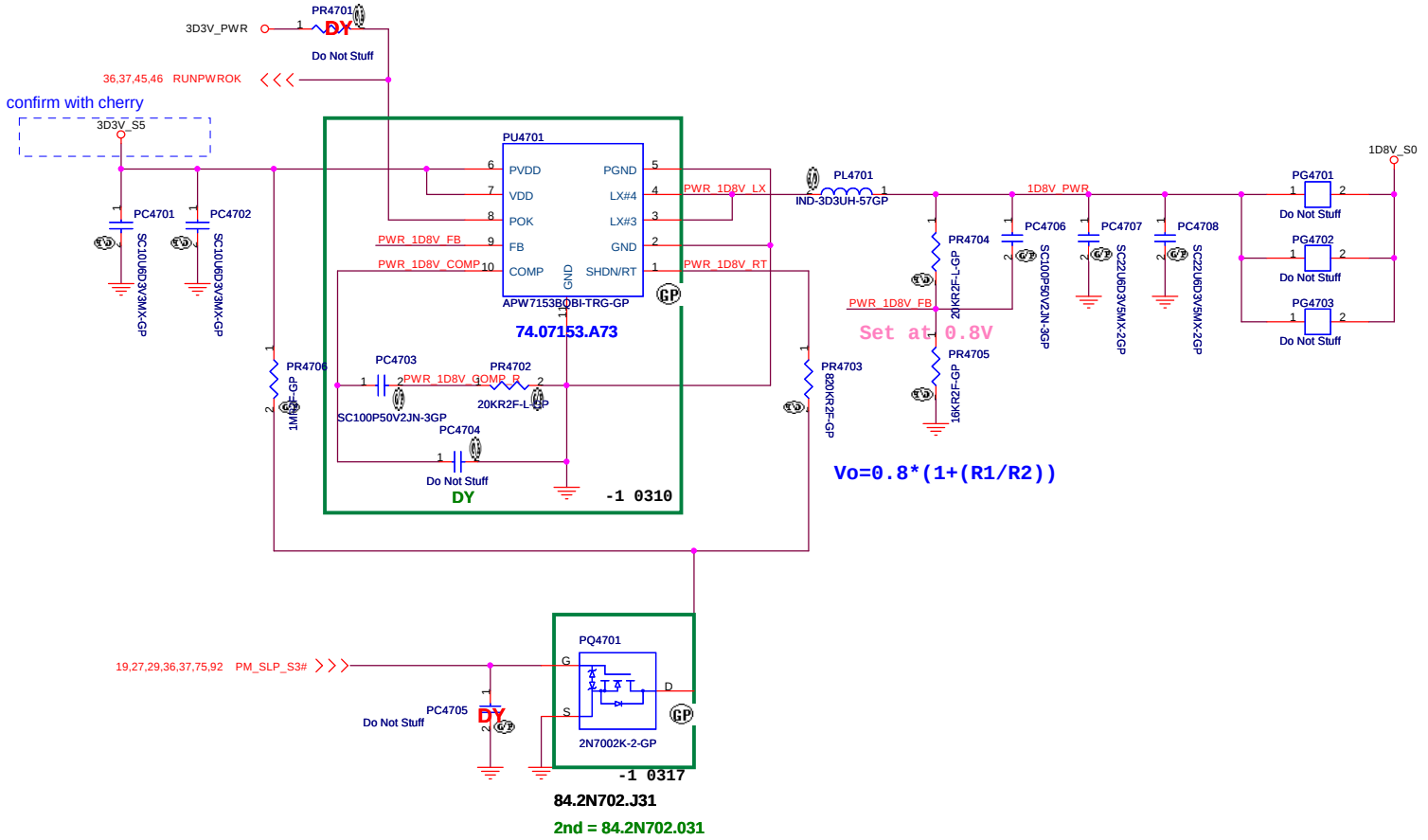


D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8207L	
Size: Custom	Document Number: BA40/50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 46 of 109	

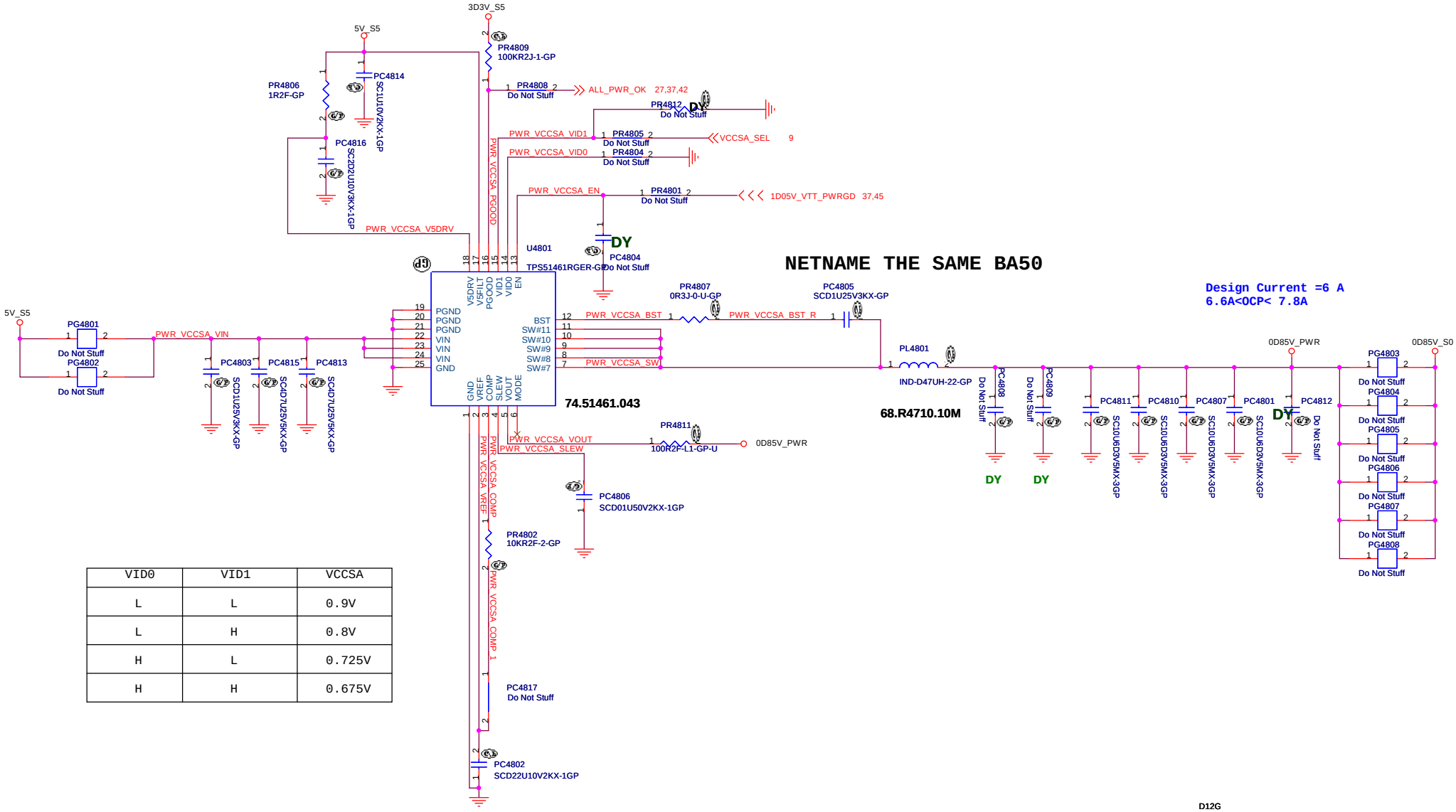
RT8015B for 1D8V_S0



D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT8015)*		
Size: A3	Document Number: BA40/50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 47 of 109	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO_VCCSA(APL5916)***

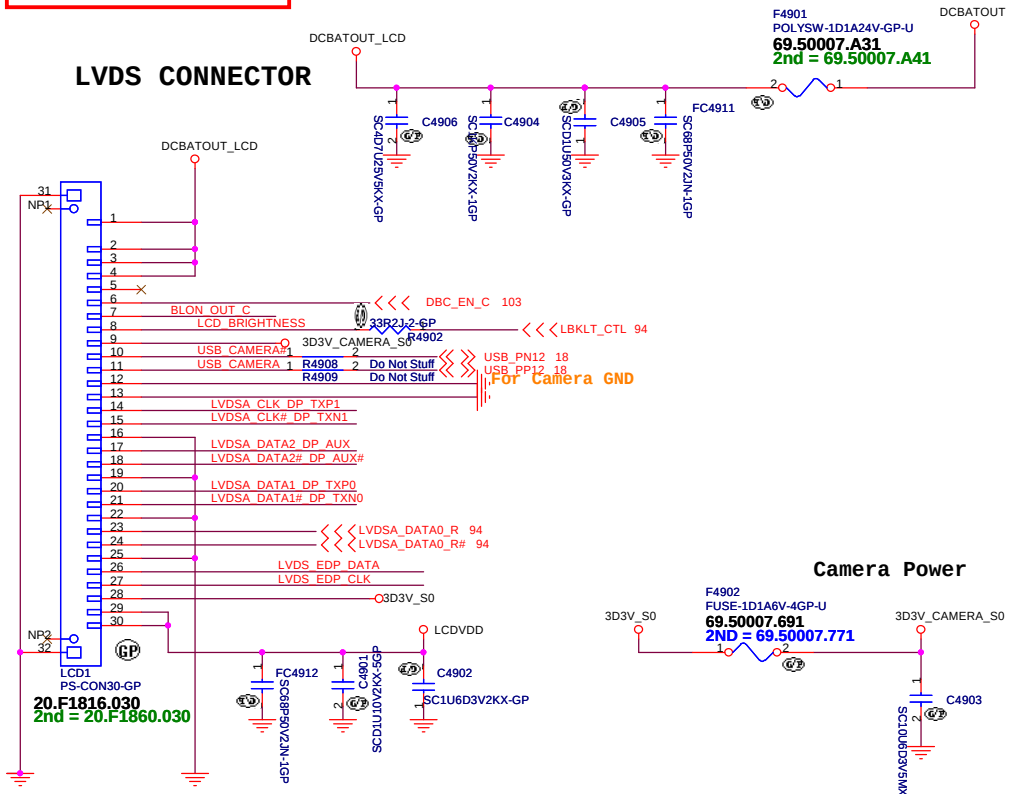
Size	Document Number	Rev
A3	BA40/50-HR	SD

Date: Thursday, April 07, 2011 Sheet 48 of 109

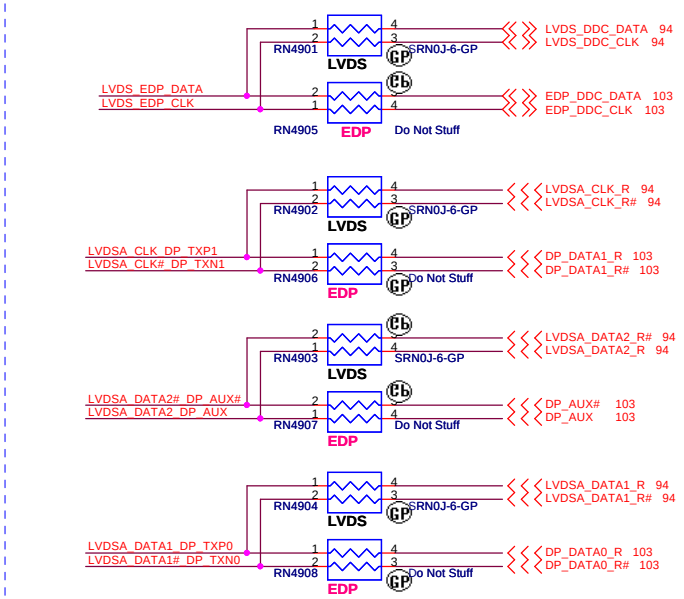
SSID = VIDEO

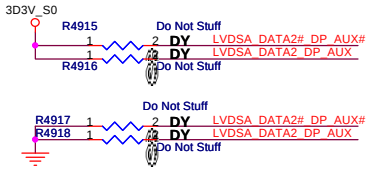
INVERTER POWER

LVDS CONNECTOR



Camera Power

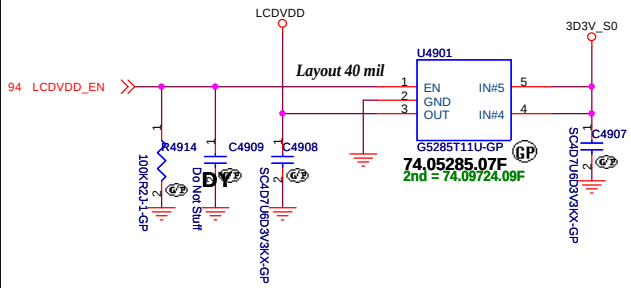


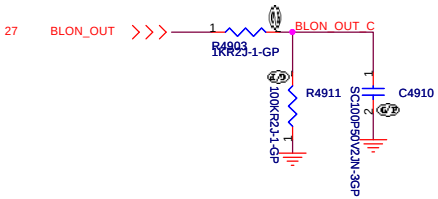


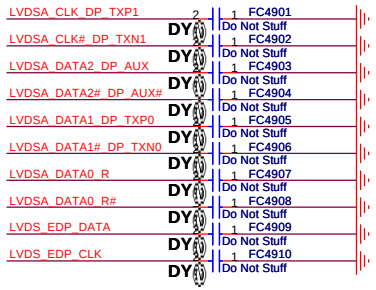
Close to LVDS connector

SSID = VIDEO

LCD POWER for ANNIE





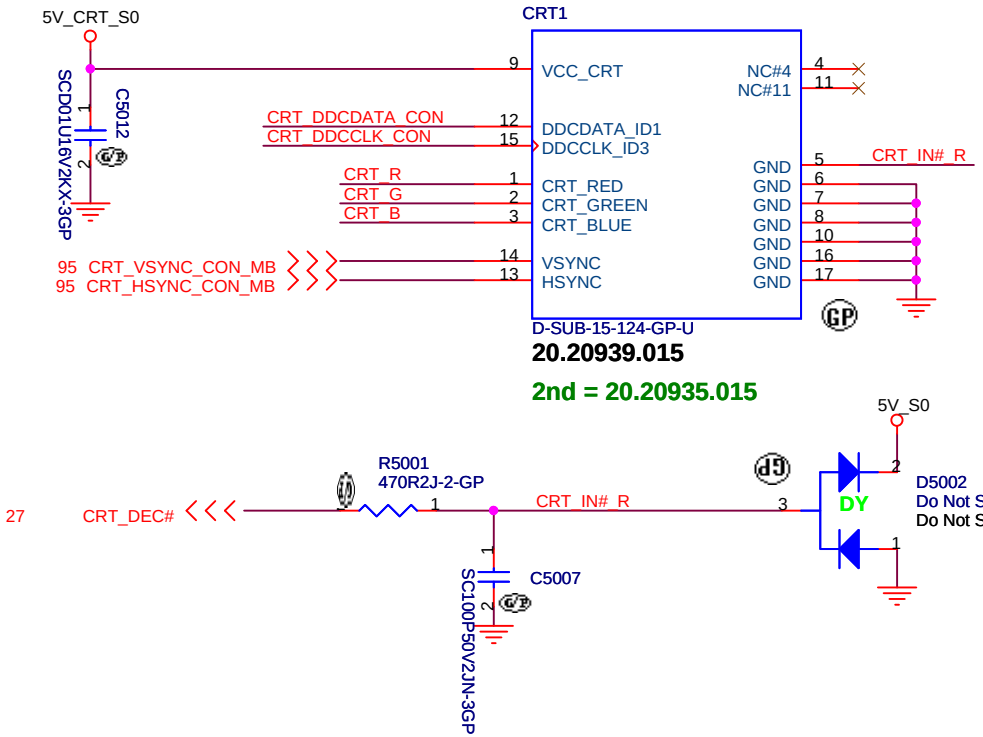


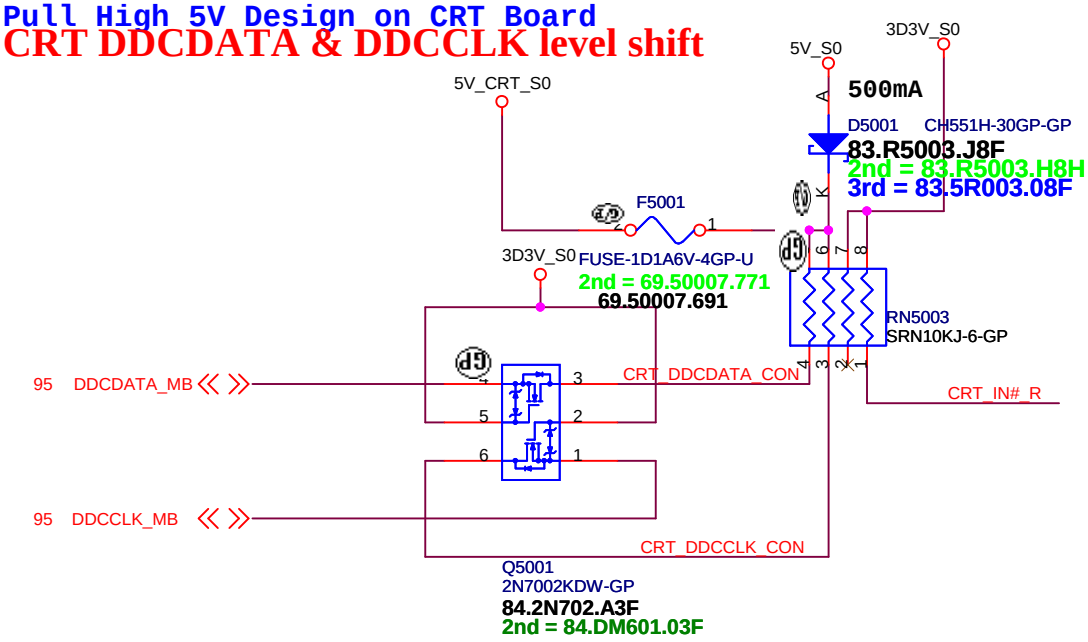
D12G

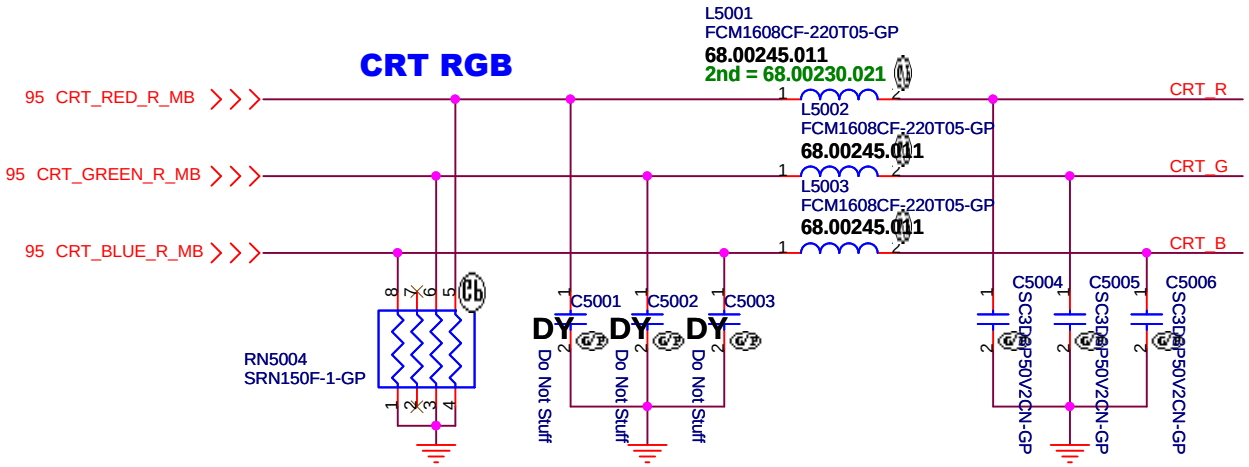
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD Connector		
Size: A3	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 49 of 109	

Pull High 5V Design on CRT Board

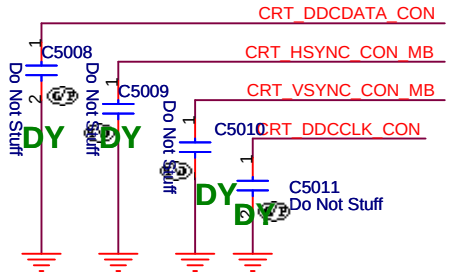
CRT DDCDATA & DDCCLK level shift







0806 check RN5004 擺放位置



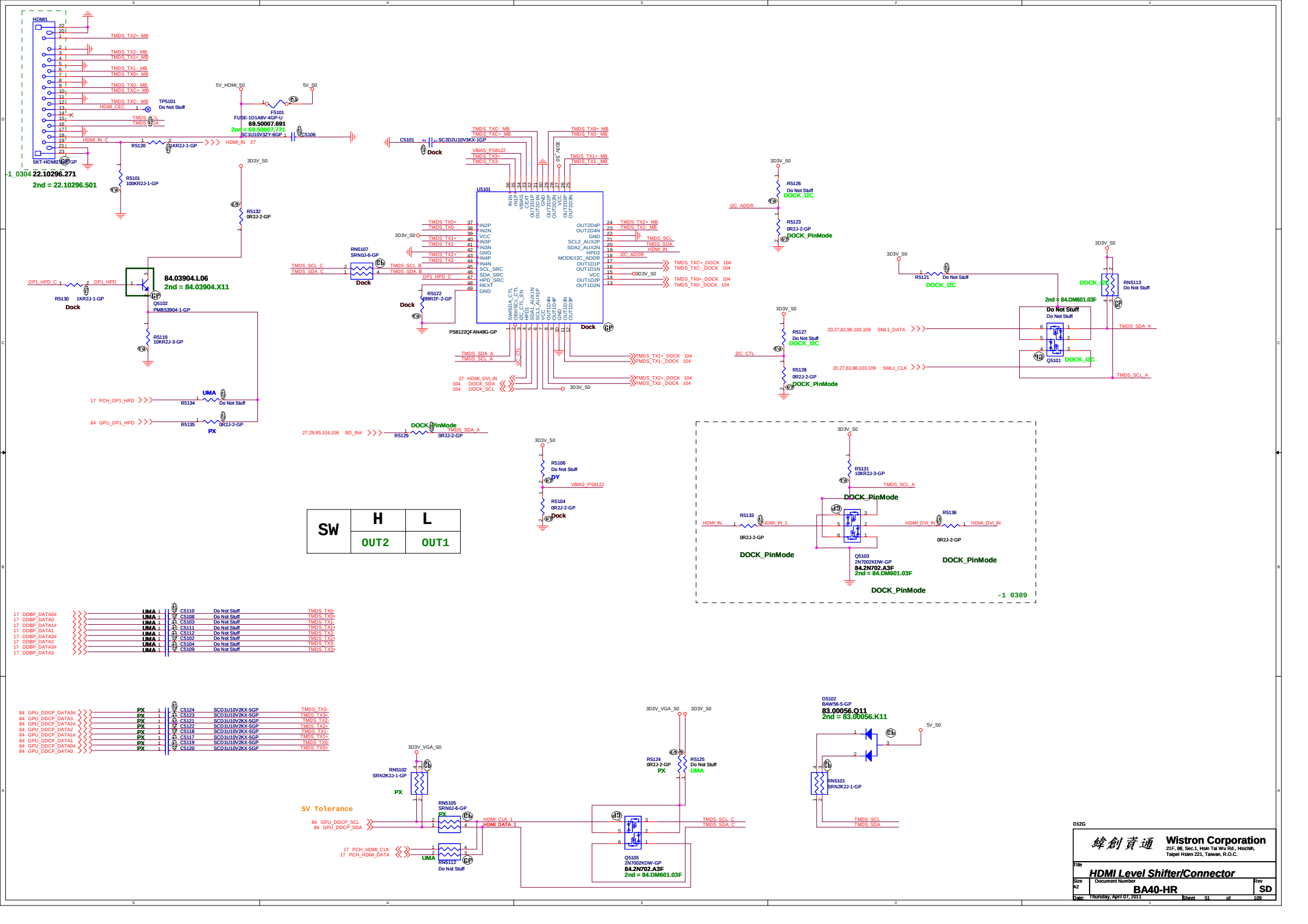
D12G

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

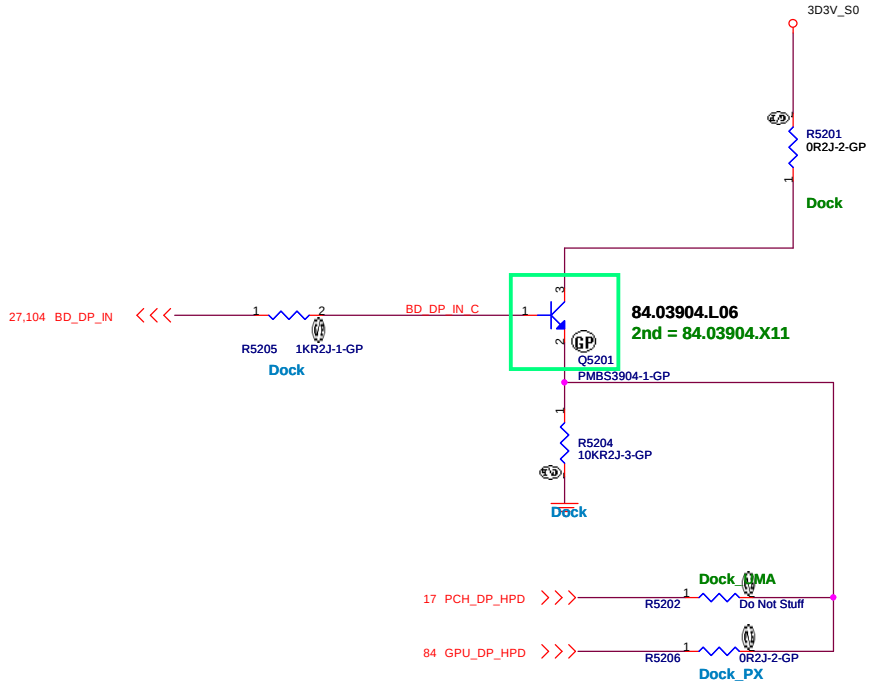
Title: **CRT Connector**

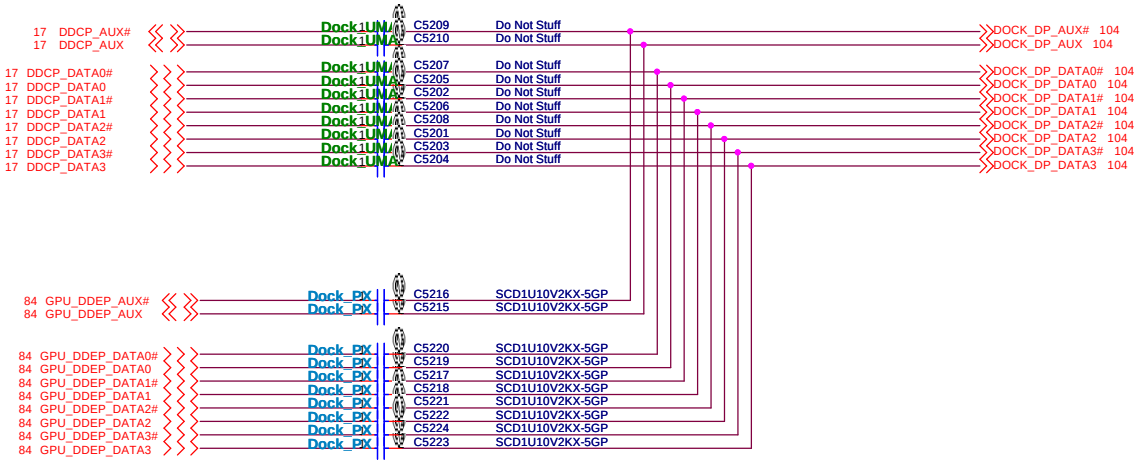
Size	Document Number	Rev
A4	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 50 of 109


HDMI1
SKT-HDMI-R-SP
TMDS_TX2+_MB
TMDS_TX2-_MB
TMDS_TX1+_MB
TMDS_TX1-_MB
TMDS_TX0+_MB
TMDS_TX0-_MB
TMDS_TXC+_MB
TMDS_TXC-_MB
HDMI_CEC
TMDS_SCL
TMDS_SDA
TP5101
Do Not Stuff
5V_HDMI_S0
5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
SC1U10V3ZY-6GP
C5106
HDMI_IN_C
R5120
0KR2J-1-GP
HDMI_IN 27
-1 0304 22.10296.271
2nd = 22.10296.501
R5101
100KR2J-1-GP
3D3V_S0
R5132
0R2J-2-GP
DP1_HPD_C
DP1_HPD
R5130
1KR2J-1-GP
Dock
84.03904.L06
2nd = 84.03904.X11
Q5102
PMBS3904-1-GP
R5119
10KR2J-3-GP
17 PCH_DP1_HPD
84 GPU_DP1_HPD
UMA
R5134
Do Not Stuff
R5135
0R2J-2-GP
PX
C5101
SC2D2U10V3KX-1GP
Dock
VBIAS_PS8122
TMDS_TX3+
TMDS_TX3-
TMDS_TX1+_MB
TMDS_TX1-_MB
5V_S0
U5101
PS8122QFAN48G-GP
Dock
TMDS_TX0+
TMDS_TX0-
TMDS_TX1+
TMDS_TX1-
TMDS_TX2+
TMDS_TX2-
IN2P
IN2N
VCC
IN3P
IN3N
GND
IN4P
IN4N
SCL_SRC
SDA_SRC
HPD_SRC
REXT
GND
OUT2D4P
OUT2D4N
GND
SCL2_AUX2P
SDA2_AUX2N
HPD2
MODE/I2C_ADDR
OUT1D1P
OUT1D1N
VCC
OUT1D2P
OUT1D2N
TMDS_TX2+_MB
TMDS_TX2-_MB
TMDS_SCL
TMDS_SDA
HDMI_IN
I2C_ADDR
TMDS_TXC+_DOCK 104
TMDS_TXC-_DOCK 104
TMDS_TX0+_DOCK 104
TMDS_TX0-_DOCK 104
RN5107
SRN0J-6-GP
Dock
TMDS_SCL_C
TMDS_SDA_C
TMDS_SCL_B
TMDS_SDA_B
DP1_HPD_C
R5122
499R2F-2-GP
Dock
TMDS_SDA_A
TMDS_SCL_A
I2C_CTL
TMDS_TX1+_DOCK 104
TMDS_TX1-_DOCK 104
TMDS_TX2+_DOCK 104
TMDS_TX2-_DOCK 104
27 HDMI_DVI_IN
104 DOCK_SDA
104 DOCK_SCL
3D3V_S0
R5126
Do Not Stuff
DOCK_I2C
I2C_ADDR
R5123
0R2J-2-GP
DOCK_PinMode
R5127
Do Not Stuff
DOCK_I2C
I2C_CTL
R5128
0R2J-2-GP
DOCK_PinMode
R5121
Do Not Stuff
DOCK_I2C
20,27,82,86,103,109 SML1_DATA
20,27,82,86,103,109 SML1_CLK
RN5113
Do Not Stuff
DOCK_I2C
2nd = 84.DM601.03F
Do Not Stuff
Do Not Stuff
Q5101
DOCK_I2C
TMDS_SDA_A
TMDS_SCL_A
27,29,95,104,106 BD_IN#
R5129
0R2J-2-GP
DOCK_PinMode
TMDS_SDA_A
R5106
Do Not Stuff
DY
VBIAS_PS8122
R5104
0R2J-2-GP
Dock
SW
H
L
OUT2
OUT1
R5131
10KR2J-3-GP
TMDS_SCL_A
DOCK_PinMode
R5133
HDMI_IN
HDMI_IN_1
0R2J-2-GP
DOCK_PinMode
R5136
HDMI_DVI_IN
HDMI_DVI_IN
0R2J-2-GP
DOCK_PinMode
Q5103
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
DOCK_PinMode
-1 0309
17 DDBP_DATA0#
17 DDBP_DATA0
17 DDBP_DATA1#
17 DDBP_DATA1
17 DDBP_DATA2#
17 DDBP_DATA2
17 DDBP_DATA3#
17 DDBP_DATA3
UMA
C5110 Do Not Stuff TMDS_TX0-
C5108 Do Not Stuff TMDS_TX0+
C5103 Do Not Stuff TMDS_TX1-
C5111 Do Not Stuff TMDS_TX1+
C5112 Do Not Stuff TMDS_TX2-
C5102 Do Not Stuff TMDS_TX2+
C5104 Do Not Stuff TMDS_TX3-
C5109 Do Not Stuff TMDS_TX3+
84 GPU_DDCP_DATA3#
84 GPU_DDCP_DATA3
84 GPU_DDCP_DATA2#
84 GPU_DDCP_DATA2
84 GPU_DDCP_DATA1#
84 GPU_DDCP_DATA1
84 GPU_DDCP_DATA0#
84 GPU_DDCP_DATA0
PX
C5124 SCD1U10V2KX-5GP TMDS_TX3-
C5123 SCD1U10V2KX-5GP TMDS_TX3+
C5121 SCD1U10V2KX-5GP TMDS_TX2-
C5122 SCD1U10V2KX-5GP TMDS_TX2+
C5118 SCD1U10V2KX-5GP TMDS_TX1-
C5117 SCD1U10V2KX-5GP TMDS_TX1+
C5119 SCD1U10V2KX-5GP TMDS_TX0-
C5120 SCD1U10V2KX-5GP TMDS_TX0+
3D3V_VGA_S0
RN5102
SRN2K2J-1-GP
PX
5V Tolerance
RN5105
SRN0J-6-GP
PX
84 GPU_DDCP_SCL
84 GPU_DDCP_SDA
HDMI_CLK_1
HDMI_DATA_1
17 PCH_HDMI_CLK
17 PCH_HDMI_DATA
UMA
RN5112
Do Not Stuff
3D3V_VGA_S0
3D3V_S0
R5124
0R2J-2-GP
PX
R5125
Do Not Stuff
UMA
Q5105
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
TMDS_SCL_C
TMDS_SDA_C
D5102
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
5V_S0
RN5101
SRN2K2J-1-GP
TMDS_SCL
TMDS_SDA
D12G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Level Shifter/Connector
Size A2
Document Number
BA40-HR
Rev SD
Date: Thursday, April 07, 2011
Sheet 51 of 109

DP





D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display Port***

Size	Document Number	Rev
A3	BAD50-HR	SD

Date: Thursday, April 07, 2011 Sheet 52 of 109

(Blanking)

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 53 of 109

(Blanking)

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

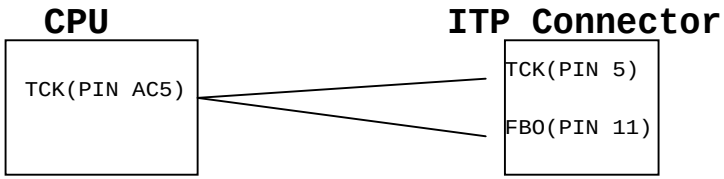
Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 54 of 109

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



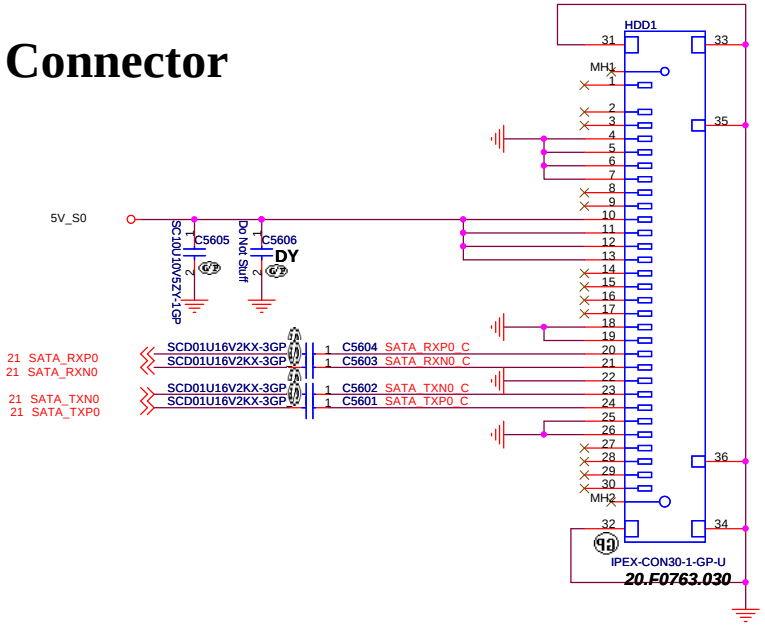
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

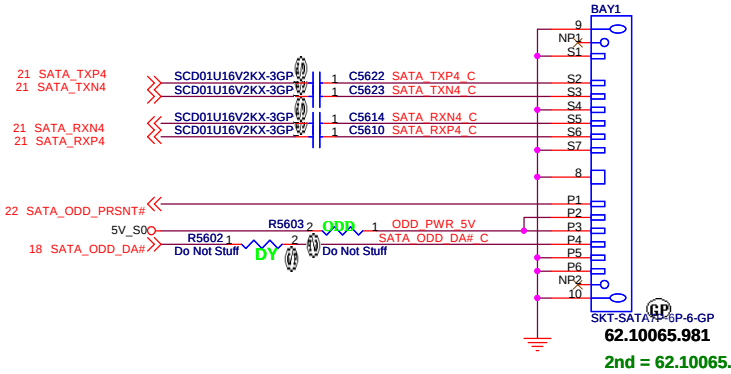
Title: ITP		
Size: A4	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 55 of 109	

SSID = SATA

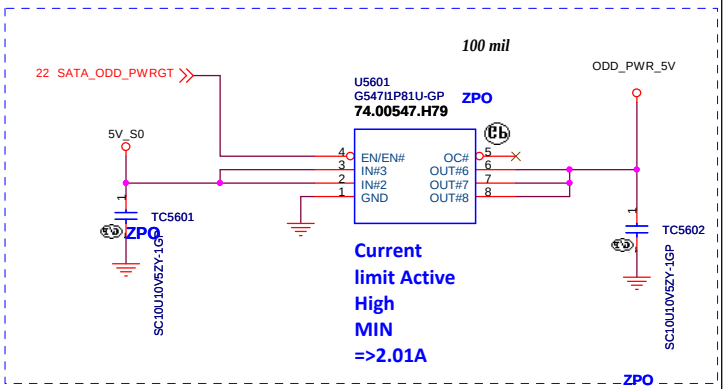
SATA HDD Connector



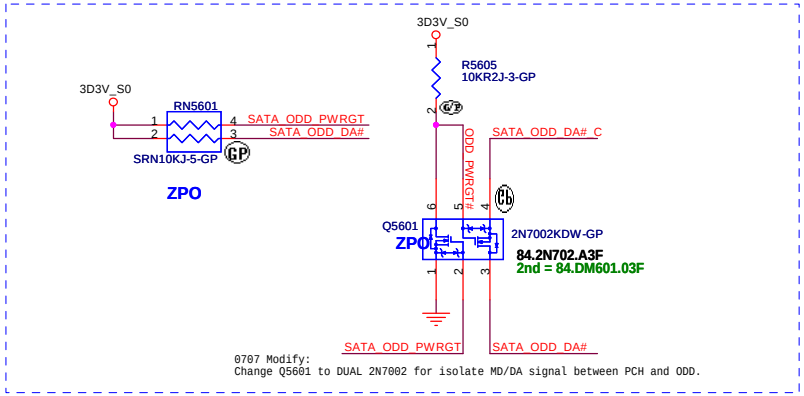
ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



SATA Zero Power ODD



SATA Zero Power ODD



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 56 of 109

ESATA Power

MIN Current limit 2.5A
LOW ACTIVE TYPE!

5V_S5
27,35,82 USB_PWR_EN#
at least 80 mil
G547E2P81U-GP
EN/EN# OC#
IN#3 OUT#6
IN#2 OUT#7
GND OUT#8
U5701
2nd = 74.00547.079
5V_USB0_S5
at least 80 mil
C5702 SCD1U10V2KX-4GP
C5709 SC1U10V3ZY-6GP
C5703 SCD1U10V2KX-4GP
C5704 SC1U10V3ZY-6GP
TC5701 SE330U6D3VM-15-GP
77.53371.04L

21 SATA_TXP5
21 SATA_TXN5
21 SATA_RXN5
21 SATA_RXP5
C5710 C5711 C5714 C5715 SCD01U16V2KX-3GP
SATA_TXP5_R SATA_TXN5_R SATA_RXN5_R SATA_RXP5_R

1D5V_S0
R5709 R5710 R5711 R5712 4K7R2J-2-GP
I-ESATA
U5702
GND A_BST# A_EQ B_EQ AUTOPW_EN VDD
A_INP A_INN GND B_OUTN B_OUTP
A_OUTP A_OUTN GND B_INN B_INP
VDD EN B_PRE A_PRE B_BST#
PS8511ATQFN20GTA3-GP
SATA_TXP5_L SATA_TXN5_L SATA_RXN5_L SATA_RXP5_L
-1_0303
1D5V_S0
R5707 R5708 R5713 4K7R2J-2-GP
I-ESATA
71.08511.C03

RN5701 Do Not Stuff
SATA_TXP5_R SATA_TXN5_R
SATA_TXP5_C SATA_TXN5_C
R-ESATA

RN5702 Do Not Stuff
SATA_RXN5_R SATA_RXP5_R
SATA_RXN5_C SATA_RXP5_C
R-ESATA

18 USB_PP1
R5701 Do Not Stuff
USB_PP1_C

18 USB_PN1
R5702 Do Not Stuff
USB_PN1_C

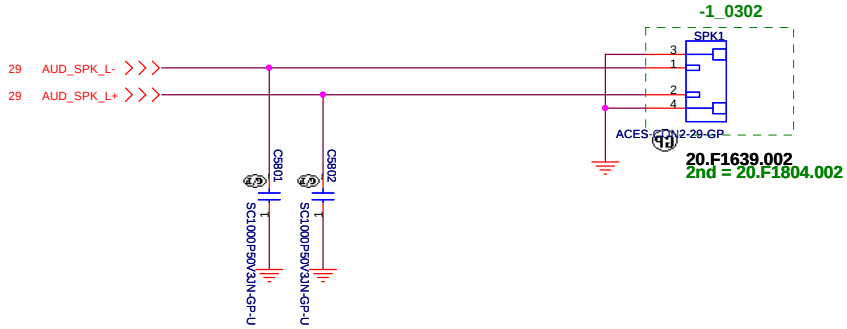
ESATA1
NP1 NP2
5V_USB0_S5
USB_PN1_C
USB_PP1_C
SATA_RXP5_C SATA_RXN5_C SATA_TXN5_C SATA_TXP5_C
C5705 C5706 C5708 C5707 SCD01U16V2KX-3GP
SATA_RXP5_L SATA_RXN5_L SATA_TXN5_L SATA_TXP5_L
SKT-USB+ESATA-8-GP
I-ESATA
-1_0303
22.10254.421
2nd = 22.10254.391

D12G

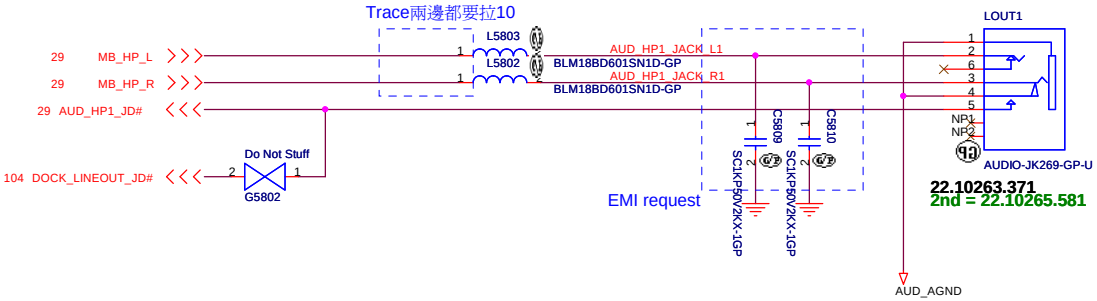
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***E-SATA/USB CHARGER***	
Size A3	Document Number **BA40-HR**	Rev **SD**
Date: Thursday, April 07, 2011	Sheet 57 of 109	

SSID = AUDIO

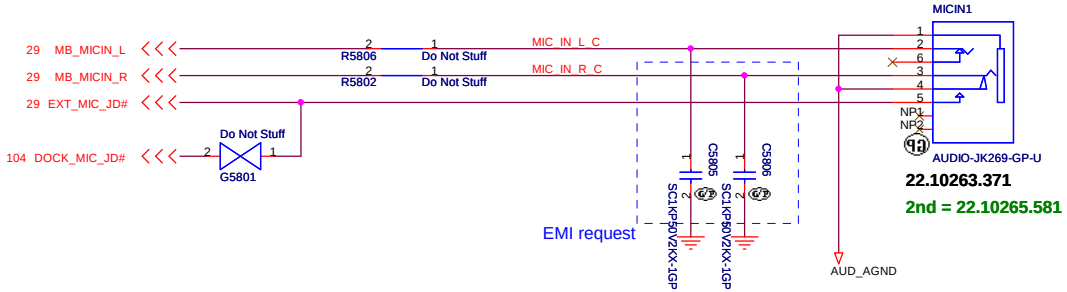
Speaker Connector

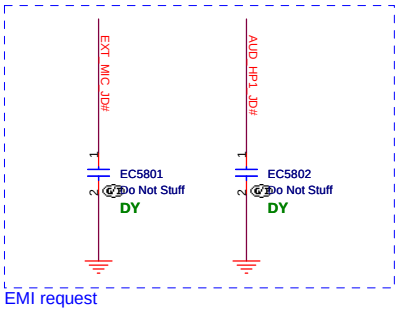


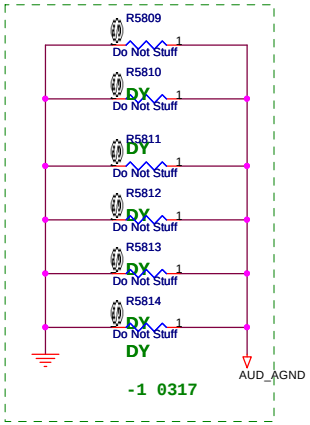
LINE1 OUT



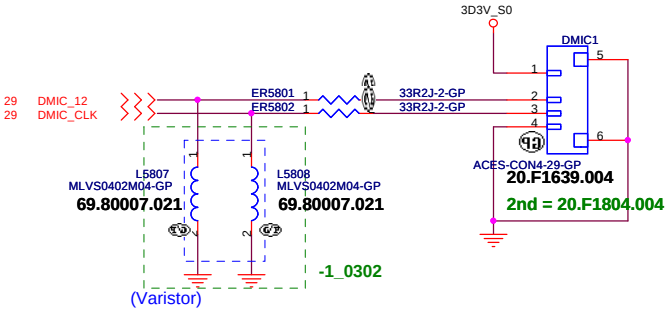
MIC IN







Internal Microphone



(Varistor)
Need confirm with EMI :
69.80007.021 or 69.80024.011 ?

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio Jack***

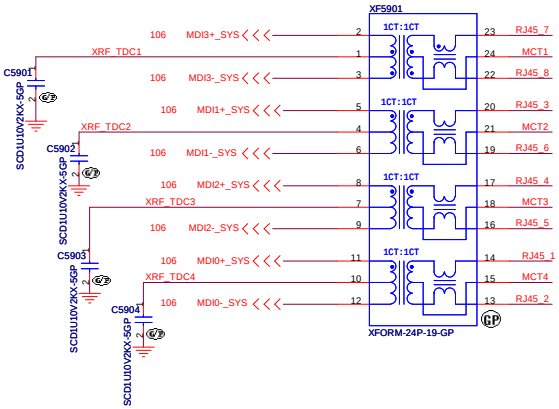
Size	Document Number	Rev
A3	BA40-HR	SA

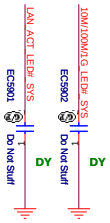
Date: Thursday, April 07, 2011 Sheet 58 of 109

GIGA Lan Transformer

SSID = LOM

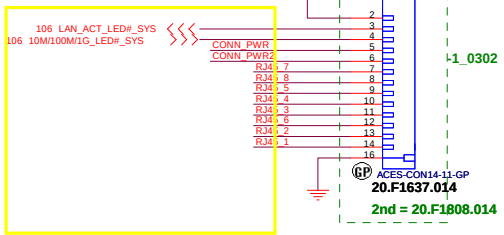
LAN MDI Off-Page

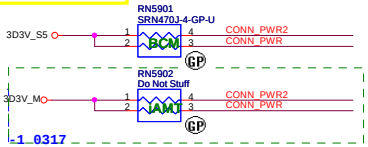




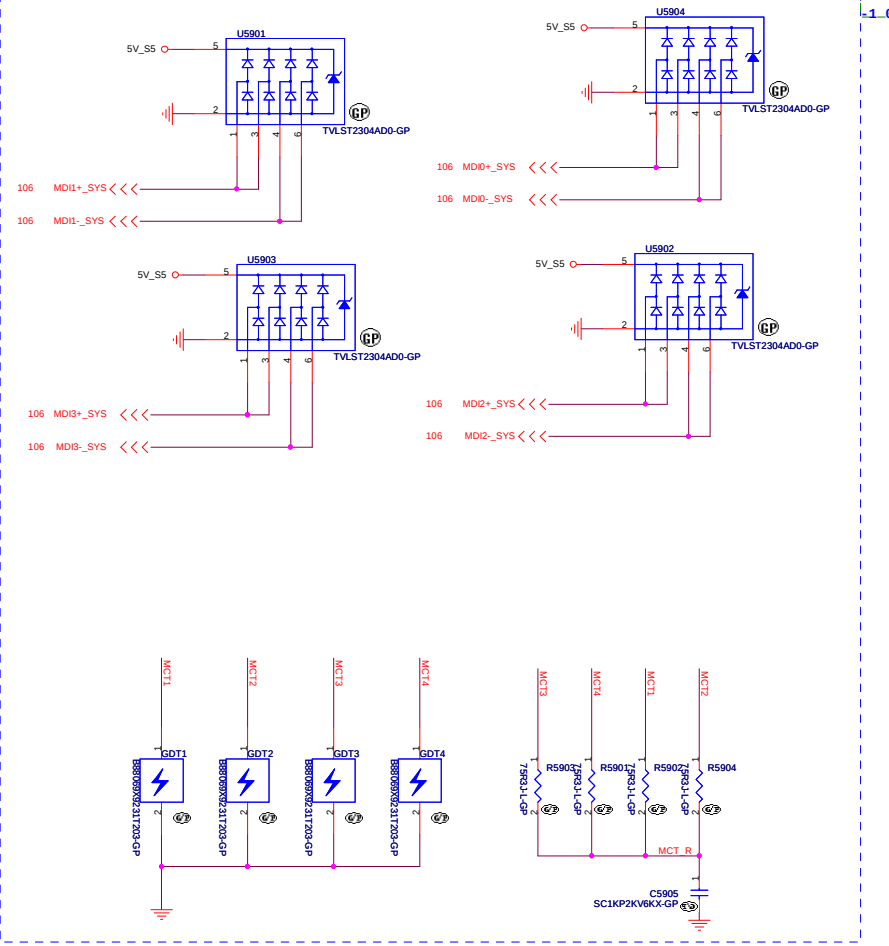
LED COLOR

10(+) 9(-)::GREEN
12(+) 13(-)::ORANGE





For EMI

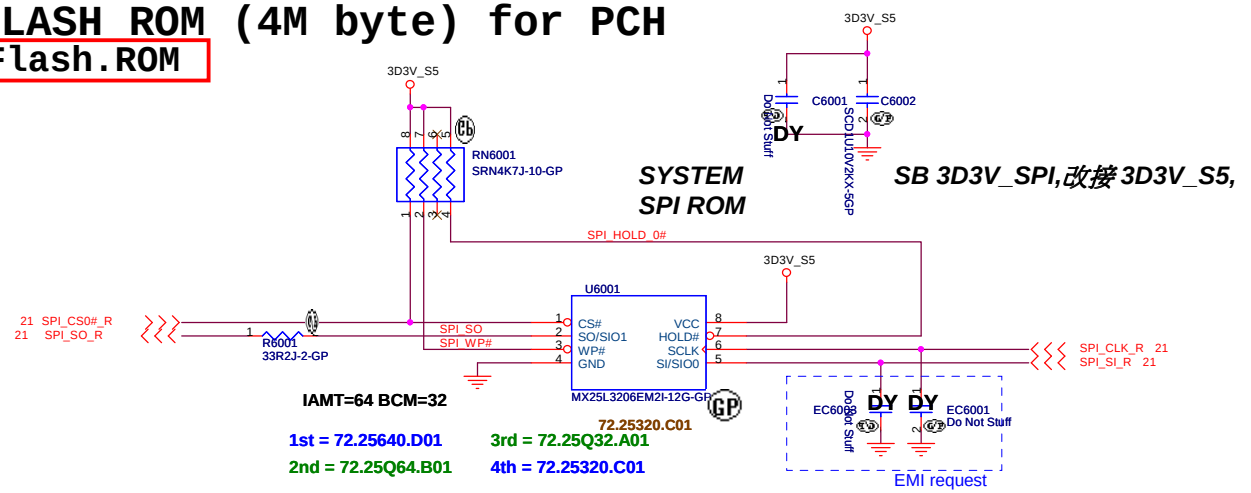


D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN CONNECTOR***	
Size: Custom	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 59 of 109	

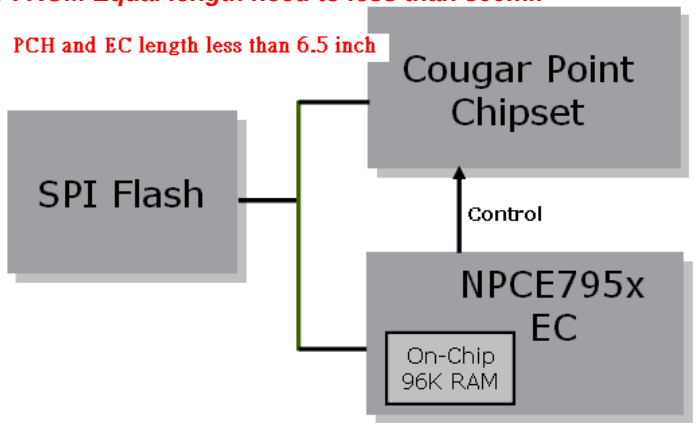
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

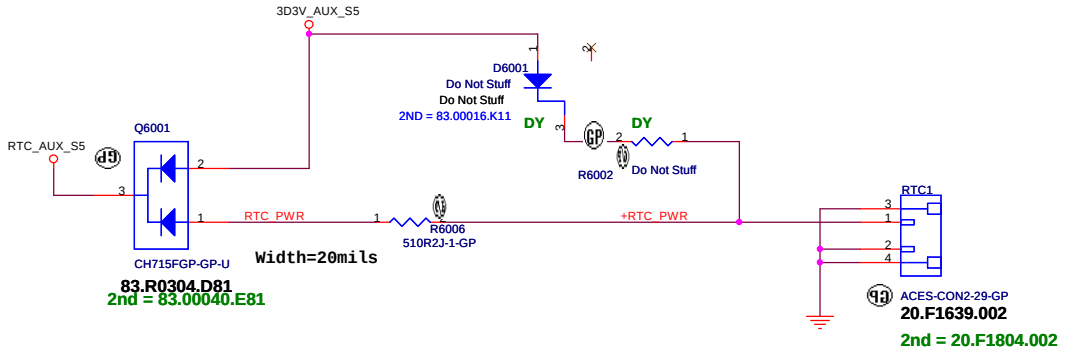


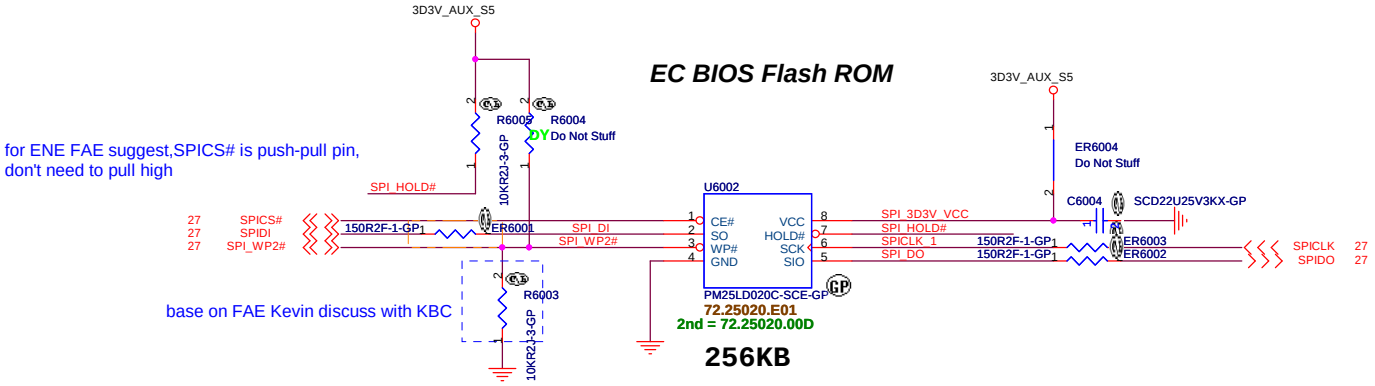
SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT





D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Flash/RTC***	
Size: Custom	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 60 of 109	

SSID = USB

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 61 of 109

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

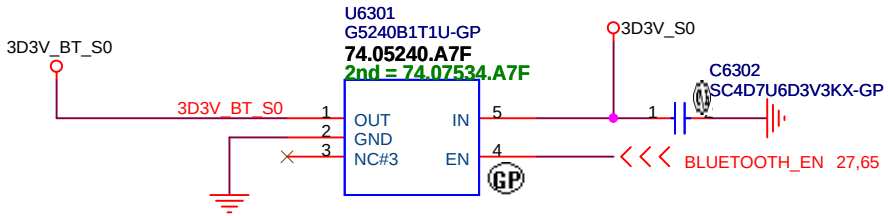
Title: ***USB 3.0 Port***

Size	Document Number	Rev
A3	**BA40-HR**	**SD**

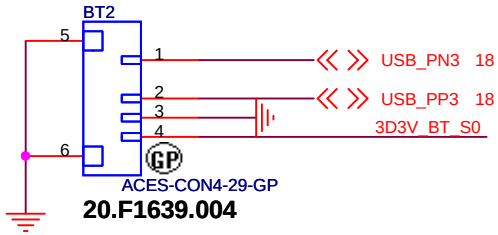
Date: Thursday, April 07, 2011 Sheet 62 of 109

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

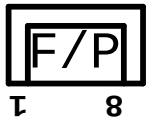
Title: ***Bluetooth***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 63 of 109

Finger printer

JE40 delete FP function

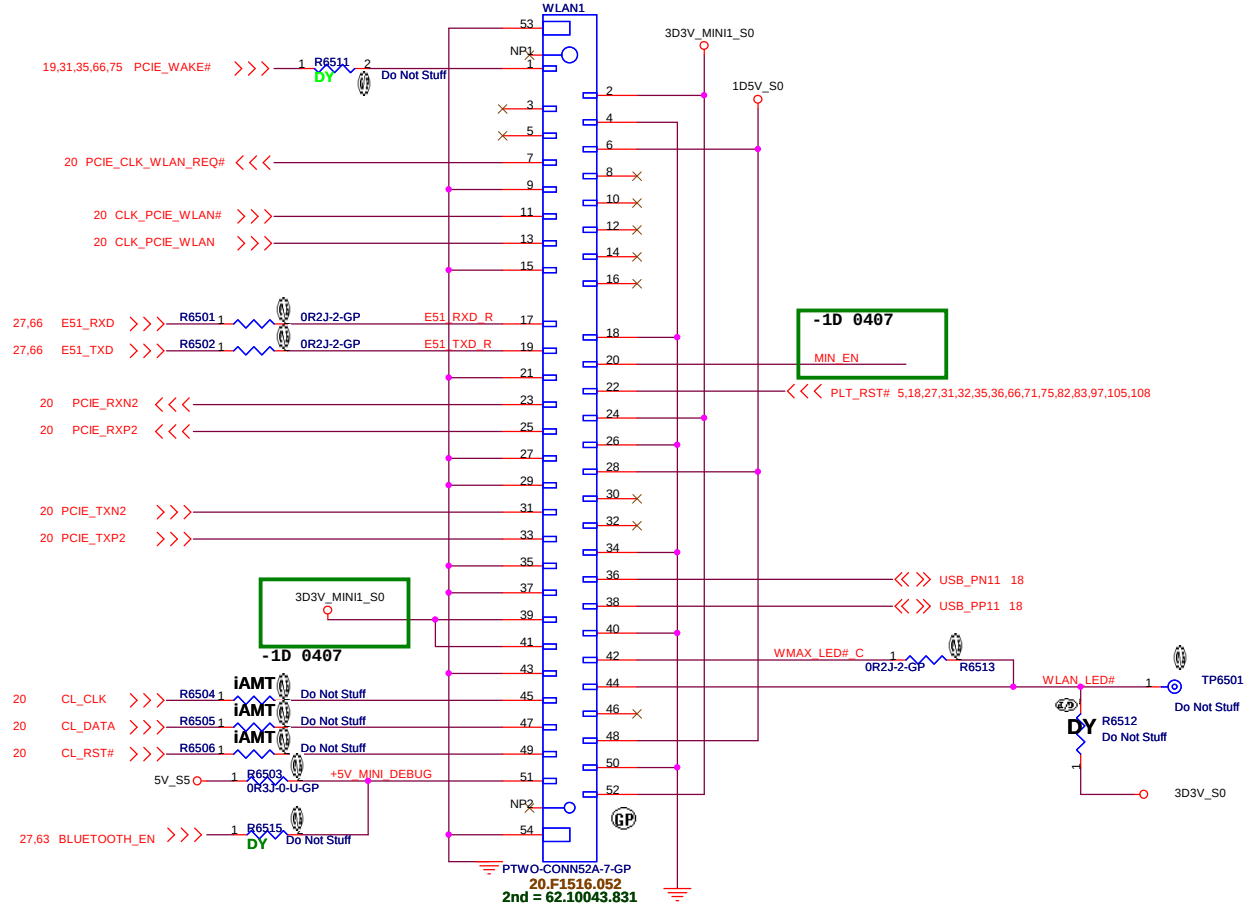


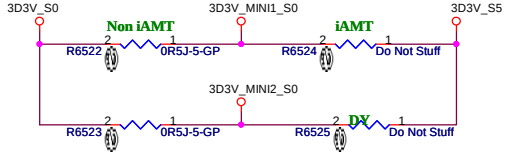
D12G

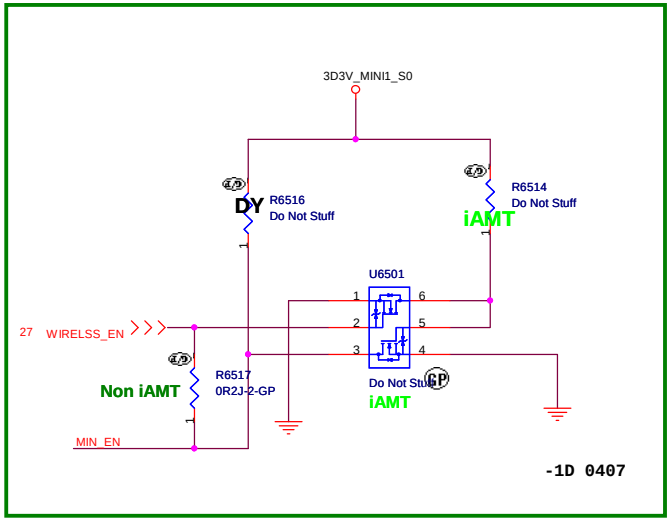
緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BA40-HR**	Rev: **SD**
Date: Thursday, April 07, 2011	Sheet 64 of 109	

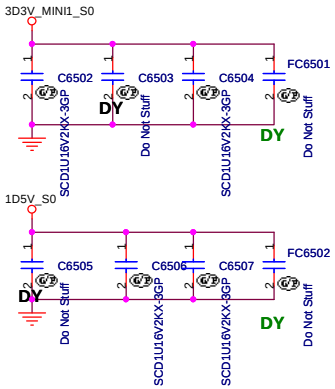
SSID = Wireless

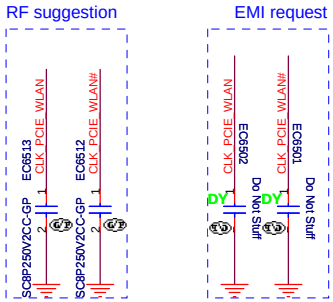
Mini Card Connector(802.11a/b/g/n)











D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
A3	BA40-HR	SD

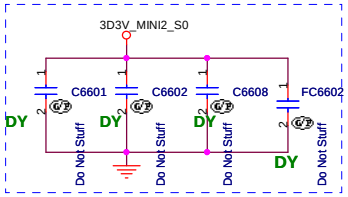
Date: Thursday, April 07, 2011 Sheet 65 of 109

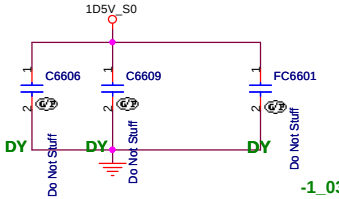
SSID = Wireless

20100712 V1.5

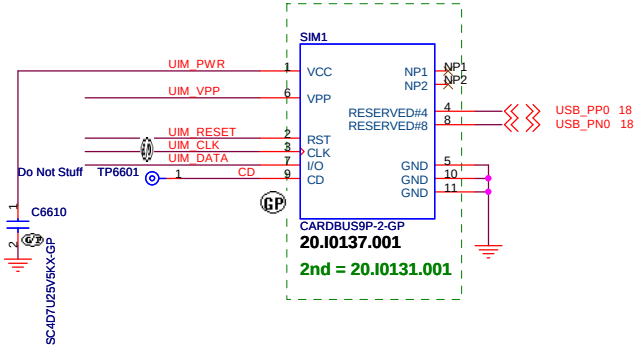
Place near MINI Card CONN

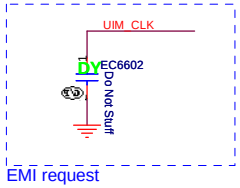
Mini Card Connector(WWAN)



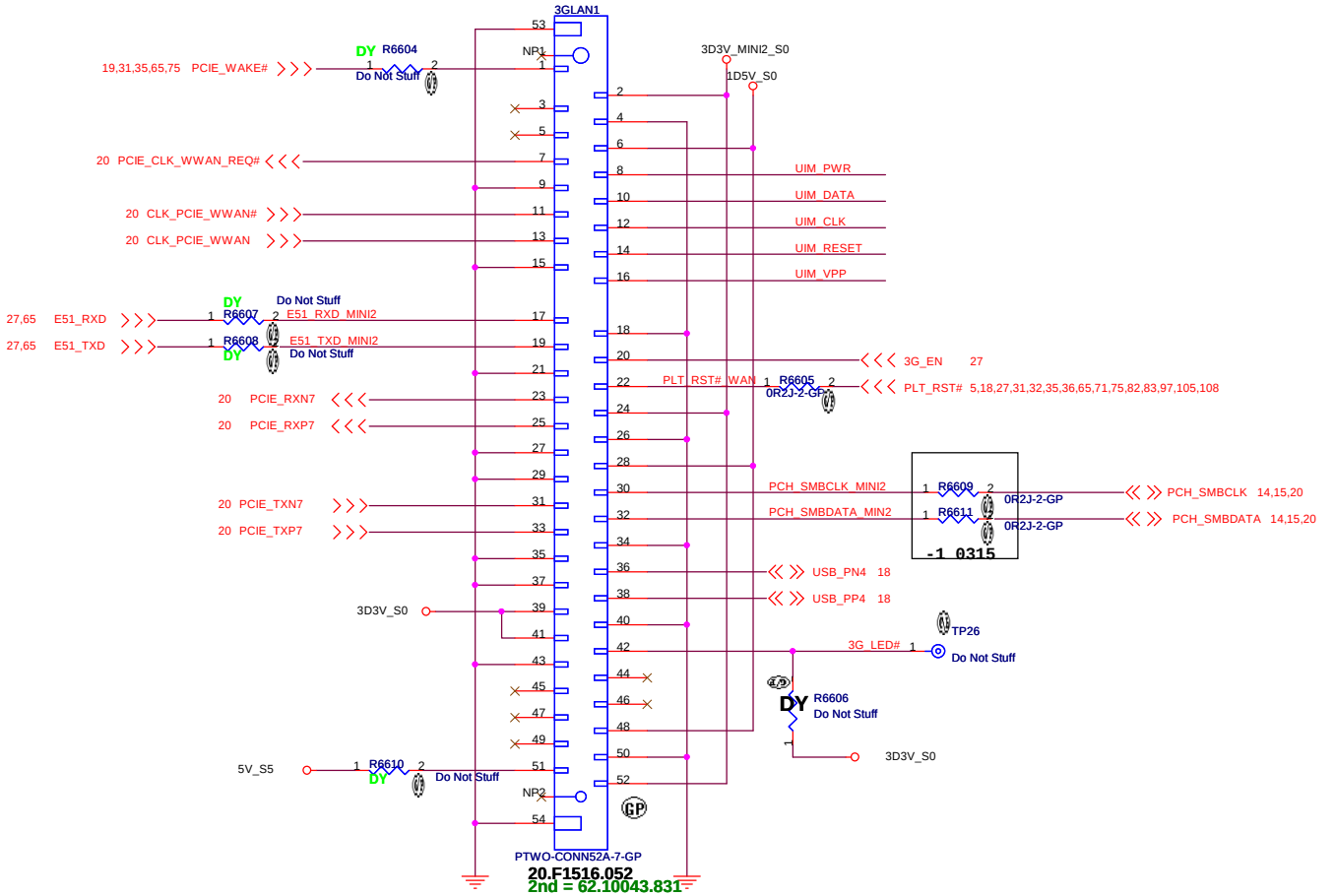


-1_0304





EMI request



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN Connector**

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 66 of 109

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

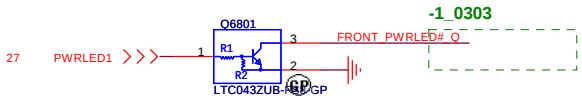
Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

Date: Thursday, April 07, 2011 Sheet 67 of 109

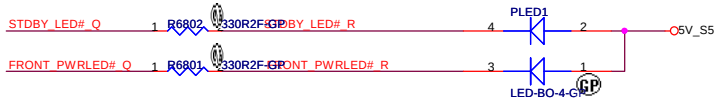
SSID = User.Interface

Power button LED

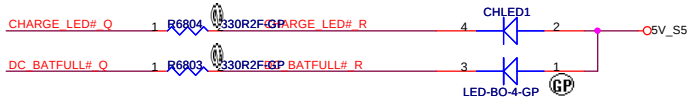


2nd = 84.05143.011

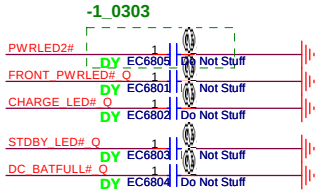
3rd = 84.00143.E1K



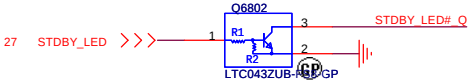
83.00195.G70



83.00195.G70



Power STDBY_LED



2nd = 84.05143.011

3rd = 84.00143.E1K

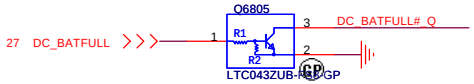
Caps Lock LED

2nd = 84.05143.011

3rd = 84.00143.E1K

83.00193.A70

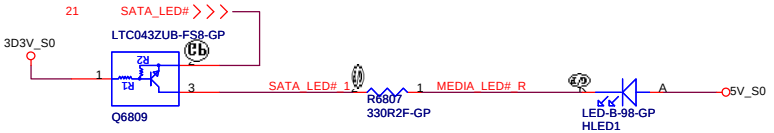
Battery LED2(DC_BATFULL)



2nd = 84.05143.011

3rd = 84.00143.E1K

SATA HDD LED

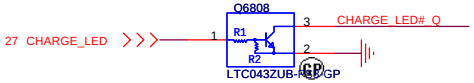


2nd = 84.05143.011

3rd = 84.00143.E1K

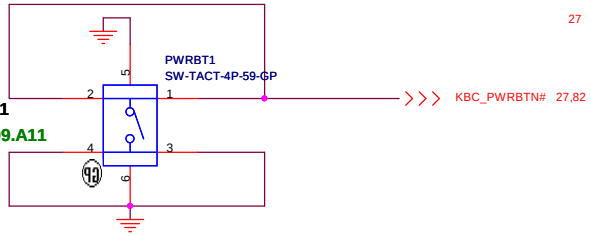
83.00193.A70

Battery LED1(CHARGE)



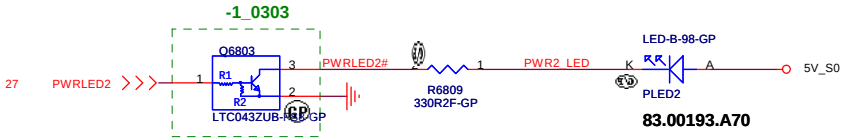
2nd = 84.05143.011

3rd = 84.00143.E1K



62.40009.E51

2nd = 62.40009.A11



2nd = 84.05143.011

3rd = 84.00143.E1K

83.00193.A70

for factory test

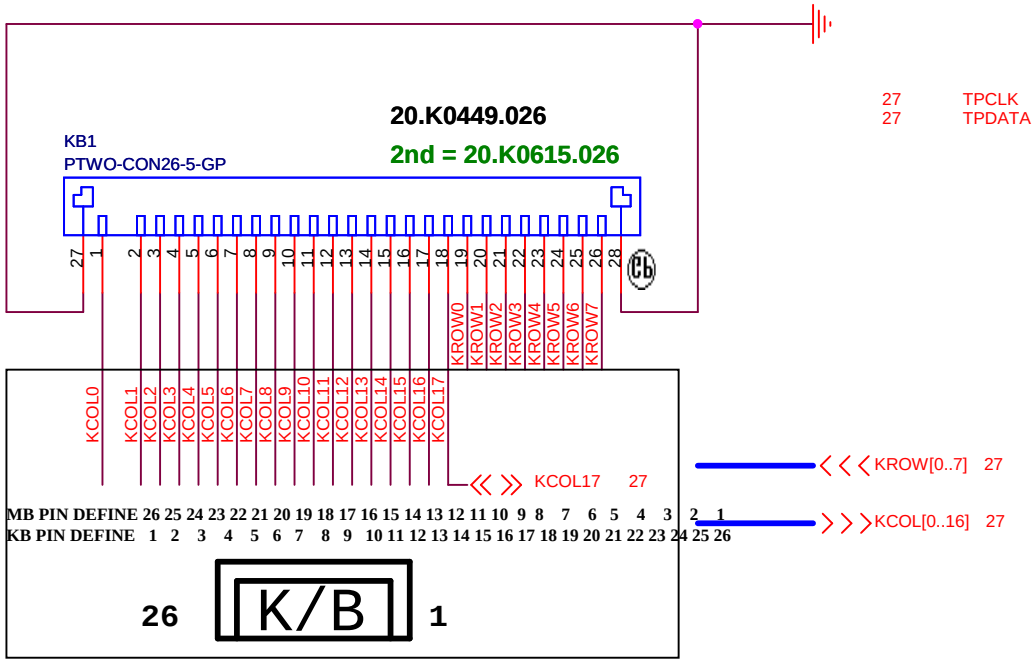
D12G

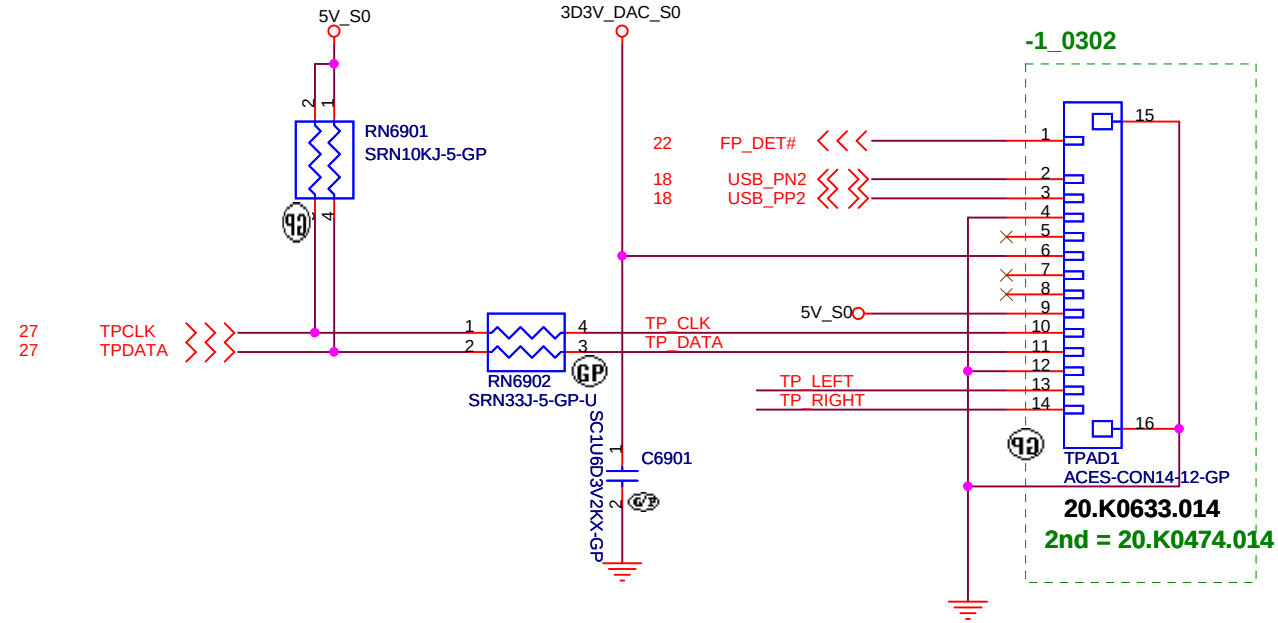
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED Bard/Power Button		
Size: Custom	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 68 of 109	

TOUCH PAD

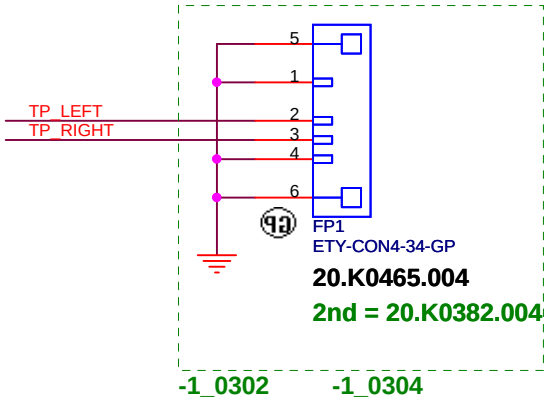
SSID = KBC

Internal KeyBoard Connector





Rubber Dome



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A4	BA40-HR	SD

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D12G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

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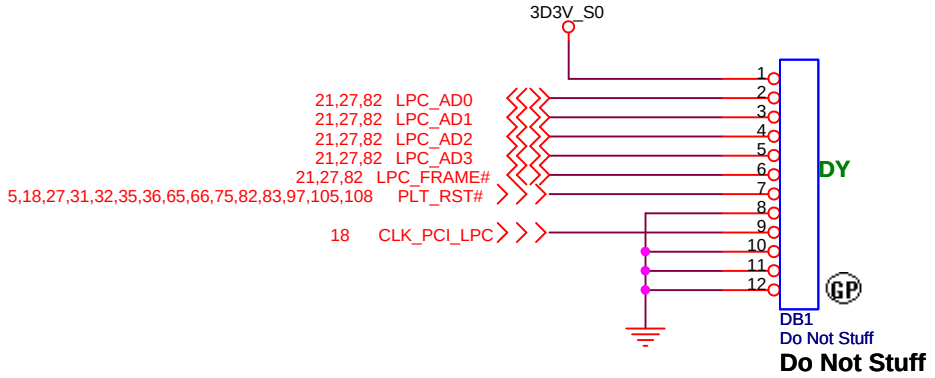
SB modify to test pad



Do Not Stuff

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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D12G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BA40-HR	SD

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A3	Document Number: **BA40-HR**	Rev: **SD**
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SD/XD/MS Card Reader

SSID = SDIO

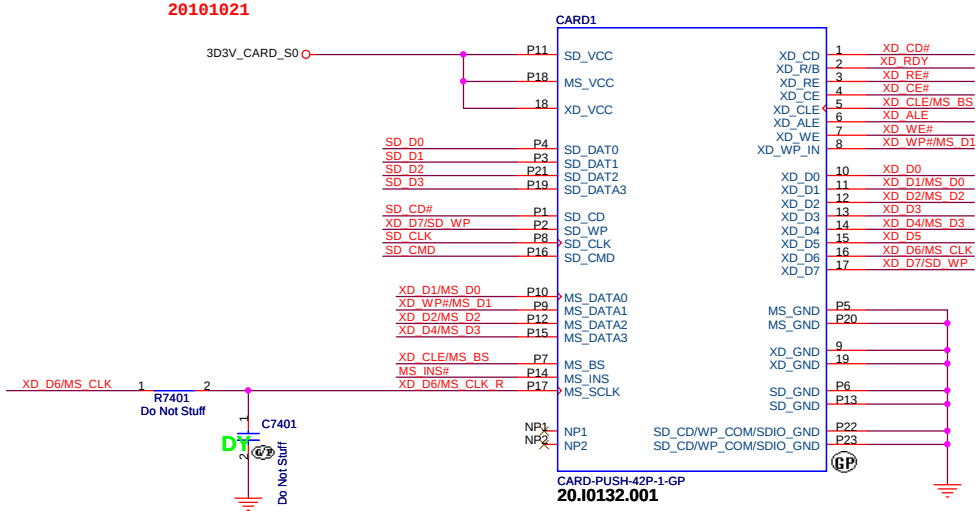
32 XD_CD#
32 SD_D1
32 SD_D0
32 SD_D2
32 SD_D3

32 SD_CLK
32 SD_CMD

32 SD_CD#
32 MS_INS#

32	XD_RDY	SP1(N0 SD_D7)
32	XD_RE#	SP2(NO SD_D6)
32	XD_CE#	SP3(NO_SD_D5)
32	XD_WE#	SP4(No SD_D4)
32	XD_CLE/MS_BS	SP5
32	XD_ALE	SP6
32	XD_WP#/MS_D1	SP7
32	XD_D0	SP8(NO MS_D4)
32	XD_D1/MS_D0	SP9
32	XD_D2/MS_D2	SP10
32	XD_D3	SP11(MS_D6)
32	XD_D4/MS_D3	SP12
32	XD_D5	SP13
32	XD_D6/MS_CLK	SP14
32	XD_D7/SD_WP	SP15

20101021



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

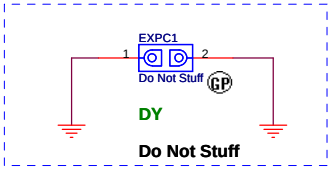
Title: **CARD Reader CONN**

Size	Document Number	Rev
A3	BA40-HR	SD

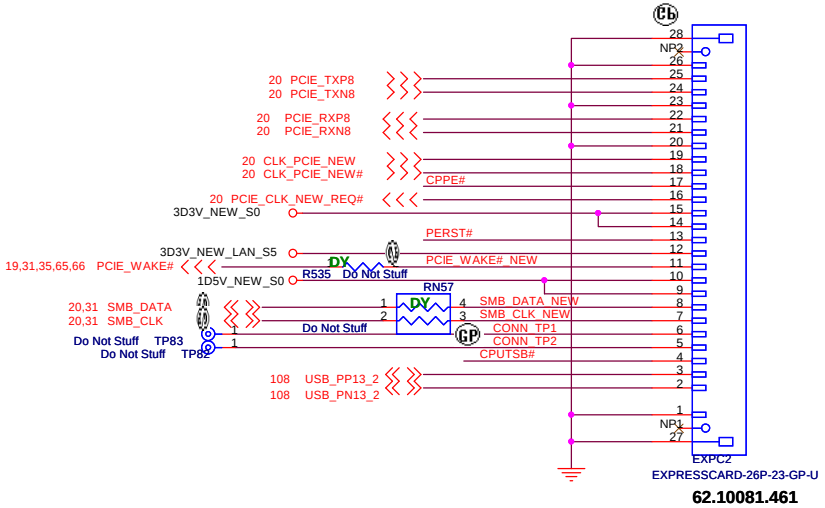
Date: Thursday, April 07, 2011 Sheet 74 of 109

SSID = ExpressCard

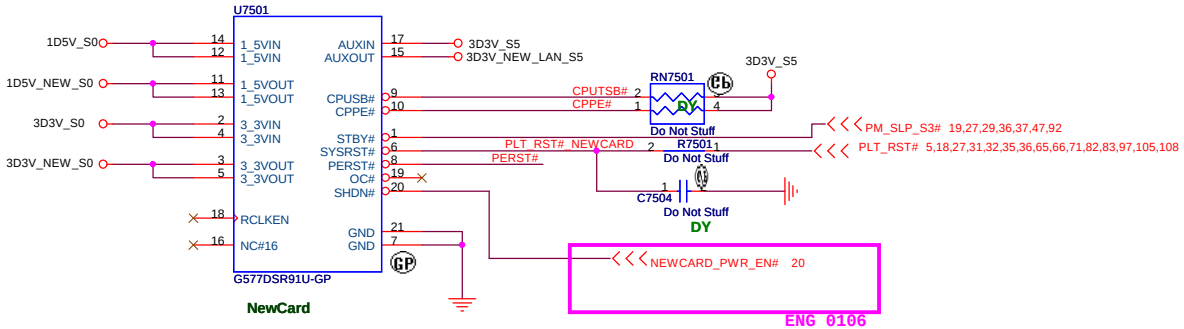
For Expresscard socket



+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

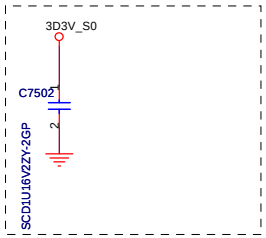


62.10081.461

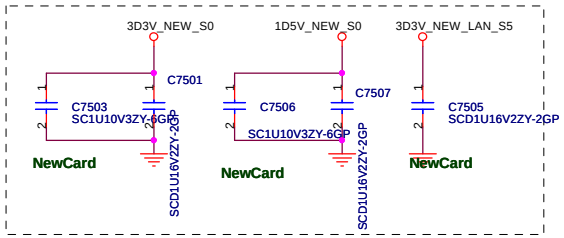


ENG 0106

Place them Near to Chip



Place them Near to Connector



For EMI

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: BA40-HR | Rev: SD

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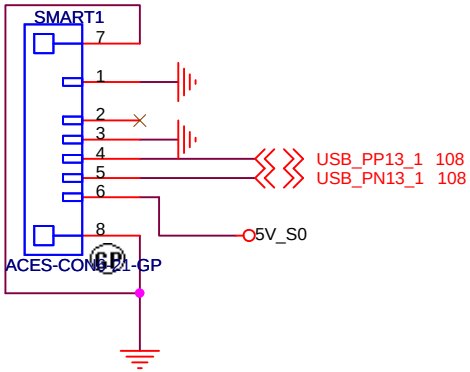

20.K0473.006
2nd = 20.K0392.006

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**BA40-HR**	**SD**

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D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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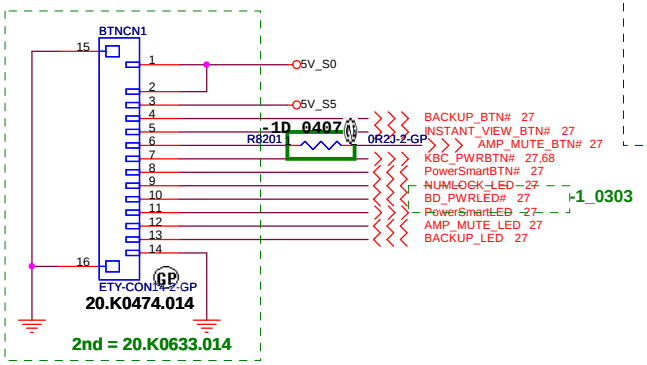
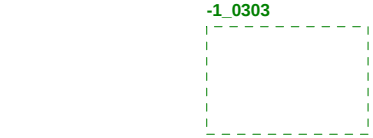
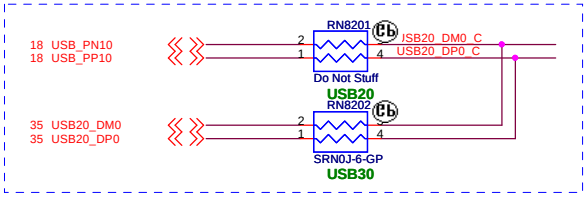
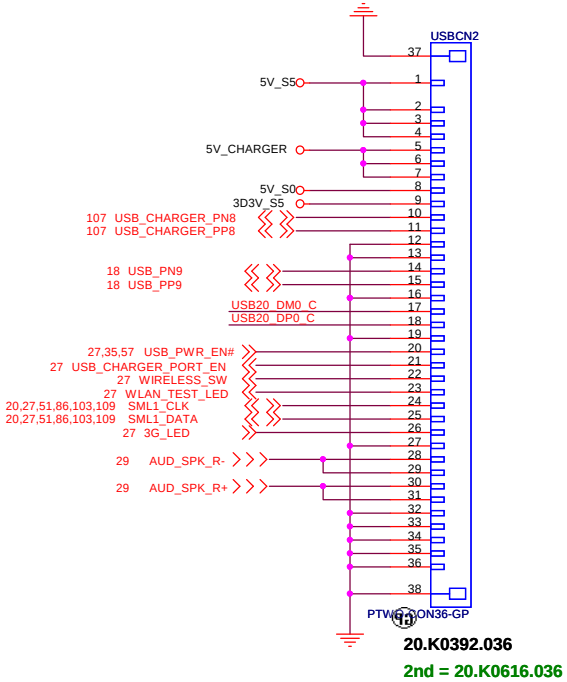
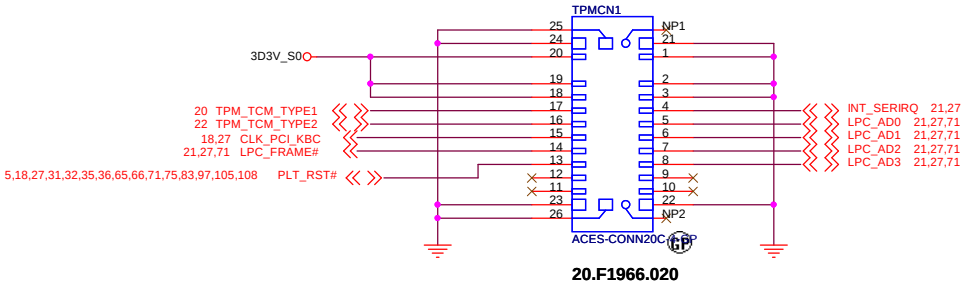
PWRCN1 FFC 異面

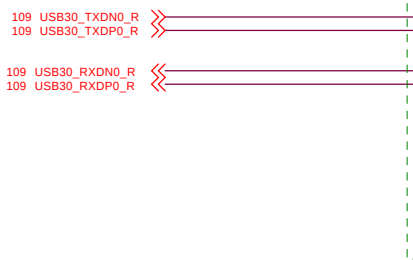


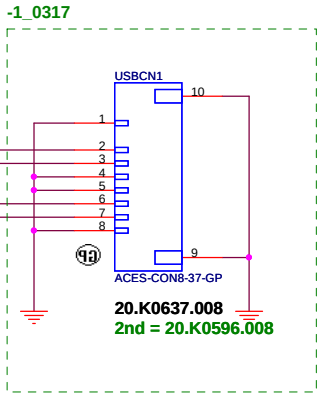






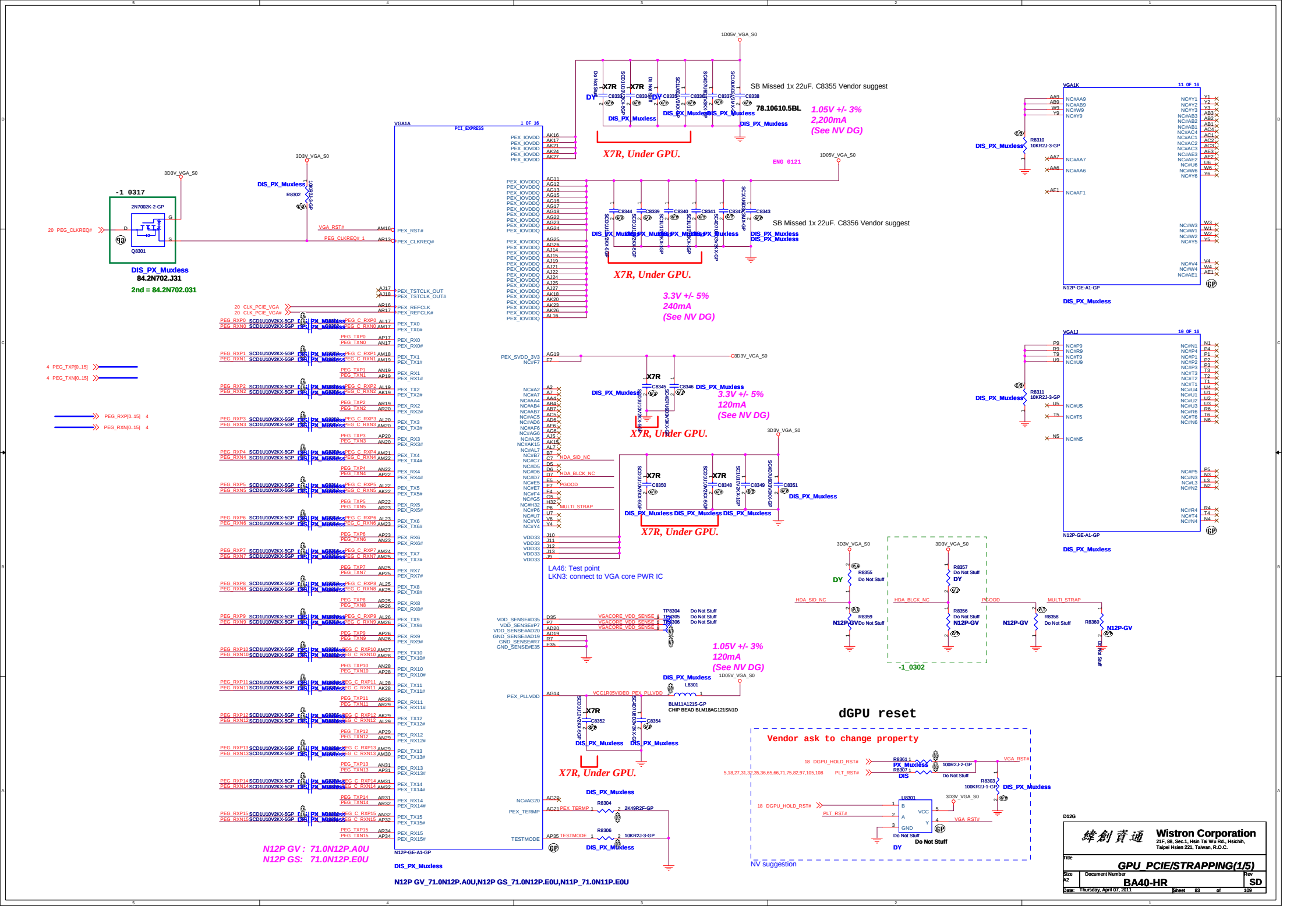






D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *IO Board Connector*		
Size: A3	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 82 of 109	


VGA1A
PCI_EXPRESS
1 OF 16
N12P-GE-A1-GP
DIS_PX_Muxless
1D05V_VGA_S0
3D3V_VGA_S0
SB Missed 1x 22uF. C8355 Vendor suggest
78.10610.5BL
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
ENG 0121
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
3.3V +/- 5%
120mA
(See NV DG)
LA46: Test point
LKN3: connect to VGA core PWR IC
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N12P GV_71.0N12P.A0U,N12P GS_71.0N12P.E0U,N11P_71.0N11P.E0U
dGPU reset
Vendor ask to change property
NV suggestion
-1 0317
-1_0302
2N7002K-2-GP
Q8301
84.2N702.J31
2nd = 84.2N702.031
VGA1K
11 OF 16
VGA1J
10 OF 16
Wistron Corporation
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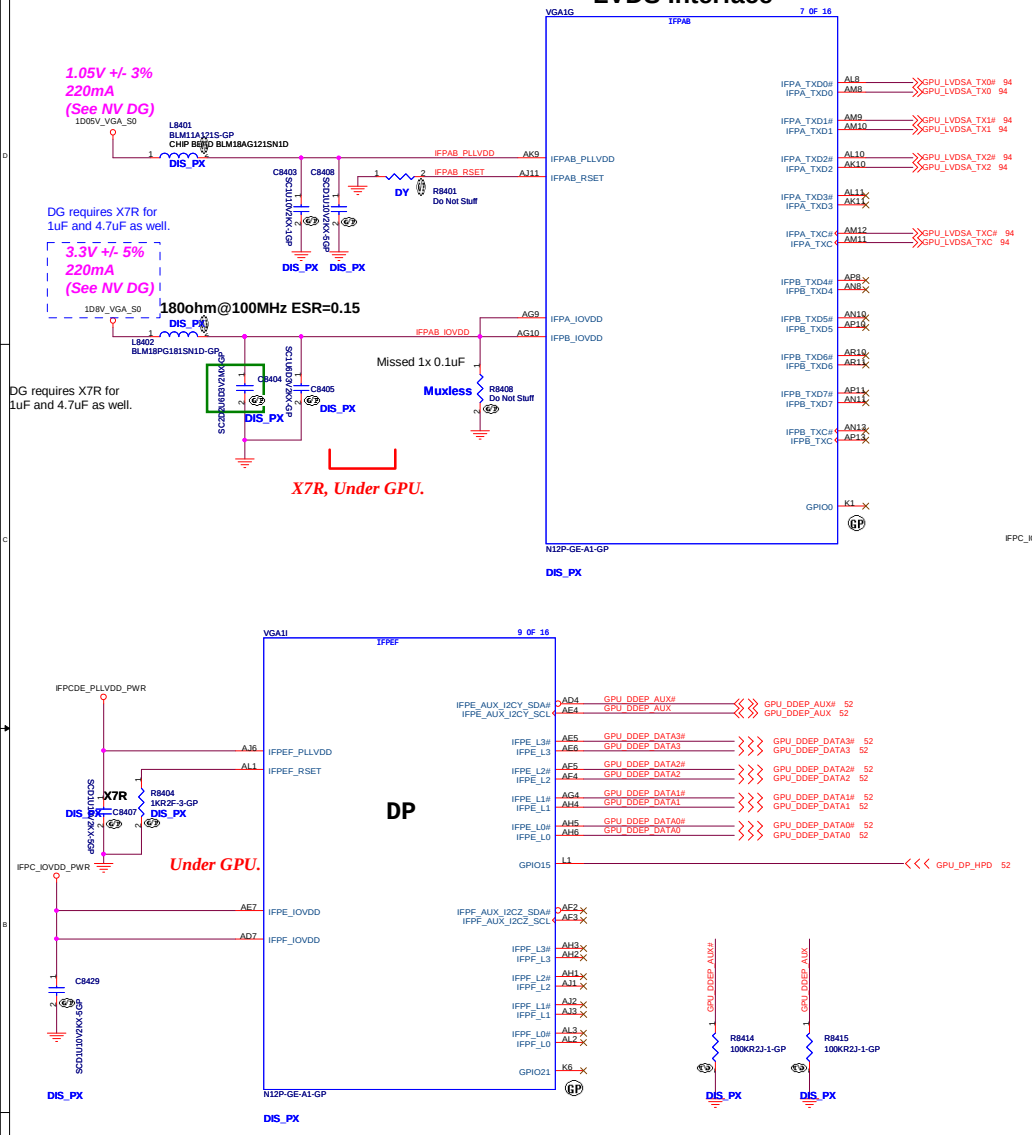
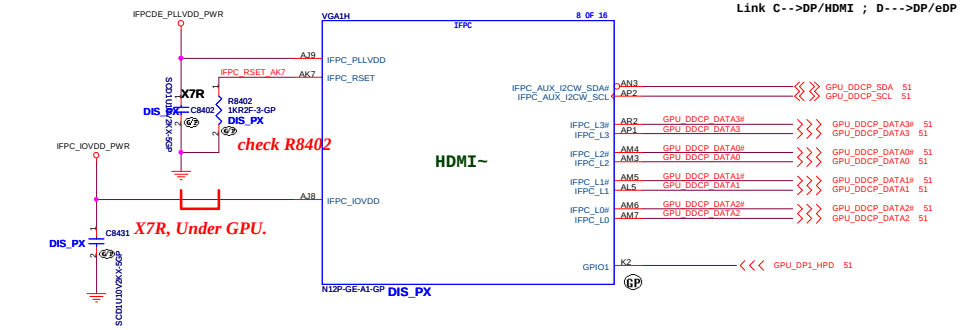
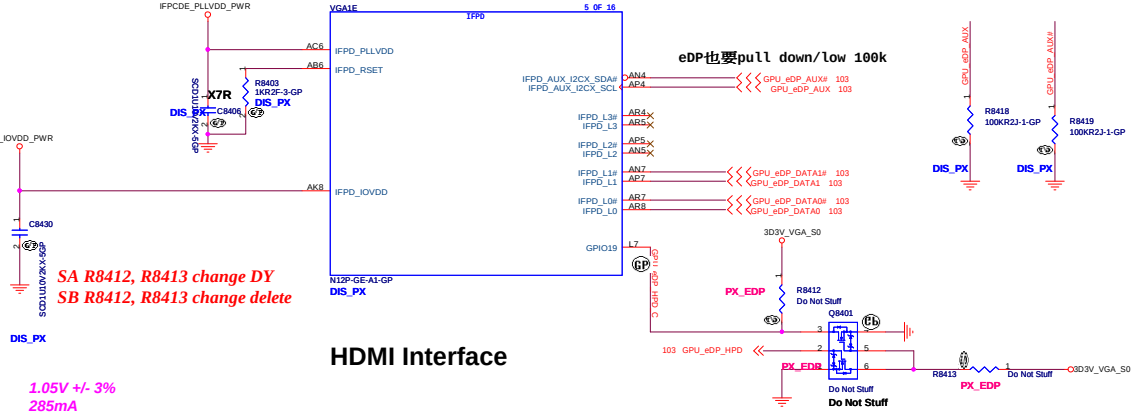
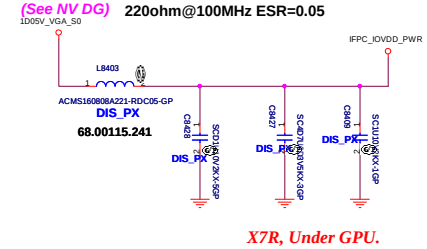
Title
GPU_PCIE/STRAPPING(1/5)
Size A2
Document Number BA40-HR
Rev SD
Date: Thursday, April 07, 2011
Sheet 83 of 109

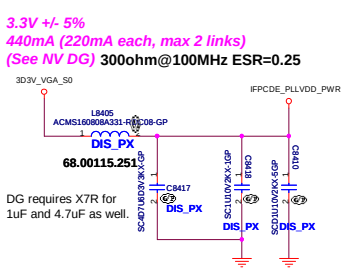
LVDS Interface











Link C-->DP/HDMI ; D--->DP/eDP ; E--->

D12G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU Memory(2/5)	
Size A2	Document Number BA40-HR	Rev SD
Date: Thursday, April 07, 2011	Sheet 84 of 109	

EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Group A

Group B

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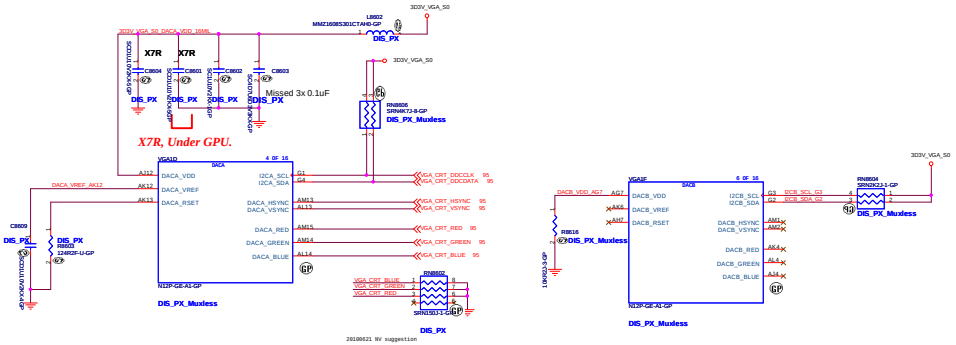
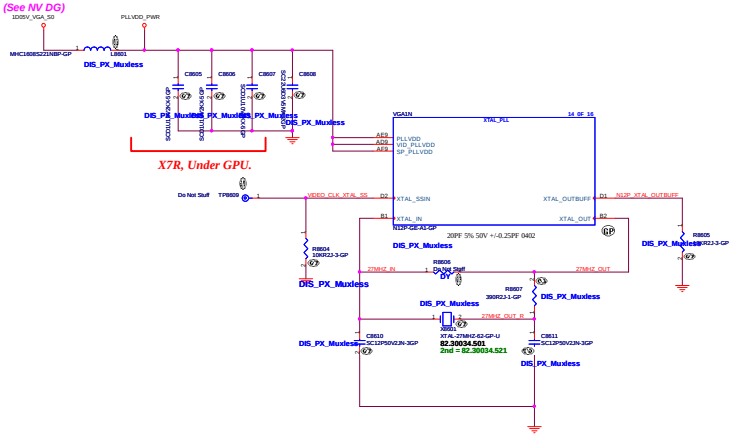
Title	GPU_DP/LVDS/CRT/GPIO(3/5)
Size: Custom	Document Number: BA40-HR
Rev	SD
Date: Thursday, April 07, 2011	Sheet 85 of 109

300ohm@100MHz ESR=0.25ohm

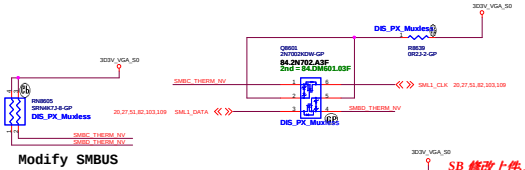
3.3V +/- 5%
120mA
(See NV DG)

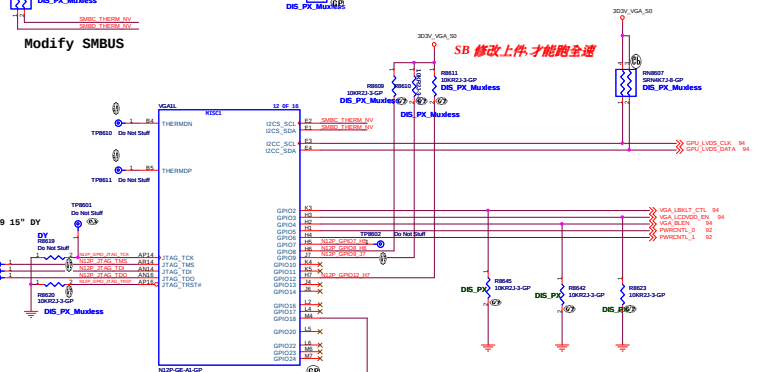


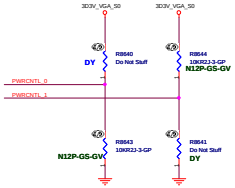
1.05V +/- 3%
150mA
(See NV DG)



VGA Thermal sensor P2800





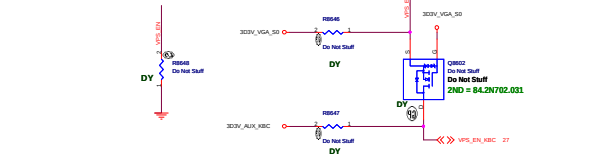


N12P-GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.825V
	H	L	0.9V
	L	H	0.975V
	H	H	1V

← default boot voltage table

Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
64Mx16 DDR3	Hynix	0x2	H5TQ1G63DFR-11C	900/800
	Samsung	0x3	K4W1G1646E-HC11	900
	Samsung	TBD	K4W1G1646G-BC11	900/800
	Hynix	0x0	H5TQ1G63BFR-12C	800
	Samsung	0x1	K4W1G1646E-HC12	800



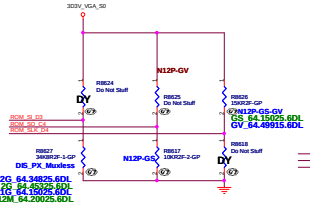
NVIDIA TABLE

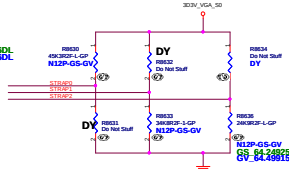
	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

TABLE NVIDIA 71.0N12P.E0U 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL
	N12P-GS USE 1111 (45K)	N12P-GV	N11P-GE Pull Low	N11P-GS Pull Low	N12P-GE

	ROM_SI	ROM_SO	ROM_CLK	STRAP0	STRAP1	STRAP2
N12P_GS		PL 10K ohm	PH 15K ohm	PH 45K ohm	PL 35K ohm	PL 25K ohm
N12P_GV		PH 10K ohm	PH 5K ohm	PH 45K ohm	PL 35K ohm	PL 5K ohm





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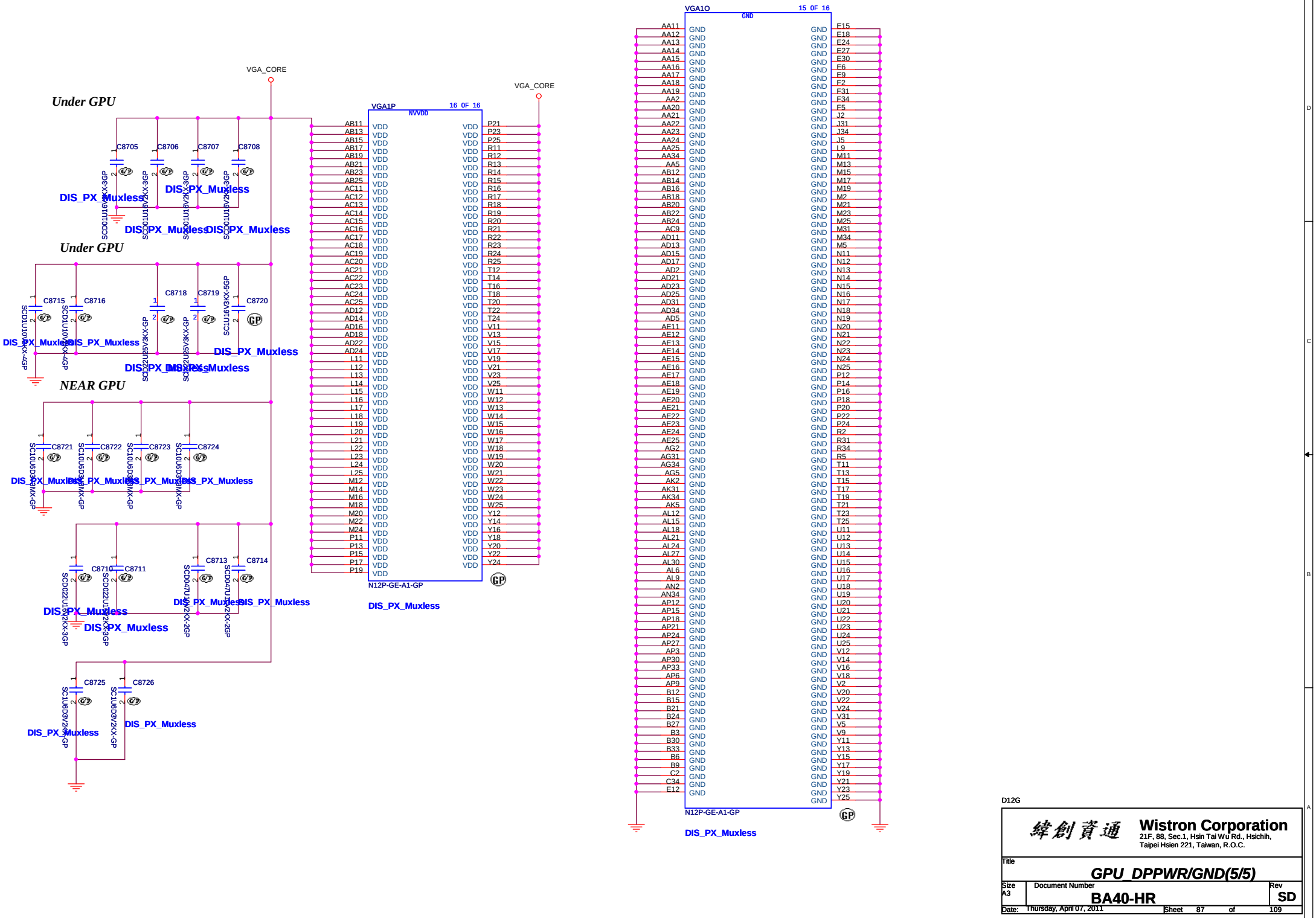
File: GPU_POWER(4/5)

Size: X1 | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 85 of 109



D12G

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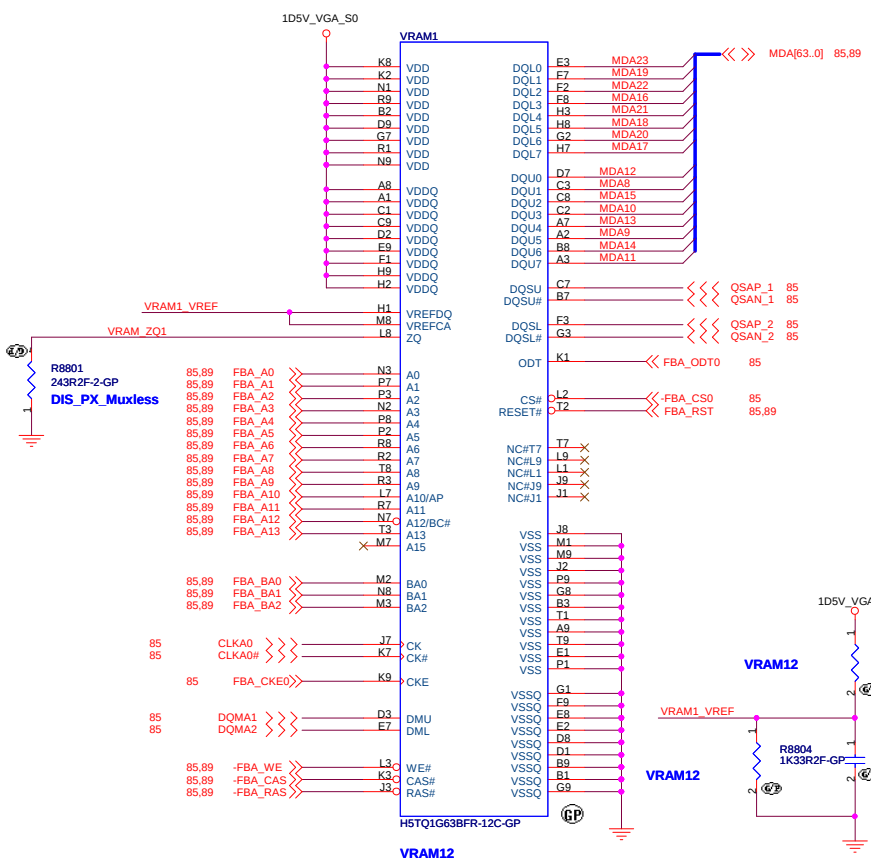
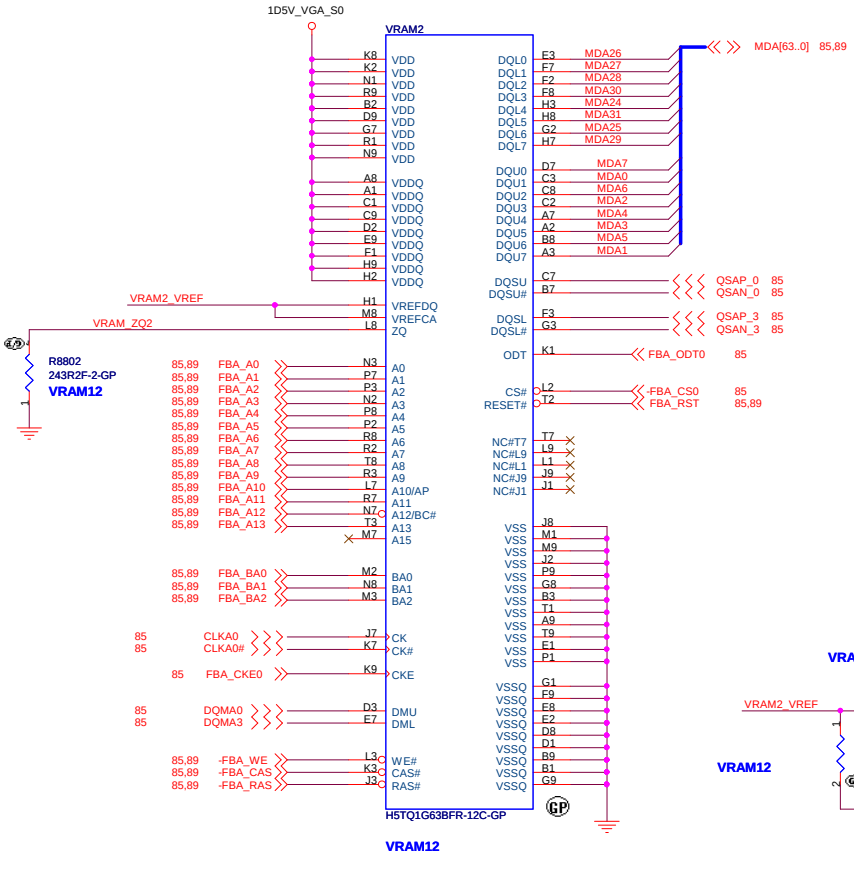
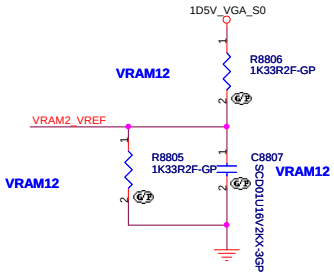
Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A3	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 87 of 109







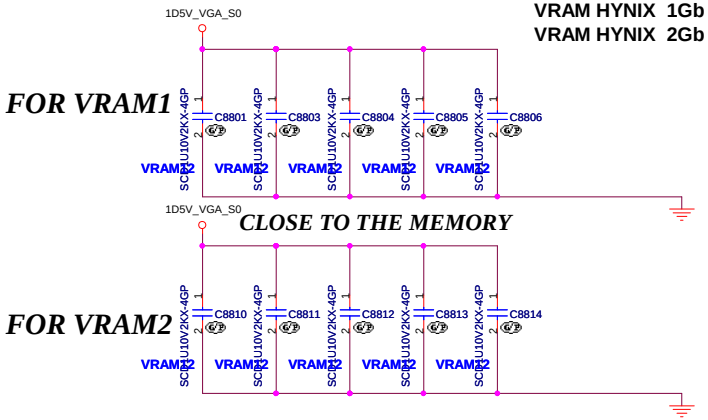
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

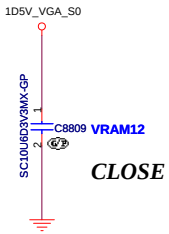
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip





CLOSE TO THE MEMORY

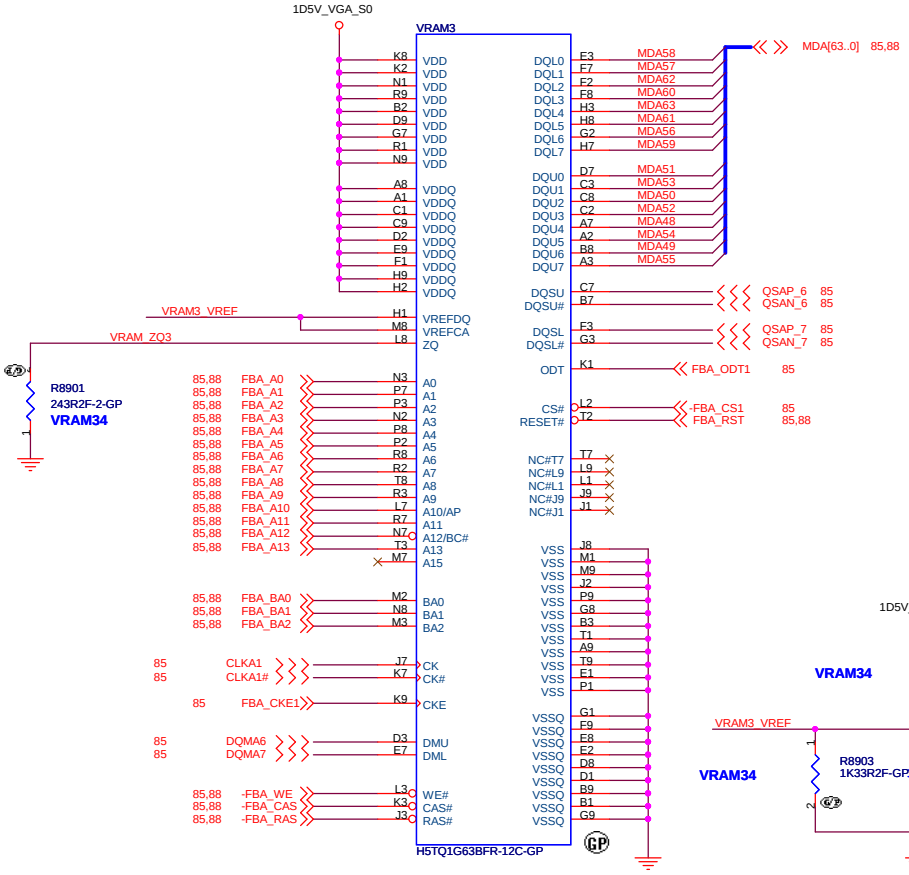
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

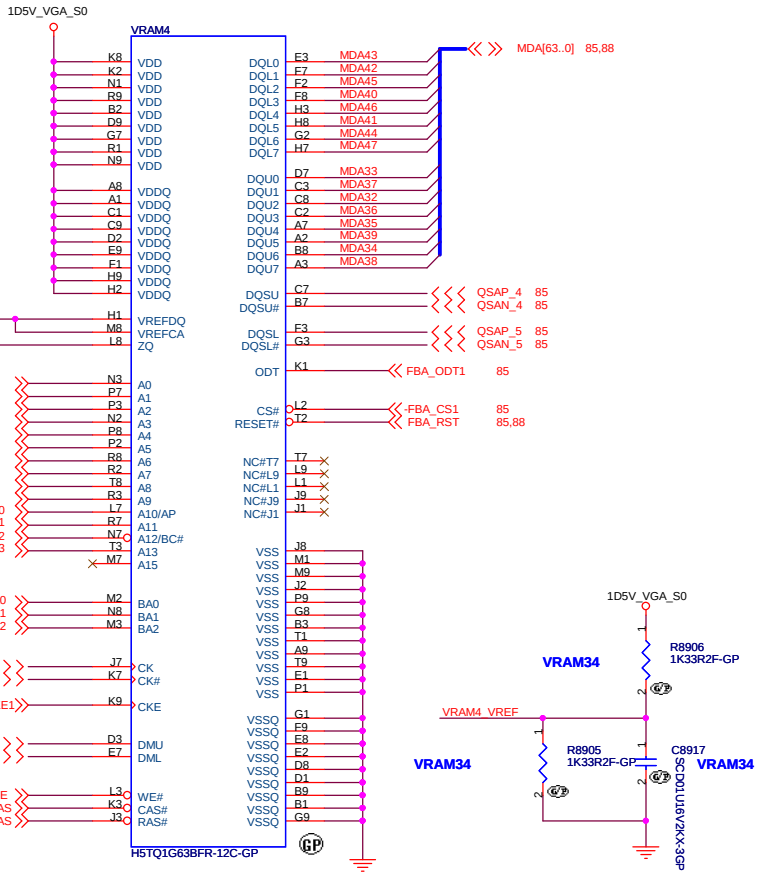
Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	BA40-HR	SD

Date: Thursday, April 07, 2011 Sheet 88 of 109



VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

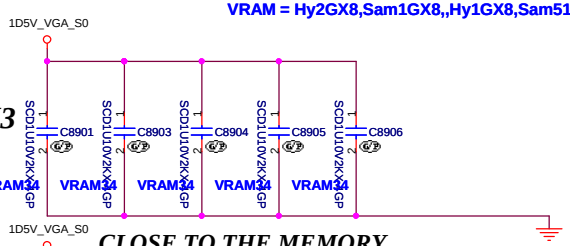


VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

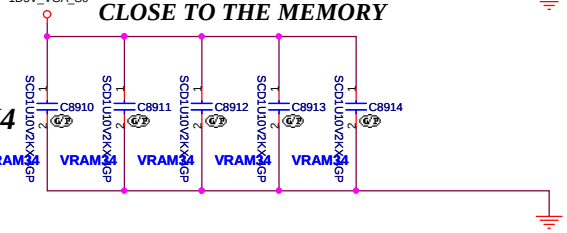
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

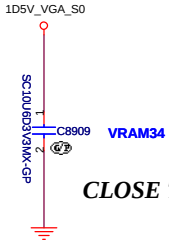
FOR VRAM3



CLOSE TO THE MEMORY

FOR VRAM4

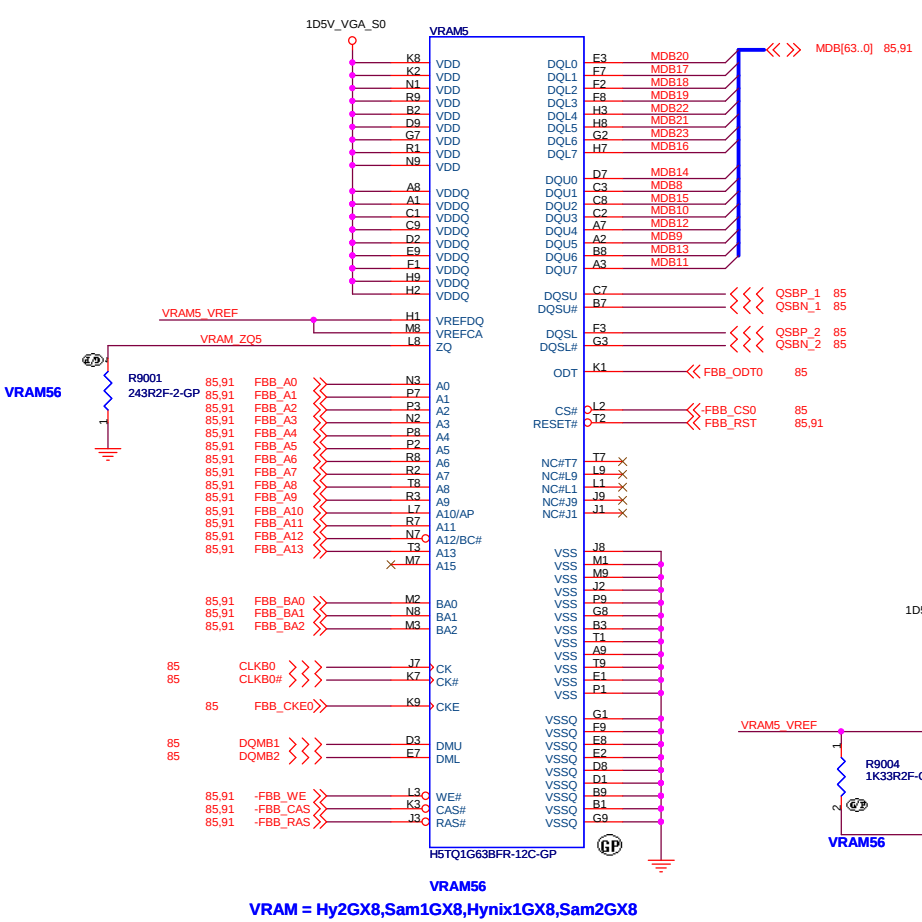




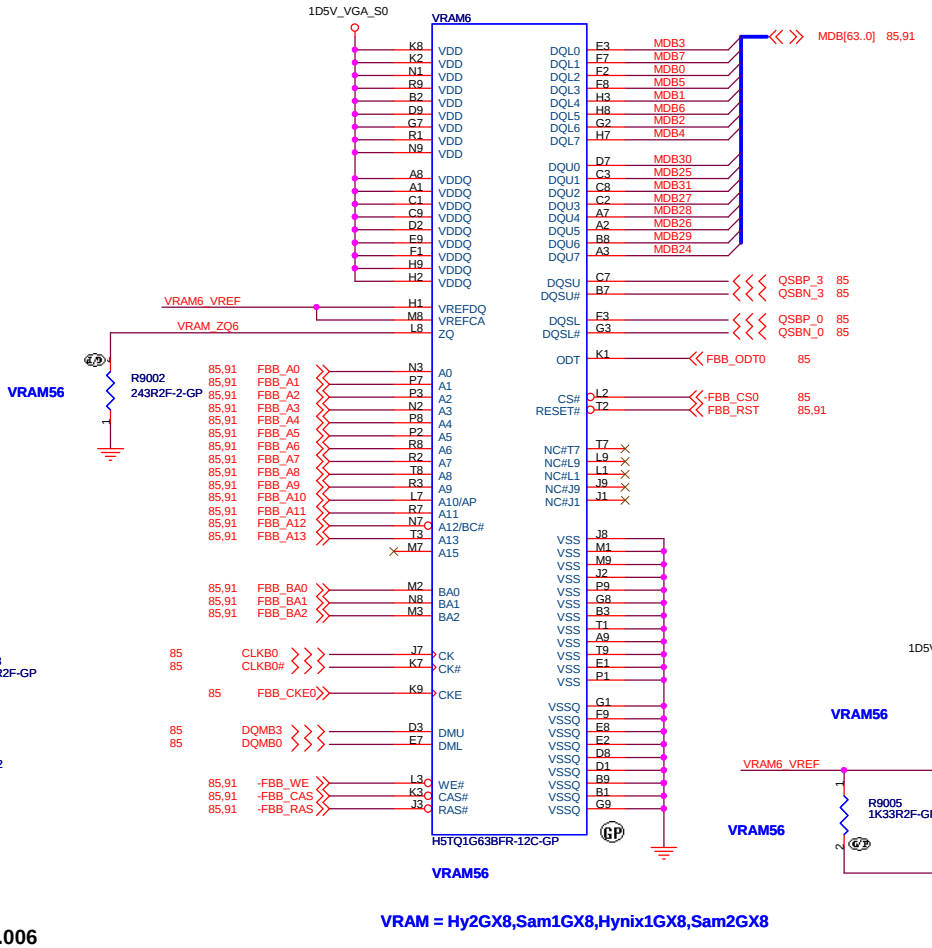
CLOSE TO THE MEMORY

D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU-VRAM3,4 (2/4)*		
Size: Custom	Document Number: BA40-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 89 of 109	

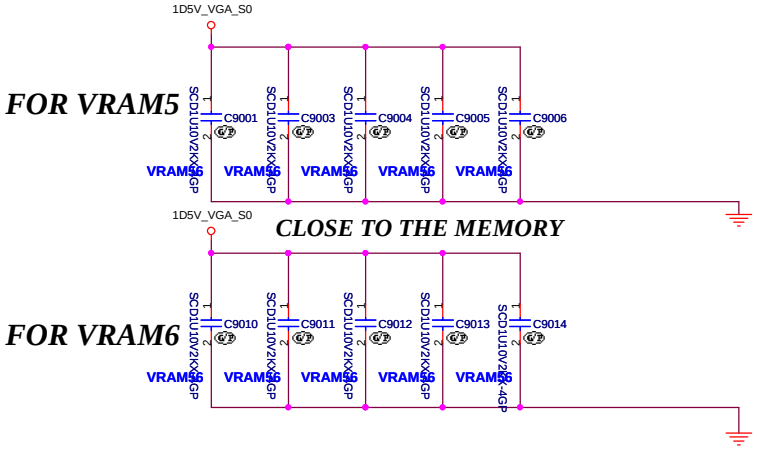


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

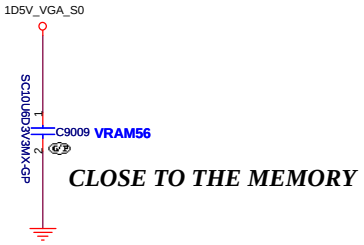


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



D12G

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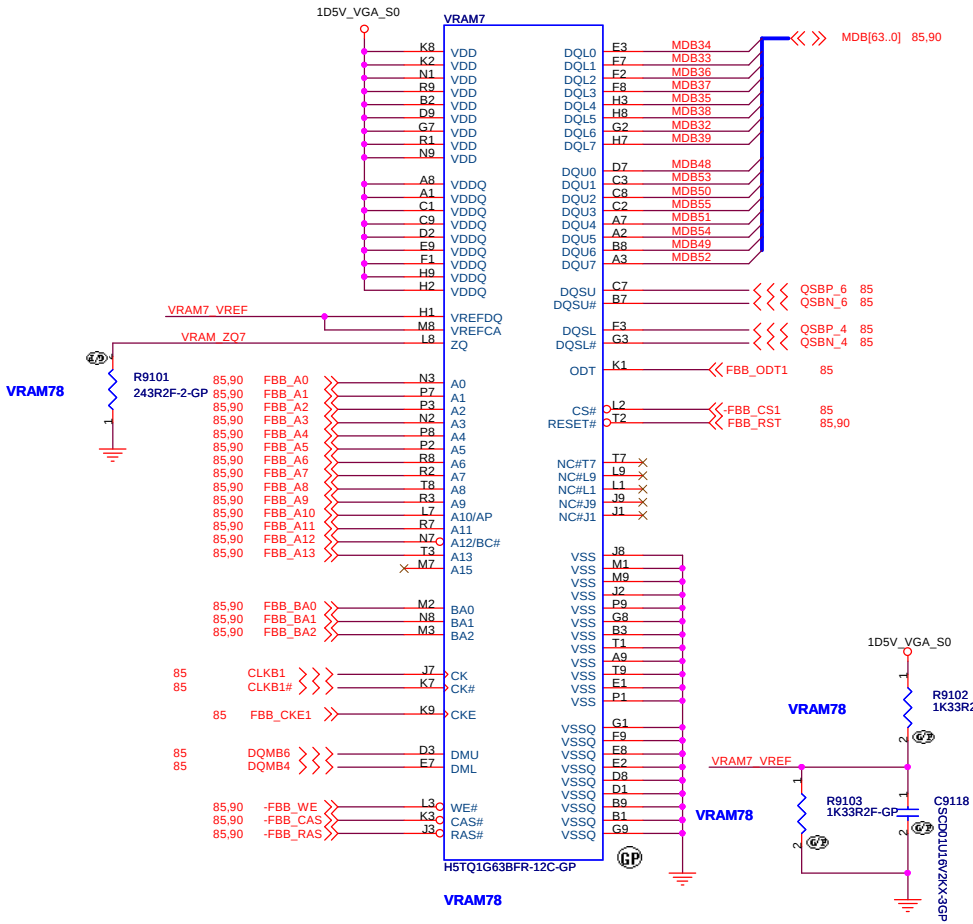
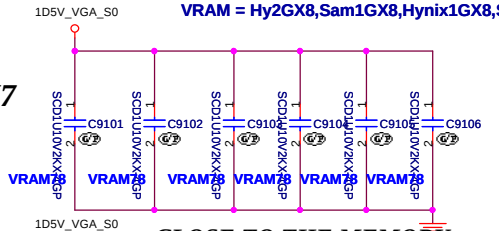
Title: GPU-VRAM5,6 (3/4)

Size: Custom | Document Number: BA40-HR | Rev: SD

Date: Thursday, April 07, 2011 | Sheet 90 of 109

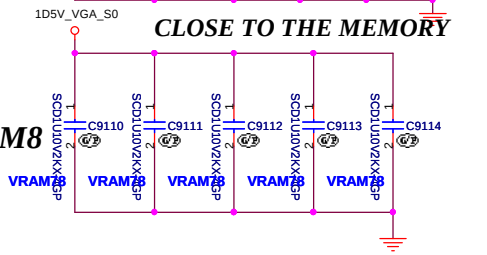


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

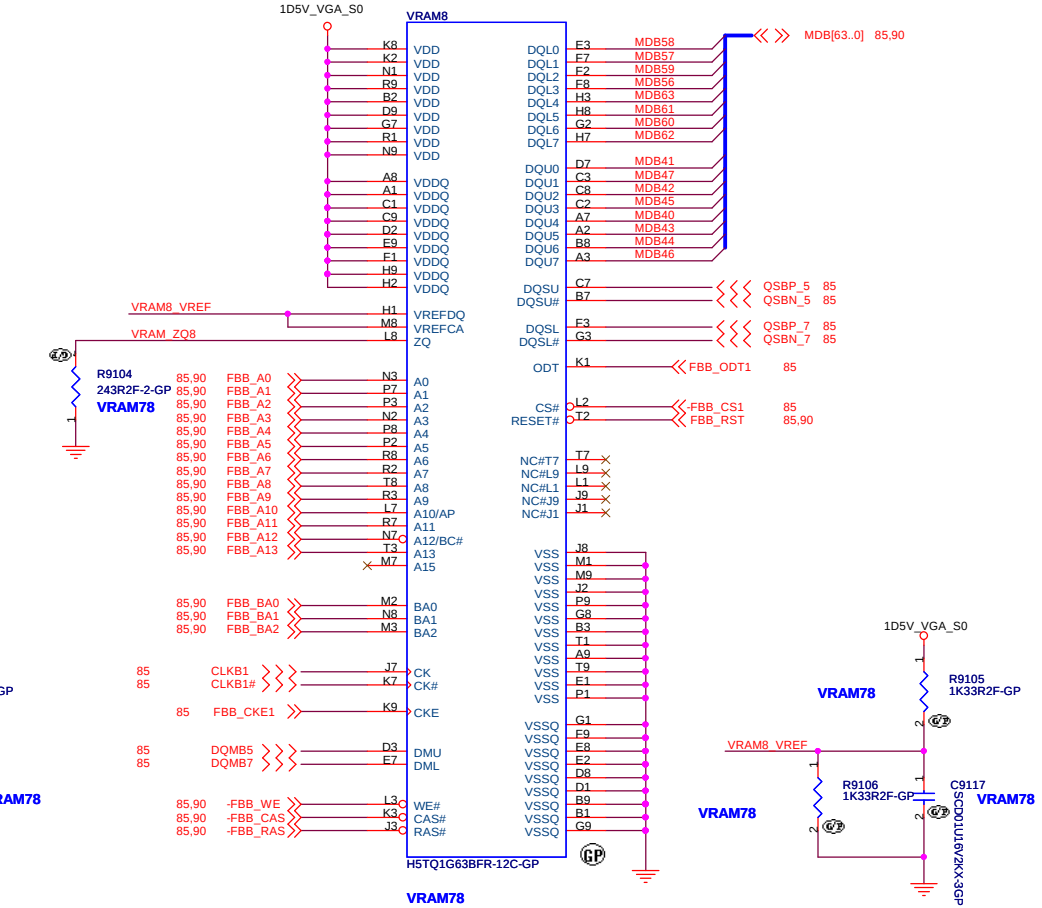


FOR VRAM7

CLOSE TO THE MEMORY



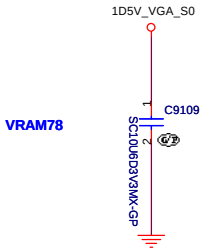
FOR VRAM8



VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

CLOSE TO THE MEMORY



D12G

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
Custom	BA40-HR	SD

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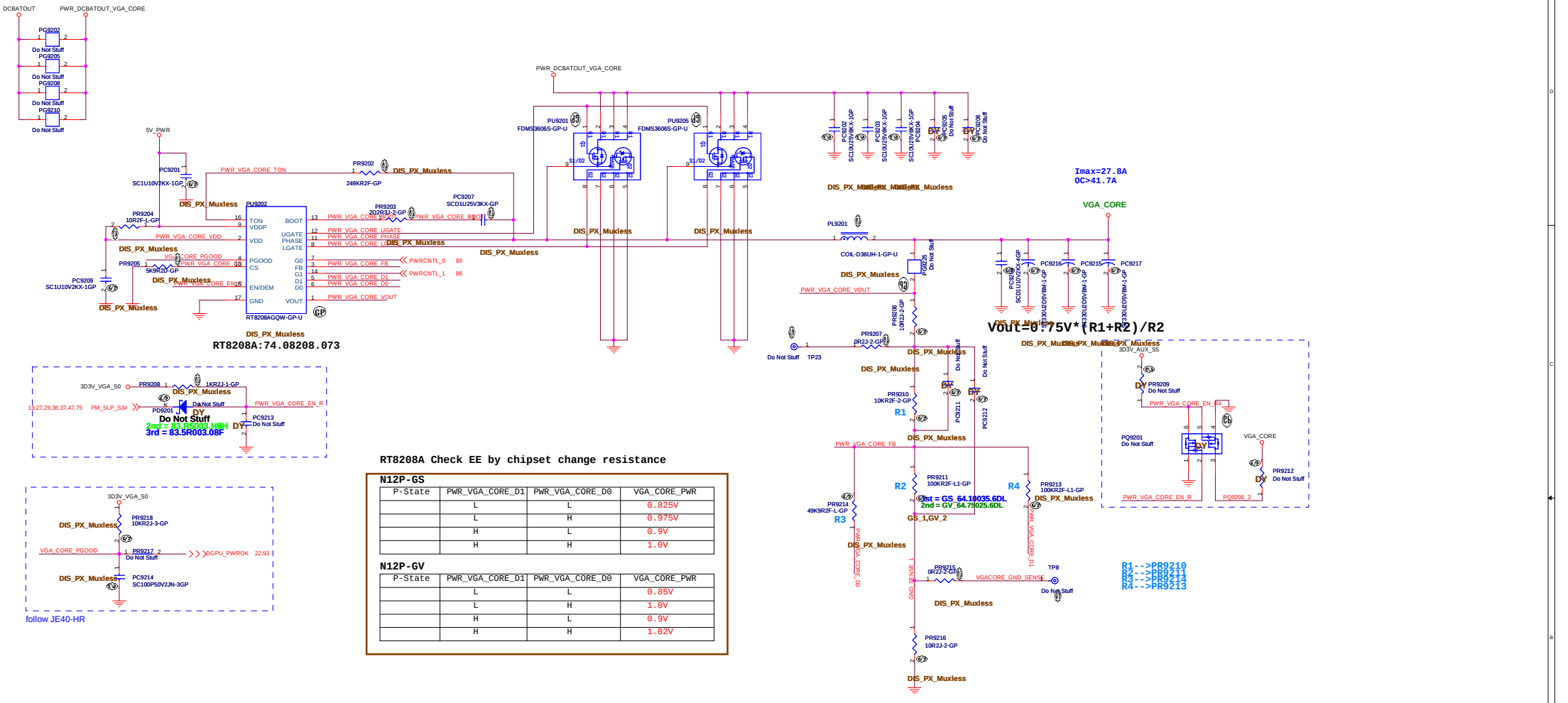


follow JE40-HR

RT8208A Check EE by chipset change resistance

N12P-GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.825V
	L	H	0.975V
	H	L	0.9V
	H	H	1.0V

N12P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
	L	L	0.85V
	L	H	1.0V
	H	L	0.9V
	H	H	1.02V

Frequency setting
470K --->165KHz
200K --->323KHz
100K --->500KHz

D12G

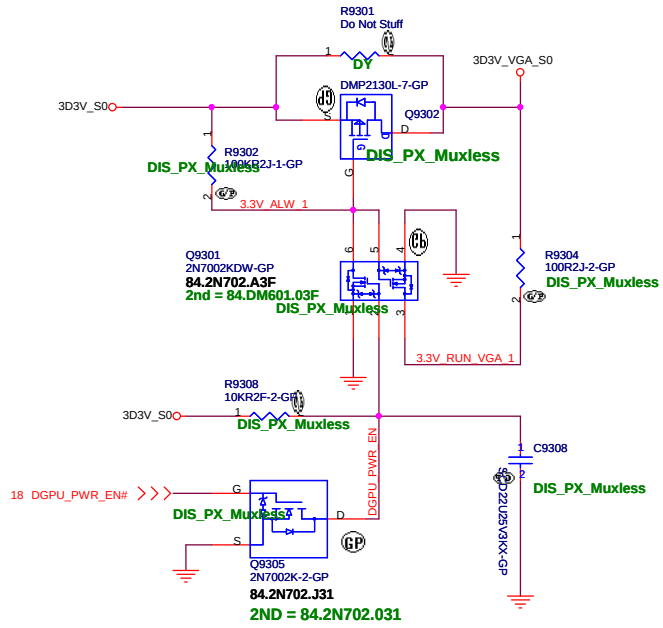
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT8208B +VGA_CORE***

Size: A2 | Document Number: **BA40/50-HR** | Rev: **SD**

Date: Thursday, April 07, 2011 | Sheet 92 of 109

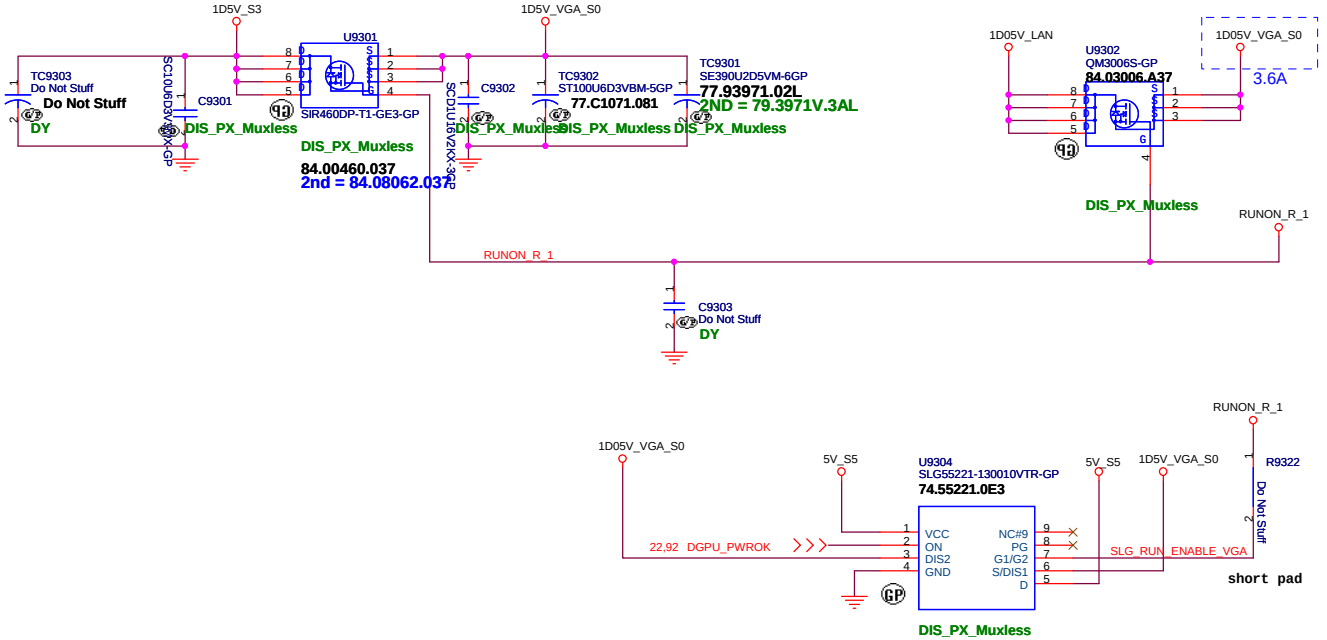
+3VS to 3.3V_DELAY Transfer

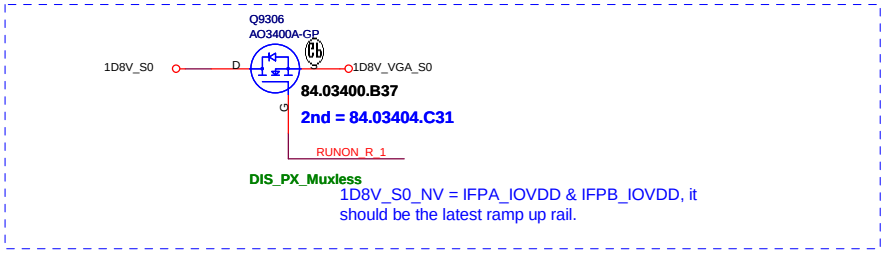


1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer





D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
Custom	BA40-HR	SD

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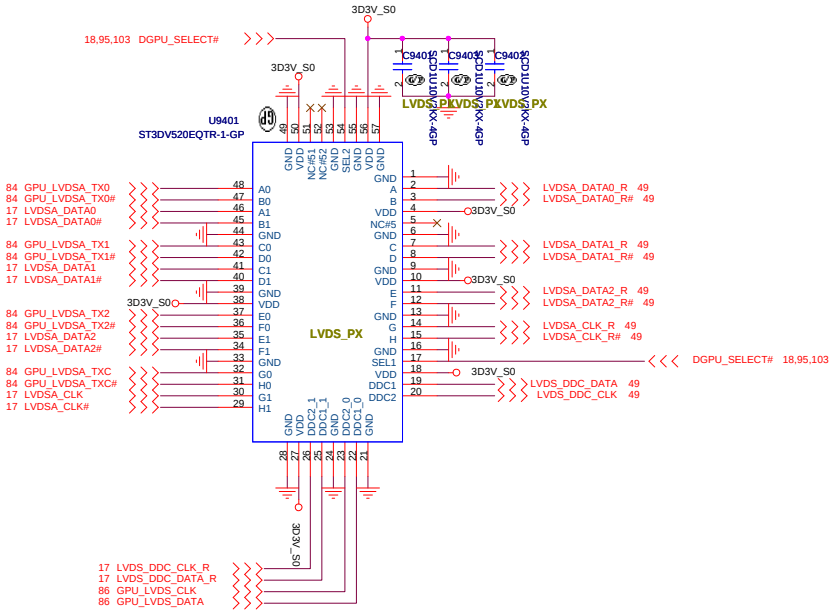
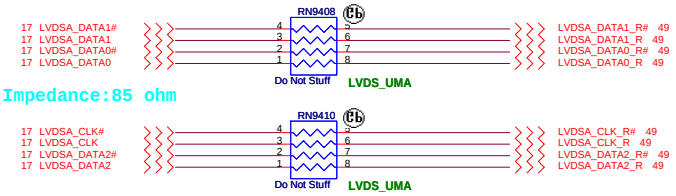
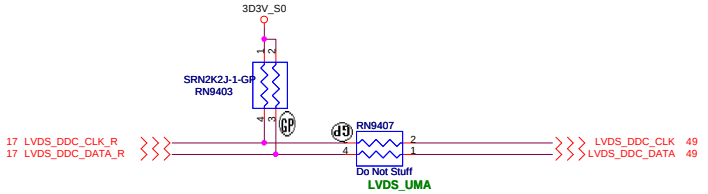
LVDS

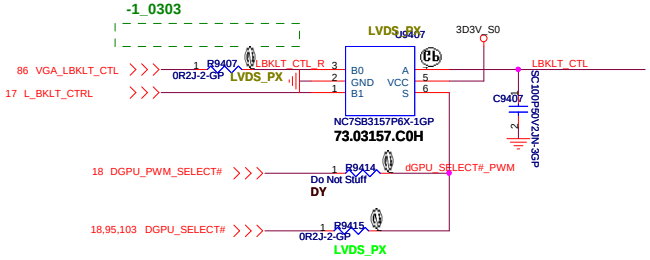




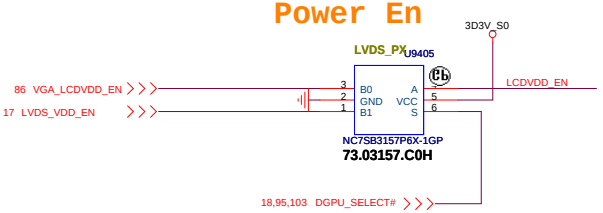
SEL->L(X=nX0),H(X=nX1)
SEL1 Control A~H
SEL2 Control DDC1,DDC2



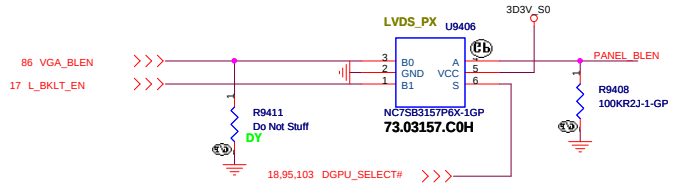
Panel BL brightness



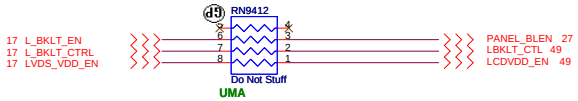
Power En



BL En



Panel BL brightness/Power En/BL En



D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LVDS_Switch***	
Size: Custom	Document Number: **BAD50-HR**	Rev: **SD**
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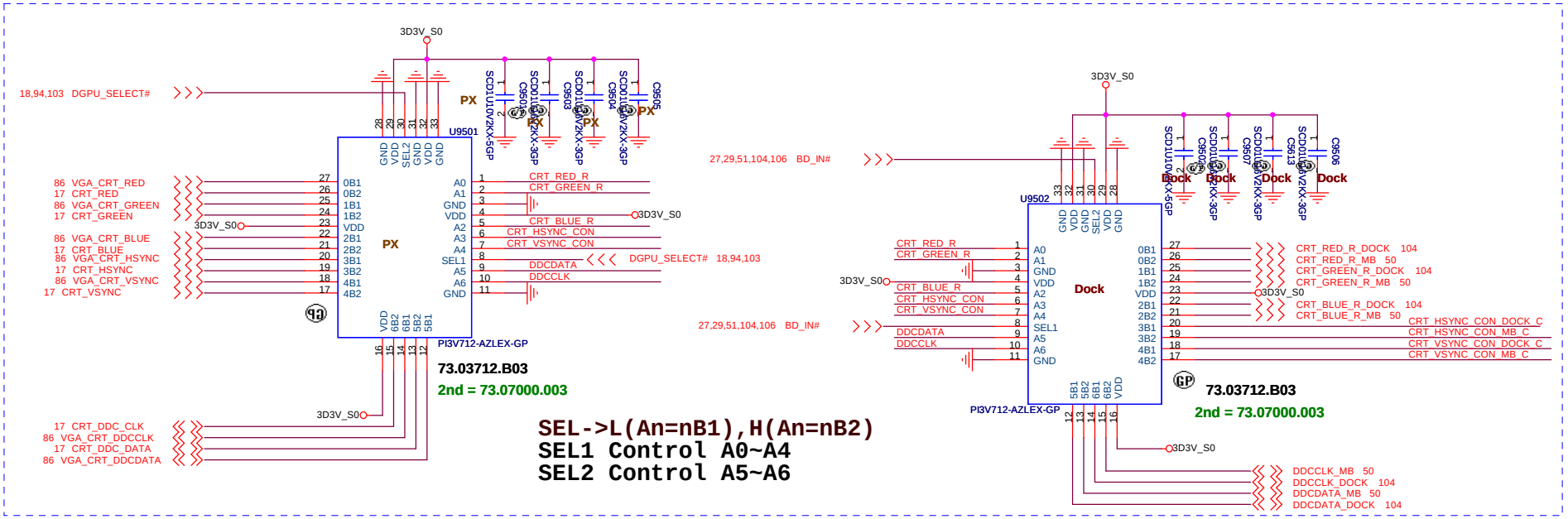
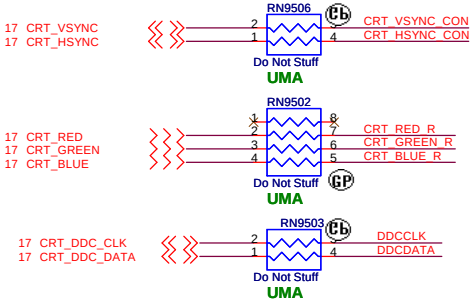
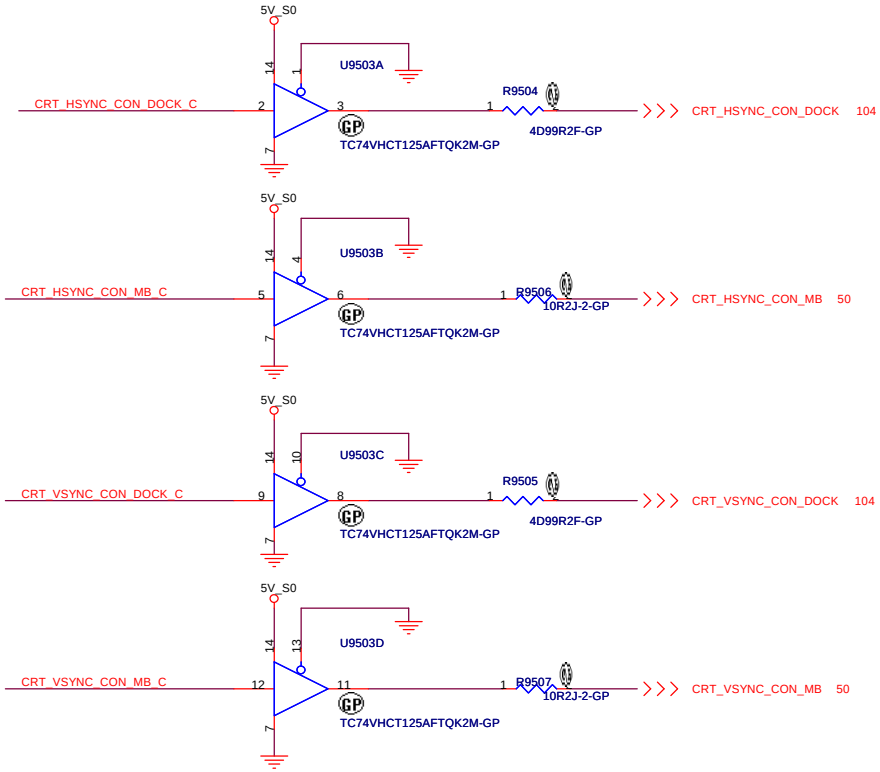
CRT DDCDATA & DDCCLK

VDD :
Recommend to use 6 caps (0.1u + 5*10nF) close to our chips



SEL->L(An=nB1),H(An=nB2)
SEL1 Control A0~A4
SEL2 Control A5~A6





D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT_Switch

Size: A3 | Document Number: Huron River | Rev: SD

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SSID = SDIO

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

Size	Document Number	Rev
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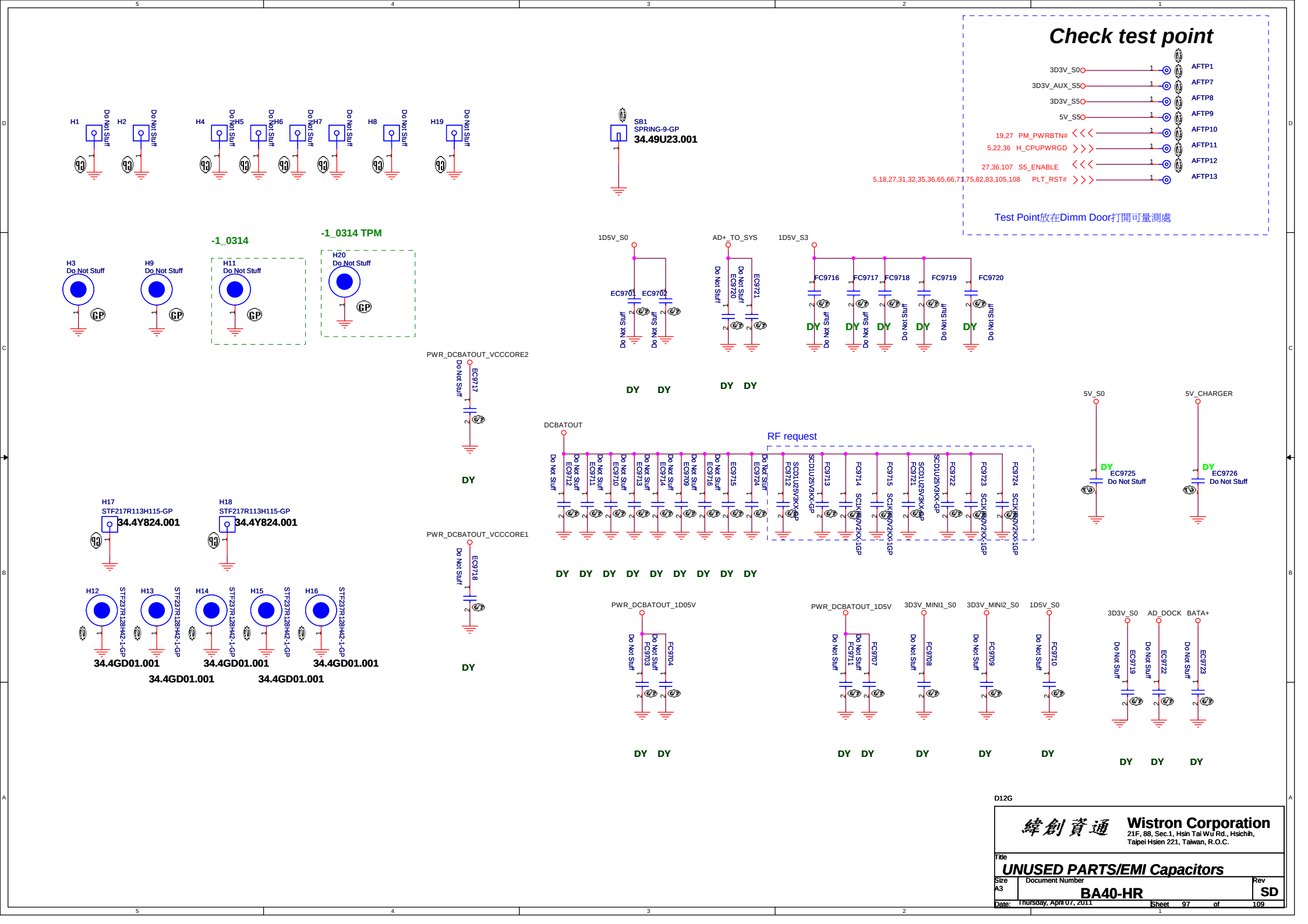
Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
19,27 PM_PWRBTN#
5,22,36 H_CPUPWRGD
27,36,107 S5_ENABLE
5,18,27,31,32,35,36,65,66,71,75,82,83,105,108 PLT_RST#
AFTP1
AFTP7
AFTP8
AFTP9
AFTP10
AFTP11
AFTP12
AFTP13
Test Point放在Dimm Door打開可量測處
H1 H2 H4 H5 H6 H7 H8 H19
Do Not Stuff
SB1
SPRING-9-GP
34.49U23.001
-1_0314
-1_0314 TPM
H3
H9
H11
H20
1D5V_S0
AD+_TO_SYS
1D5V_S3
EC9701 EC9702
EC9720 EC9721
FC9716 FC9717 FC9718 FC9719 FC9720
DY
PWR_DCBATOUT_VCCCORE2
EC9717
PWR_DCBATOUT_VCCCORE1
EC9718
DCBATOUT
RF request
EC9712 EC9711 EC9710 EC9713 EC9714 EC9709 EC9716 EC9715 EC9724
FC9712 FC9713 FC9714 FC9715 FC9721 FC9722 FC9723 FC9724
SCD1U25V3KX-GP
SC1K50V2KX-1GP
5V_S0
5V_CHARGER
EC9725
EC9726
H17 H18
STF217R113H115-GP
34.4Y824.001
H12 H13 H14 H15 H16
STF237R128H42-1-GP
34.4GD01.001
PWR_DCBATOUT_1D05V
FC9703 FC9704
PWR_DCBATOUT_1D5V
FC9711 FC9707
3D3V_MINI1_S0
FC9708
3D3V_MINI2_S0
FC9709
1D5V_S0
FC9710
3D3V_S0
AD_DOCK
BATA+
EC9719 EC9722 EC9723
D12G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size A3
Document Number
BA40-HR
Rev SD
Date: Thursday, April 07, 2011
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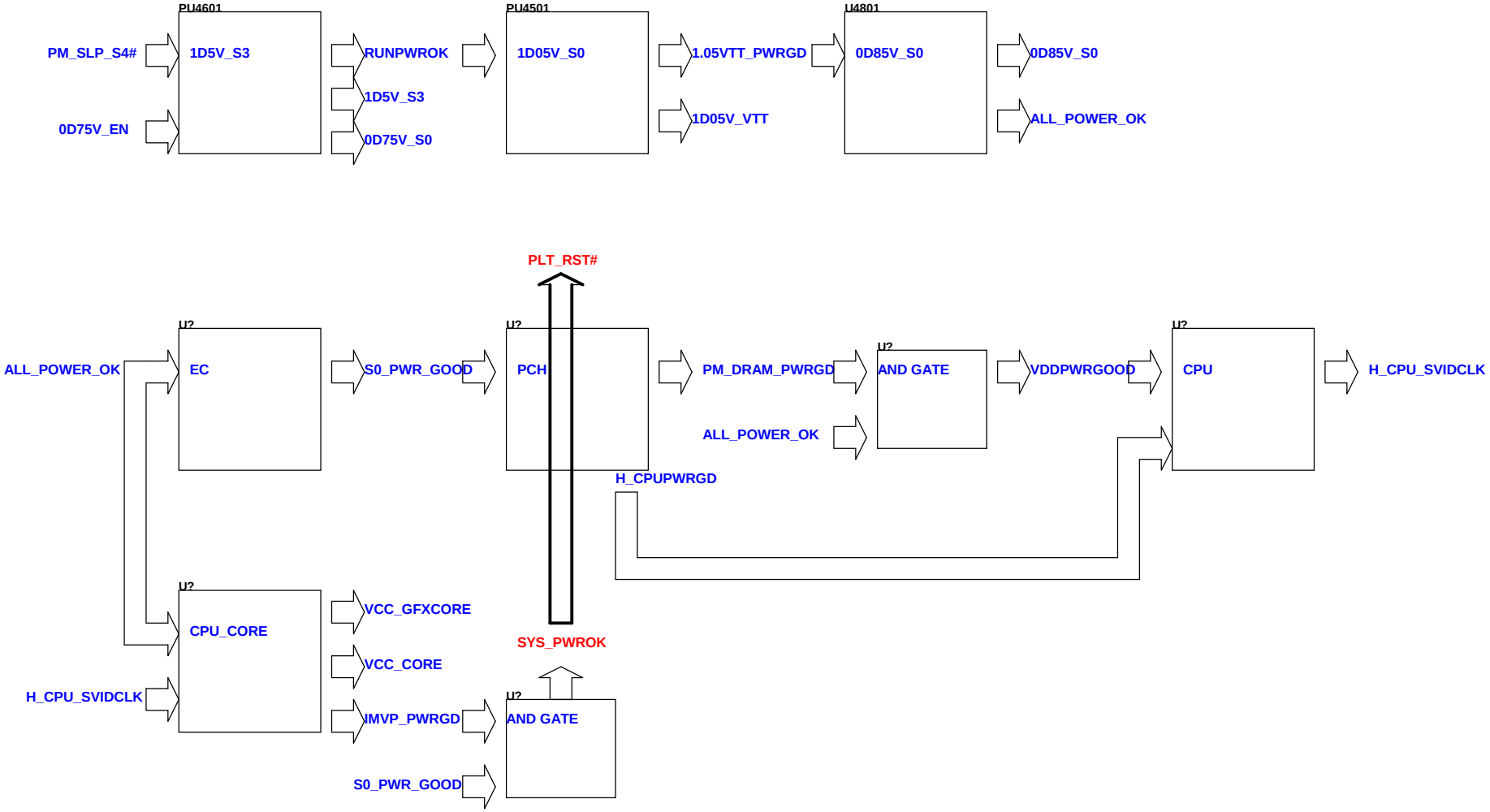
Power Sequence



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: A3 | Document Number: BA40-HR | Rev: SD

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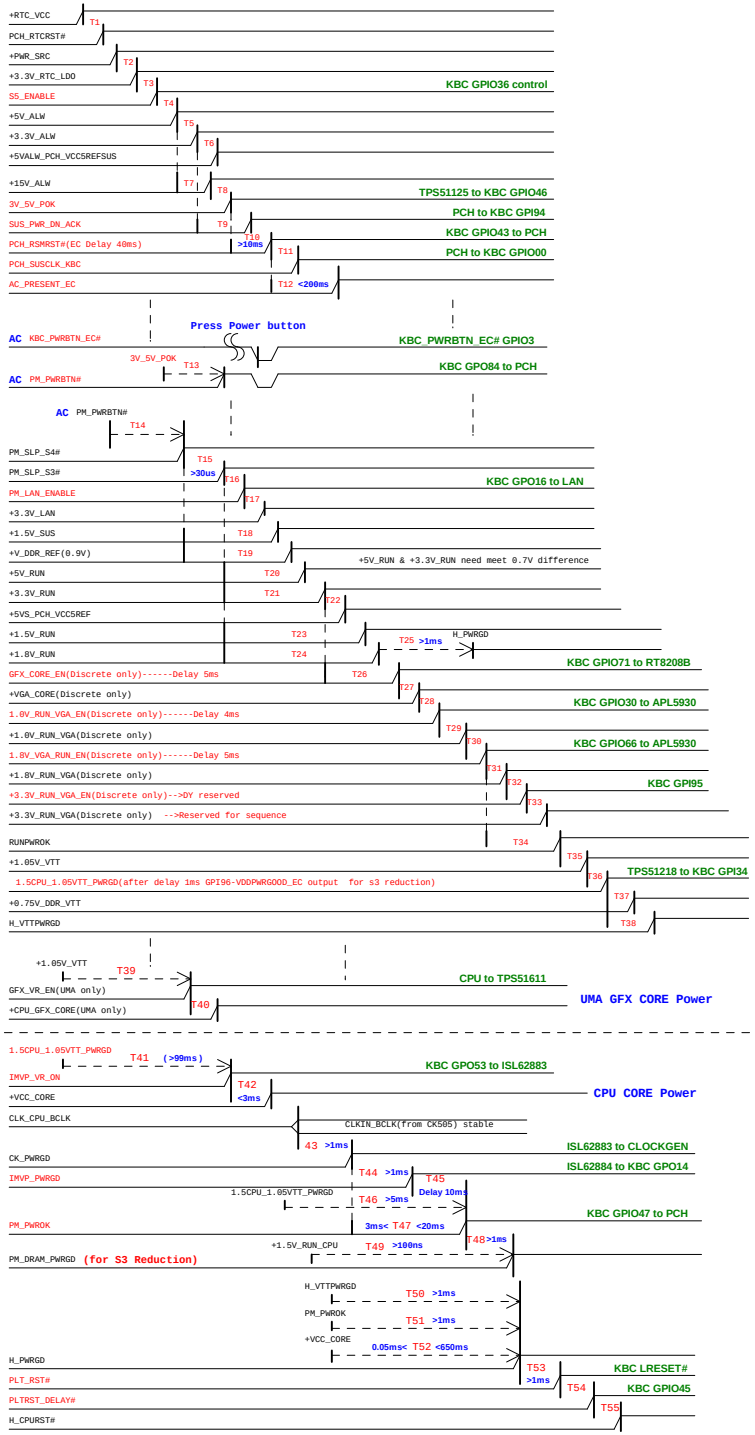
Intel-Power Up Sequence

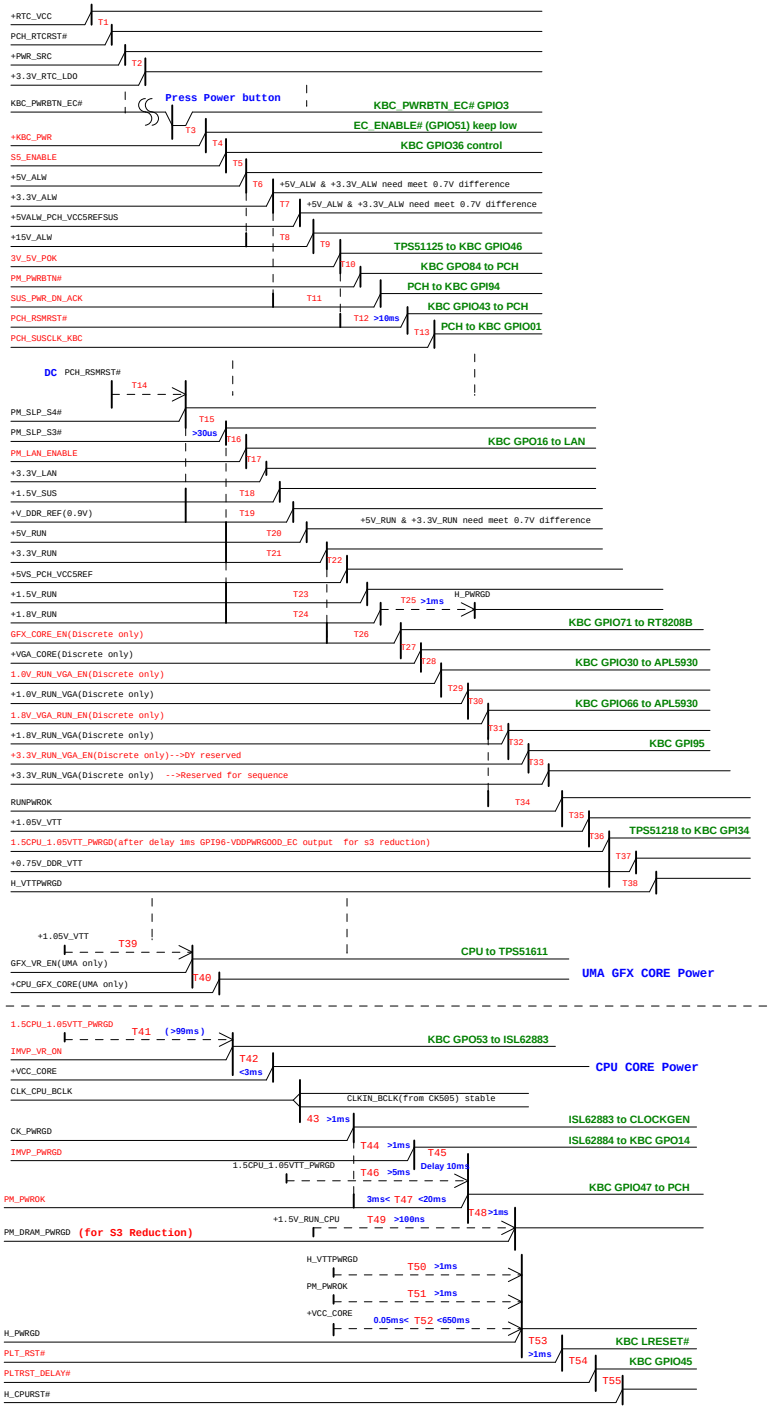
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

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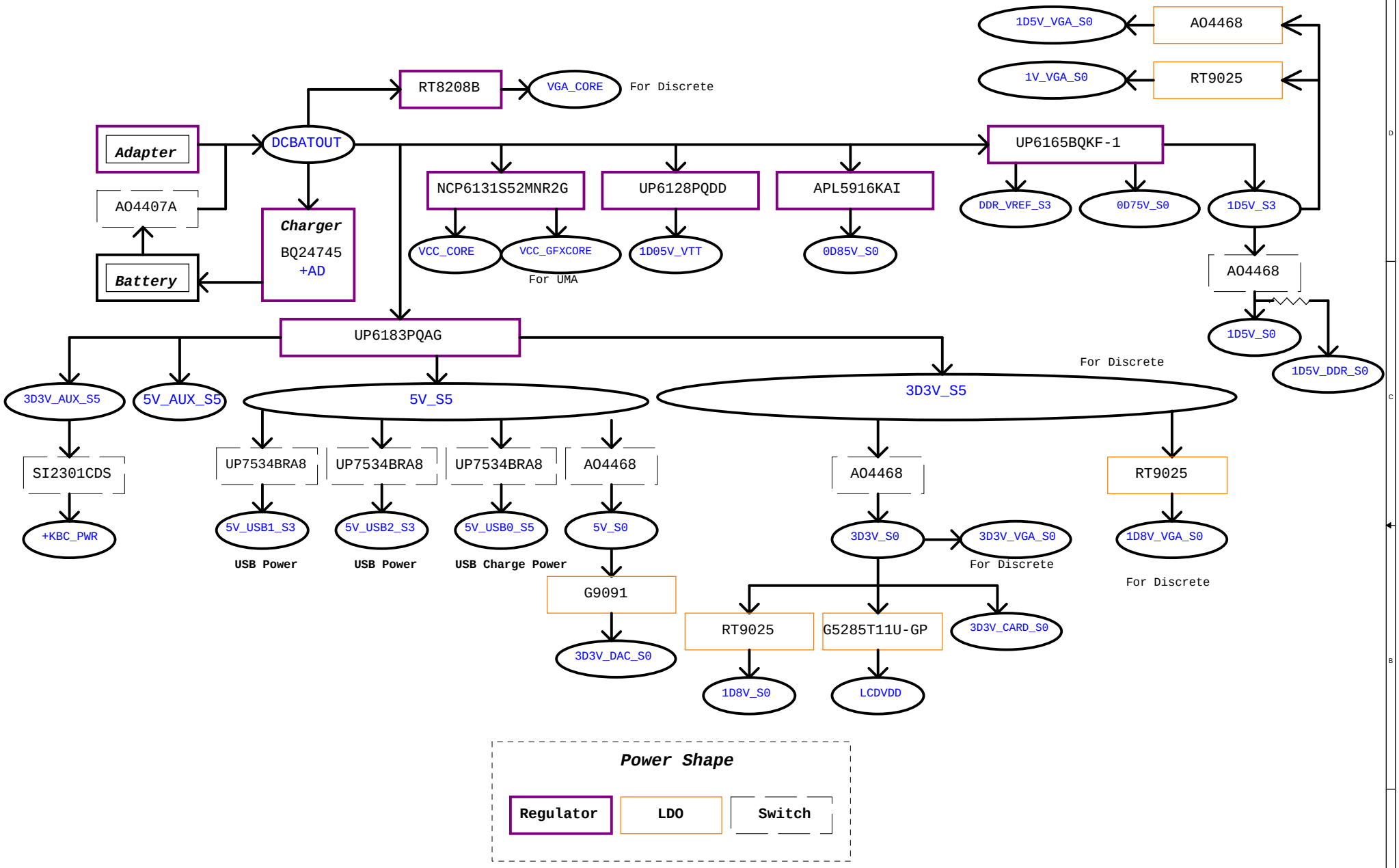

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	BA40-HR	SD

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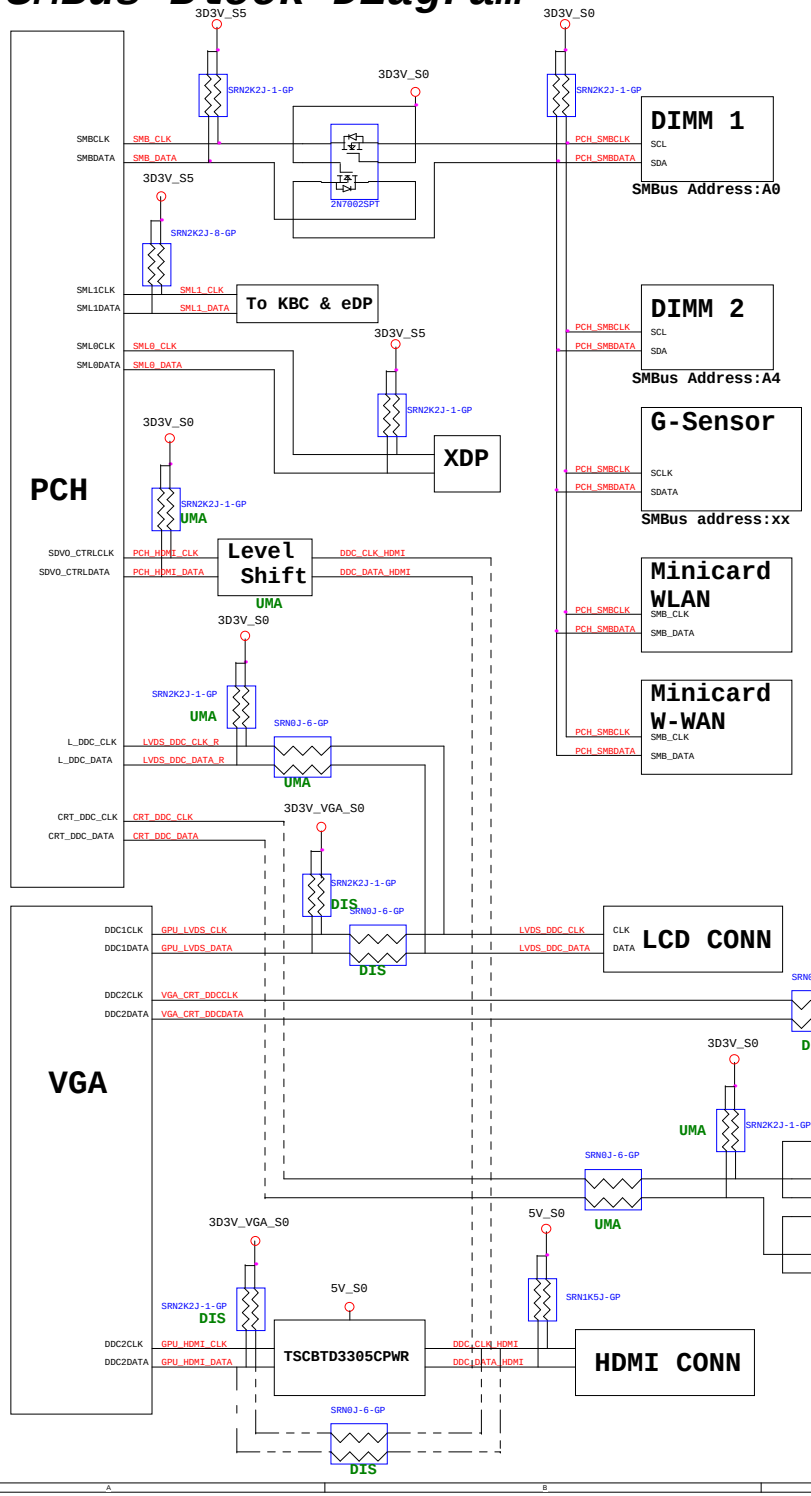
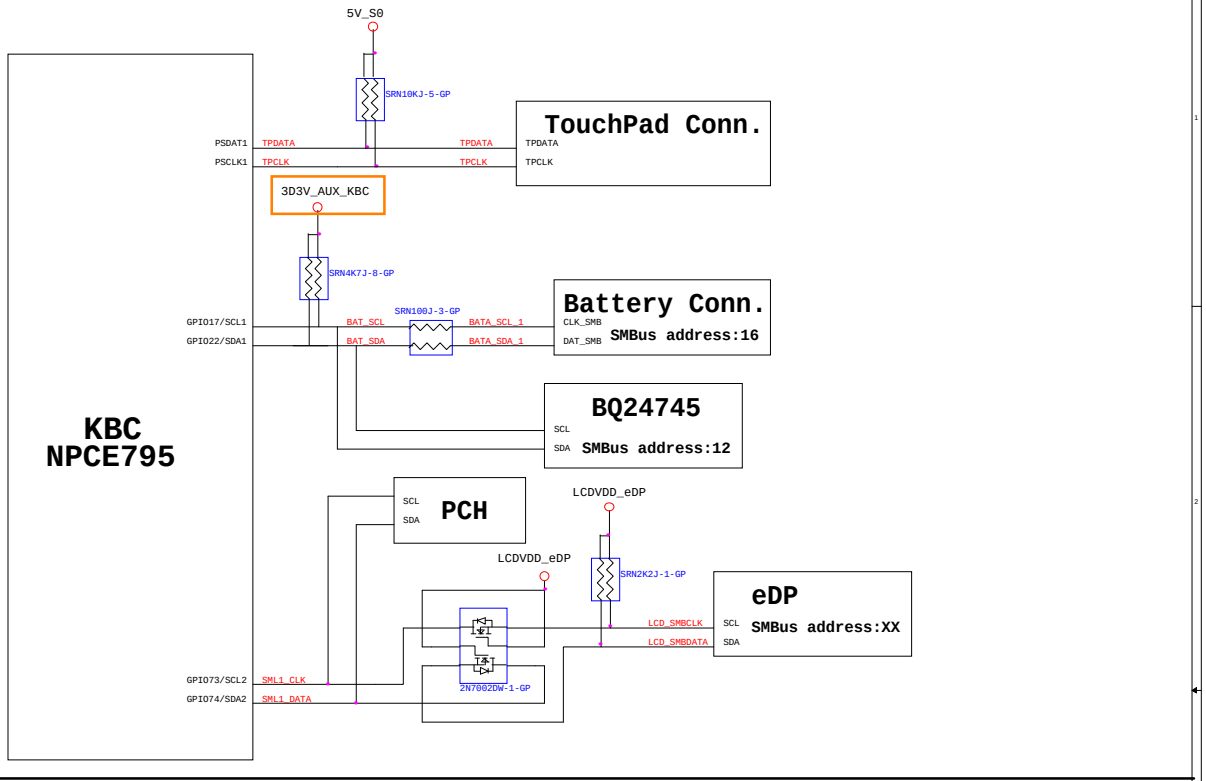
PCH SMBus Block Diagram



KBC SMBus Block Diagram



D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	BA40-HR	SD

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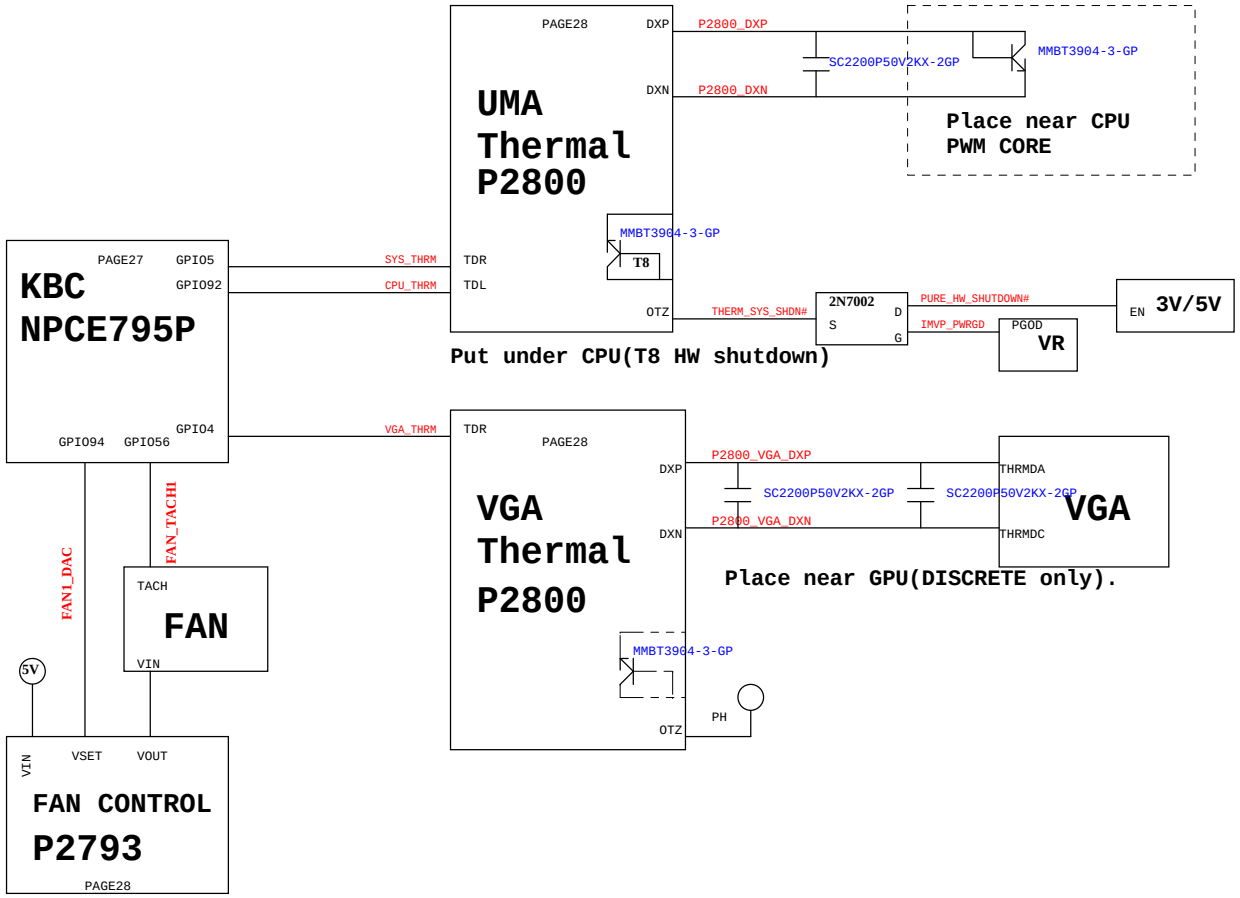
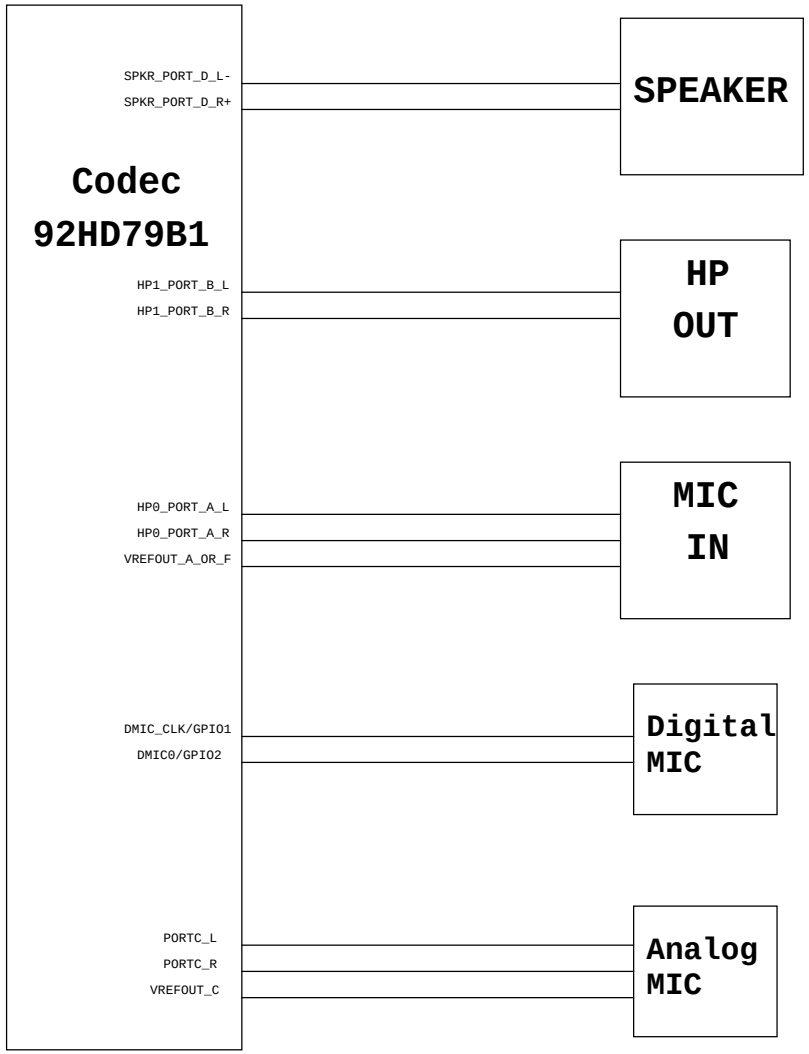
Thermal Block Diagram



Audio Block Diagram



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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Custom	BA40-HR	SD

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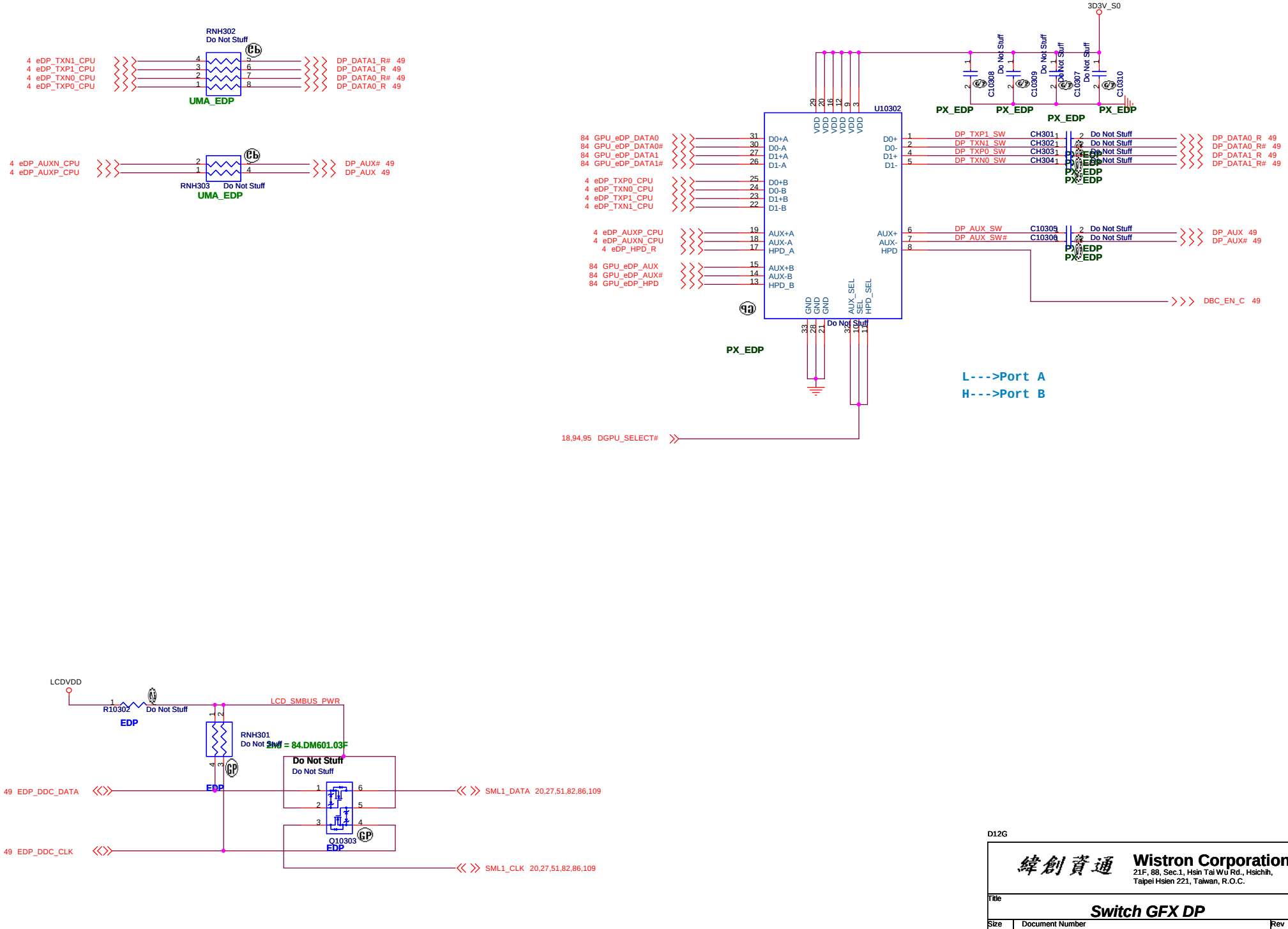

D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switch GFX DP*		
Size: A3	Document Number: BA40-HR	Rev: SD
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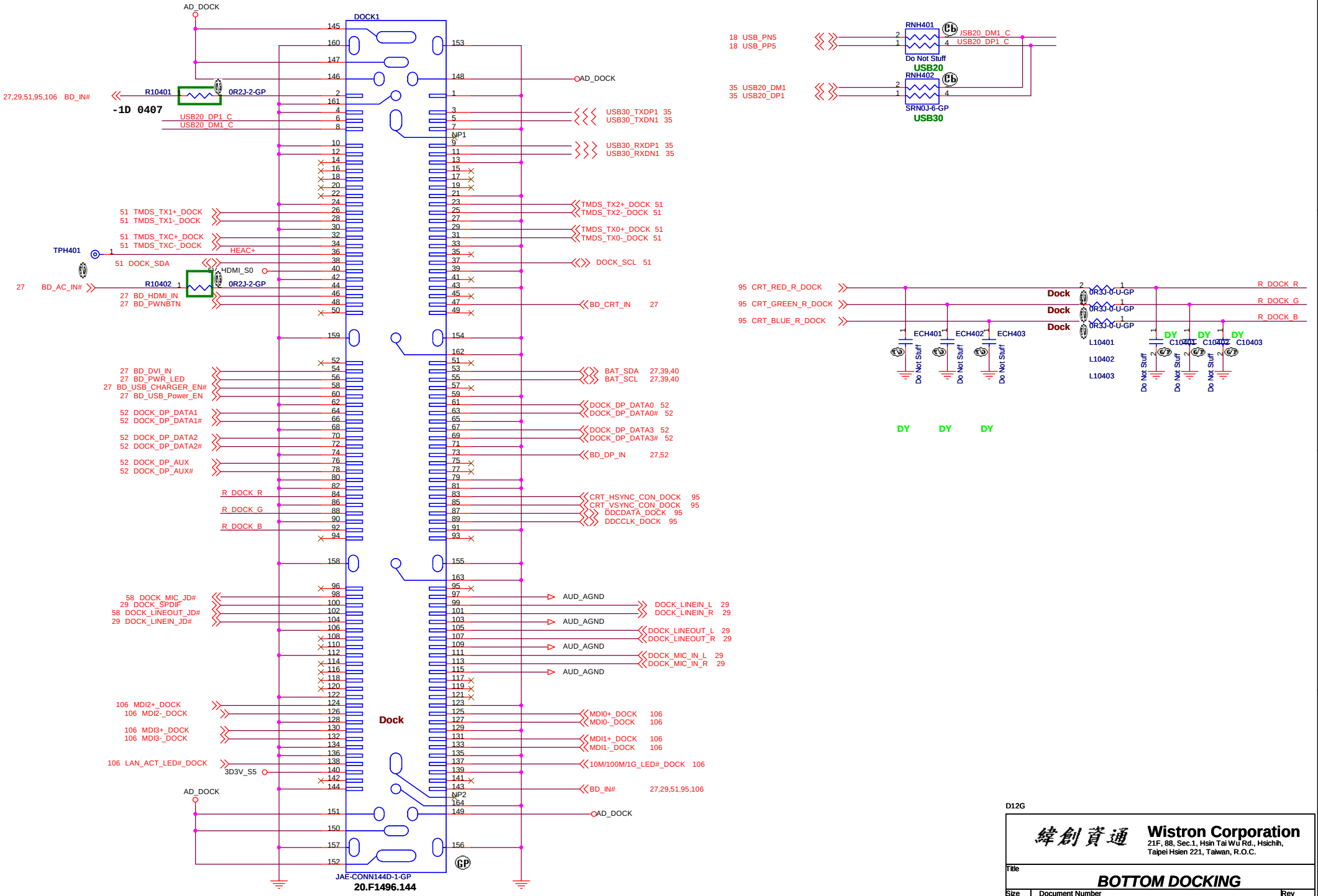

D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BOTTOM DOCKING***	
Size A3	Document Number **BA40-HR**	Rev **SD**
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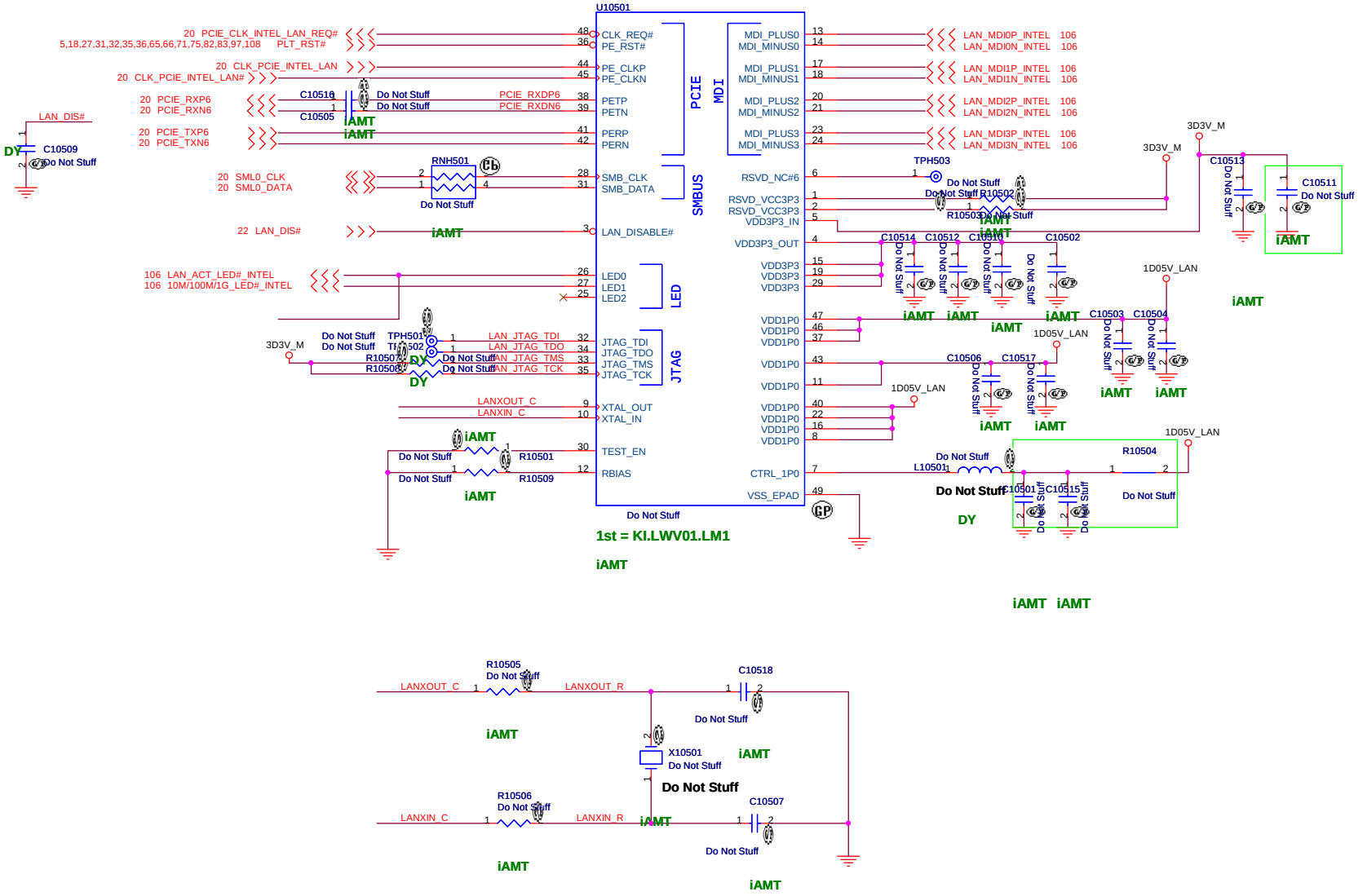

D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN INTEL 82579***	
Size A3	Document Number **BA40-HR**	Rev **SD**
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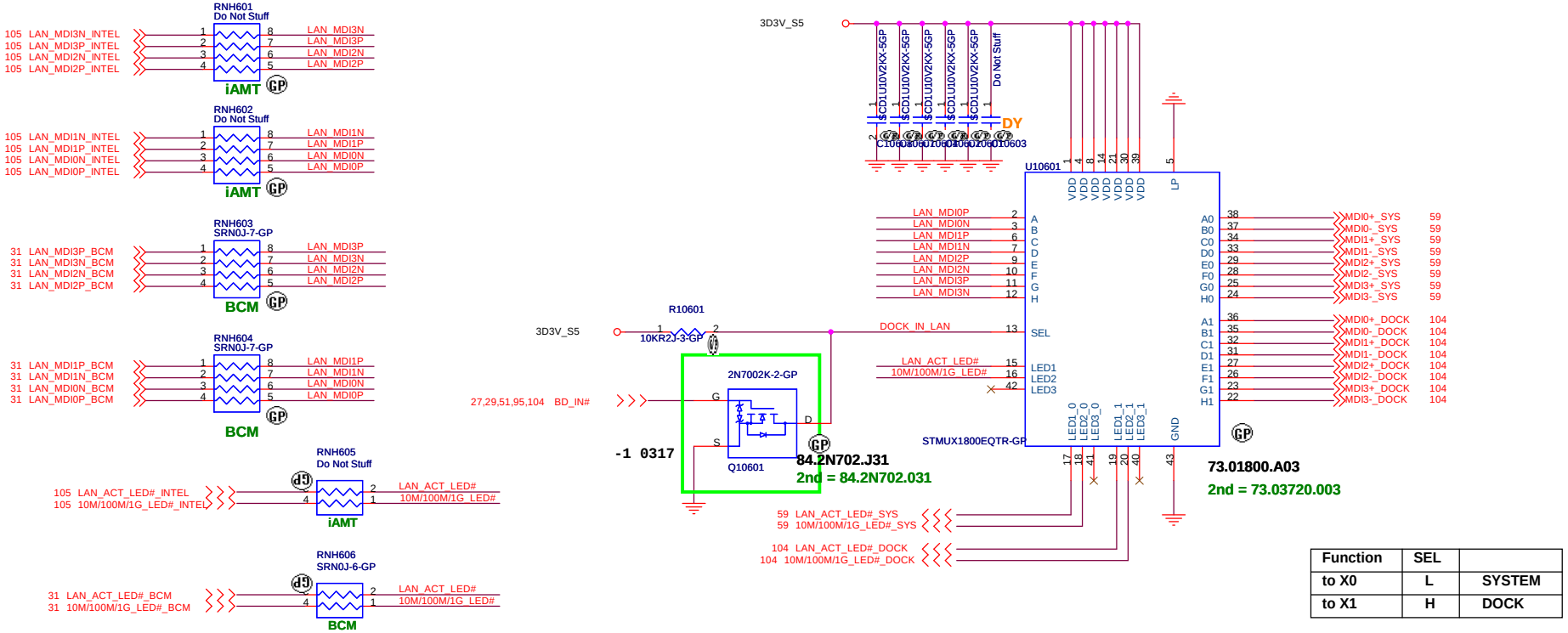
LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN SWITCH

Size: A3 | Document Number: BAD50-HR | Rev: SD

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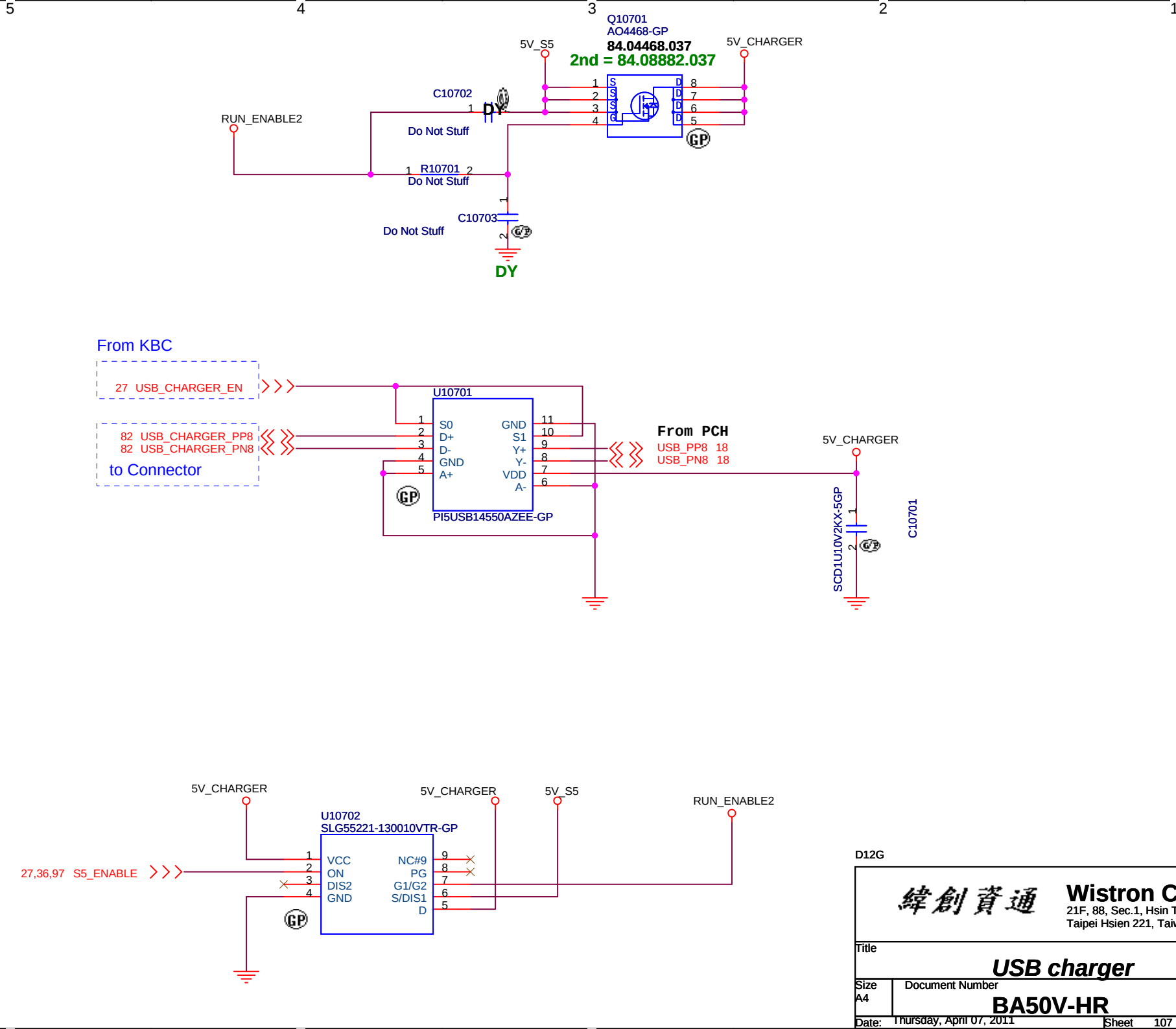

D12G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB charger*

Size	Document Number	Rev
A4	BA50V-HR	SD

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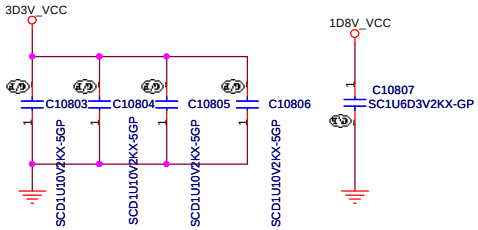
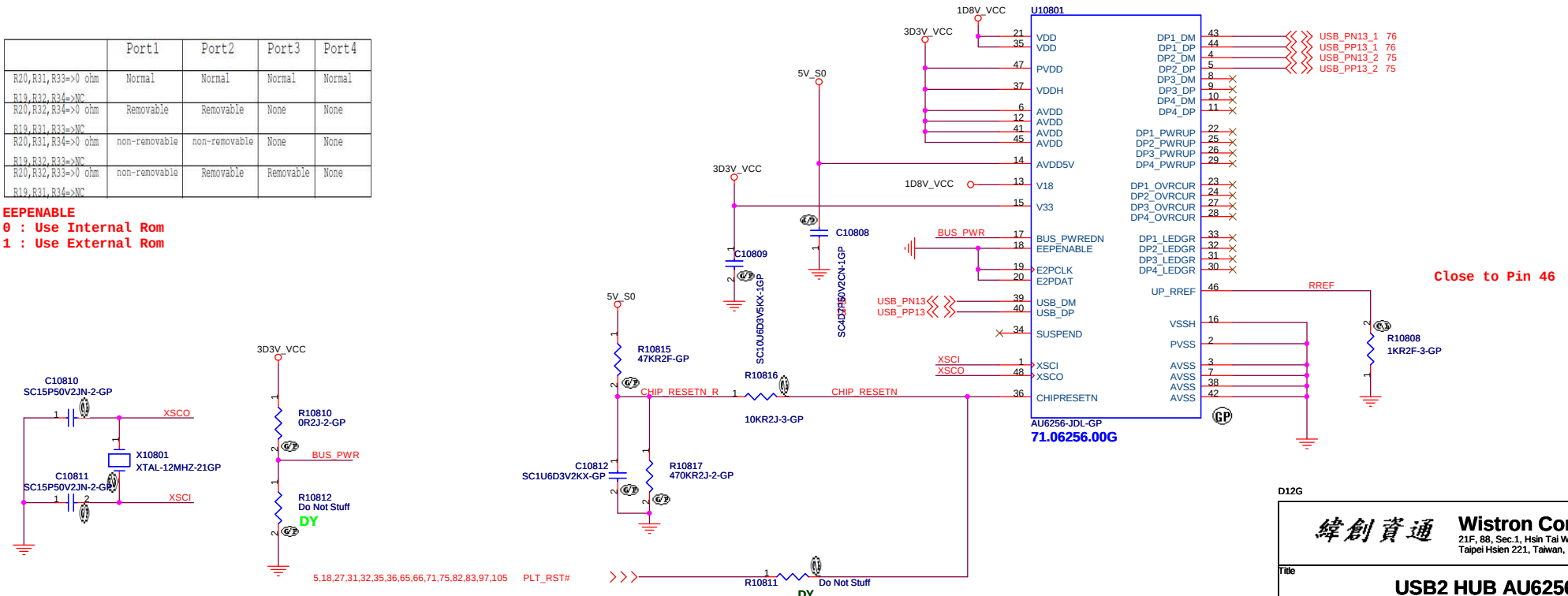


	Port1	Port2	Port3	Port4
R20,R31,R33=>0 ohm R19,R32,R34=>NC	Normal	Normal	Normal	Normal
R20,R32,R34=>0 ohm R19,R31,R33=>NC	Removable	Removable	None	None
R20,R31,R34=>0 ohm R19,R32,R33=>NC	non-removable	non-removable	None	None
R20,R32,R33=>0 ohm R19,R31,R34=>NC	non-removable	Removable	Removable	None

EEPENABLE
0 : Use Internal Rom
1 : Use External Rom



D12G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB2 HUB AU6256**	
Size	Document Number **BAD50-HR**	Rev SD
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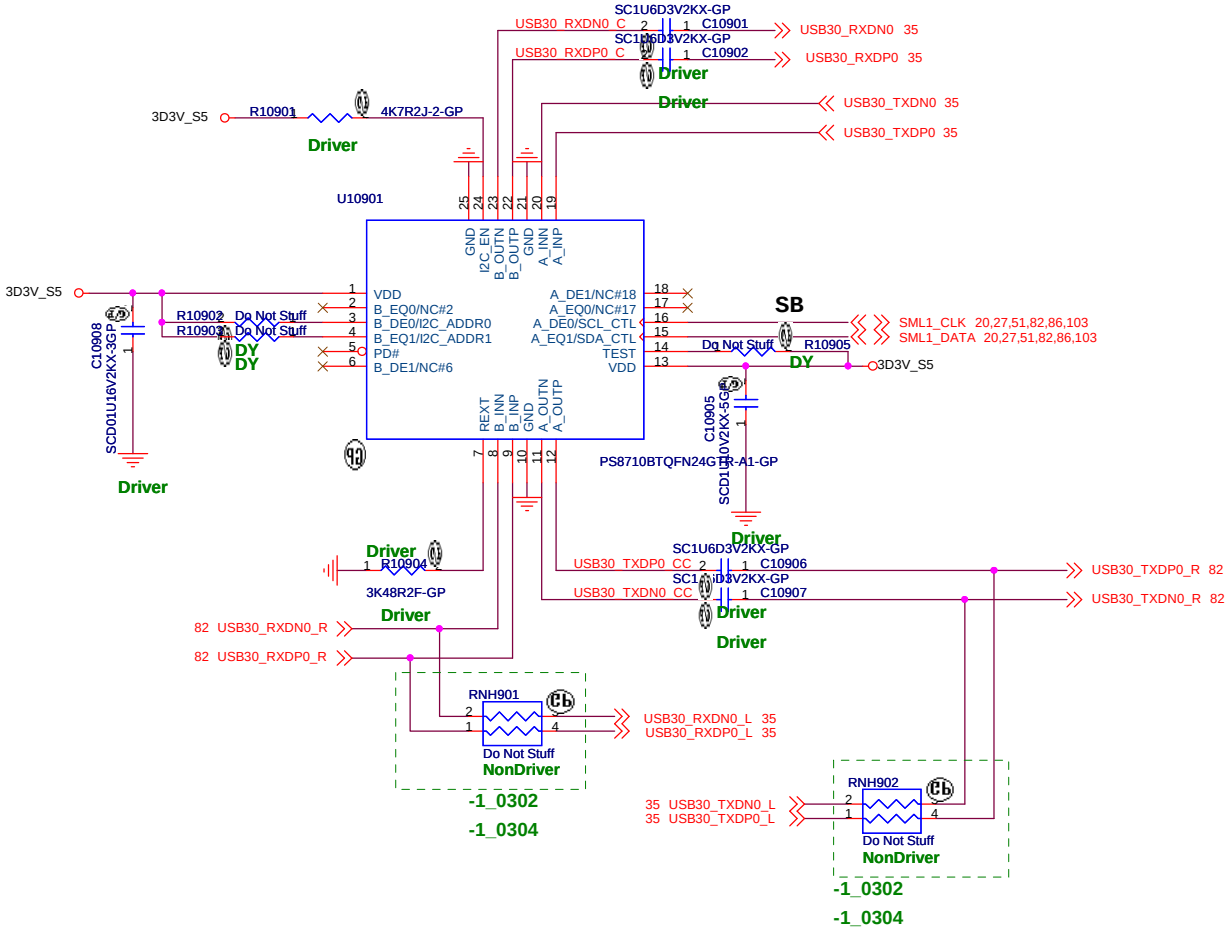
I2C mode
To USB BD



D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB30 re-driver*		
Size: B	Document Number: BAD50-HR	Rev: SD
Date: Thursday, April 07, 2011	Sheet 109 of 109	