

Compal Confidential

Model Name : Olvia_BE
Compal Project Name : A4W1E
File Name : LA-C801P

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A4W1E Schematics Document

AMD "Beema" Platform

AMD 15W APU With Puma+ Core

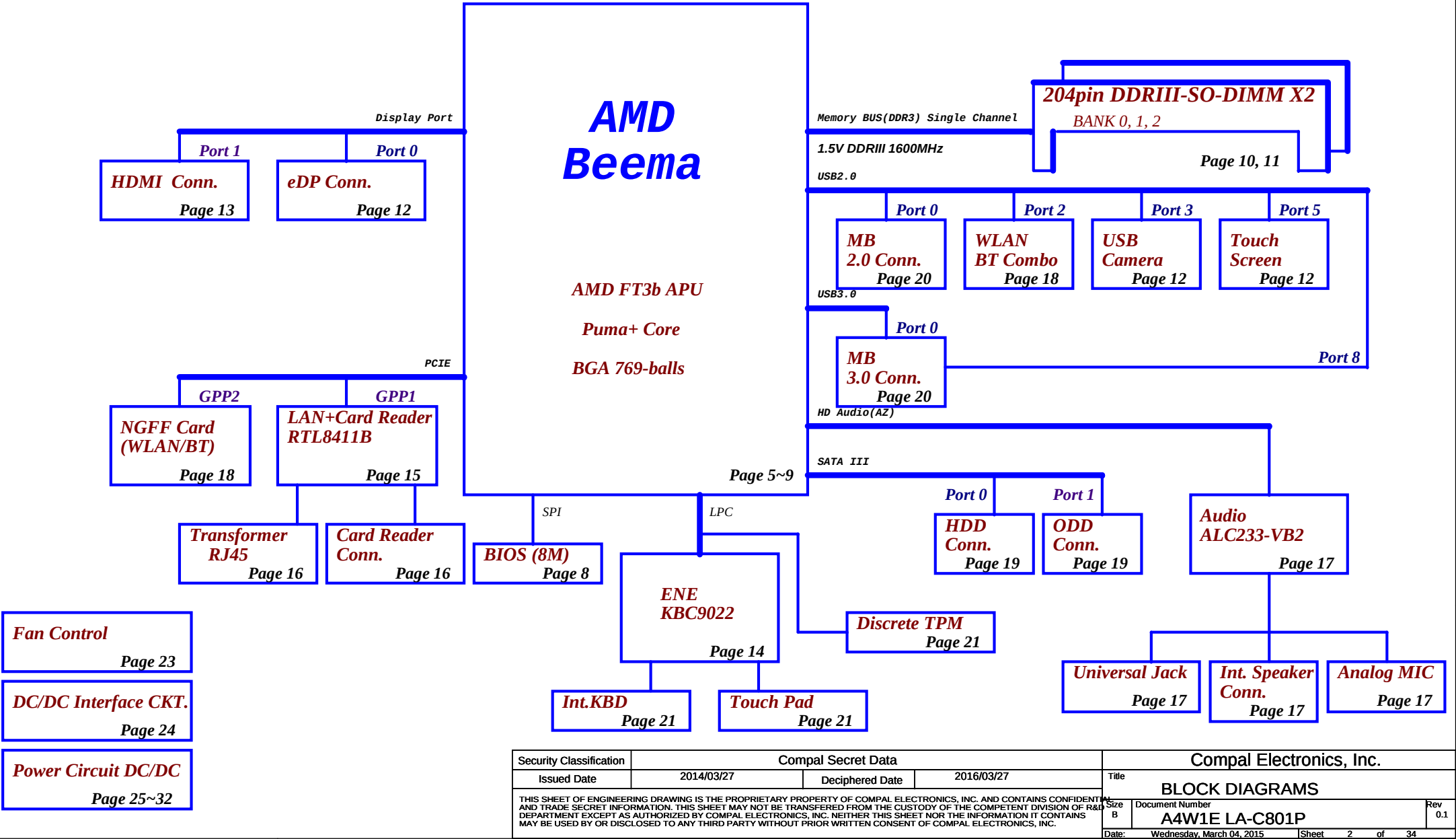
LA-C801P REV: 1.A

2015-03-30

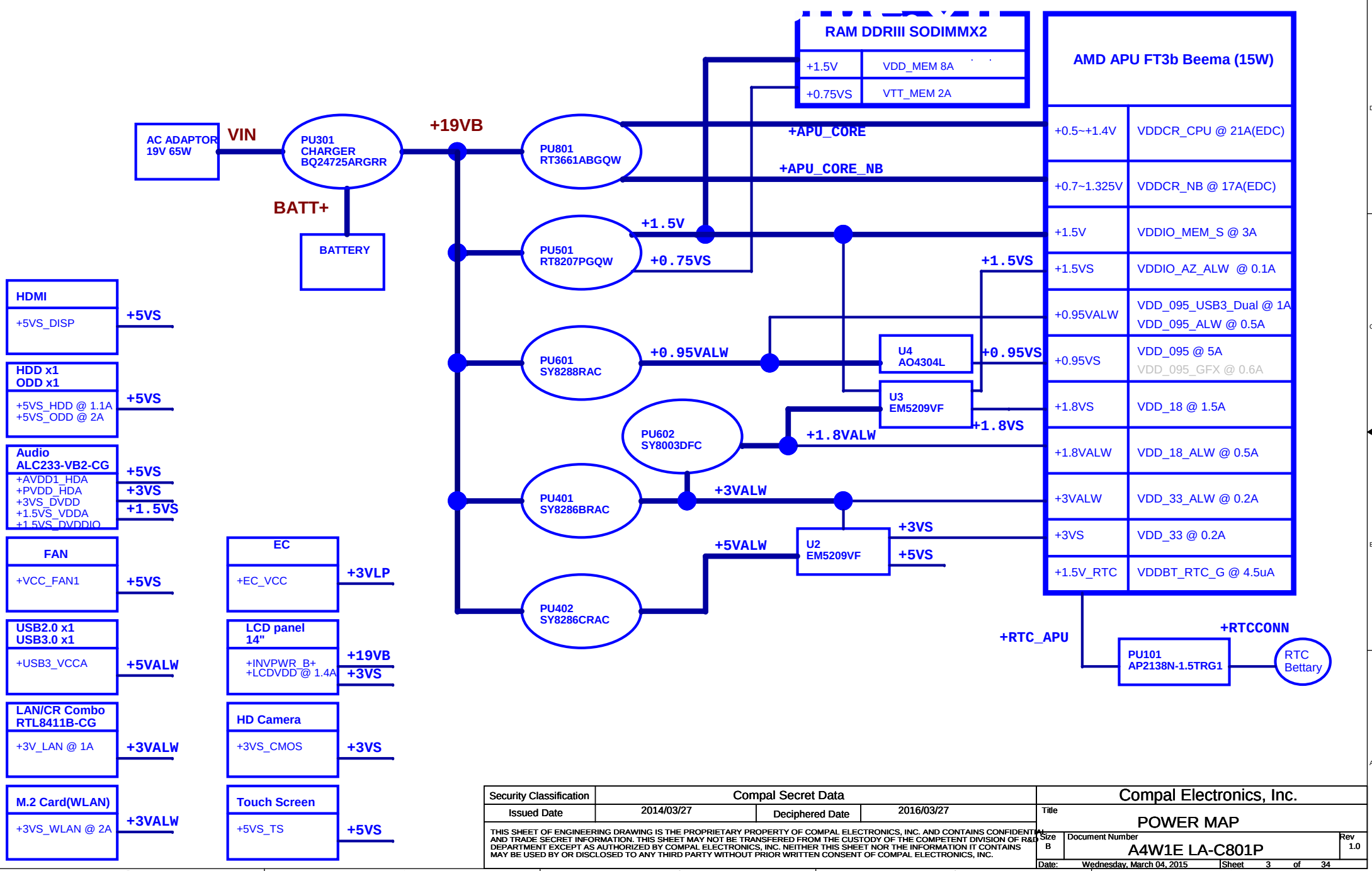
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Model Name : A4W1E



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						Size	Document Number			Rev	
						B	A4W1E LA-C801P			0.1	
						Date:	Wednesday, March 04, 2015		Sheet	2	of

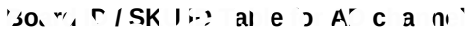


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								Size	Document Number			Rev	
								B	A4W1E LA-C801P			1.0	
								Date:		Wednesday, March 04, 2015		Sheet 3 of 34	

[illegible]

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			



Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
EMC@	EMI pop component
@EMC@	EMI unpop component
JP@	Jump
TP@	Test point
SP@	Short pad for clear CMOS
HDT@	HDT+ for test phase, MP remove
RS@	R-short
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
A8@, A6@, A4@	APU Part Number for A4,A6,A8 APU
E1@, E2@	APU Part Number for E1,E2 APU
BL@	Keyboard backlight
TPM@	Use discrete TPM module
TPUSB@	Use USB to I2C IC for T/P
ECI2C@	Use EC I2C T/P
@RF@	RF unpop component
233@	Use for Audio Codec ALC233-VB2
KBN@	Stuff when use Kabini APU
BMA@	Stuff when use Beema APU
CZL@	Stuff when use Carrizo-L APU
BYOC@	Stuff when support BYOC
NBYOC@	Stuff when non-support BYOC

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3*	Pre-MP
4	
5	
6	
7	

<i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1(Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

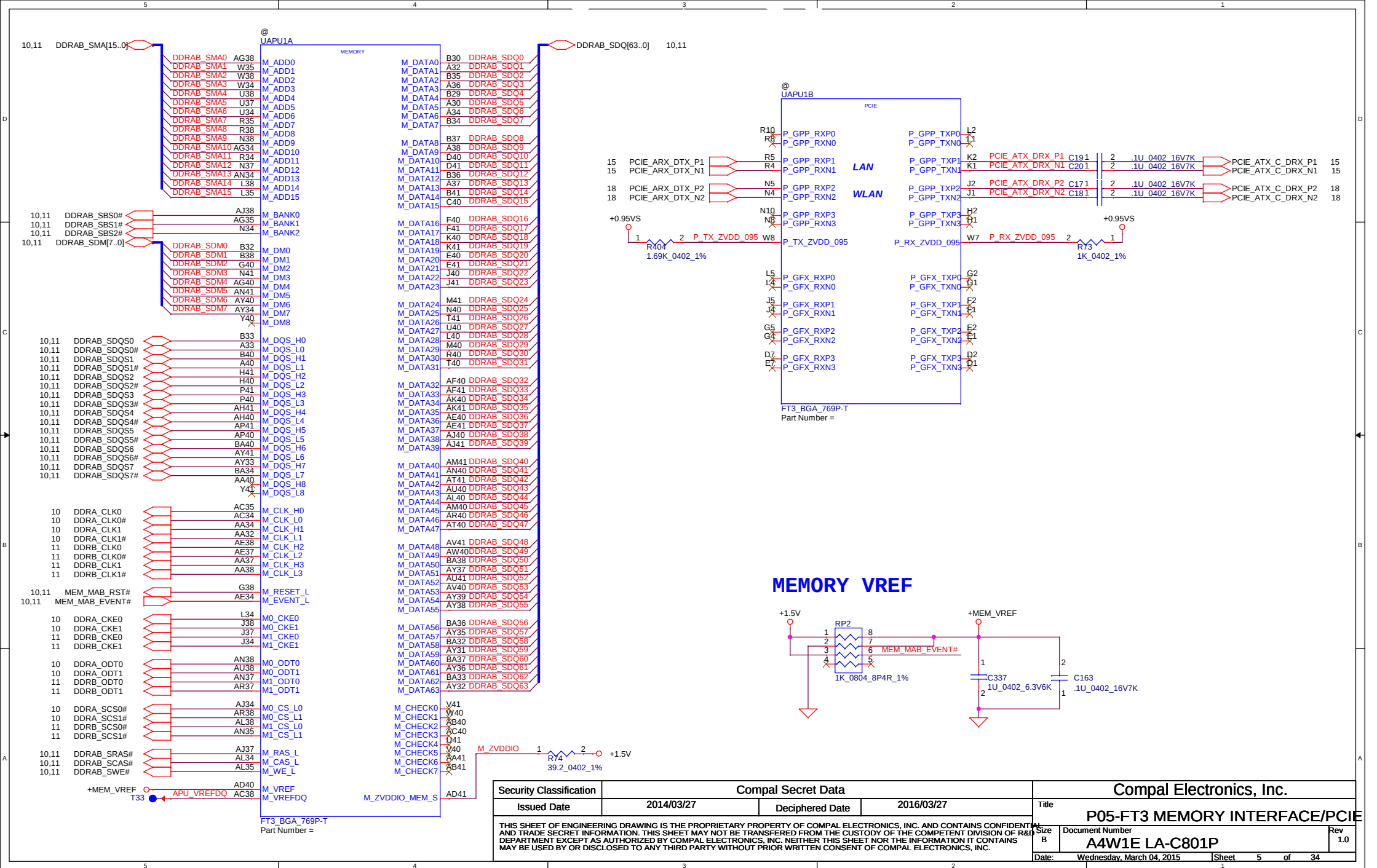
The timing diagram illustrates the sequence of events for various control signals. The signals are grouped as follows:

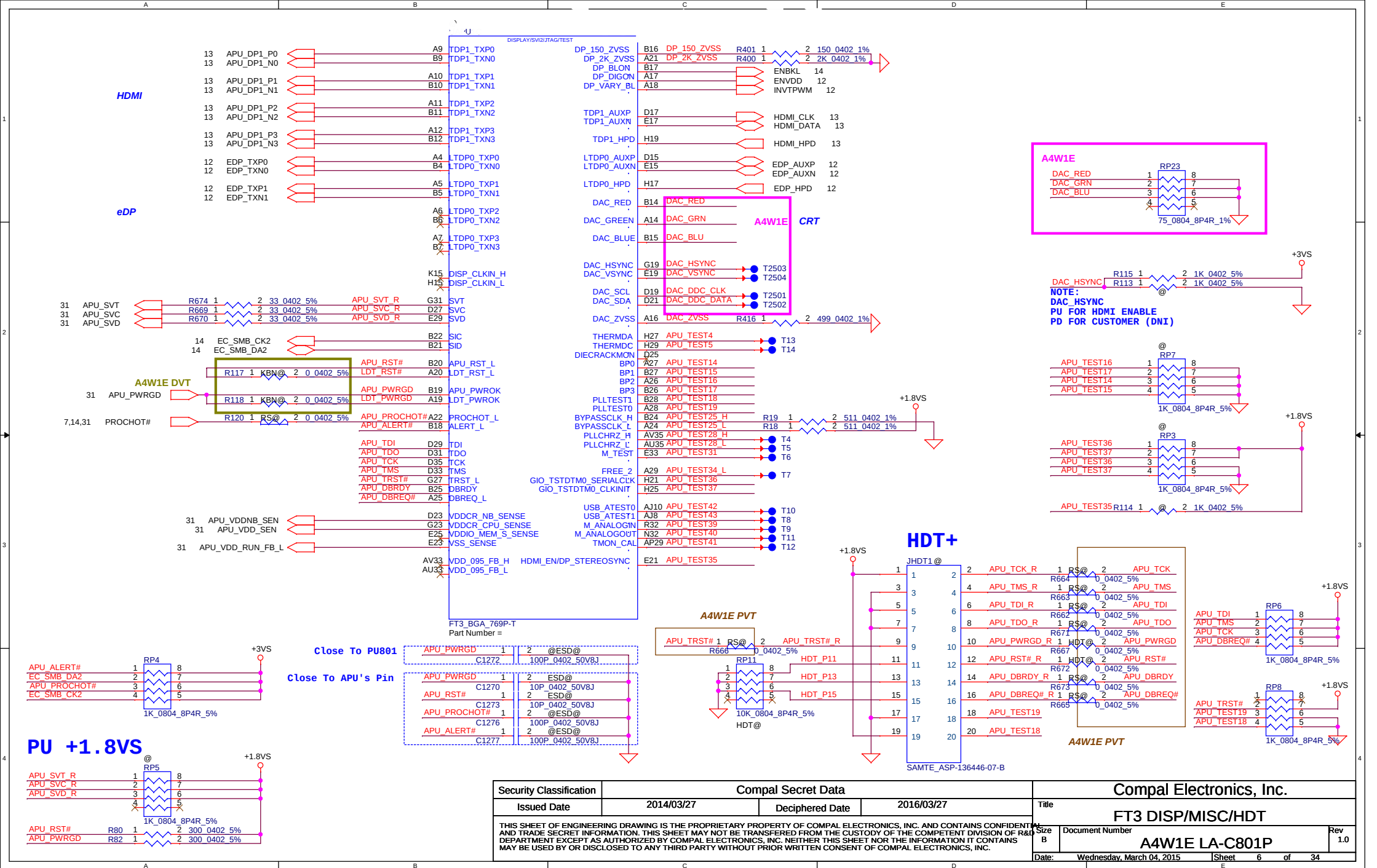
- G-A**: +RTC, EC_ON
- G-B**: +3VALW/+5VALW, +1.8VALW, +0.95VALW, SYSON
- G-C**: +1.5V, SUSP#
- G-D**: +3VS, +1.8VS, +1.5VS, +0.95VS, VR_ON
- G-E**: +APU_CORE, +APU_CORE_NB

The diagram shows the relative timing of these signals, with some signals like +3VALW/+5VALW and +3VS being active for longer durations than others.

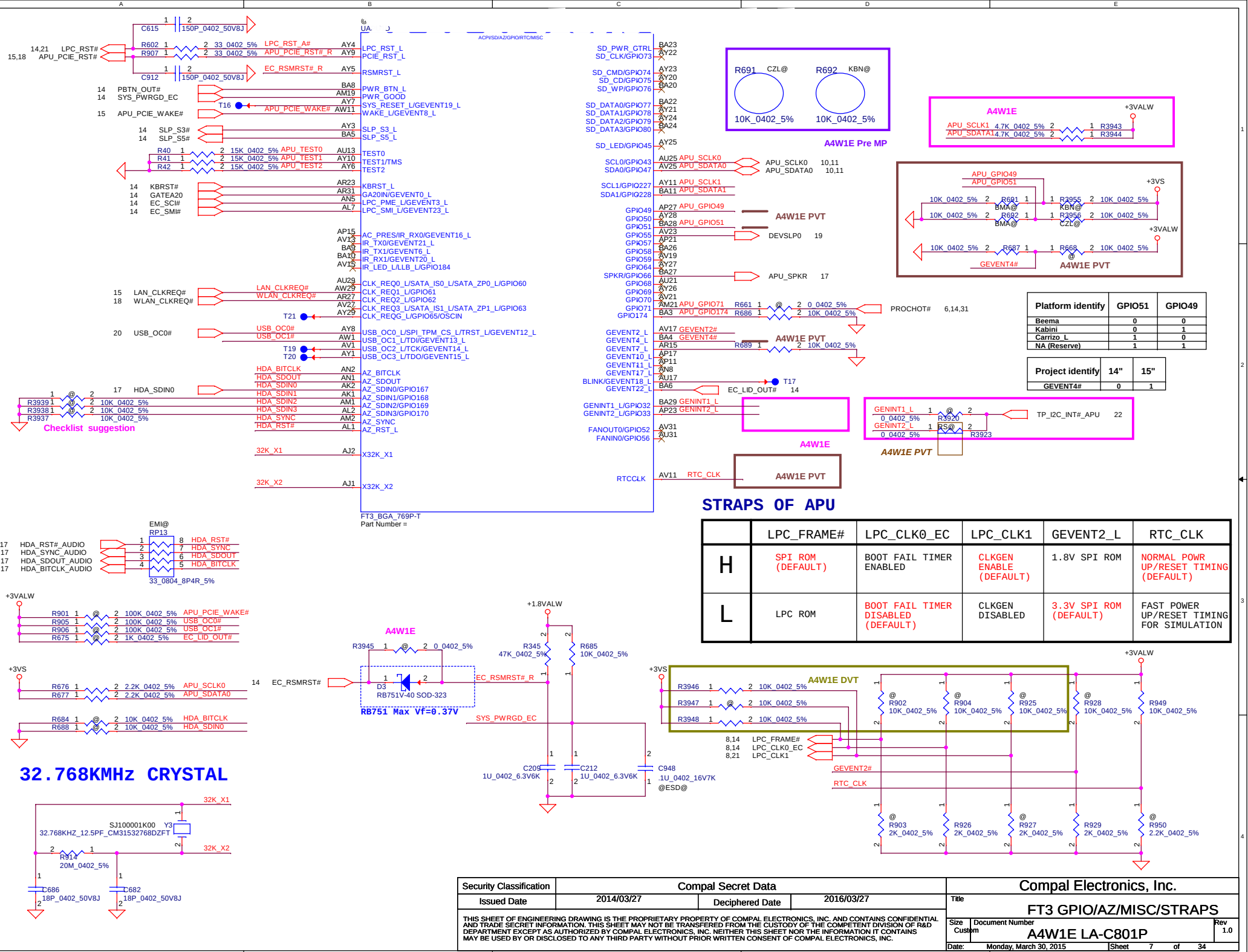
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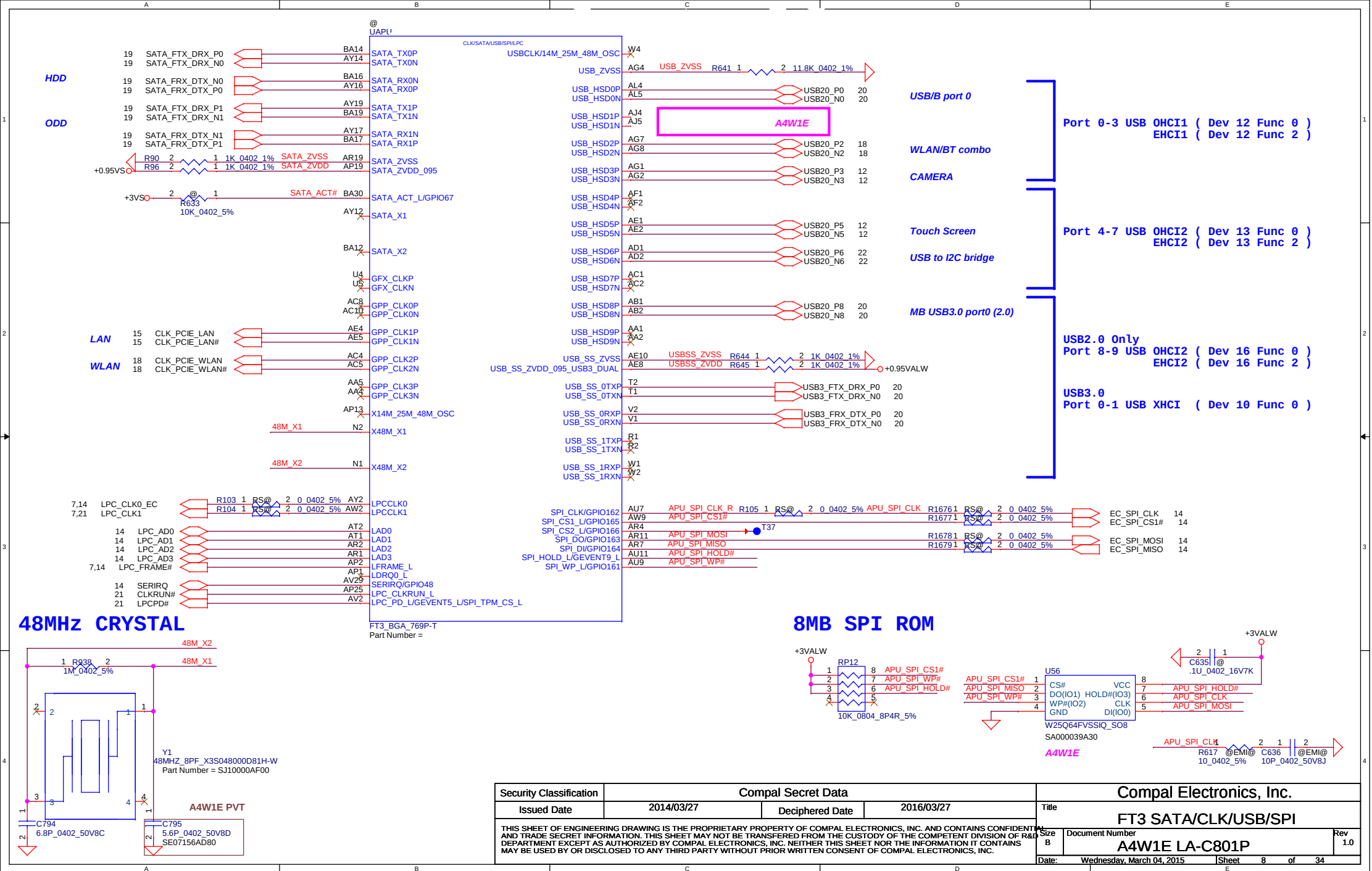
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Platform identify	GPIO51	GPIO49
Beema	0	0
Kabini	0	1
Carrizo L	1	0
NA (Reserve)	1	1

Project identify	14"	15"
GEVENT4#	0	1

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

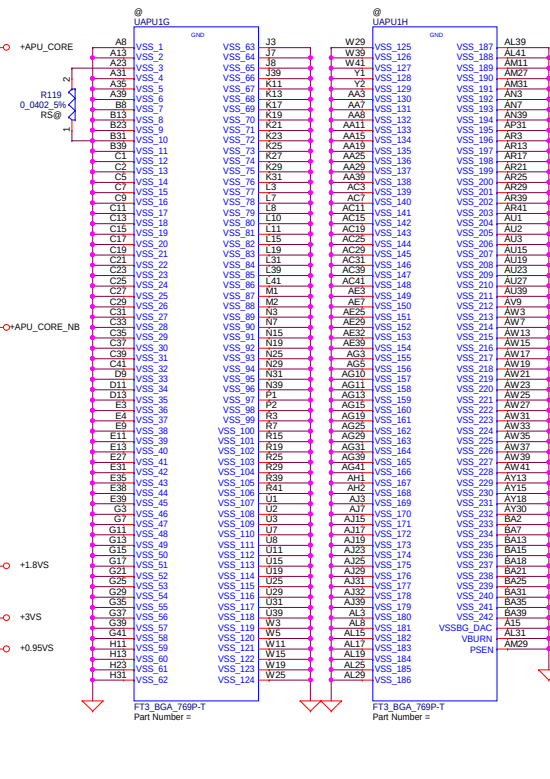


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FT3 SATA/CLK/USB/SPI								FT3 SATA/CLK/USB/SPI			
A4W1E PVT								A4W1E LA-C801P			
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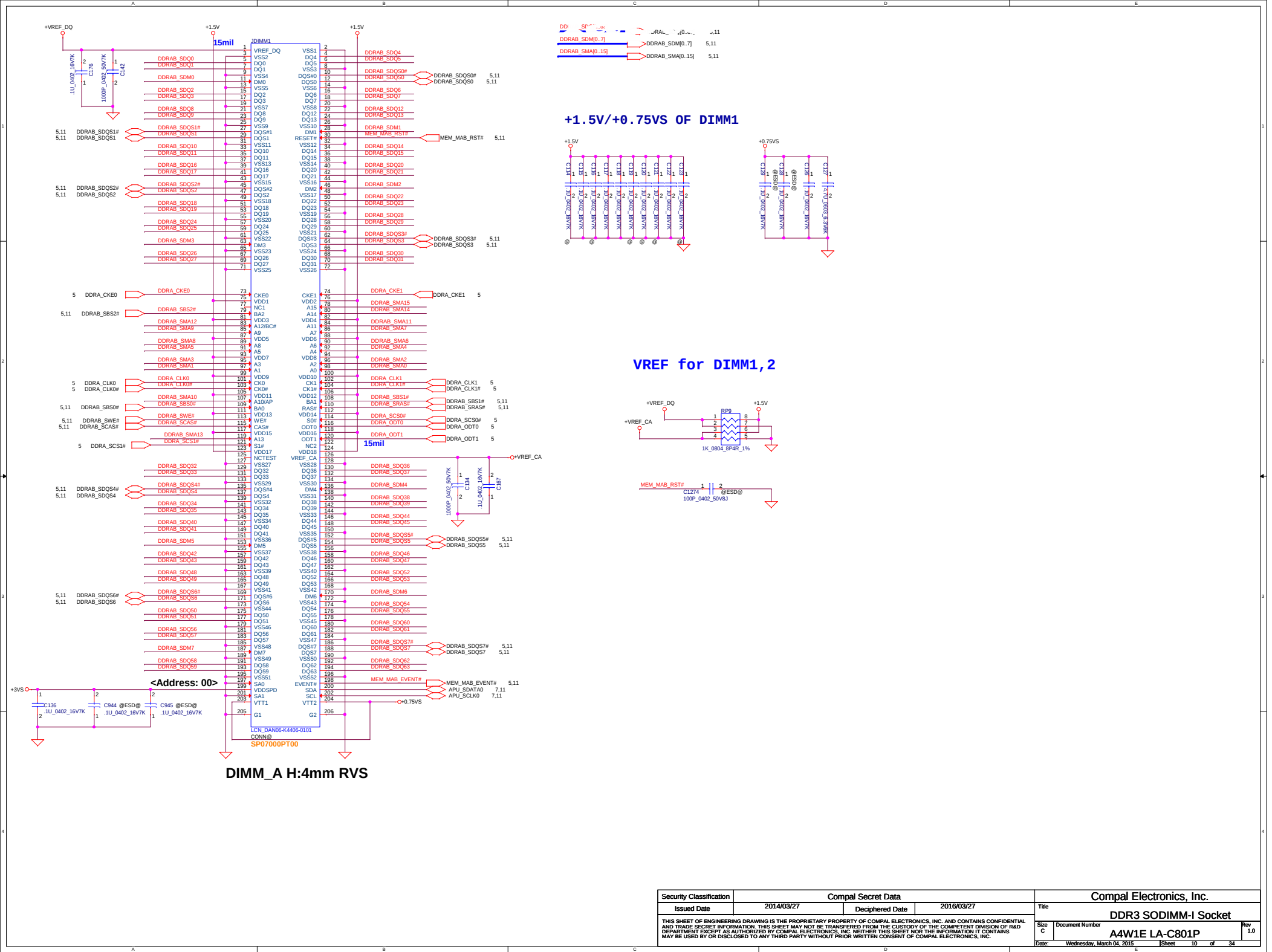
The schematic diagram illustrates the power supply network for the AD9288. It features two main power planes, VDD_095 and VDD_18, which are connected to a central ground plane. The VDD_095 plane is connected to a +0.95VS source, and the VDD_18 plane is connected to a +1.8VS source. Both planes are connected to the central ground plane via multiple vias. The ground plane is labeled 'GND' and 'GND@ESD@'. The VDD_095 plane is connected to the ground plane via 10 vias, and the VDD_18 plane is connected via 10 vias. The ground plane is also connected to a central ground plane via 10 vias.

VDDBT_RTC_G

The schematic shows a CMOS input buffer. The input node is connected to a pull-up resistor labeled "R93" with a value of "2 10K 0402 5%". This node also has a label "+RTC_APU" at the top right. A capacitor labeled "C166" with a value of "0.22UJ_0402_10V6K" is connected between the input node and ground. The input node is also labeled "W=28mils". The input signal is connected to pin 1 of a logic device. Pin 2 is connected to ground. Pin 3 is labeled "CLR/P1 SP @ SHORT PADS". Pin 4 is labeled "CLR/P2 SHORT PADS". The output of the device is connected to pin 1, which is also labeled "Need OPEN for clear CMOS". The output is connected to a resistor labeled "A4W1E".

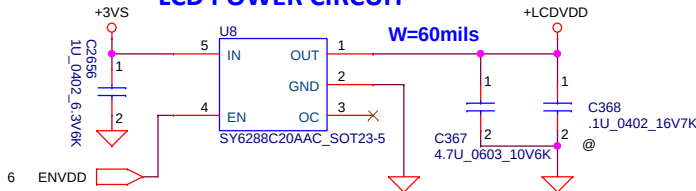


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FT3 PWR/GND			
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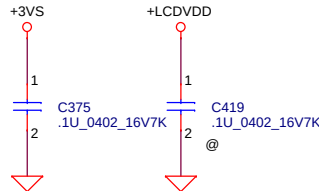


DIMM_B H:4mm STD

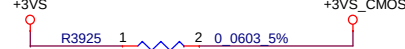
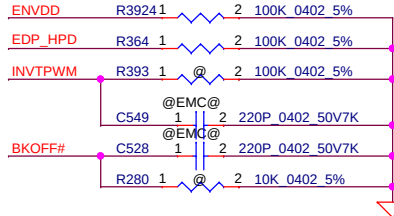
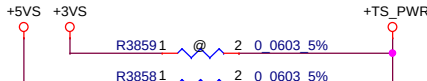
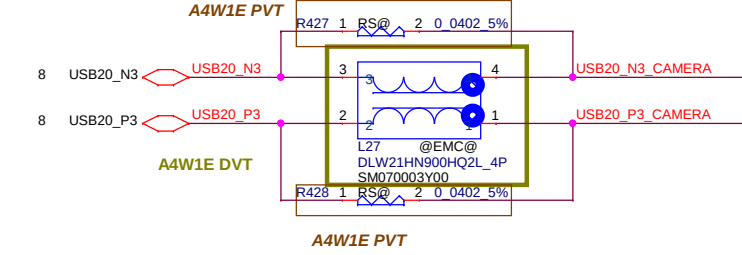
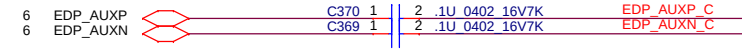
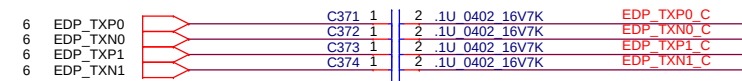
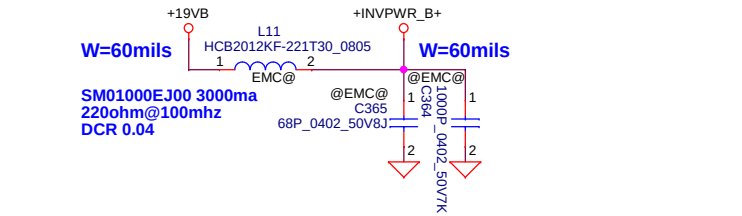
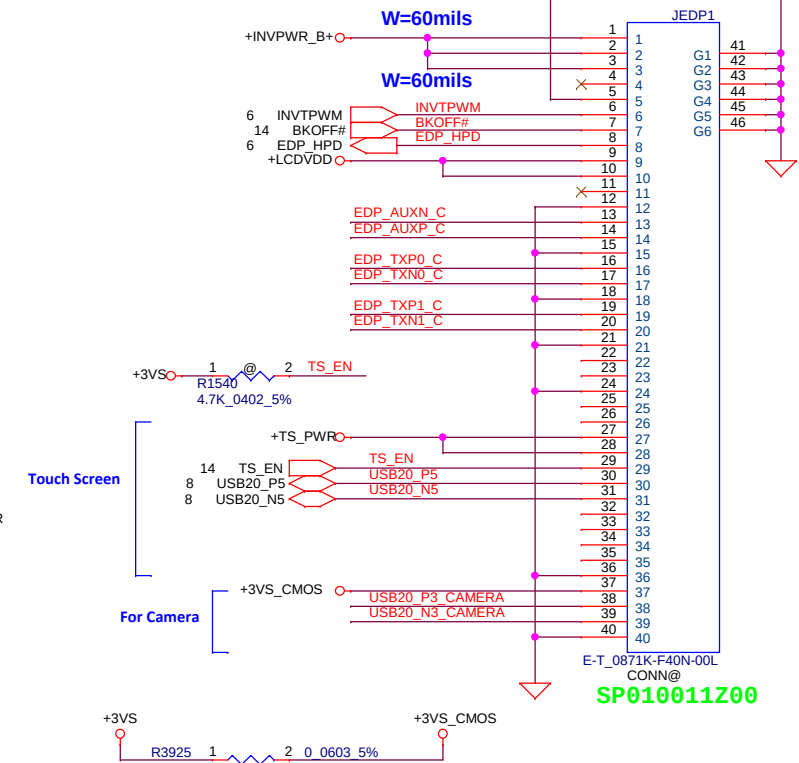
LCD POWER CIRCUIT



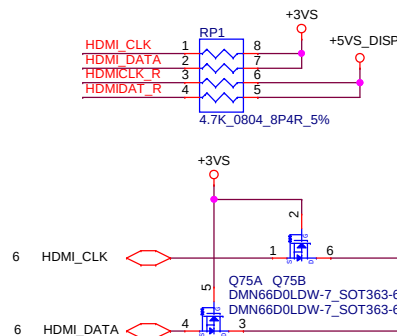
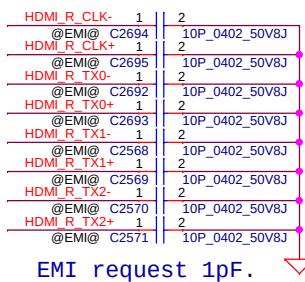
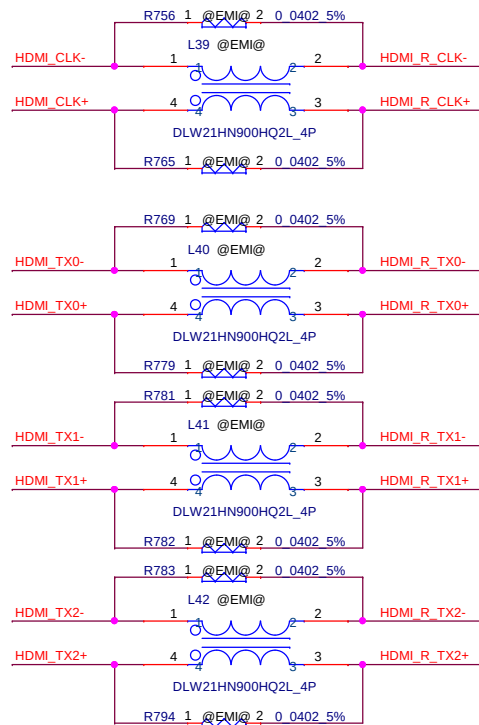
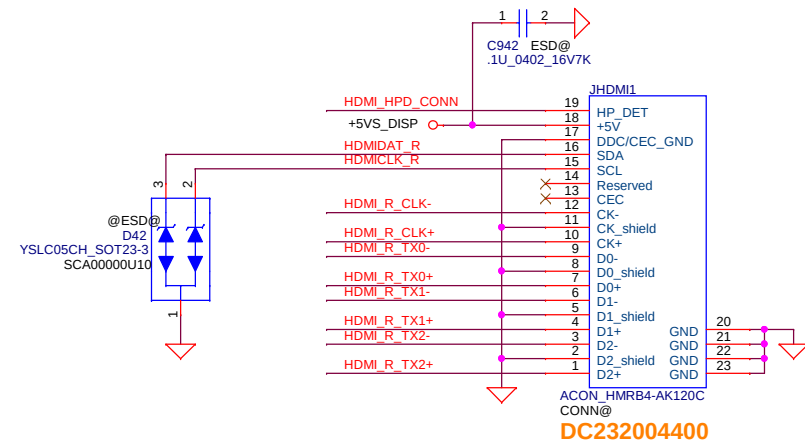
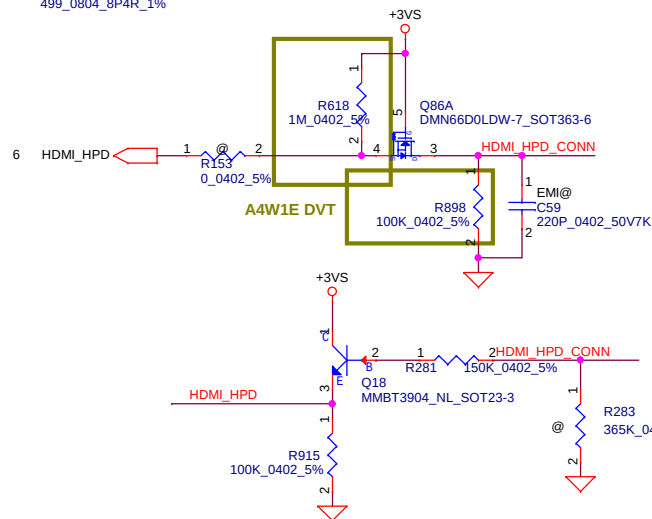
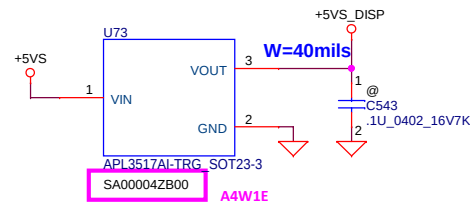
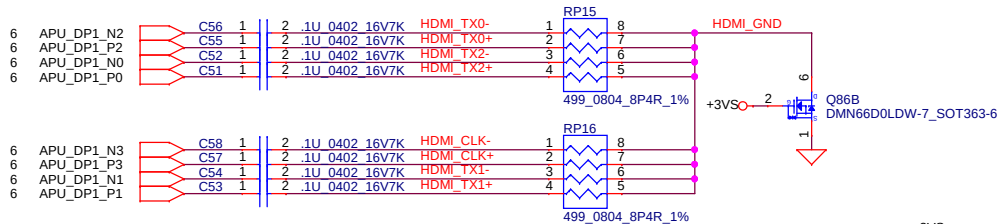
Place closed to JEDP1



LED PANEL Conn.



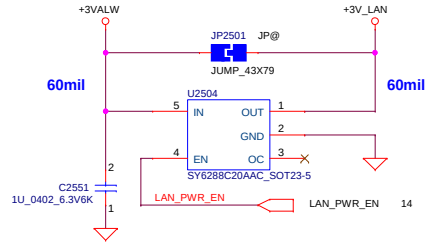
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EMI request 1pF.

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Size B		Document Number		Rev 1.0	
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LAN-RTL8411B

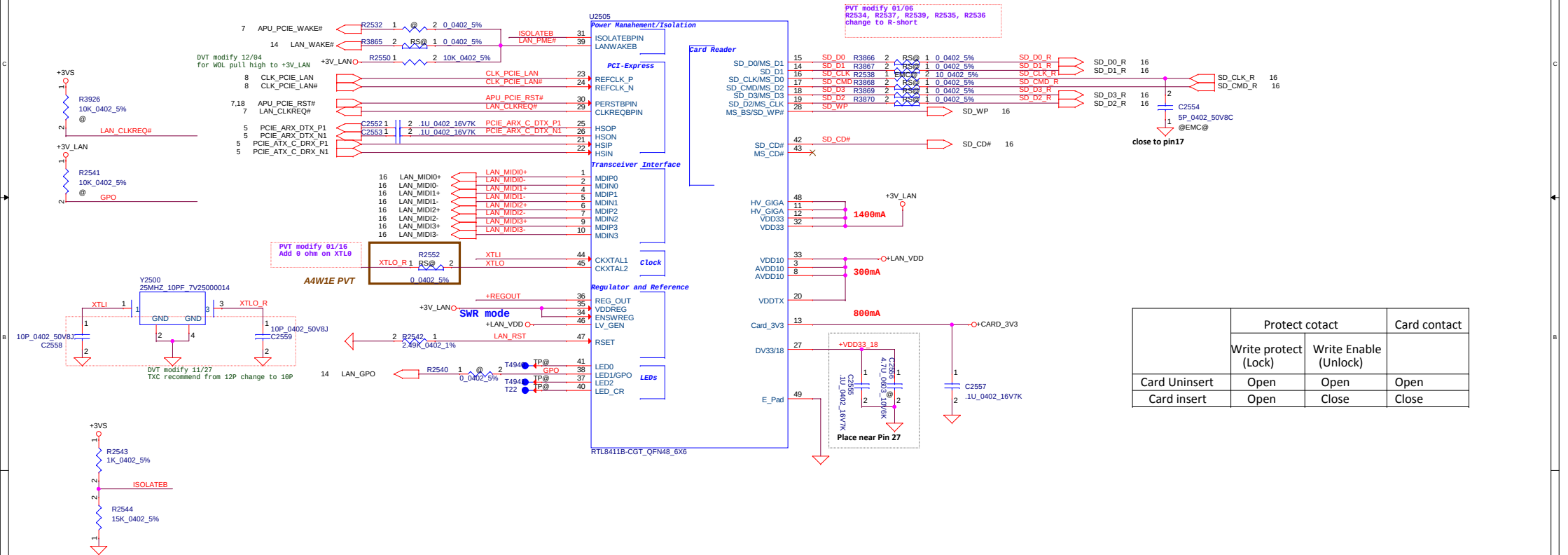
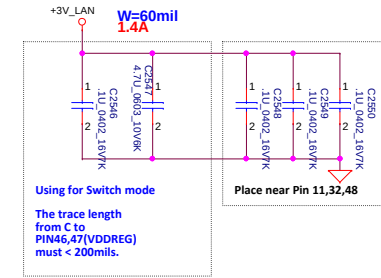
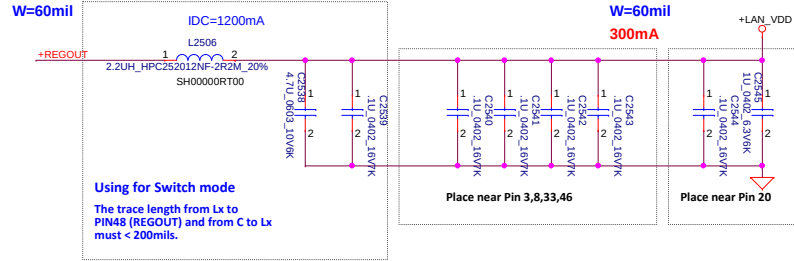


High active

High active.

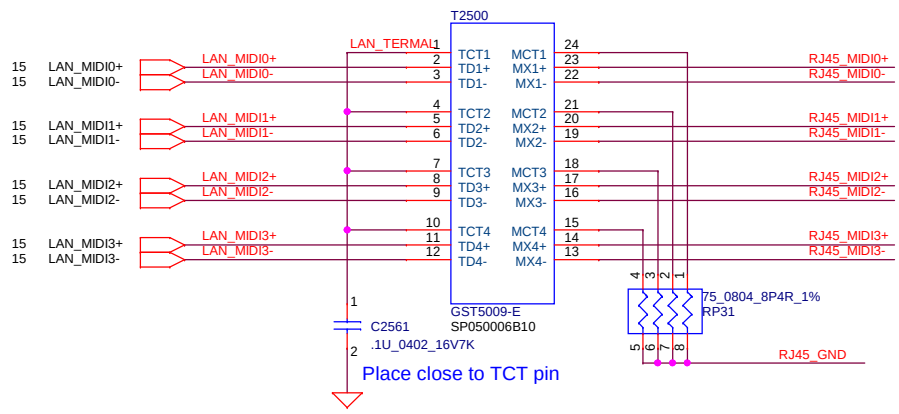
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must $>0.5\text{ms}$ and $<100\text{ms}$

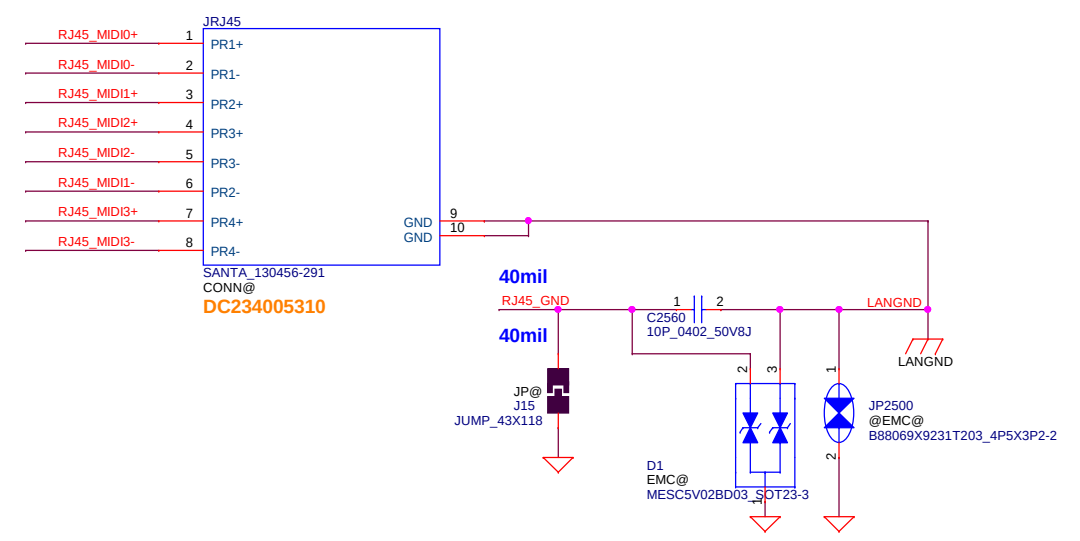


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

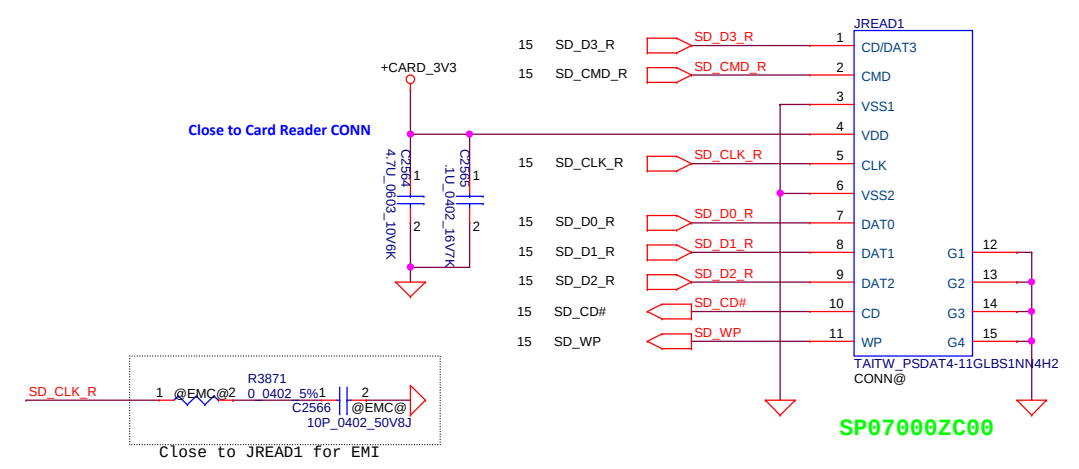
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LAN Connector



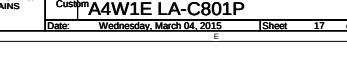
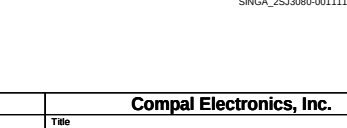
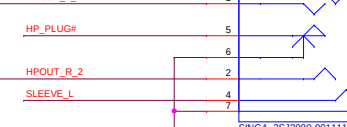
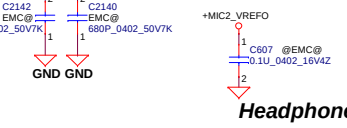
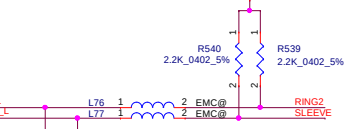
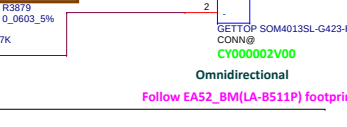
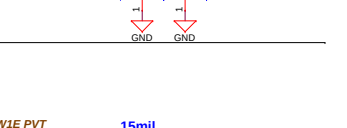
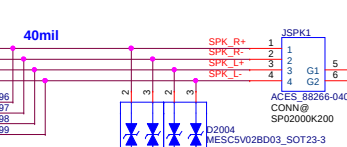
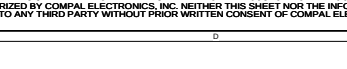
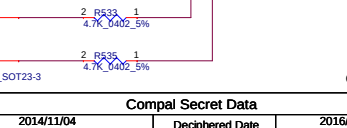
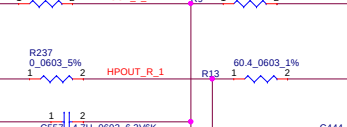
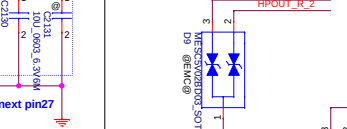
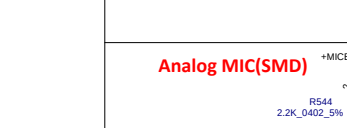
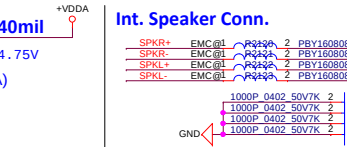
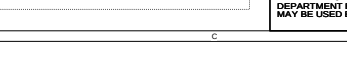
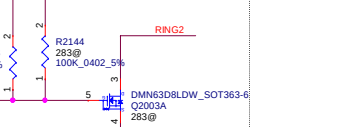
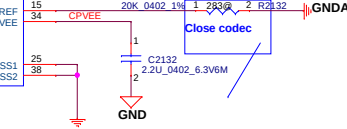
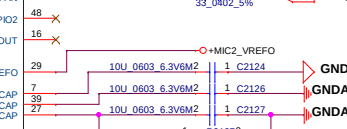
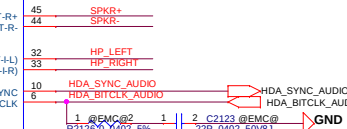
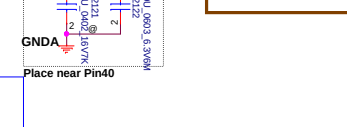
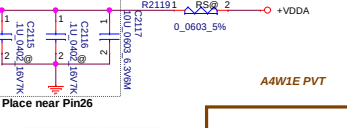
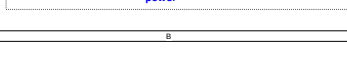
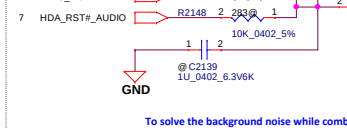
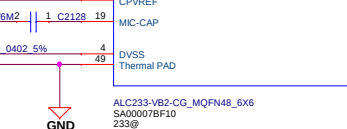
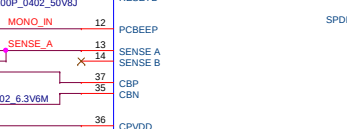
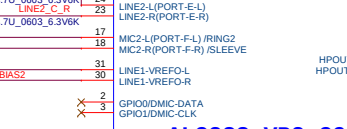
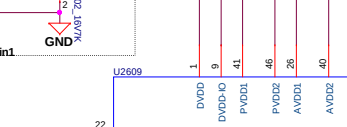
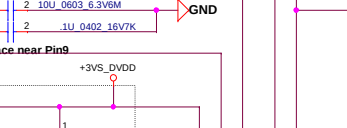
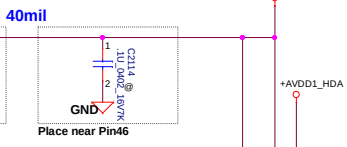
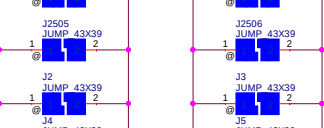
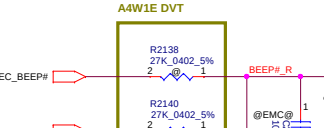
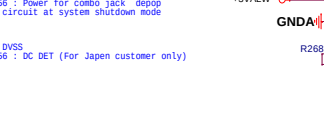
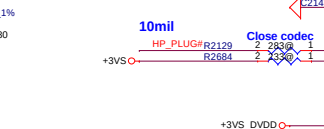
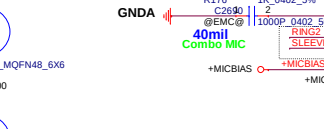
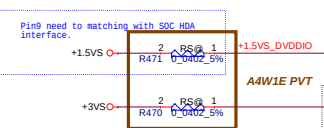
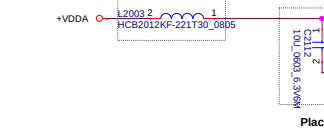
Card Reader Connector



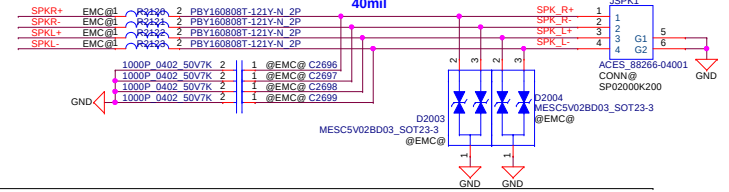
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/04	Deciphered Date	2016/11/04	Title	LAN RJ45/CR SD Connector	
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HD Audio Codec

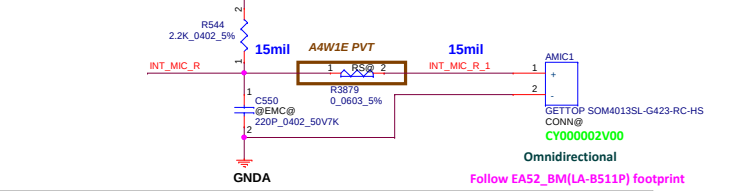
SM01000EJ00 3000ma 220ohm@100mhz DCR 0.04



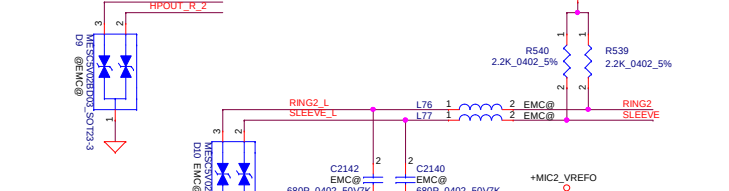
Int. Speaker Conn.



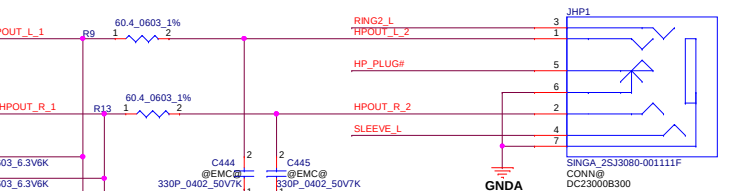
Analog MIC(SMD)



Headphone Out

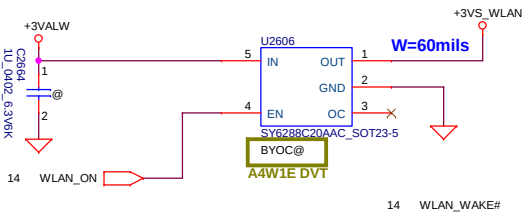


Headphone Out

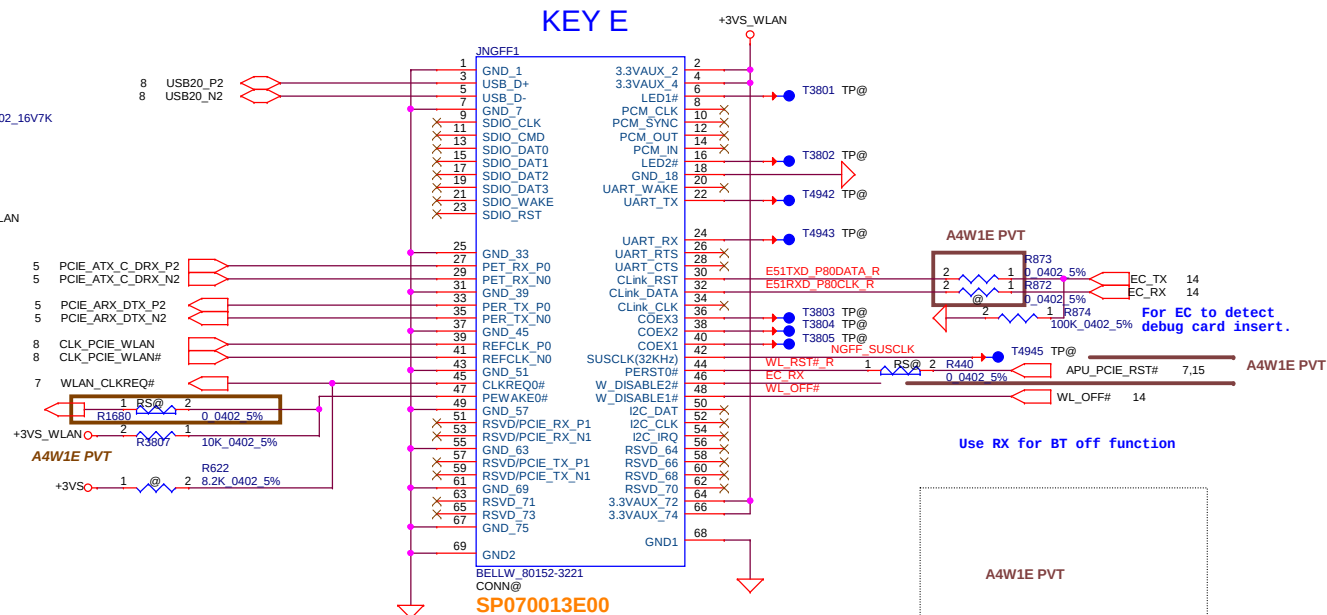


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Title		Compal Electronics, Inc.	
Size		HD Audio Codec ALC233-VB2	
Customer		A4W1E LA-C801P	
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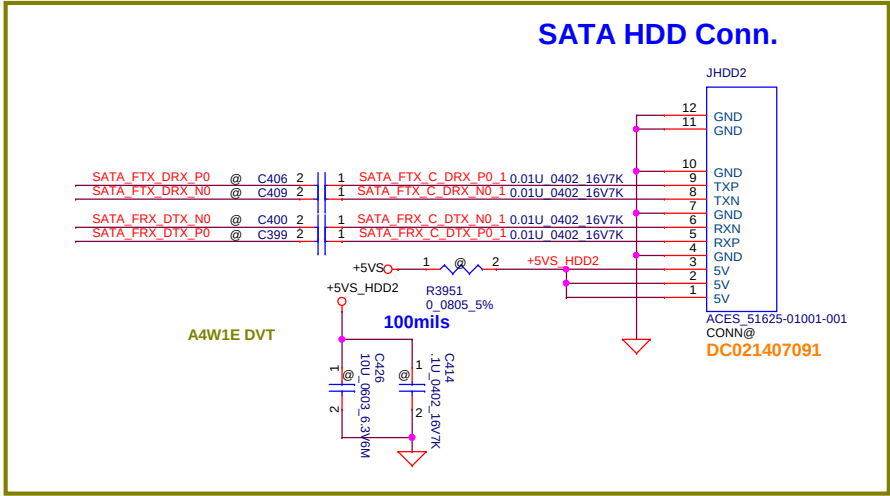
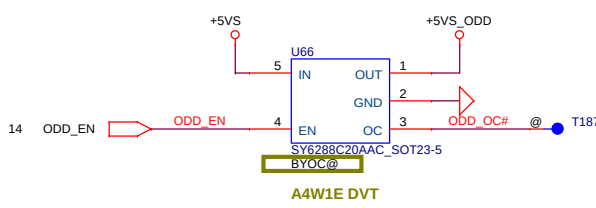
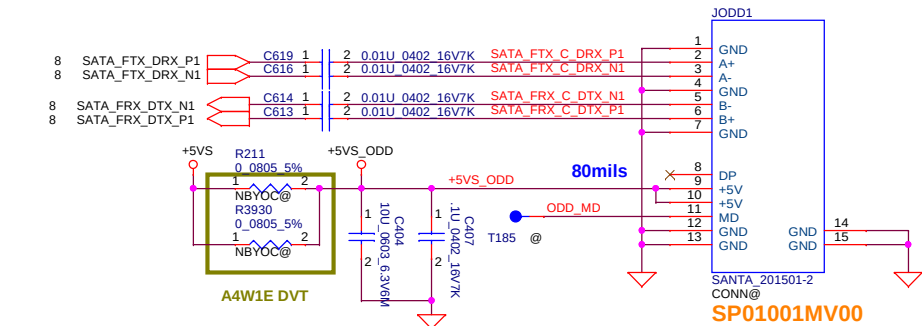
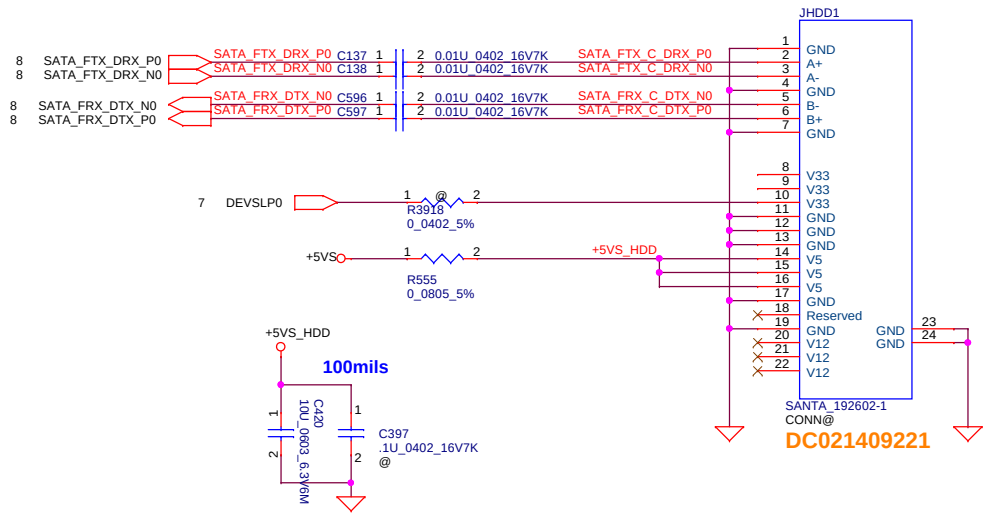
74	SRV	SRV	SRV	75
72	SRV	SRV	SRV	76
70	UM_Power_SRC/GPIO/PEWakeSt	SRV	SRV	77
68	UM_Power_SRC/GPIO/PEWakeSt	SRV	SRV	78
66	UM_Power_SRC/GPIO/PEWakeSt	SRV	SRV	79
64	RESERVED	SRV	SRV	80
62	ALERT0 (GPIO3.3)	SRV	SRV	81
60	OCCLK (GPIO3.3)	SRV	SRV	82
58	OCDATA (GPIO3.3)	SRV	SRV	83
56	WQ_DATAIN1 (GPIO3.3)	SRV	SRV	84
54	Reserved/PL2_DATAIN1 (GPIO3.3)	SRV	SRV	85
52	PERST0 (GPIO3.3)	SRV	SRV	86
50	SUSC120HPS (GPIO3.3)	SRV	SRV	87
48	CODEX1 (GPIO3.3)	SRV	SRV	88
46	CODEX2 (GPIO3.3)	SRV	SRV	89
44	CODEX3 (GPIO3.3)	SRV	SRV	90
42	VENDOR_DEFINED	SRV	SRV	91
40	VENDOR_DEFINED	SRV	SRV	92
38	VENDOR_DEFINED	SRV	SRV	93
36	UART15 (GPIO3.3)	SRV	SRV	94
34	UART16 (GPIO3.3)	SRV	SRV	95
32	UART17 (GPIO3.3)	SRV	SRV	96
30	UART18 (GPIO3.3)	SRV	SRV	97
28	UART19 (GPIO3.3)	SRV	SRV	98
26	UART20 (GPIO3.3)	SRV	SRV	99
24	UART21 (GPIO3.3)	SRV	SRV	100
22	UART22 (GPIO3.3)	SRV	SRV	101
20	UART23 (GPIO3.3)	SRV	SRV	102
18	SRV	SRV	SRV	103
16	SRV	SRV	SRV	104
14	PCMC1_OUT25 (GPIO3.3)	SRV	SRV	105
12	PCMC1_OUT26 (GPIO3.3)	SRV	SRV	106
10	PCMC1_OUT27 (GPIO3.3)	SRV	SRV	107
8	PCMC1_OUT28 (GPIO3.3)	SRV	SRV	108
6	SRV	SRV	SRV	109
4	SRV	SRV	SRV	110
2	SRV	SRV	SRV	111



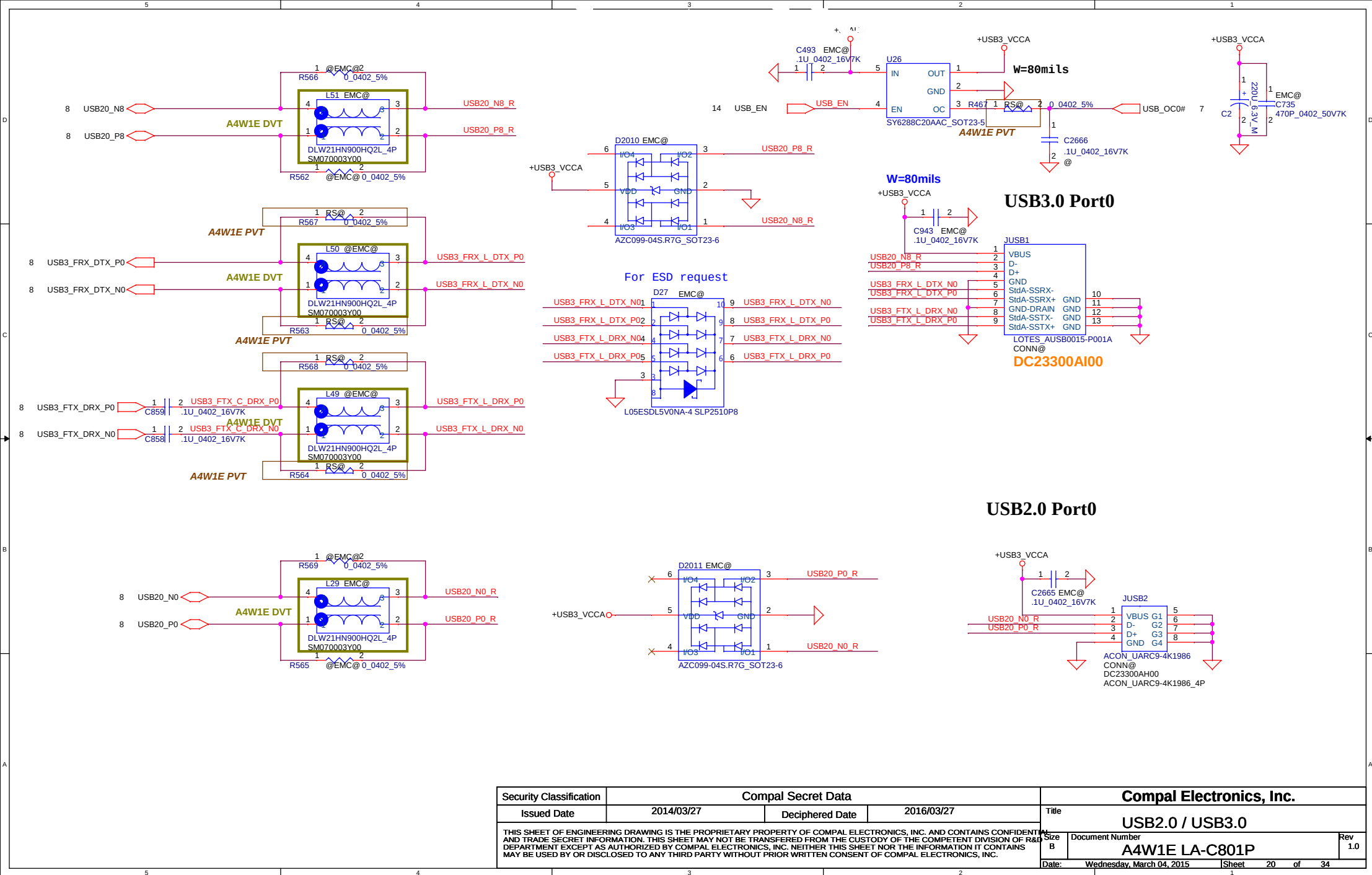
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M.2 Key E (WLAN)			
Size	Document Number	Rev	
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SATA HDD Conn.

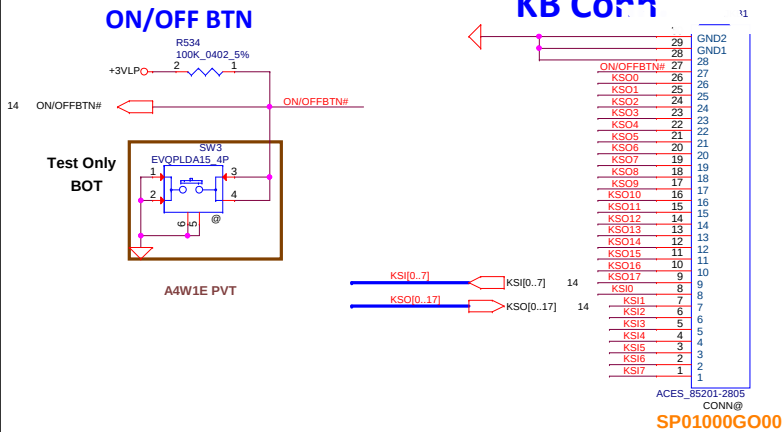
SATA ODD Conn.



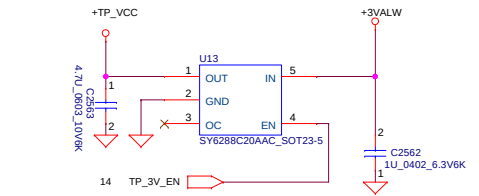
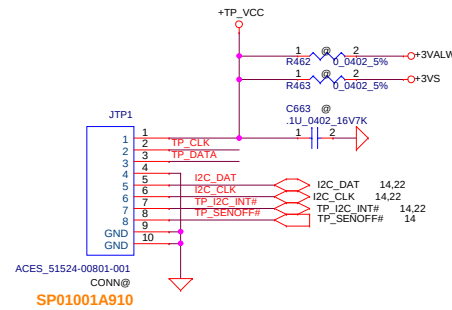
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2014/11/04		2016/11/04		HDD/ODD	
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A4W1E DVT		A4W1E LA-C801P		0.1	
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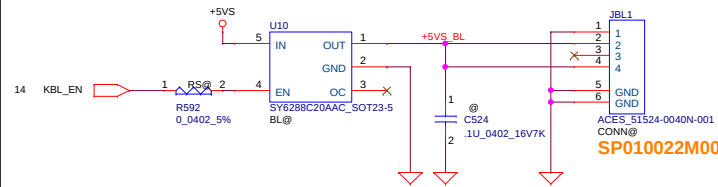
ON/OFF BTN



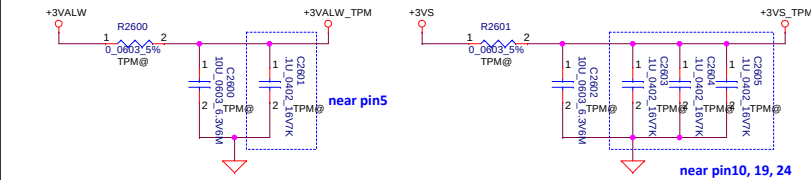
TP/TP Conn



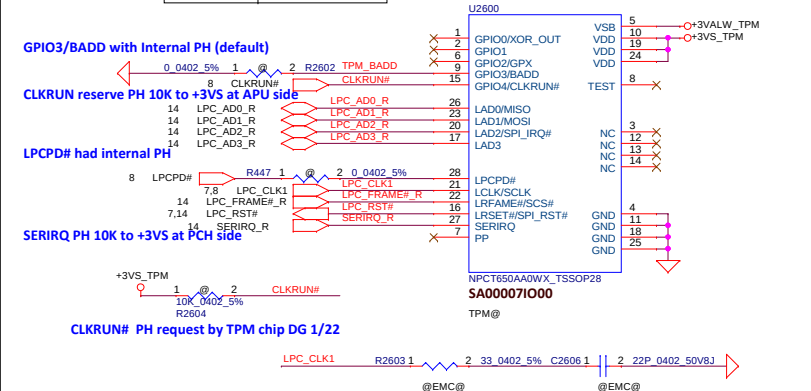
KB BackLight Conn. Reserve



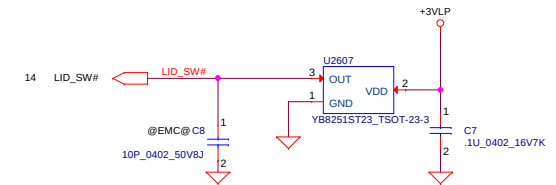
TPM Board for 2015



BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



Lid Switch (Hall Effect Switch)



Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

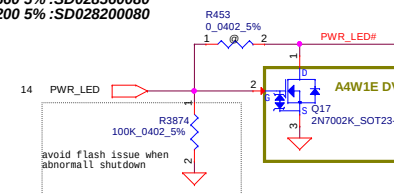
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

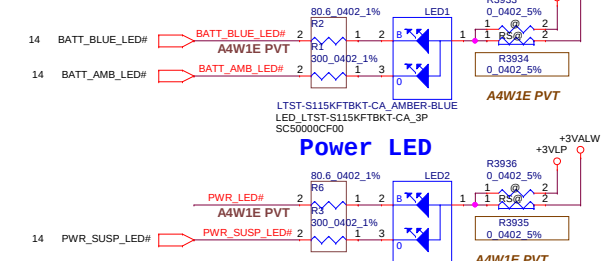
CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080

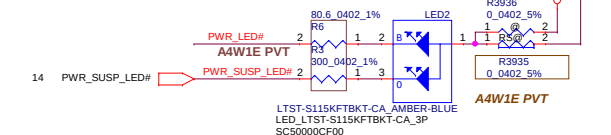
LED



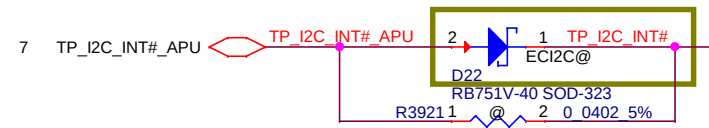
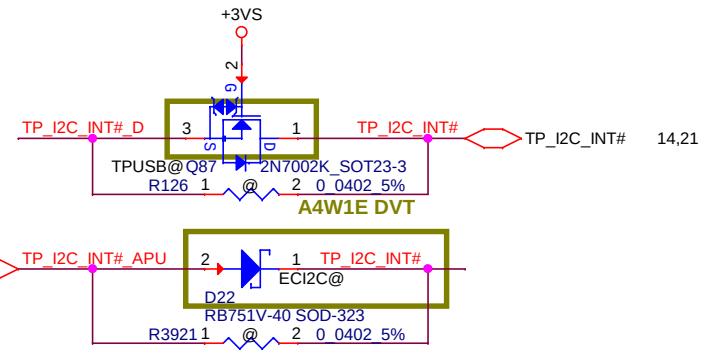
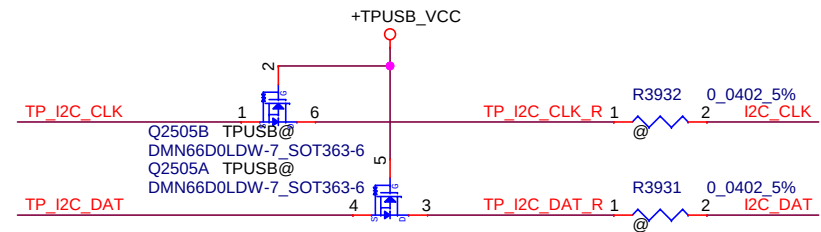
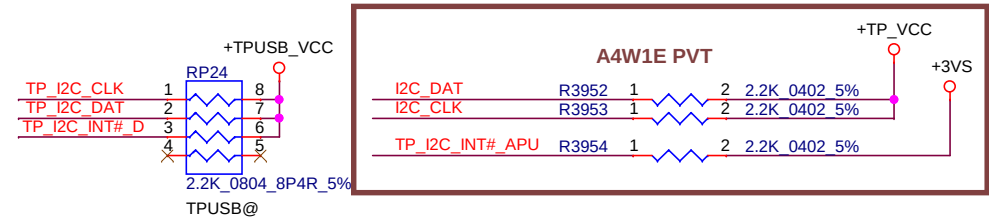
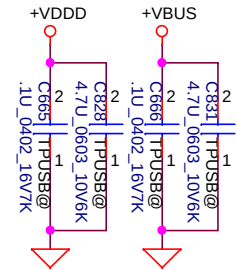
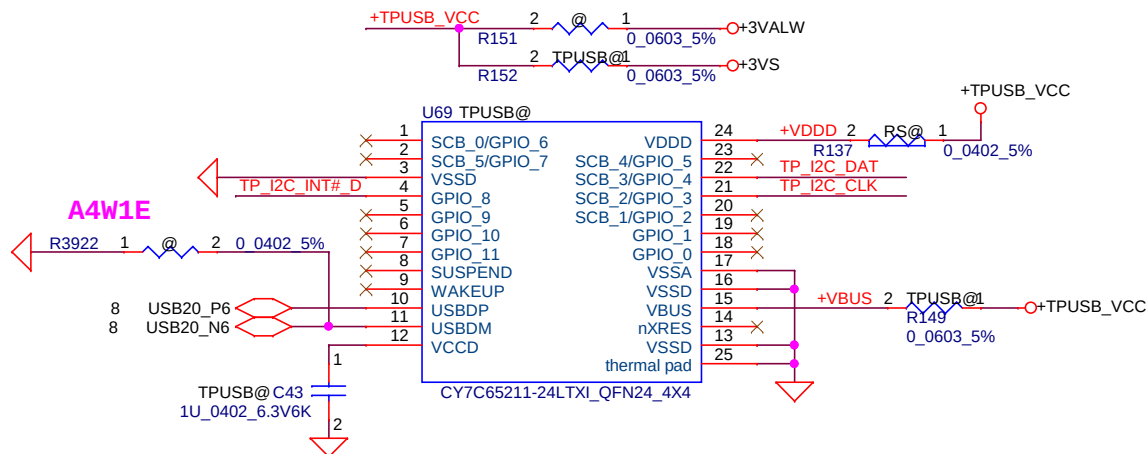
Battery LED



Power LED

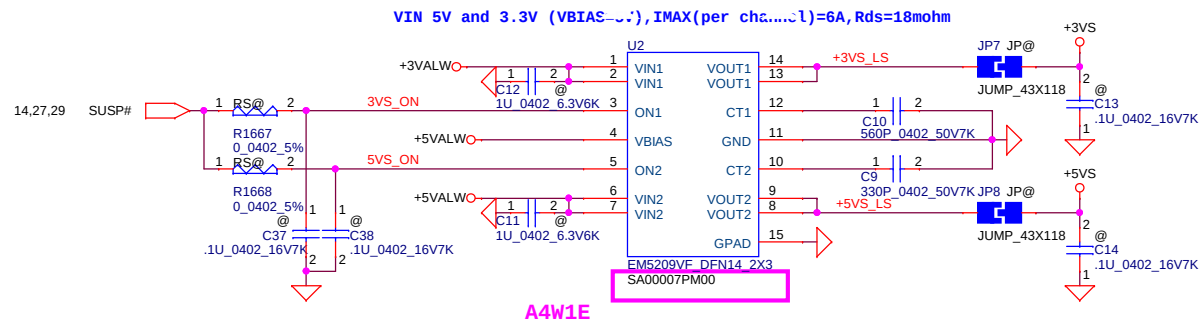


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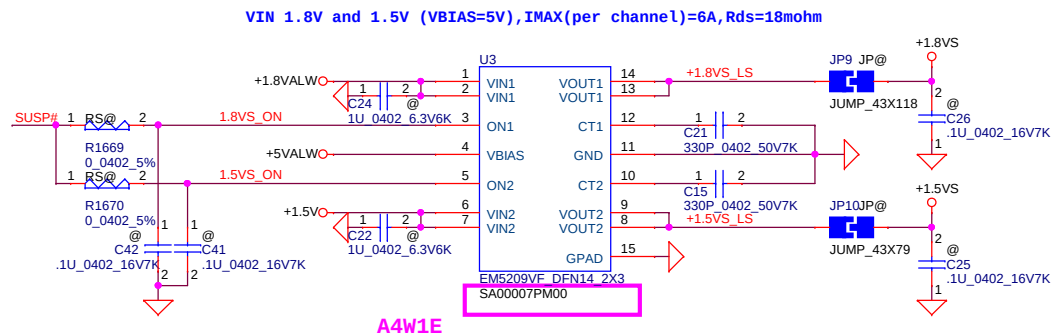


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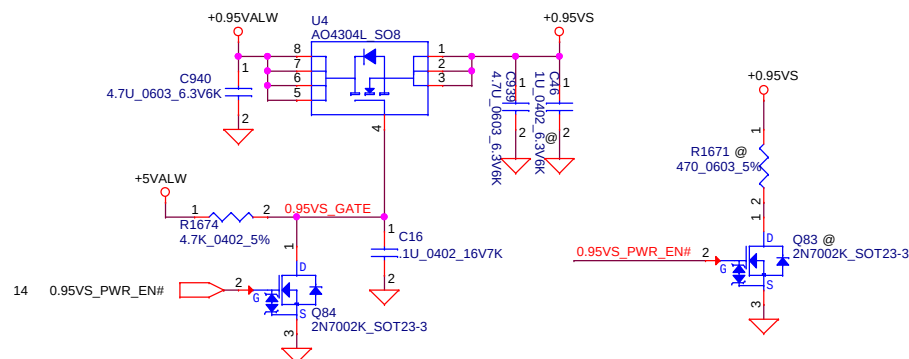
**+5VALW TO +5VS
+3VALW TO +3VS
Load switch**



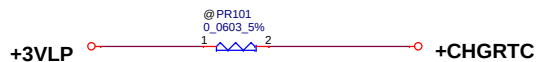
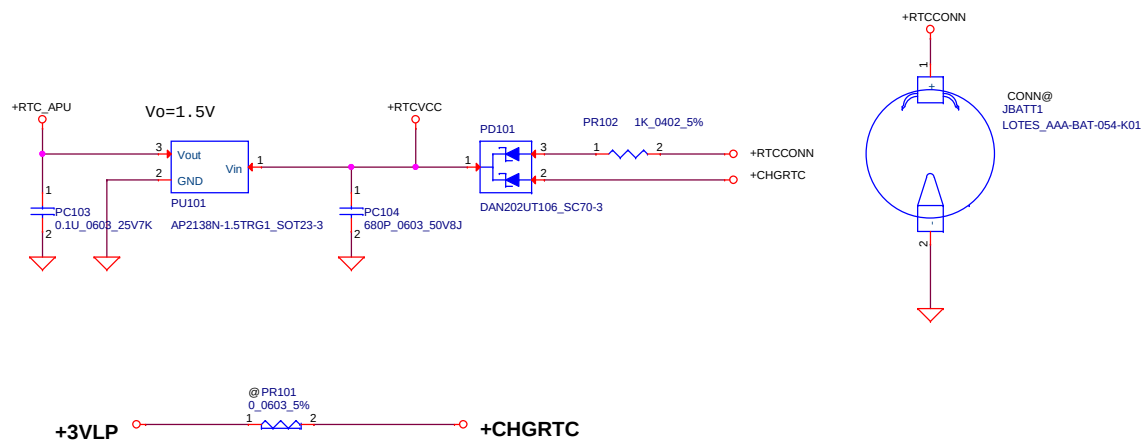
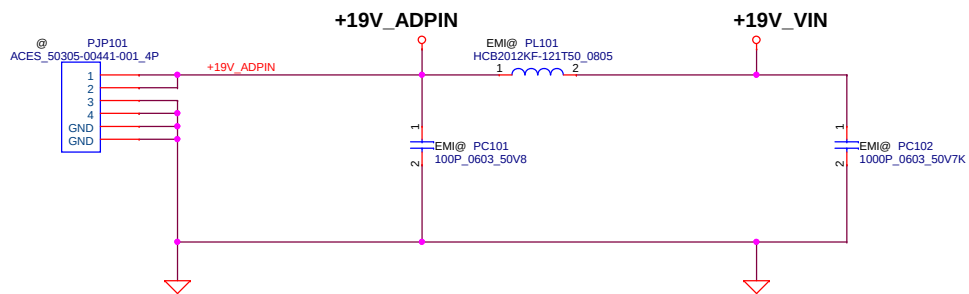
**+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch**



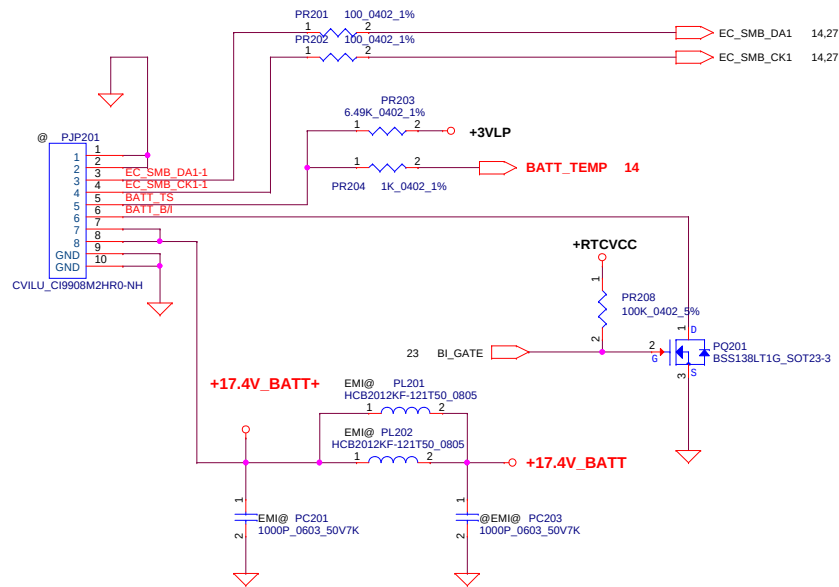
+0.95VALW to +0.95VS



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---Battery_pin define---

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

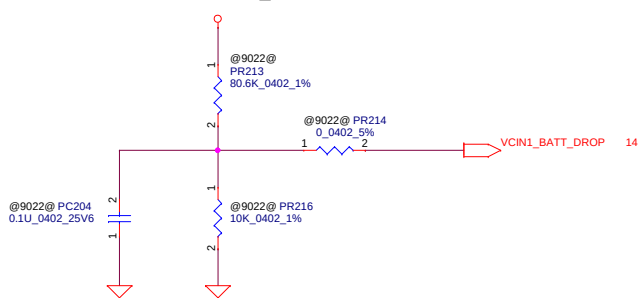
---Battery Con_pin define---

PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design

+19VB_5V



For 45W adapter==>action 48.15W , Recovery 38.7W

48.15W:
 $I_{ada} = 0 \sim 2.253A$ ($48.15W/19V=2.534A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.534 * 0.02 = 1.01$
38.7W:
 $I_{ada} = 0 \sim 2.036A$ ($38.7W/19V=2.036A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.036 * 0.02 = 0.814$

$CP = 45W * 0.85 = 38.25W$

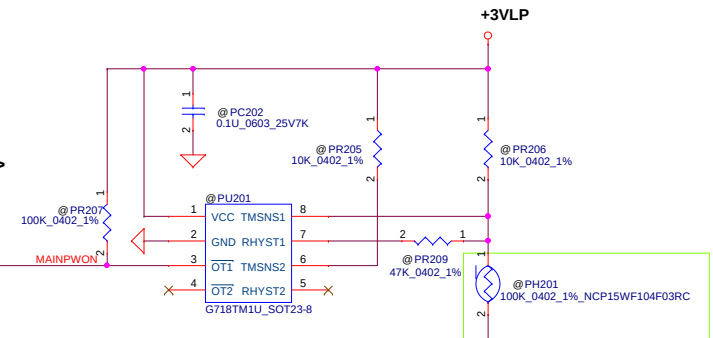
For 65W adapter==>action 69.55W , Recovery 55.9W

69.55W:
 $I_{ada} = 0 \sim 3.661A$ ($69.55W/19V=3.661A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 3.661 * 0.02 = 1.464$
55.9W:
 $I_{ada} = 0 \sim 2.942A$ ($55.9W/19V=2.942A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.942 * 0.02 = 1.177$

$CP = 65W * 0.85 = 55.25W$

<45, 47>

14,23,28 MAINPWON

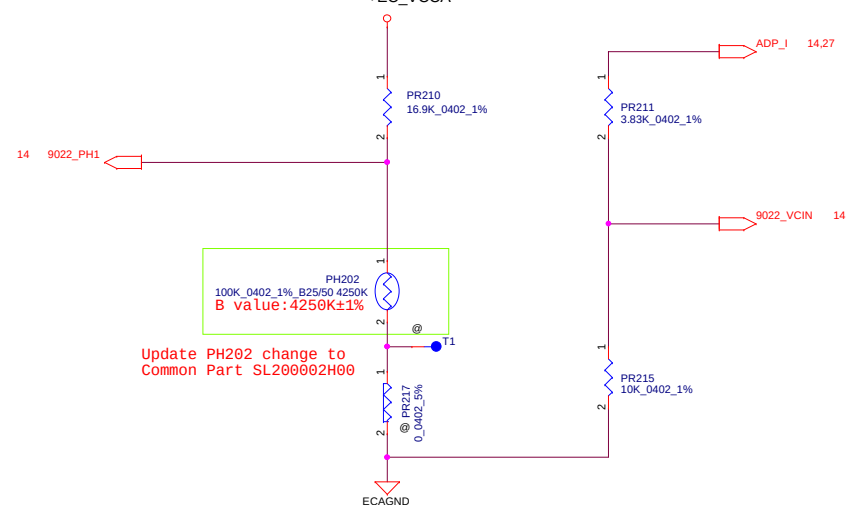


Update PH201 change to
Common Part SL200002H00

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.V
PH202(ohm)	7.3K	26.11K

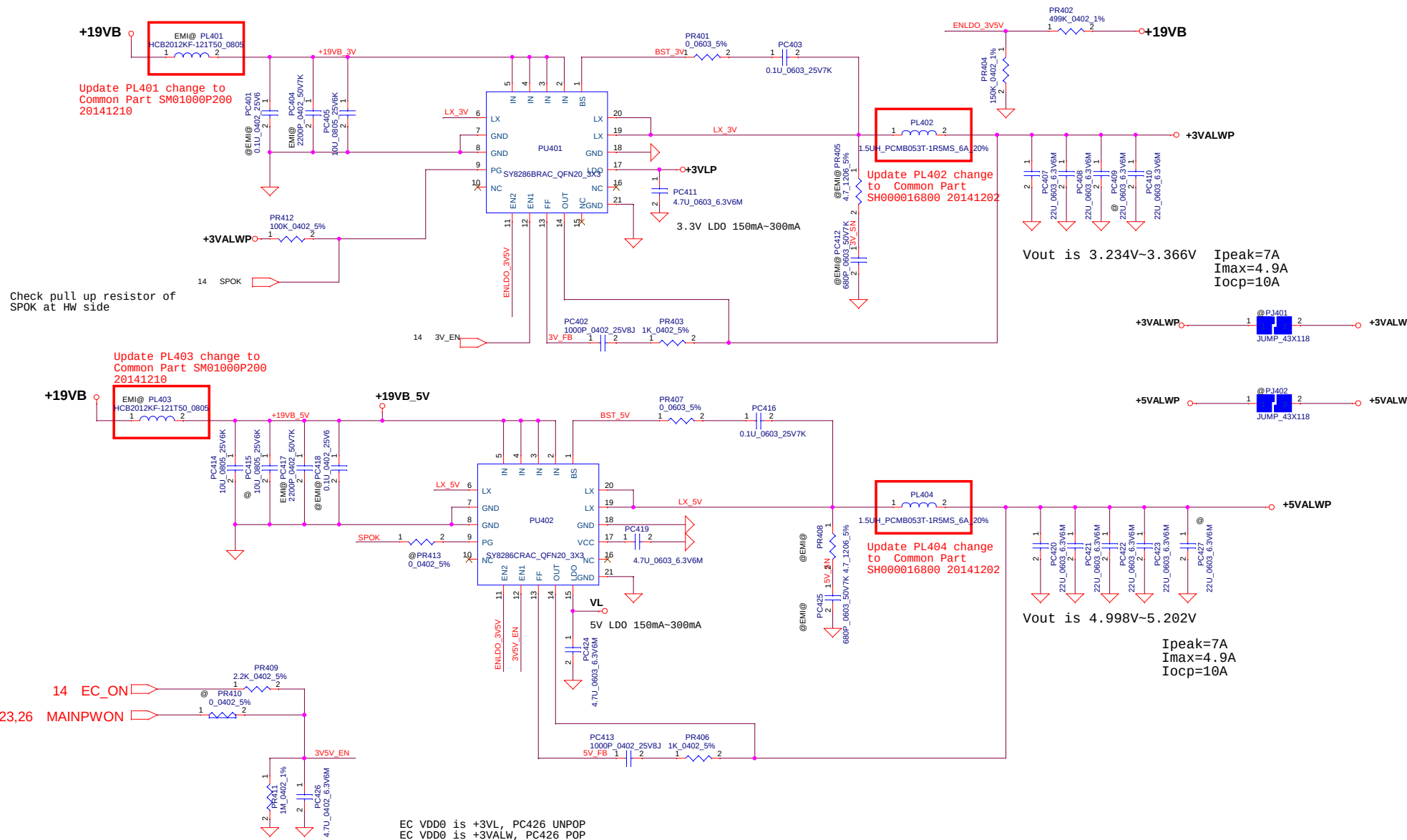
For KB9012 sense 20mΩ	Active	Recovery
45W	48.15W, 0.73V	38.7W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

PH202 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



Update PH202 change to
Common Part SL200002H00

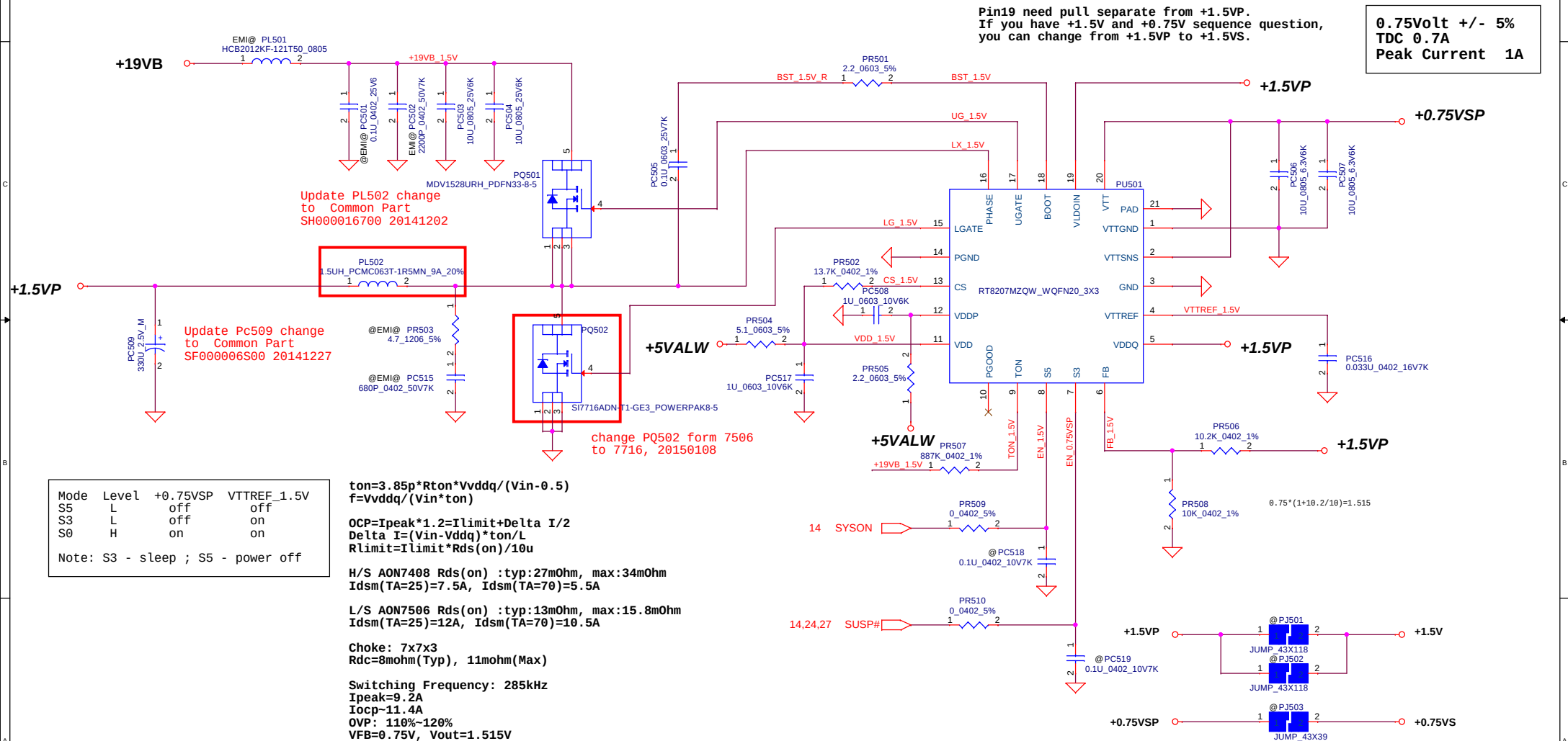
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

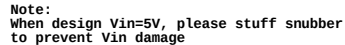


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The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VDDP_ALW_VCTRL	VDDPALW
1	1.062V
0	0.96V


$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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2013/10/16 Modify
PQ801,PQ803 change to AON6552.
PQ802,PQ804,PQ805 change to AON6554.

Module model information
RT8880A_V1A.mdd for IC portion
RT8880A_V1B.mdd for SW portion

2013/10/22 Modify
PH801,PH802 change to common part.

Close to Control IC

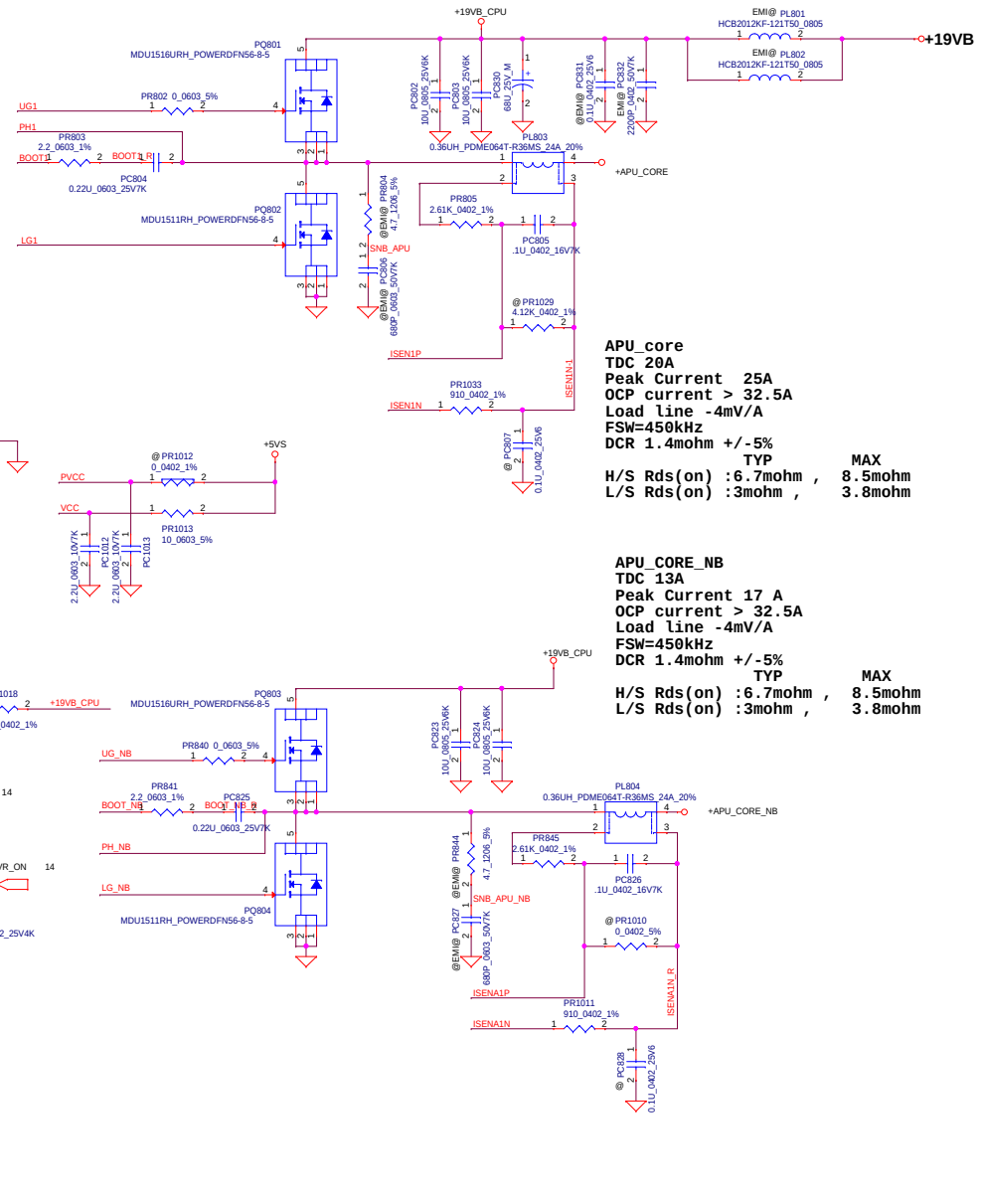
close to PL803

close to PL804

Pull high at HW side

PR1030=80.6K
LL=3.92m

Delete PR834.PR835.PR836.PR839.PR840.PR841,
follow vender FAE suggest.
2013/11/29 modify.



APU_core
TDC 20A
Peak Current > 25A
OCP current > 32.5A
Load line -4mV/A
FSW=450kHz
DCR 1.4mohm +/- 5%
TYP
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm

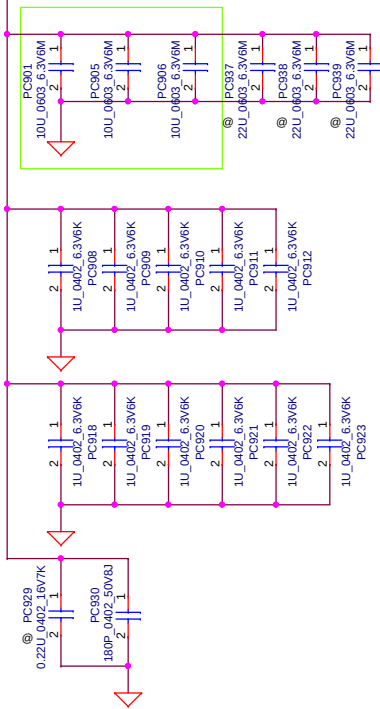
APU_CORE_NB
TDC 13A
Peak Current 17 A
OCP current > 32.5A
Load line -4mV/A
FSW=450kHz
DCR 1.4mohm +/- 5%
TYP
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm

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2012/06/19		2012/07/31		CPU CORE	
Size		Document Number		Rev	
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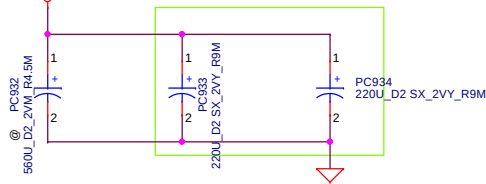
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+APU_CORE (36.4)

+APU_CORE

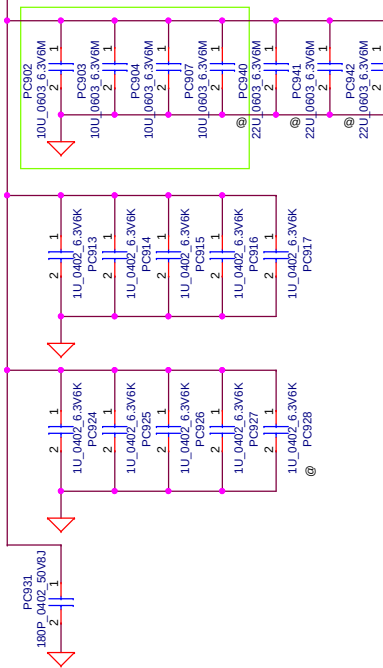


+APU_CORE

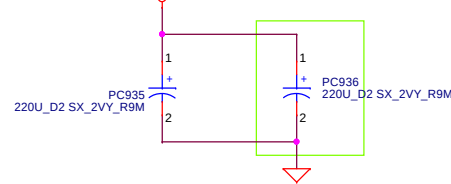


+APU_CORE_NB (36.5)

+APU_CORE_NB



+APU_CORE_NB



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for PWR

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Item	Page	Date	Reason for change	Phase
01	06	2015/01/05	For AMD Beema and Kabini APU colay	DVT
02	14	2015/01/05	Board ID update from 0 to 1	
03	19	2015/01/05	HDD connector too close to speaker	
04	07	2015/01/12	Power leakage when S3/S4/S5	
05	13	2015/01/19	HDMI test	
06	14	2015/01/19	For AMD Beema and Kabini APU colay	
07	21	2015/01/23	Layout PCB footprint correct	
08	11	2015/01/27	BOM update for DDR 1.5V power	
09	12,20	2015/01/27	BOM update as source request (SM070003K00->X1)	
10	17	2015/01/27	PC Beep issue on DOS mode	
11	21,22	2015/01/27	BOM update to Main source	
12	14	2015/01/27	BOM update to Main source	
13	18	2015/01/27	BOM structure update for BYOC/NBYOC	
14	19	2015/01/27	BOM structure update for BYOC/NBYOC	
15	14	2015/02/25	Board ID update from 1 to 2	PVT
16	22	2015/02/25	Debug convenience	
17	18	2015/02/25	Intel WLAN module request(pin 32 & 46 disconnect)	
18	18	2015/02/25	Remove un-used net from WLAN	
19	08	2015/02/25	48MHz crystal tolerance fine tune	
20	07	2015/02/25	To identify project(14" & 15")	
21	07	2015/02/25	To identify platform(Beema/Kabini)	
22	21	2015/02/25	LED brightness test result	
23	23	2015/03/01	ME drawing update	
24		2015/03/04	Part count request	
25	21	2015/03/10	Unstuff un-used component for PCB R1.0	
26	14	2015/03/30	Board ID update from 2 to 3	Pre MP
27	04	2015/03/30	PCB part number update to 1A	