NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

VELLFIRE

2020.06.05

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION MAIN BOARD		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 1 of 139			

TABLE OF CONTENTS

SMALL BOARD1&2

SMALL BOARD3

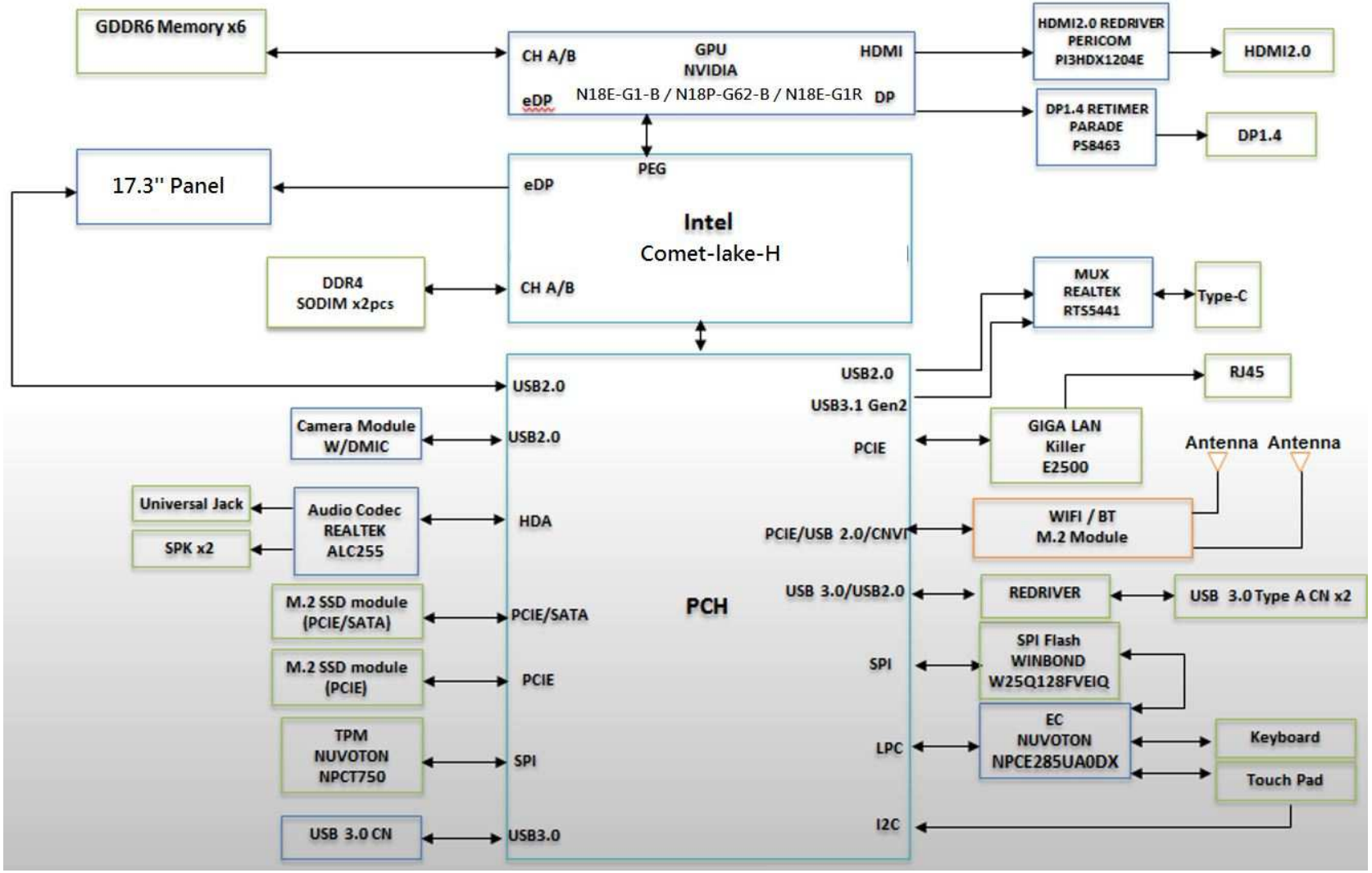
FOR 17 SMALL BOARD1&2

GPU PAGE 71-116 FROM PAGE 72

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF THE CONTENT

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 2 of 139			



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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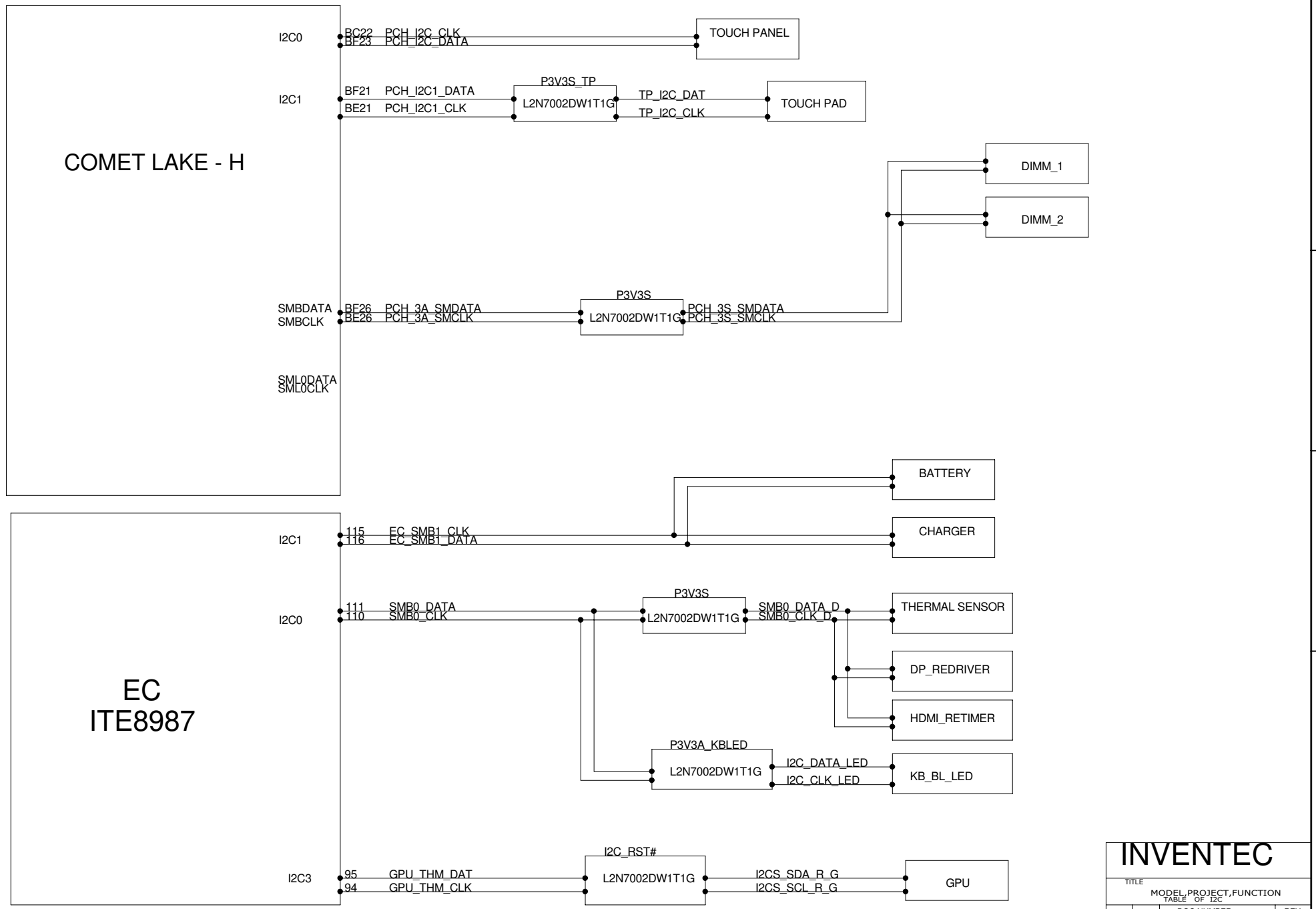

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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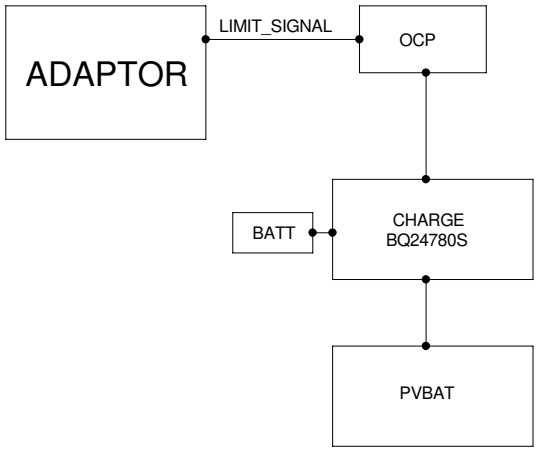
POWER BLOCK



IN/EN		OUT
PVBAT, EN_5V	SY8288CRAC	P5V0DS
PVBAT, EN_5V0	SY8284CRAC	P5V0
PVBAT, EN_3V	NB680AGD	P3V3DS
PVBAT, EN_VDDQ, EN_VTT	NB685AGQ	P1V2, P0V6S
PVBAT, EN_1V05V	SY8288CRAC	P1V05A
PVBAT, EN_VCCIO	NB681GD	PVCCIO
PVBAT, EN_PVCORE	NCP81215MNTXG	PVCORE
PVBAT, VRACPU_DRVON	NCP81151MNTBG	PVCCGT
PVBAT, VRACPU_DRVON	NCP81253MNTBG	PVCCSA

IN/EN		OUT
P5V0DS, EN_2V5	RT8097ALGE	P2V5
P3V3DS, EN_1V8	SY8088AAC	P1V8A
P3V3DS, P3V3A_5A_PWEN, CORE_PWEN	APL3523A	P3V3A, P3V3S
P5V0DS, CORE_PWEN, P1V8A, CORE_PWEN	APL3523A	P5V0S, P1V8S
P1V2, VCCPLL_OC_EN	PM514BA	VCCPLL_OC
P1V05A, RESUME_PWEN, CORE_PWEN	APL3523A	PVCCSTG, PVCCST

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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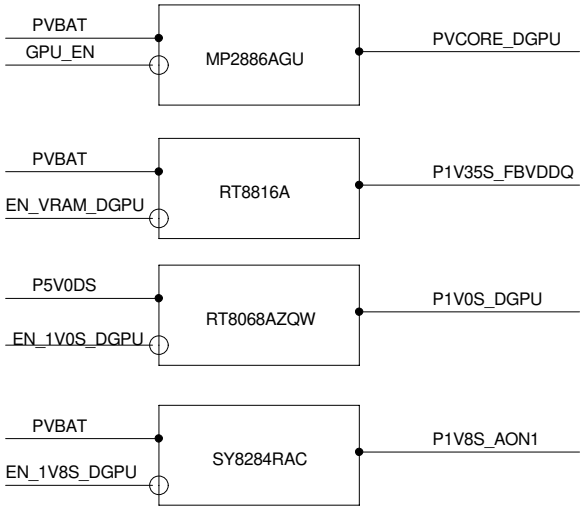
GPU POWER BLOCK

IN/EN OUT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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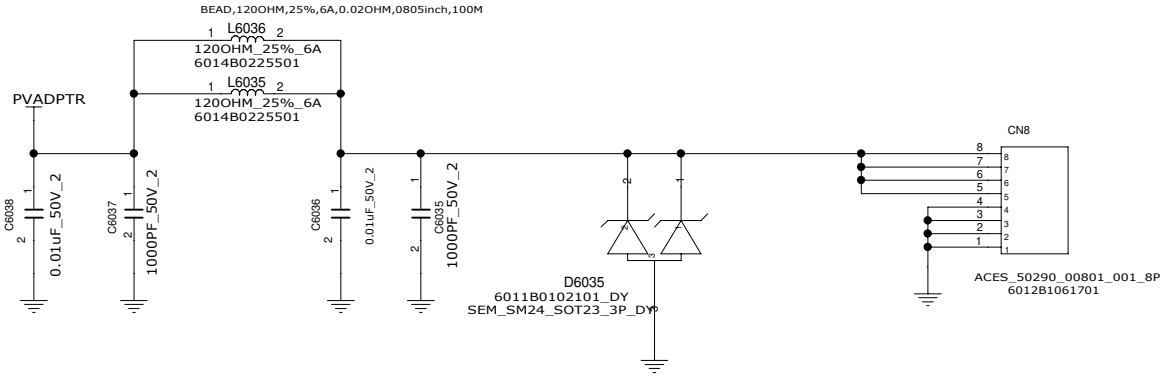

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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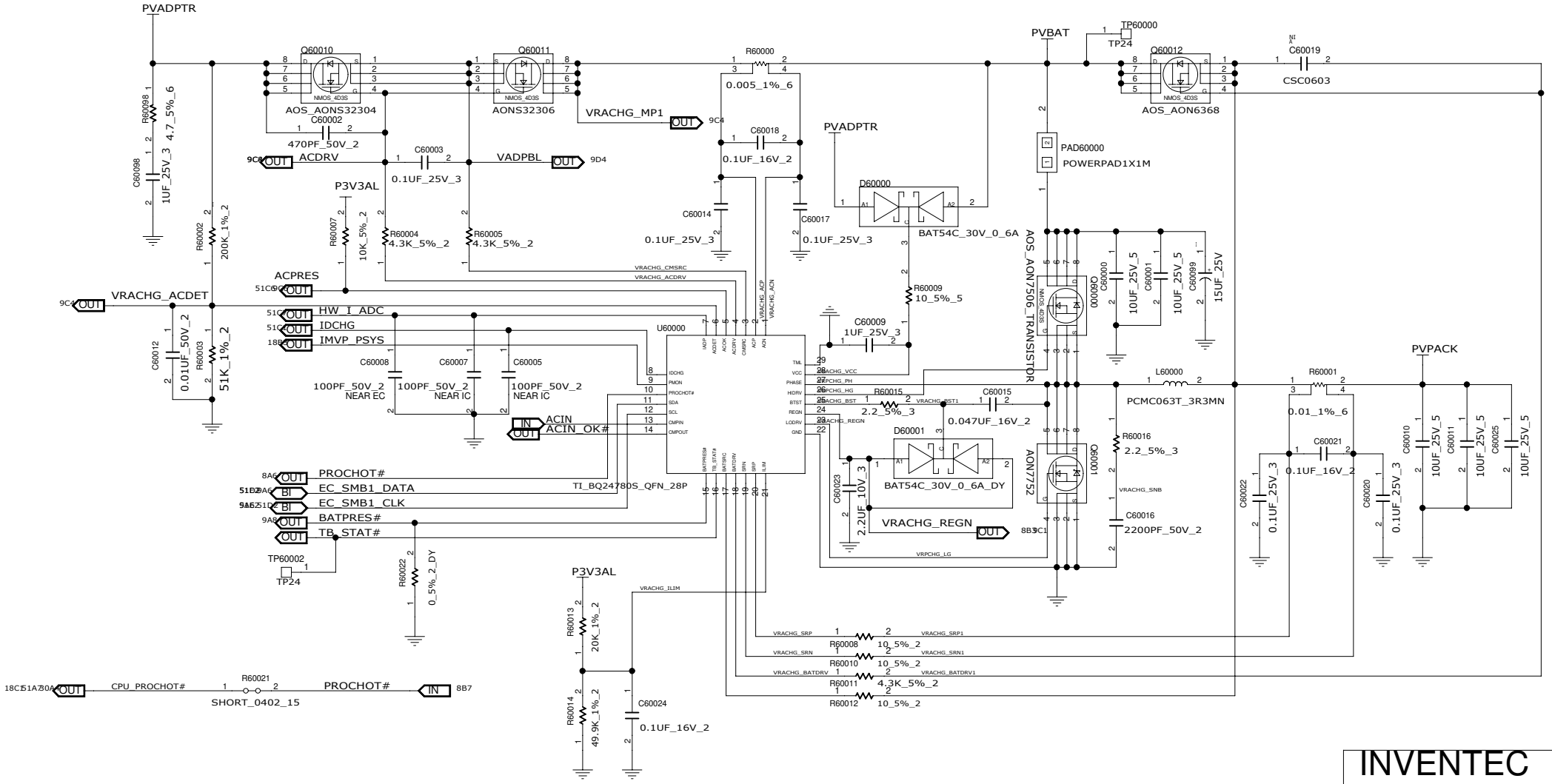

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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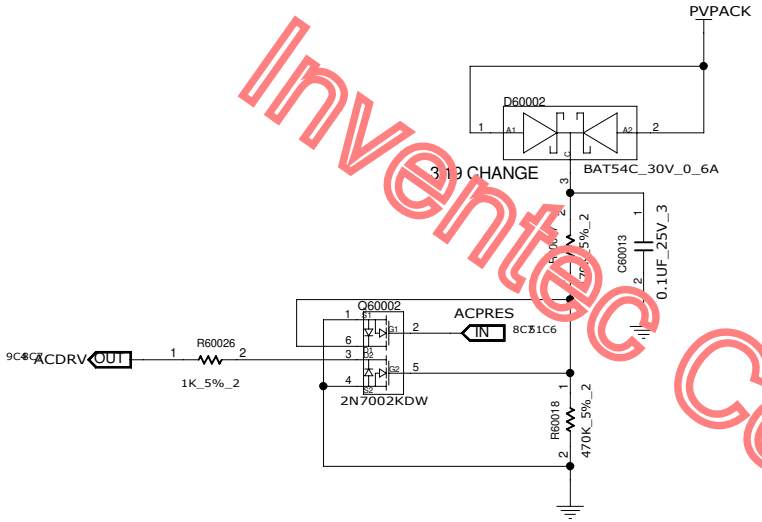
FOR CHARGER

SCP



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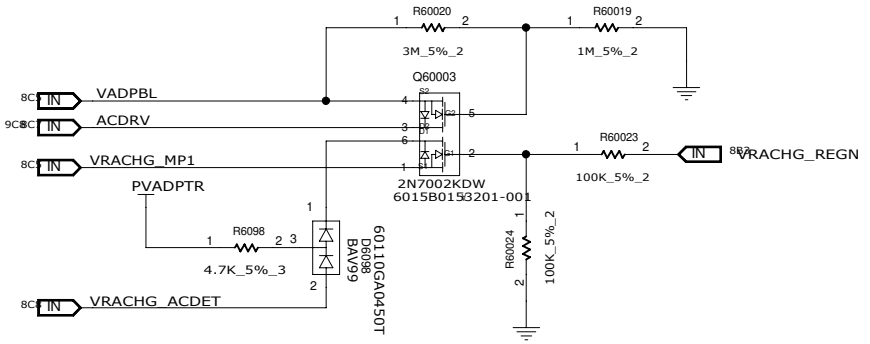

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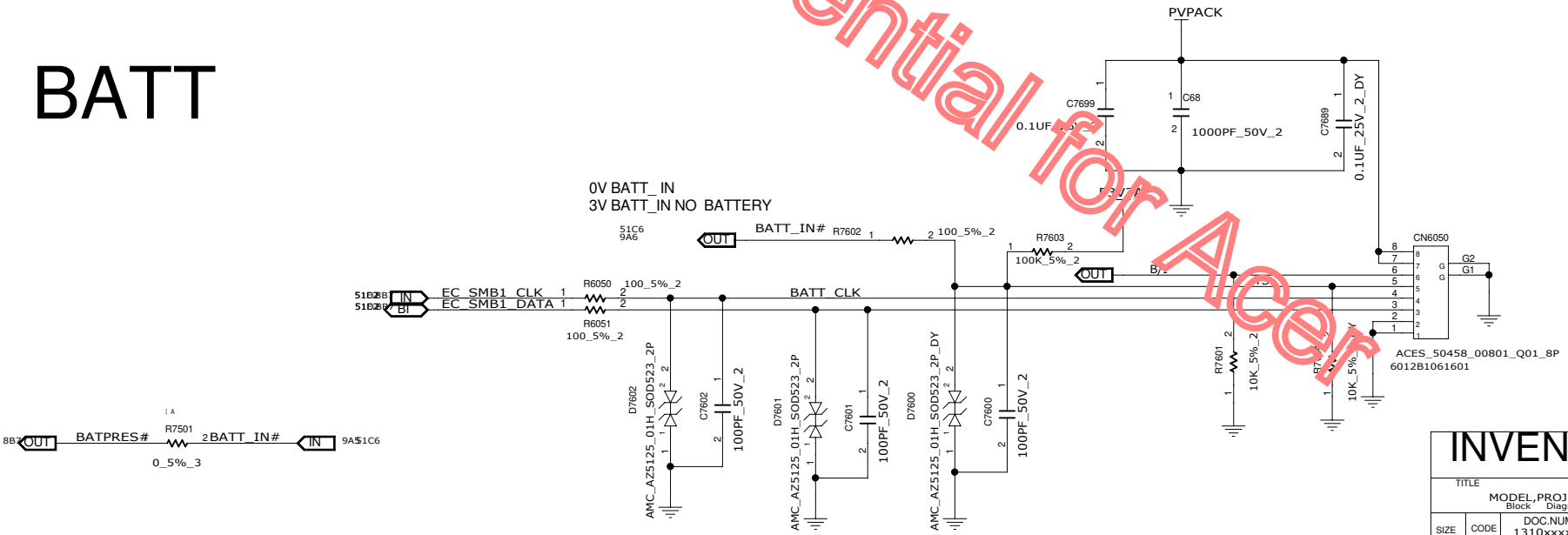

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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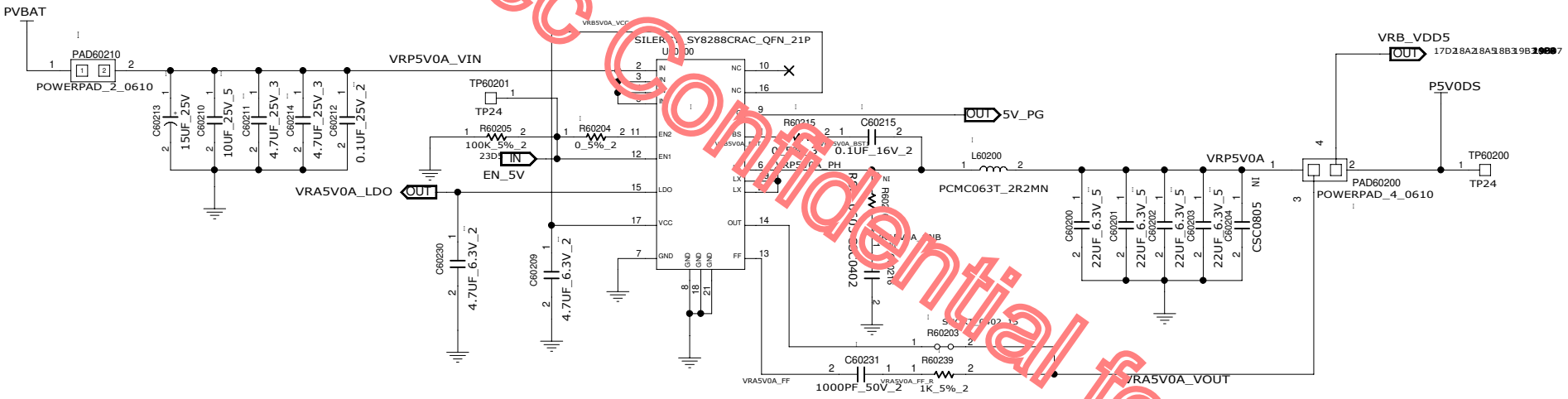
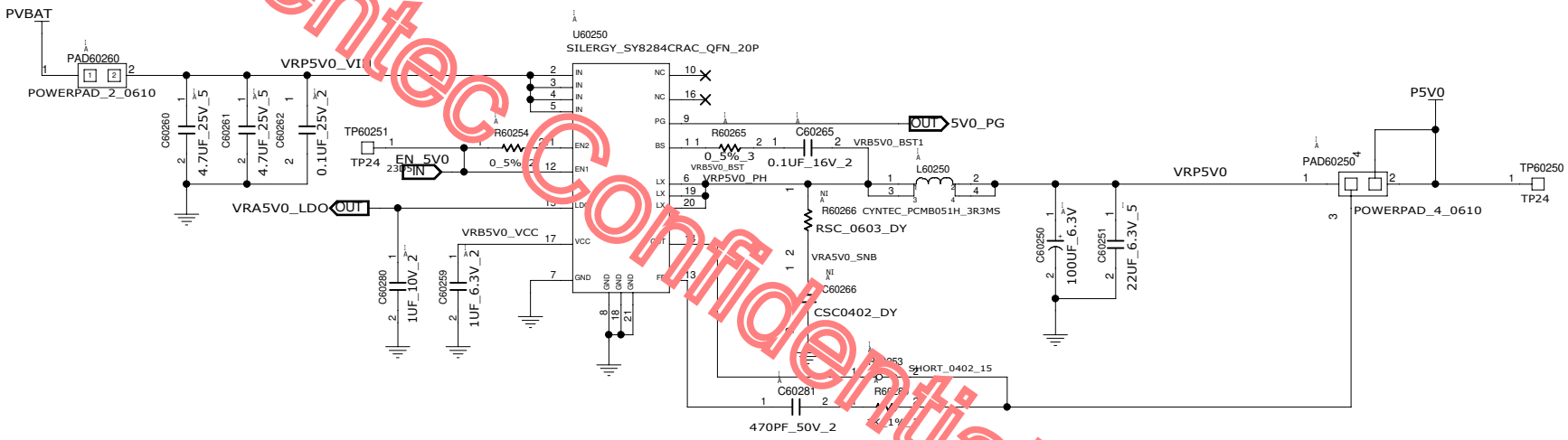


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P5V0DS
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	10 of 139

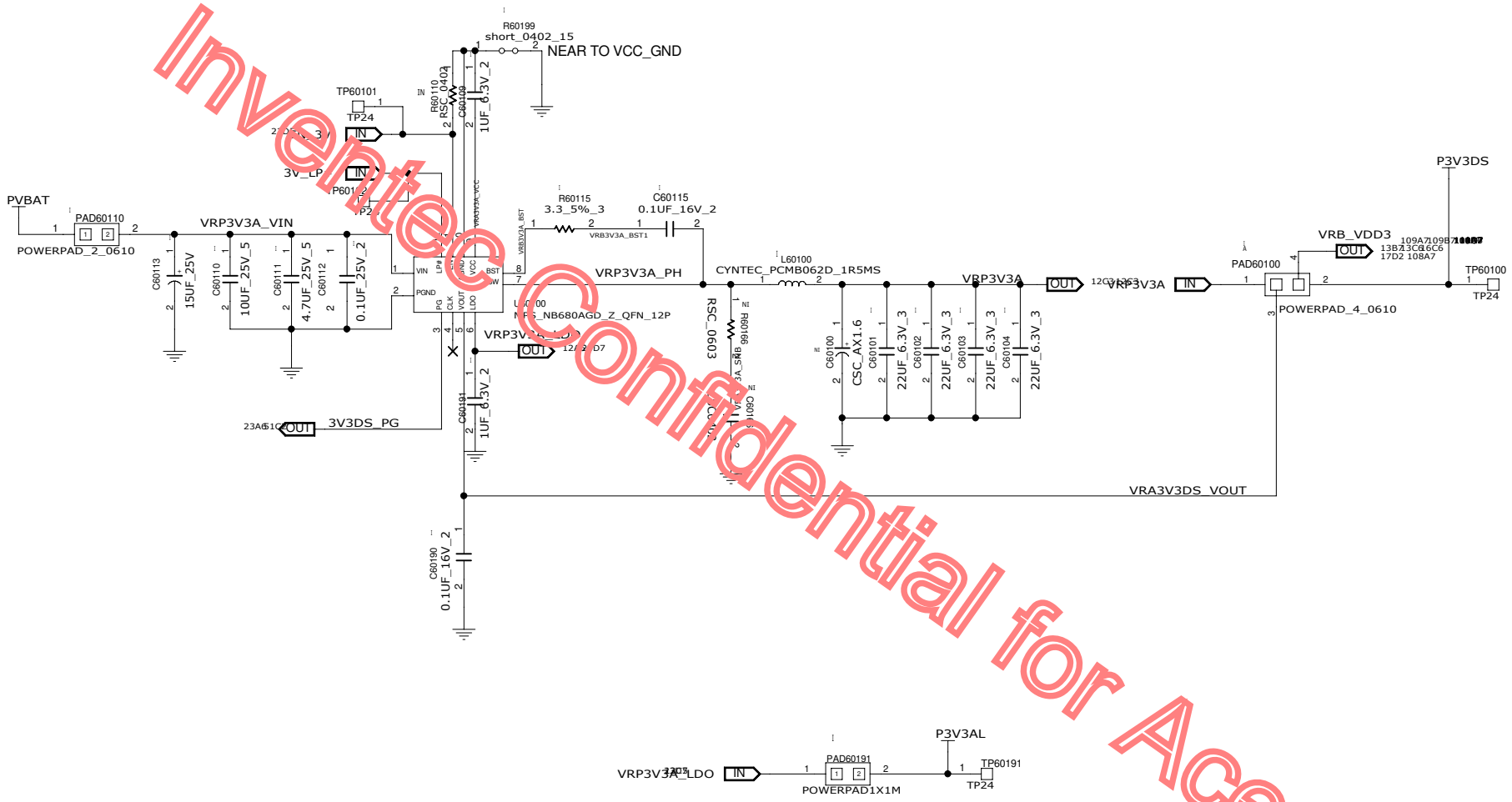
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	11 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



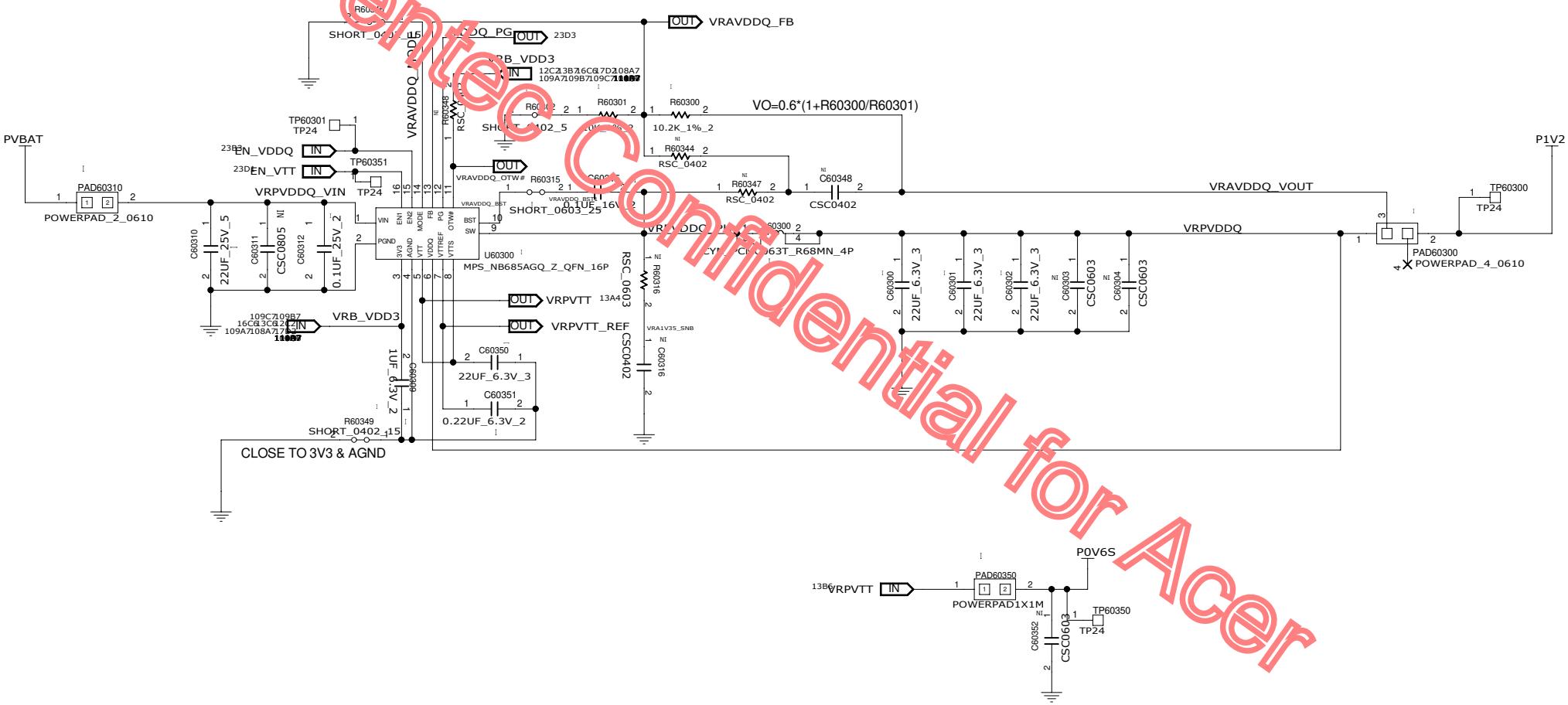
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P3V3DS_NB680A
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	12 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
VDDQ

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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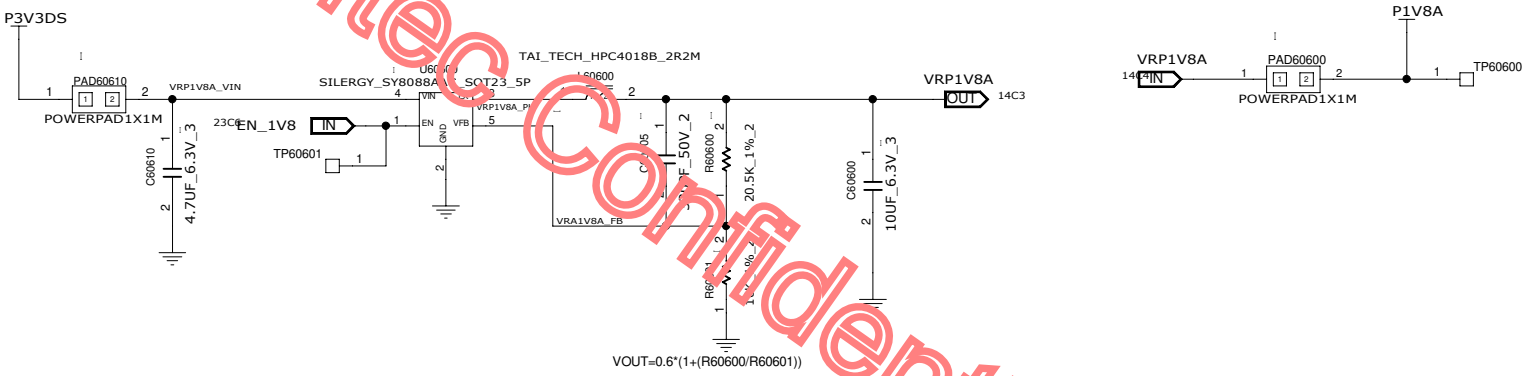

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P1V8DS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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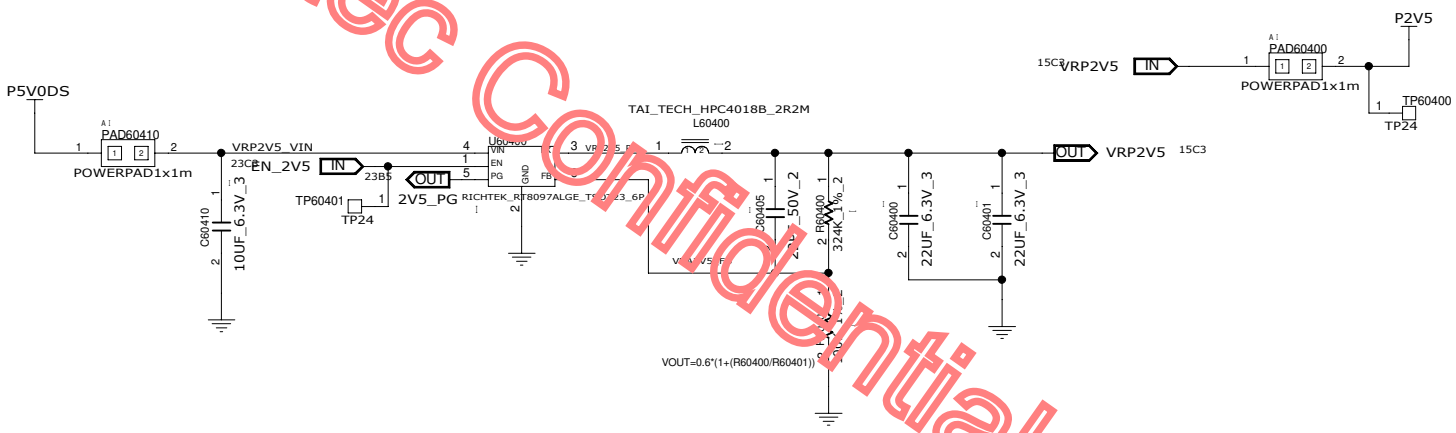
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P2V5

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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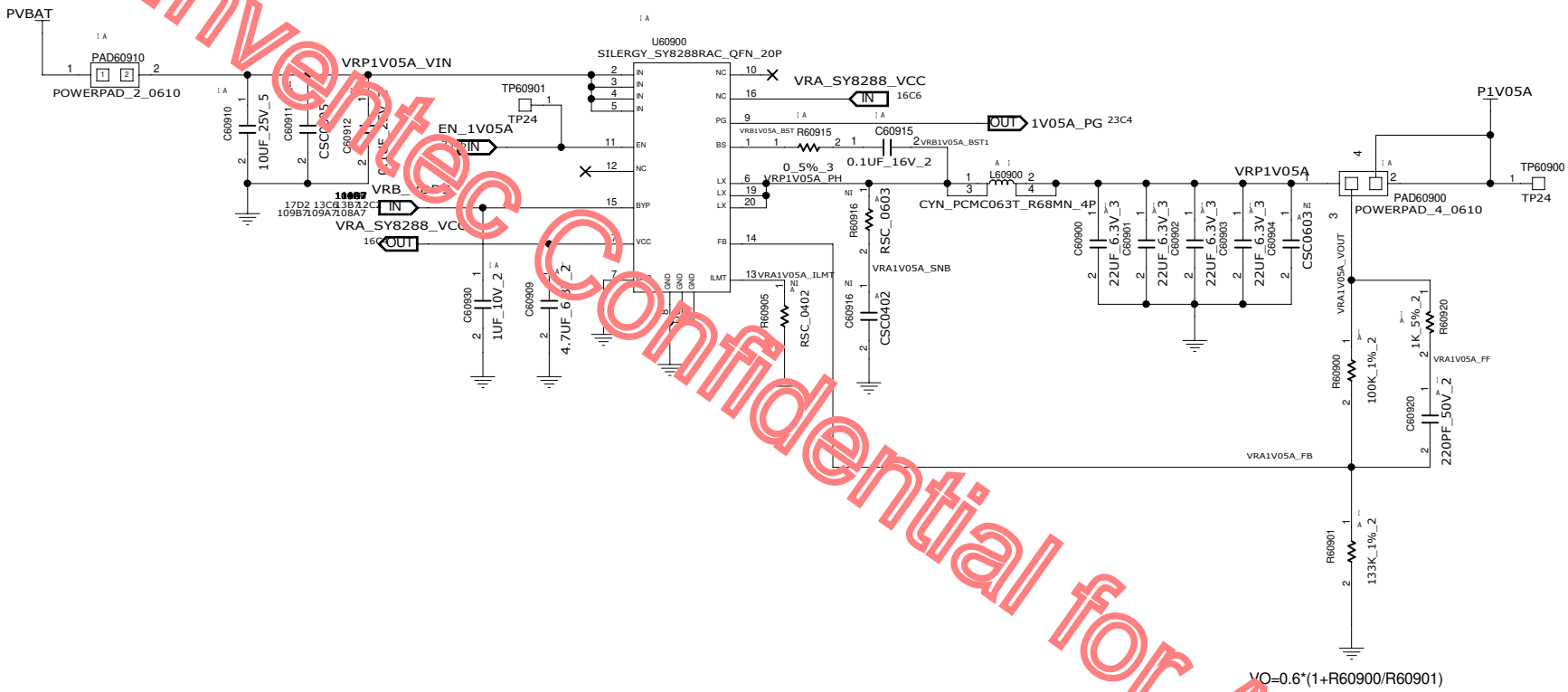

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V0A

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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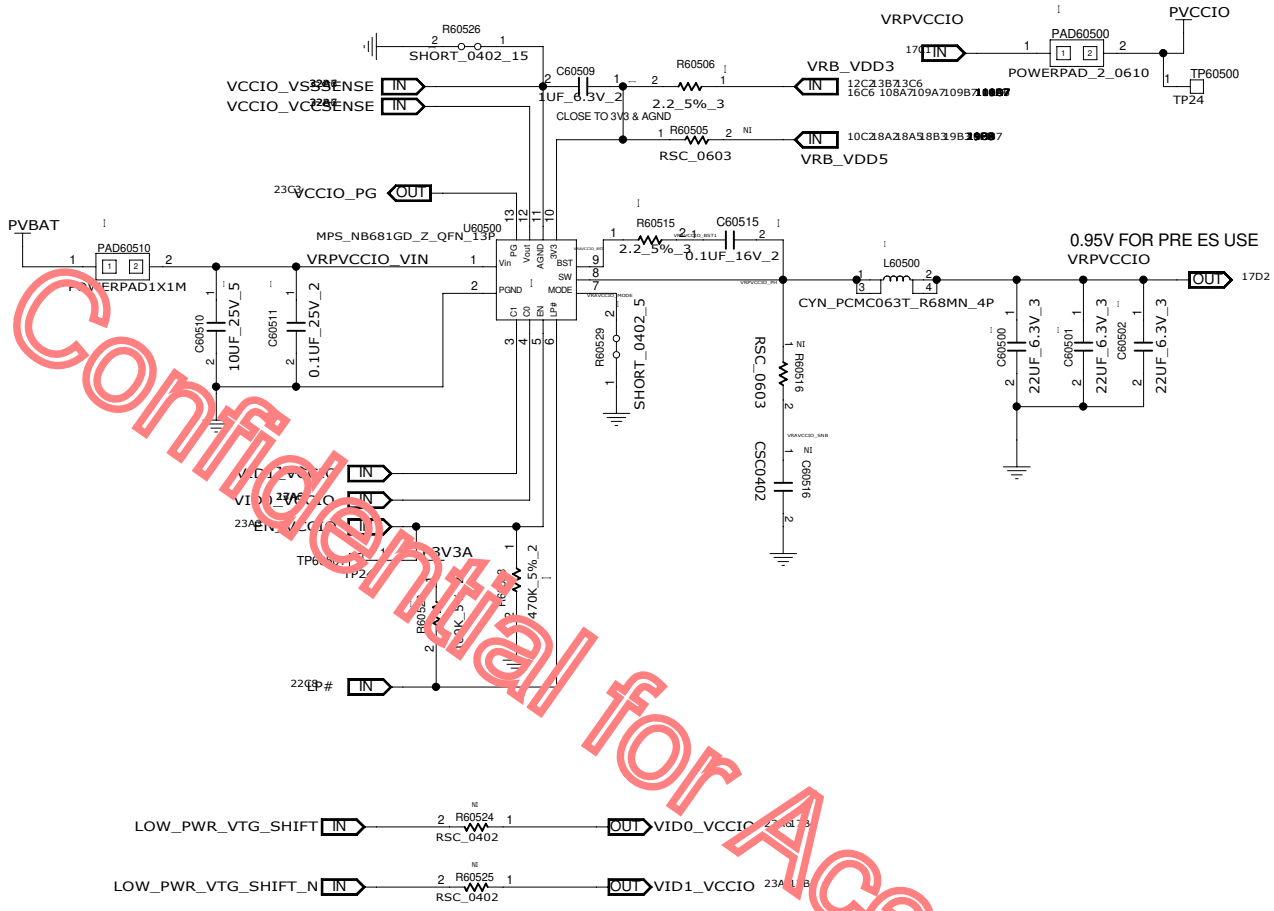
MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCIO

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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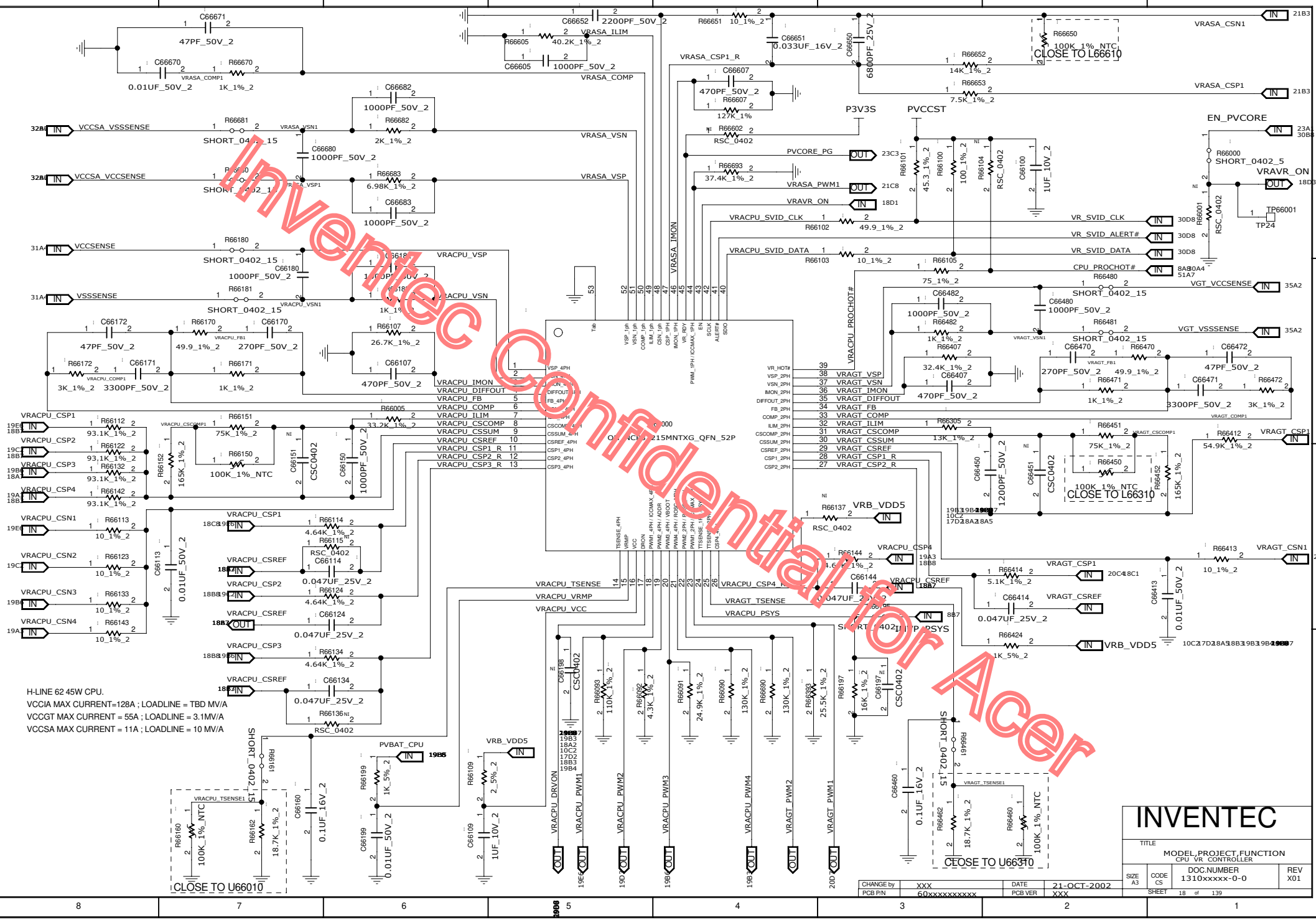

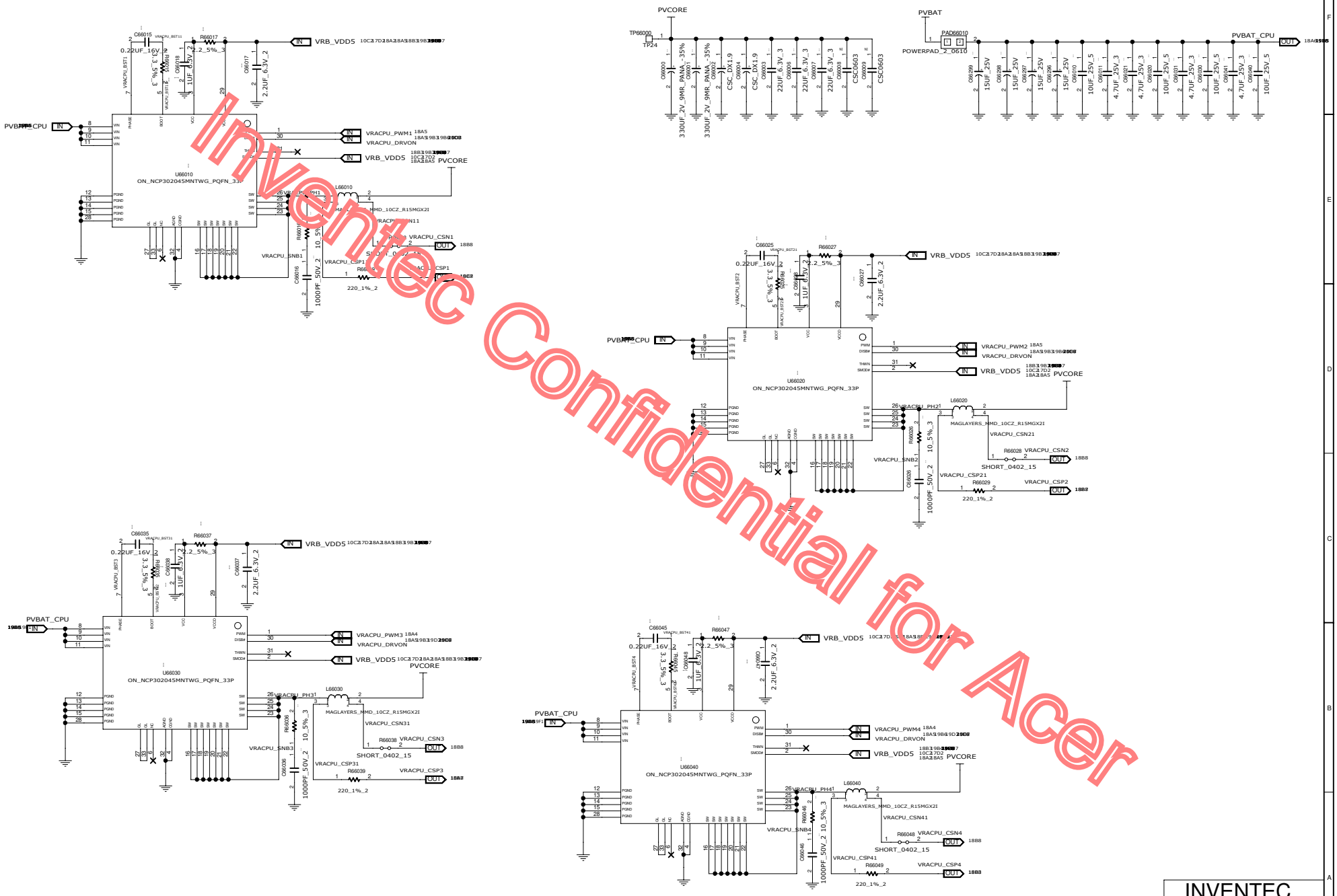

CHANGE By	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCORE

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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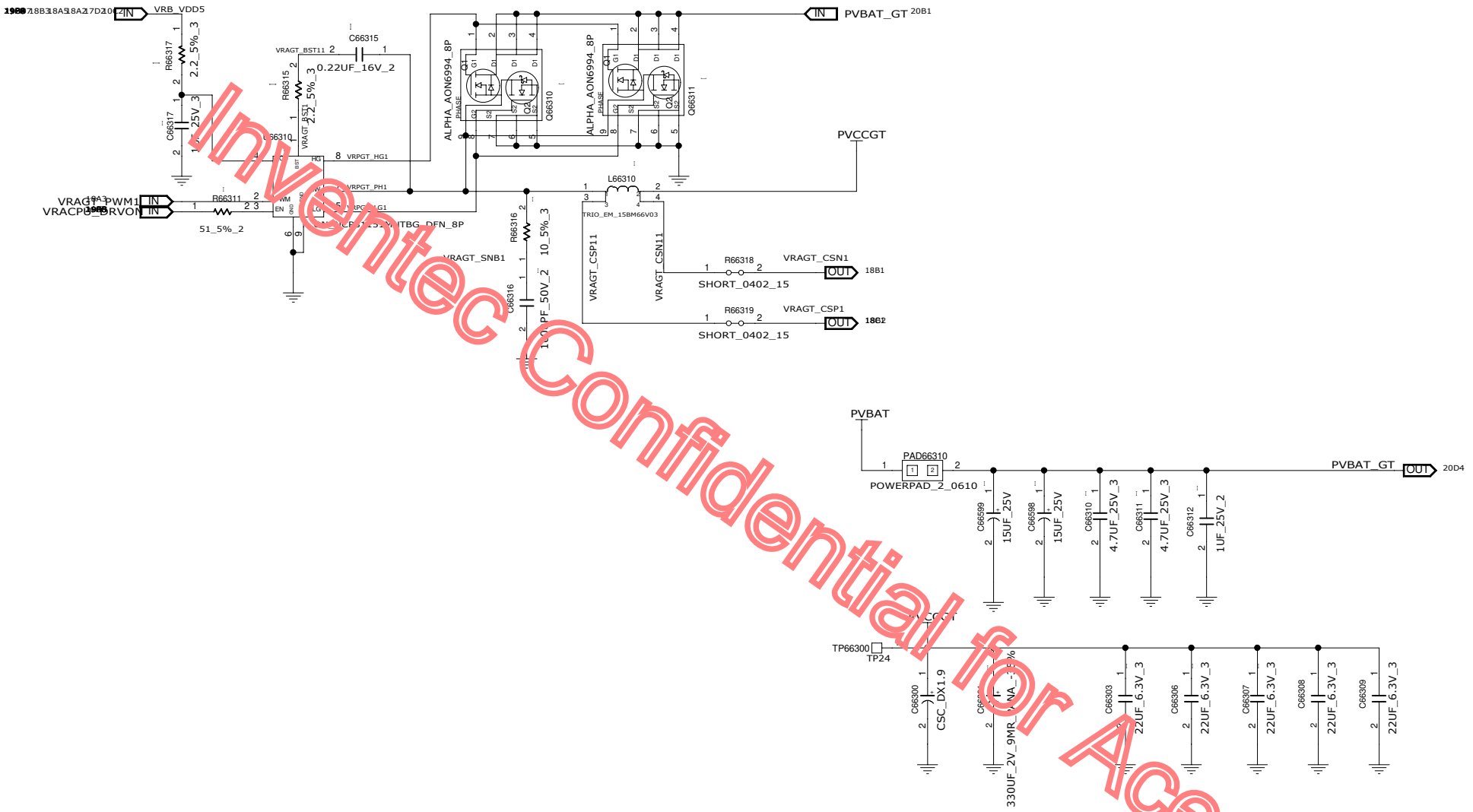

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PVCCGT		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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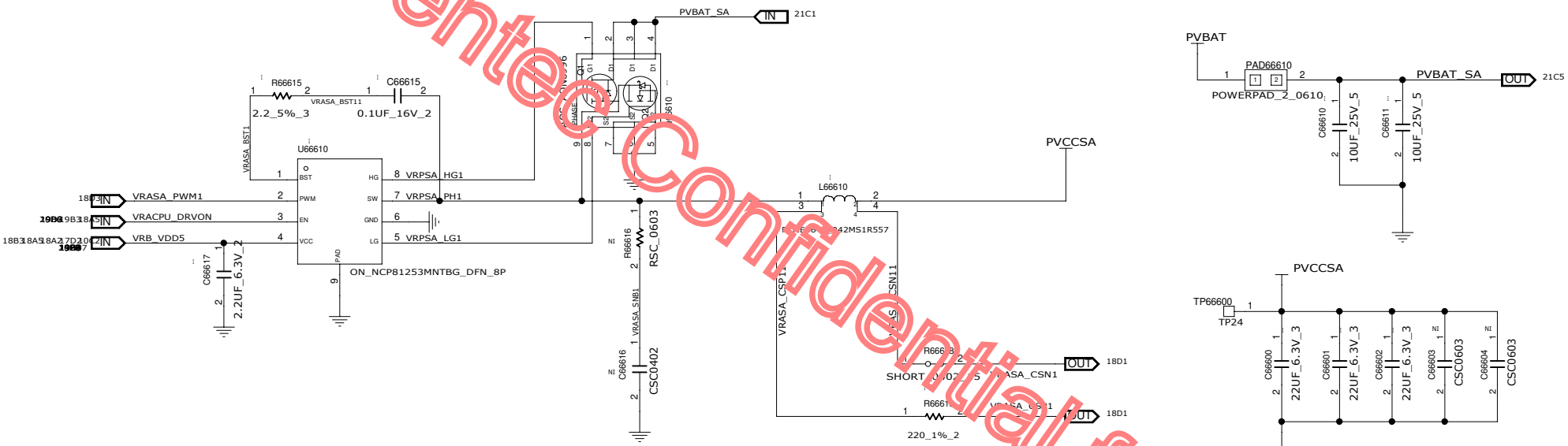
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCSA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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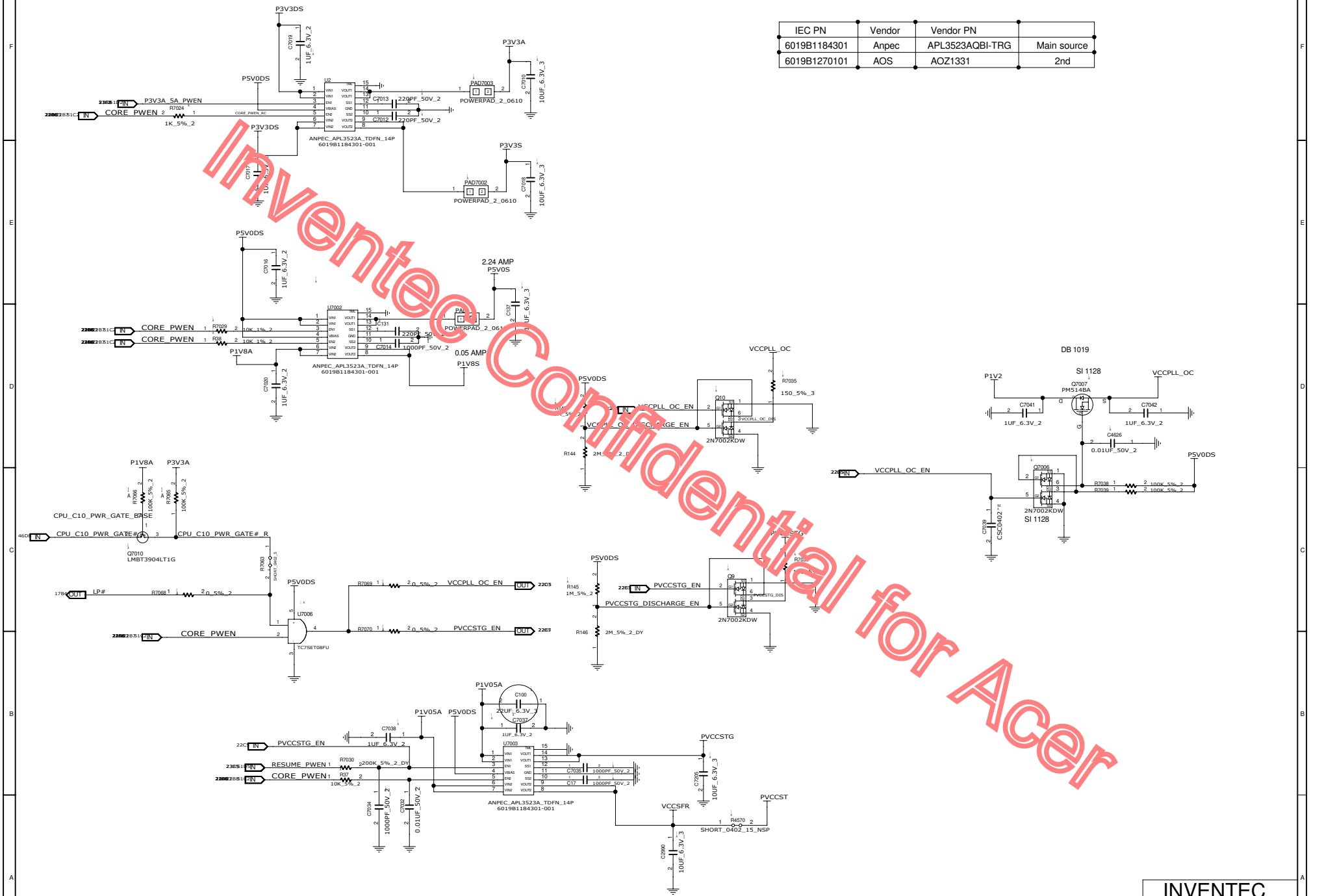

IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

INVENTEC

MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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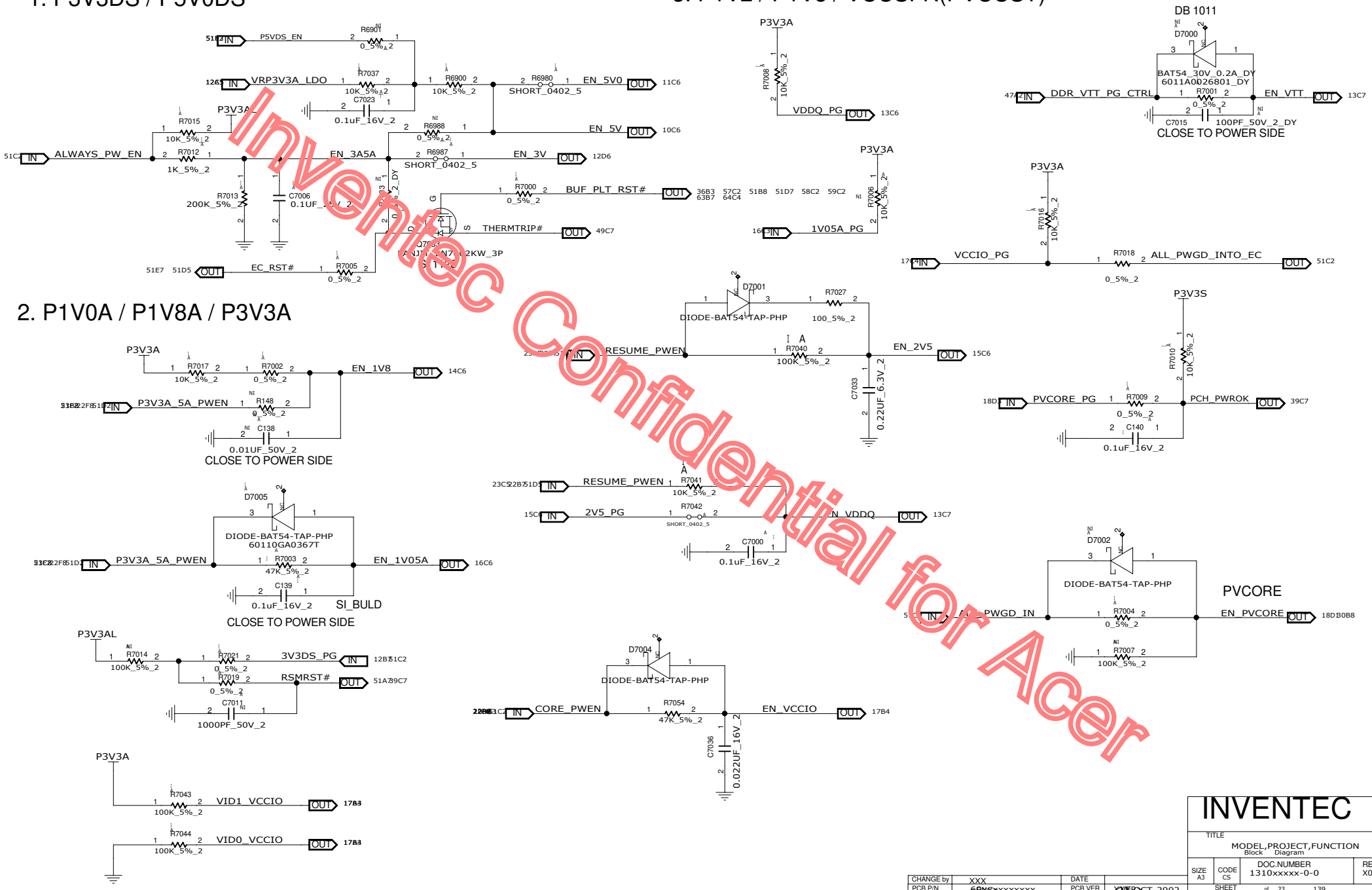
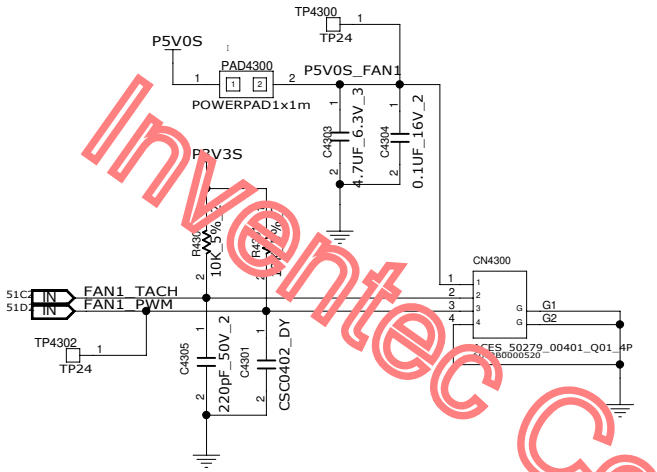
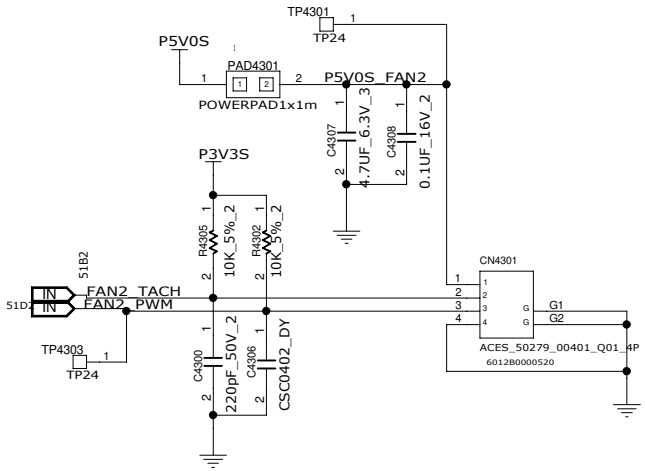


REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

TITLE: MODEL,PROJECT,FUNCTION
FAN & THERMAL

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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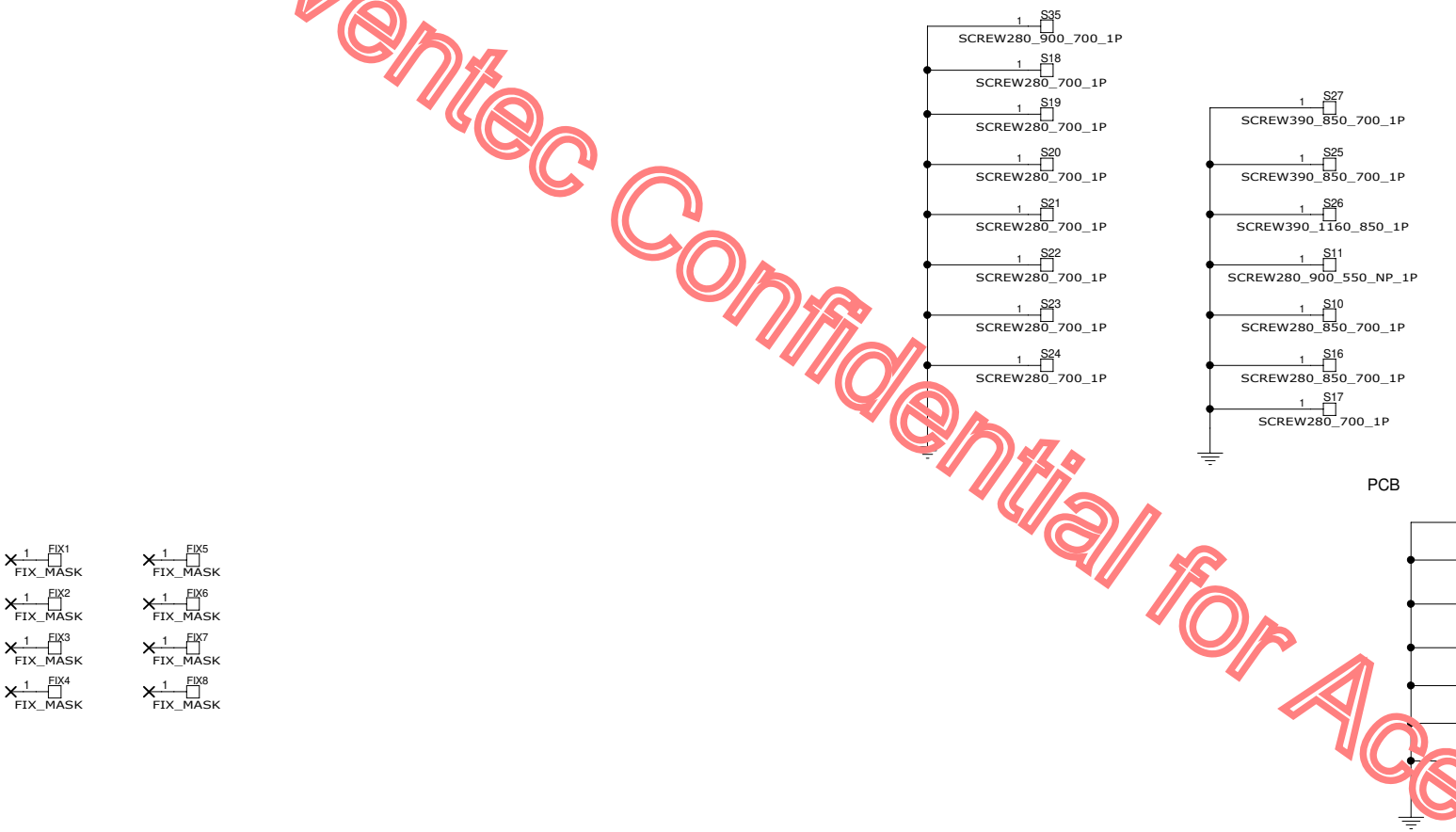
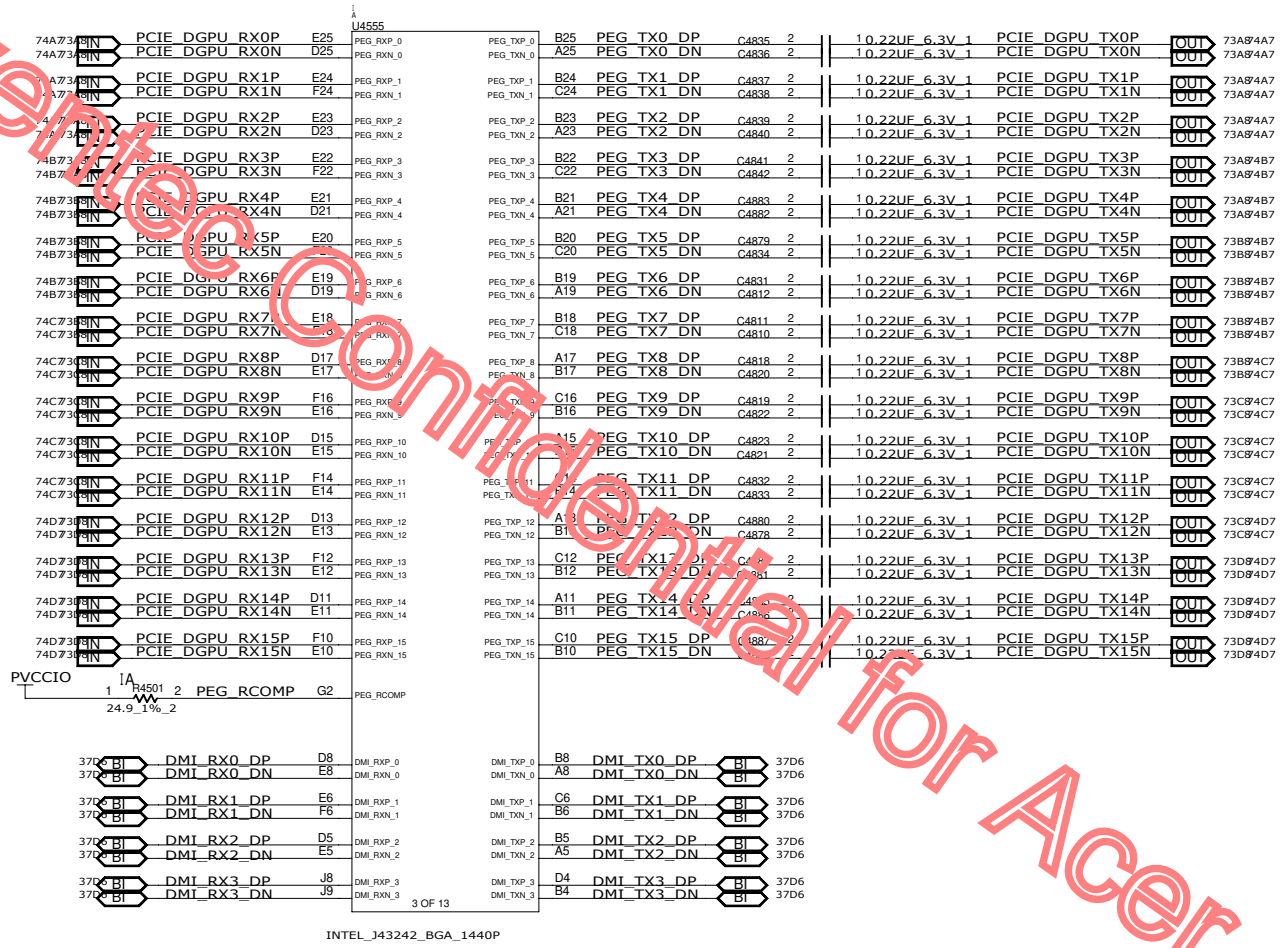
REFERENCE 0~49(PCB SCREW)



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION XDP & ME CONN.		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 25 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE1_H-PEG,HDMI

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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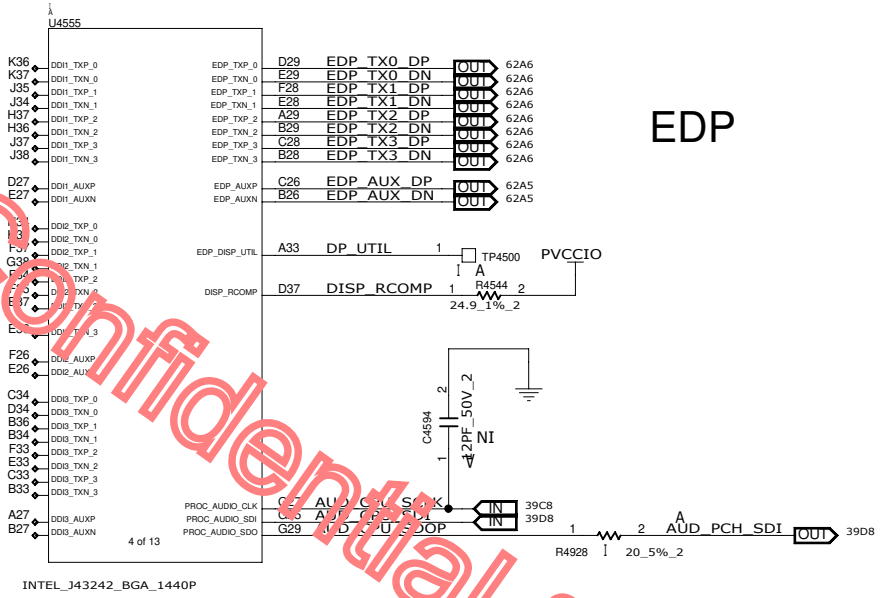
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EDP



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE2_H-DDI,EDP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INTEL_J43242_BGA_1440P

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE_H-DDR-1

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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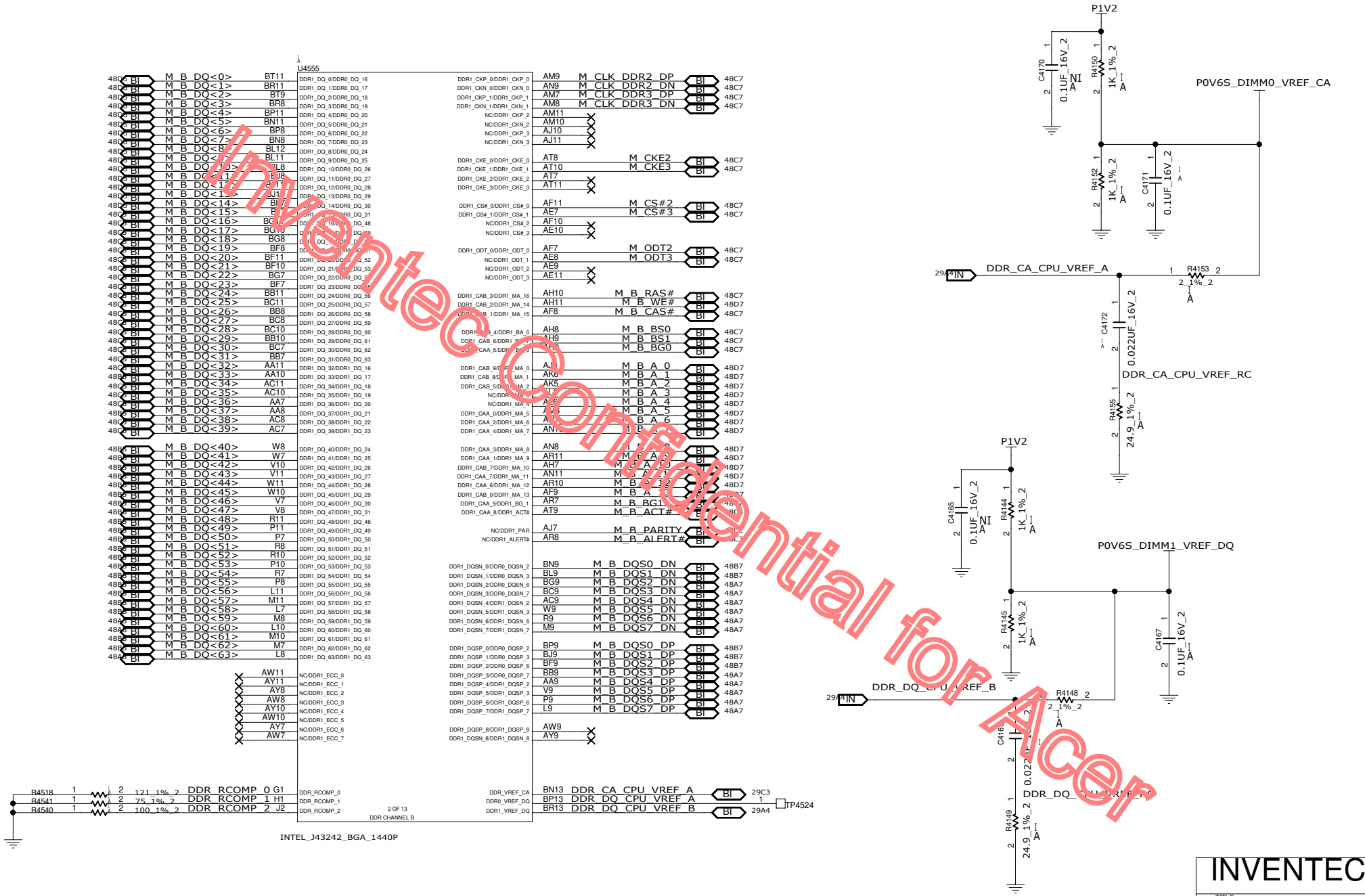

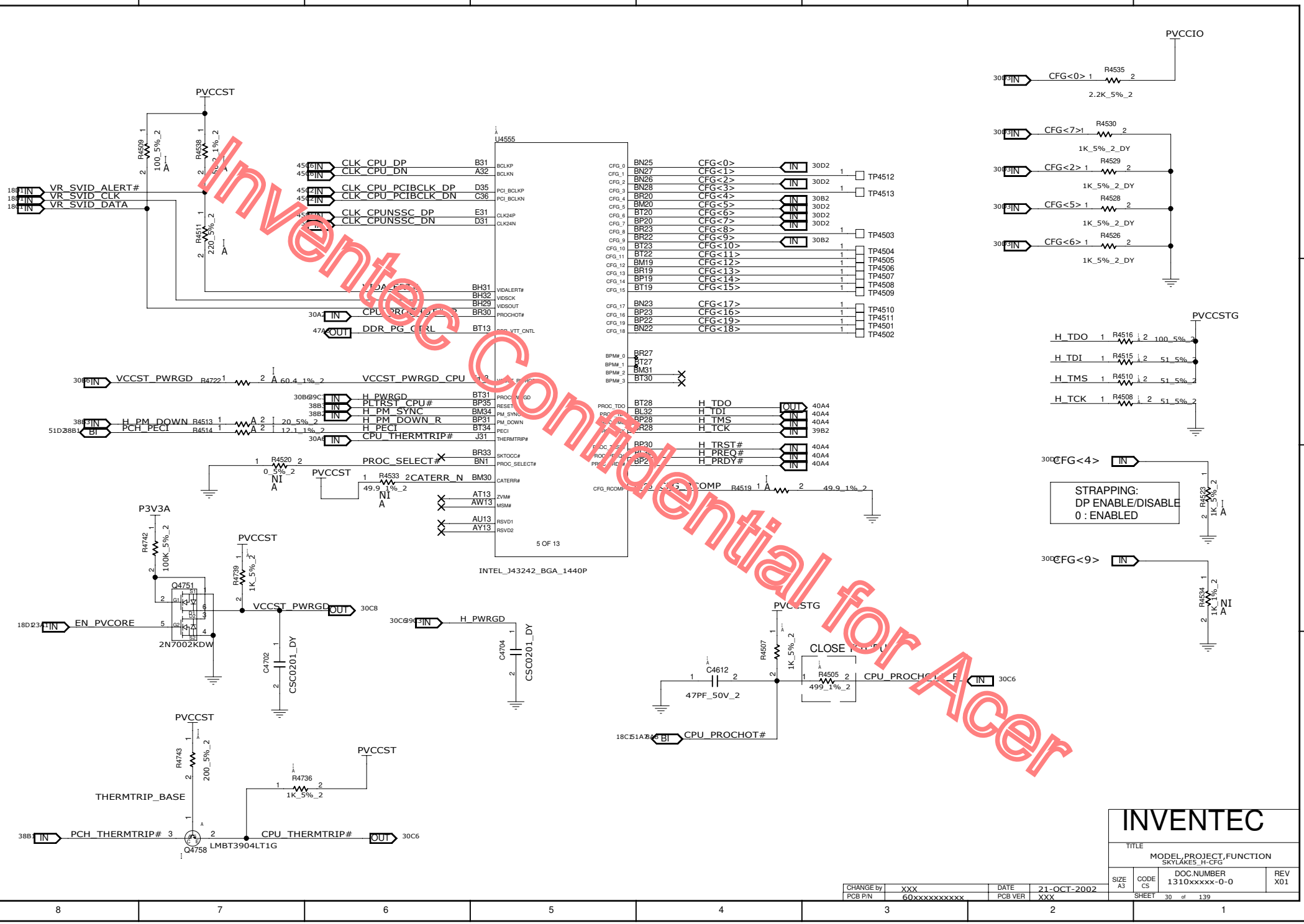

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKES_H-CFG

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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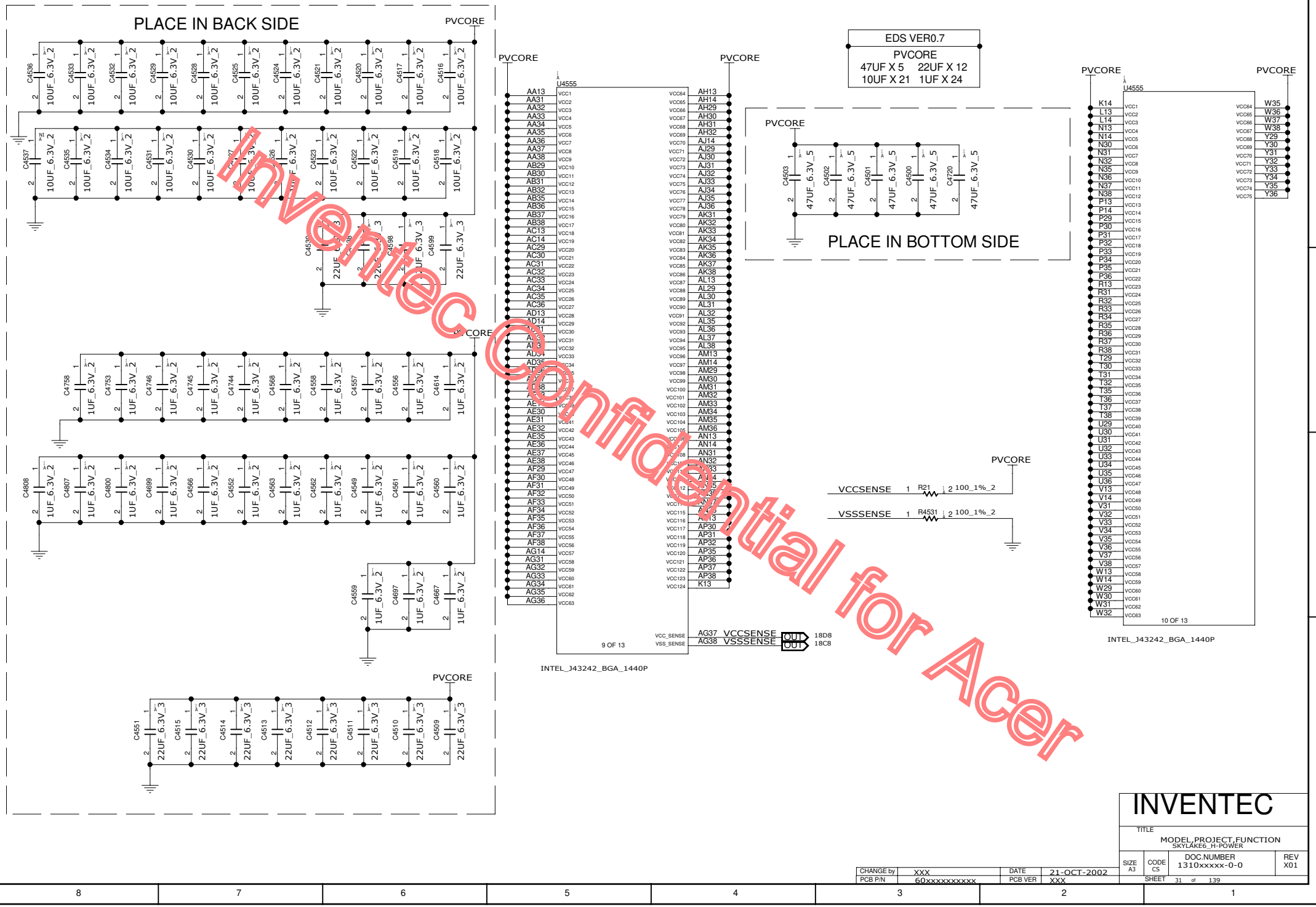
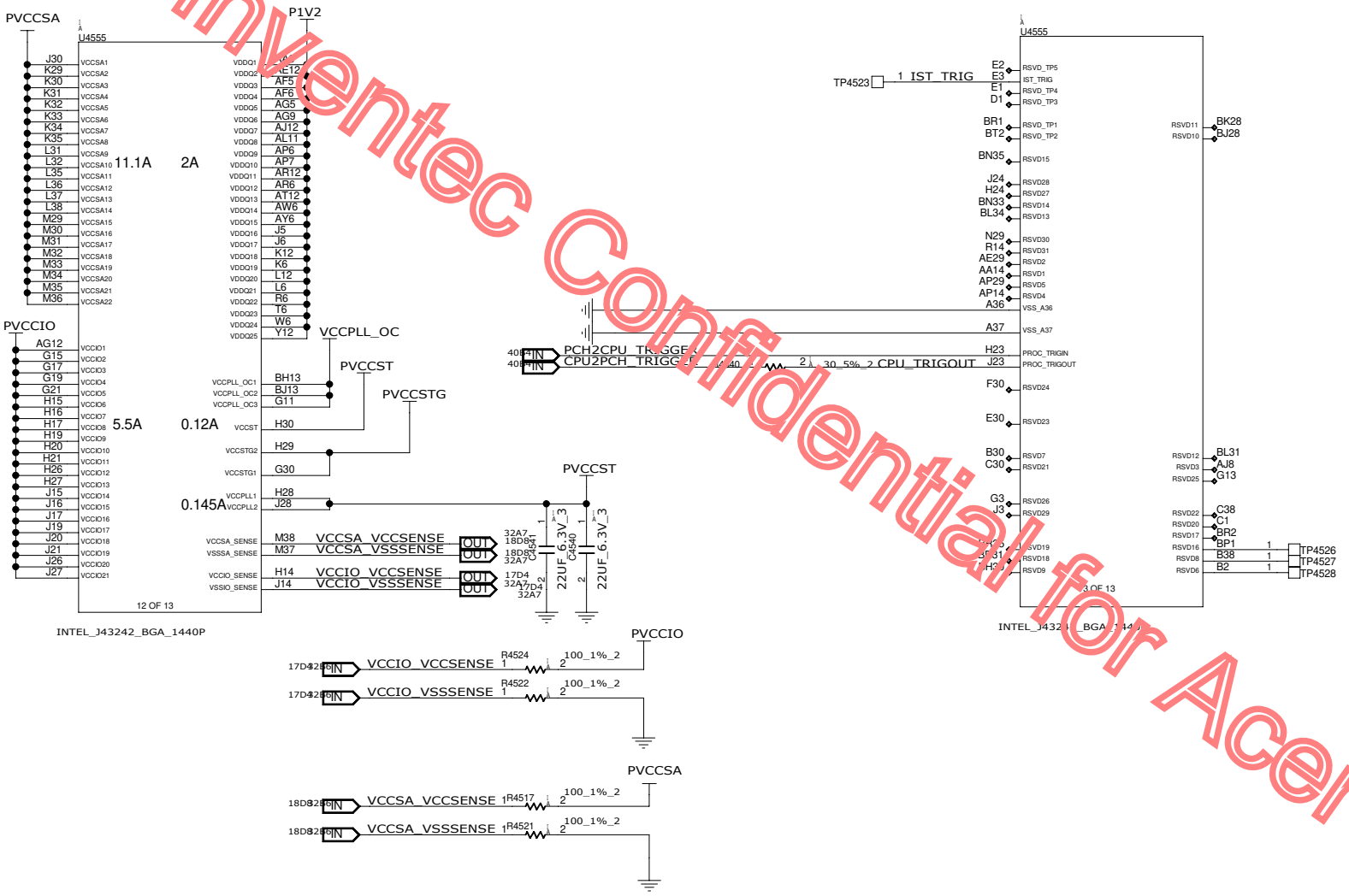
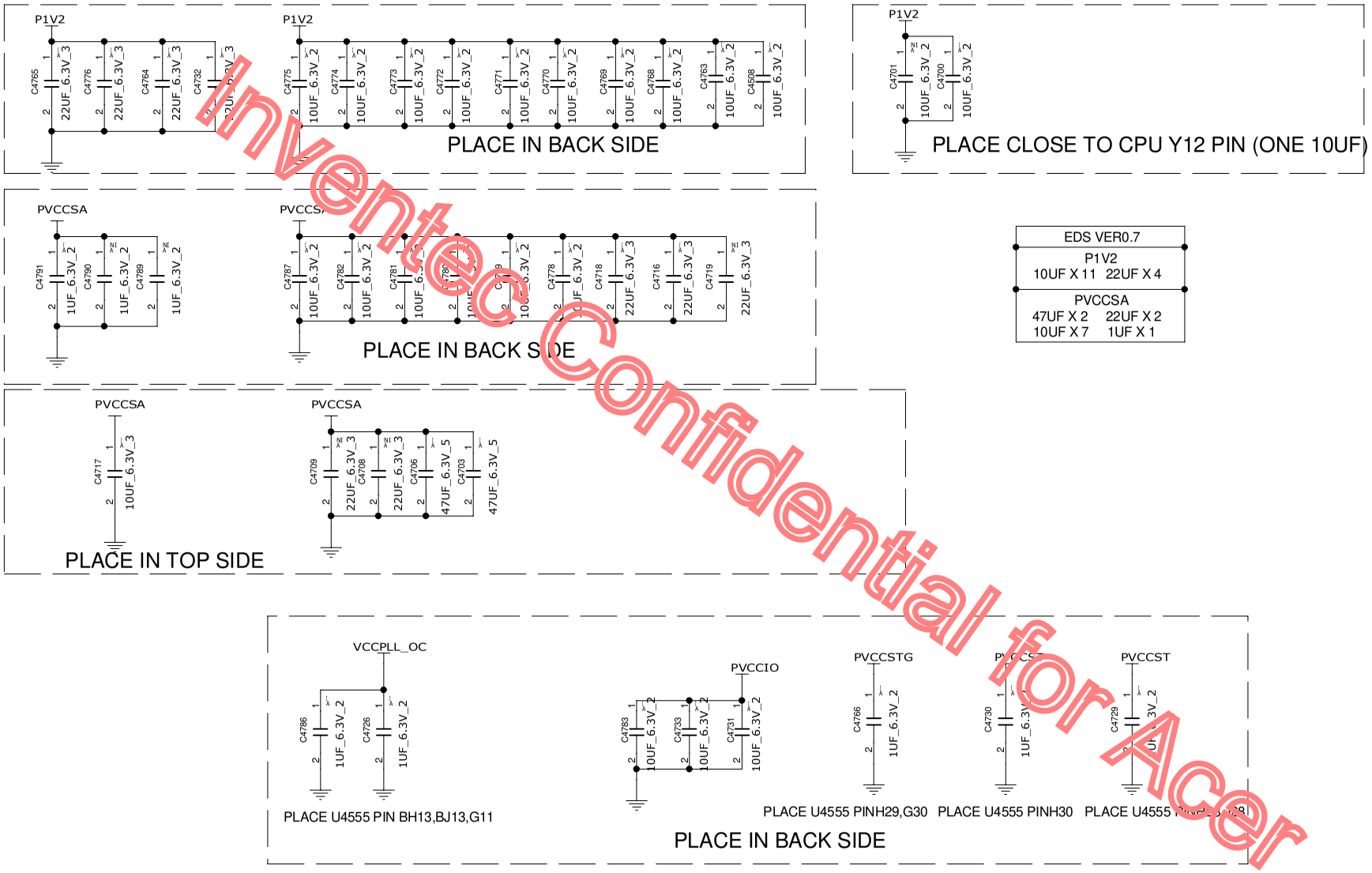

PLACE IN BACK SIDE
PVCORE
10UF_6.3V_2
22UF_6.3V_3
1UF_6.3V_2
EDS VER0.7
PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24
PLACE IN BOTTOM SIDE
47UF_6.3V_5
U4555
9 OF 13
10 OF 13
INTEL_J43242_BGA_1440P
VCCSENSE
VSSSENSE
R21
R4531
100_1%_2
AG37 VCCSENSE OUT 18D8
AG38 VSSSENSE OUT 18C8
Inventec Confidential for Acer
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE6_H-POWER
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 31 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE7_H-POWER				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0			REV X01
SHEET 32 of 139					
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

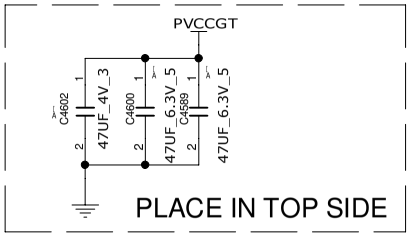
TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE8_H-DECOUPLING

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

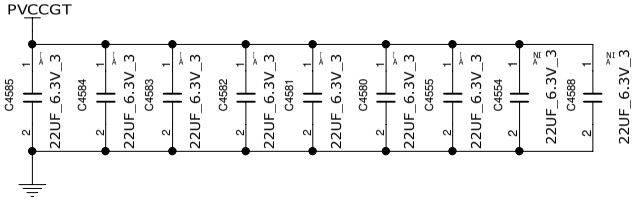
SHEET 33 of 139

EDS VER0.7

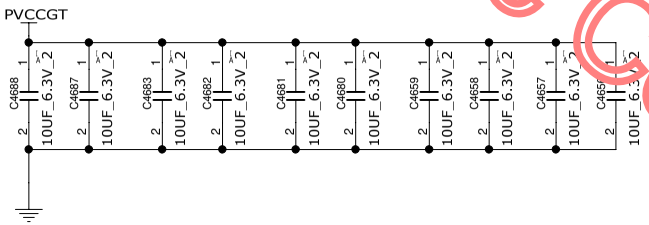
PVCCGT
47UF X 3 22UF X 7
10UF X 10 1UF X 12

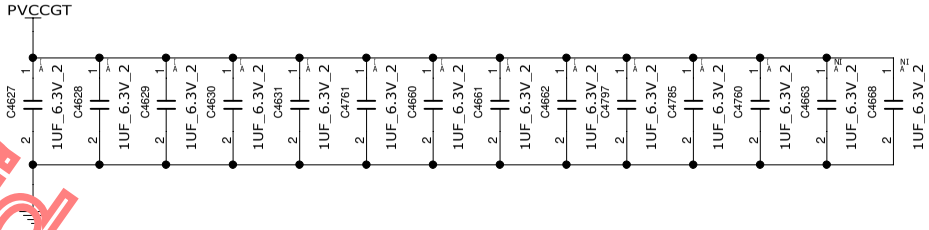


PLACE IN TOP SIDE

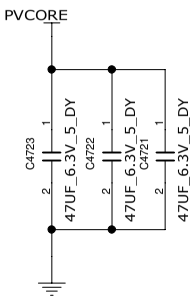


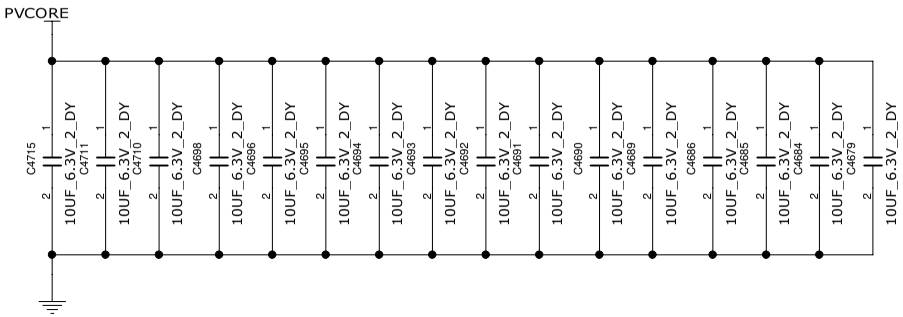
PLACE IN BACK SIDE

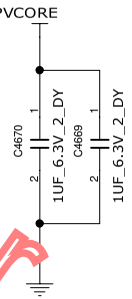




H82 CPU







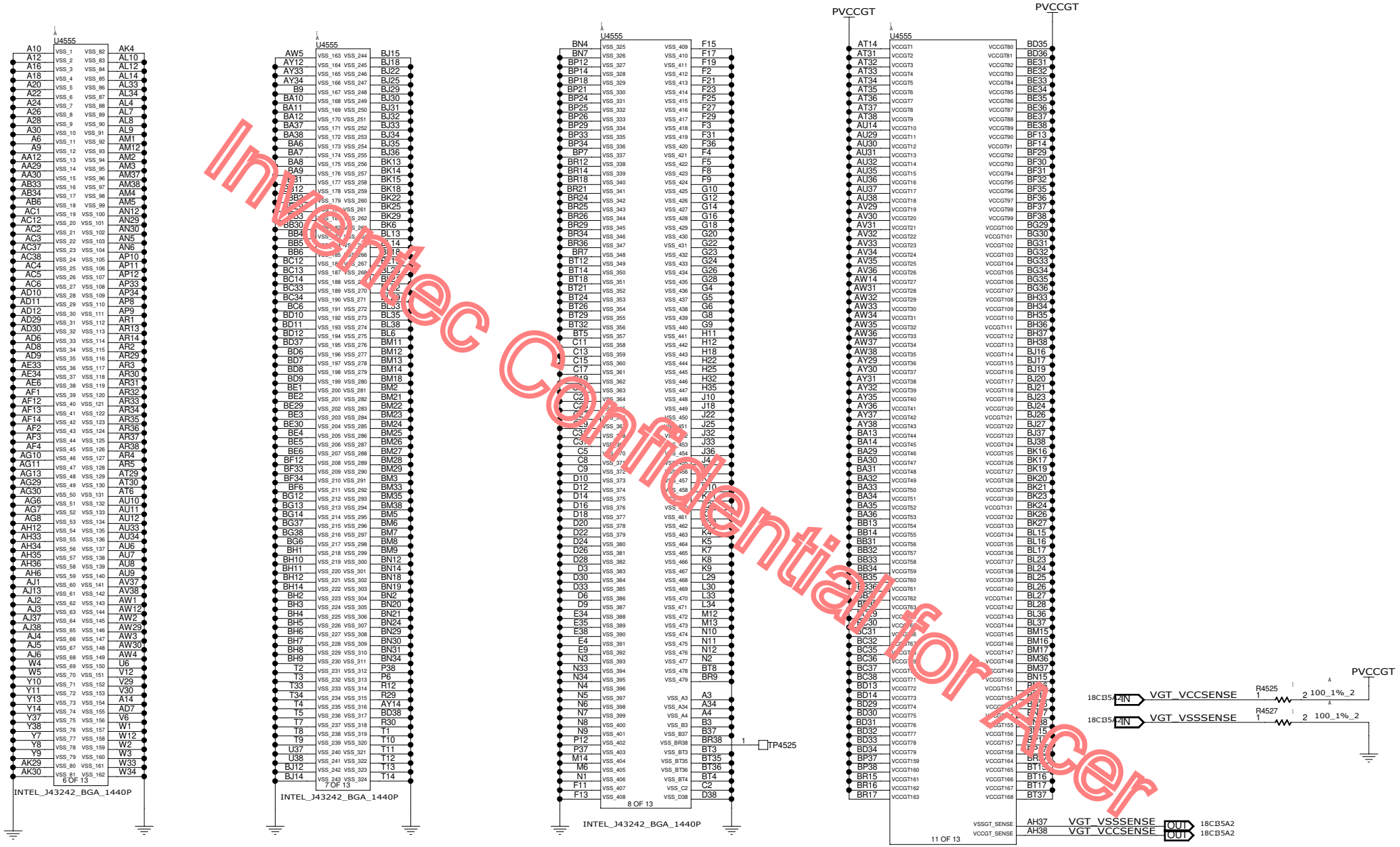
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE9_H-GT DECOUPLING

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

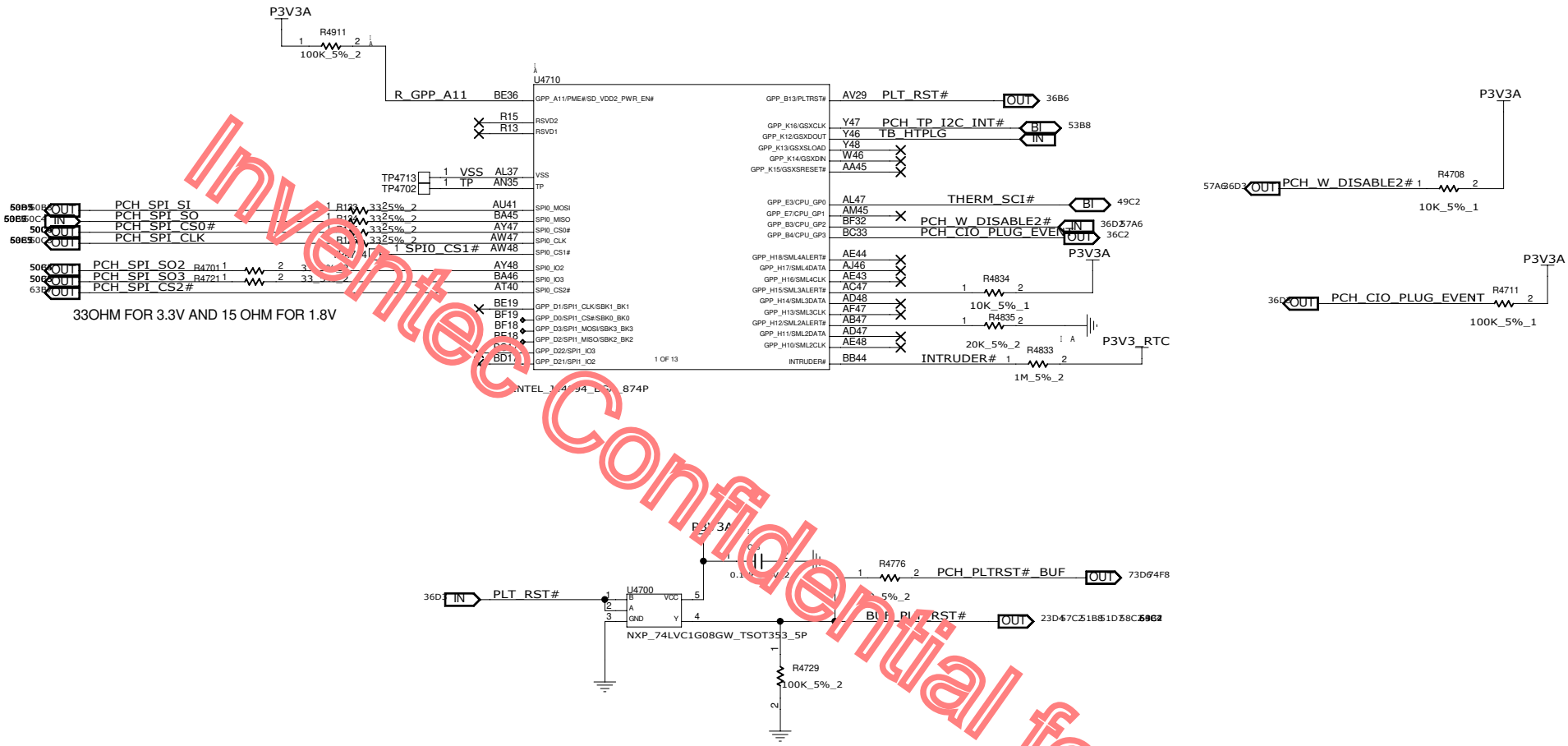
SHEET 34 of 139



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SKYLAKE10_H-GND		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 35 of 139			

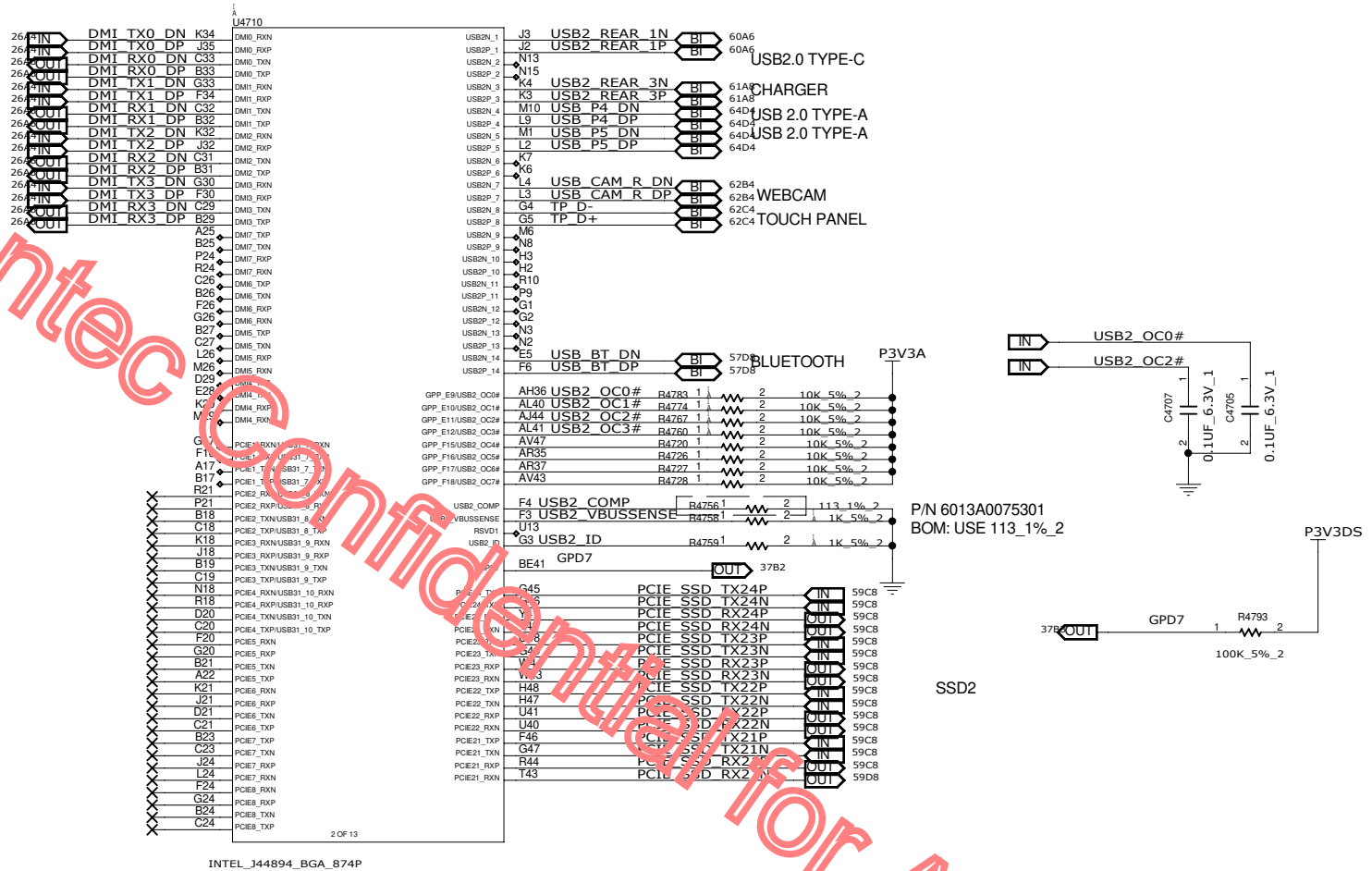
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PCH-SPI,GPP
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	36 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



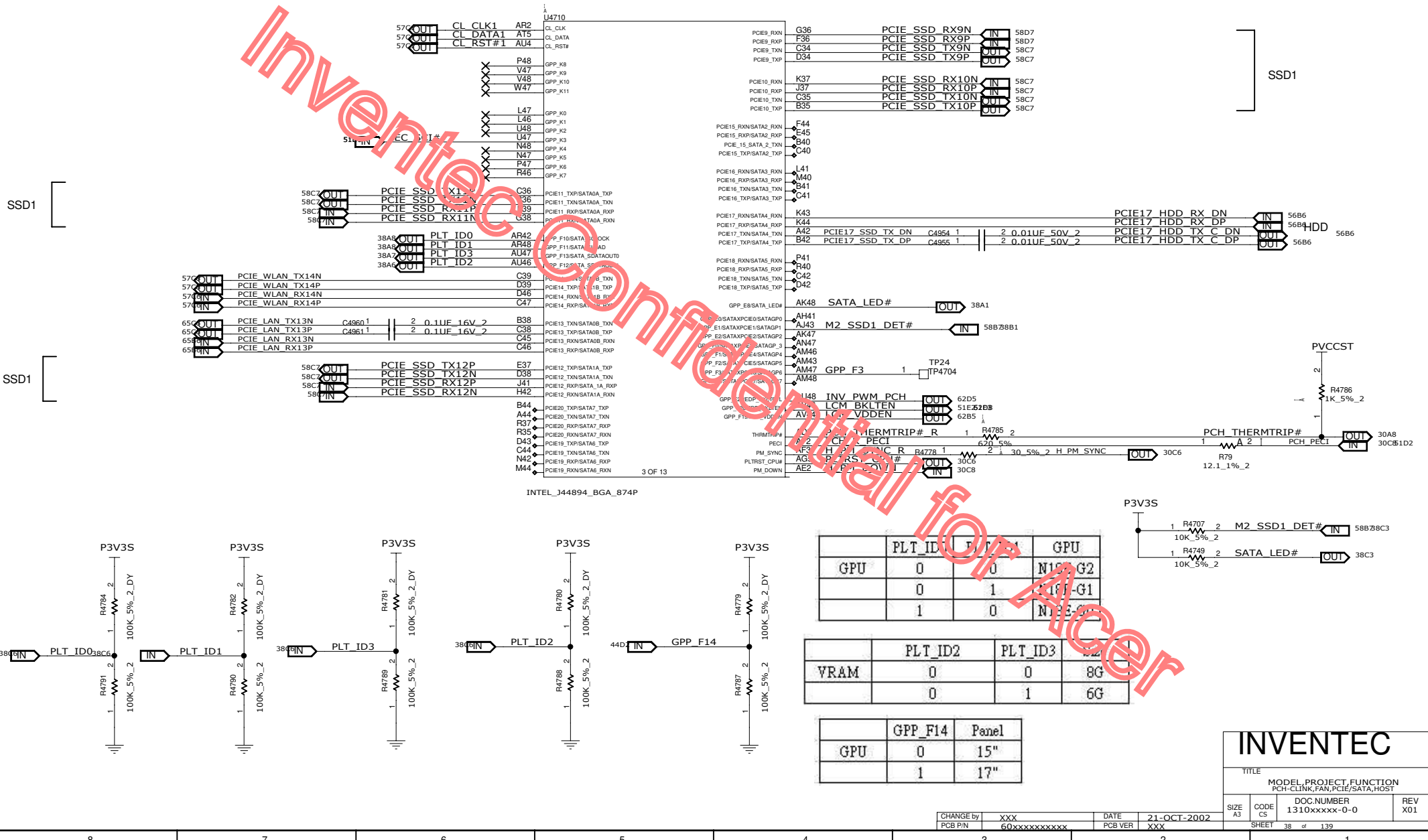
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-DMI,USB2,USB3

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 37 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



	PLT_ID0	PLT_ID1	GPU
GPU	0	0	N16P-G2
	0	1	N16P-G1
	1	0	N16E-G

	PLT_ID2	PLT_ID3	
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

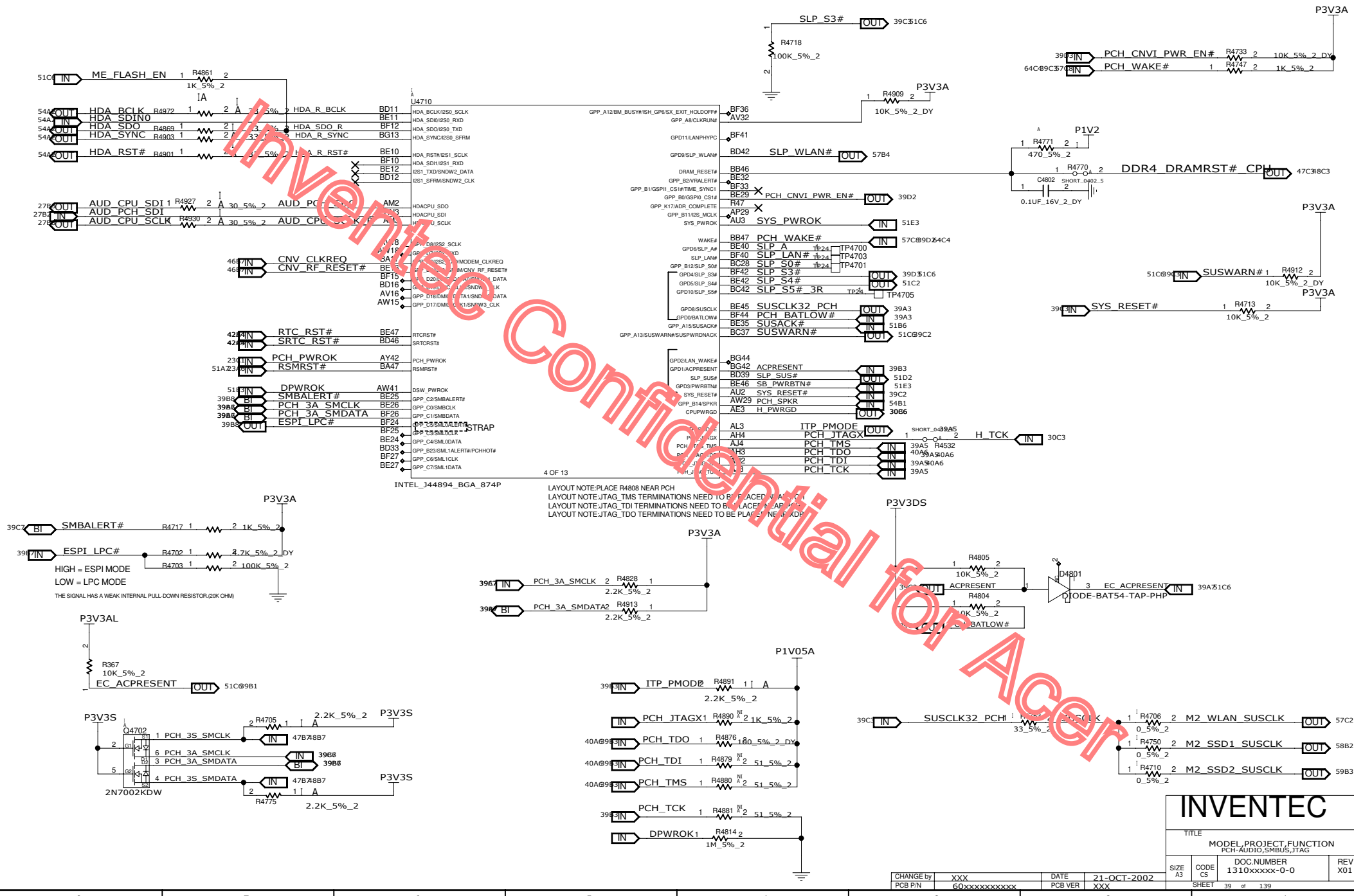
INVENTEC

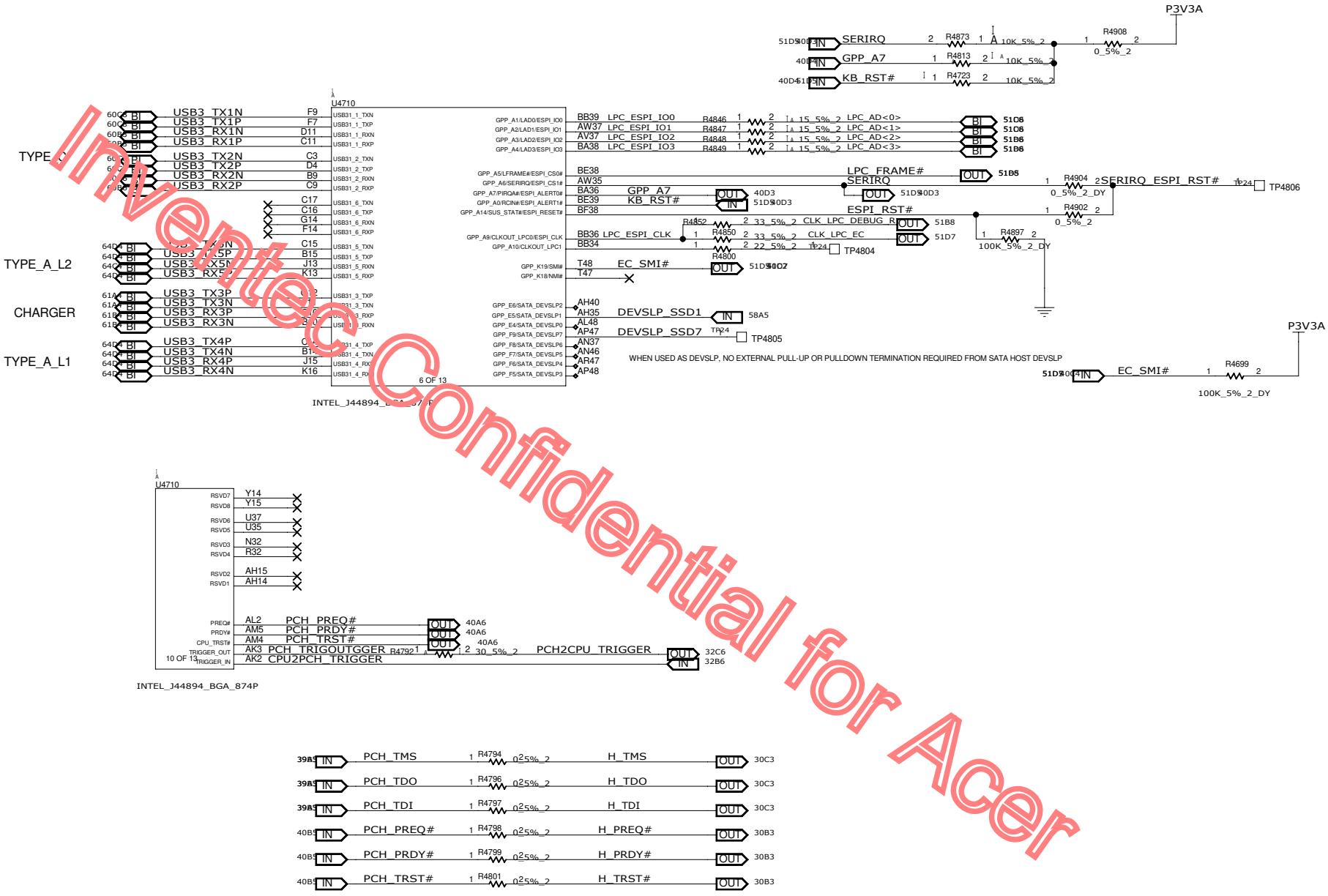
TITLE: MODEL,PROJECT,FUNCTION
PCH-CLINK,FAN,PCIE/SATA,HOST

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 38 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX





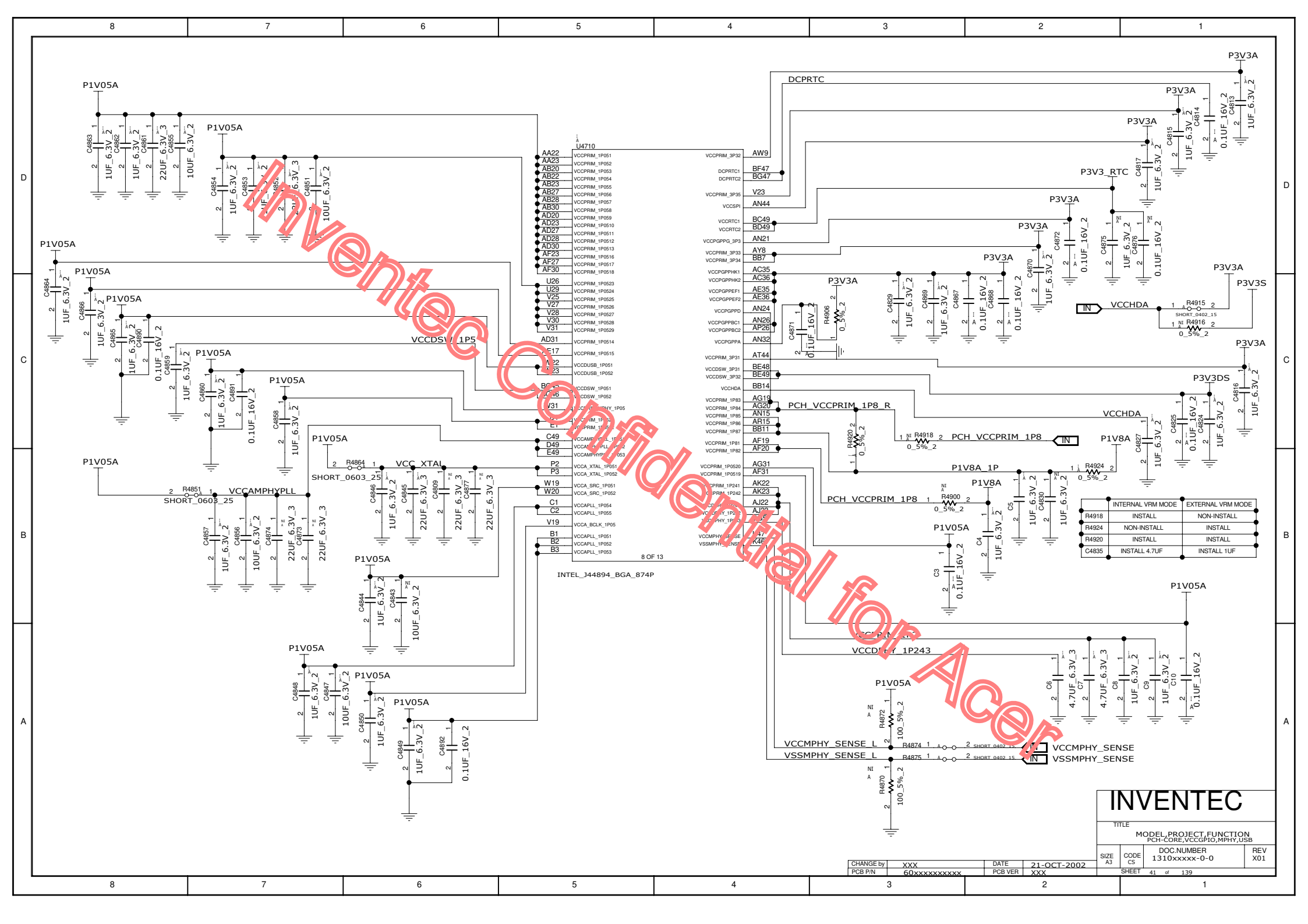
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

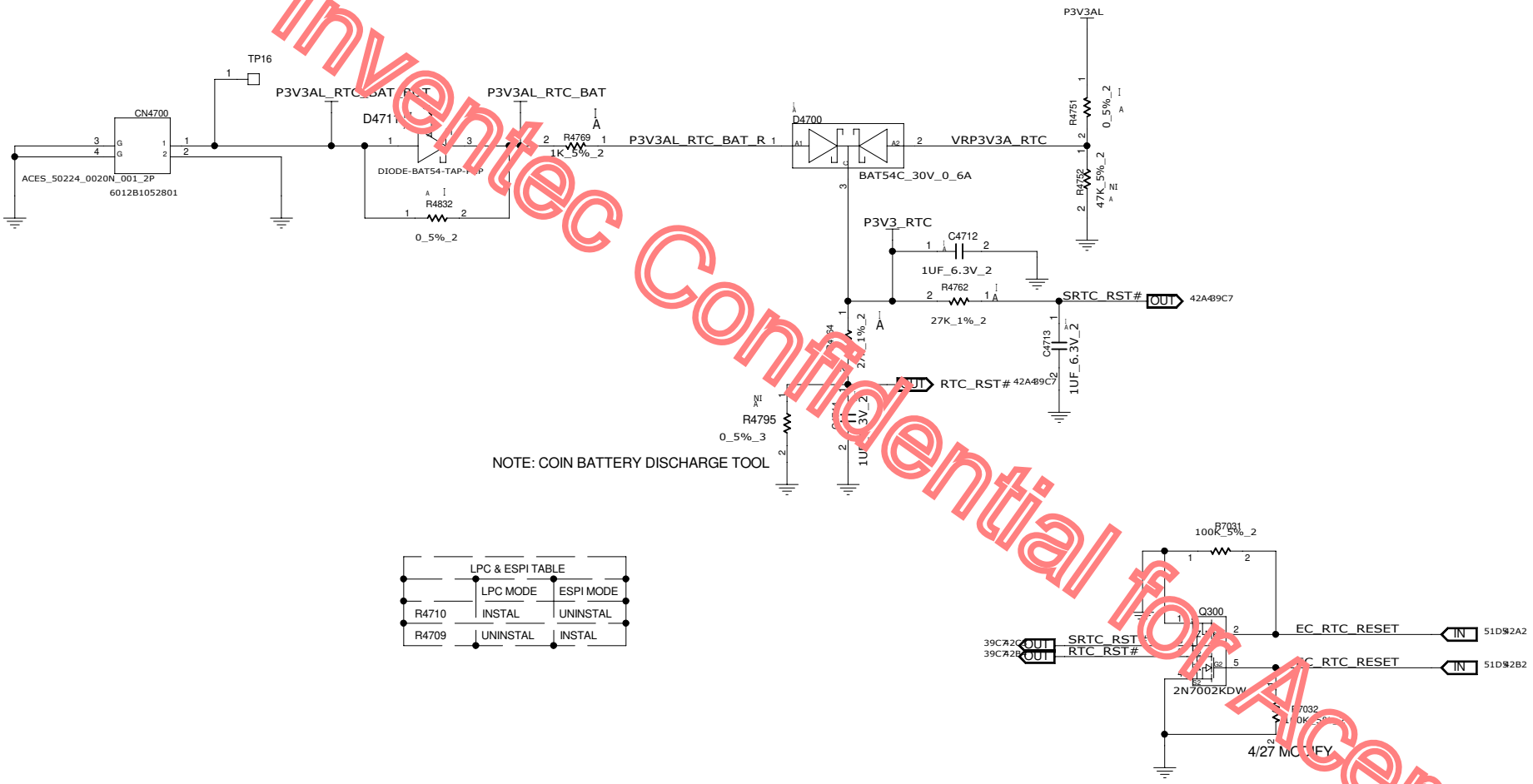
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-LPC/ESPI,USB,SATA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 40 of 139


U4710
INTEL_J44894_BGA_874P
8 OF 13
P1V05A
P3V3A
P3V3_RTC
P3V3S
P3V3DS
P1V8A
VCCHDA
DCPRTC
VCCDSW_1P1
VCCAMPHYPLL
VCC_XTAL
PCH_VCCPRIM_1P8_R
PCH_VCCPRIM_1P8
P1V8A_1P
VCCDSW_1P243
VCCMPHY_SENSE_L
VSSMPHY_SENSE_L
VCCMPHY_SENSE
VSSMPHY_SENSE
IN
R4915
R4916
R4918
R4920
R4924
R4900
R4851
R4864
R4872
R4874
R4875
R4870
SHORT_0603_25
SHORT_0402_15
0_5%_2
100_5%_2
INTERNAL VRM MODE
EXTERNAL VRM MODE
R4918 INSTALL NON-INSTALL
R4924 NON-INSTALL INSTALL
R4920 INSTALL INSTALL
C4835 INSTALL 4.7UF INSTALL 1UF
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
PCH-CORE,VCCGPIO,MPHY,USB
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 41 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX
Inventec Confidential for Acer



LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R4710	INSTAL	UNINSTAL
R4709	UNINSTAL	INSTAL

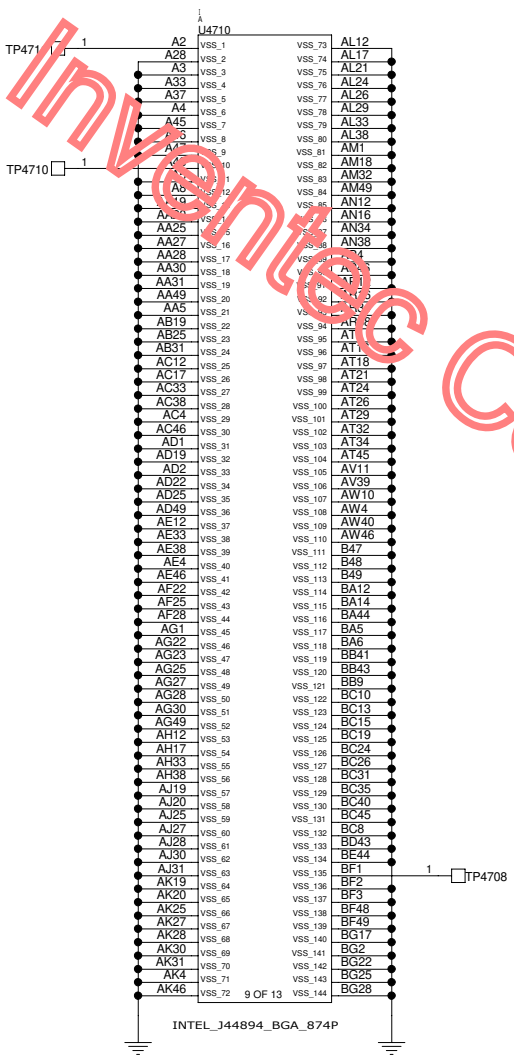
INVENTEC

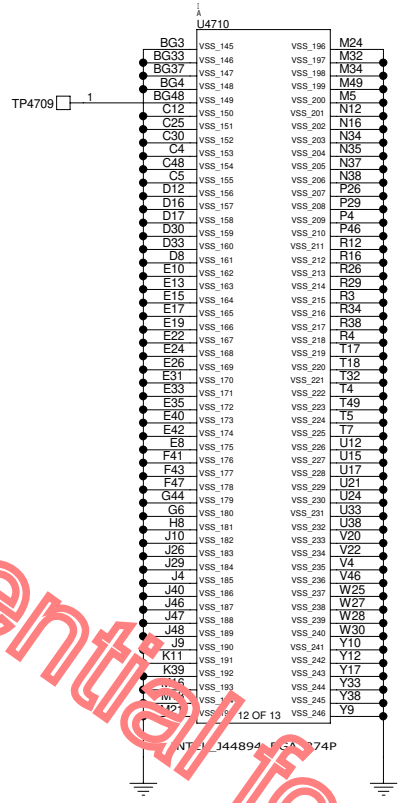
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 42 of 139





CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GND

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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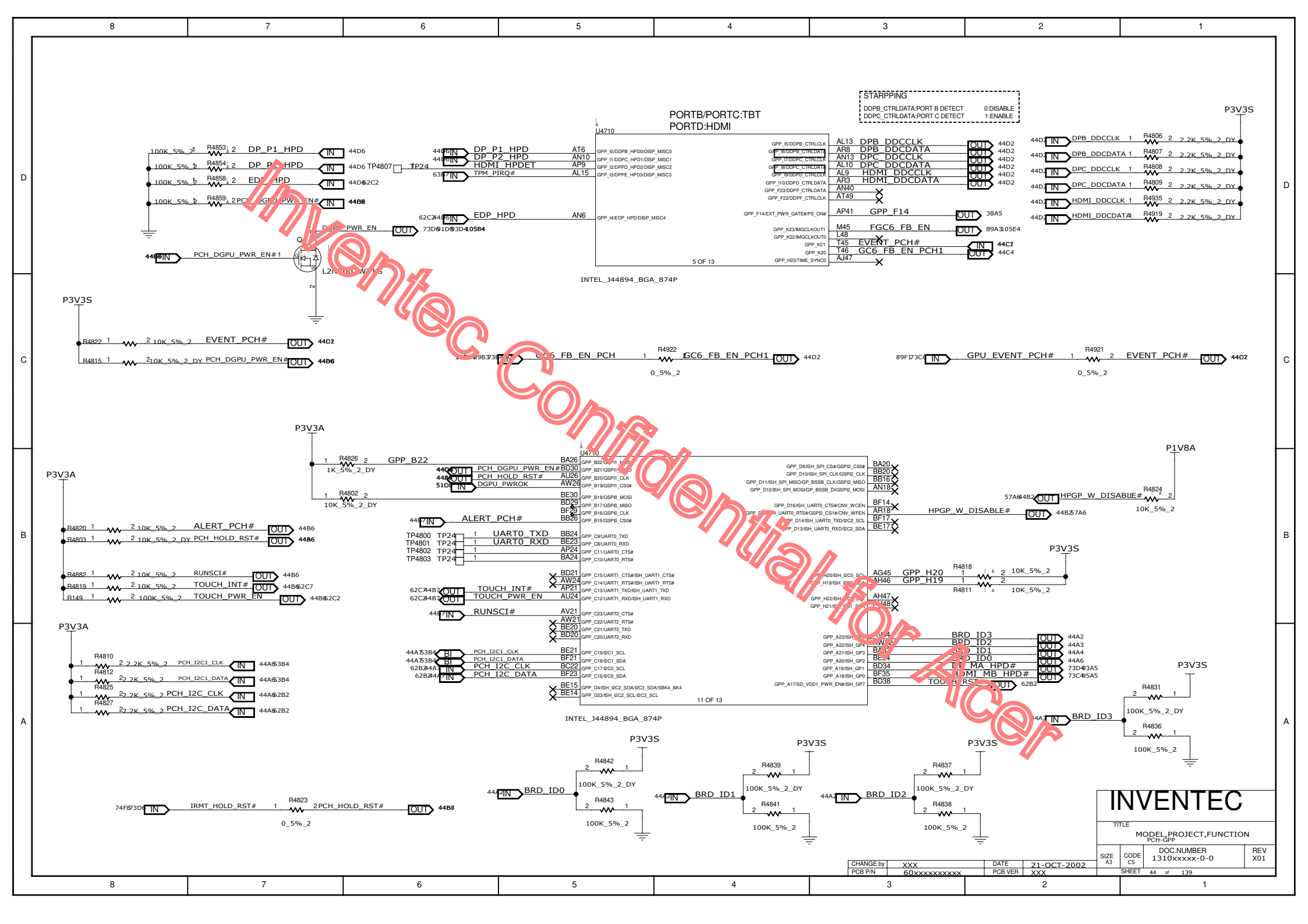


CHANGE by	XXX
PCB P/N	60xxxxxxxxxx
DATE	21-OCT-2002
PCB VER	XXX

INVENTEC

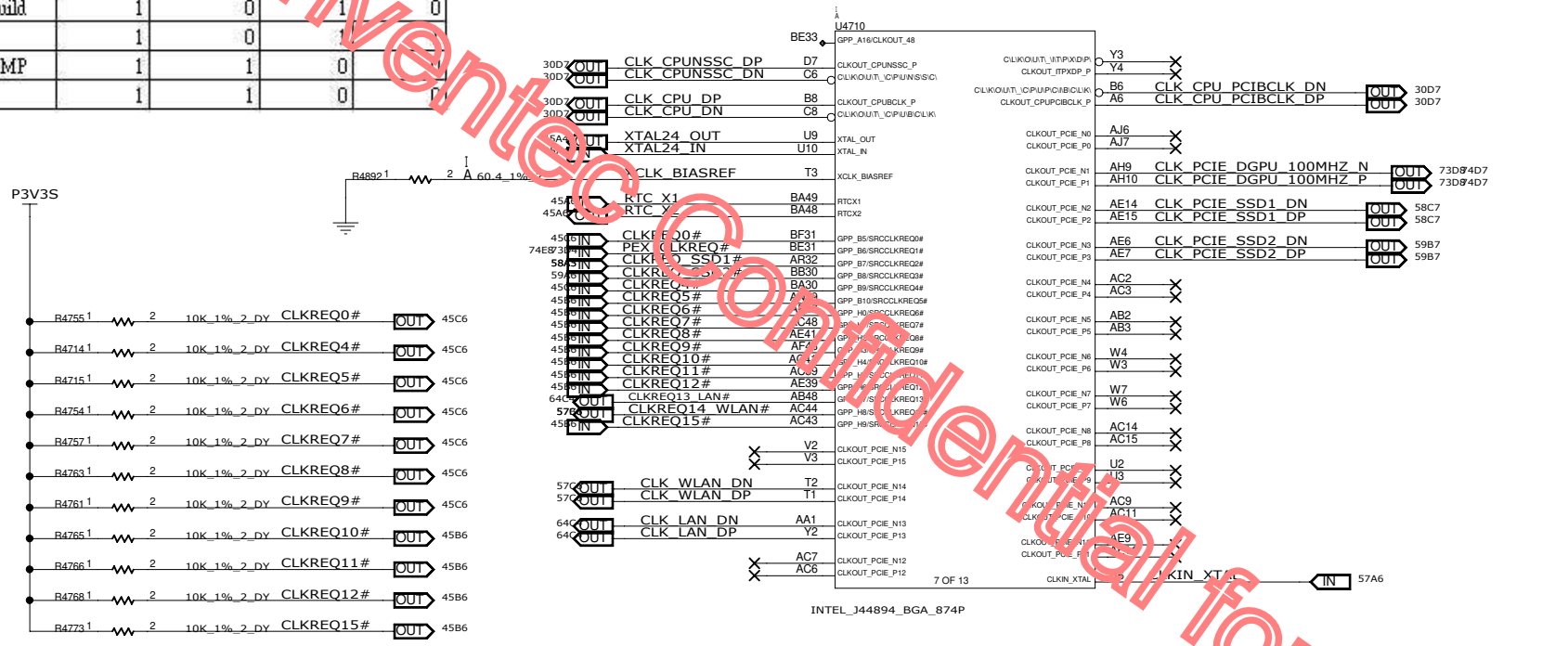
TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP

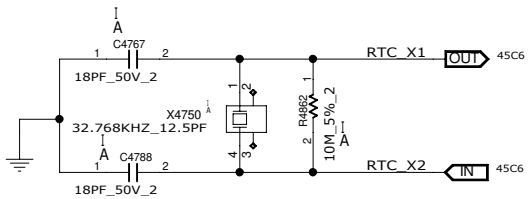
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

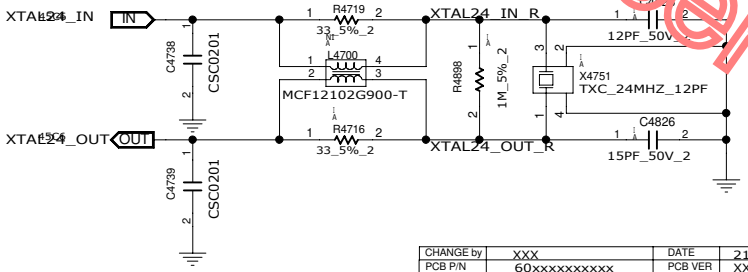
SHEET 44 of 139

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	1

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







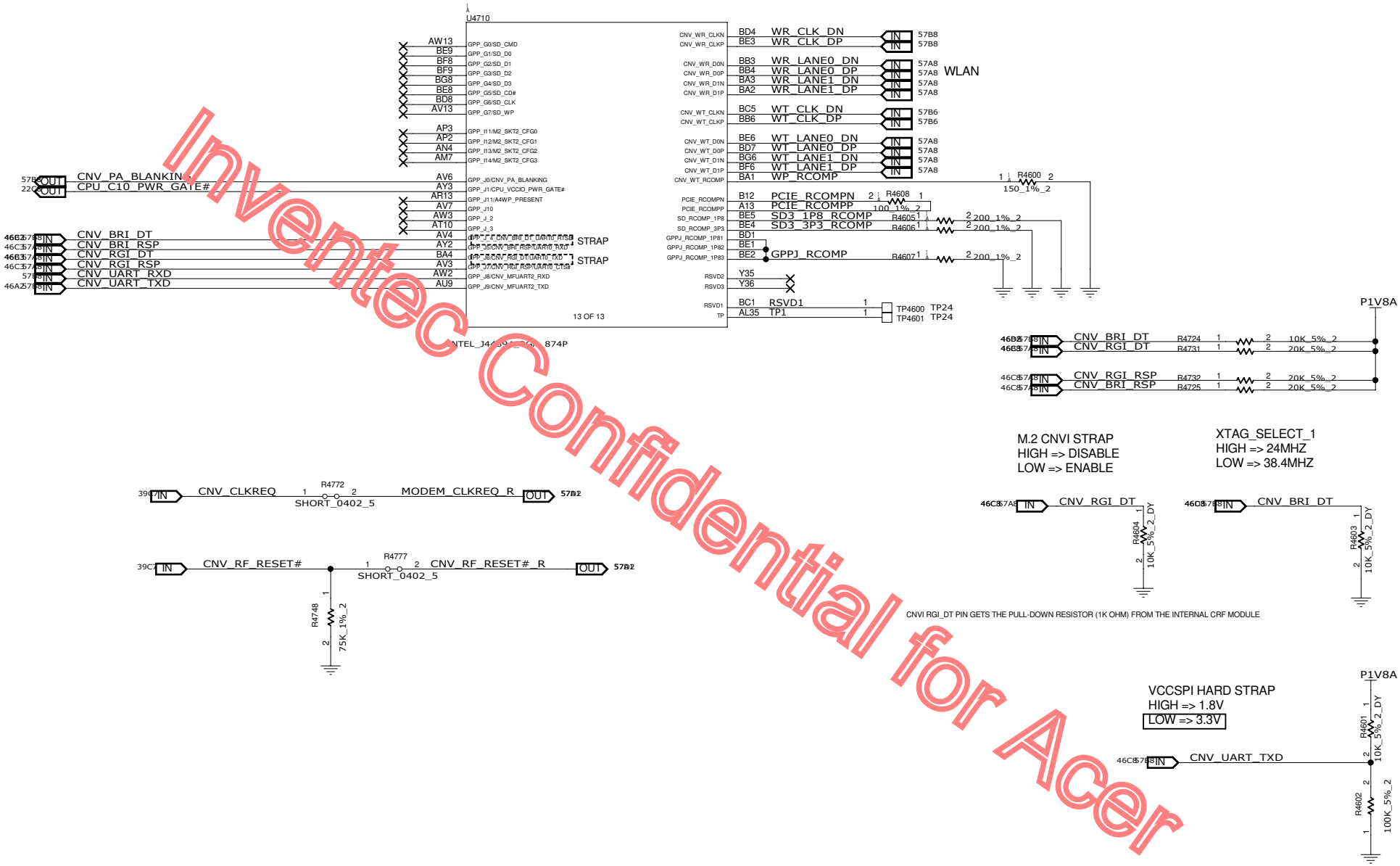
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

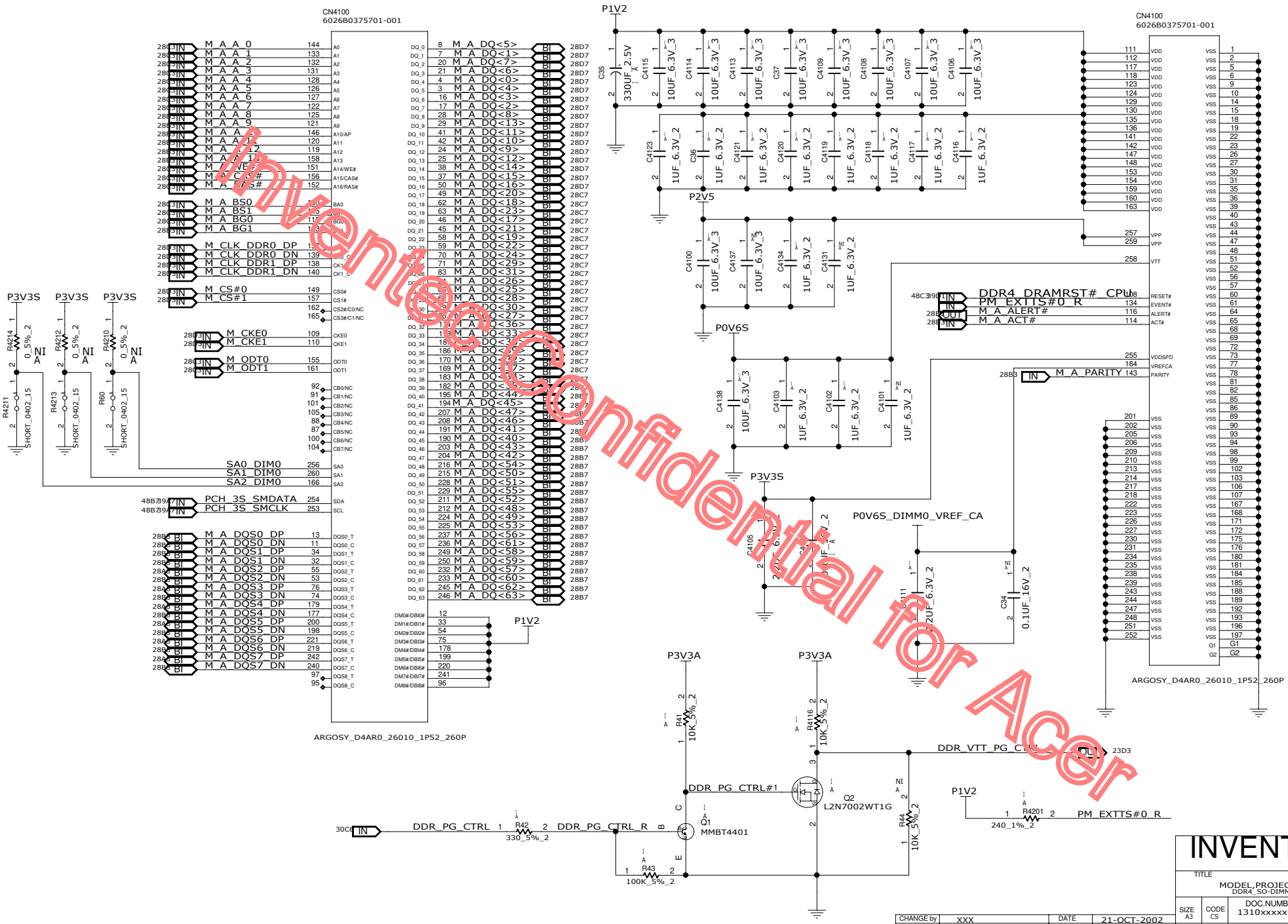
INVENTEC

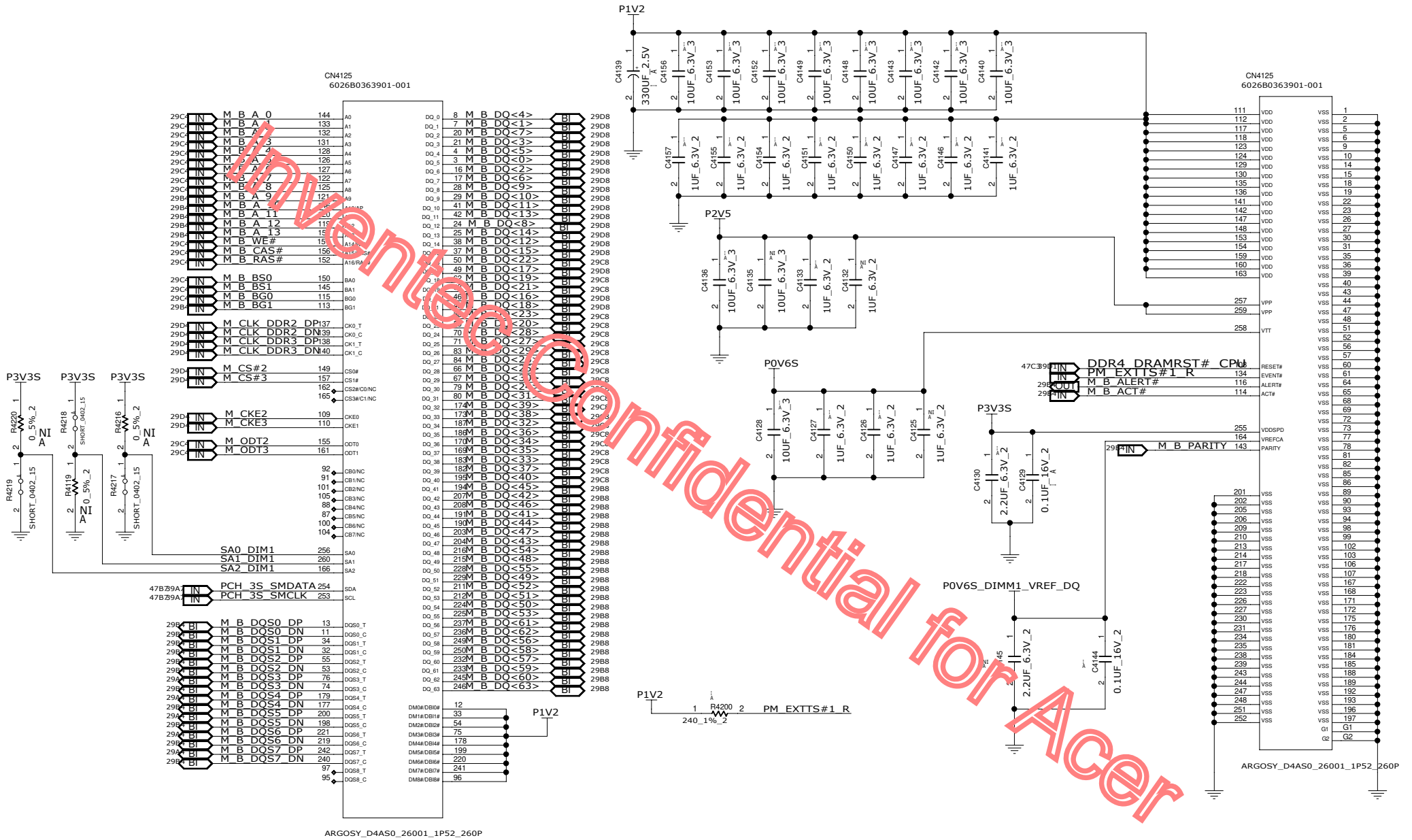
TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP,CLKOUT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 45 of 139







CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DDR4,SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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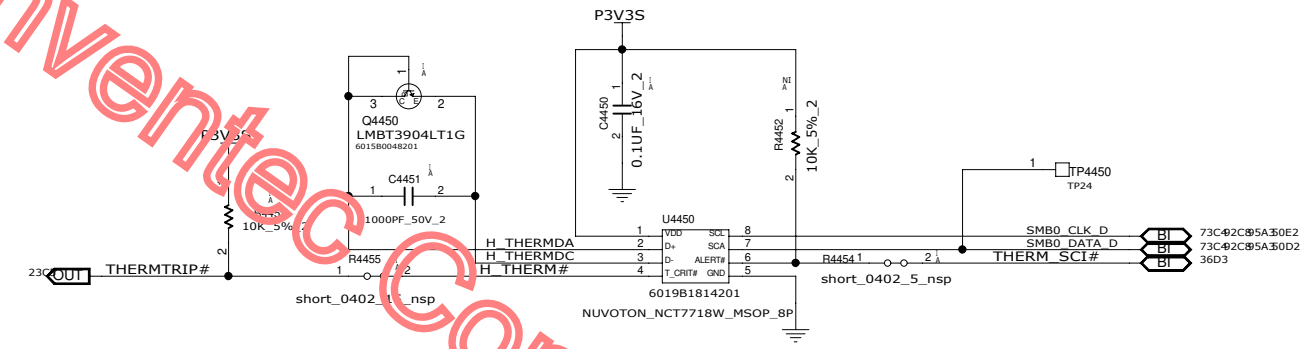
REFERENCE NUMBER:4450~4499

THERM SENSOR

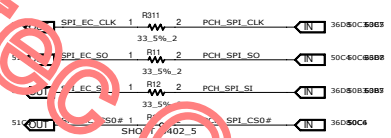


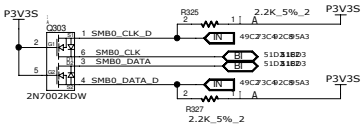
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 49 of 139			

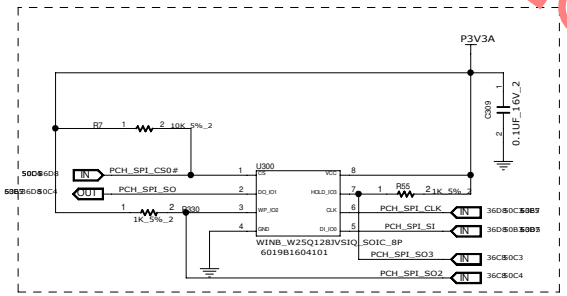
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

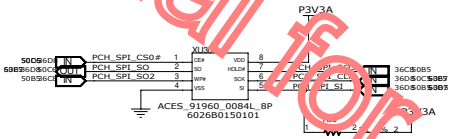
REFERENCE 300~389(KBC)





THERMAL SENSOR
HDMI
DP





R390 FOR INTEL DEBUG

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5

U1

ITE_IT8987E_CX_LQFP_128P_HP

6019B1650401

Platform	Intel	AMD
R319,R318	10KΩ	NA

Platform	Intel	AMD
R315	330Ω	0Ω

	MOUNT	OPEN
R392	MOUNT	OPEN
R393	OPEN	MOUNT

Phase_ID	B	A	C / D
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	G2	G1	G0
R343	10K_short	10K_open	10K_short
R338	10K_open	10K_short	10K_short

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

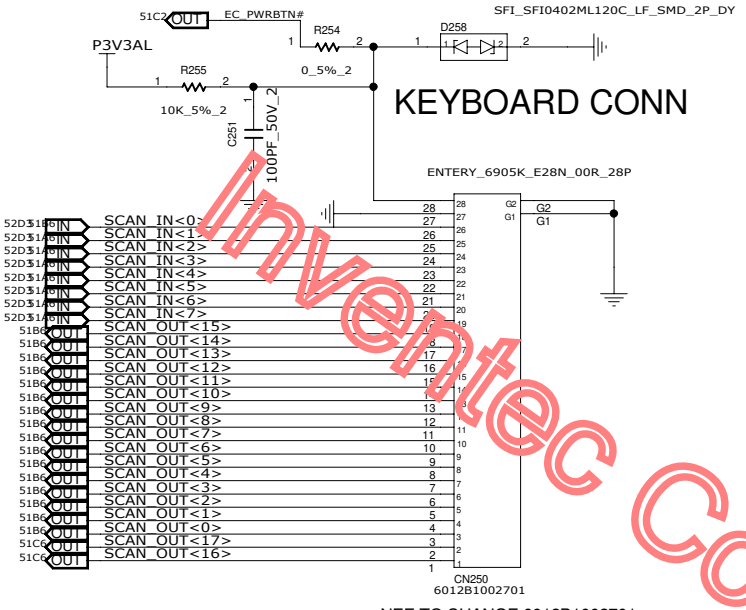
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 51 of 139

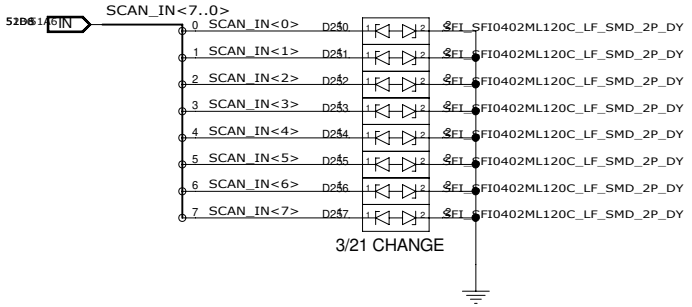
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)

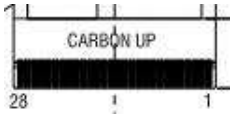


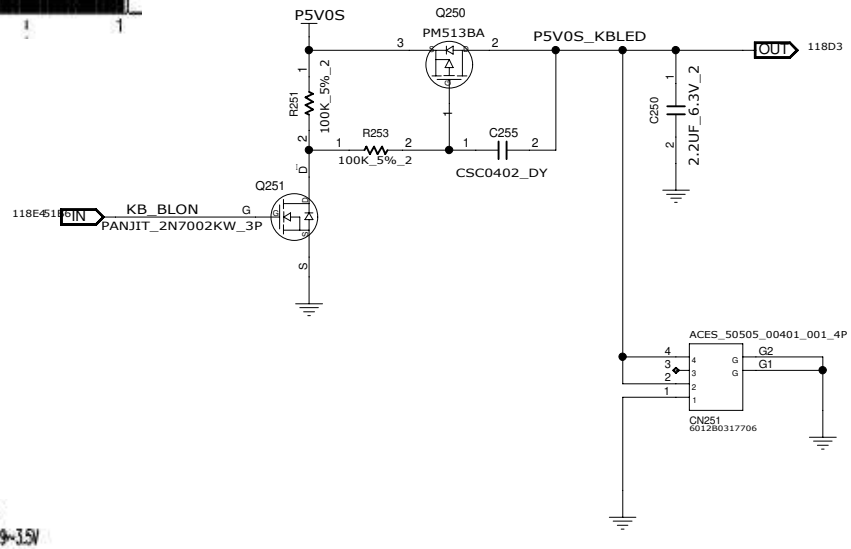
KEYBOARD CONN

NEE TO CHANGE 6012B1002701
5/2 REVERSE

	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
	R17







KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

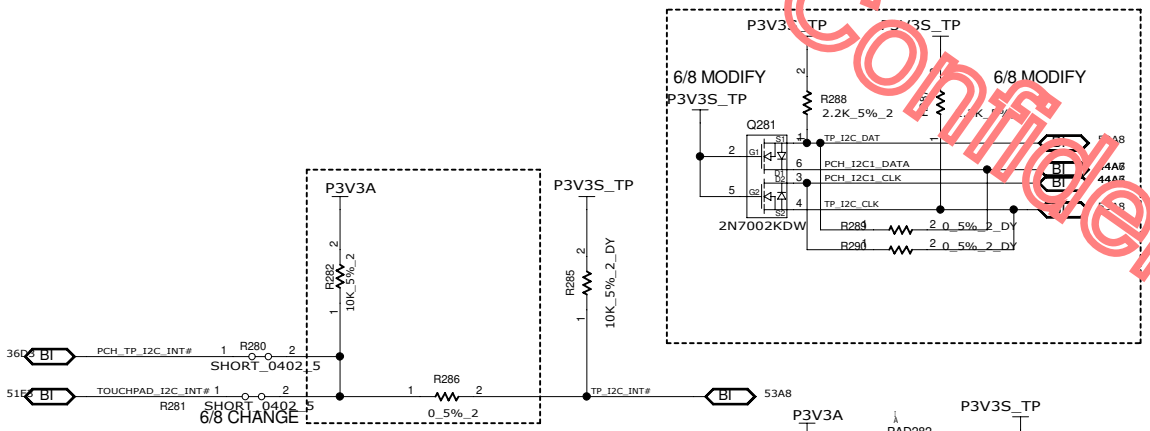
INVENTEC

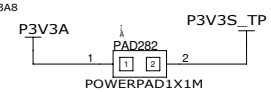
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

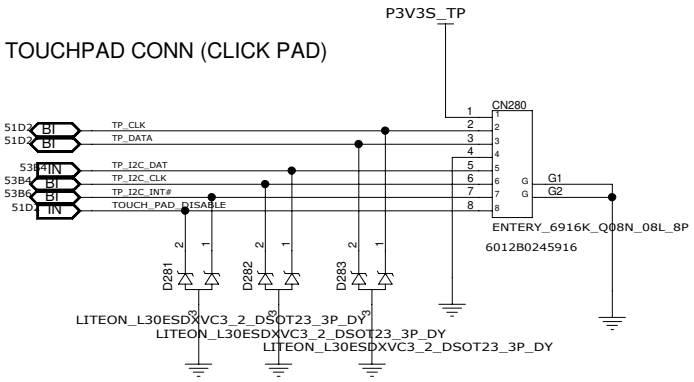
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 52 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX







CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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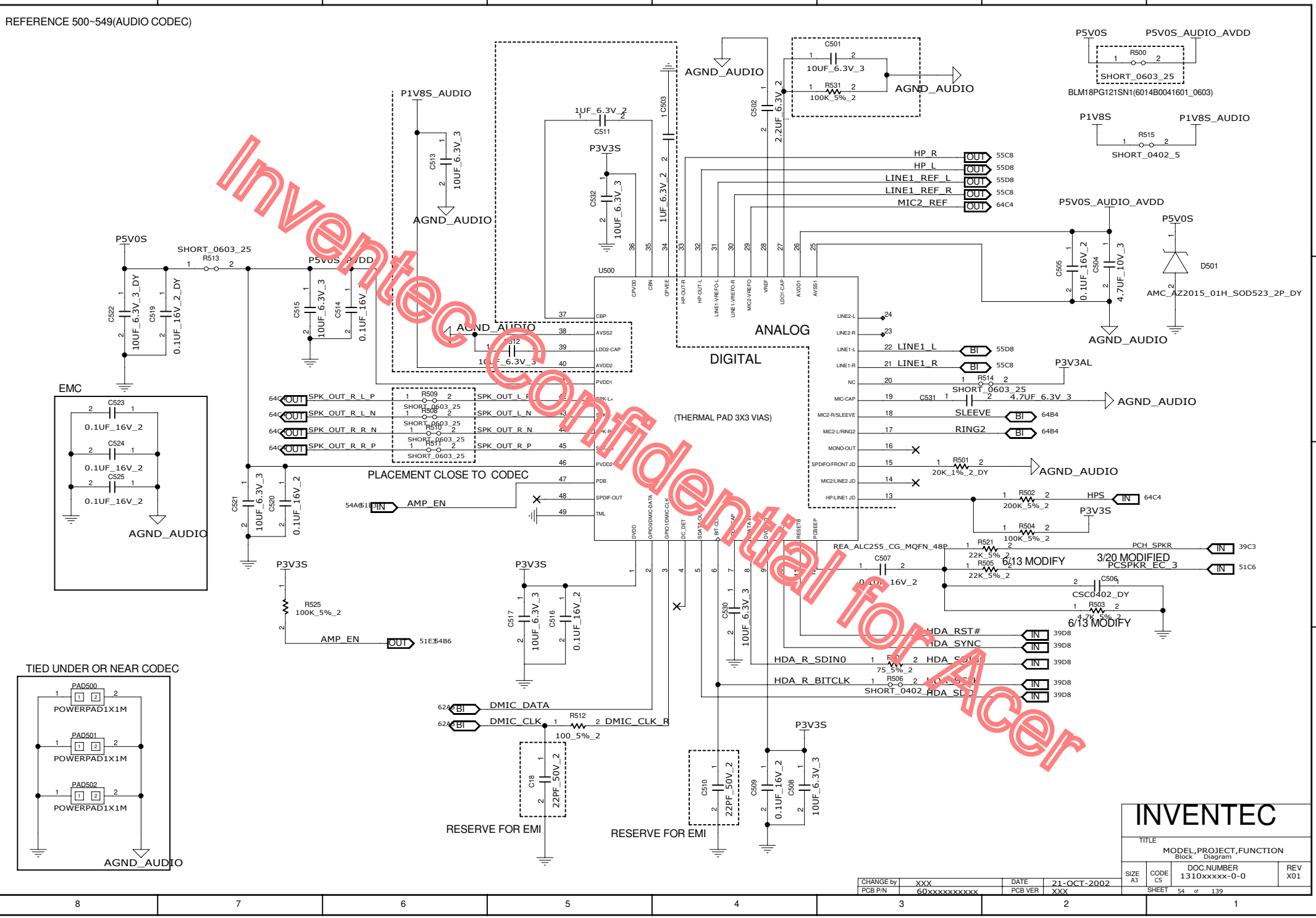
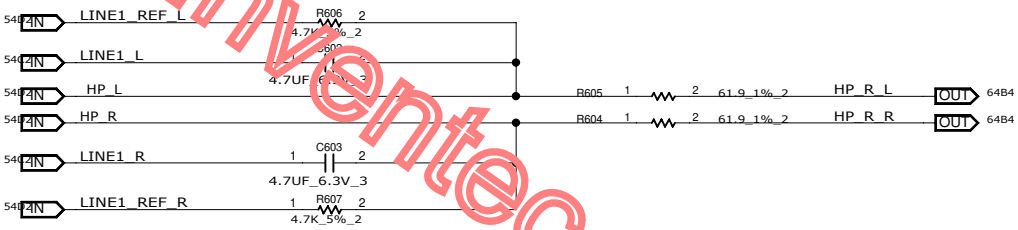


REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749

1.15A

PAD1700

POWER_PAD1X1M

22UF_6.3V_5

0.1uF_16V_2

CABLE PIN DEFINE FOLLOW ARGAMA

CN1700

PCIE17_HDD_RX_DP
PCIE17_HDD_RX_DN
PCIE17_HDD_TX_C_DN
PCIE17_HDD_TX_C_DP

C1702
C1703

PCIE17_HDD_RX_C_DP
PCIE17_HDD_RX_C_DN

G1
G2

ACES_51540_01041_Q01_10P
6012B0541002

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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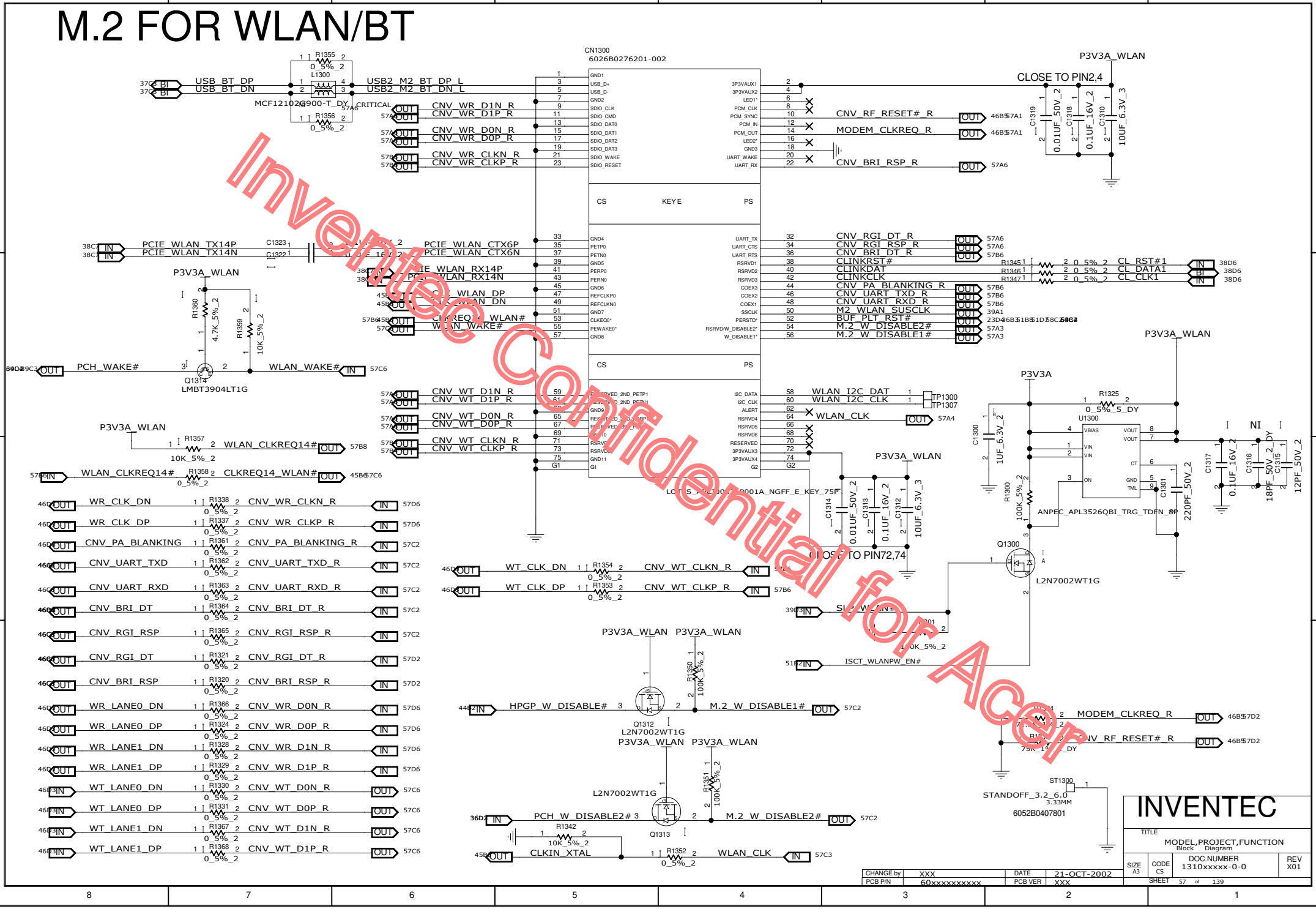
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

M.2 FOR WLAN/BT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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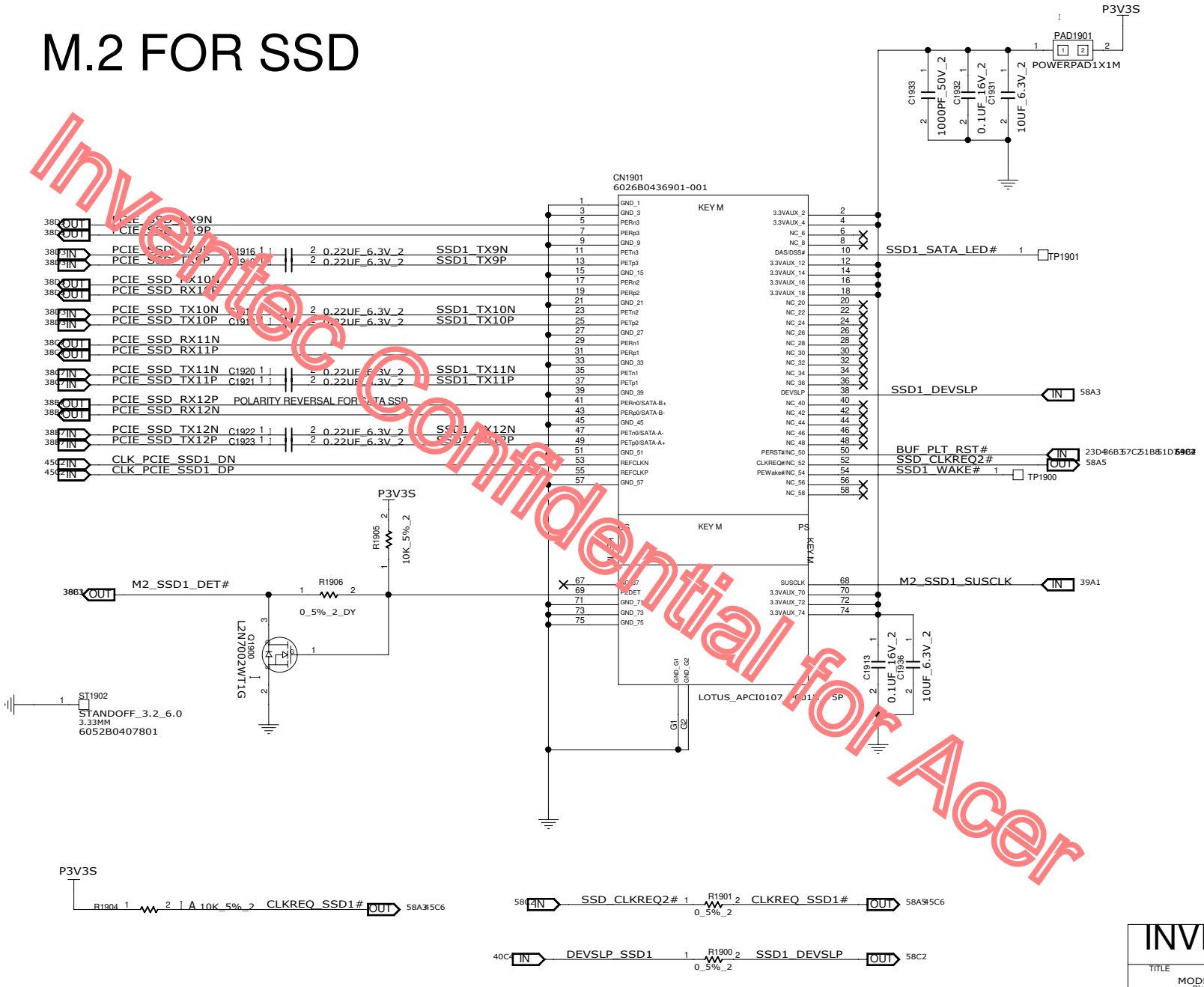
M.2 FOR SSD



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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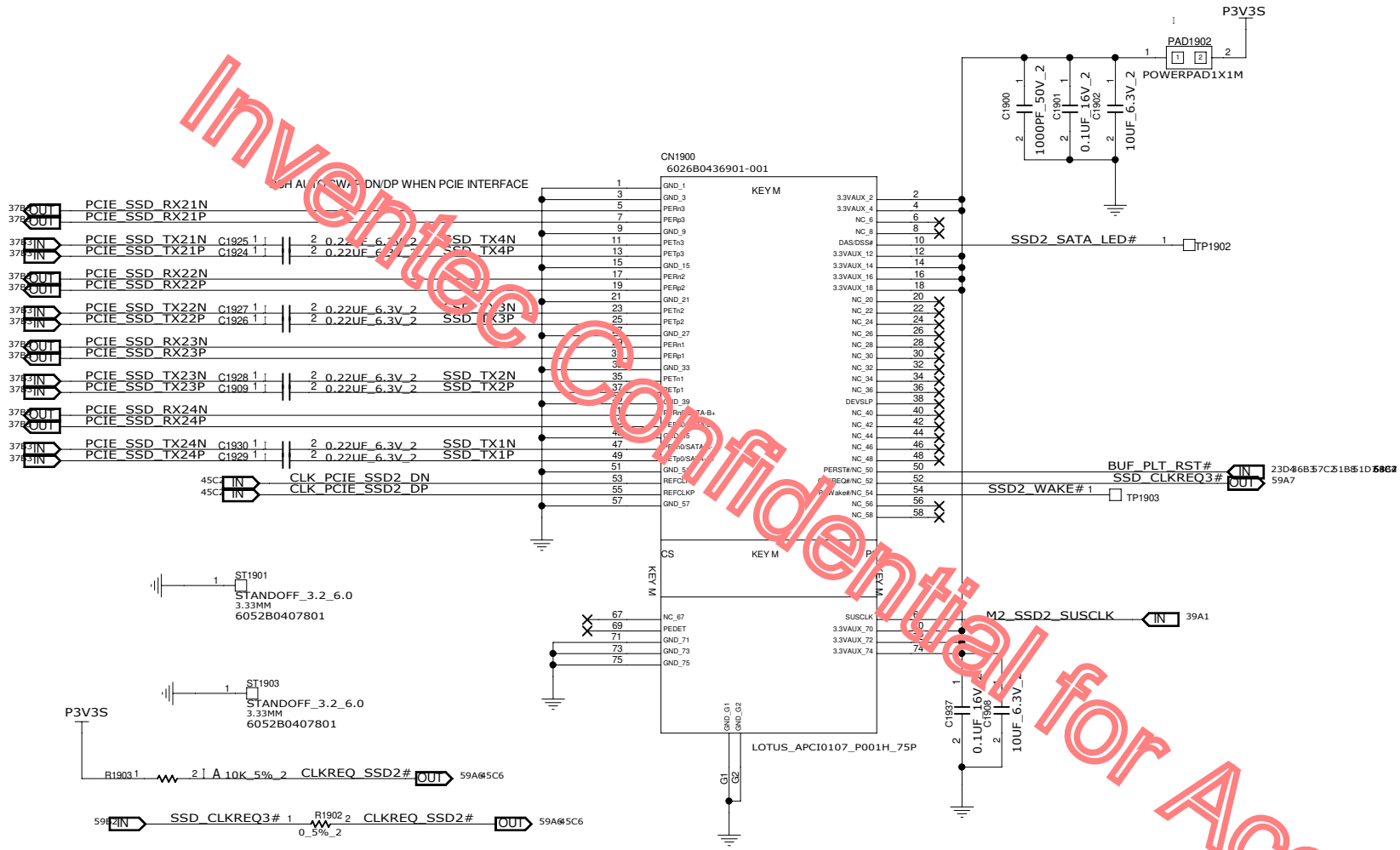
NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

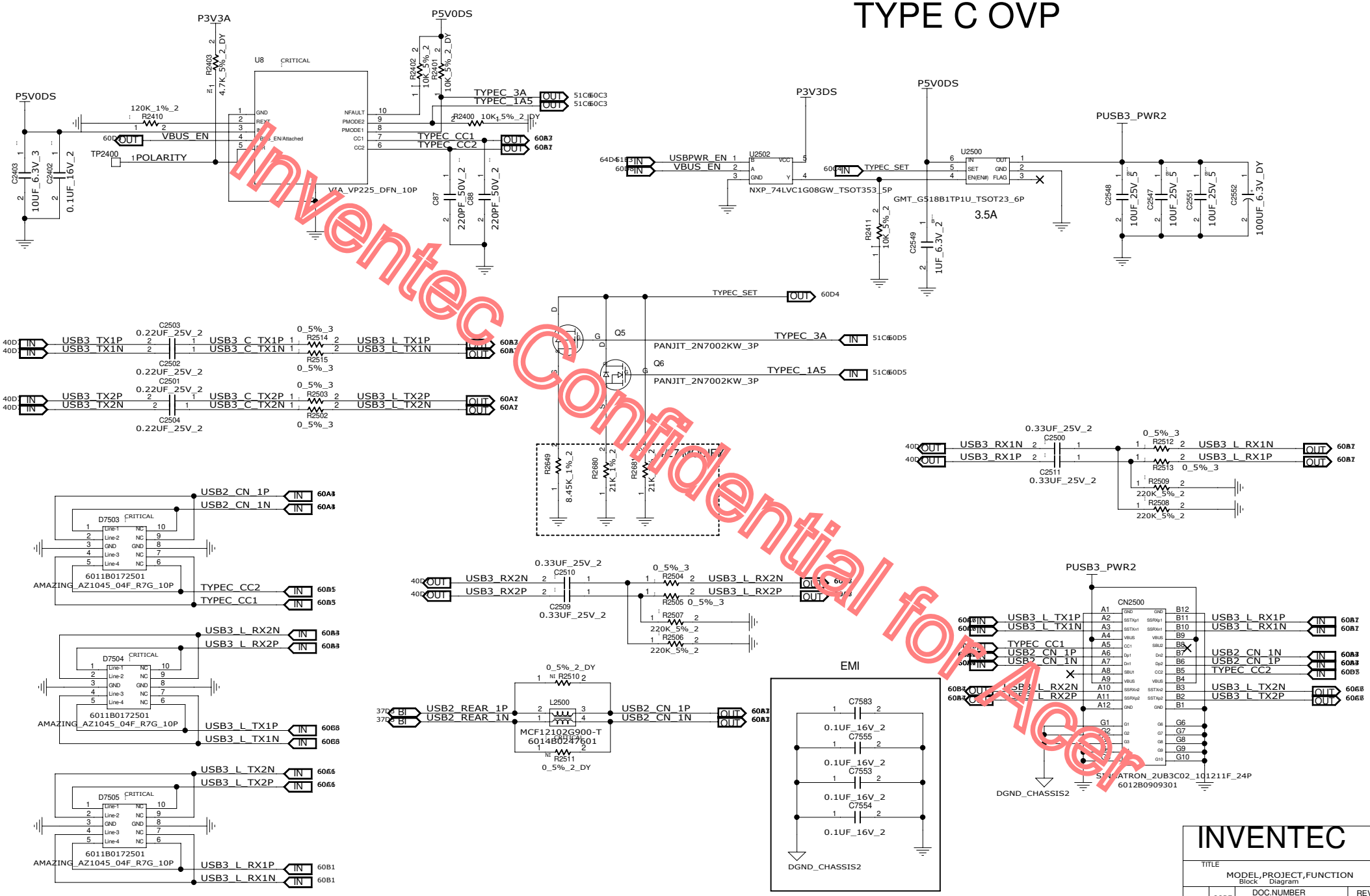
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION SATA HDD CONN.
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	59 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TYPE C OVP



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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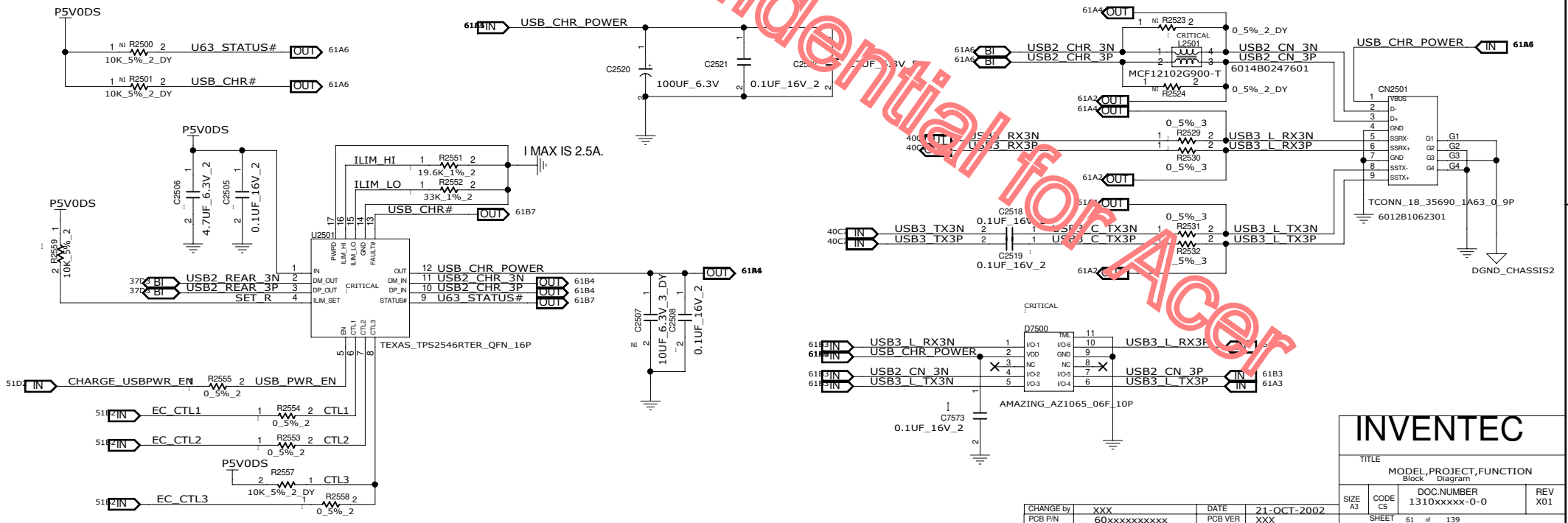
USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl-Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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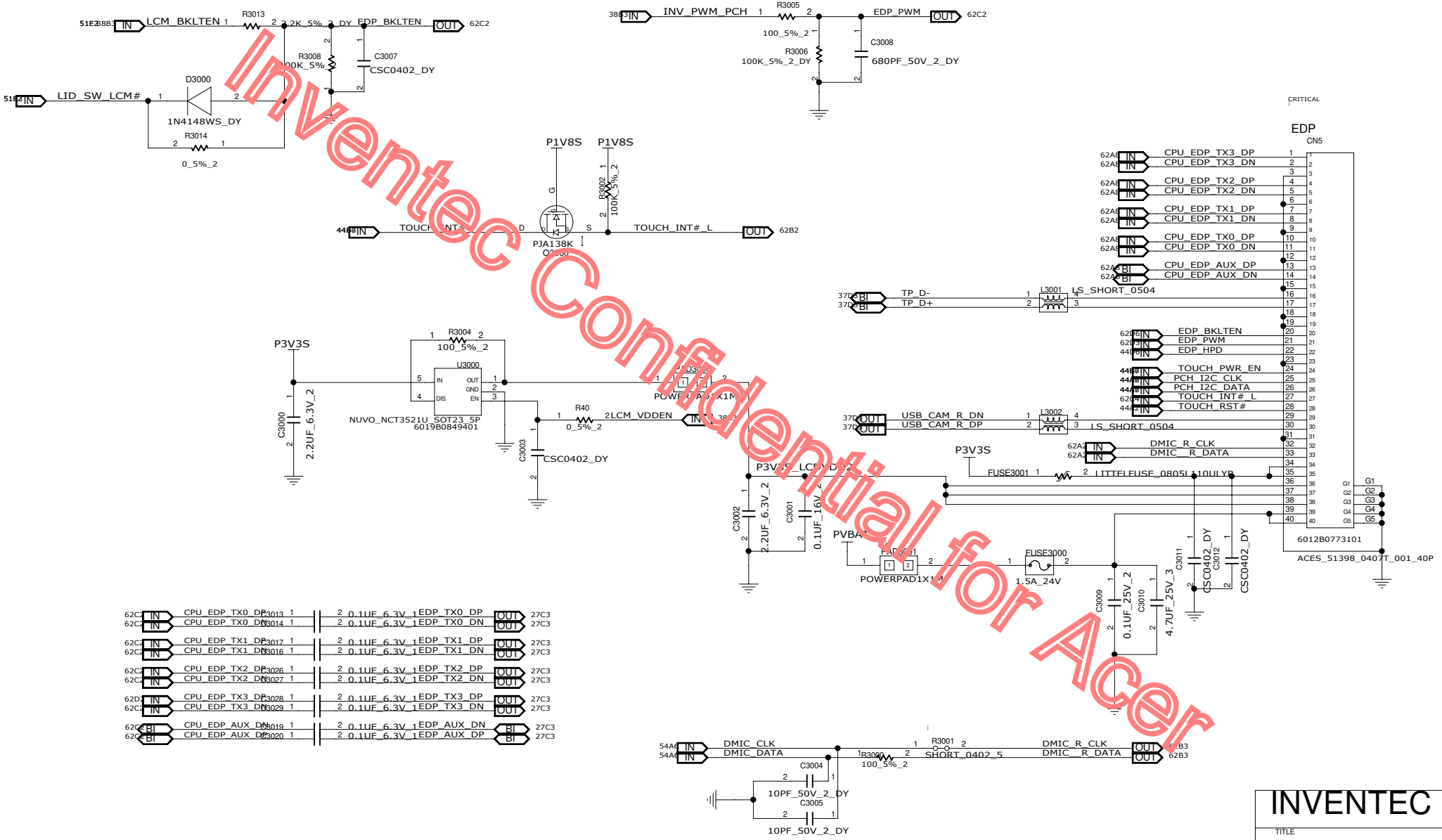
REFFERENCE 3000~3049(LCM)

EDP CONN



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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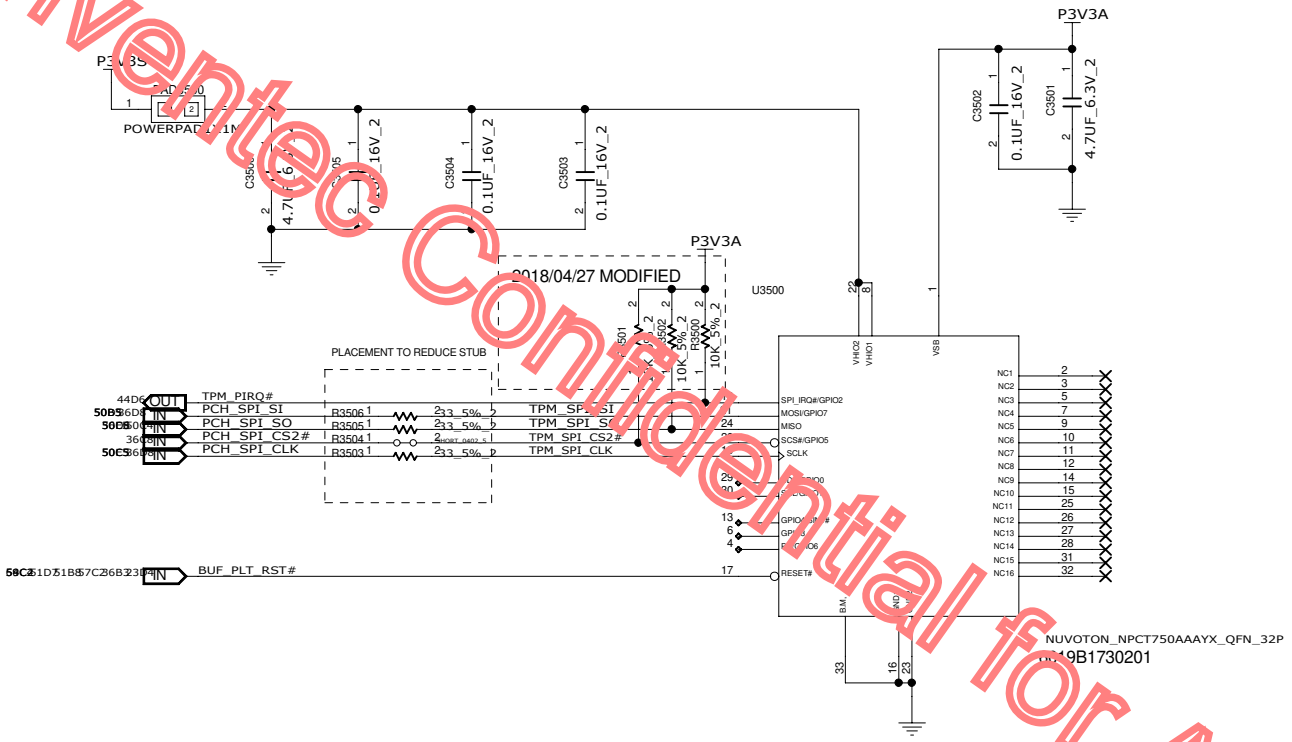
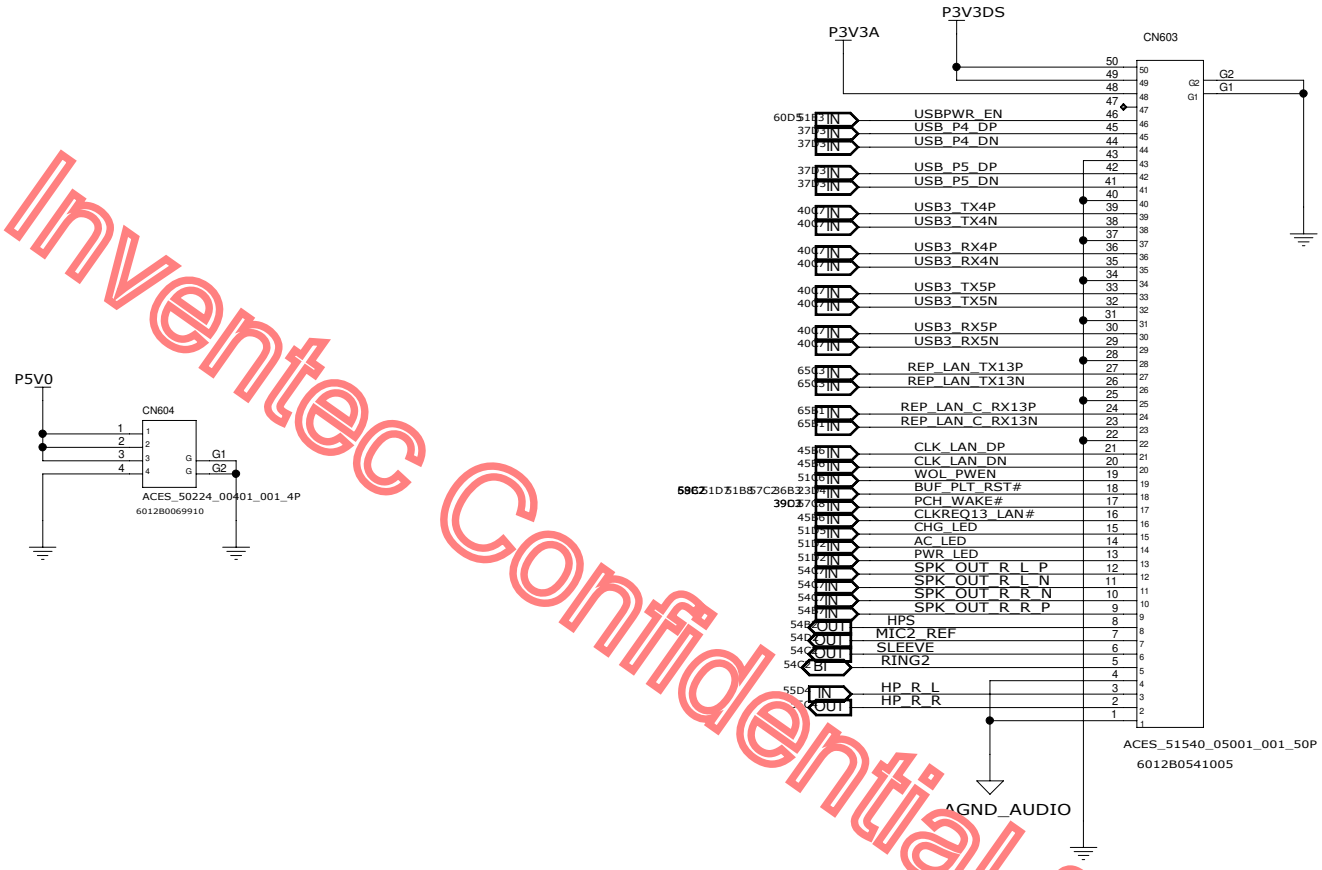


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 63 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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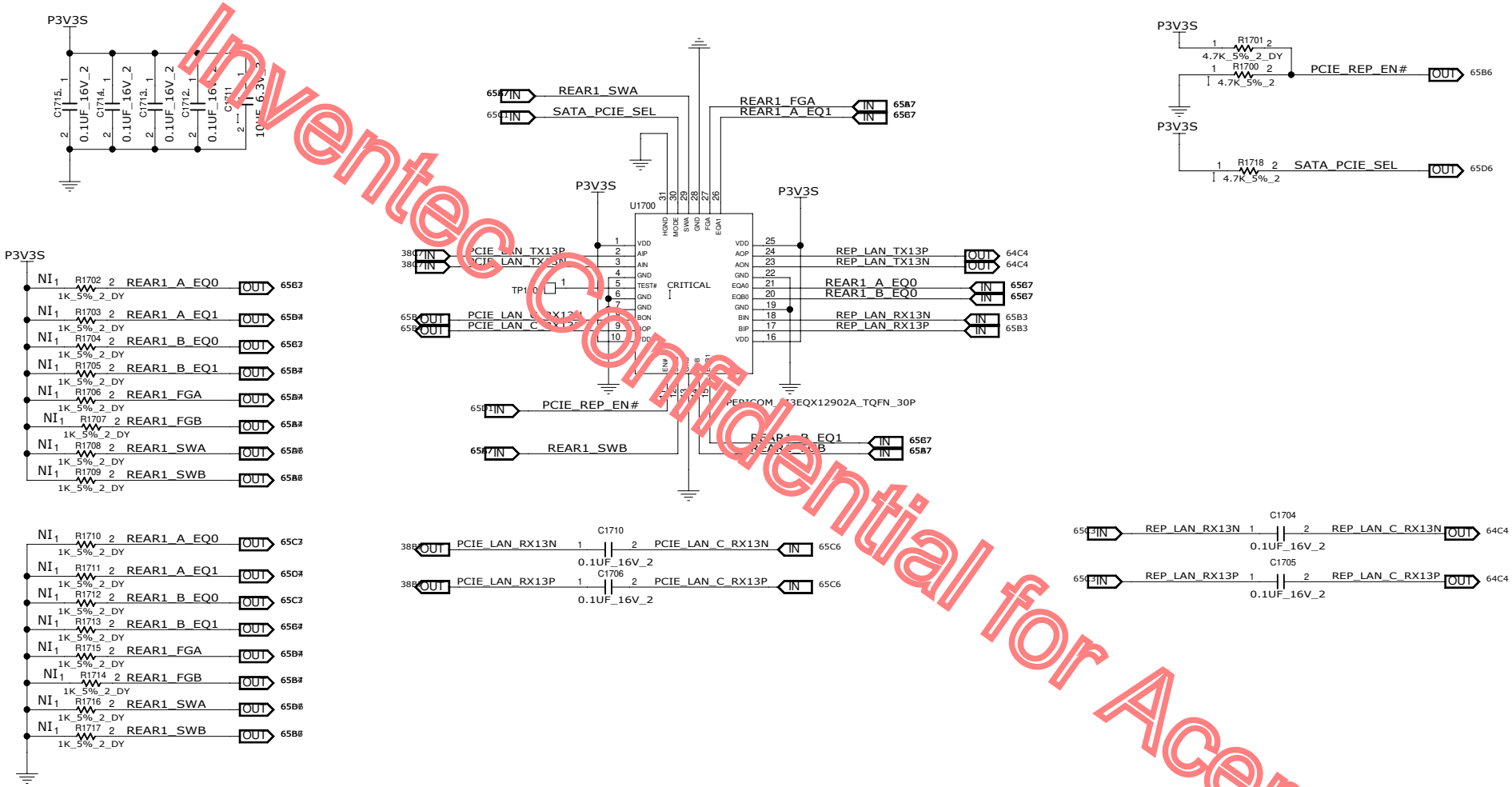
PCIE REPEATER



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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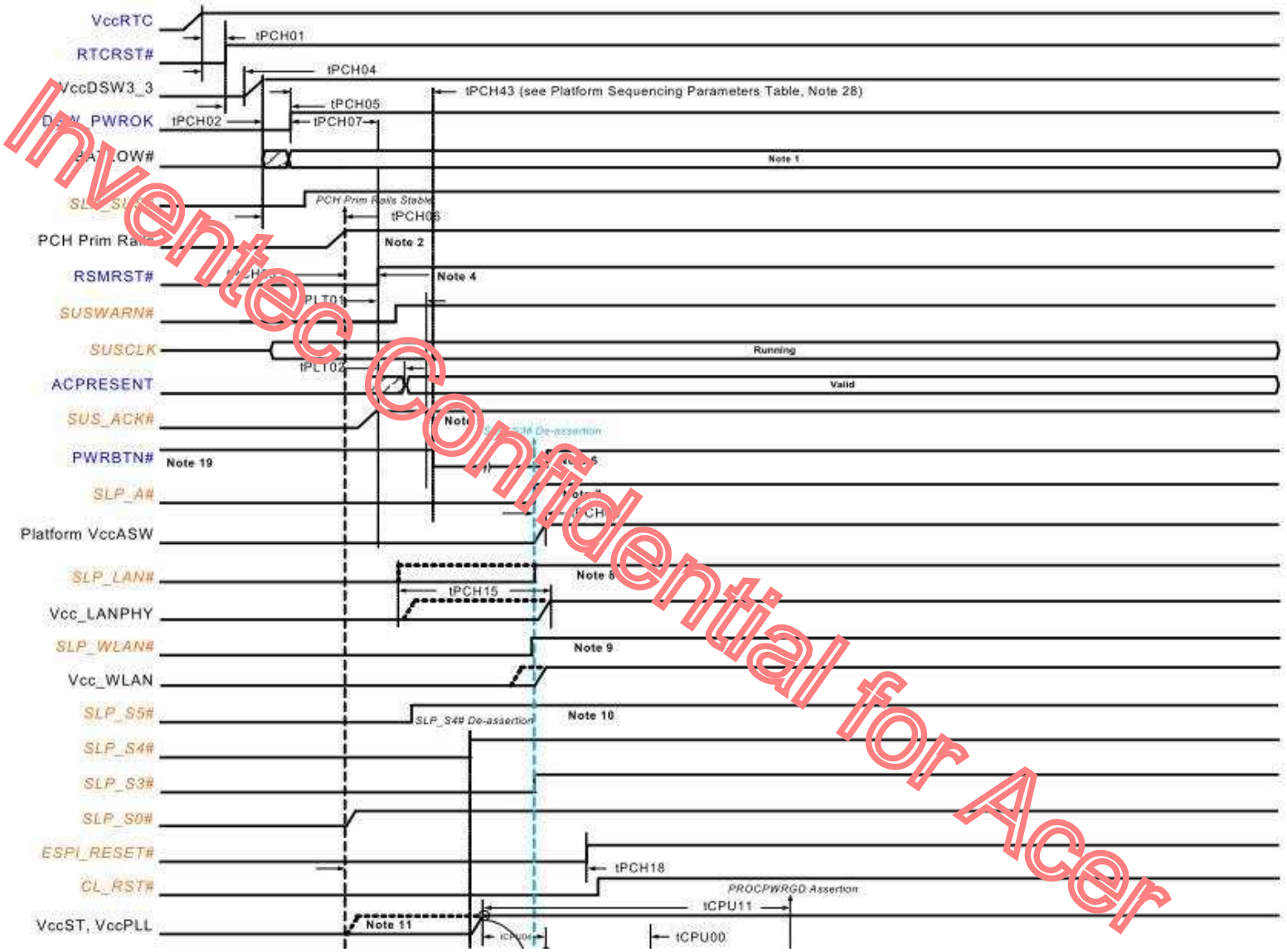
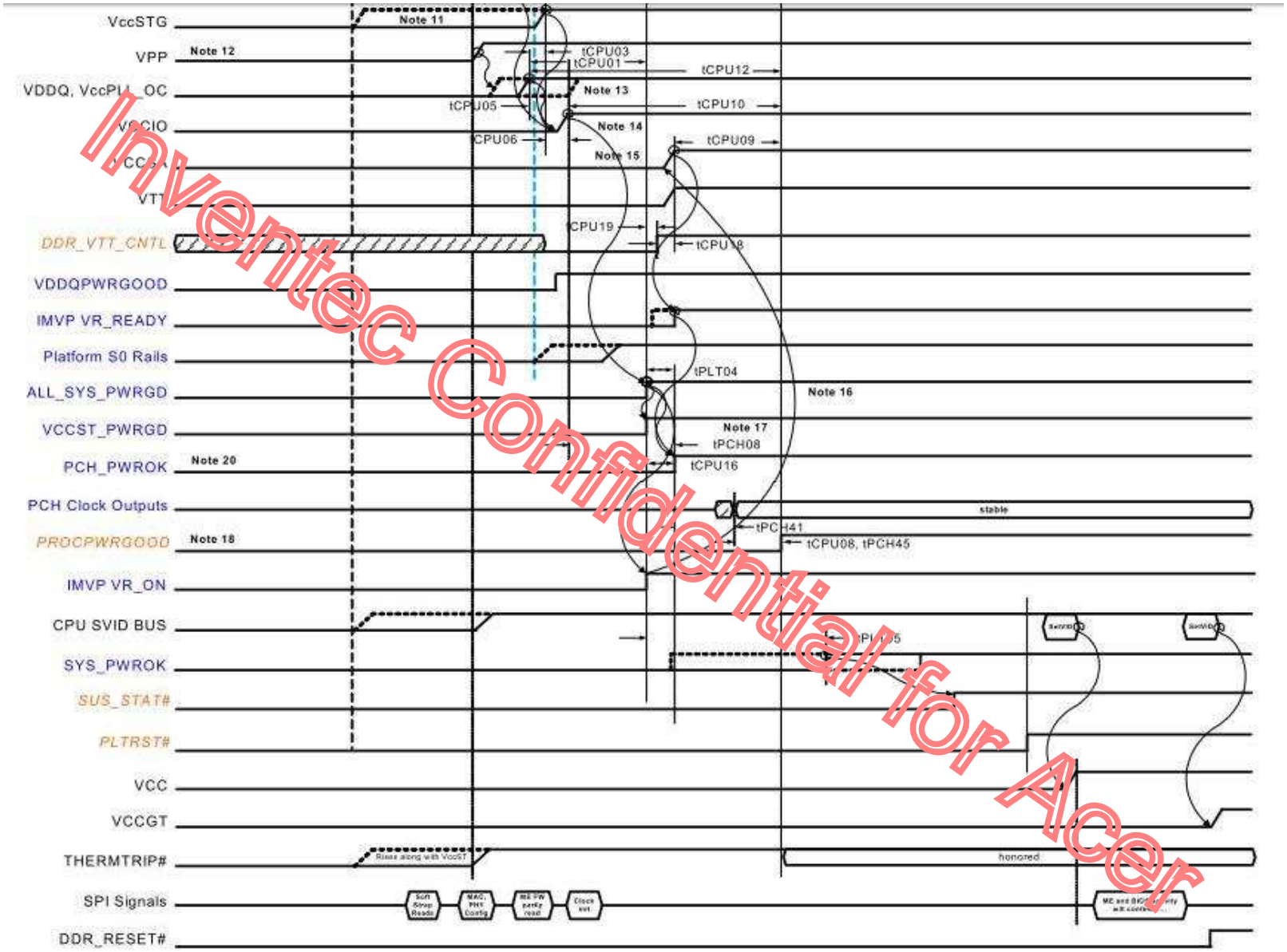


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 66 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 67 of 139	

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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N18E-G0
N18E-G1
N18E-G2 MAX-Q

8GB DDR5 256M X 16 X 2 X6

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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PCA CODE NAME： N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001
G1 : 6019B1849201
G2 MAXQ:6019B1849301

PCB VERSION：X01
BOARD SIZE:

SCH P/N:
PCB P/N:
PCA P/N:

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MAINBOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (MP86916A_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (RT8068A)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (RT8068A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOS	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
93	GPU DP CONNECTOR	123	
94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OVR-M	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL
NI: NON-INSTALL
DY: NON-INSTALL
MP: PRODUCTION
PROTO: PRE-PRODUCTION
CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847901

MICRON MT61K256M32JE-14:A
6019B1847701

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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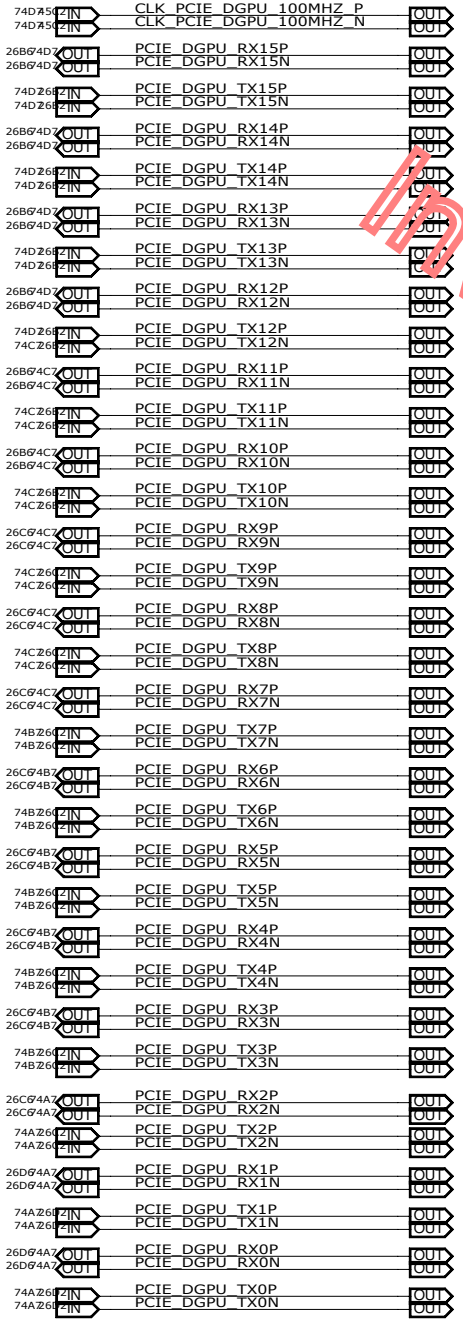
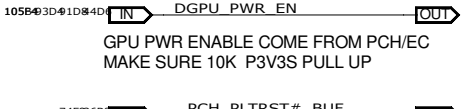
CONNECTION TO MAINBOARD

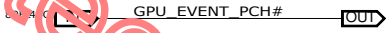




GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND
TO PCH



OR / GPU WILL EXIT GC6 MODS

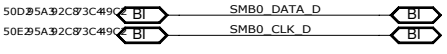
15.3.2 PWR_LEVEL* (GPIO12)

The POWER_LEVEL input signal triggers an immediate GPU hardware slowdown followed by the driver capping the GPU power state to the appropriate limit. There are events that can trigger this signal assertion: AC to battery power transition, total system power overdraw event.

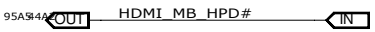
PCIE CLK REQUESTD#

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

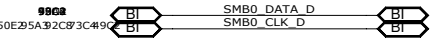
DP HPD TO MAINBOARD
MAKE SURE 10K P3V3S PULL UP



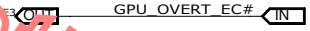
DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP



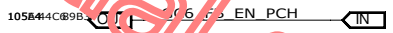
HDMI HPD TO MB



HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

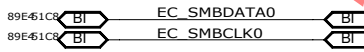


3.3V LEVEL
OVER TEMPERATURE TO PCH OR EC



3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC



GPU I2C, COMMUNCATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

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INVENTEC

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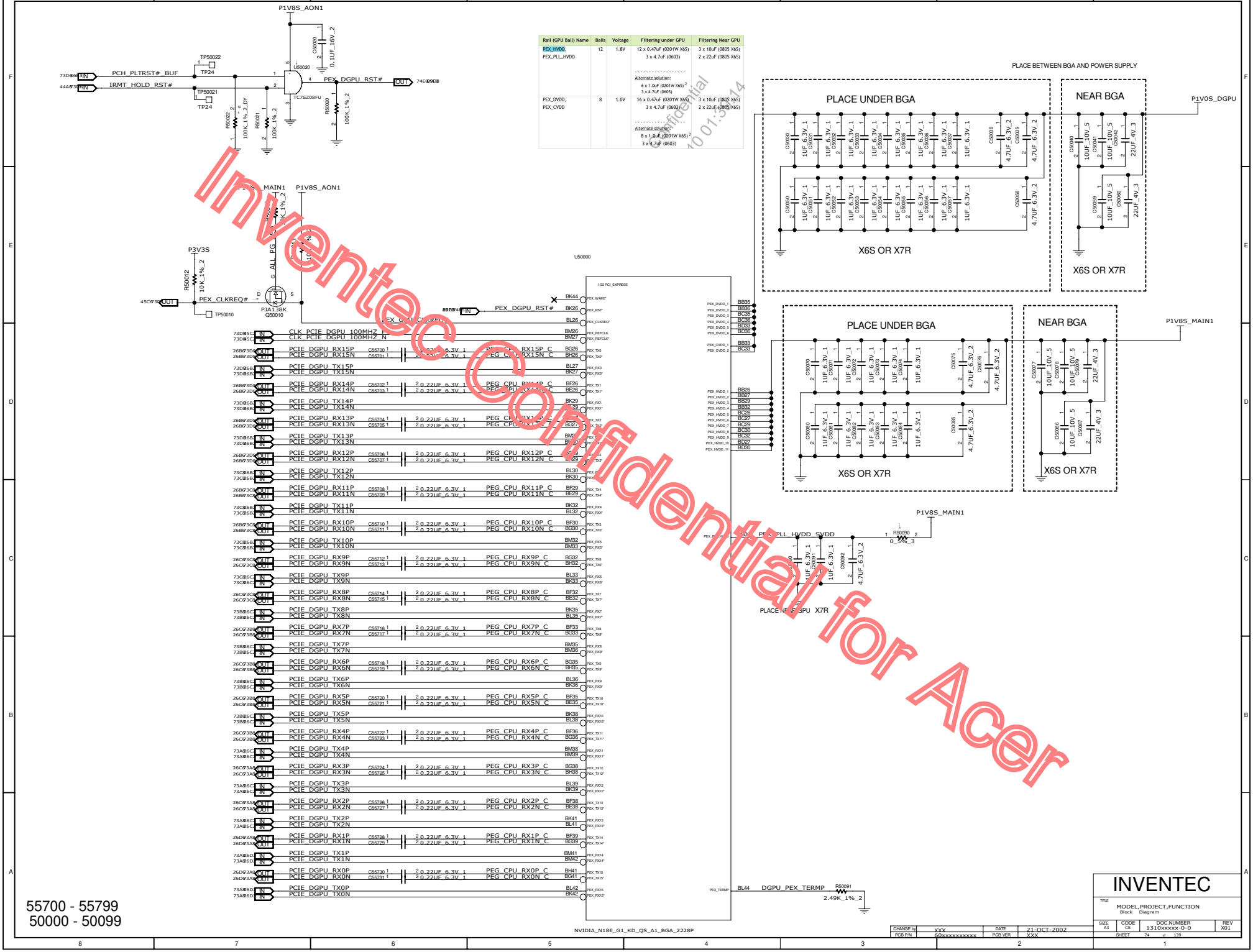

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD, PEX_PLL_HVDD	12	1.8V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603) Alternate solution: 6 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
PEX_DVDD, PEX_CVDD	8	1.0V	16 x 0.47uF (0201W X6S) 3 x 4.7uF (0603) Alternate solution: 8 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)

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PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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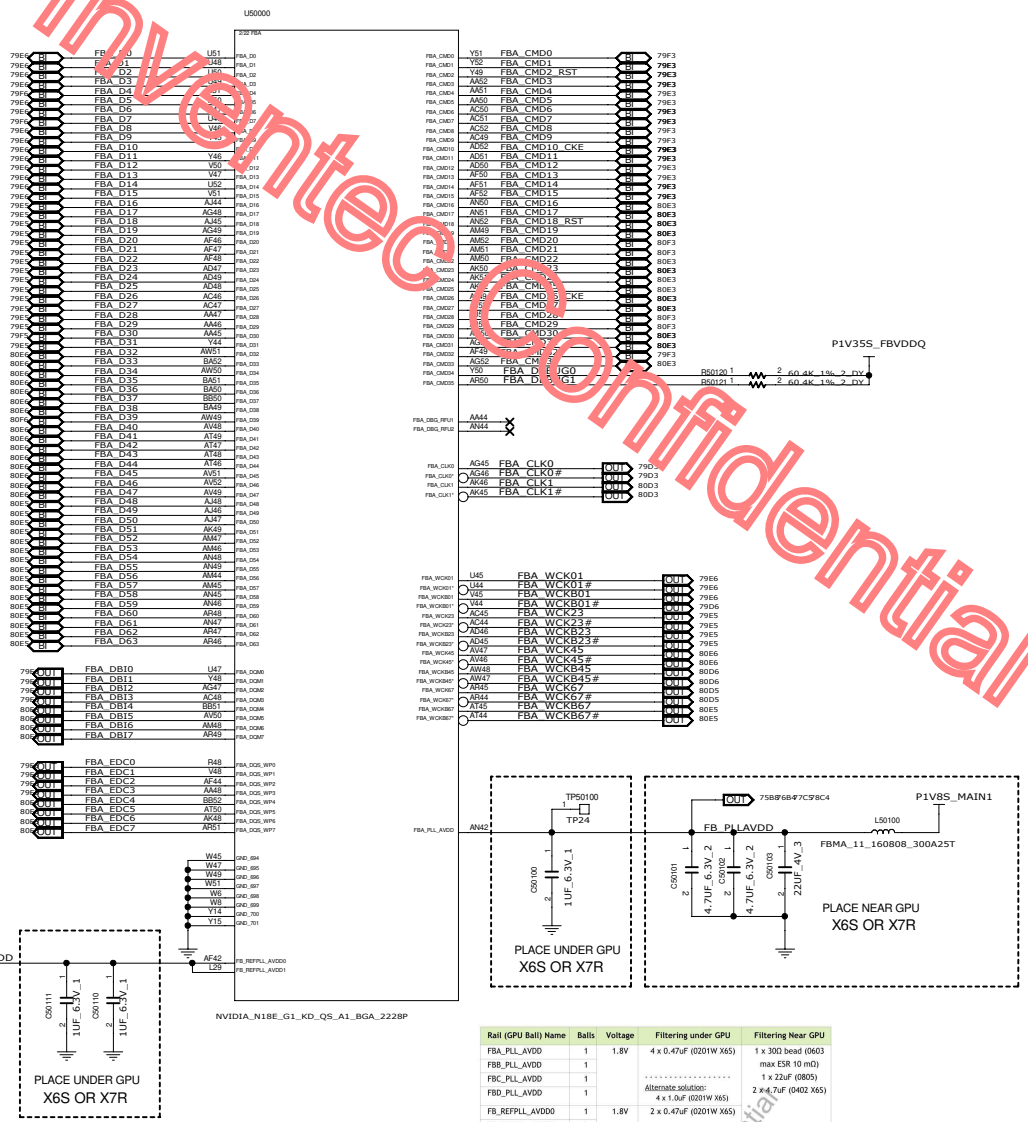
GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ) 1 x 22uF (0805) 2 x 4.7uF (0402 X6S)
FBB_PLL_AVDD	1			
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - - -	
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		- - - - - - - - - - - - - - - - - -	
			Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ) 1 x 22uF (0805) 2 x 4.7uF (0402 X6S)
FBB_PLL_AVDD	1			
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - - -	
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		- - - - - - - - - - - - - - - - - -	
			Alternate solution: 2 x 1.0uF (0201W X6S)	

50100 - 50199

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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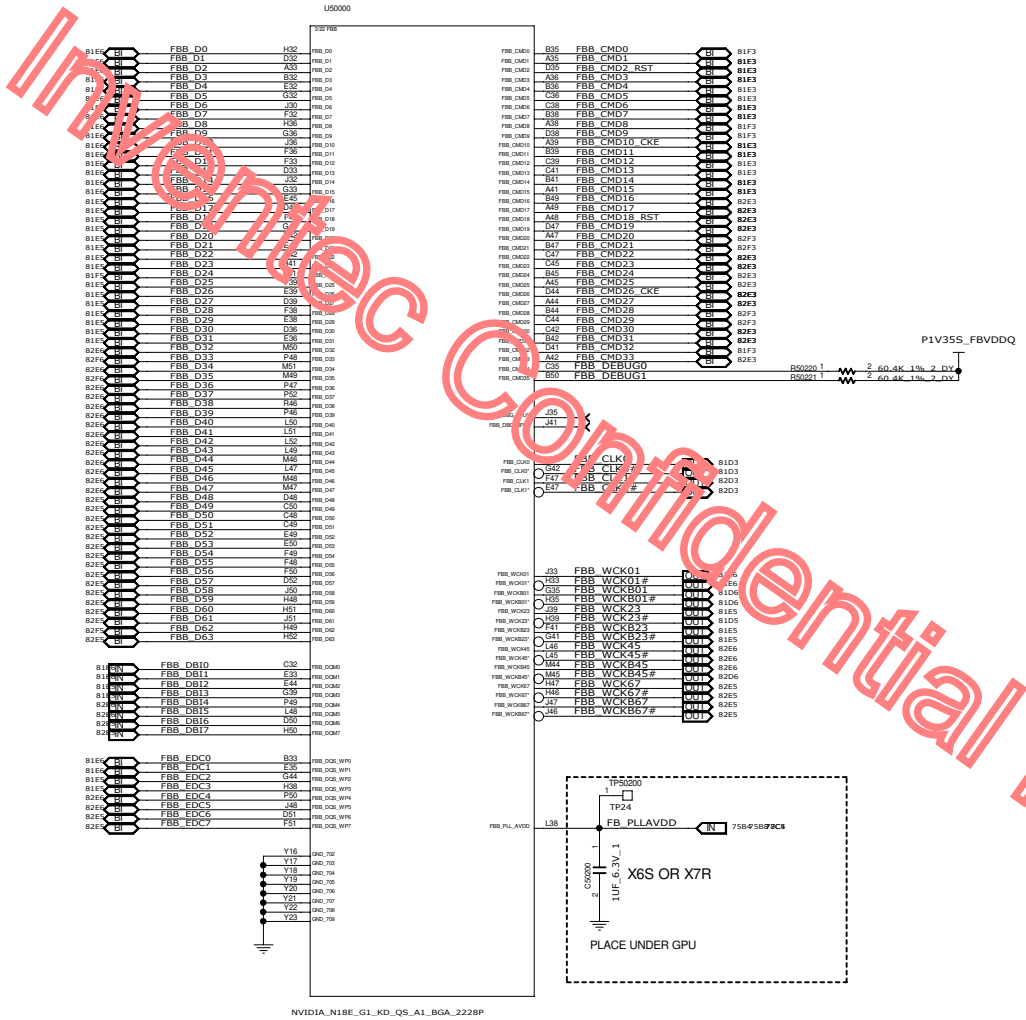
GPU FRAME BUFFER B



50200 - 50299

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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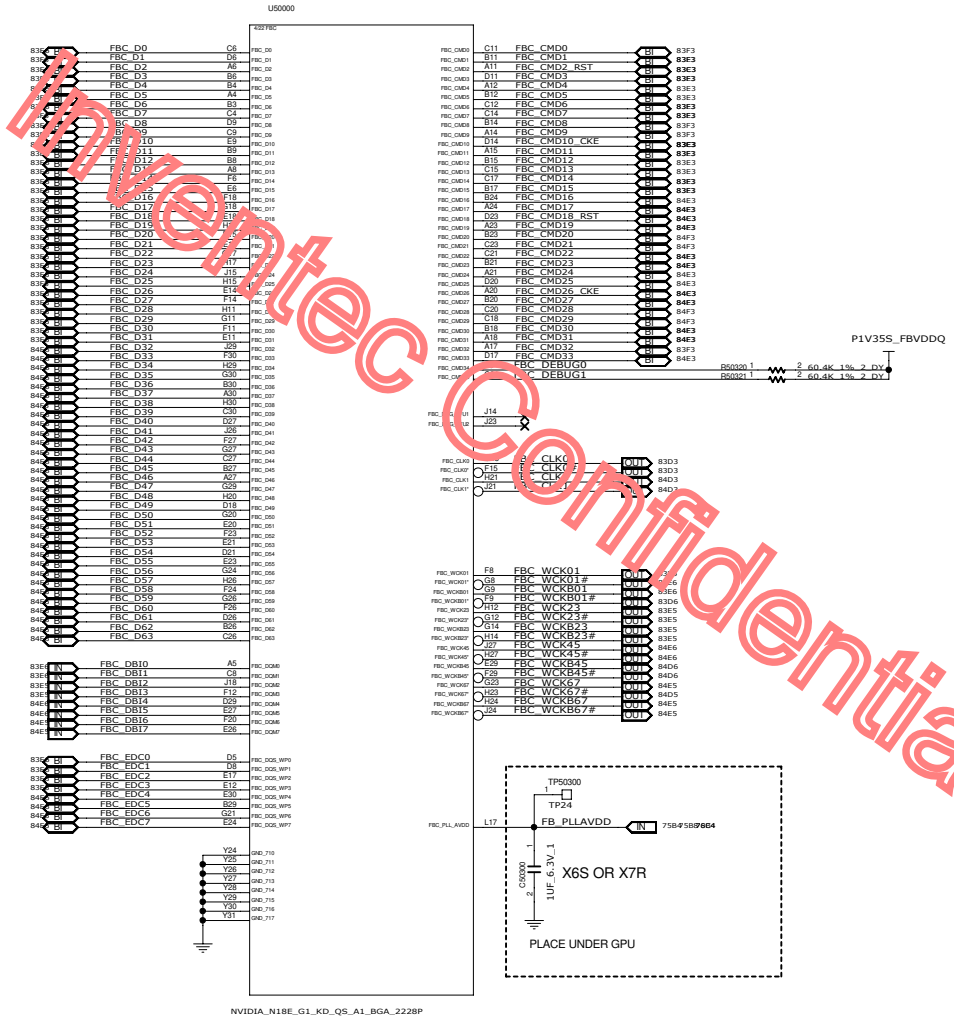
GPU FRAME BUFFER C



50300 - 50399

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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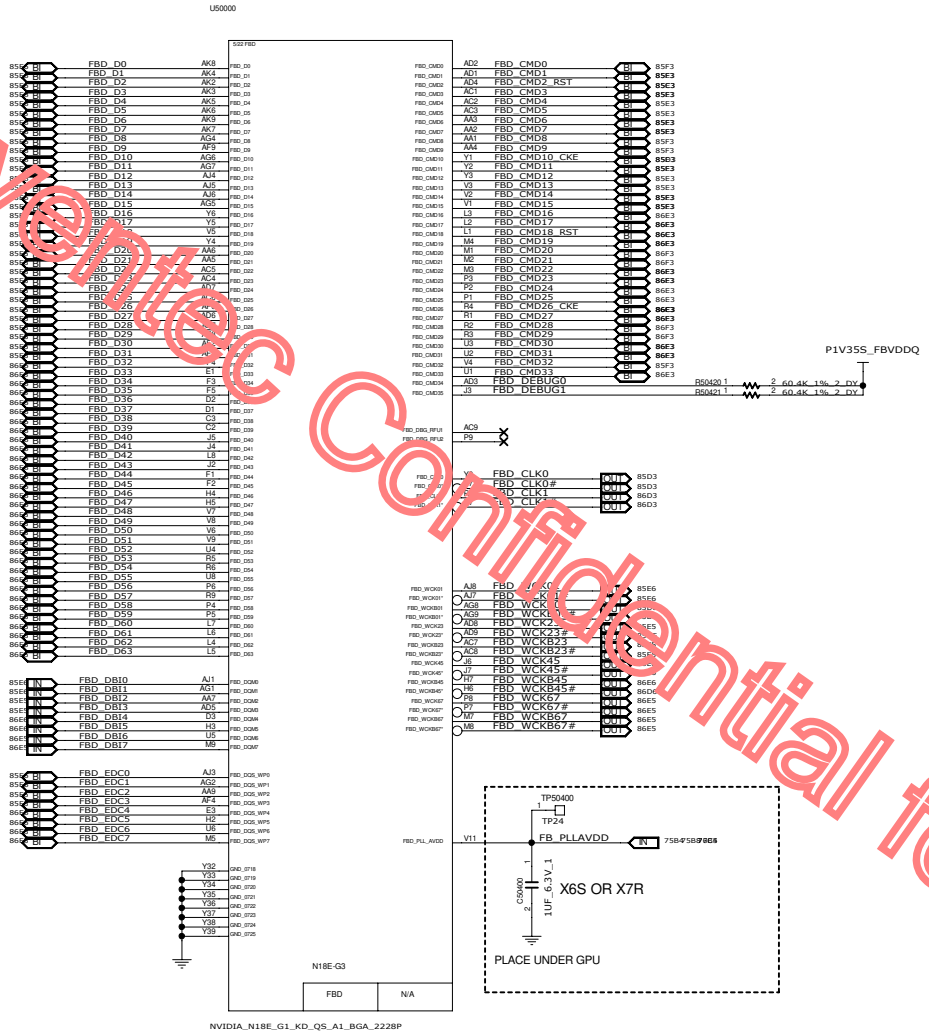
GPU FRAME BUFFER D



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A3	CS	1310xxxxx-0-0	X01

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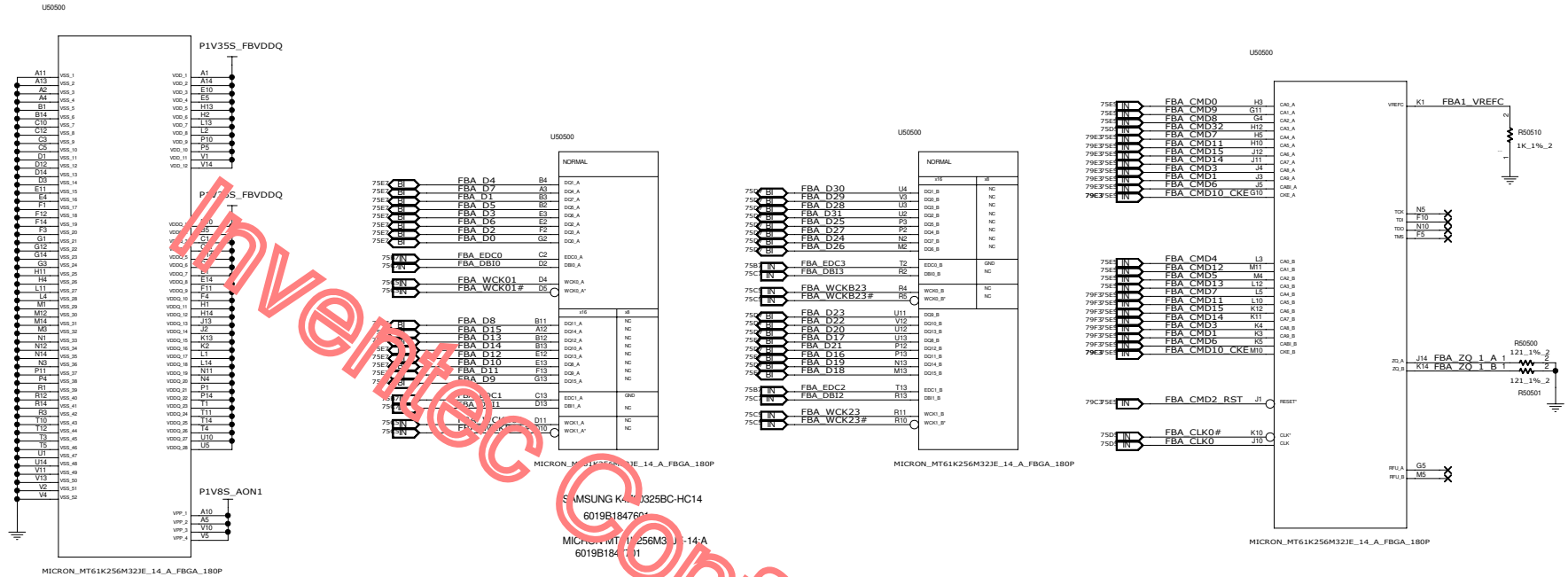

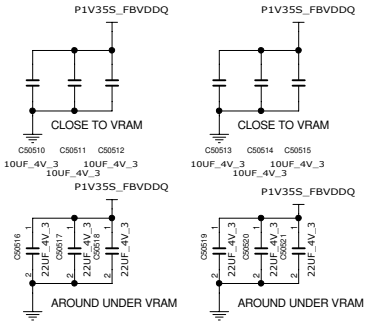

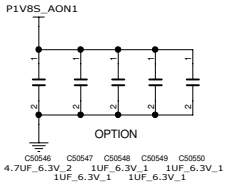

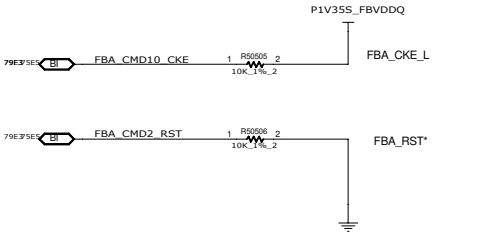

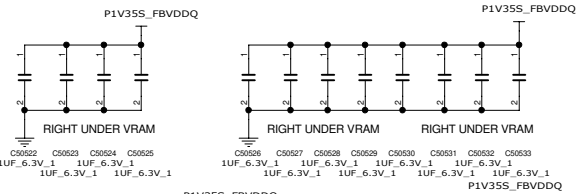

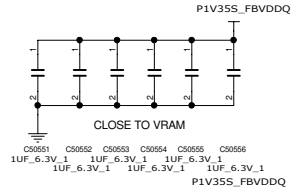

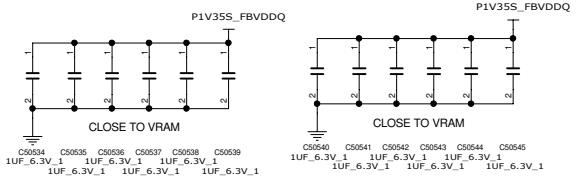

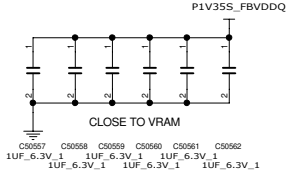

Table 8-[illegible] DRAM-Side Decoupling

[illegible] Capacitors		Recommended Quantity and Placement (per DRAM device)	
	Type, [Size NOTE 1]	Quantity	Placement
VDD/[illegible] Rail			
0.47 uF [illegible]	X6S [020[illegible]	36	Under or very close to DRAM
10 [illegible]	X6S [0603]		
10 uF	[illegible]	2	Around DRAM
22 uF	X6S [06[illegible]		
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	[illegible]	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

NOTE 1: NVIDIA reference designs use and recommend 0201 or 0201W capacitors where needed. PCB design teams should ensure that component placement equipment can support the smaller package size.

NOTE 2: Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0 uF (X6S, 0201W).

NOTE 3: Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 4 capacitors of value 1.0 uF (X6S, 0201W), one per VPP ball.

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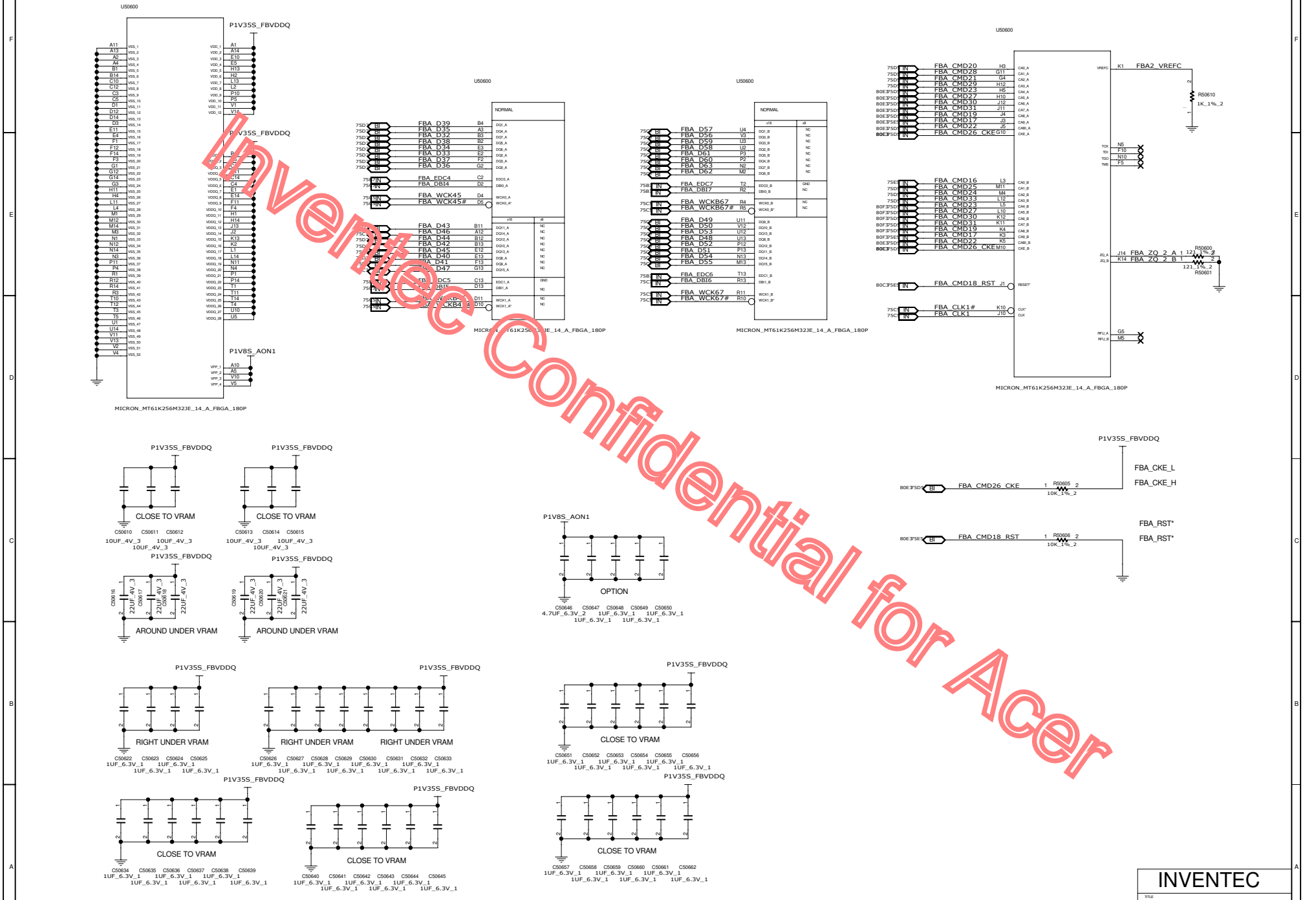

50600 - 50699

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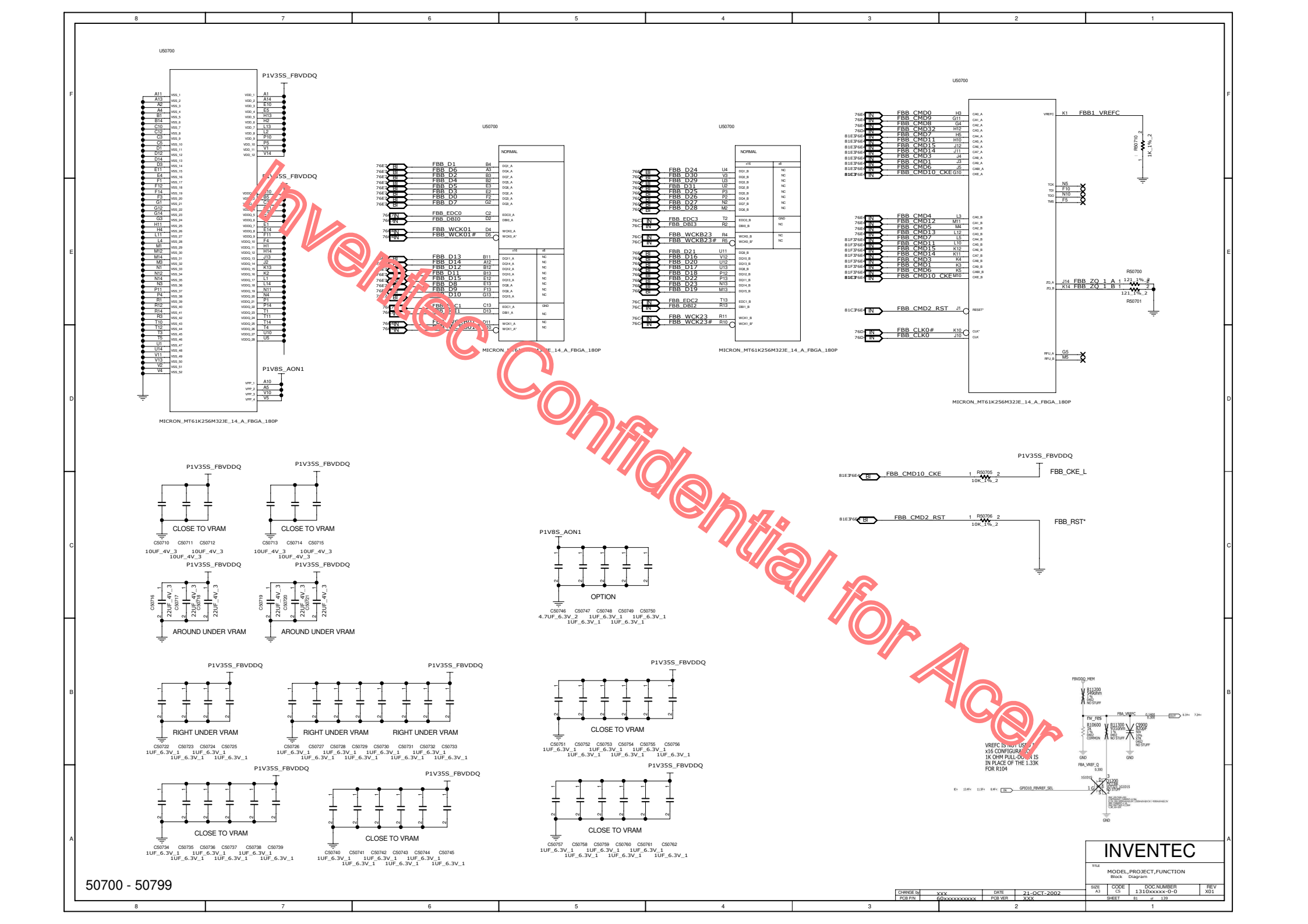

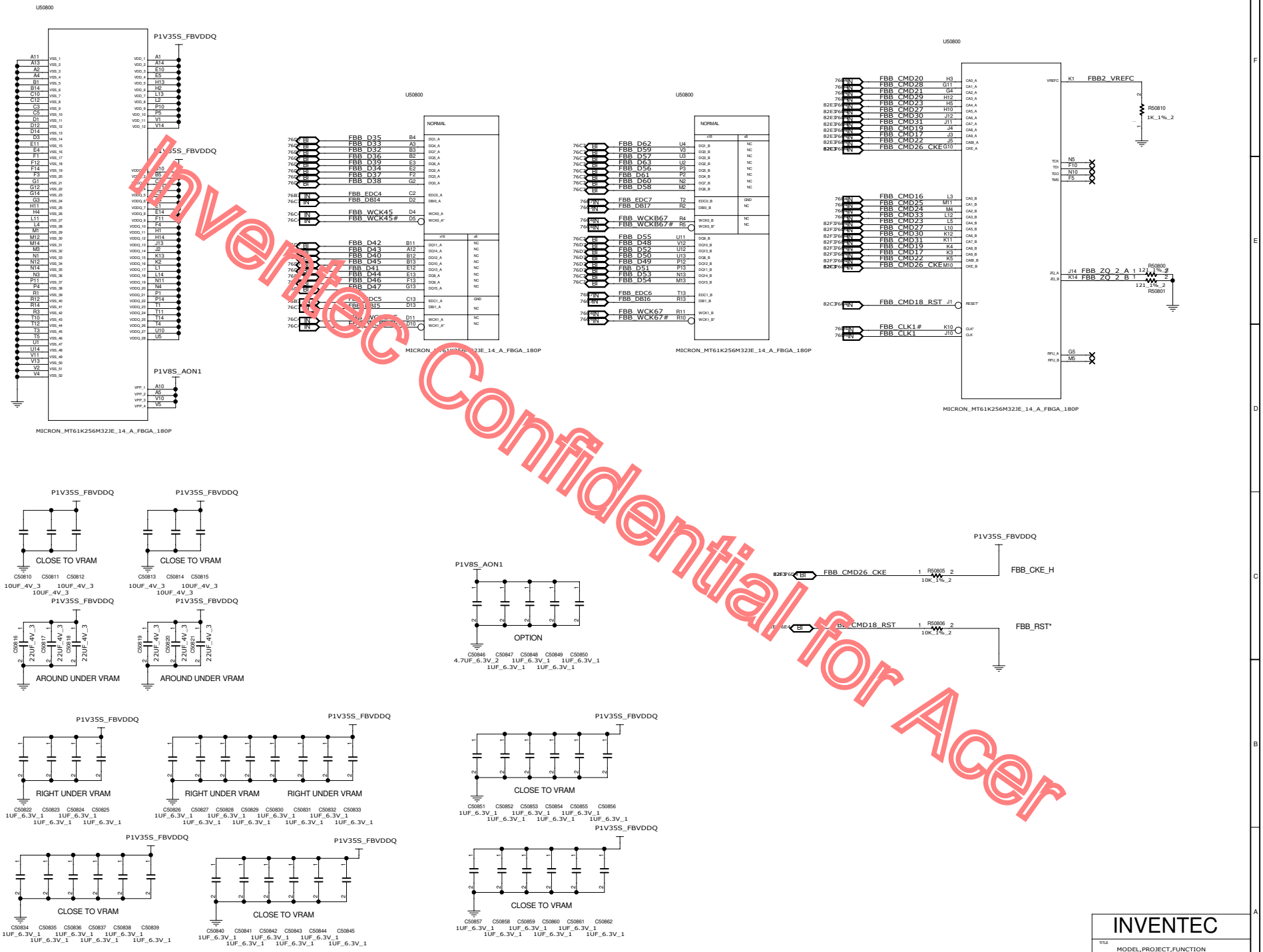

50800 - 50899

CHANGE by	XXX	DATE	21-OCT-2002		
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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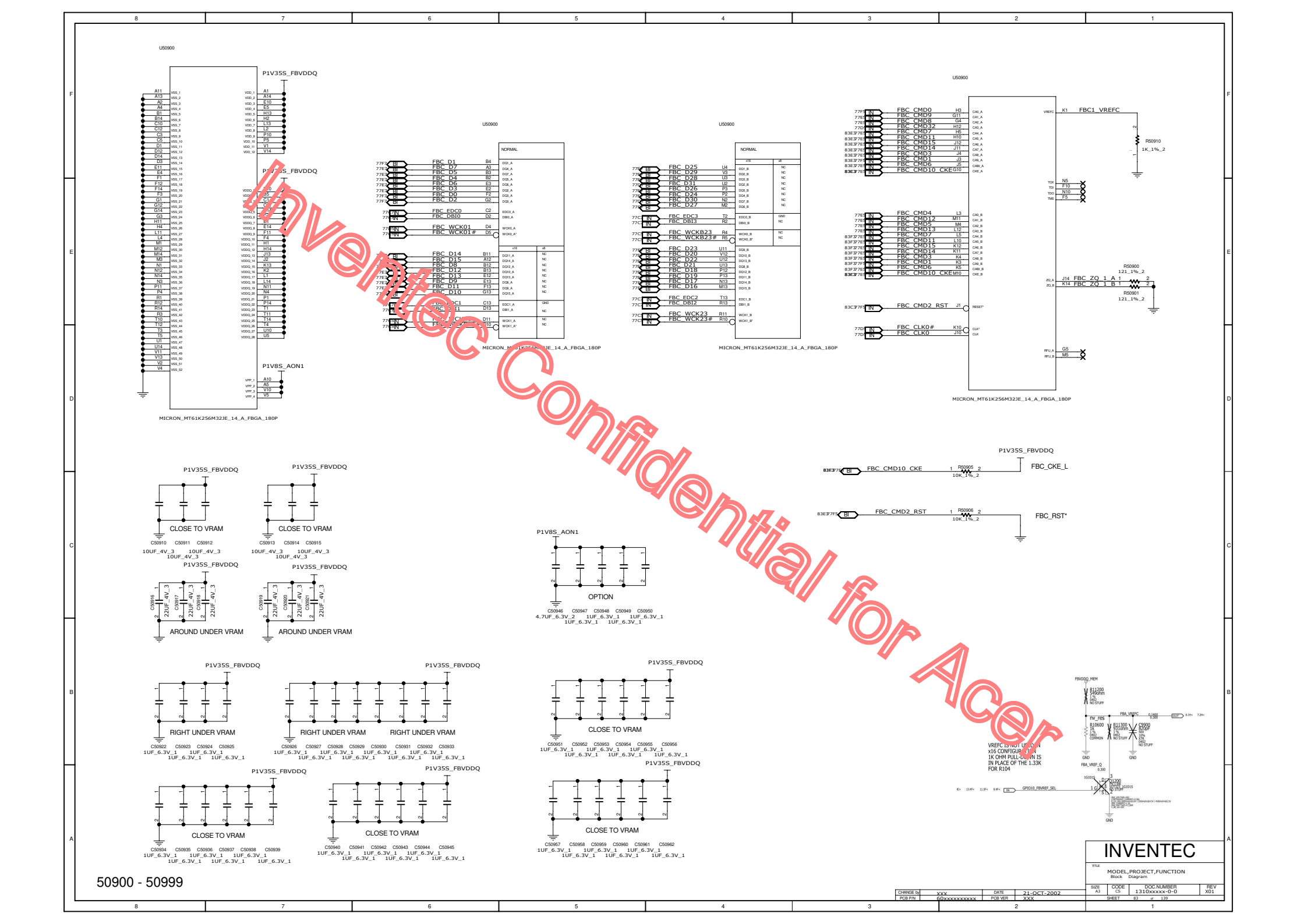

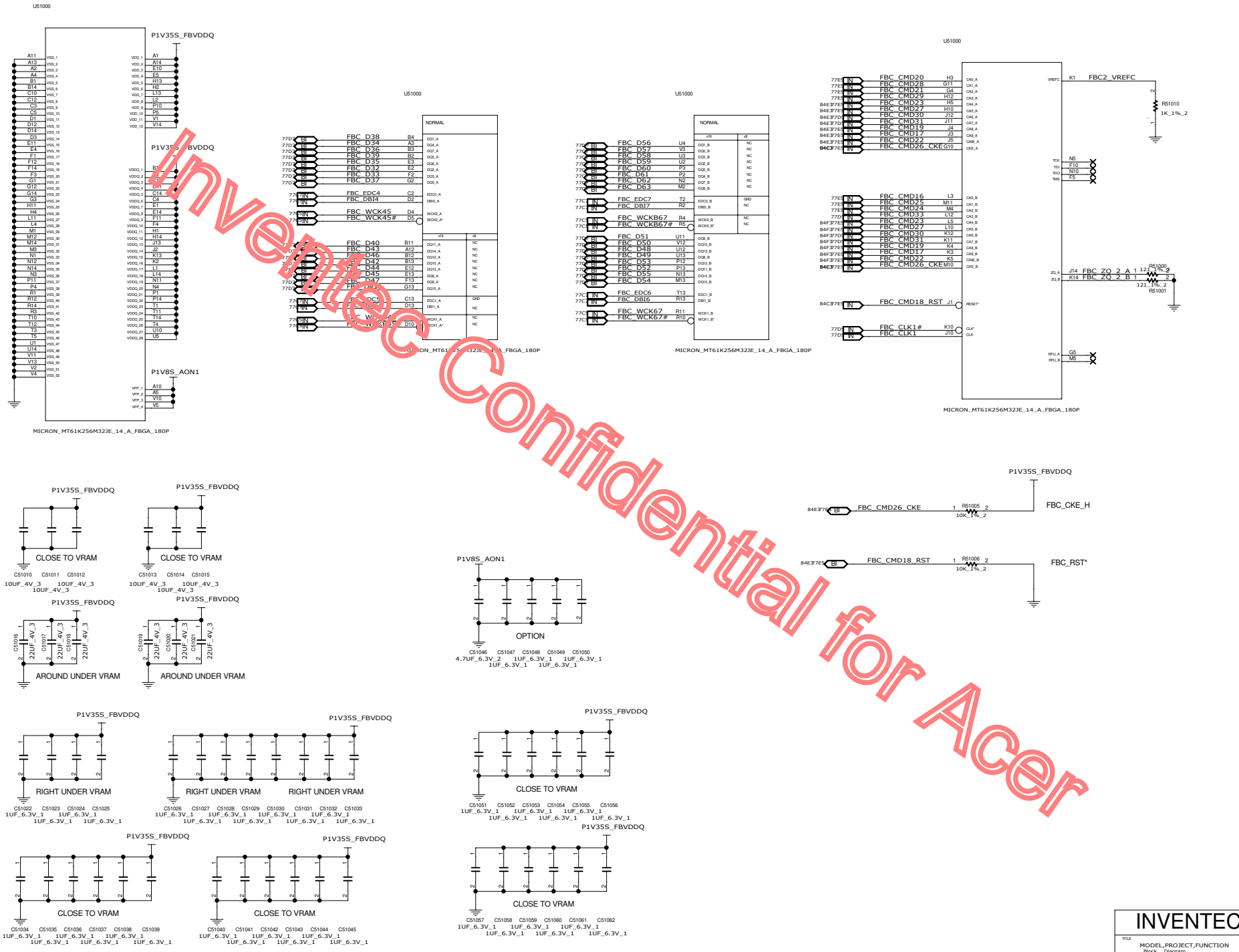

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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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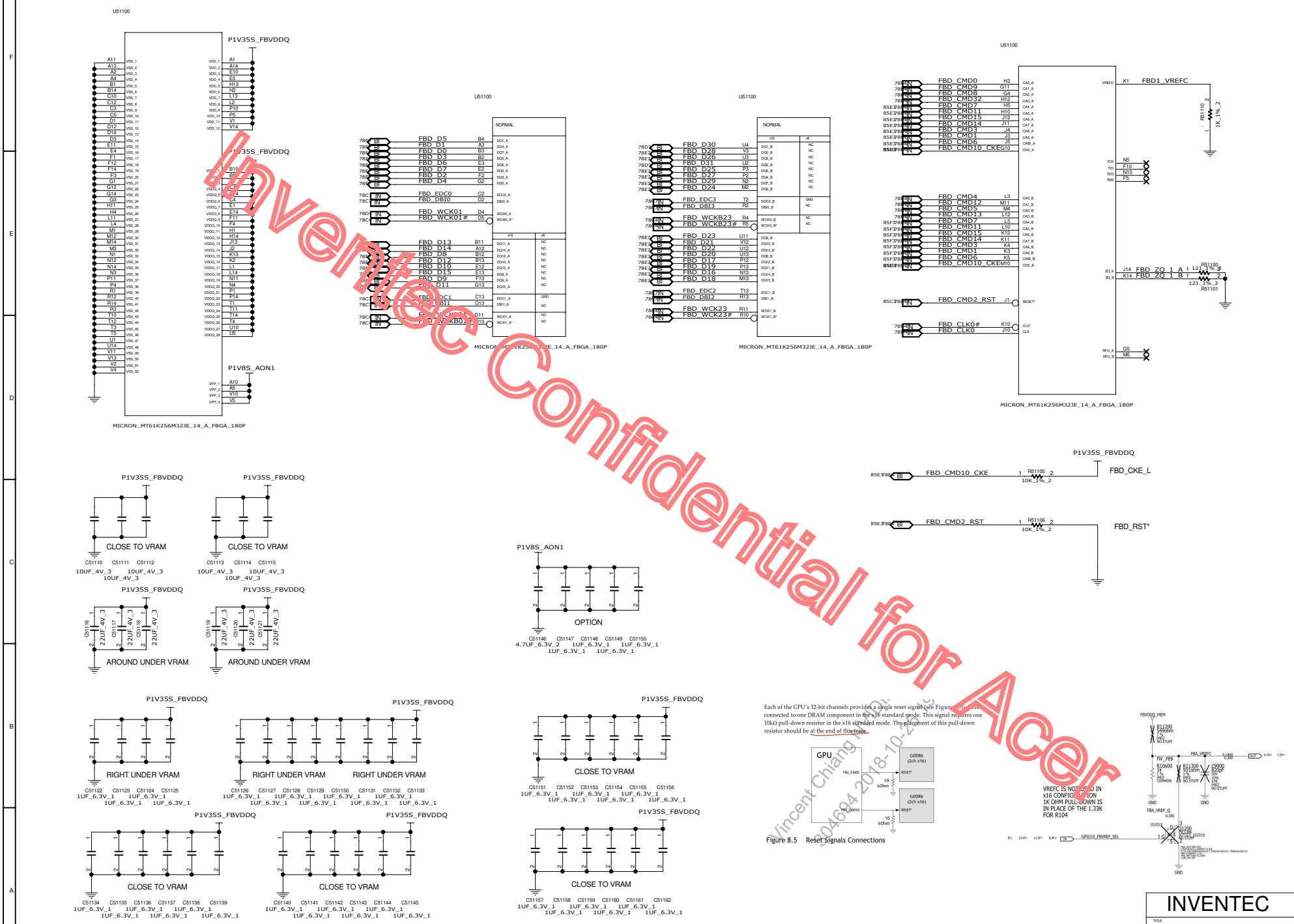
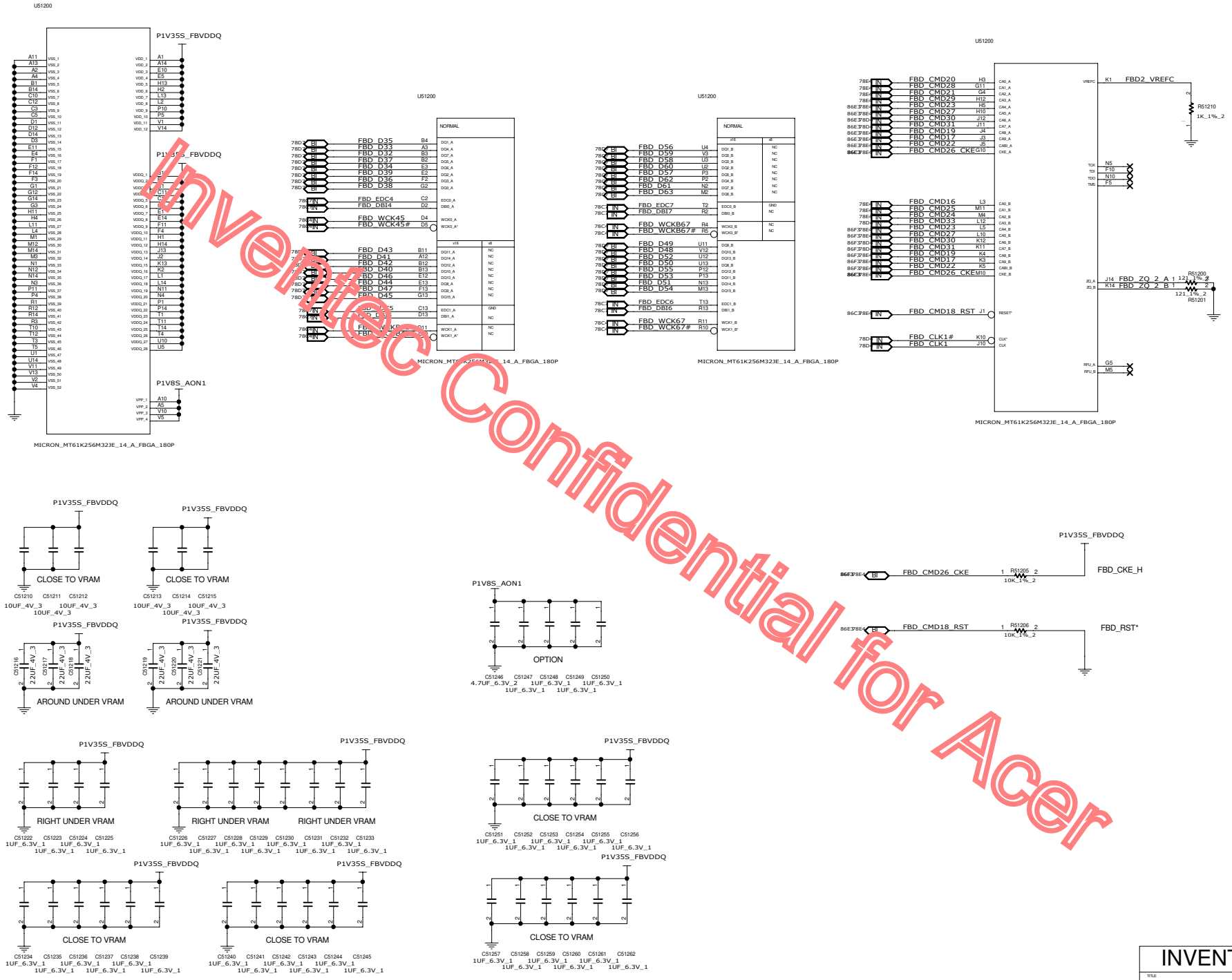
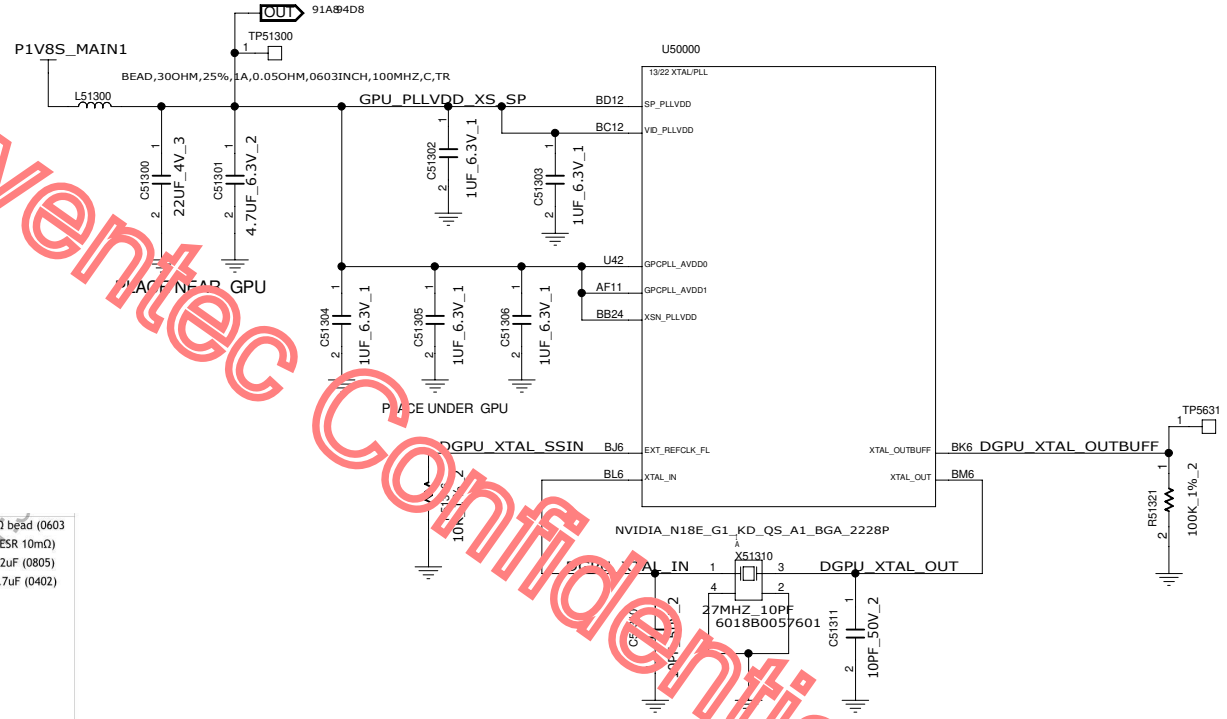




27 MHZ XTAL



CL=2*10-(5+3)=12

CL_trim = 2 × CLoad - (Cstray + Ci)

Where:

- C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} is ~ 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S)	1 x 300 bead (0603 max ESR 10mΩ)
IFPCD_PLLVDD	1			1 x 22uF (0805)
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X6S)	1 x 4.7uF (0402)
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S) Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1.0uF (0201W X6S)	

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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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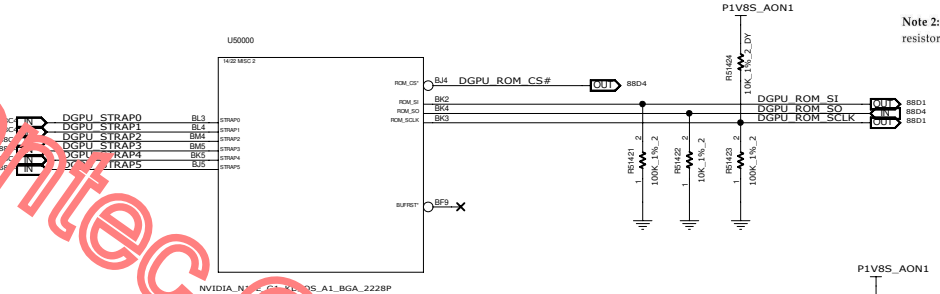
GPU VBIOS, EXTERNAL STRAPS

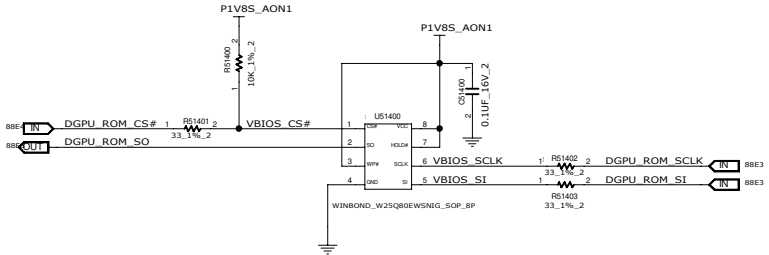
Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.





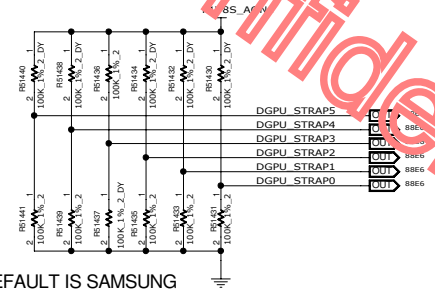


Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M	Reserved			
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	H				
M	H	M				
H	M	M				
M	M	M				

DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG:R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
MICRON :R51430 STUFF
R51431 NOT STUFF

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDI/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[1]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

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SIZE	CODE	DOC.NUMBER	REV
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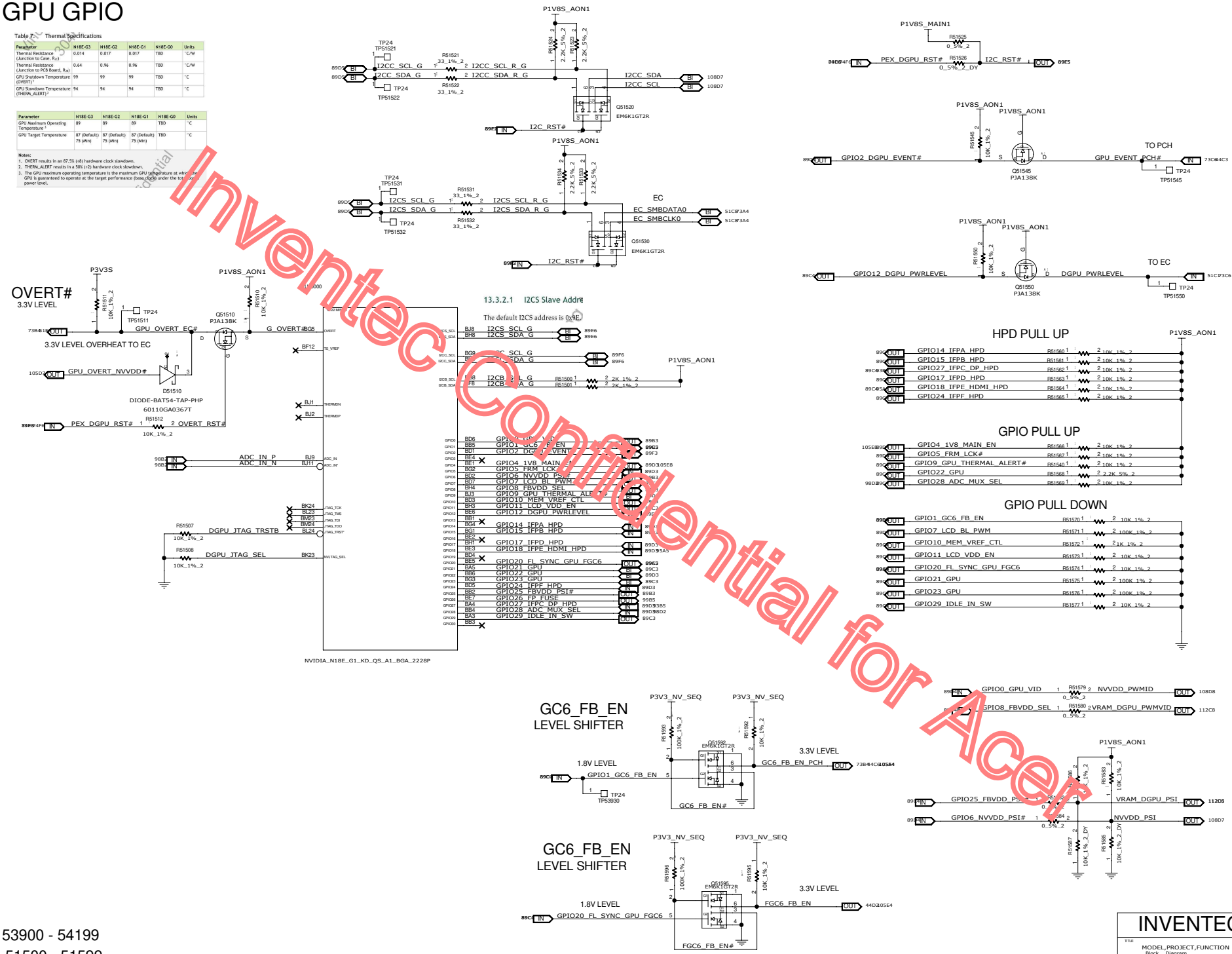
GPU GPIO

Table 7 Thermal Specifications

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, $R_{\theta JC}$)	0.014	0.017	0.017	TBD	°C/W
Thermal Resistance (Junction to PCB Board, $R_{\theta JB}$)	0.64	0.96	0.96	TBD	°C/W
GPU Shutdown Temperature (OVERT)[1]	99	99	99	TBD	°C
GPU Slowdown Temperature (THERM_ALERT)[2]	94	94	94	TBD	°C

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature[3]	89	89	89	TBD	°C
GPU Target Temperature	87 (Default) 75 (Min)	87 (Default) 75 (Min)	87 (Default) 75 (Min)	TBD	°C

Notes:
1. OVERT results in an 87.5% (-8) hardware clock slowdown.
2. THERM_ALERT results in a 50% (-2) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clock) under the total power level.



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51500 - 51599

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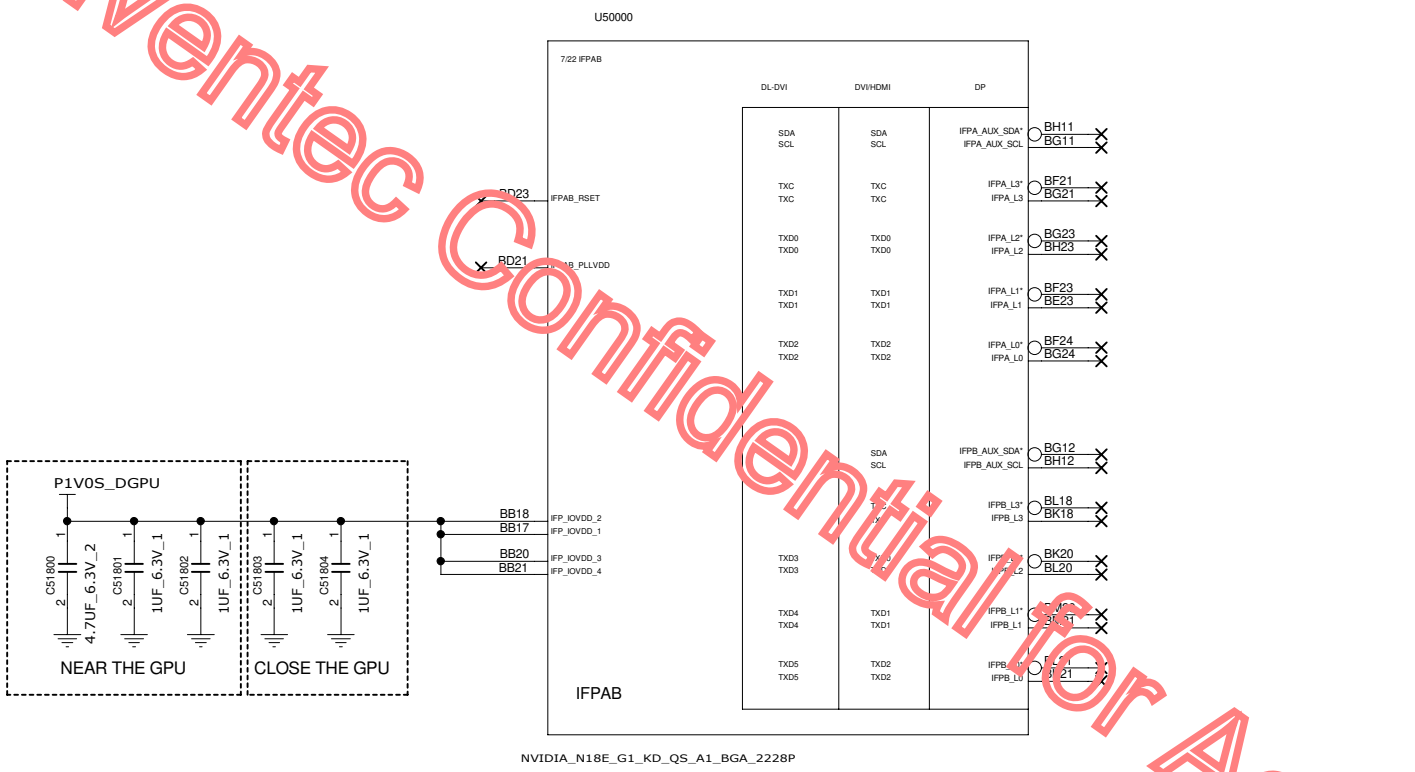

51800 - 51899

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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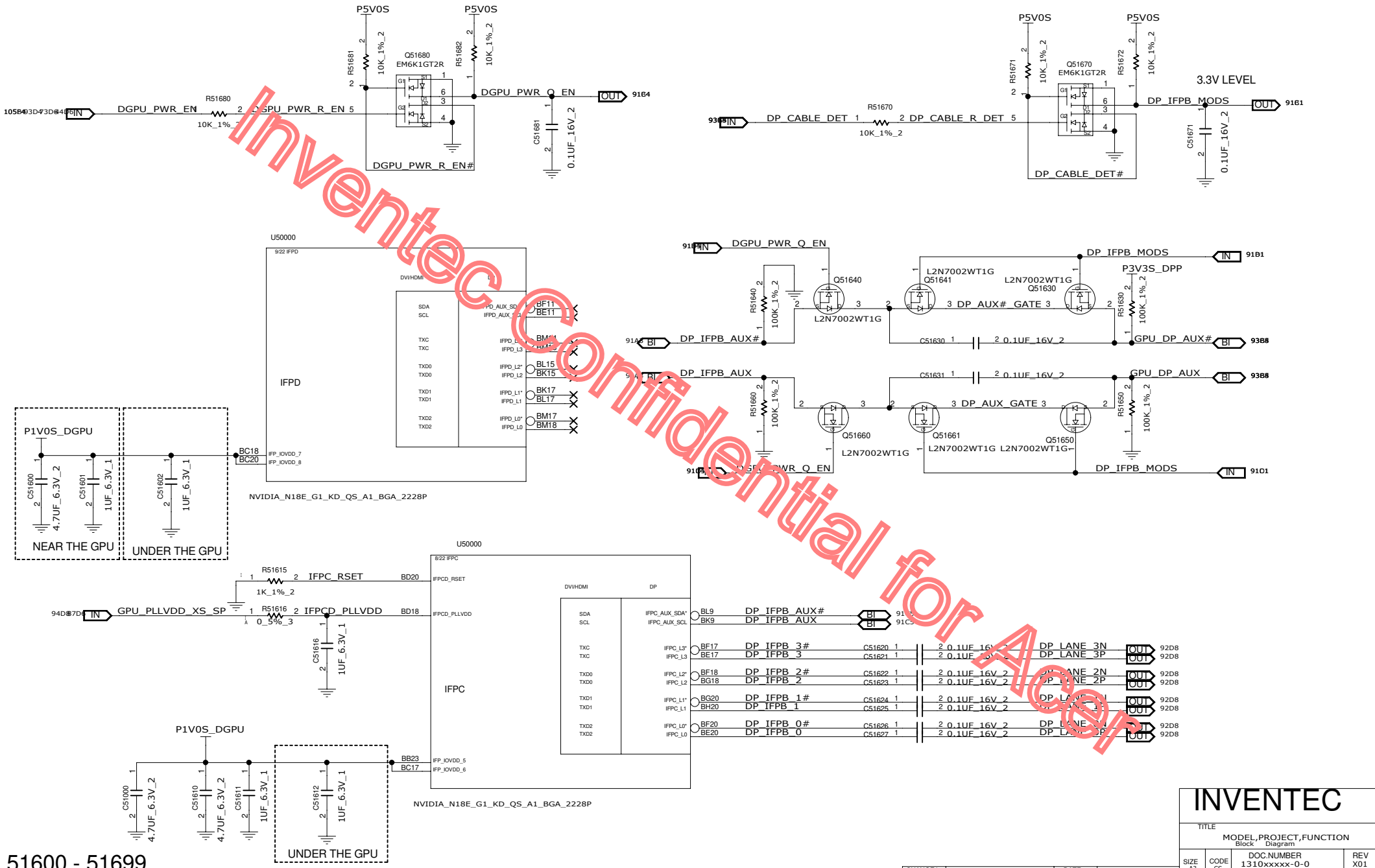

51600 - 51699

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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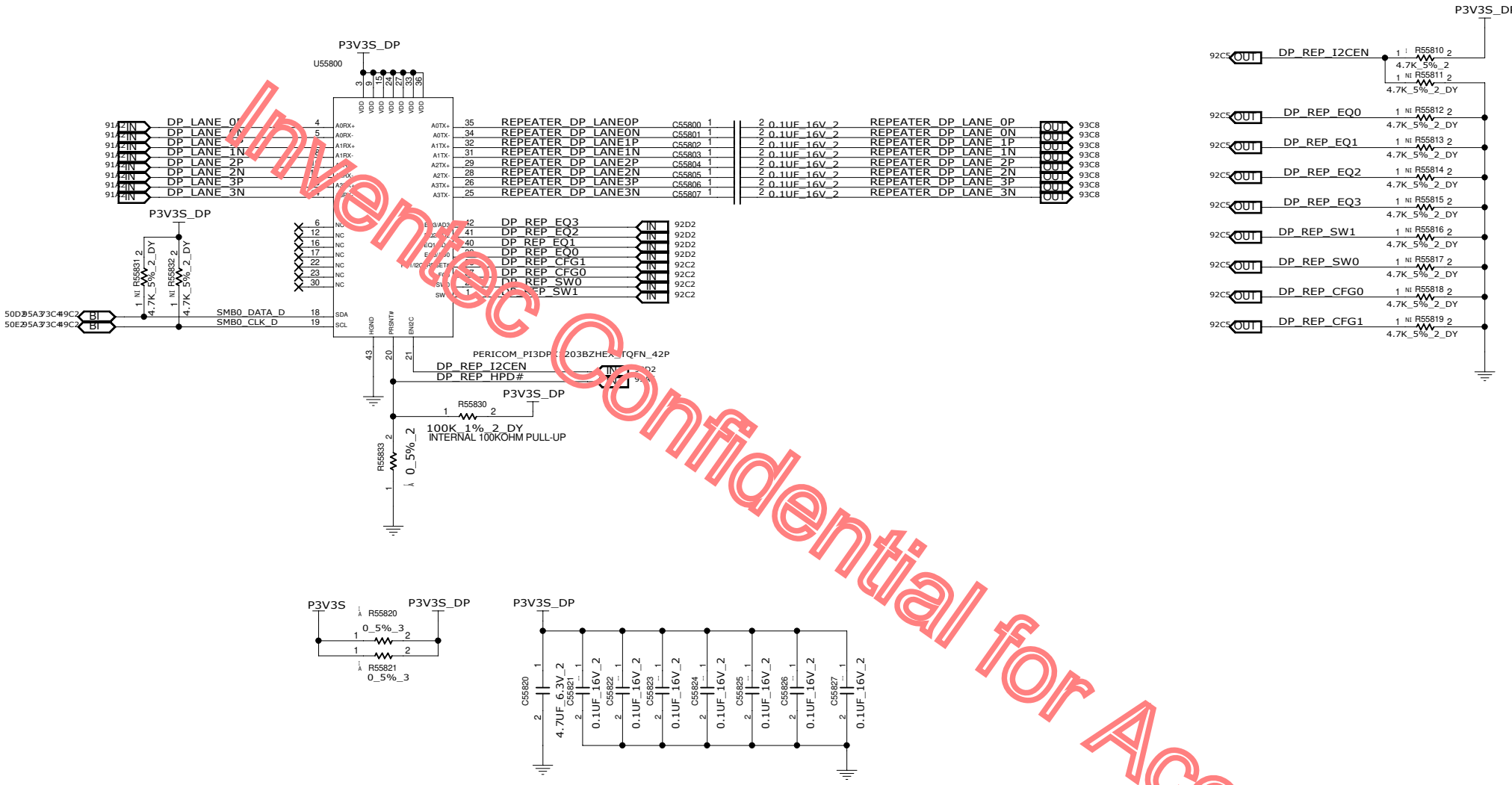
DP REDRIVER



55800 - 55999 56000 - 56199

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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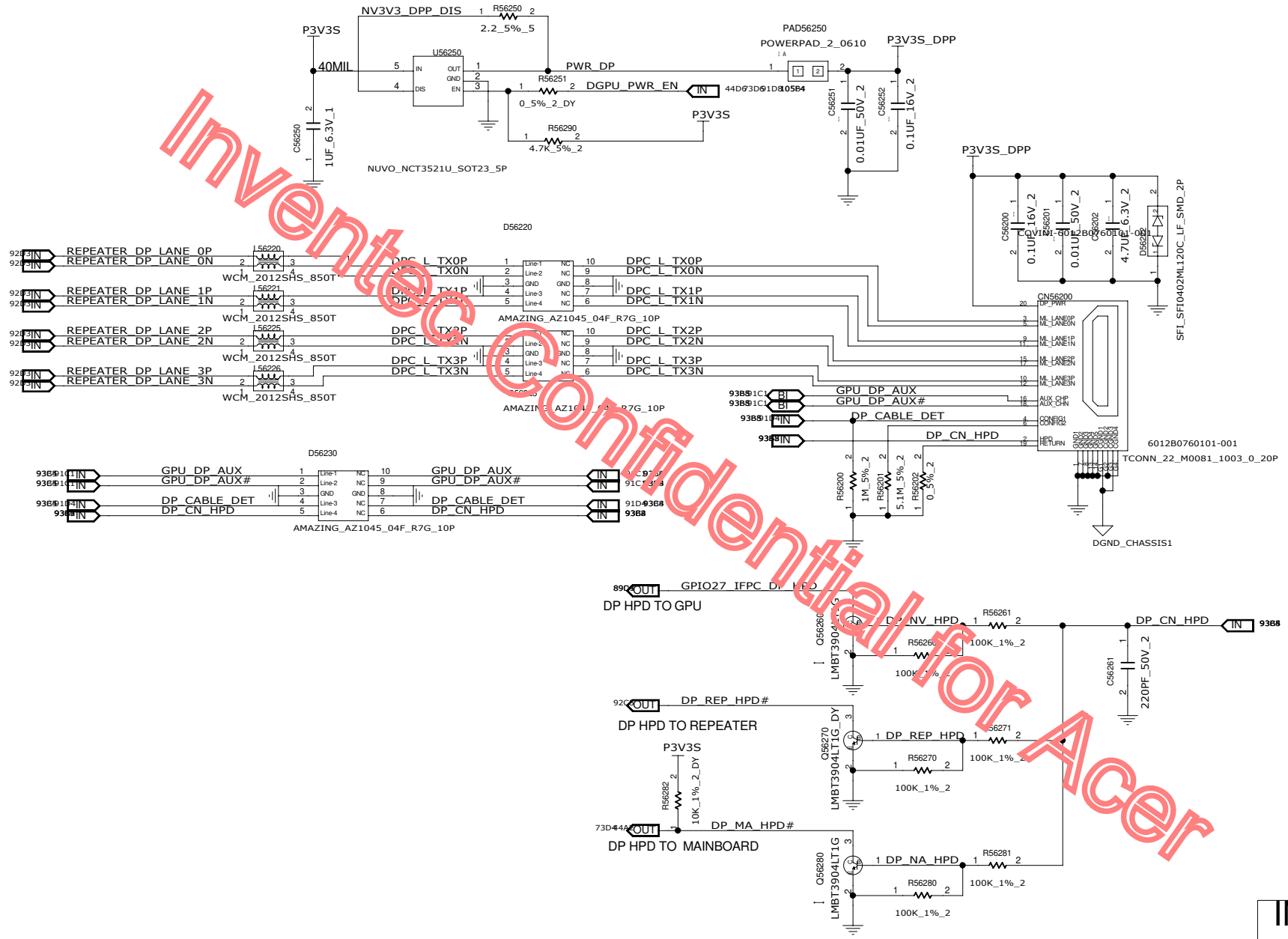

56200 - 56399

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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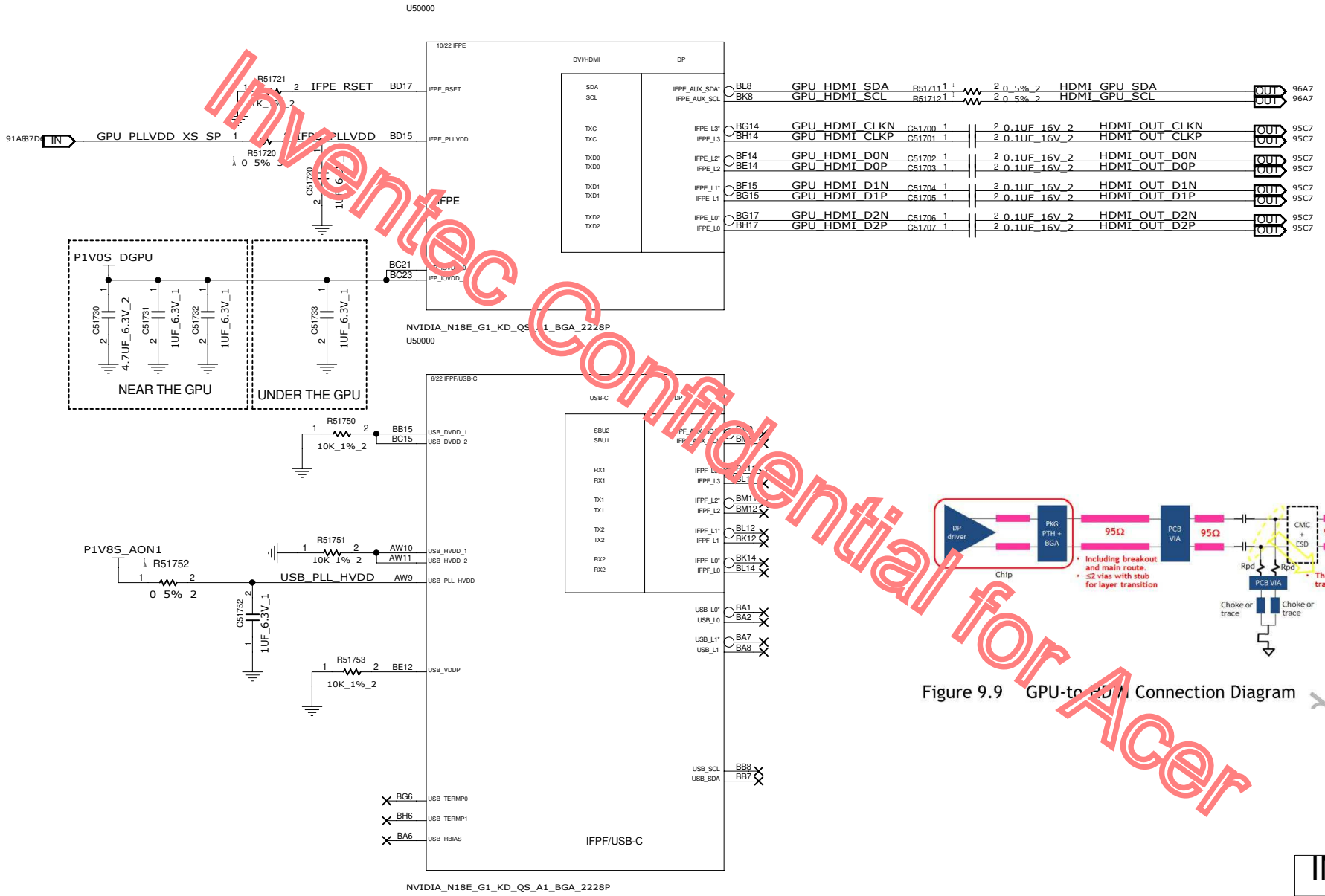

Figure 9.9 GPU-to-PD/HDMI Connection Diagram

51700 - 51799

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A3	CS	1310xxxxx-0-0	X01

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HDMI 2.0 RETIMER

ITE_IT66317FN_BW_0006_R_QFN_48P

HDMI HPD TO MB

DP HPD TO GPU

TO MAINBOARD

Reserve for system control

Reserve for system control

While IT66317 power off, please drive GPIO1,2 to low.

Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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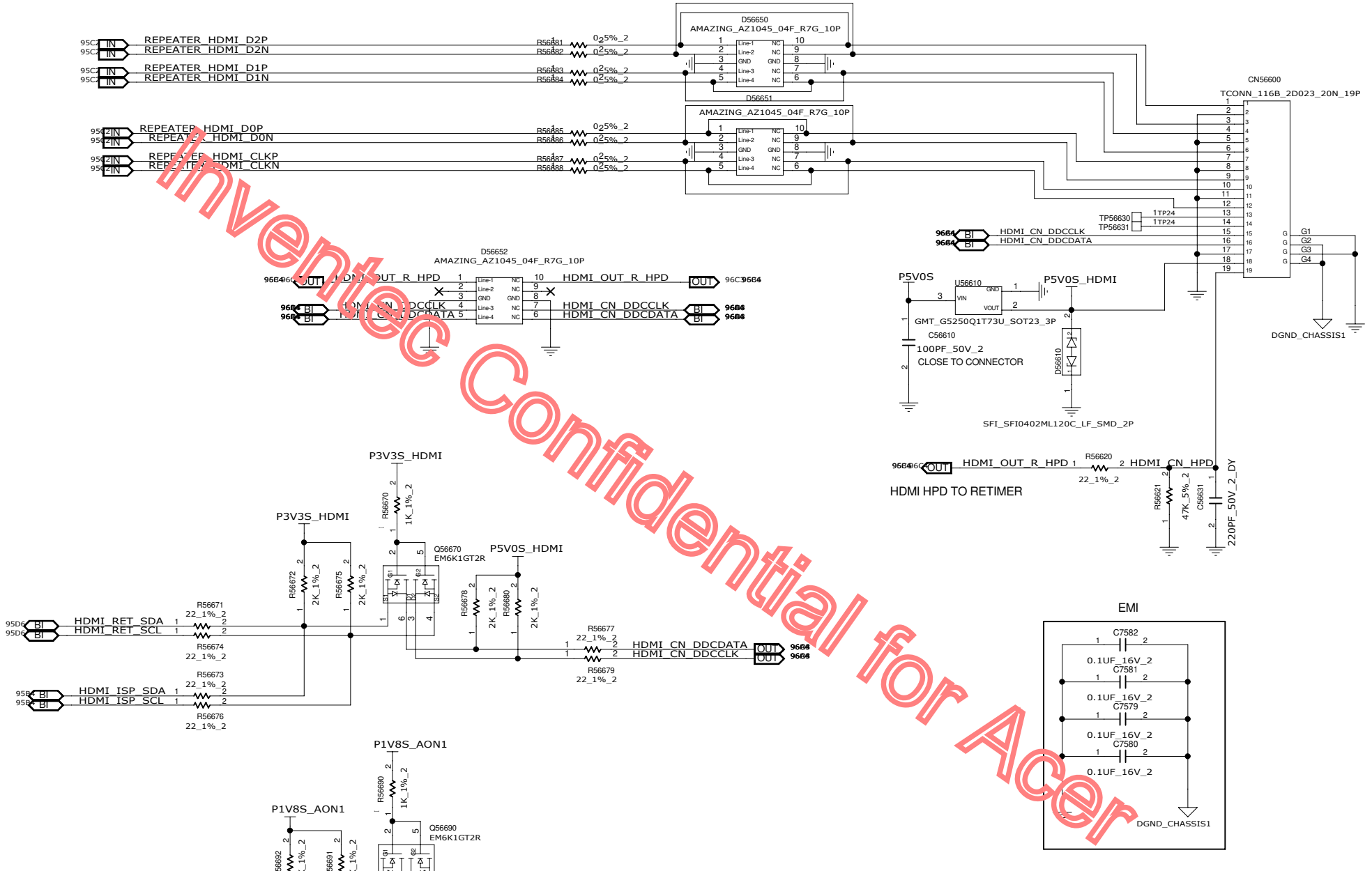
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



56600 - 56799

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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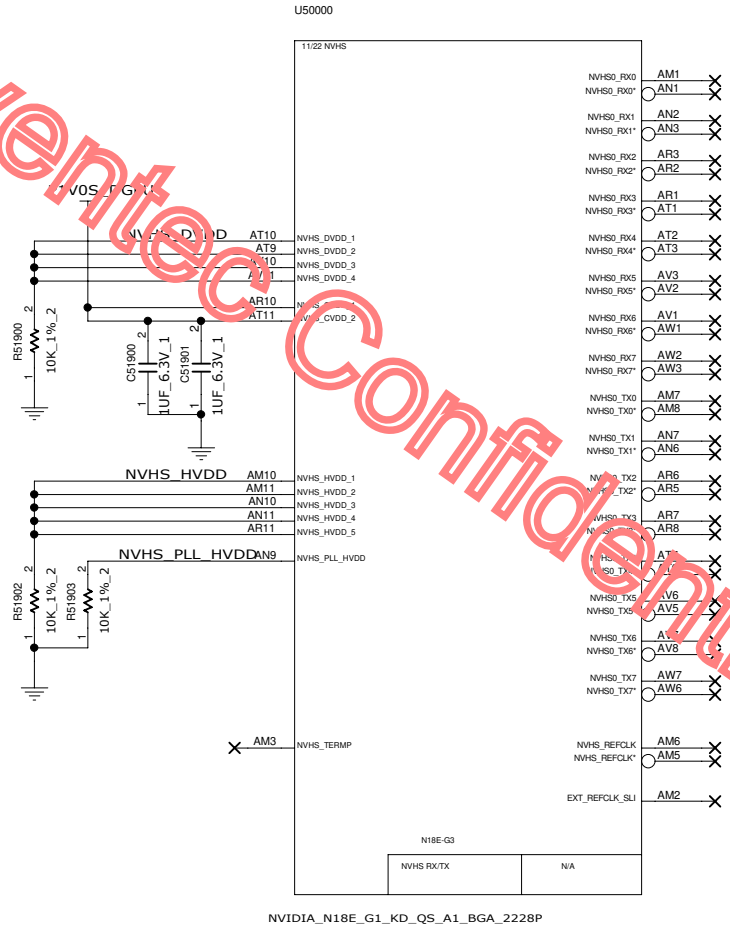

51900 - 51999

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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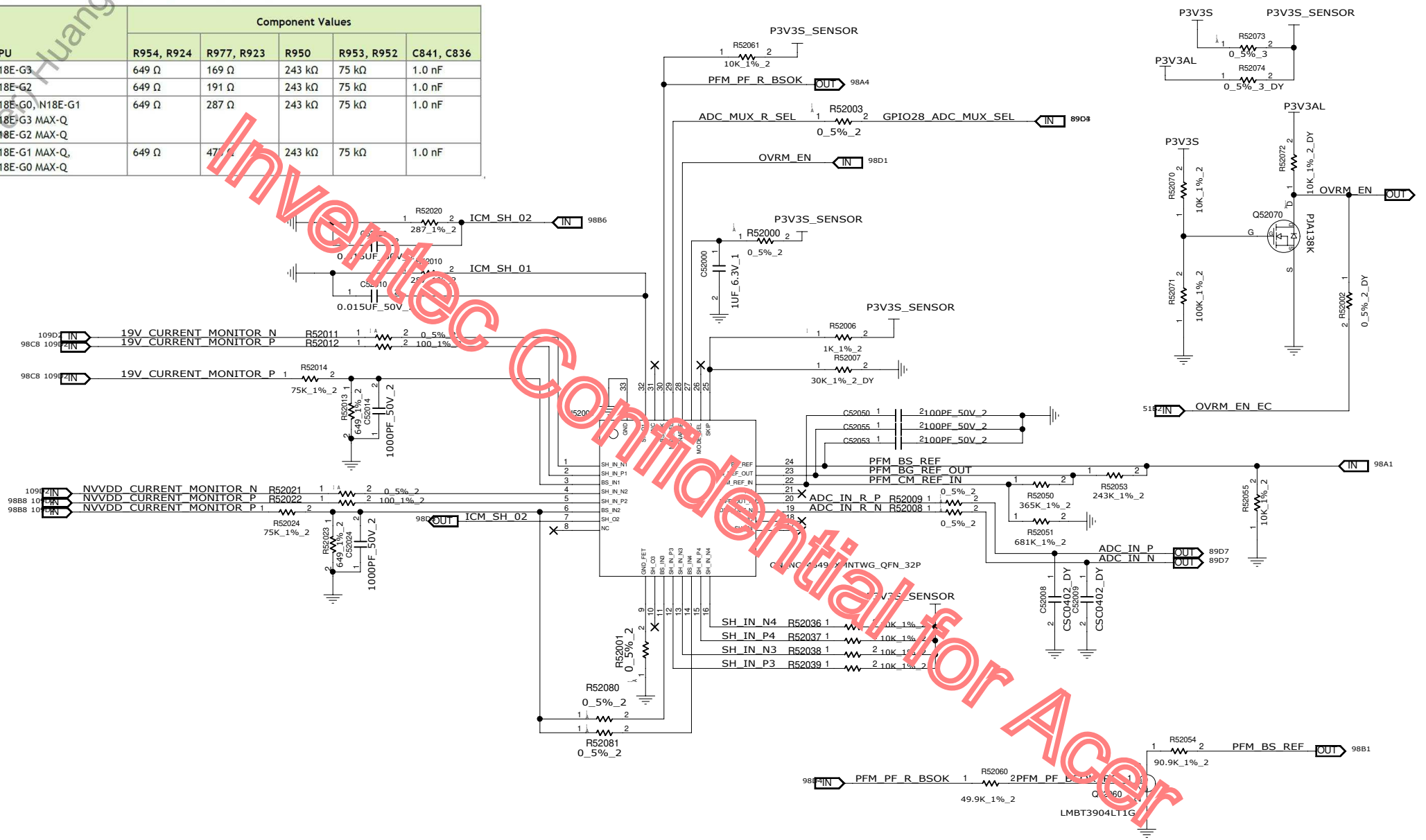
Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	47[illegible]	243 kΩ	75 kΩ	1.0 nF



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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION (Block Diagram)

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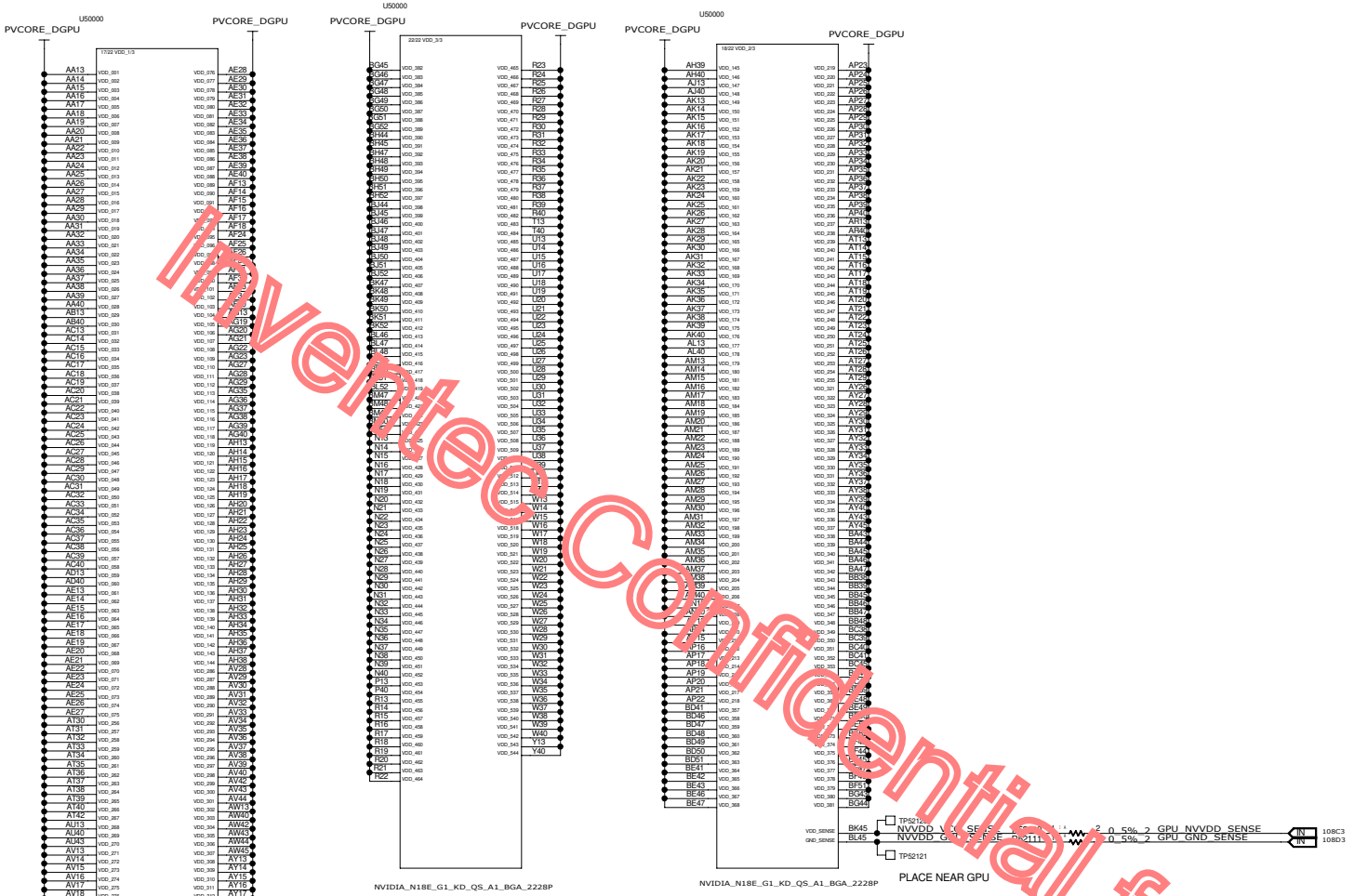


The required subcircuit is shown in detail in Figure 15.6.

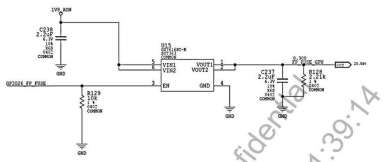
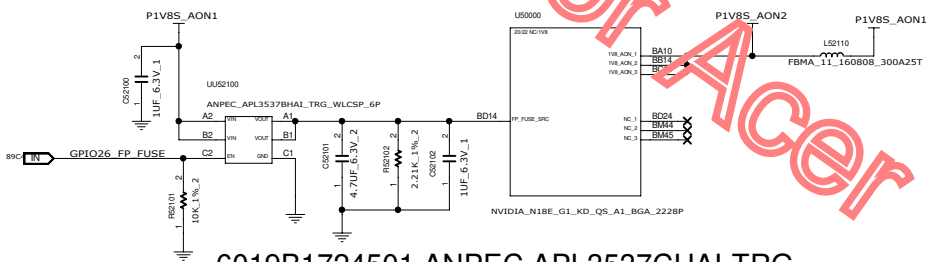


Figure 15.6 Subcircuit Schematic

In Figure 15.6, the component labeled "U15" is an active switch; devices equivalent to the GS76165C-R are acceptable as long as they meet the following requirements:

- The active switch must be capable of driving 100mA or more.
- The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100msec or less.
- There must be no glitch during power up or GC6/GC-OFF entry or exit.
- The FP_FUSE_GPU (output) trace width must be 0.25 mm (10 mil) or greater.



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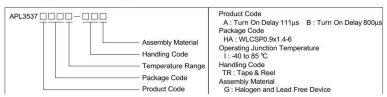

52100 - 52199

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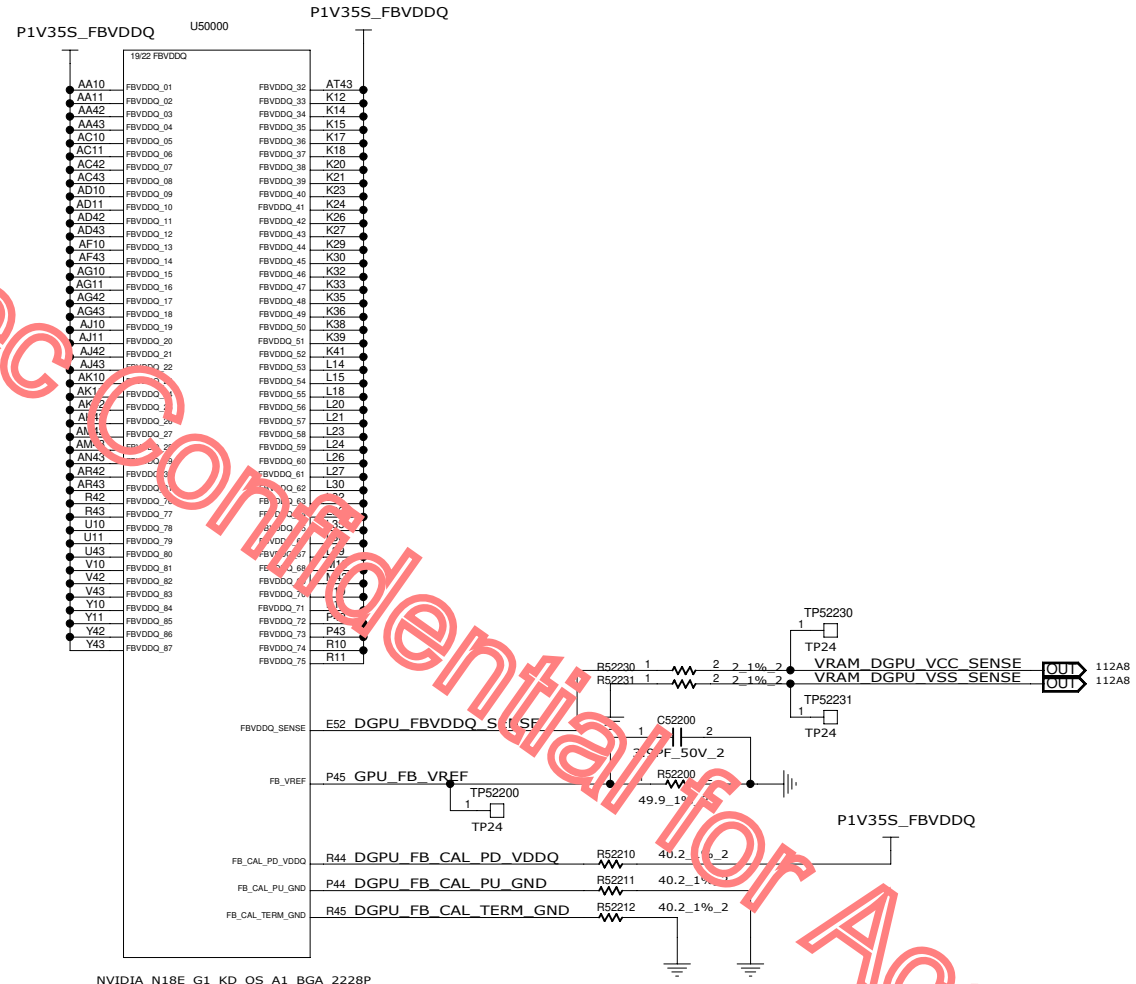
TITLE: MODEL,PROJECT,FUNCTION Block Diagram



55600 - 55699

52200 - 52299

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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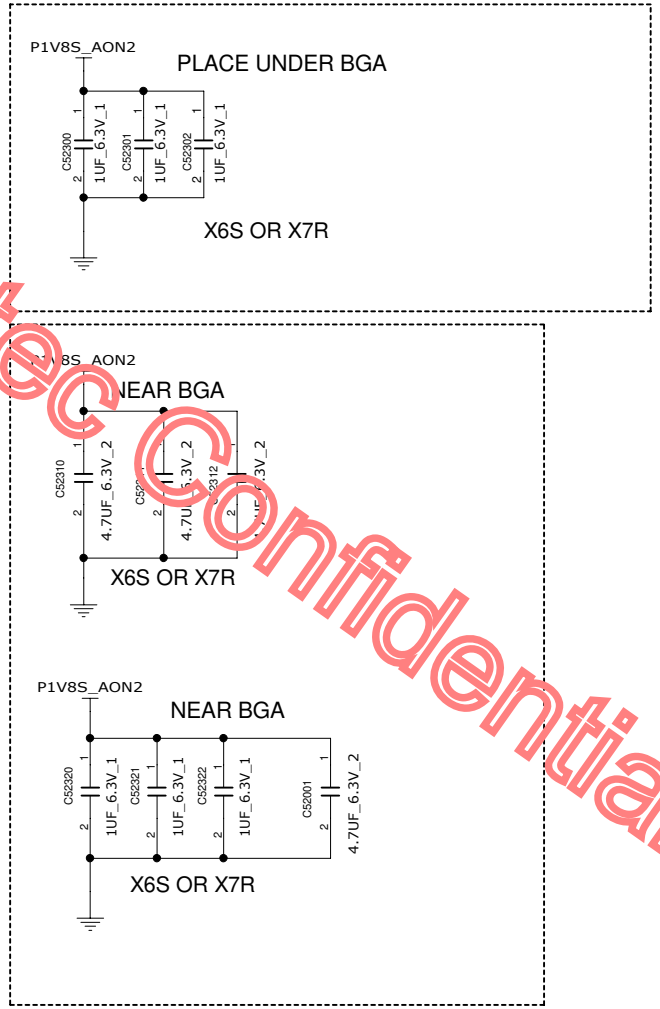
GPU 1V8_AON DECOUPLING



1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S) Alternate solution: 3 x 1.0uF (0201W X6S)	3 x 1uF (0402 X6S) 3 x 4.7uF (0603 X6S)

52300 - 52399

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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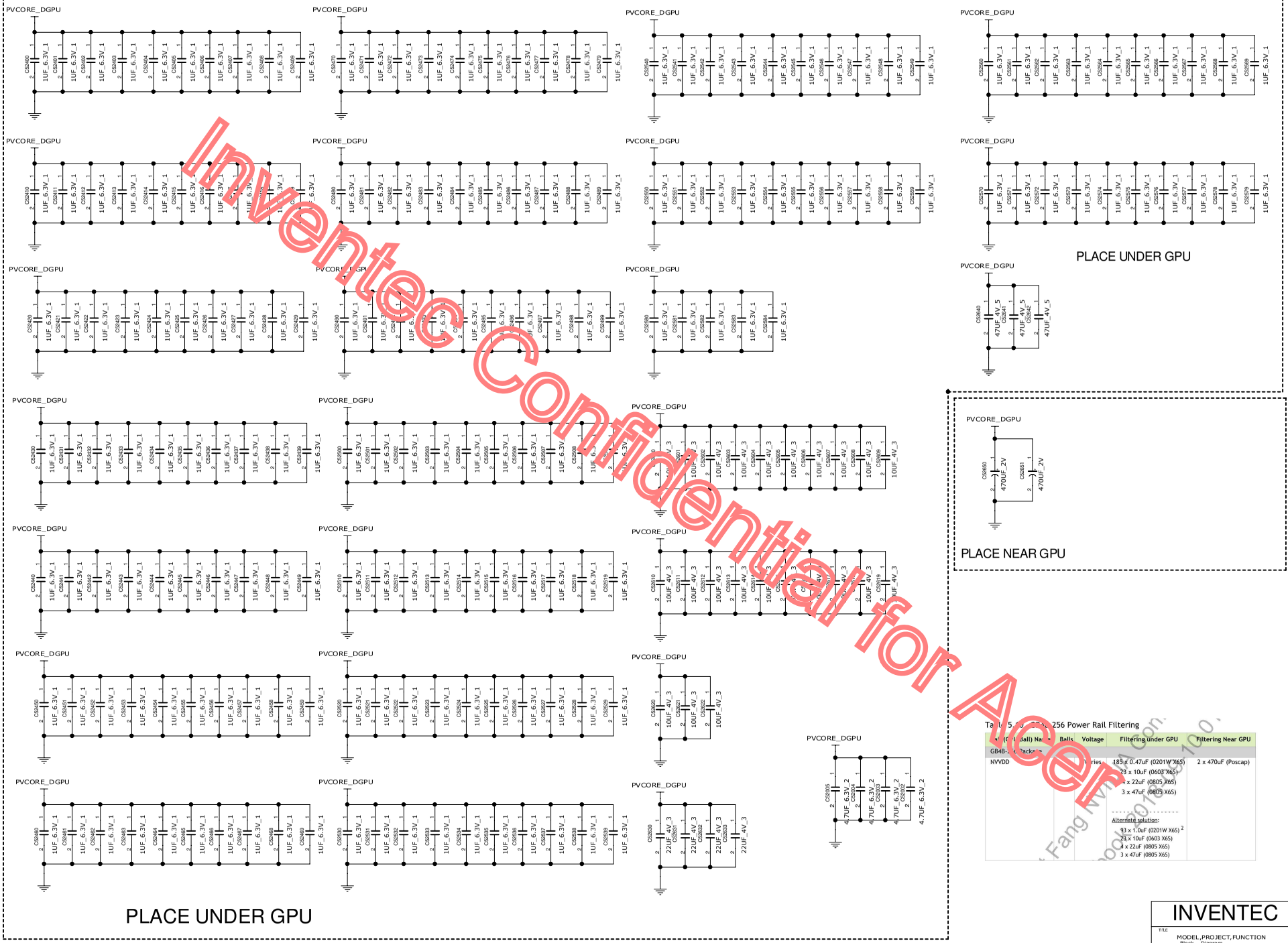

Table 5-[illegible] 256 Power Rail Filtering

[illegible] (GB48-[illegible] Ball) Name	Balls	Voltage	Filtering Under GPU	Filtering Near GPU
GB48-[illegible] Package				
NVVDD	[illegible]ries		185 x 0.47uF (0201W X6S) 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S) --- Alternate solution: 93 x 1.0uF (0201W X6S) [2] 23 x 10uF (0603 X6S) 3 x 22uF (0805 X6S) 3 x 47uF (0805 X6S)	2 x 470uF (Poscap)

52400 - 52999

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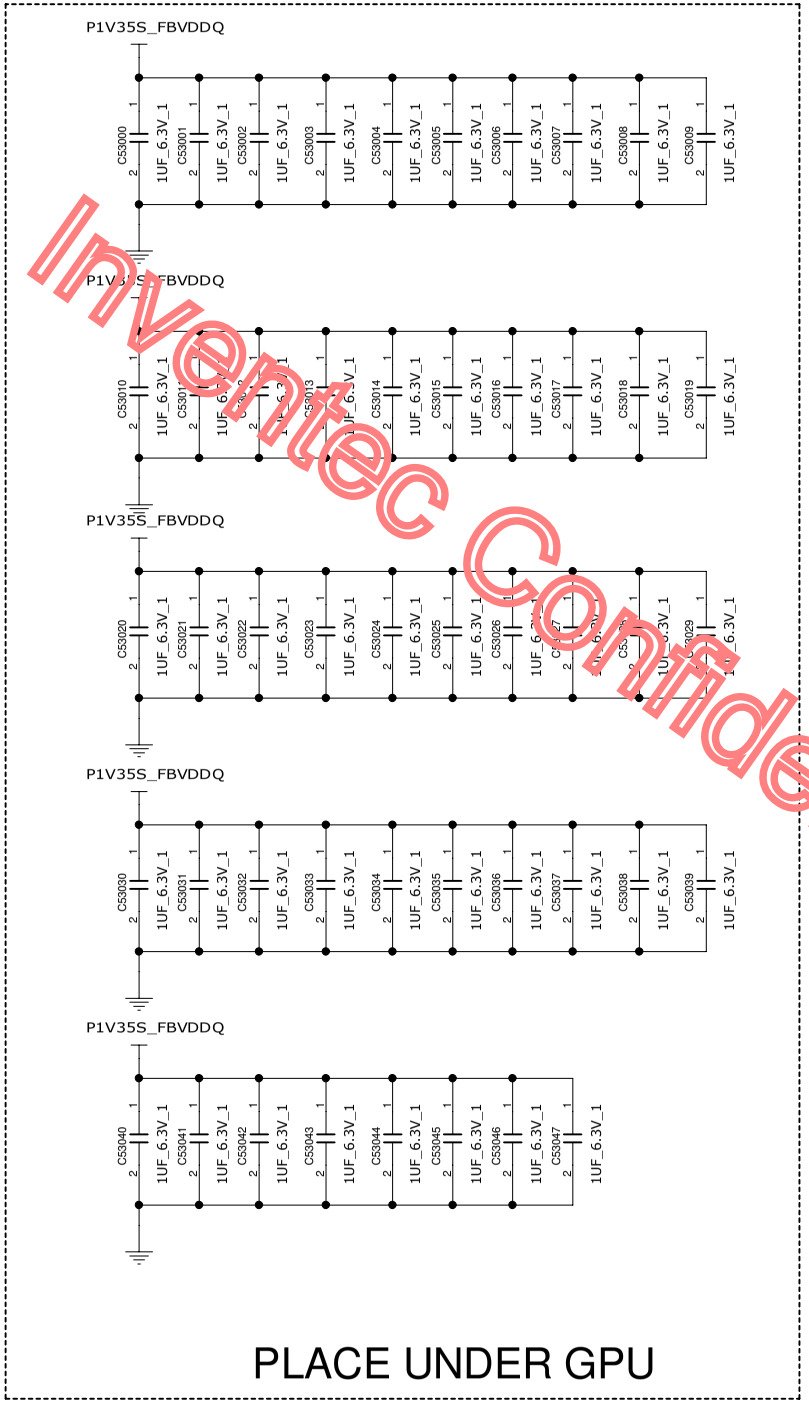

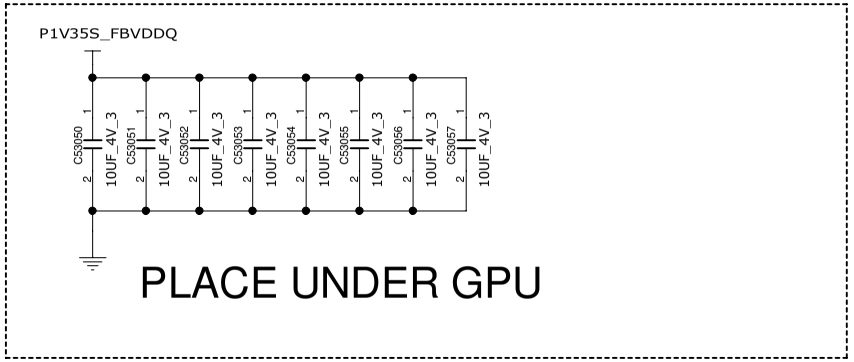

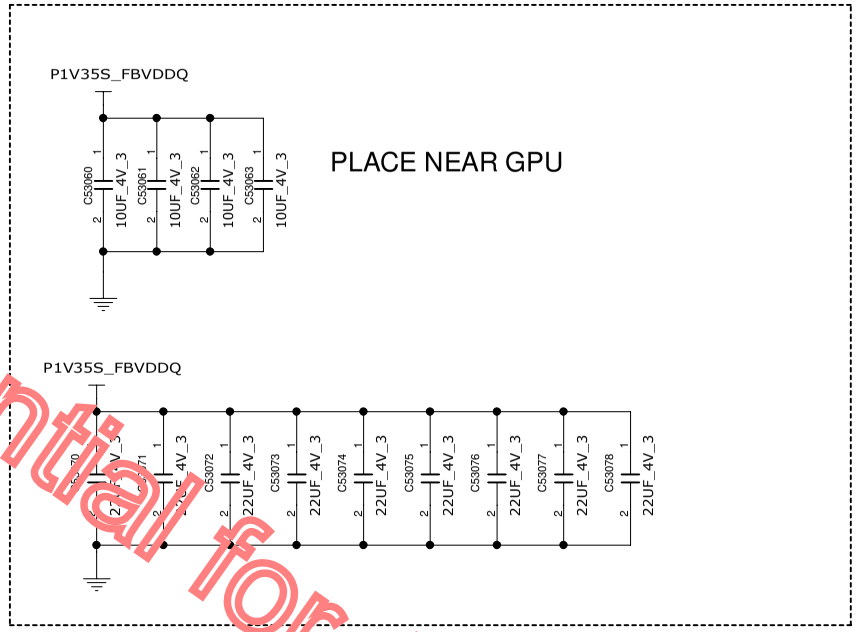

FBVDDQ (GPU side)	25V	48 x 0.47uF (0201W X6S) 8 x 10uF (0603 X6S)	4 x 10uF (0603 X6S) 9 x 22uF (0603 X6S)
		Alternate solution: 24 x 1.0uF (0201W X6S) [2] 8 x 10uF (0603 X6S)	

53000 - 53299

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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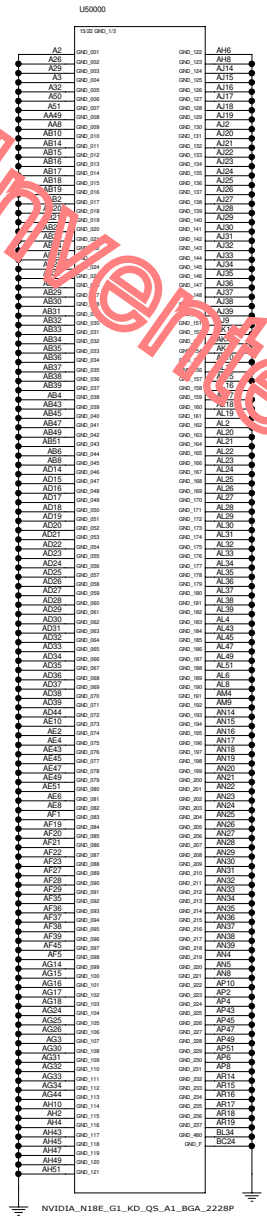
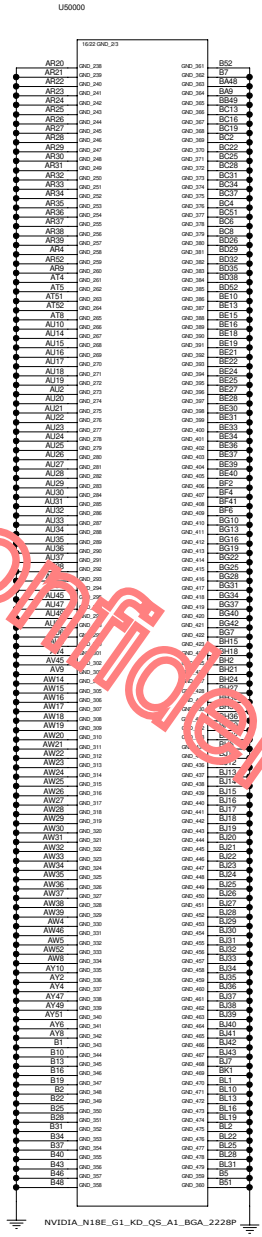
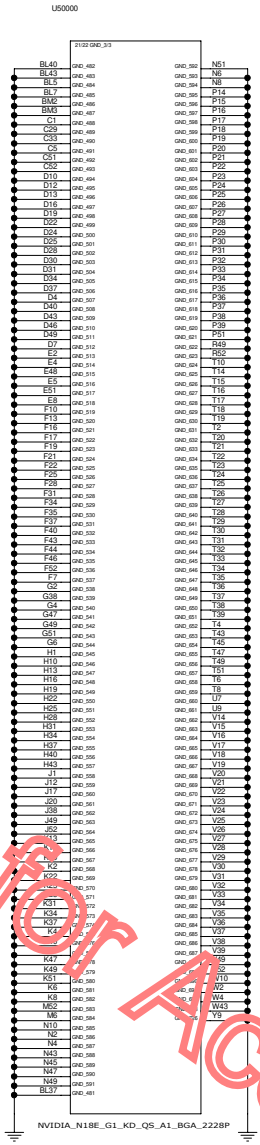
GND







53300 - 53499

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INVENTEC

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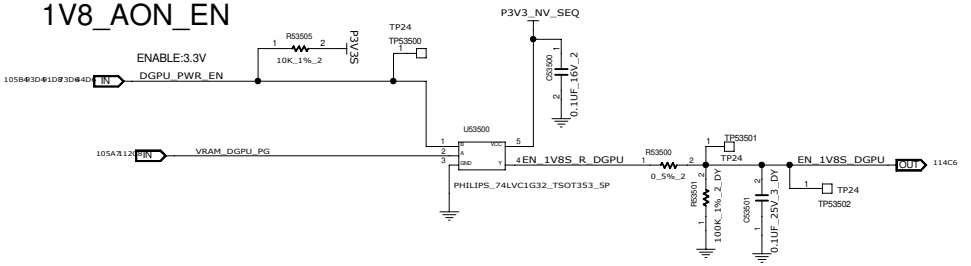
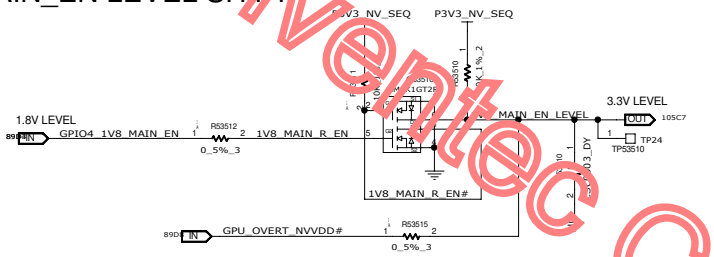
1V8_AON_EN



1V8_MAIN_EN LEVEL SHIFT



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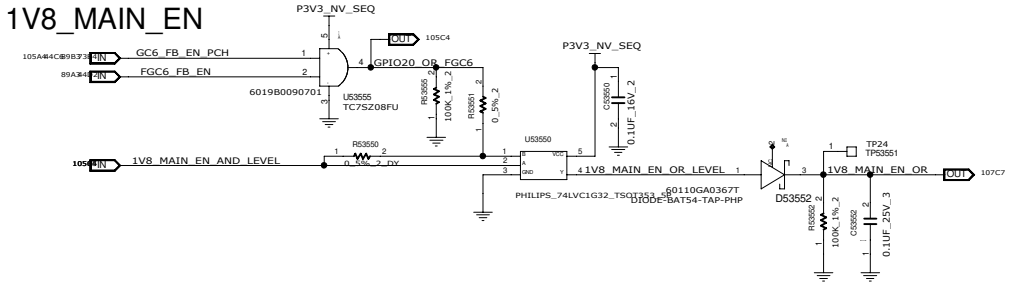
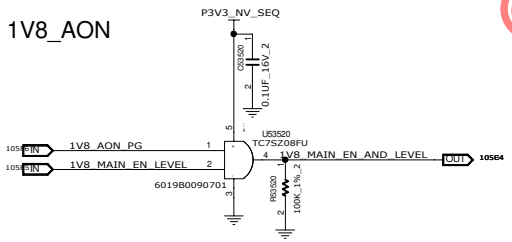
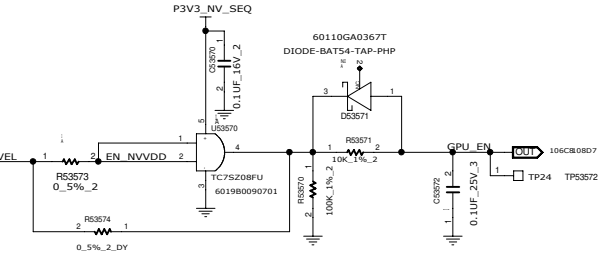


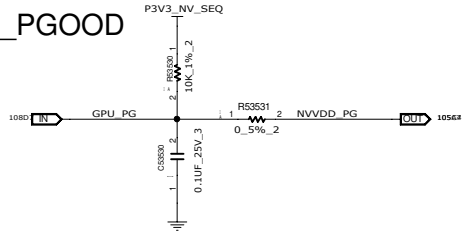
1V8_MAIN_EN AND WITH 1V8_AON



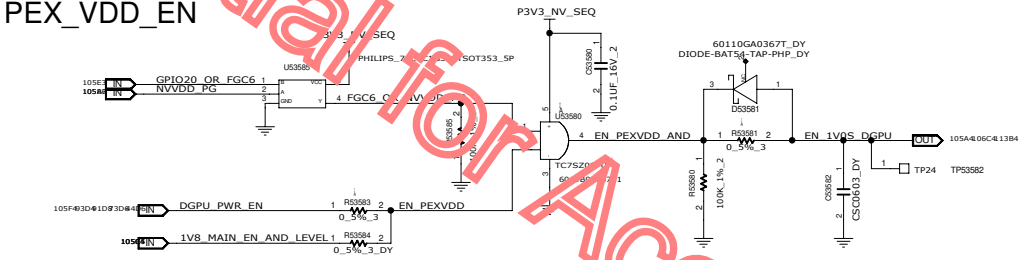
NVVDD_EN



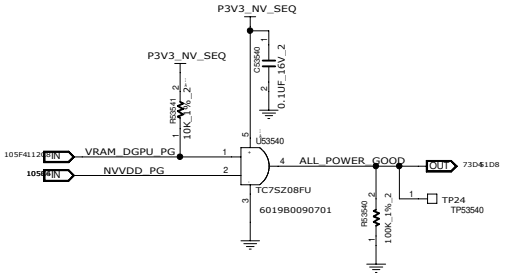
NVVDD_PGOOD



PEX_VDD_EN



ALL POWER GOOD

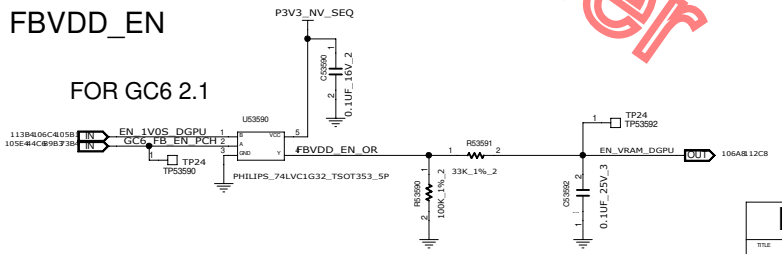


55600 - 55699

53500 - 53899

FBVDD_EN

FOR GC6 2.1



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MODEL,PROJECT,FUNCTION
Block Diagram

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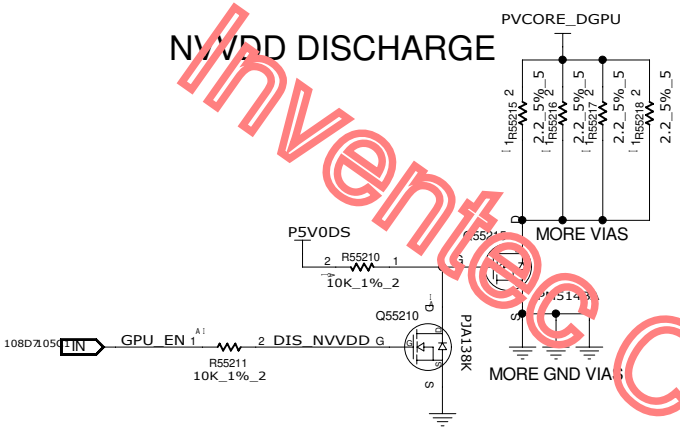
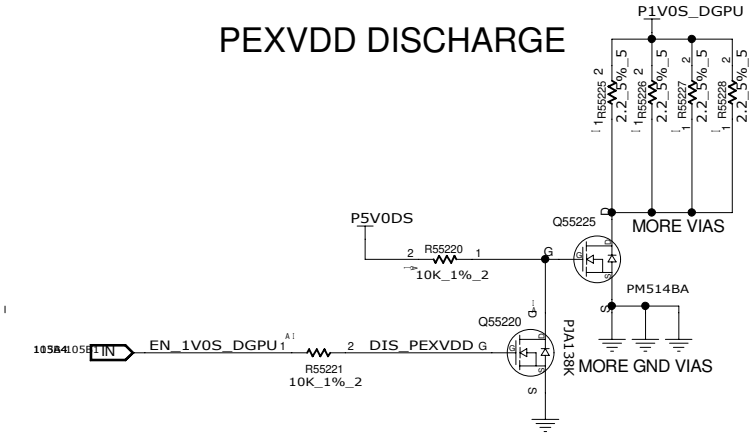
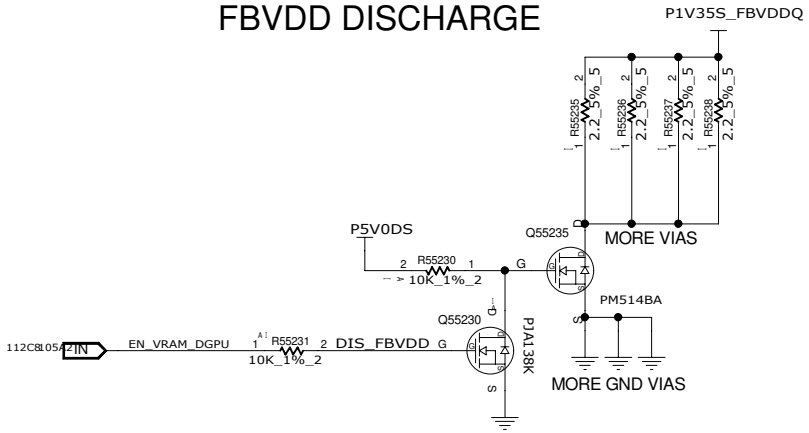
DISCHARGE CIRCUIT







55200 - 55299

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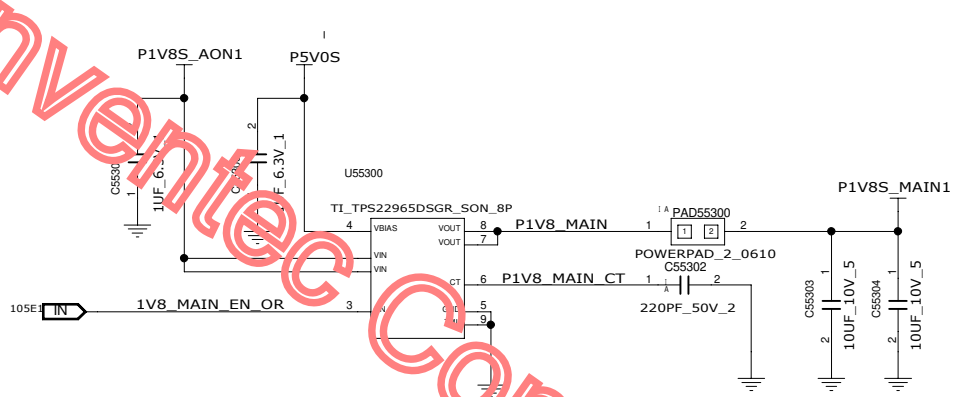
1V8_MAIN



55300 - 55399

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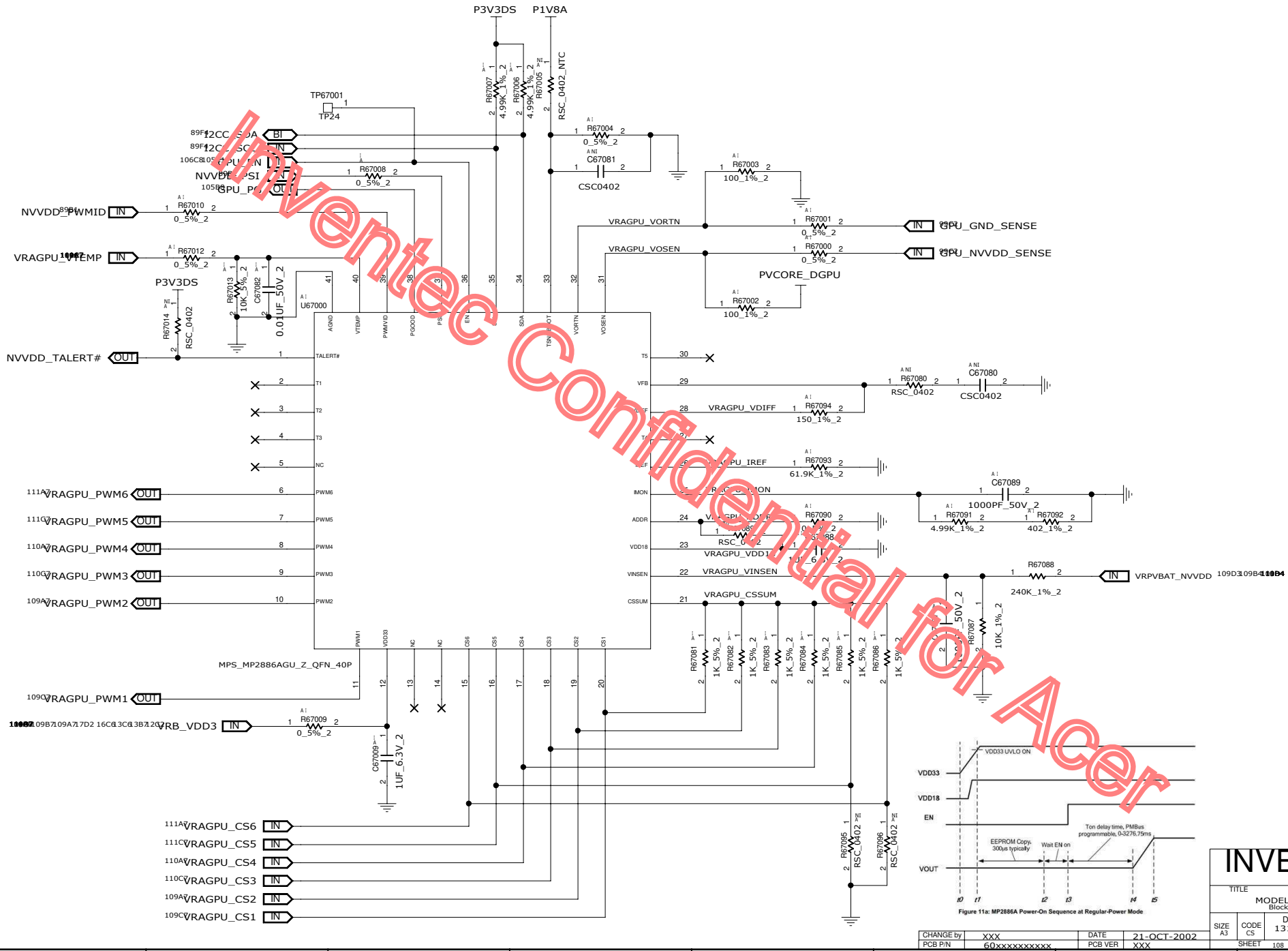

Figure 11a: MP2886A Power-On Sequence at Regular-Power Mode

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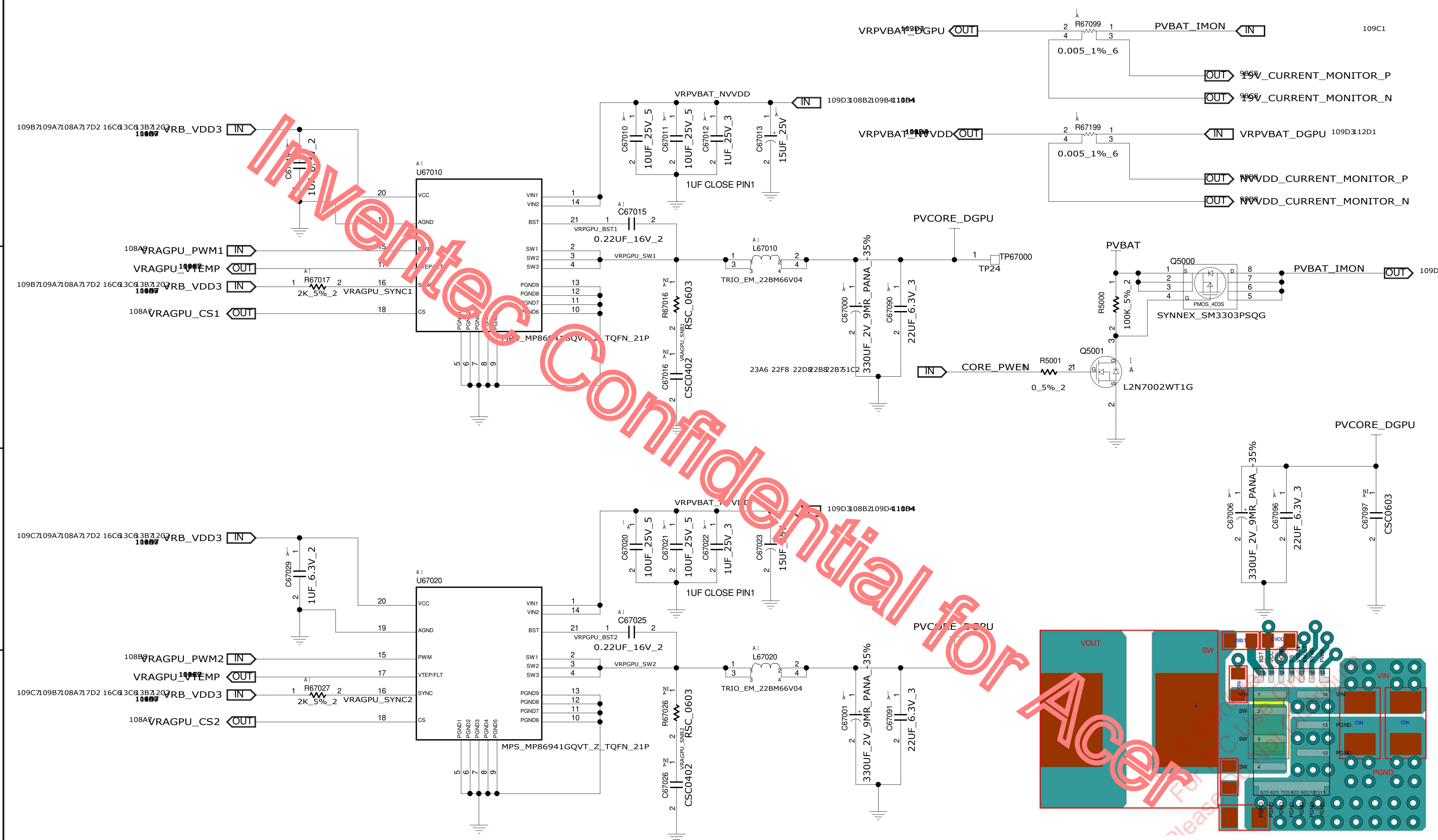

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TITLE

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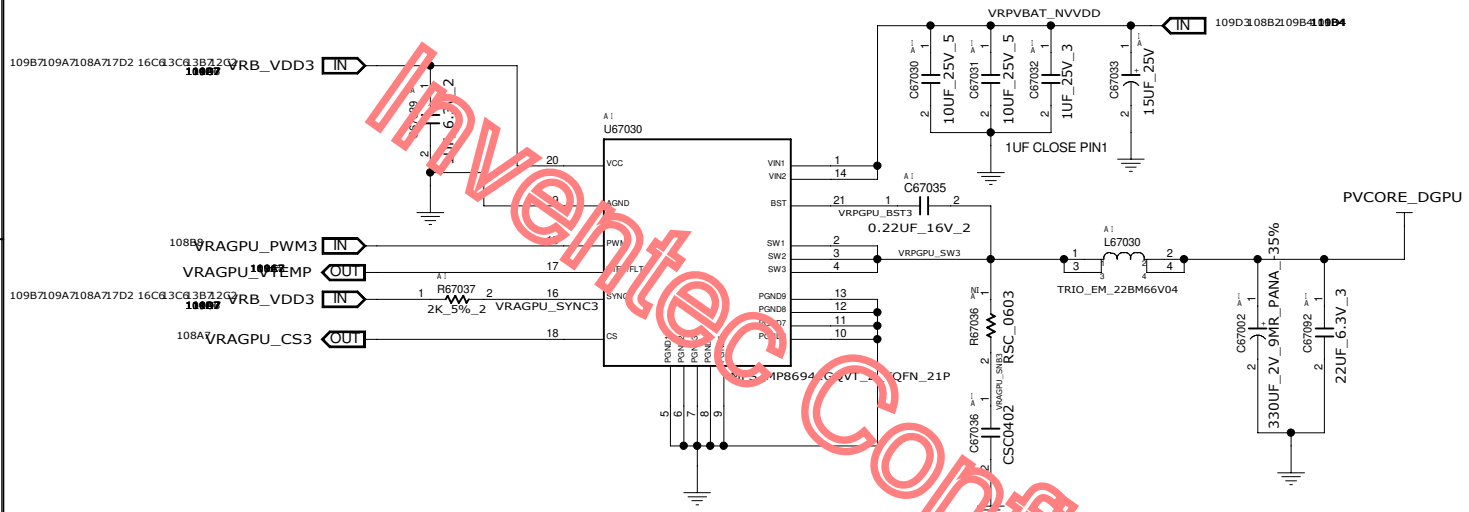

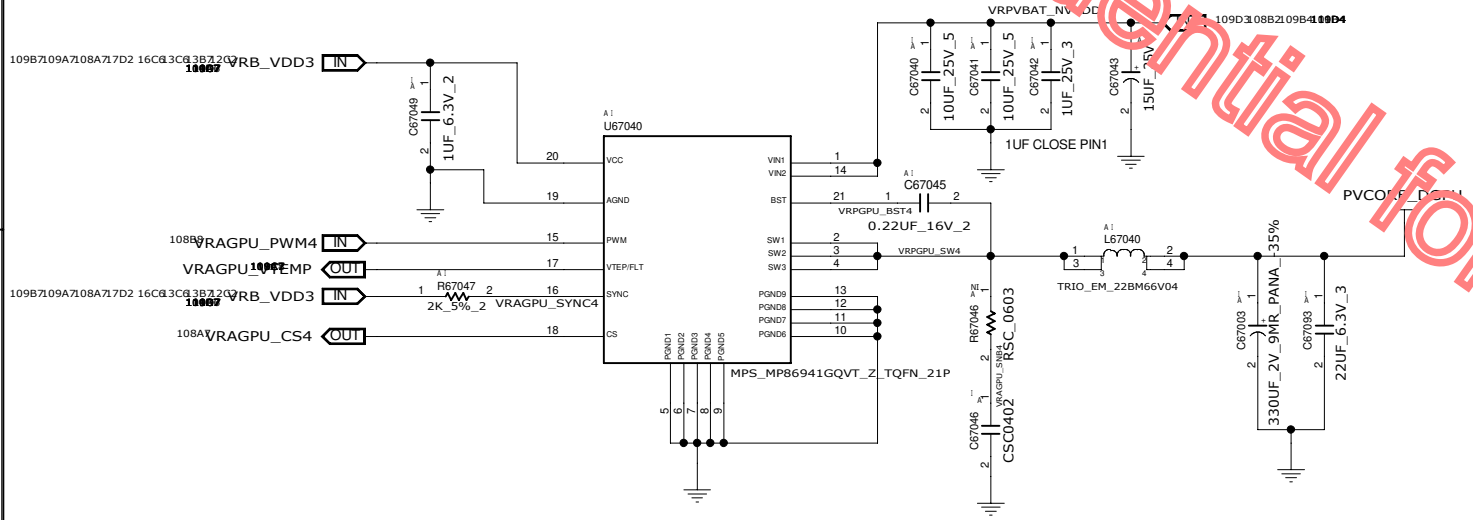

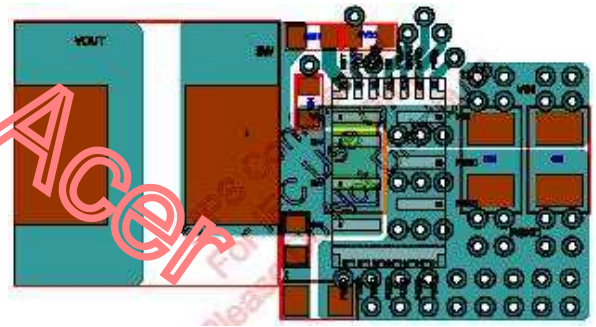

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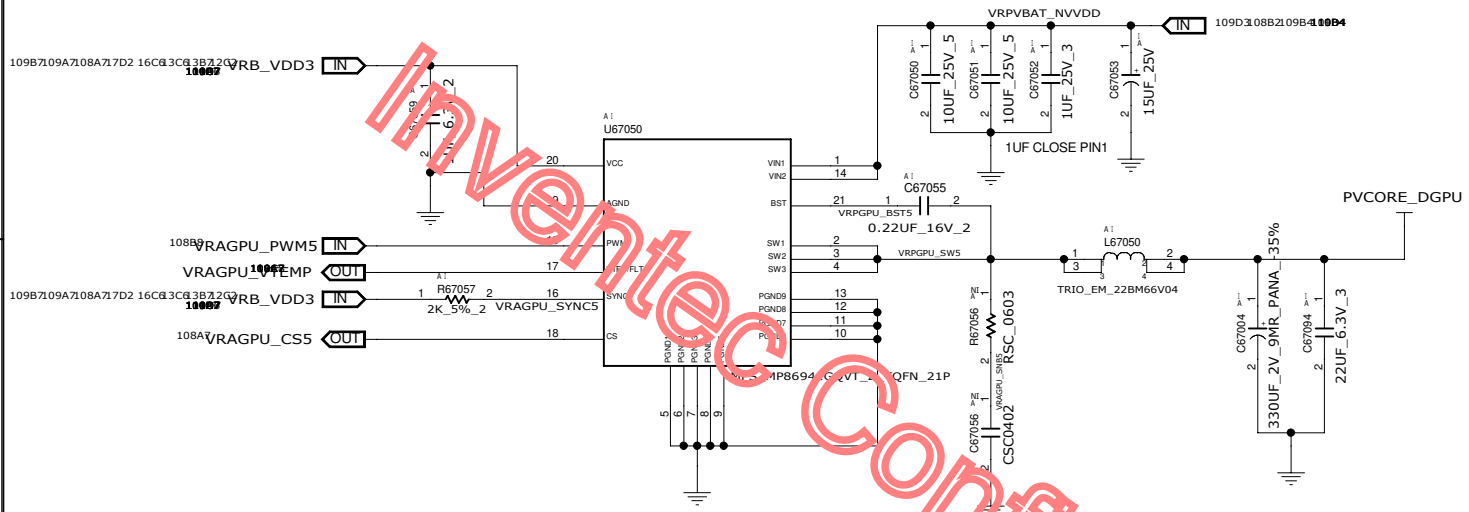

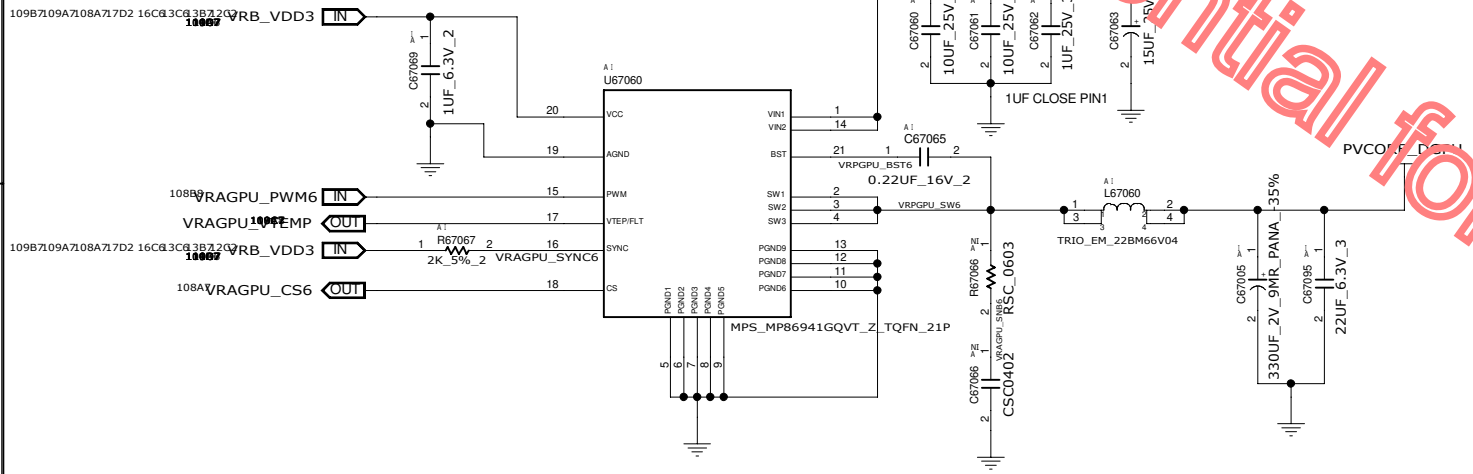

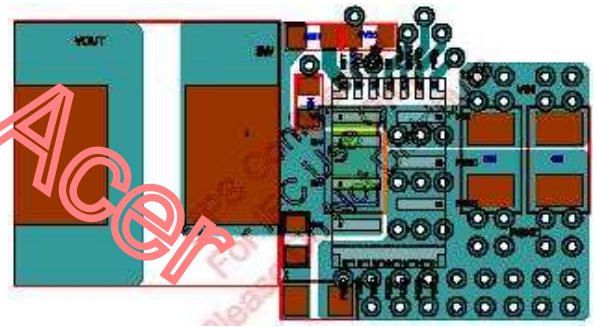

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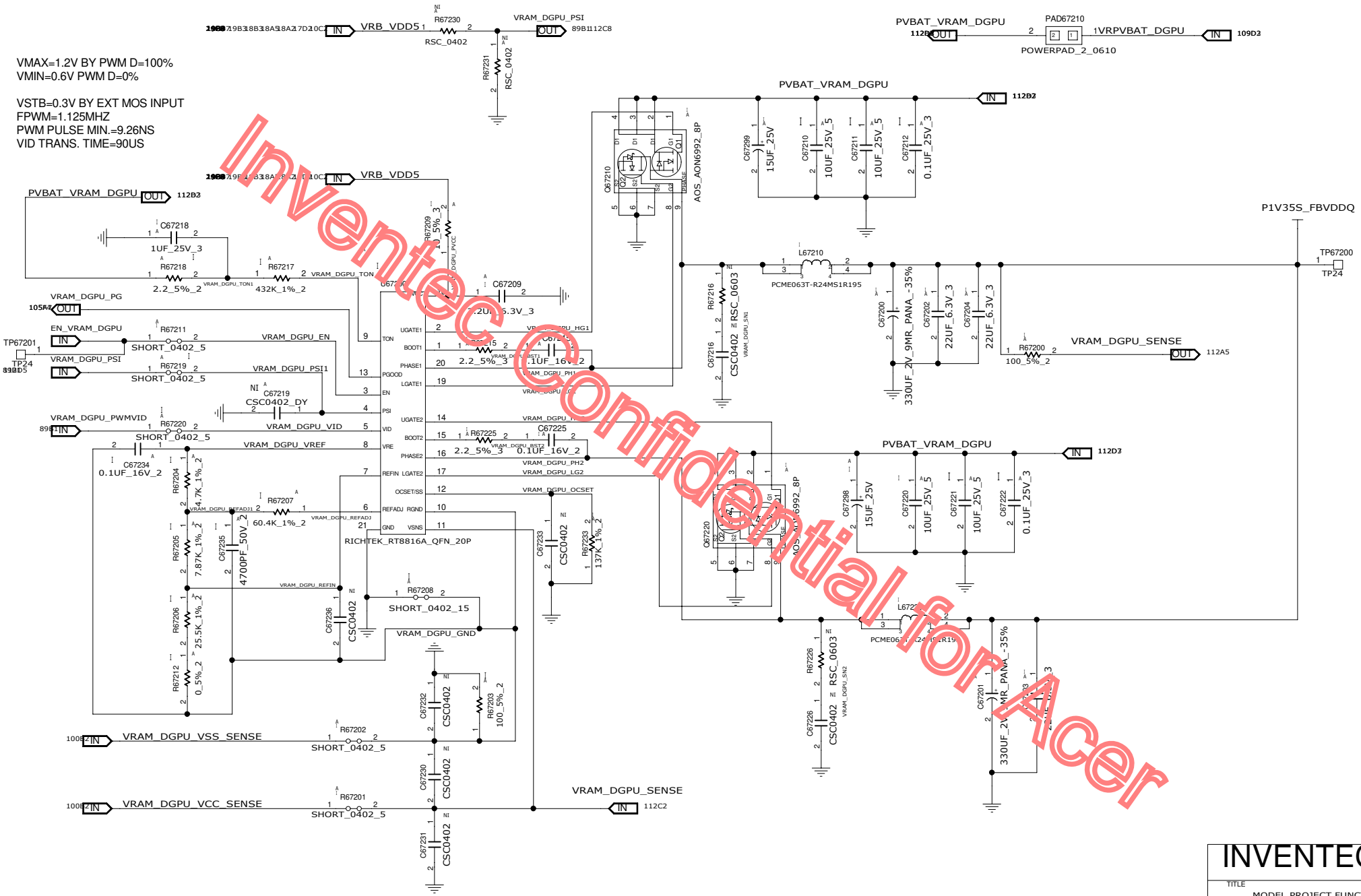

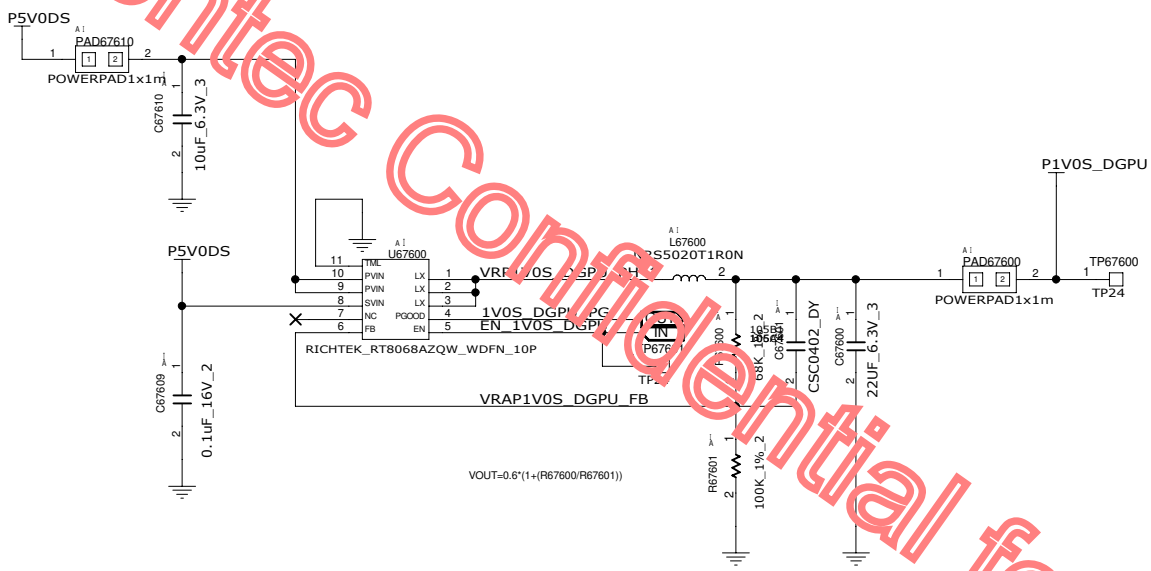

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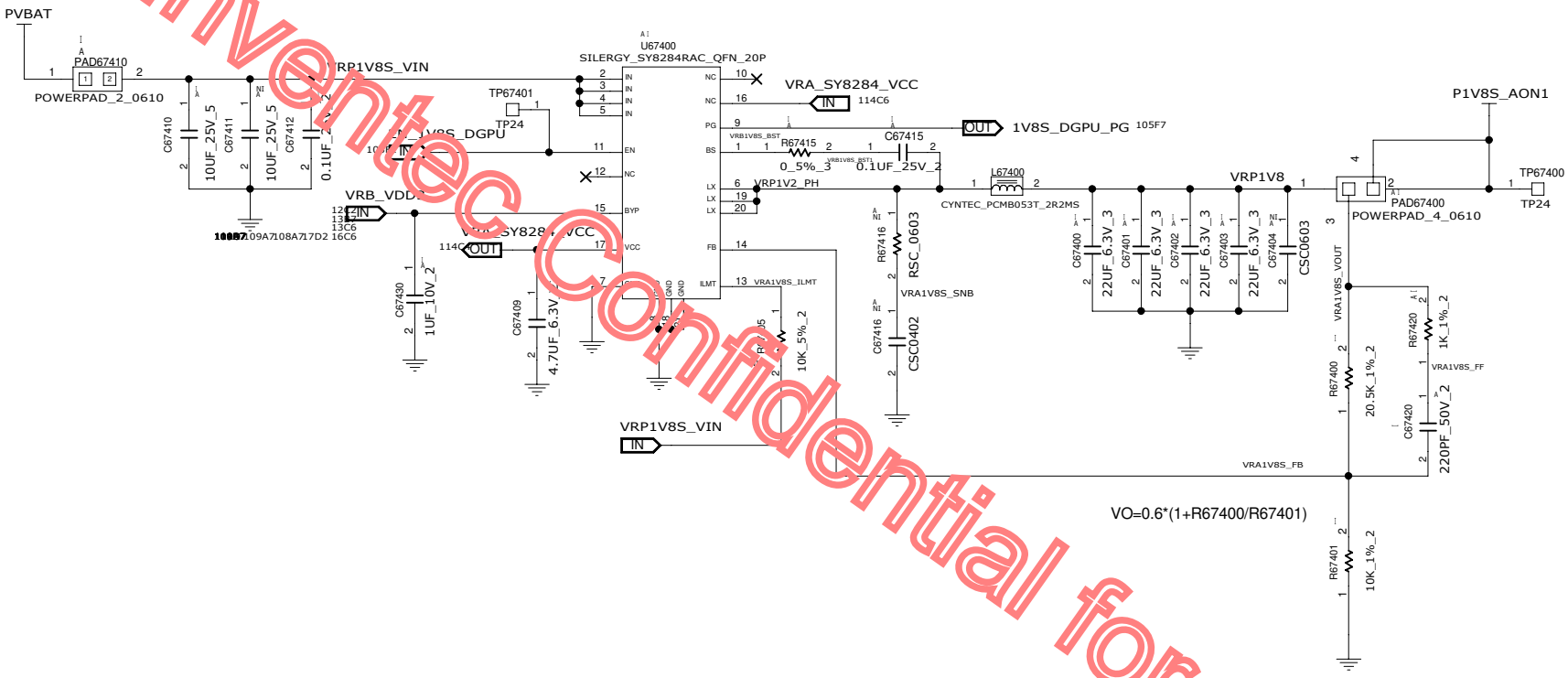

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SIZE	CODE	DOC.NUMBER	REV
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Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms)[2] (A)	Input EDPp (5ms)[2] (A)	Input EDPc (1sec)[1] (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$Input\ EDPc\ Current\ (A) = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$Input\ EDPp\ (A) at\ V_{new} = Input\ EDPp(A)\ at\ 19V x\ \frac{19V}{V_{new}(V)}$$

Table 12. Output EDP-Continuous

Product	TGP (W)	NVVDD – (A)	FB TOTAL[5] 1.35V[3, 4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
N18E-G3	150	14	46	1.6	2.3
	160	15			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

Product	TGP (W)	NVVDD - (A)	FB TOTAL[4] 1.35V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)	1.8V Total[2] 1.8V[5] (A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

HISTORY

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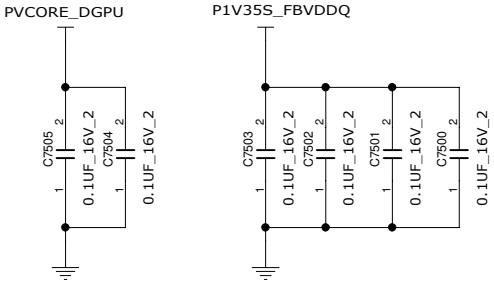
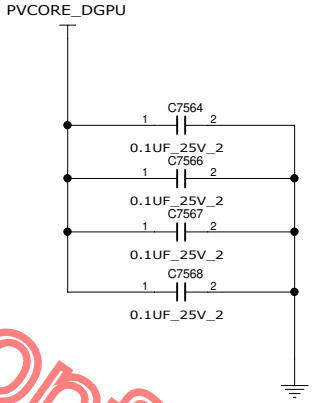
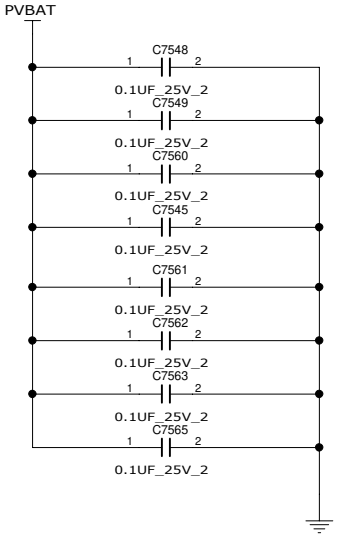
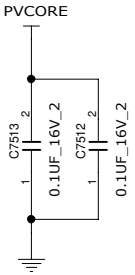
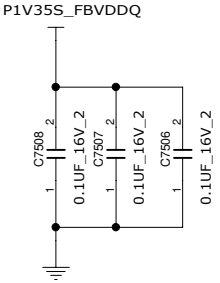
EMI

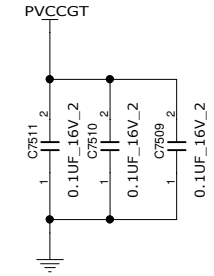


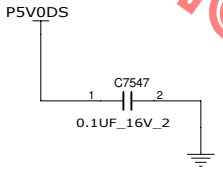


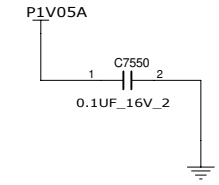


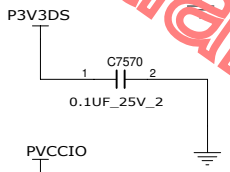


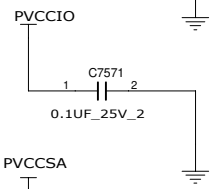


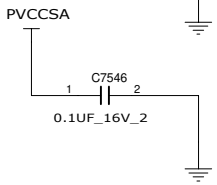


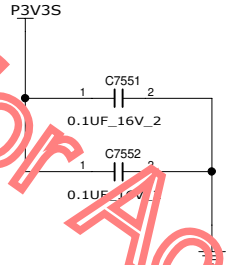












CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NFC CNNN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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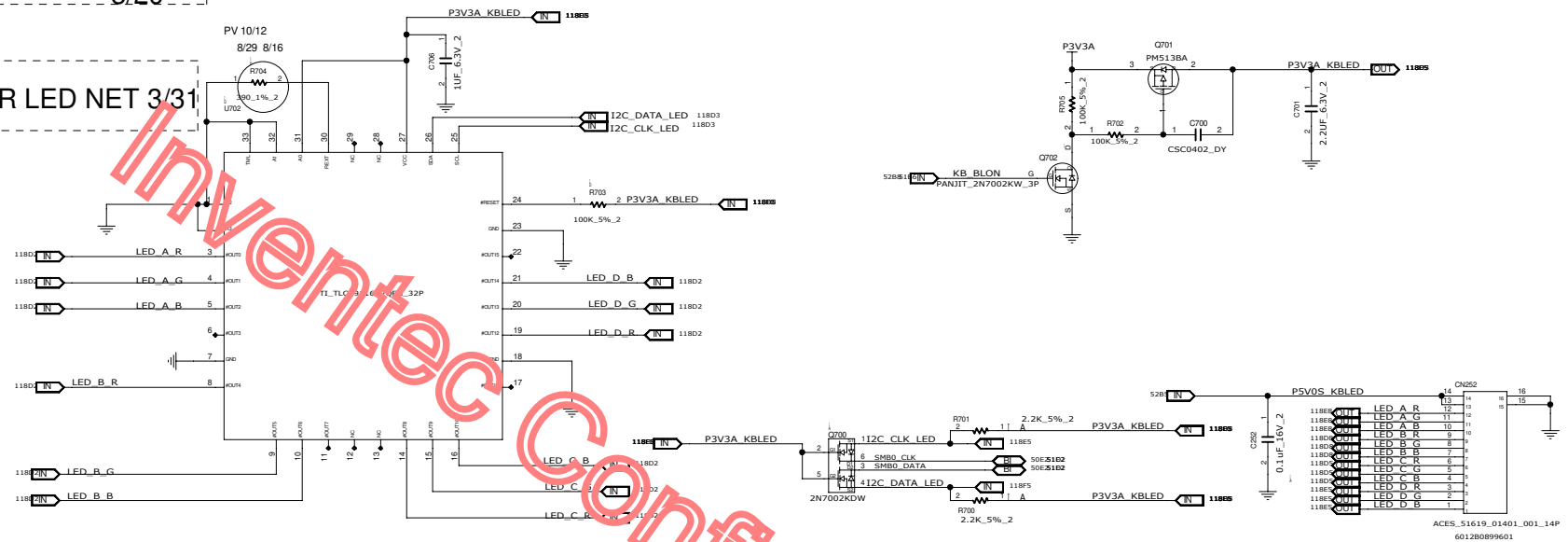
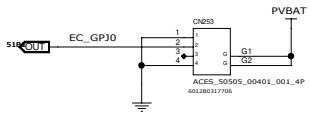
ADJUST LED RES 8/16
8/29

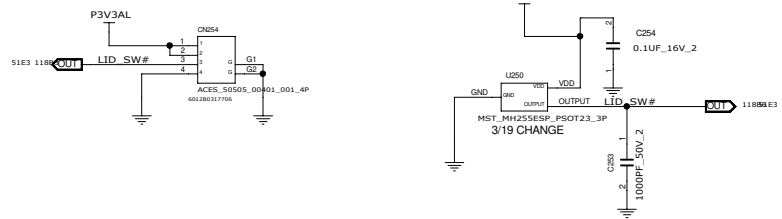
RE-ORDER LED NET 3/31



TURBO#



HALL_SENSOR



REFERENCE NUMBER:700~800

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
RING LED

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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TURBO# BOARD

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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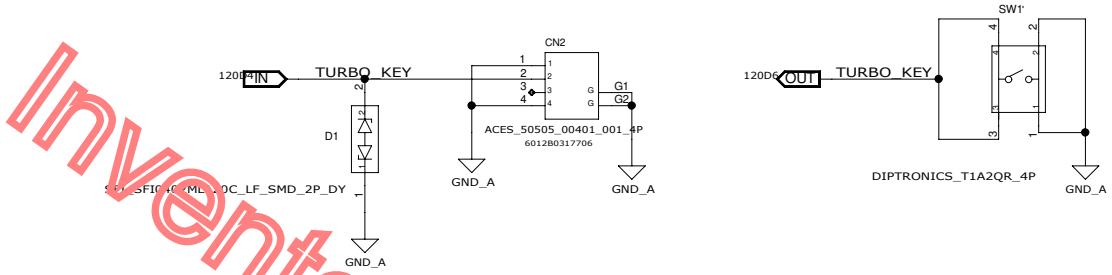
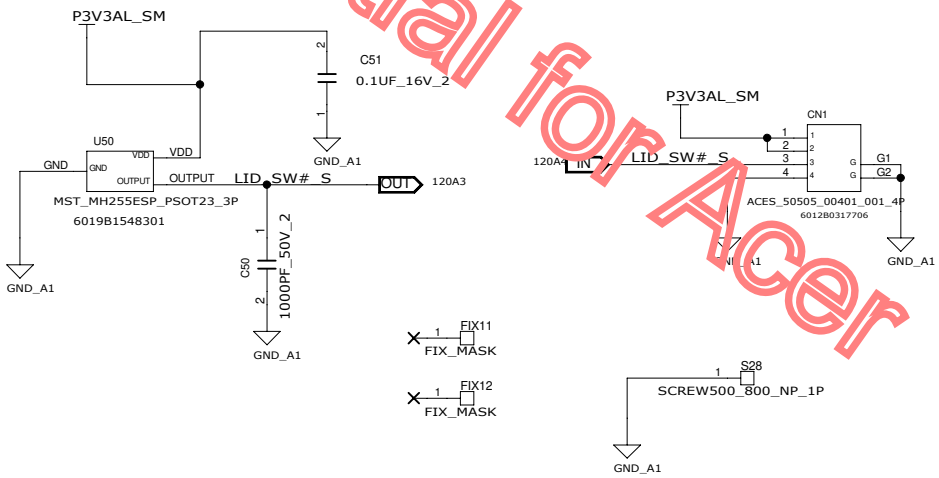
TURBO#



HALL_SENSOR



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

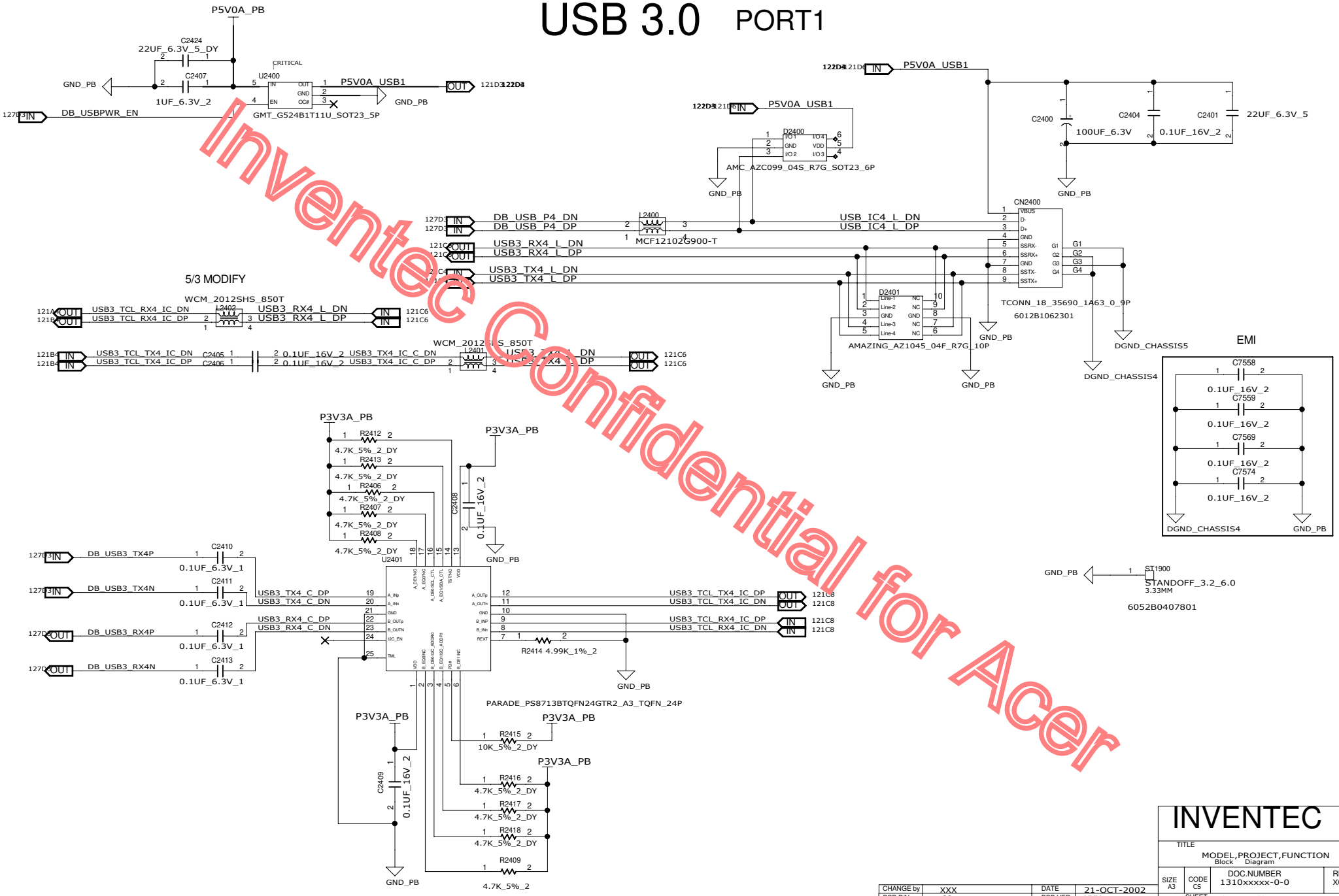
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 120 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

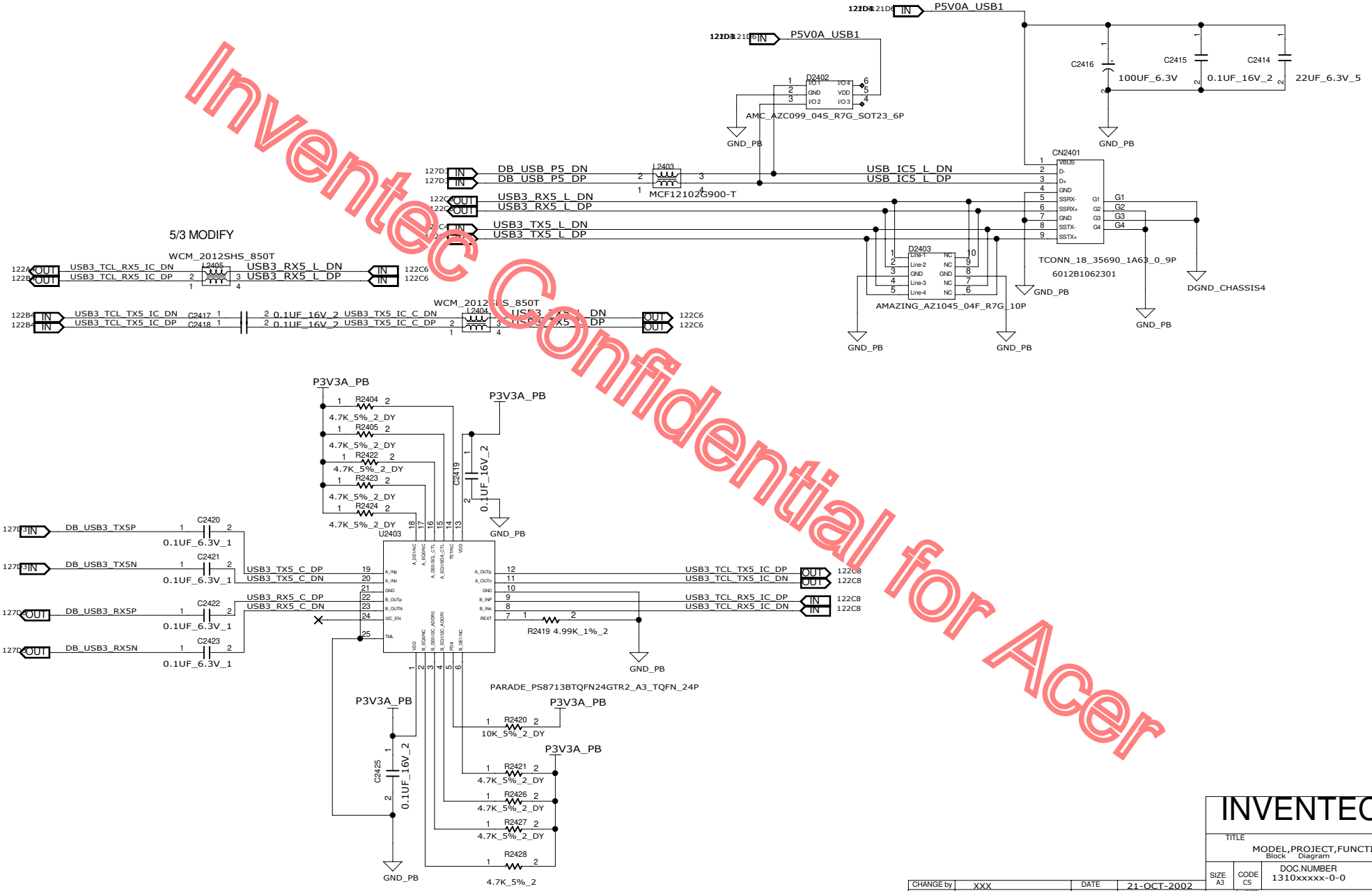
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 121 of 139

REFERENCE 2400~2450(USB3.0)

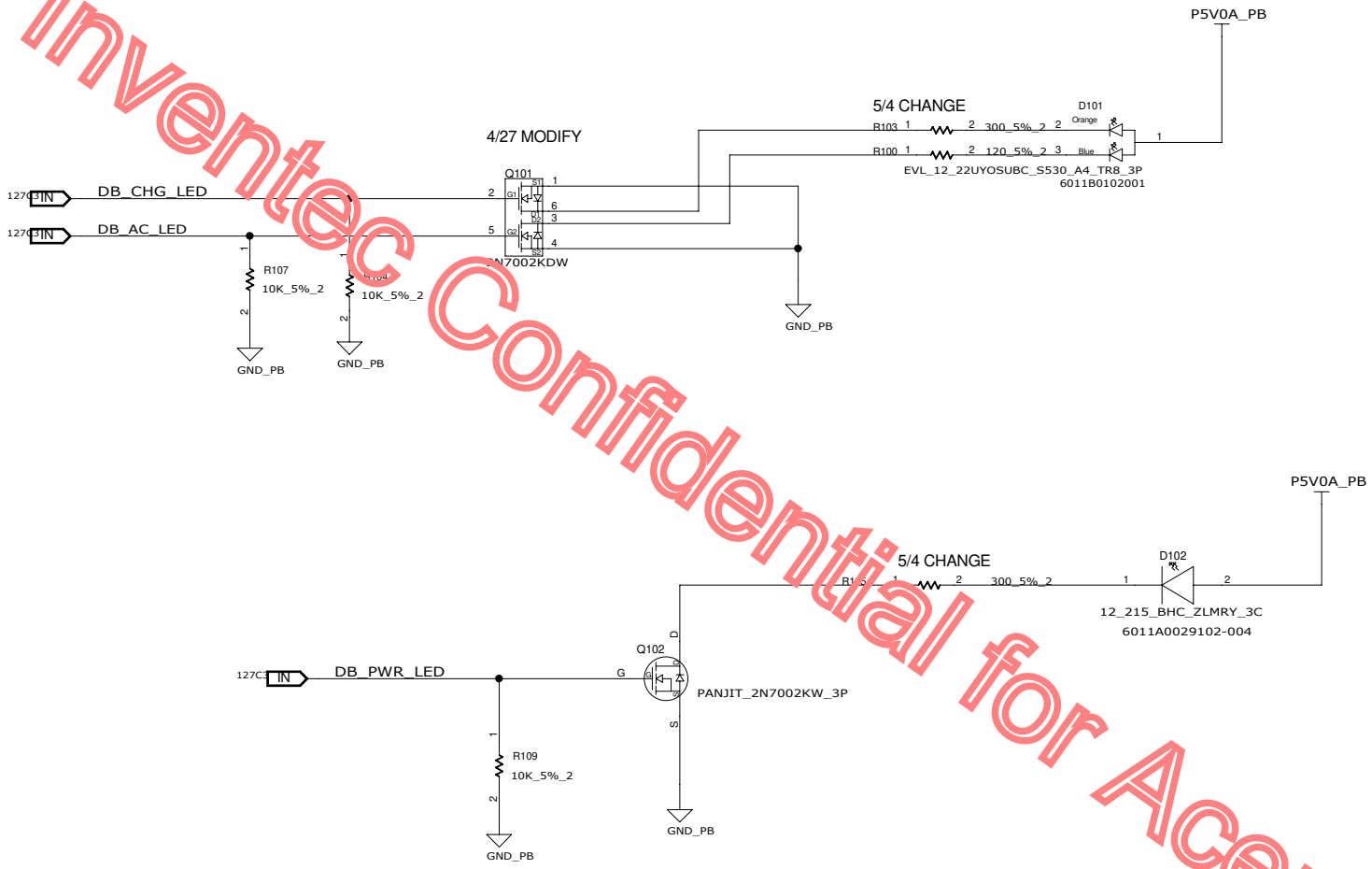
USB 3.0 PORT2



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 122 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

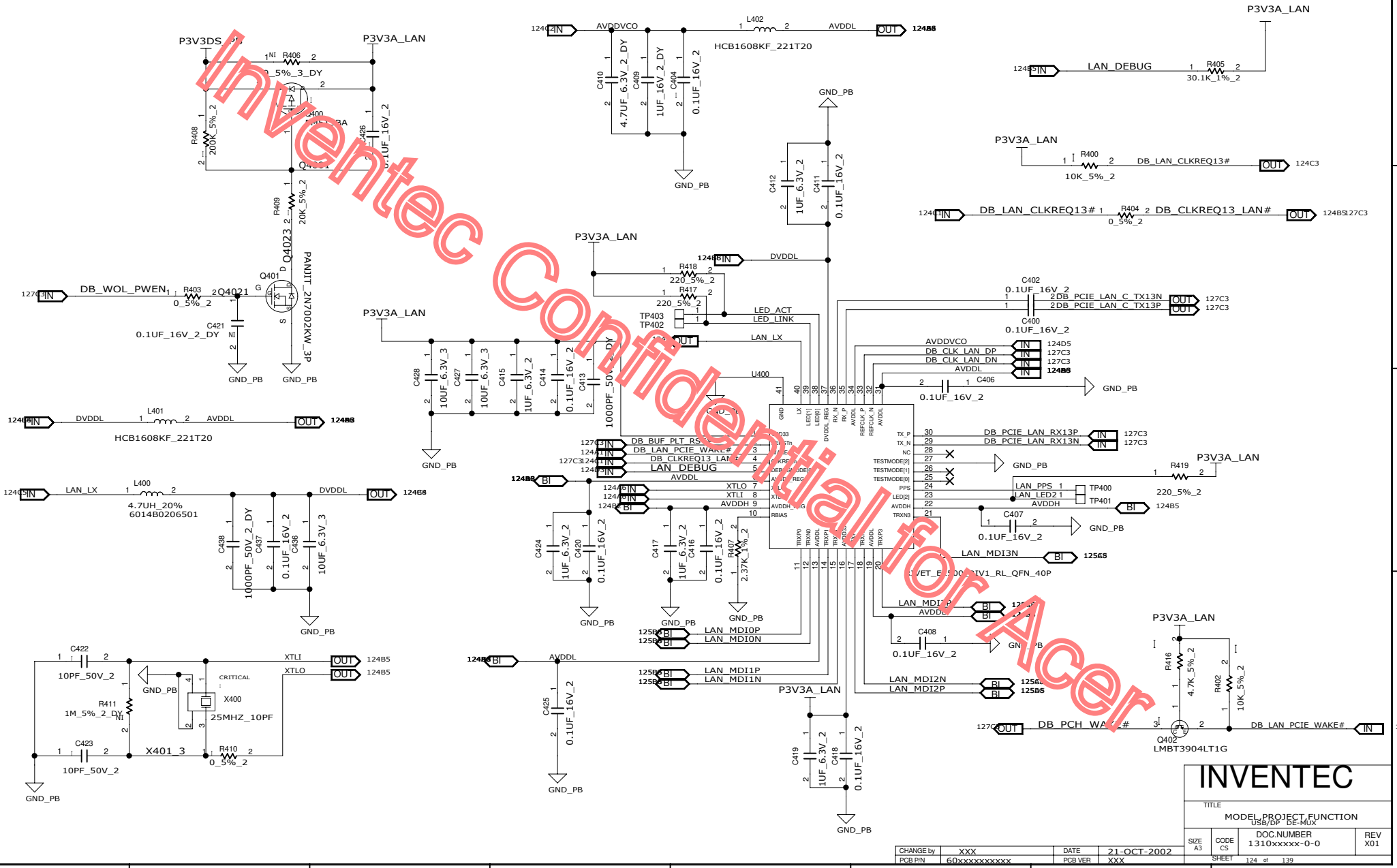


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 123 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

LAN (CONTROLLER)
E2500

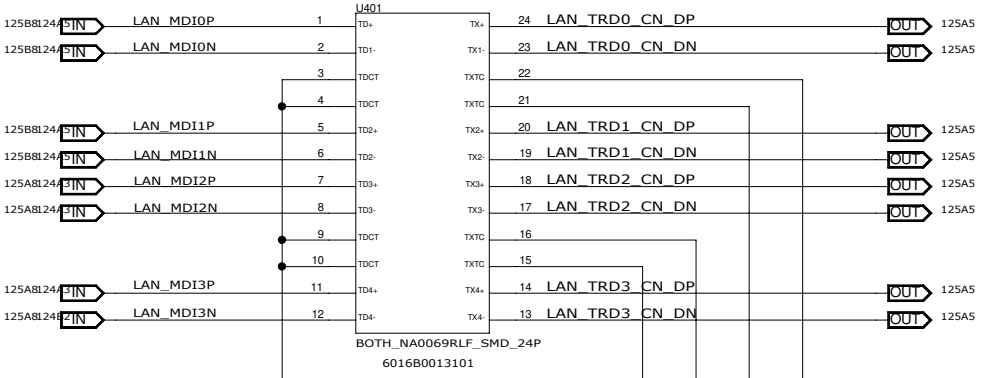


INVENTEC

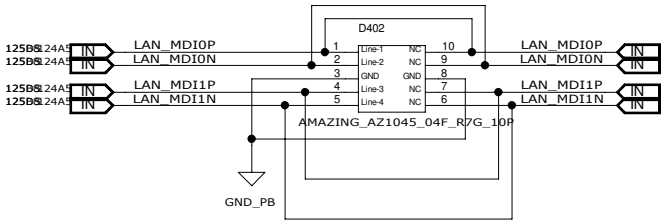
TITLE: MODEL_PROJECT_FUNCTION
USB/DP DE-MUX

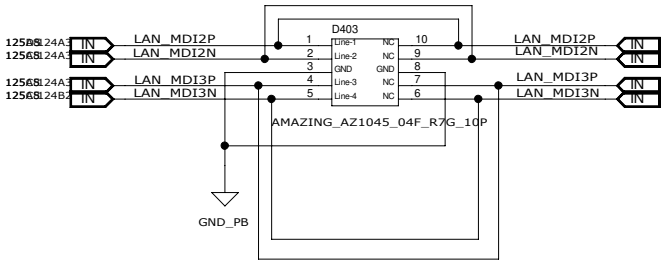
CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET 124 of 139	

TRANSFORMER

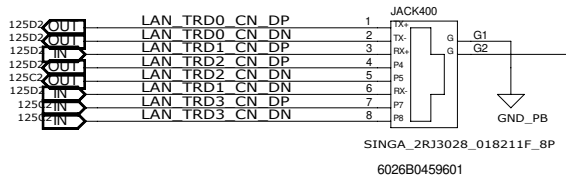


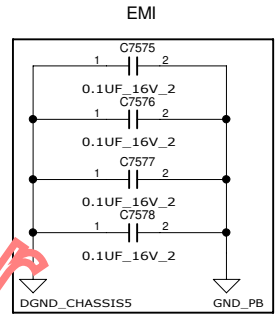
ESD





RJ-45

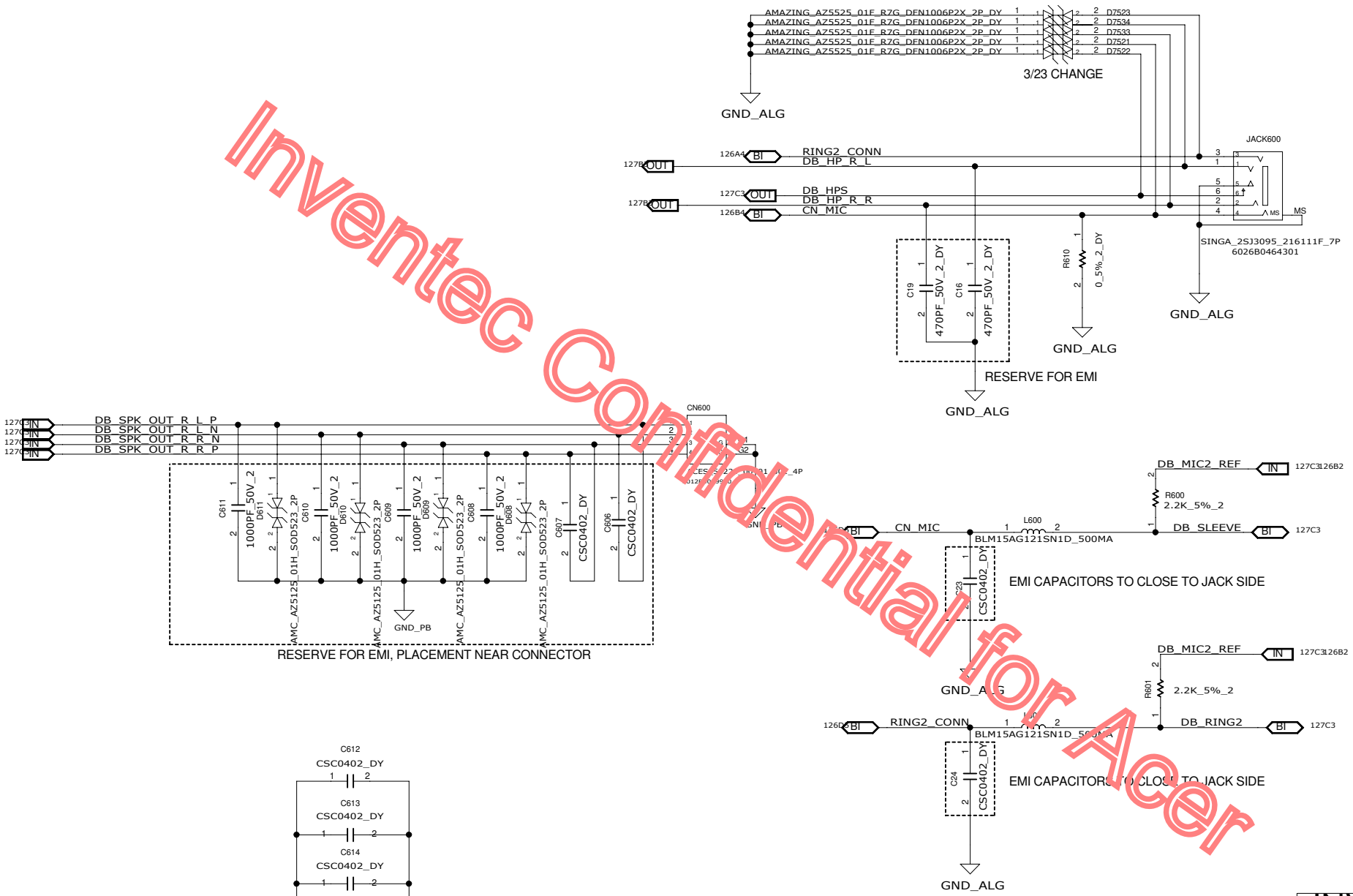




INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 125 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



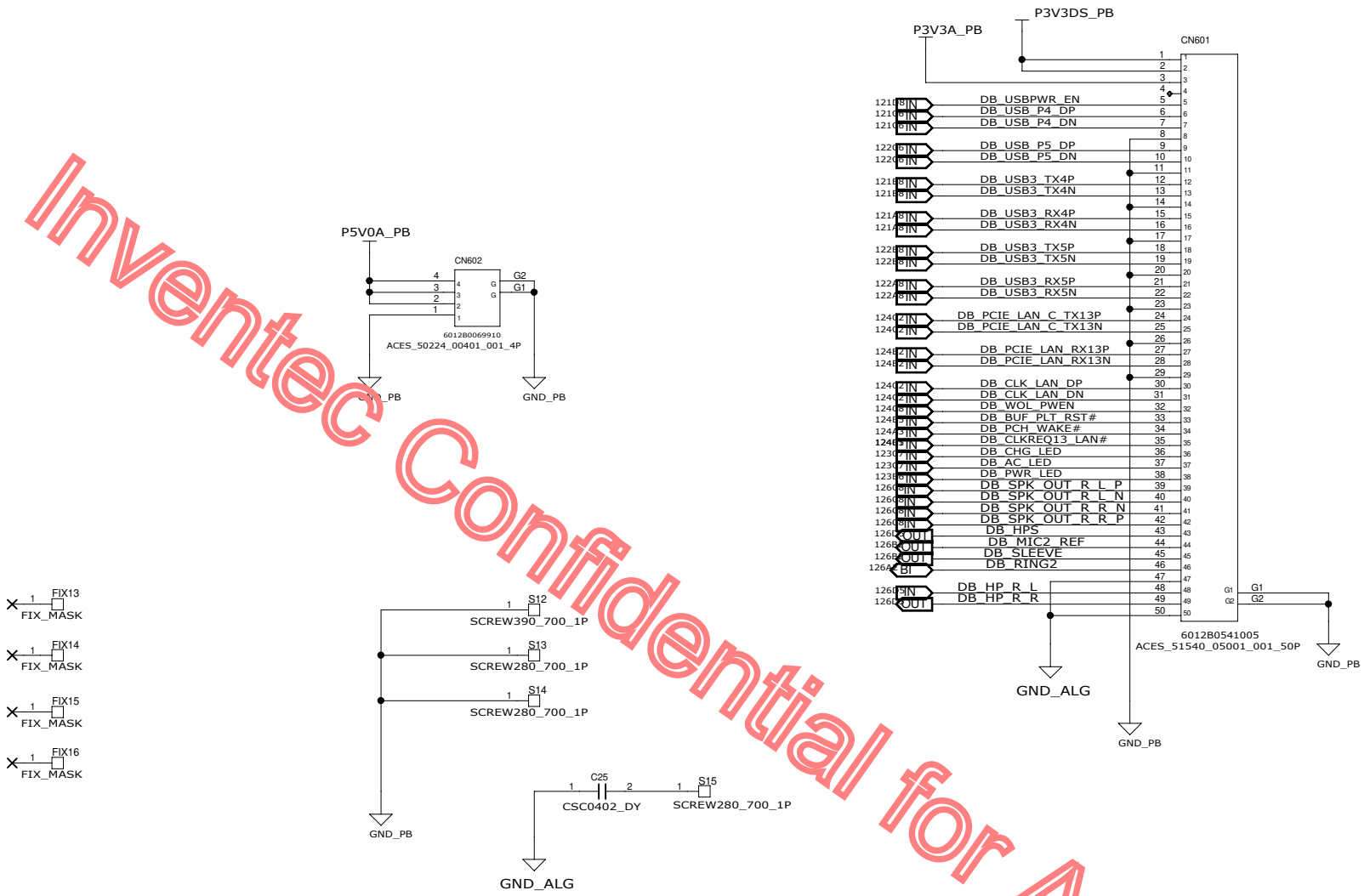
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 126 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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FOR 17 SMALL BOARD

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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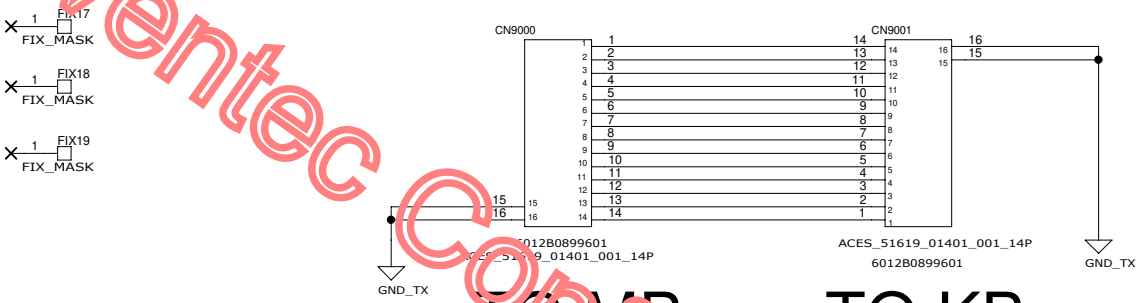
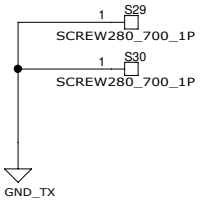
6050A3090601



TO MB TO KB



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 129 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

6050A3090501

TO MB TO KB

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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FOR I5 AUDIO BOARD

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

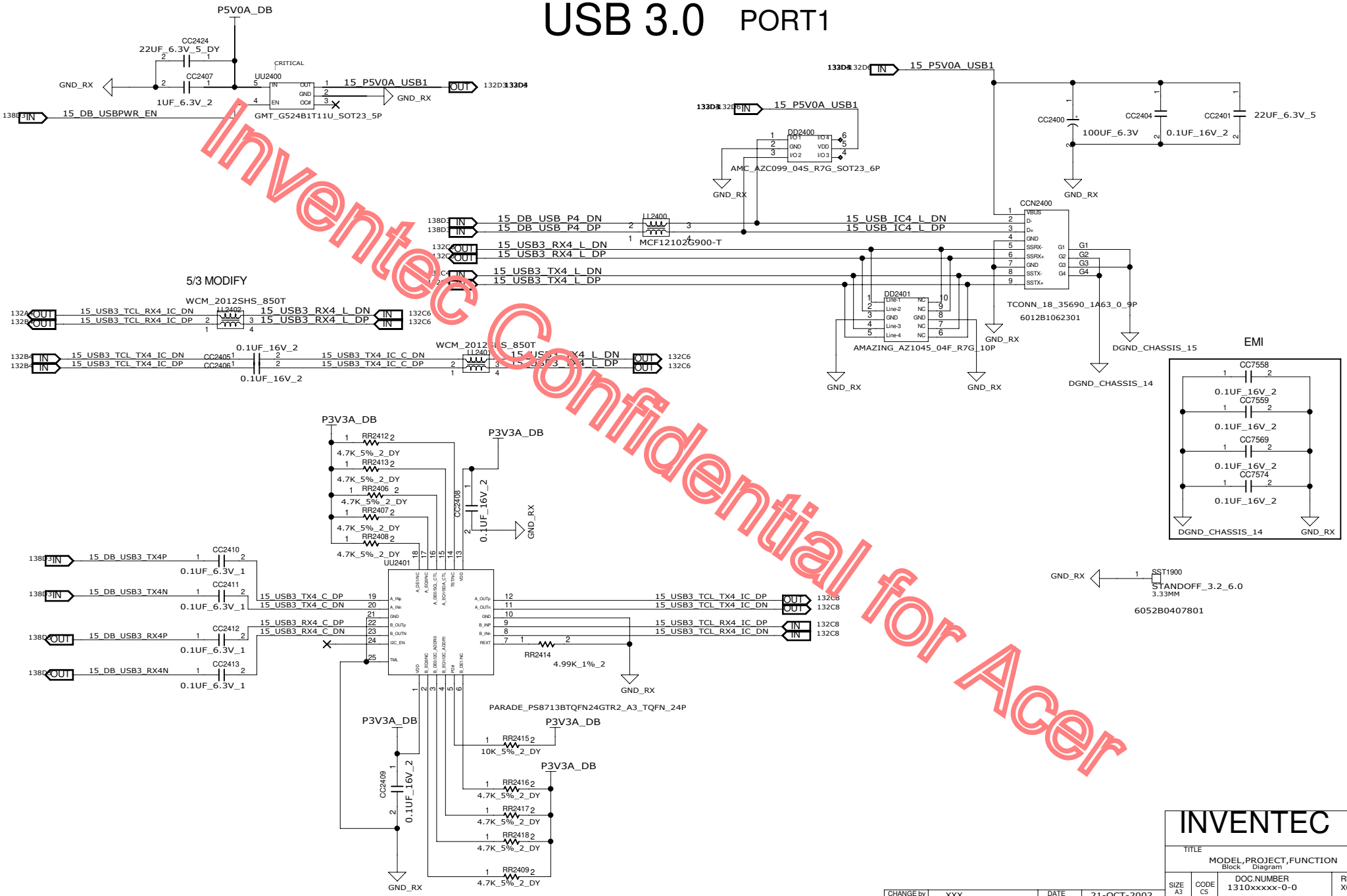
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 131 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

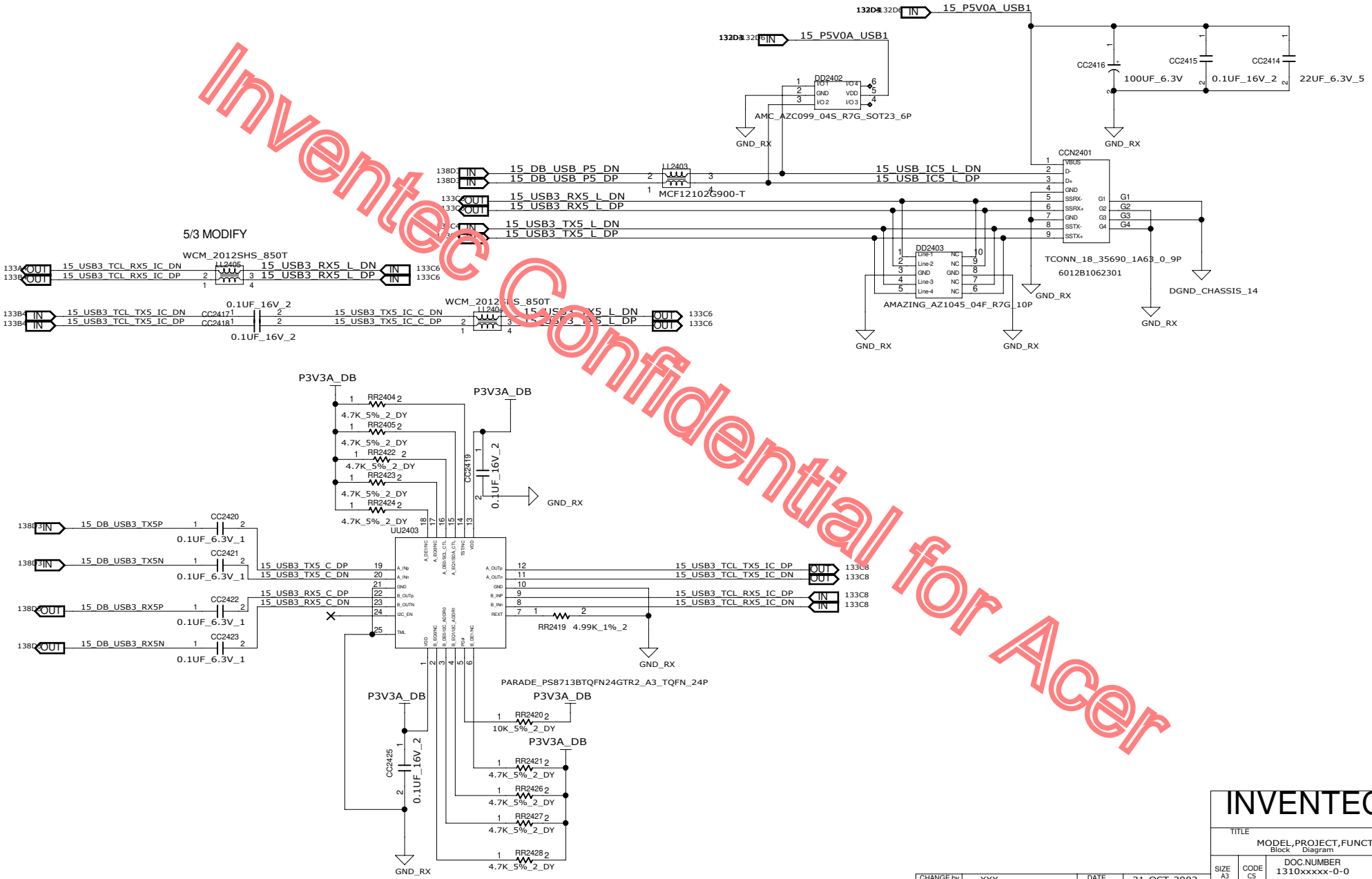
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 132 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



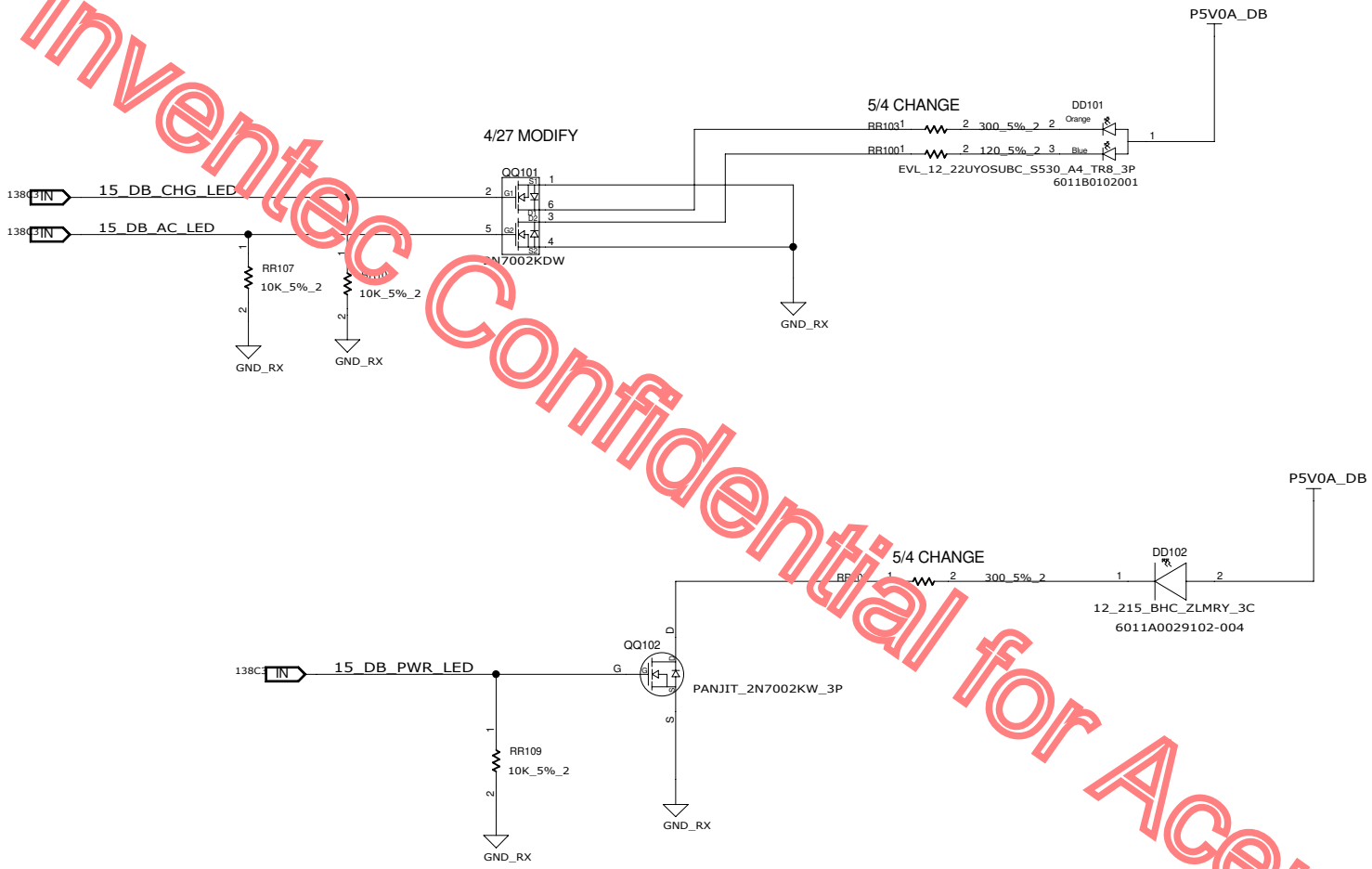
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 133 of 139



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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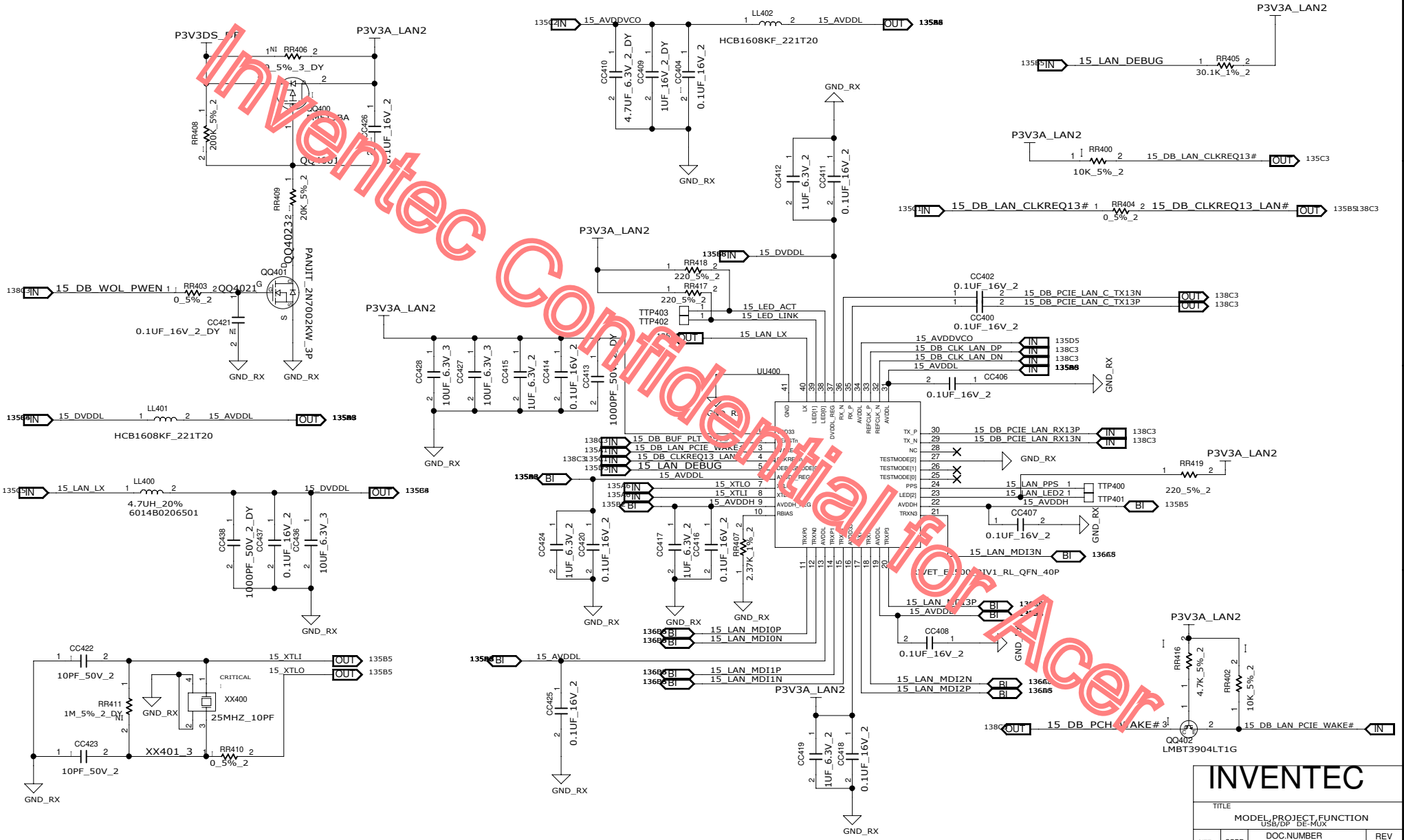
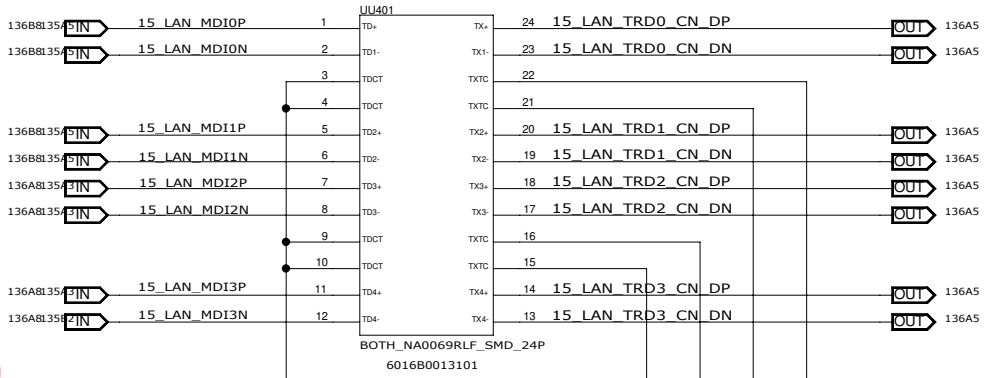
LAN (CONTROLLER)
E2500



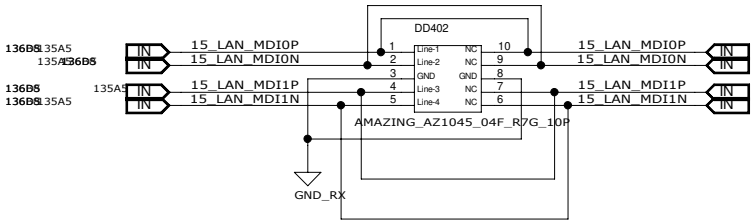
INVENTEC

TITLE	MODEL_PROJECT_FUNCTION		
	USB/DP DE-MUX		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX
SHEET	135 of 139		

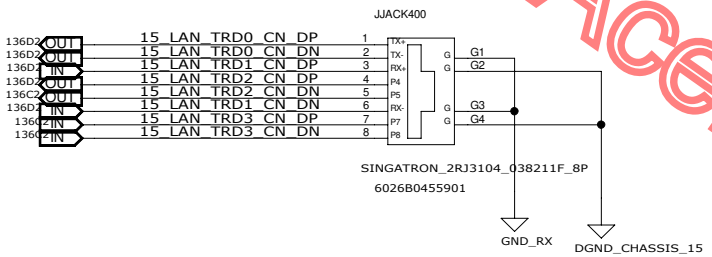
TRANSFORMER

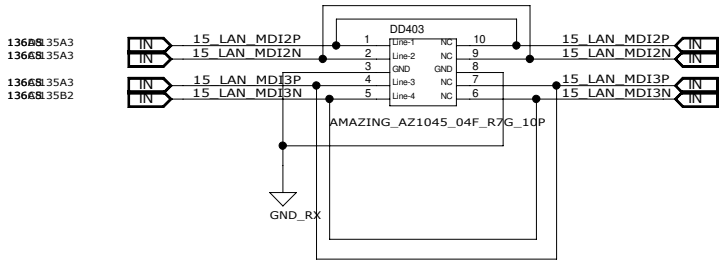


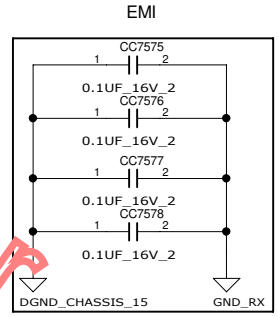
ESD



RJ-45



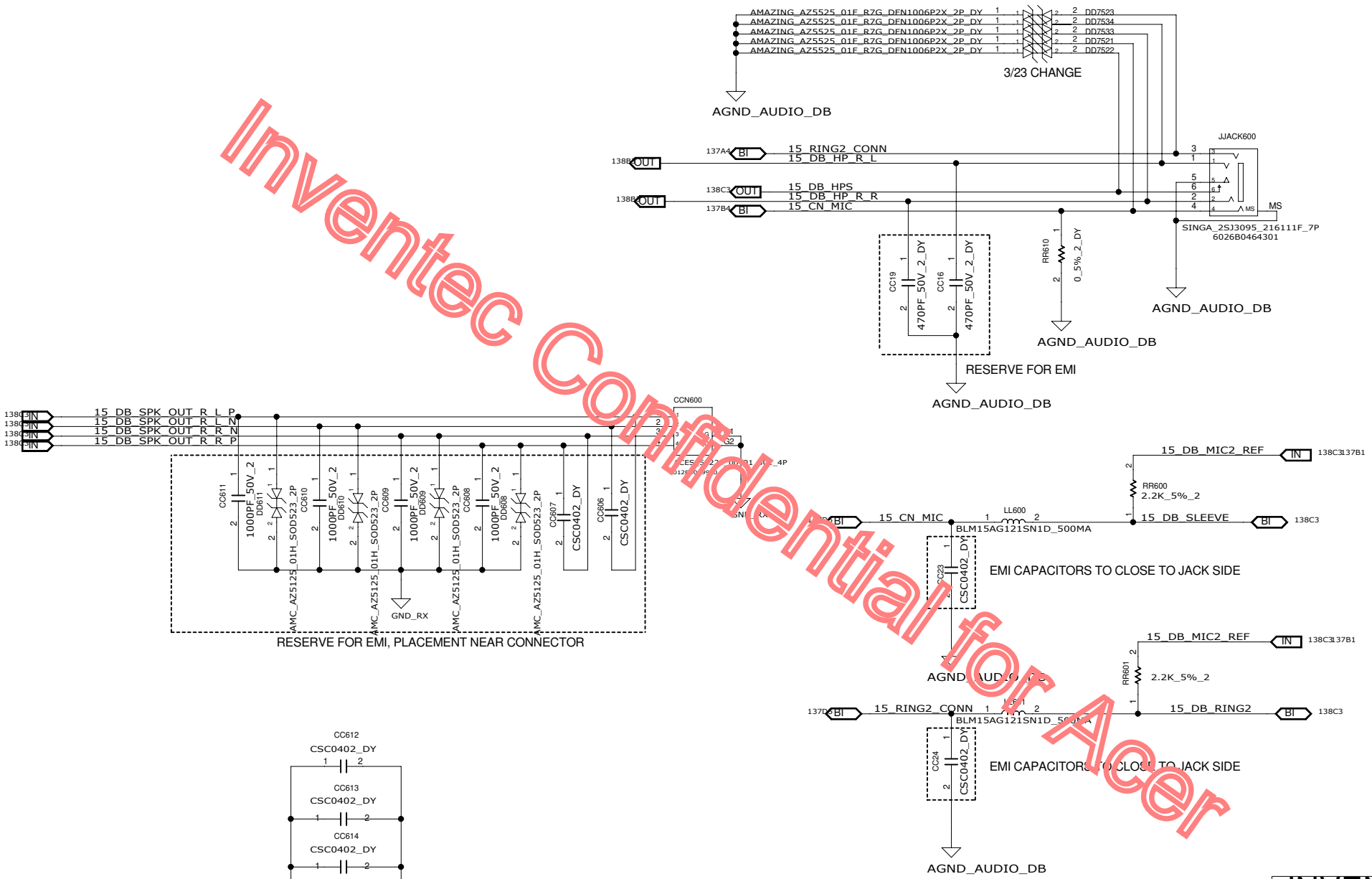




INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 136 of 139			

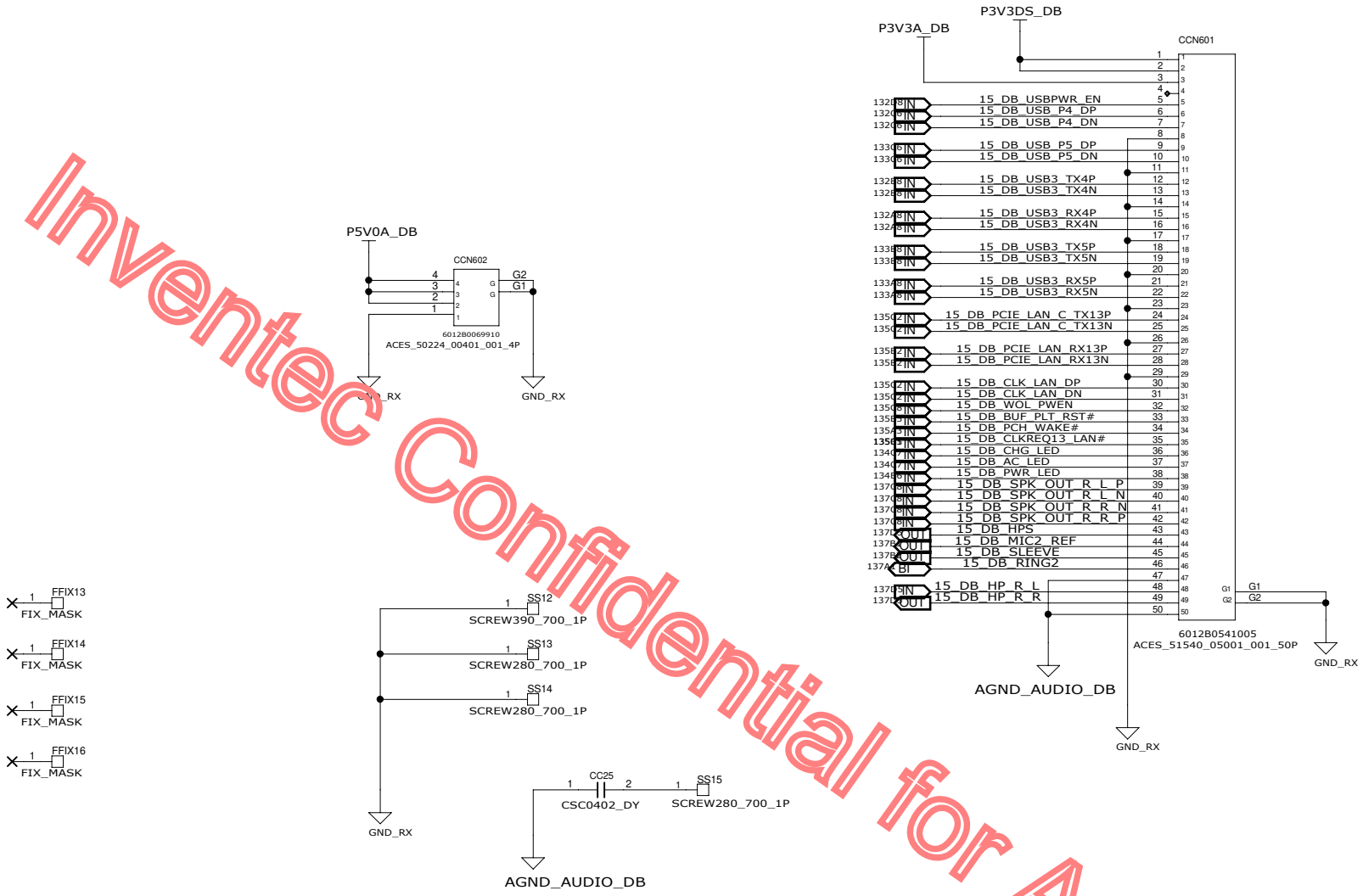
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 137 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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