

8	7	6	5	4	3	2	1																																		
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F								F																																	
E								E																																	
D								D																																	
C								C																																	
B								B																																	
A								A																																	
VELLFIRE 2020.06.05																																									
<table><tr><td colspan="3">INVENTEC</td></tr><tr><td colspan="3">TITLE MODEL, PROJECT, FUNCTION MAIN BOARD</td></tr><tr><td>DESIGN / DRAWER</td><td>XXX</td><td>DATE</td><td>21-OCT-2002</td></tr><tr><td>CHECK</td><td></td><td></td><td></td></tr><tr><td>APPROVAL</td><td></td><td></td><td></td></tr><tr><td>FILE NAME</td><td></td><td></td><td></td></tr><tr><td>PCB P/N</td><td>60xxxxxxxxxx</td><td>PCB VER</td><td>XXX</td></tr><tr><td>SIZE A3</td><td>CODE CS</td><td>DOC NUMBER 1310xxxxx-0-0</td><td>REV X01</td></tr><tr><td colspan="2">SHEET 1</td><td colspan="2"># 139</td></tr></table>								INVENTEC			TITLE MODEL, PROJECT, FUNCTION MAIN BOARD			DESIGN / DRAWER	XXX	DATE	21-OCT-2002	CHECK				APPROVAL				FILE NAME				PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	SHEET 1		# 139	
INVENTEC																																									
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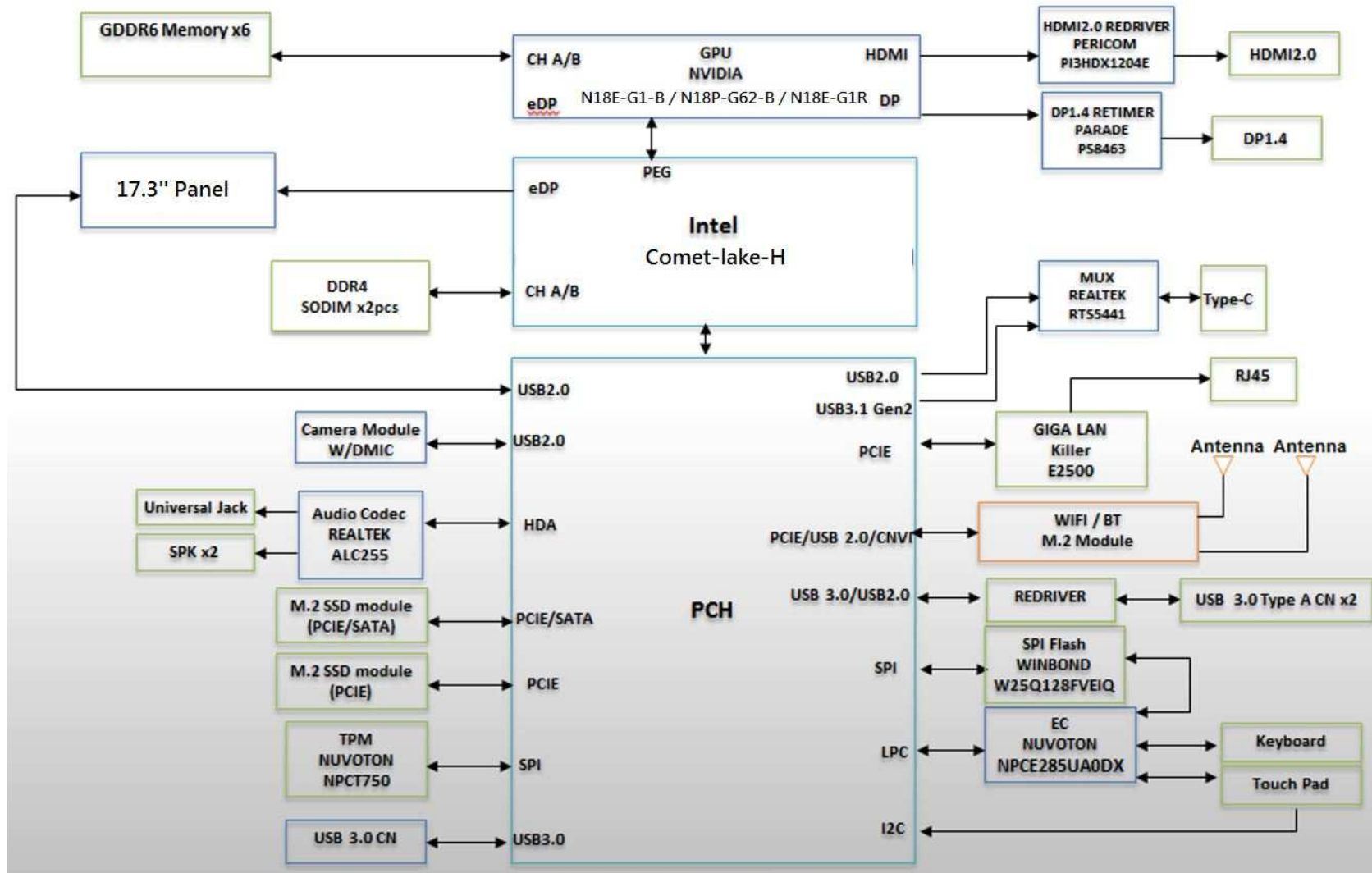
FOR 17 SMALL BOARD1&2

129.KB_BL
130.KB

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TITLE			
MODEL PROJECT FUNCTION			
TABLE OF THE CONTENT			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX



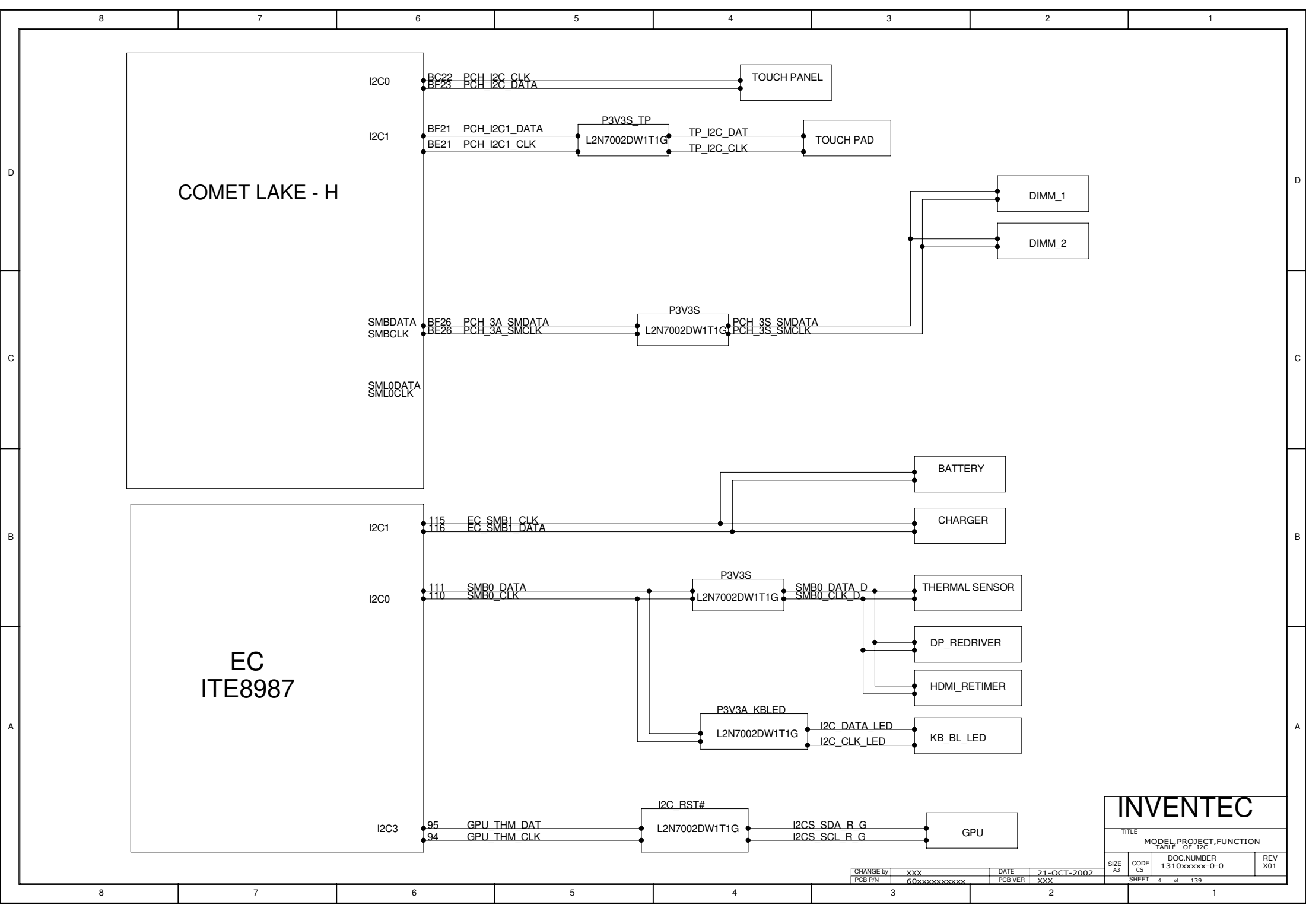
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TITLE MODEL PROJECT FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
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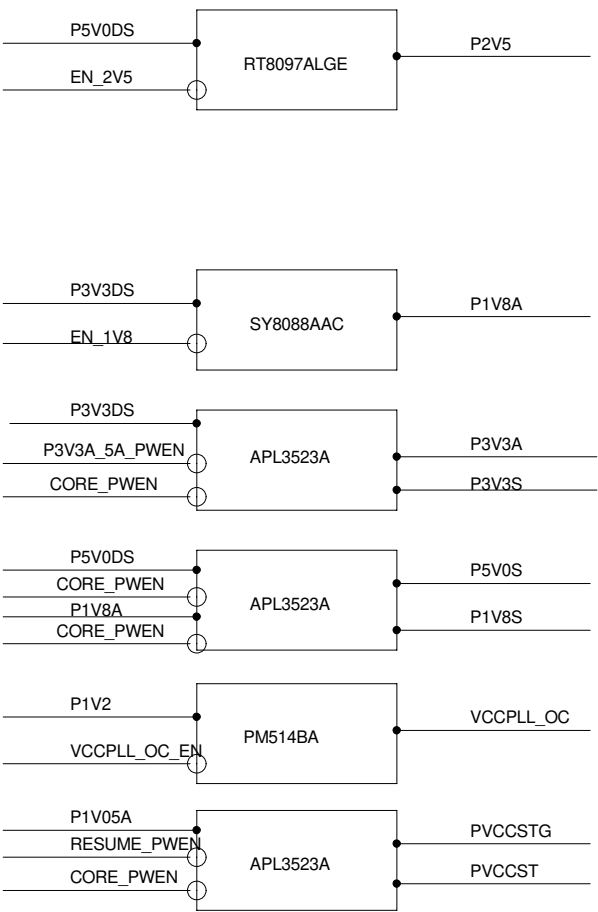
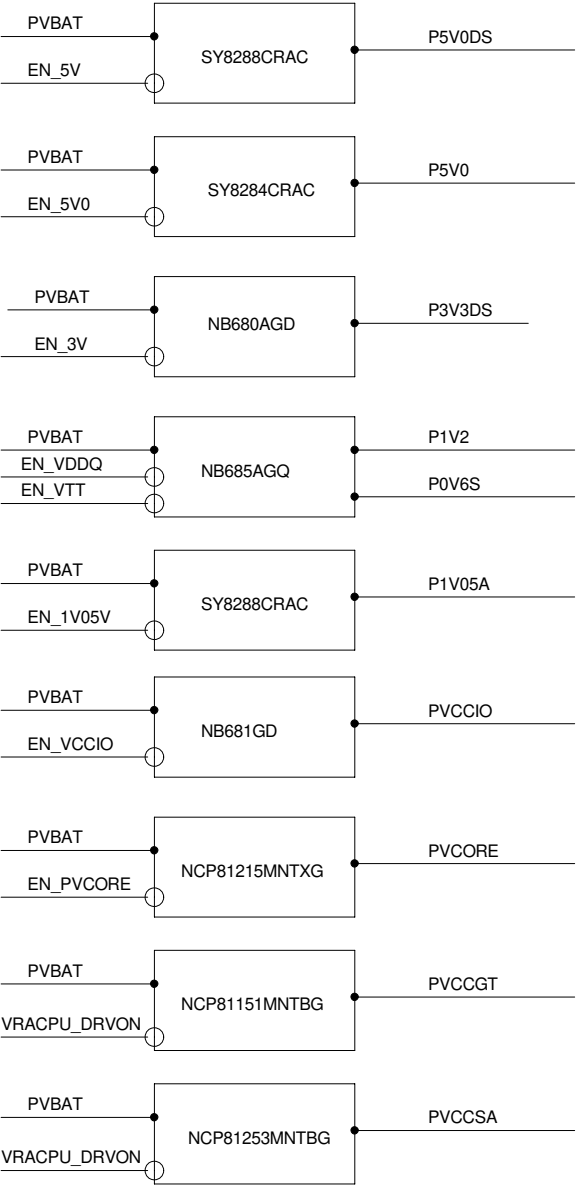
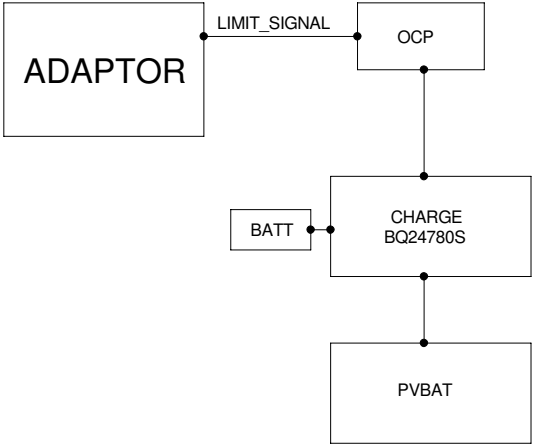


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SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 4 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

POWER BLOCK

IN/EN OUT IN/EN OUT

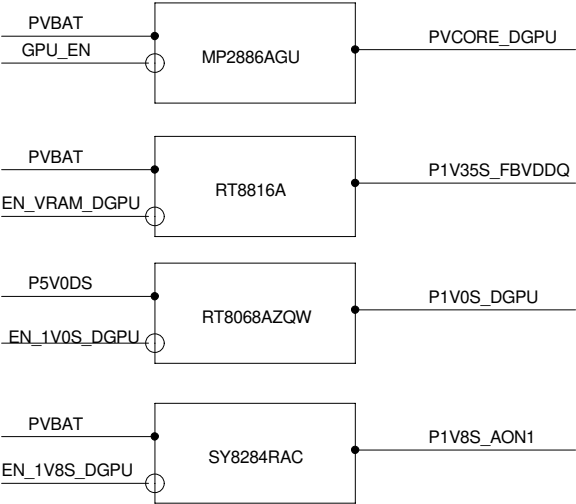


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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	5	of	139				

GPU POWER BLOCK

IN/EN OUT



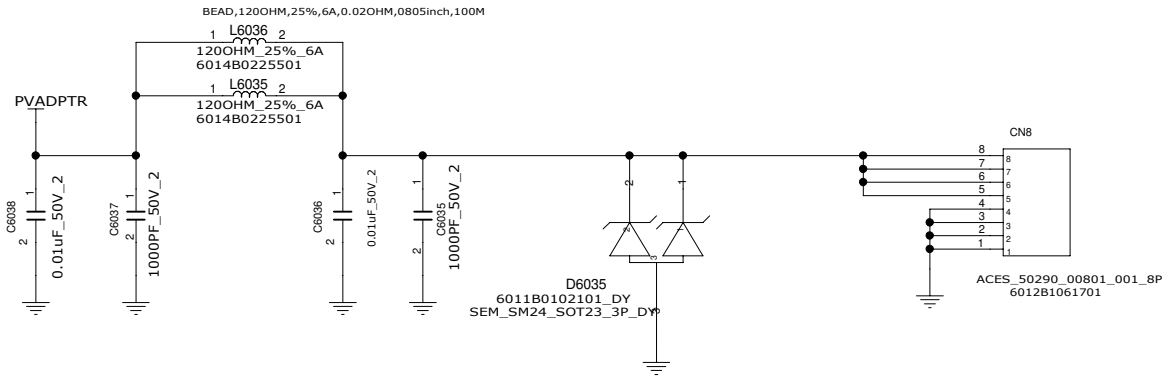
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TITLE
MODEL PROJECT, FUNCTION
TABLE OF 12C

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

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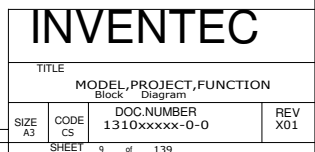
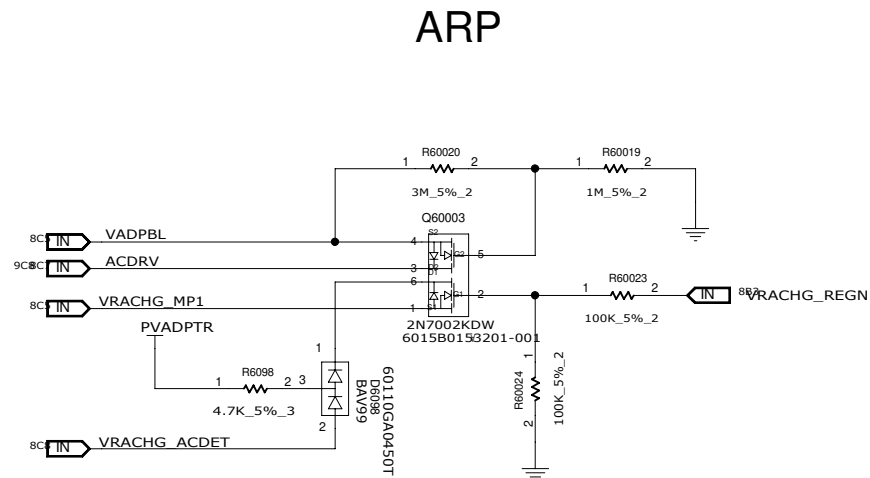
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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

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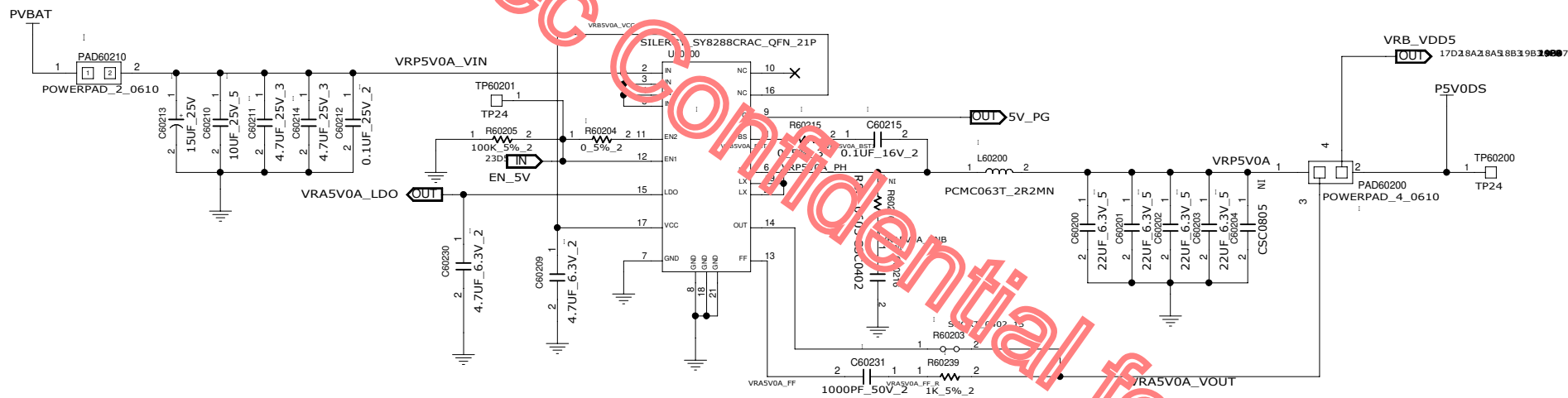
CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

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[illegible]

CHANGE by		XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
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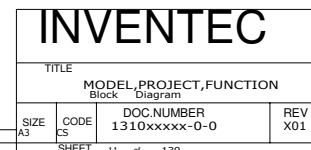
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TITLE
MODEL PROJECT,FUNCTION
P5V0DS

SIZE A3 CODE CS 1310xxxx-0-0 REV X01

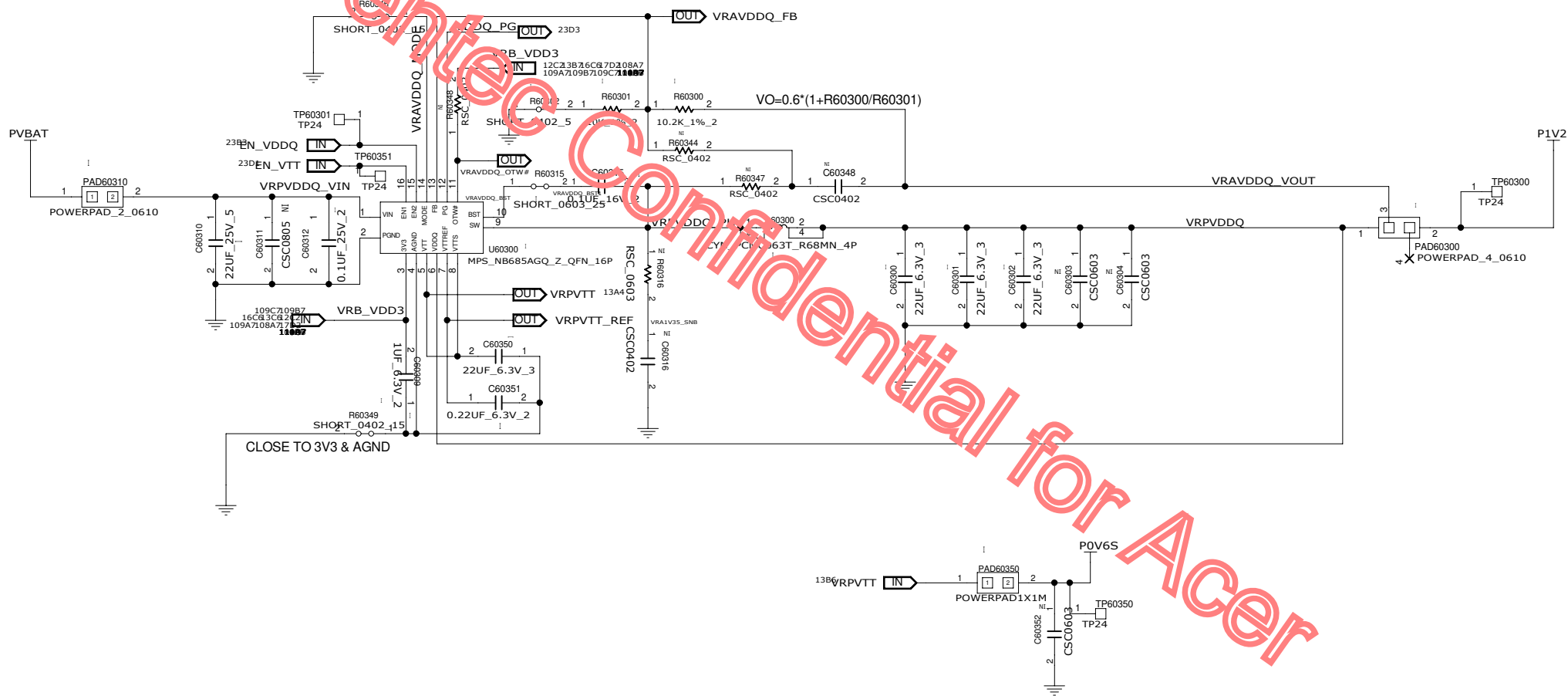
CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

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gh	High	ON	ON	ON
w	High	ON	ON	OFF(High-Z)
w	Low	OFF	OFF	OFF
gh	Low	OFF	OFF	OFF

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



TITLE	MODEL,PROJECT,FUNCTION
VDDO	

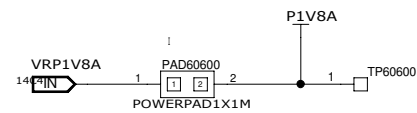
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CHANGE by	XXX
PCB P/N	60xxxxxxxxxxxx

DATE	21-OCT-2002
PCB VER	XXX

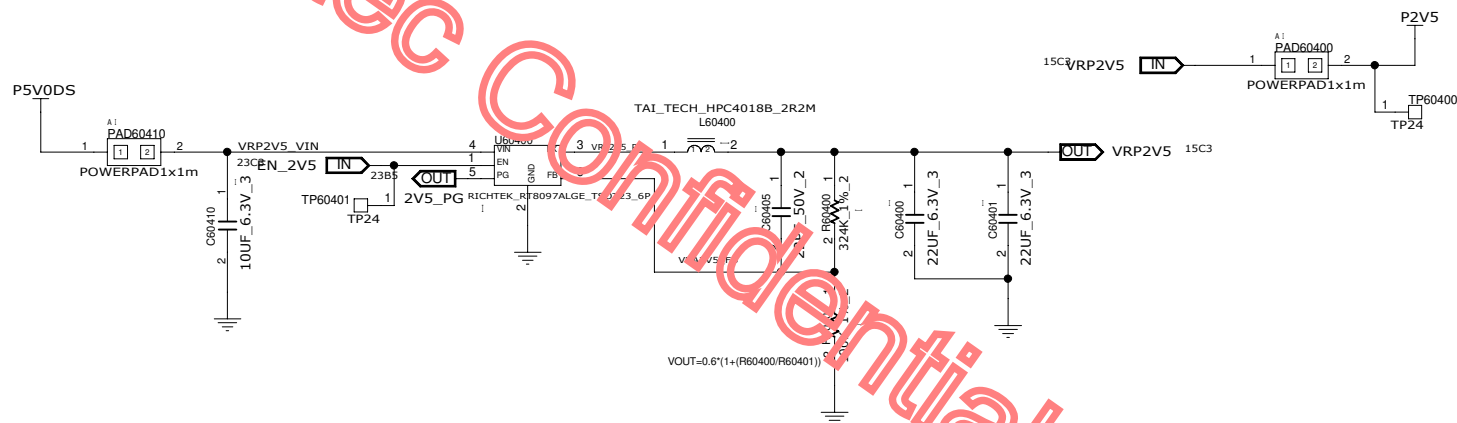
A3	CS	13 of 139	
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INVENTEC			
TITLE MODEL,PROJECT,FUNCTION P1VBDS			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 14 of 139			

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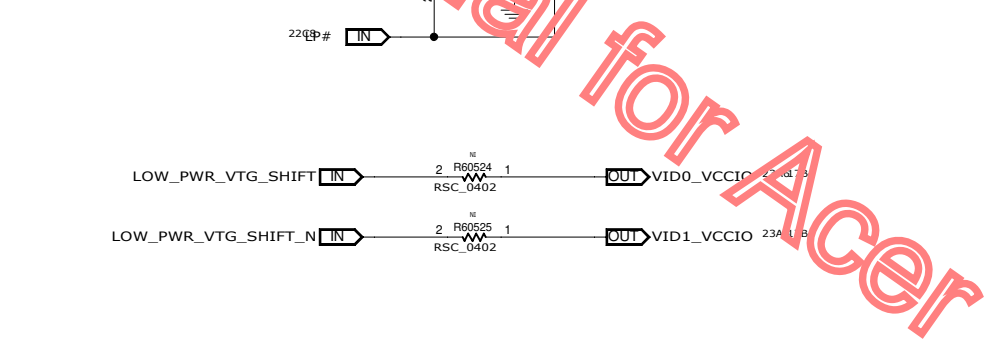
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TITLE			
MODEL, PROJECT, FUNCTION			
P2V5			
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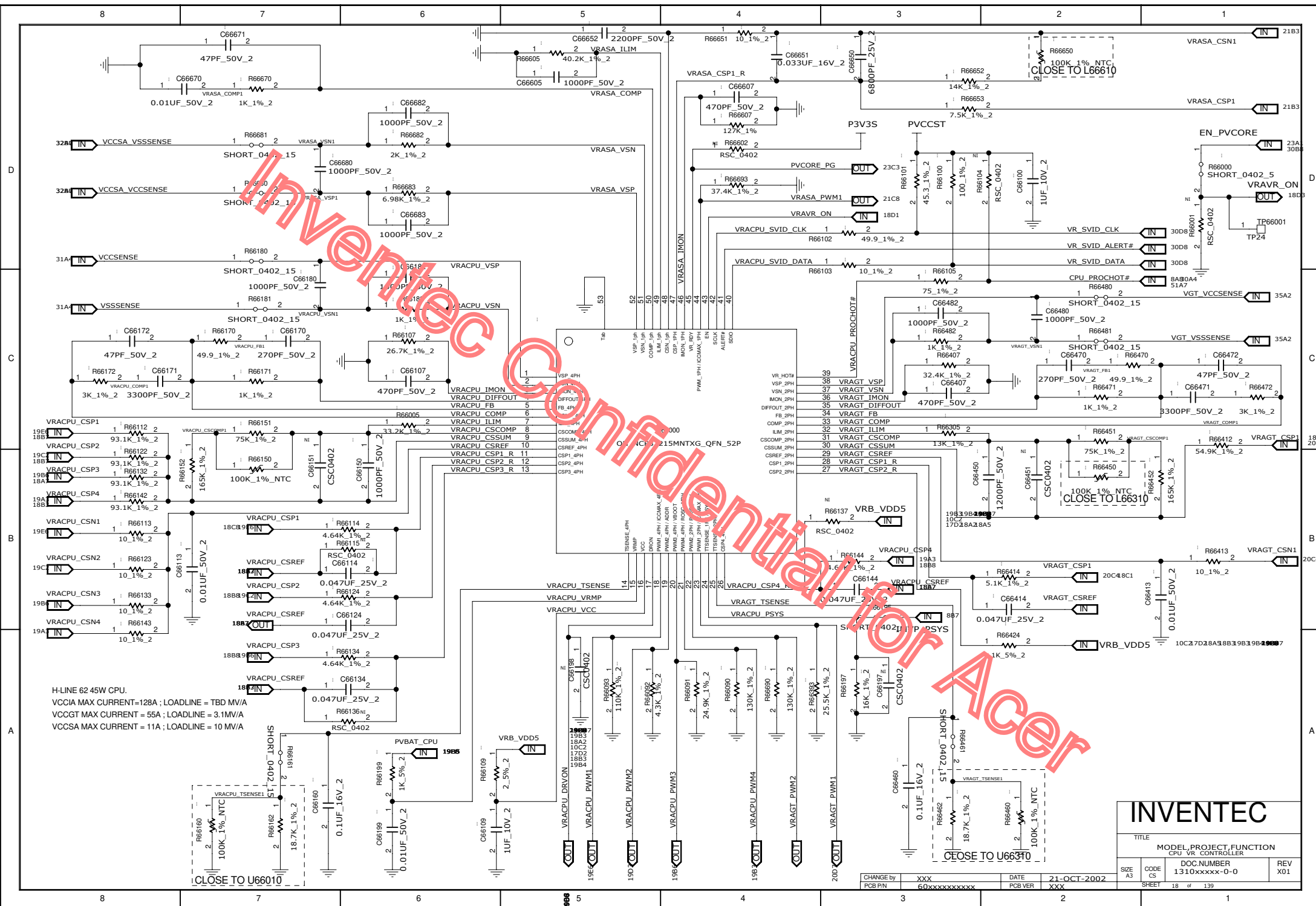
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

OPIC	100 K
	150 K

C1	C2	VOUT(V)
X	X	0.85
0	0	0.85
0	1	0.875
1	0	0.95

	1	1.00
X	X	0
0	0	0.8(MSM)
0	1	0.95
1	0	1
1	1	1.05
X	X	0
0	0	1.0
0	1	1.075
1	0	1.15
1	1	1.2

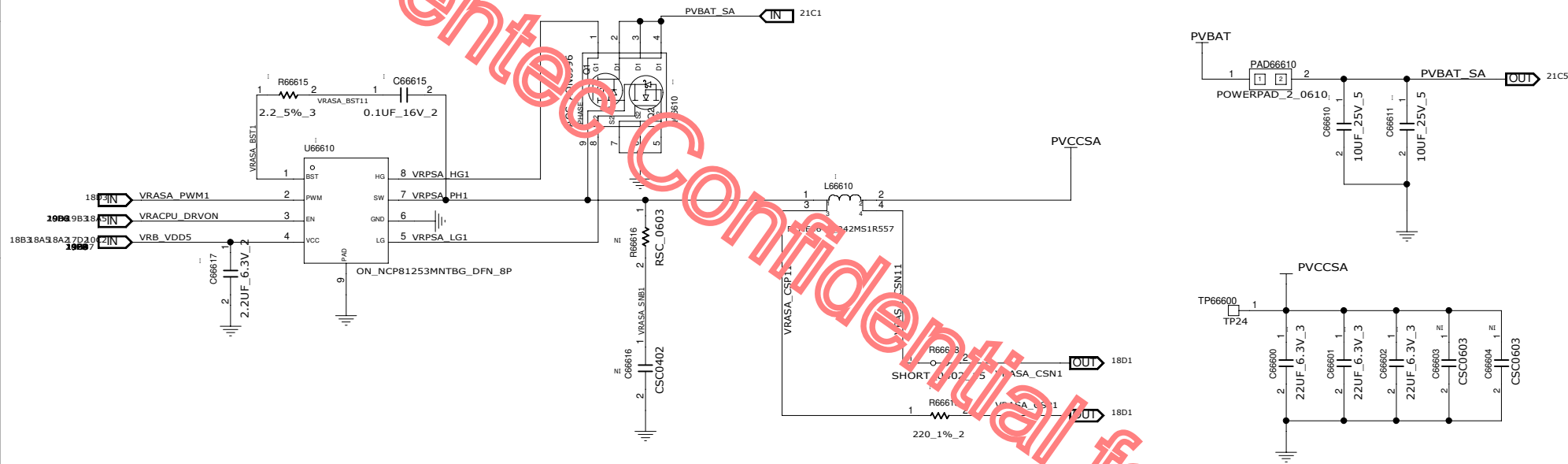




INVENTEC

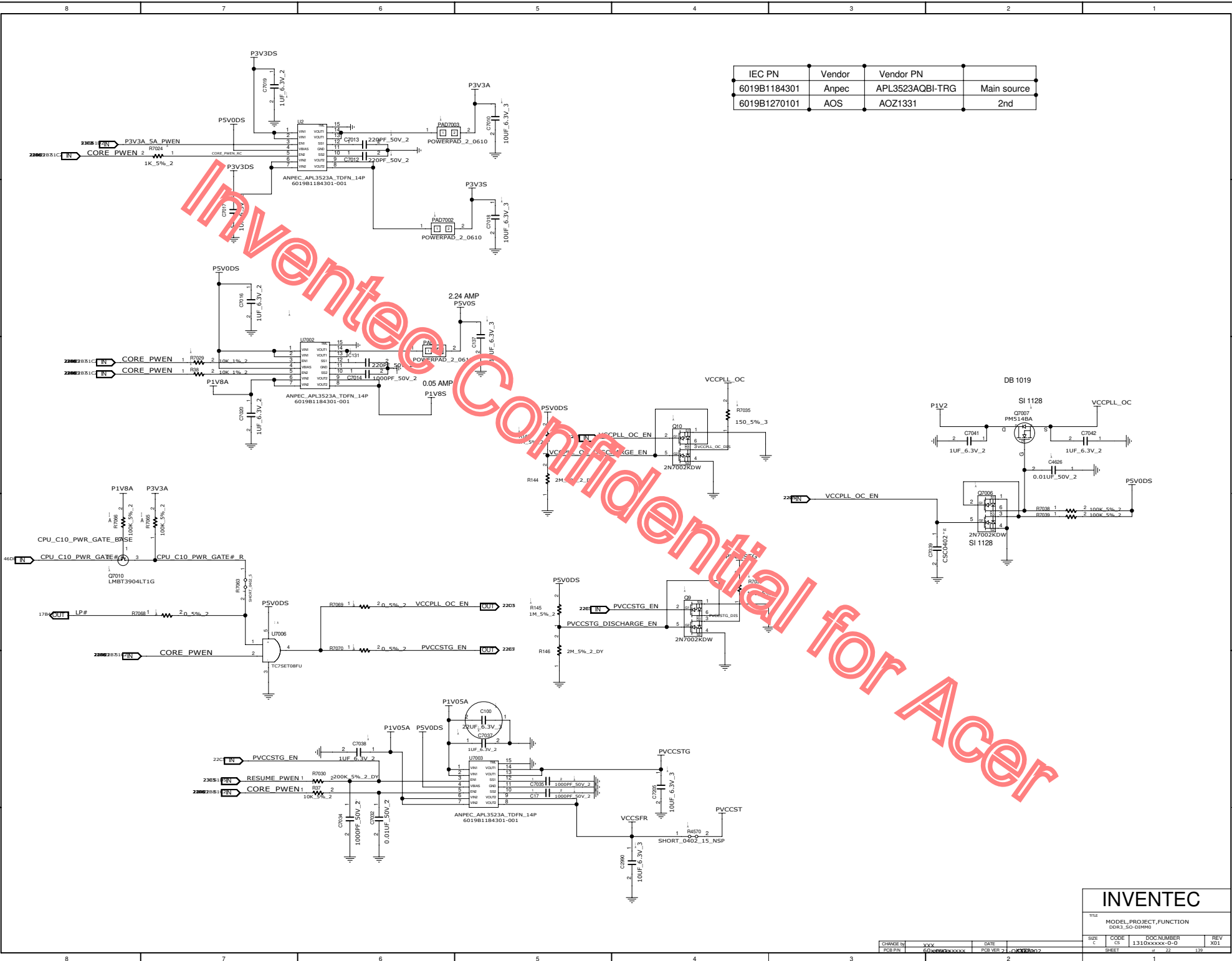
TITLE			
MODEL,PROJECT,FUNCTION CPU VR CONTROLLER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION PVCCSA				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0		REV X01
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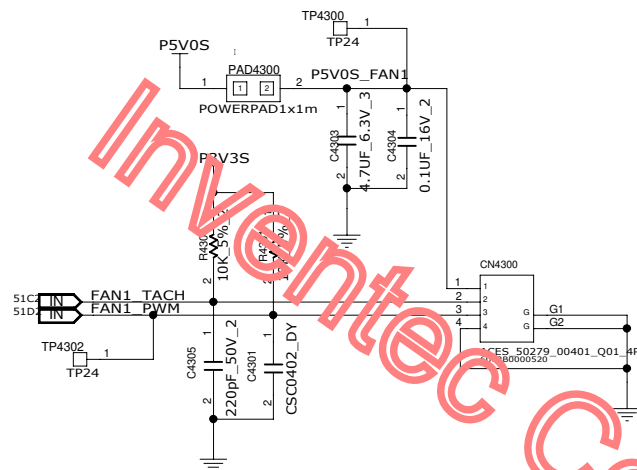
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PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



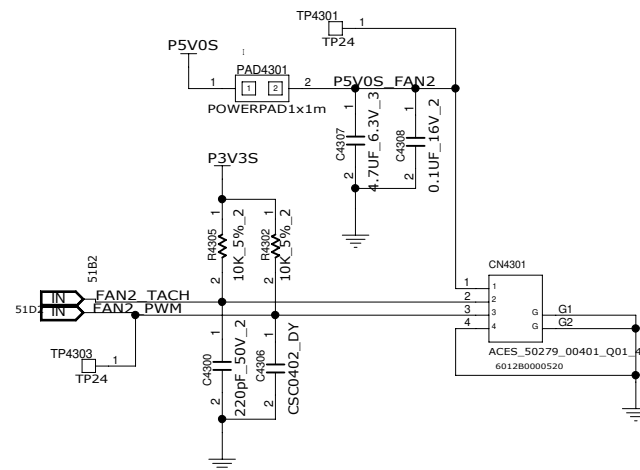
IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

FAN1 CN CPU

FAN2 CN CPU



FAN1 CN CPU



FAN2 CN_{CPU}

TITLE	MODEL, PROJECT, FUNCTION
	FAN & THERMAL

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 24 of 139			

REFERENCE 0~49(PCB SCREW)

1 FIX1
FIX_MASK
1 FIX2
FIX_MASK
1 FIX3
FIX_MASK
1 FIX4
FIX_MASK

1 FIX5
FIX_MASK
1 FIX6
FIX_MASK
1 FIX7
FIX_MASK
1 FIX8
FIX_MASK

1 S35
SCREW280_900_700_1P
1 S18
SCREW280_700_1P
1 S19
SCREW280_700_1P
1 S20
SCREW280_700_1P
1 S21
SCREW280_700_1P
1 S22
SCREW280_700_1P
1 S23
SCREW280_700_1P
1 S24
SCREW280_700_1P

1 S27
SCREW390_850_700_1P
1 S25
SCREW390_850_700_1P
1 S26
SCREW390_1160_850_1P
1 S11
SCREW280_900_550_NP_1P
1 S10
SCREW280_850_700_1P
1 S16
SCREW280_850_700_1P
1 S17
SCREW280_700_1P

PCB

1 S2
SCREW420_700_1P
1 S3
SCREW420_700_1P
1 S4
SCREW420_700_1P
1 S5
SCREW420_700_1P
1 S6
SCREW420_700_1P
1 S7
SCREW420_700_1P
1 S8
SCREW420_700_1P

INVENTEC

TITLE
MODEL PROJECT FUNCTION
XDP & ME CONN.

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

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D							
C							
B							
A							
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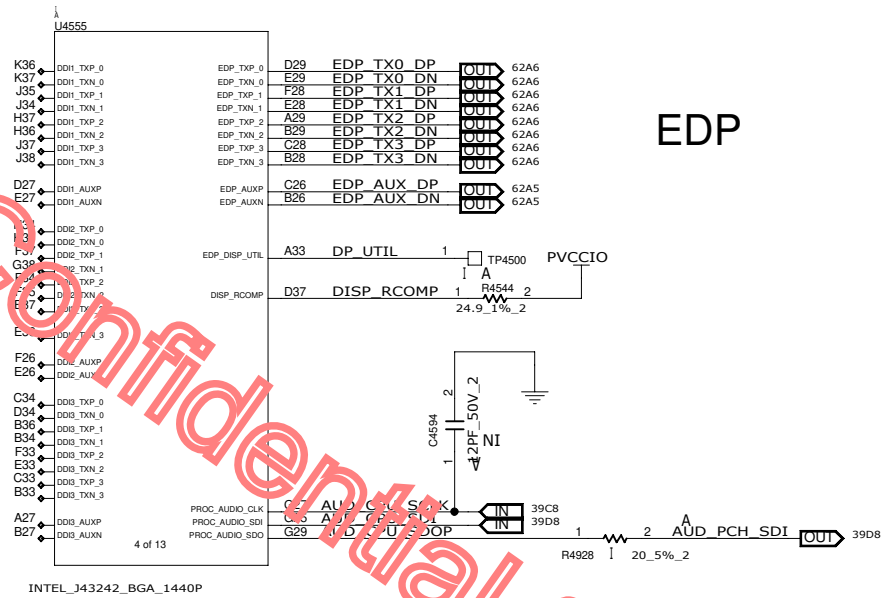
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J4555							
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74D7348IN	PCIE DGPU RX15P F10	PEG_RXP_15	C10 PEG TX15 DP C4887 2	10.22UF 6.3V 1	PCIE DGPU TX15P	73D84D7	
74D7348IN	PCIE DGPU RX15N E10	PEG_RXN_15	B10 PEG TX15 DN C4887 2	10.22UF 6.3V 1	PCIE DGPU TX15N	73D84D7	
PVCCIO 1A							
1 R4501 2 PEG_RCOMP G2		PEG_RCOMP					
24.9_1%_2							
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370CBI	DMI_RX0_DN E8	DMI_RXN_0	A8 DMI TX0 DN	37D6			
370CBI	DMI_RX1_DP E6	DMI_RXP_1	C6 DMI TX1 DP	37D6			
370CBI	DMI_RX1_DN F6	DMI_RXN_1	B6 DMI TX1 DN	37D6			
370CBI	DMI_RX2_DP D5	DMI_RXP_2	B5 DMI TX2 DP	37D6			
370CBI	DMI_RX2_DN E5	DMI_RXN_2	A5 DMI TX2 DN	37D6			
370CBI	DMI_RX3_DP J8	DMI_RXP_3	D4 DMI TX3 DP	37D6			
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3 OF 13							

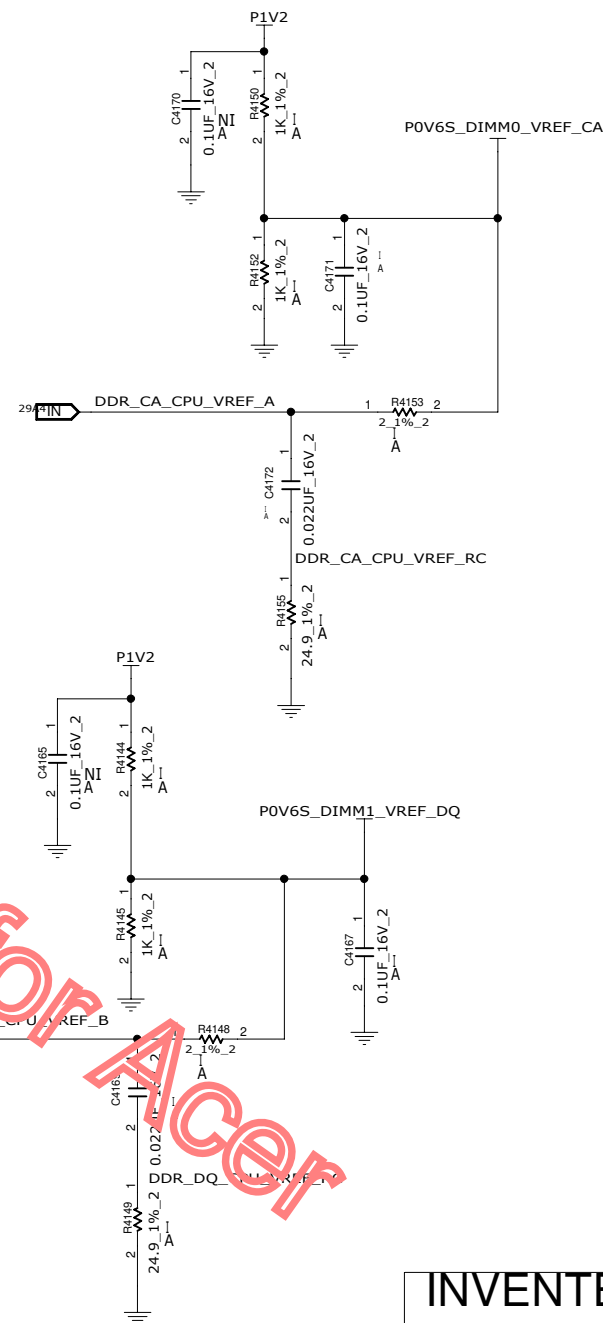
INTEL_J43242_BGA_1440P

INVENTEC			
TITLE			
MODEL PROJECT.FUNCTION SKYLAKE_L_H-PEG,HDMI			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	
XXX 60xxxxxxxxxxx		21-OCT-2002 XXX	
SHEET 26 of 139			

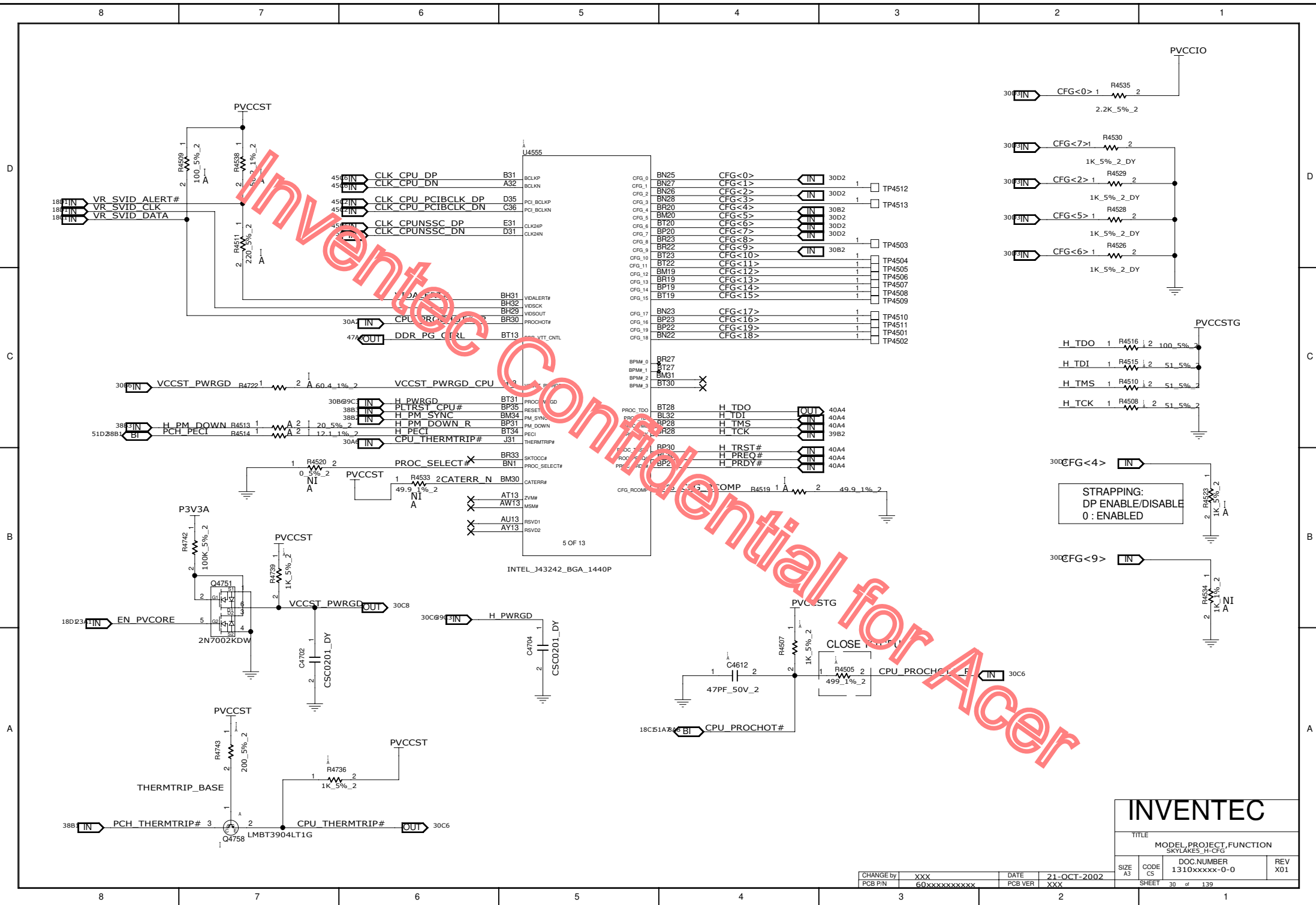
Inventec Confidential for Acer



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION SKYLAKE2_H-DD1,EDP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		27 of	139

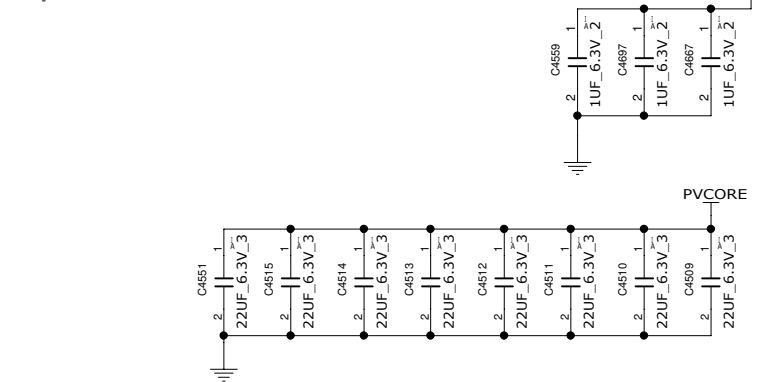
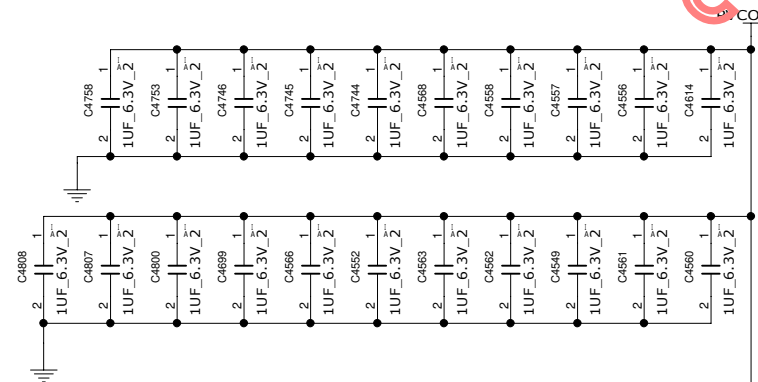
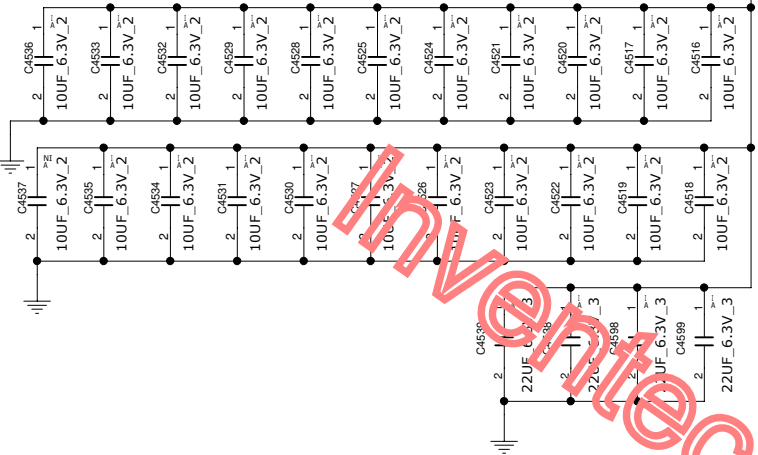


CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 29 of 139			



PLACE IN BACK SIDE

PVCORE



PVCORE

- AA13
- AA31
- AA32
- AA33
- AA34
- AA35
- AA36
- AA37
- AA38
- AB29
- AB30
- AB31
- AB32
- AB33
- AB34
- AB35
- AB36
- AB37
- AB38
- AC13
- AC14
- AC19
- AC24
- AC29
- AC30
- AC31
- AC32
- AC33
- AC34
- AC35
- AC36
- AD13
- AD14
- AE13
- AE14
- AE15
- AE16
- AE17
- AE18
- AE19
- AE20
- AE21
- AE22
- AE23
- AE24
- AE25
- AE26
- AE27
- AE28
- AE29
- AE30
- AE31
- AE32
- AE33
- AE34
- AE35
- AE36
- AE37
- AE38
- AF29
- AF30
- AF31
- AF32
- AF33
- AF34
- AF35
- AF36
- AF37
- AF38
- AG14
- AG31
- AG32
- AG33
- AG34
- AG35
- AG36

INTEL_J43242_BGA_1440P

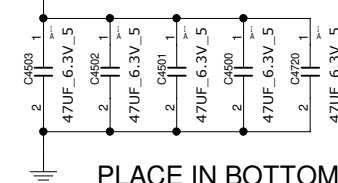
PVCORE

- U4555
- VCC04
- VCC05
- VCC06
- VCC07
- VCC08
- VCC09
- VCC10
- VCC11
- VCC12
- VCC13
- VCC14
- VCC15
- VCC16
- VCC17
- VCC18
- VCC19
- VCC20
- VCC21
- VCC22
- VCC23
- VCC24
- VCC25
- VCC26
- VCC27
- VCC28
- VCC29
- VCC30
- VCC31
- VCC32
- VCC33
- VCC34
- VCC35
- VCC36
- VCC37
- VCC38
- VCC39
- VCC40
- VCC41
- VCC42
- VCC43
- VCC44
- VCC45
- VCC46
- VCC47
- VCC48
- VCC49
- VCC50
- VCC51
- VCC52
- VCC53
- VCC54
- VCC55
- VCC56
- VCC57
- VCC58
- VCC59
- VCC60
- VCC61
- VCC62
- VCC63

VCC_SENSE
VSS_SENSE

AG37 VCCSENSE
AG38 VSSSENSE

PVCORE



PLACE IN BOTTOM SIDE

EDS VER0.7

PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24

PVCORE

- K14
- L13
- L14
- N13
- N14
- N30
- N31
- N32
- N35
- N36
- N37
- N38
- P13
- P29
- P30
- P31
- P32
- P33
- P34
- P35
- P36
- R13
- R31
- R32
- R33
- R34
- R35
- R36
- R37
- R38
- T29
- T30
- T31
- T32
- T35
- T36
- T37
- T38
- U29
- U30
- U31
- U32
- U33
- U34
- U35
- U36
- V13
- V31
- V32
- V33
- V34
- V35
- V36
- V37
- W13
- W14
- W29
- W30
- W31
- W32

10 OF 13

INTEL_J43242_BGA_1440P

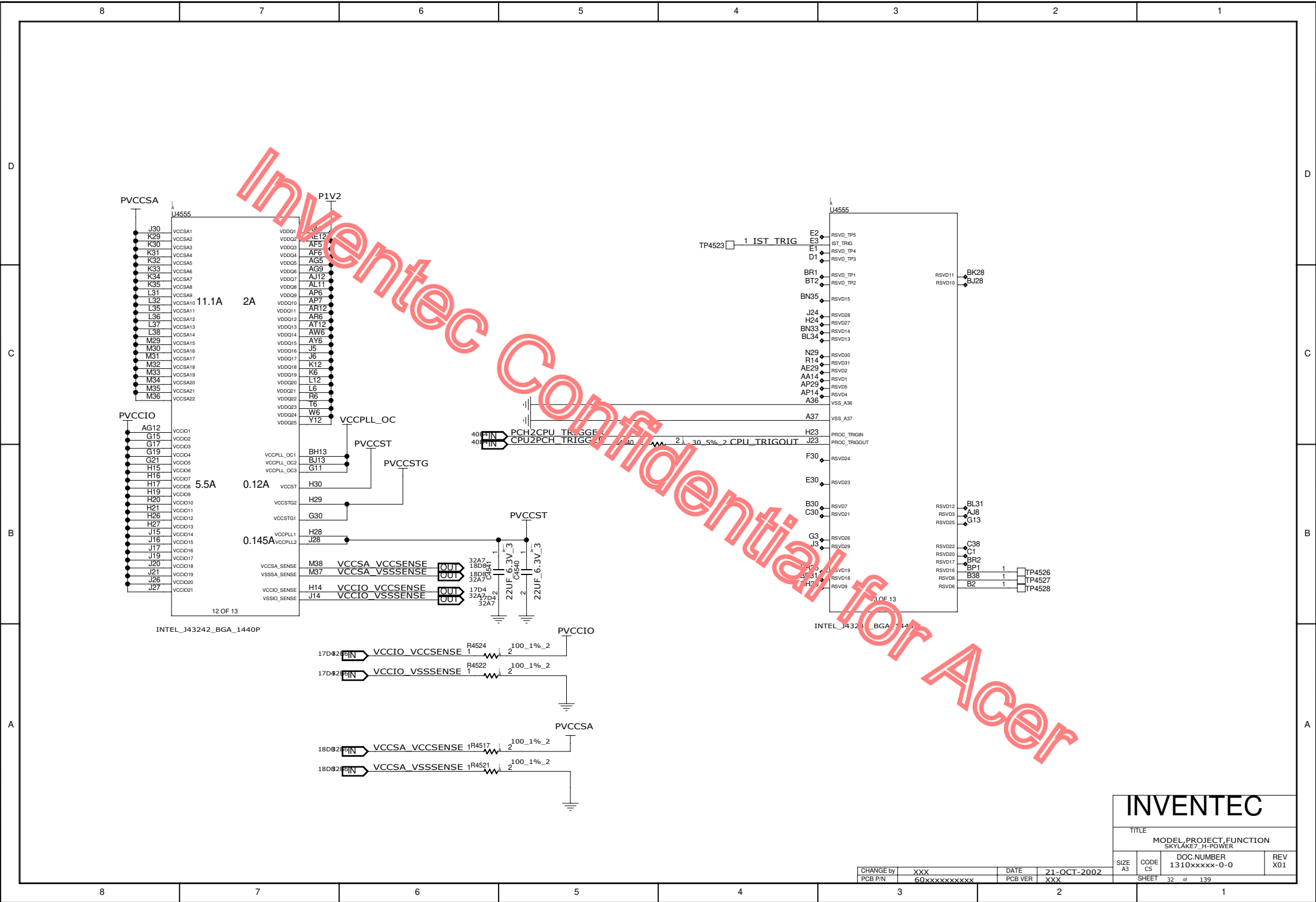
INVENTEC

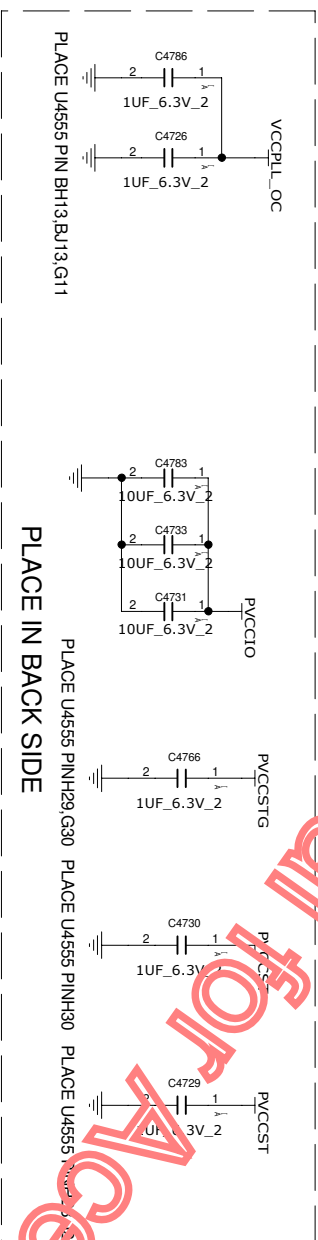
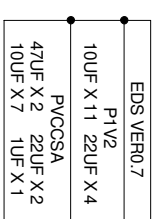
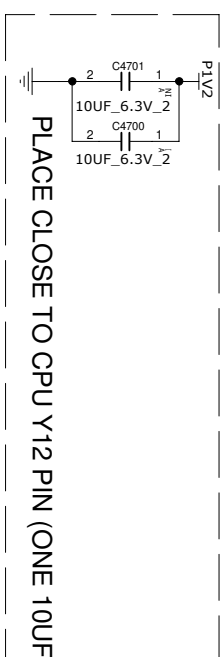
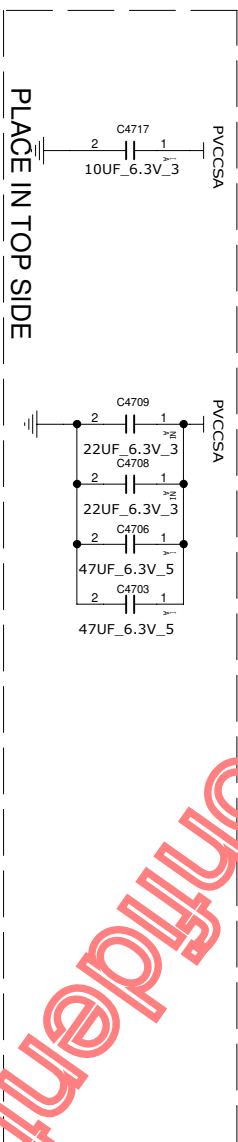
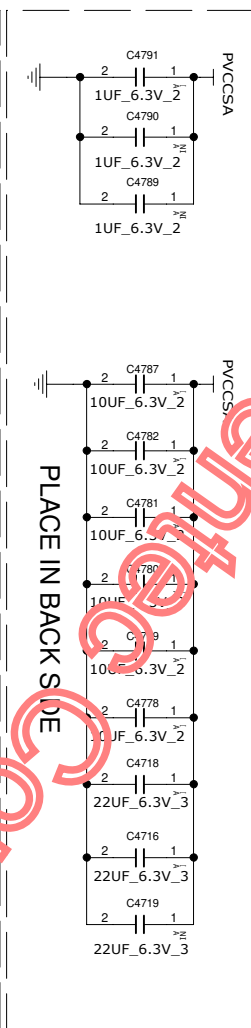
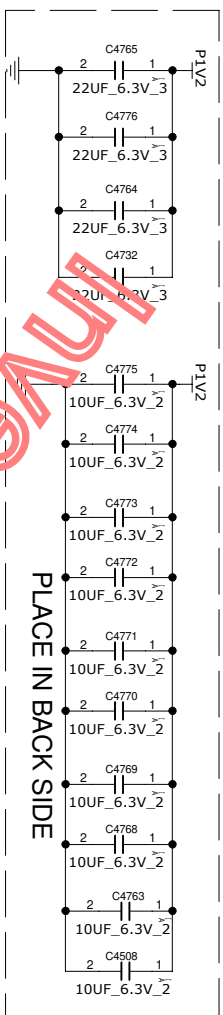
TITLE
MODEL PROJECT FUNCTION
SKYLAKES_HI-POWER

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

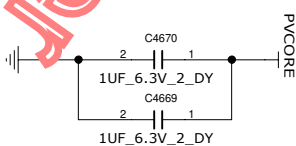
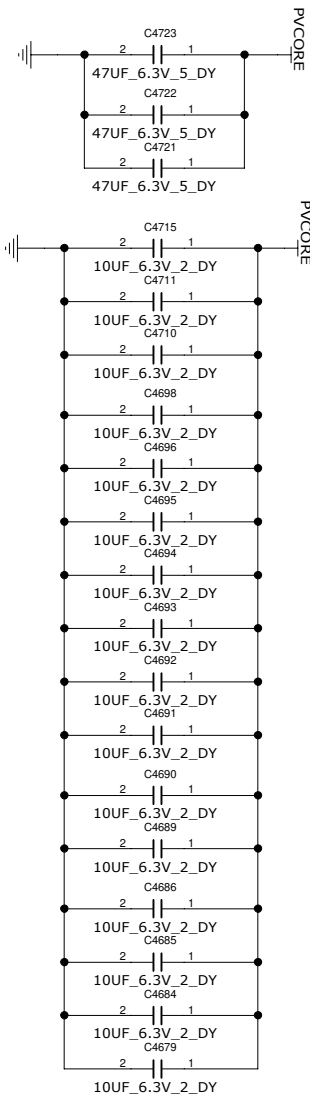
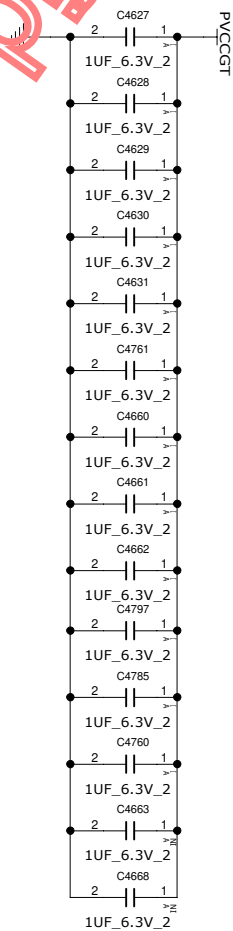
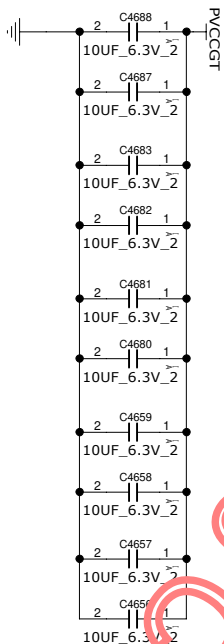
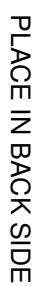
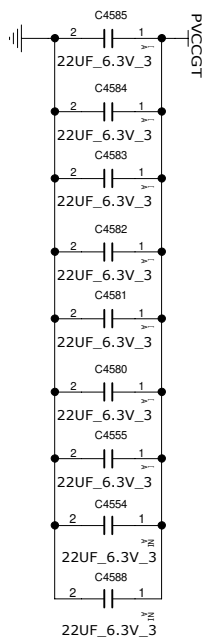
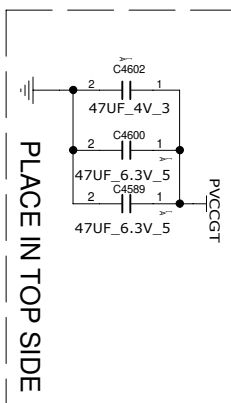
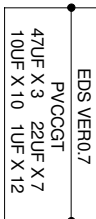
SHEET 31 of 139





CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION STRIPPER, H-BE-DECOUPLING			
SIZE A3	CODE CS	DOC,NUMBER 1310xxxx-0-0	REV X01
SHEET		33	of 139



H82 CPU

10UF_6.3V_2_DY
C4711

2 1

10UF_6.3V_2_DY
C4710

2 1

10UF_6.3V_2_DY
C4698

2 1

10UF_6.3V_2_DY
C4696

2 1

10UF_6.3V_2_DY
C4695

2 1

10UF_6.3V_2_DY
C4694

2 1

10UF_6.3V_2_DY
C4693

2 1

10UF_6.3V_2_DY
C4692

2 1

10UF_6.3V_2_DY
C4691

2 1

10UF_6.3V_2_DY
C4690

2 1

10UF_6.3V_2_DY
C4689

2 1

10UF_6.3V_2_DY
C4686

2 1

10UF_6.3V_2_DY
C4685

2 1

10UF_6.3V_2_DY
C4684

2 1

10UF_6.3V_2_DY
C4679

2 1

10UF_6.3V_2_DY

H82 CPU

2 1

10UF_6.3V_2_DY

PVCOR

C4670

2 1

2 C4683 1

10UF_6.3V_2

2 C4682 1

10UF_6.3V_2

2 C4681 1

10UF_6.3V_2

2 C4680 1

10UF_6.3V_2

2 C4659 1

10UF_6.3V_2

2 C4658 1

10UF_6.3V_2

2 C4657 1

10UF_6.3V_2

2 C4656 1

10UF_6.3V_2

PVCCGT

2 C4627 1

1UF_6.3V_2

2 C4628 1

1UF_6.3V_2

2 C4629 1

1UF_6.3V_2

2 C4630 1

1UF_6.3V_2

2 C4631 1

1UF_6.3V_2

2 C4761 1

1UF_6.3V_2

2 C4660 1

1UF_6.3V_2

2 C4661 1

1UF_6.3V_2

2 C4662 1

1UF_6.3V_2

2 C4797 1

1UF_6.3V_2

2 C4785 1

1UF_6.3V_2

2 1

2 C4585 1

22UF_6.3V_3

2 C4584 1

22UF_6.3V_3

2 C4583 1

22UF_6.3V_3

2 C4582 1

22UF_6.3V_3

2 C4581 1

22UF_6.3V_3

2 C4580 1

22UF_6.3V_3

2 C4555 1

22UF_6.3V_3

2 1

22UF_6.3V_3

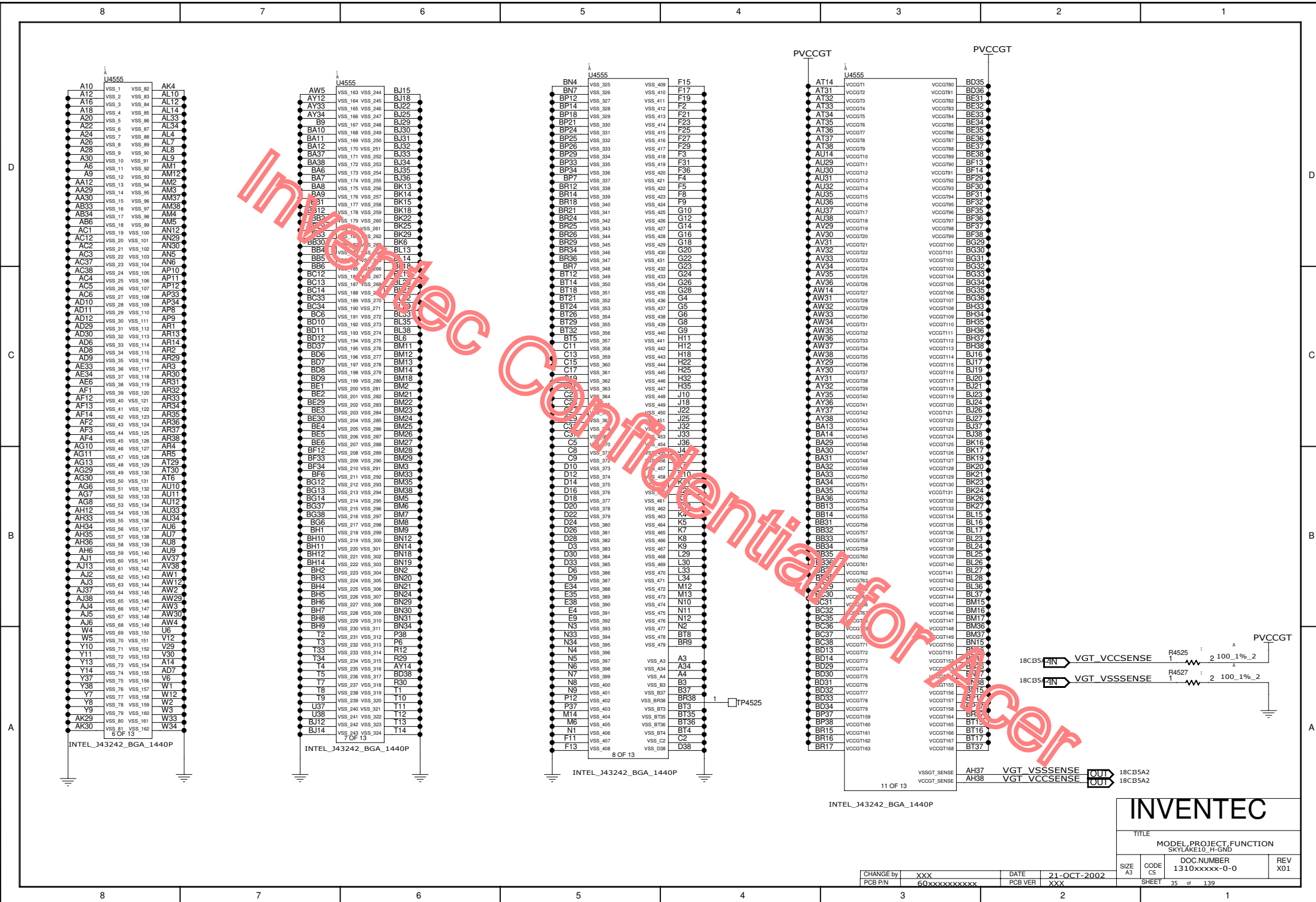
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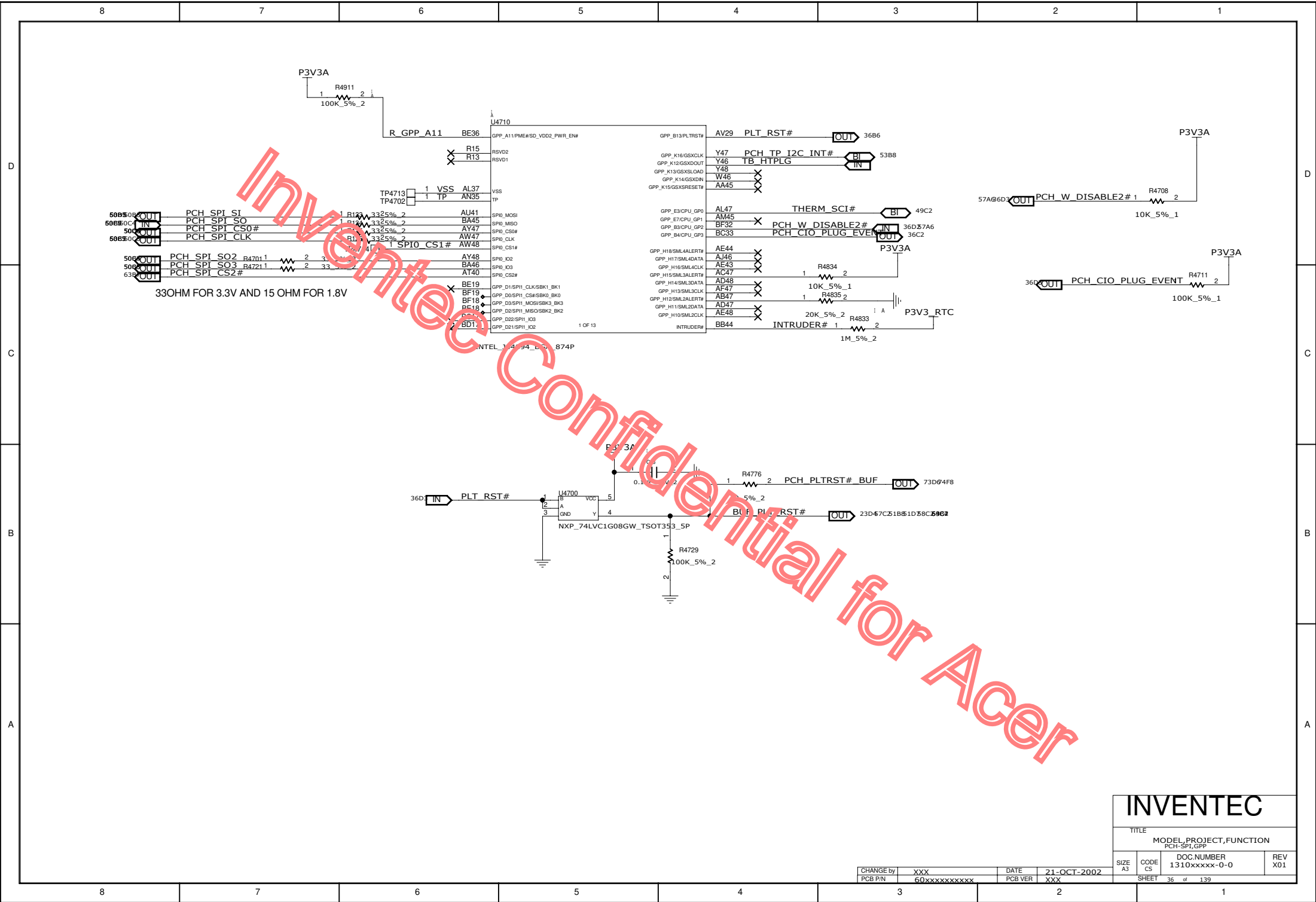
PLACE IN BOTTOM SIDE

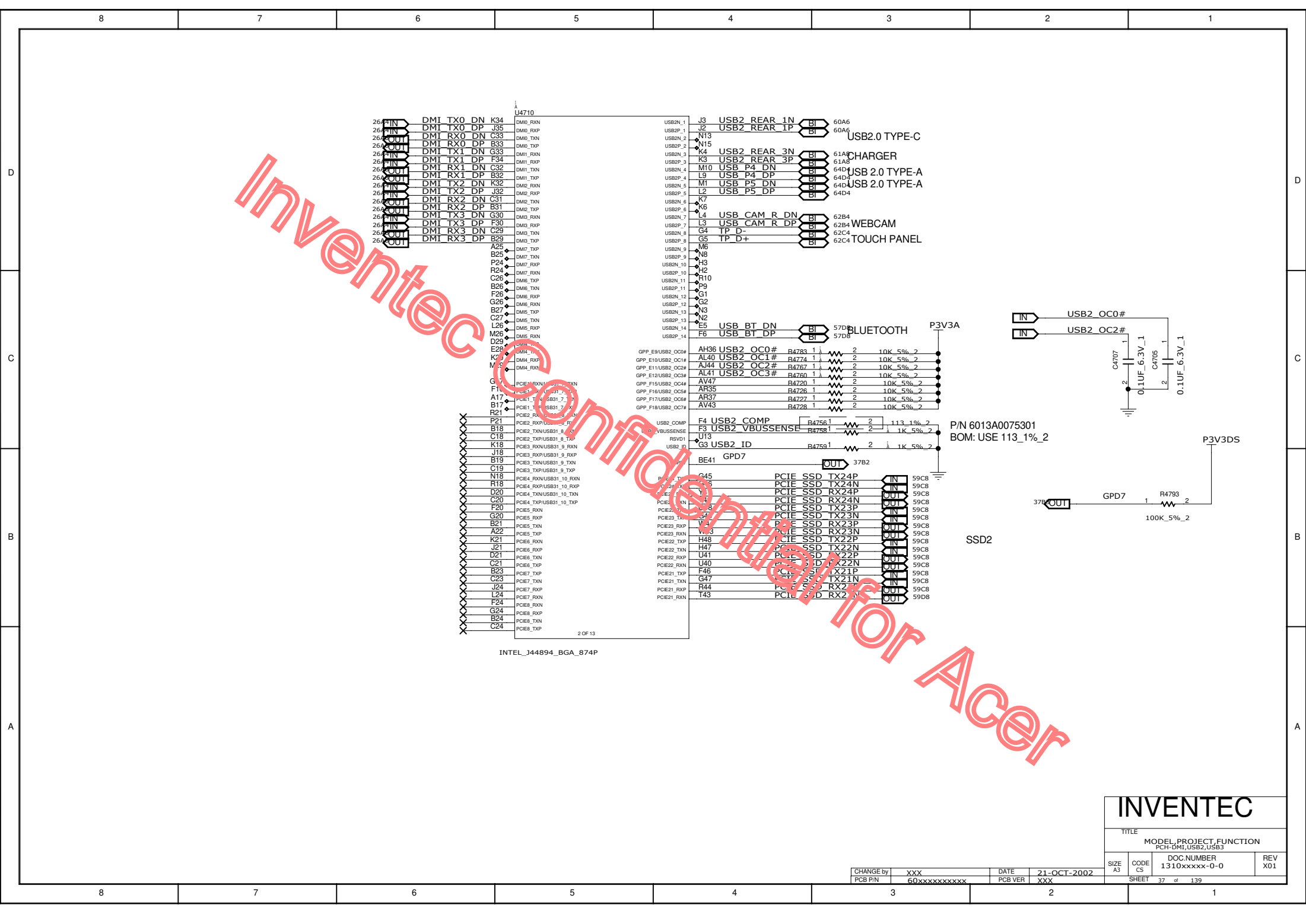
CHANGE by	XXX	DATE	21-OCT-2002	A3	5	
PCB P/N	60XXXXXXXXXX	PCB VER	XXX			
				SHEET 34 of 139		

INVENTEC

MODEL PROJECT FUNCTION SKYLAKES9_H-GT DECOUPLING		
CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SIZE A3		



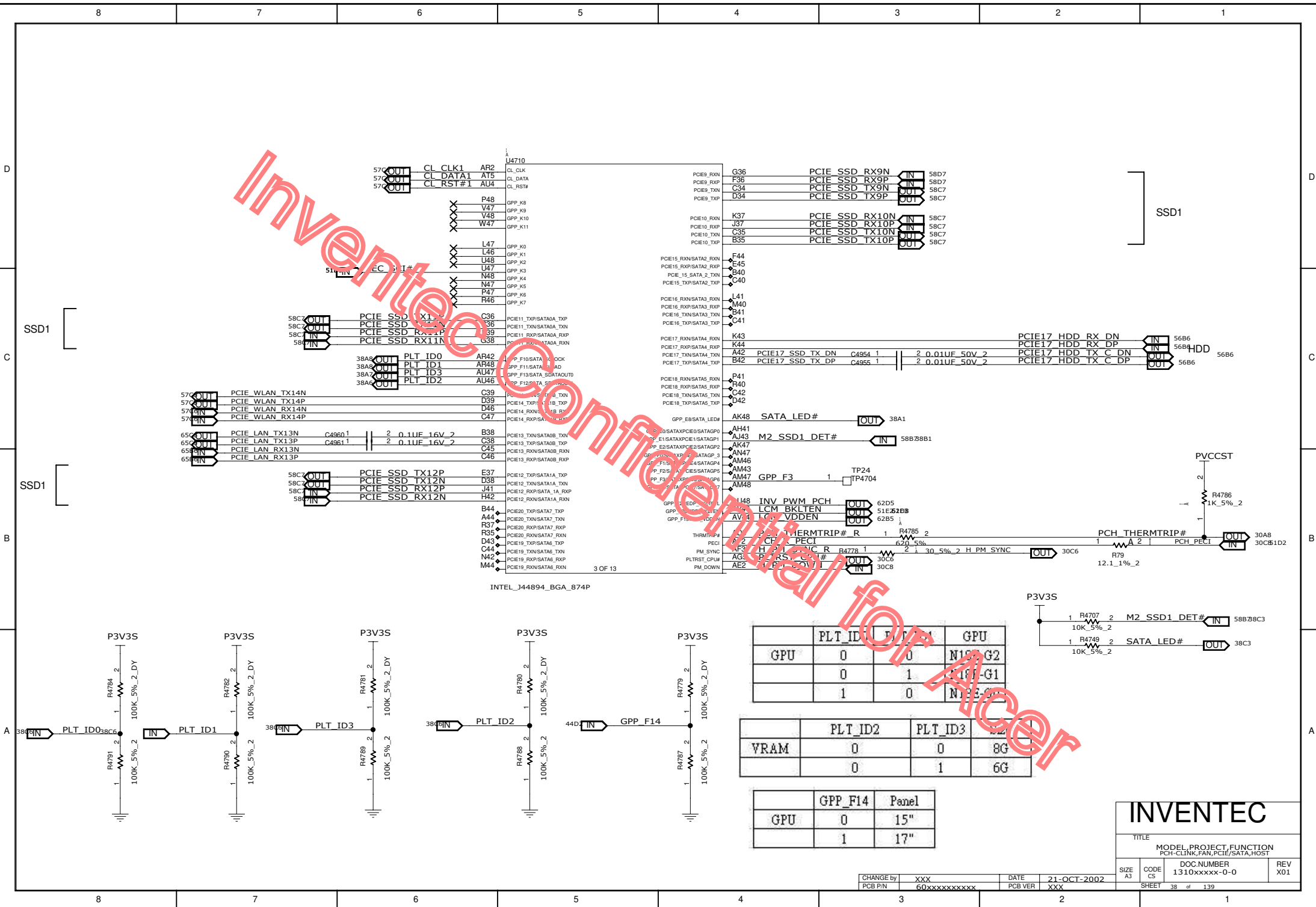


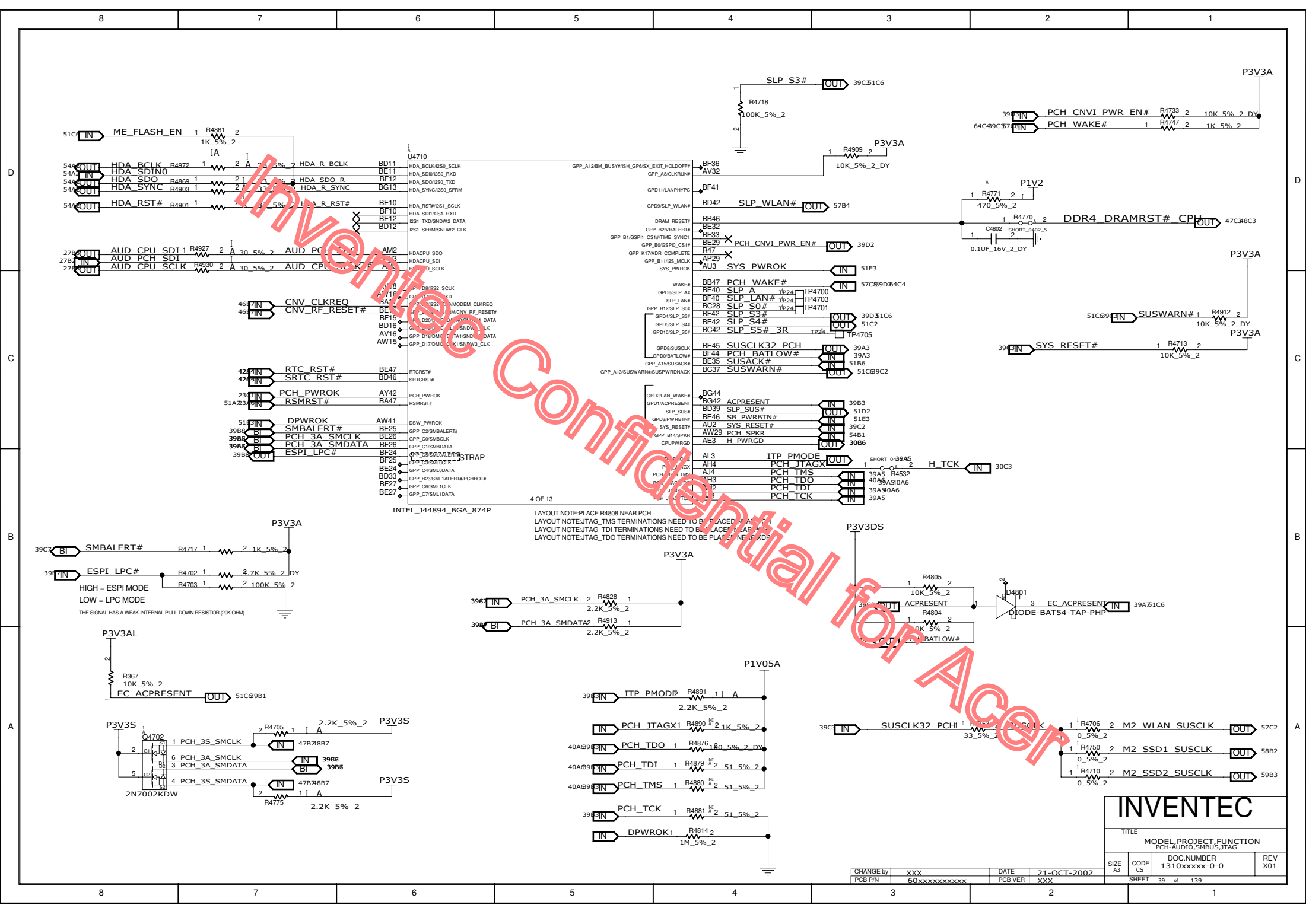


INTEL_J44894_BGA_874P

INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION PCH-DMI,USB2,USB3				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0		REV X01
SHEET 37 of 139				

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





LAYOUT NOTE: PLACE R4808 NEAR PCH
LAYOUT NOTE: JTAG_TMS TERMINATIONS NEED TO BE PLACED IN A 0.5mm x 0.5mm PAD
LAYOUT NOTE: JTAG_TDI TERMINATIONS NEED TO BE PLACED IN A 0.5mm x 0.5mm PAD
LAYOUT NOTE: JTAG_TDO TERMINATIONS NEED TO BE PLACED IN A 0.5mm x 0.5mm PAD

INVENTEC

TITLE
MODEL PROJECT FUNCTION
PCH AUDIO, SMBUS, JTAG

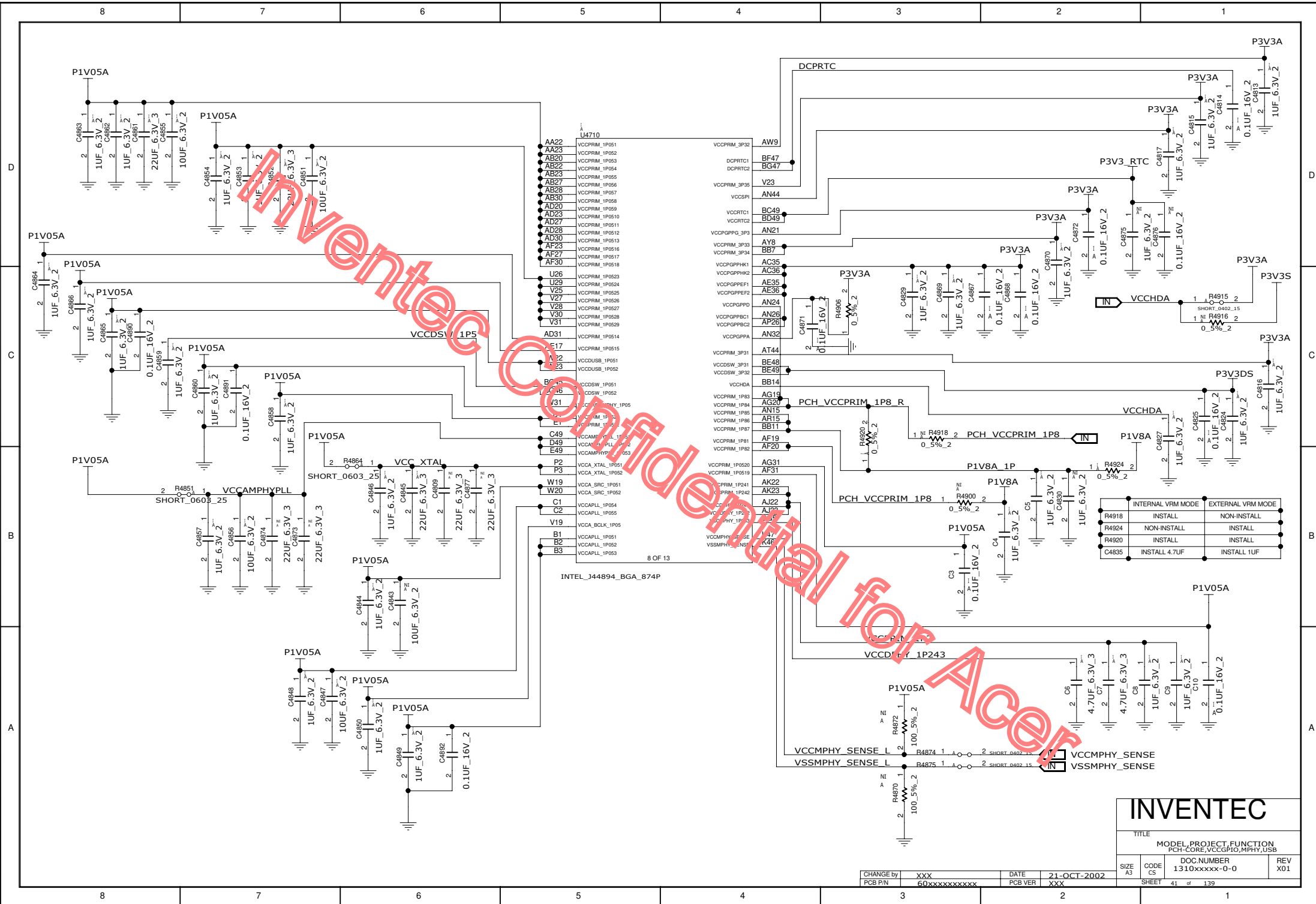
DOC NUMBER
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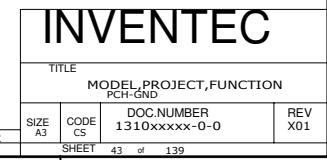
REV
X01

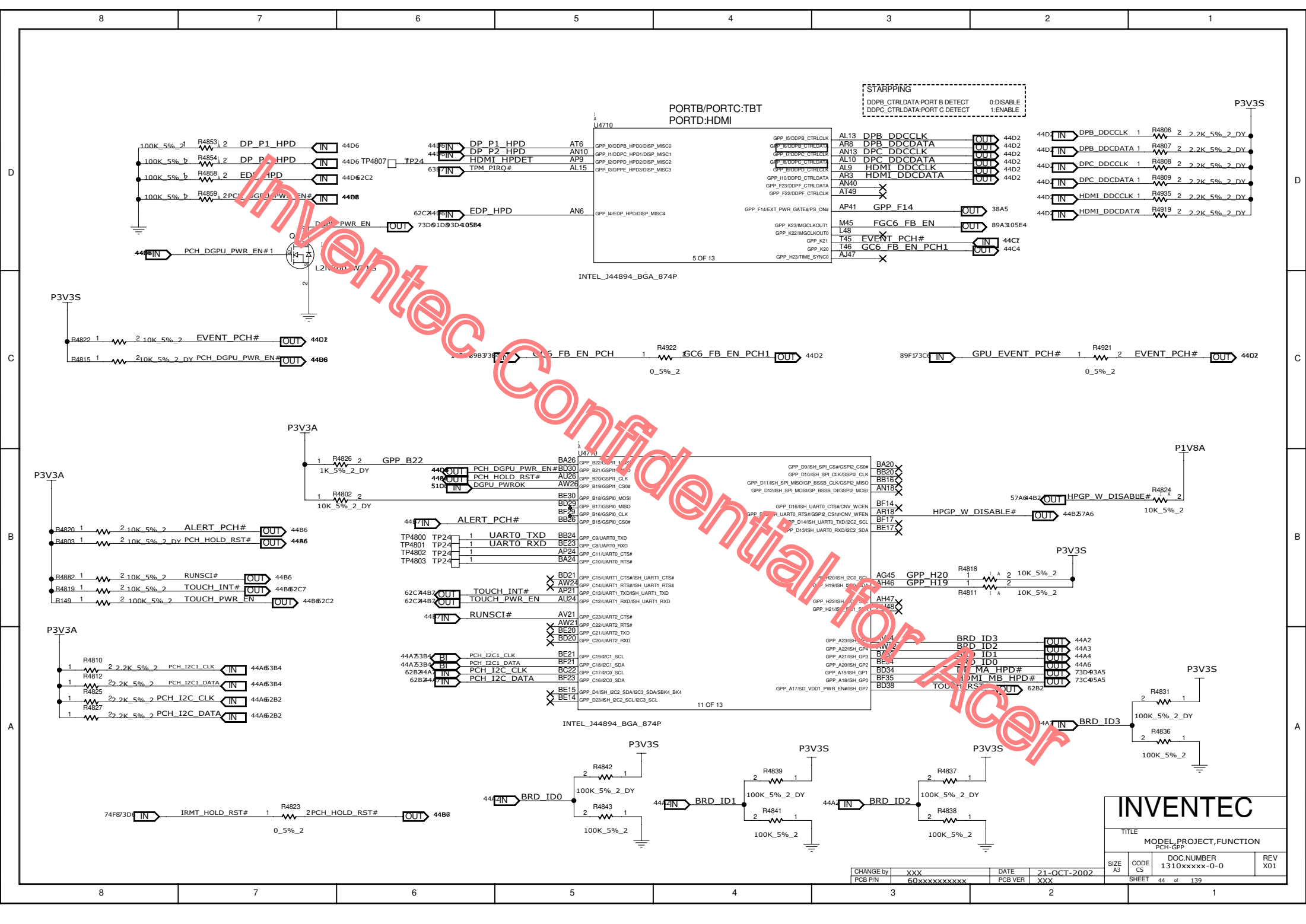
CHANGE by XXX
PCB P/N 60xxxxxxxxxxx

DATE
21-OCT-2002

SHEET 39 of 139







STARPPING

DDPB_CTRLDATA:PORT B DETECT	0:DISABLE
DDPC_CTRLDATA:PORT C DETECT	1:ENABLE

PORTB/PORTC:TB
PORTD:HDMI

INTEL_J44894_BGA_874P

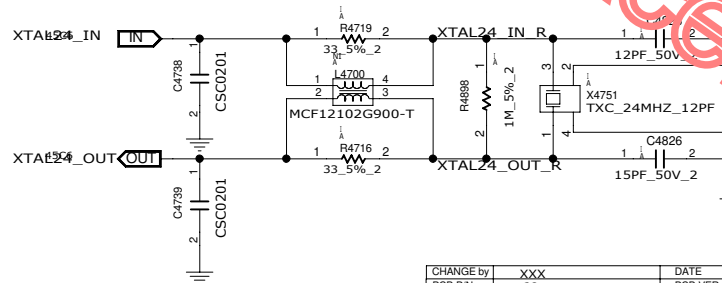
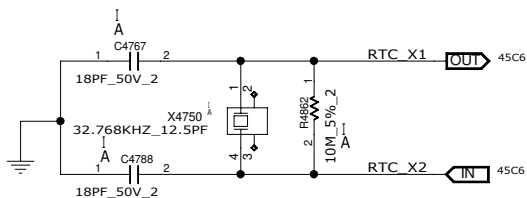
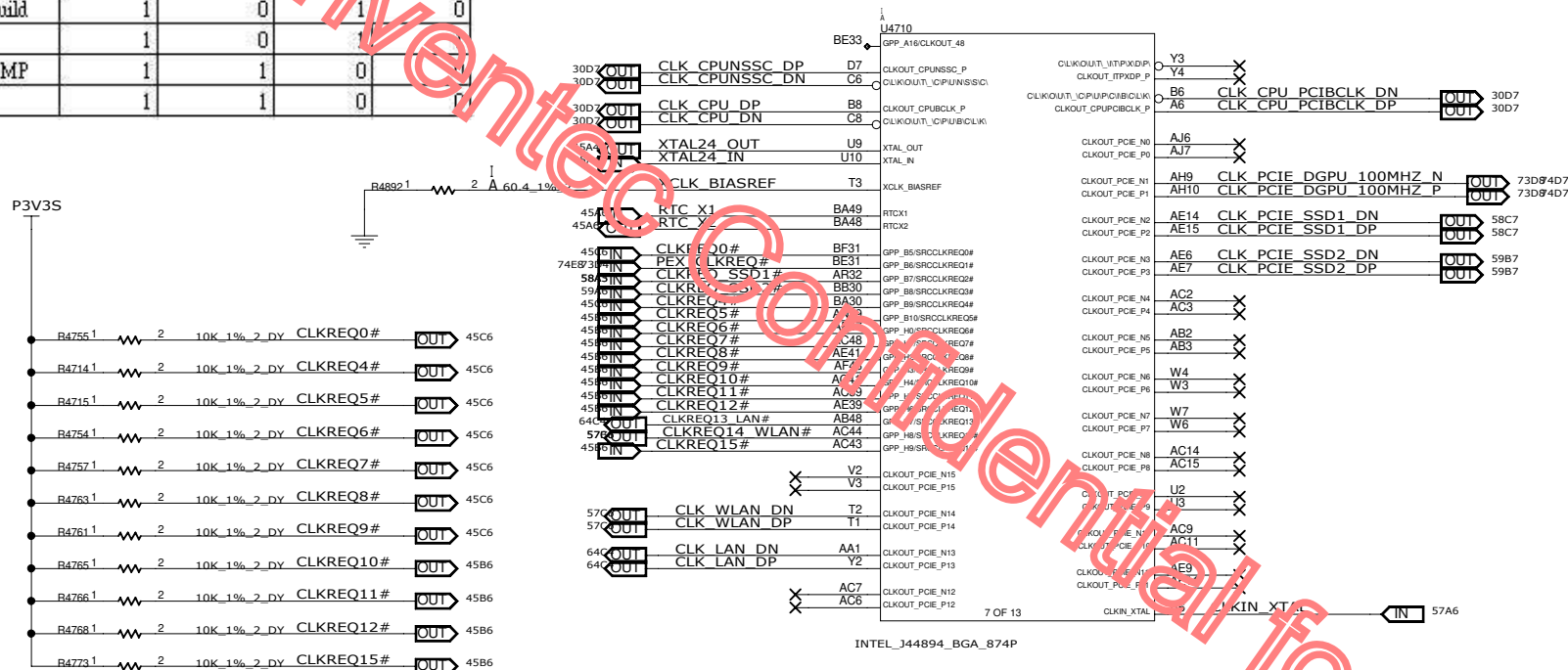
INTEL_J44894_BGA_874P

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
PCH/GPP			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 44 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

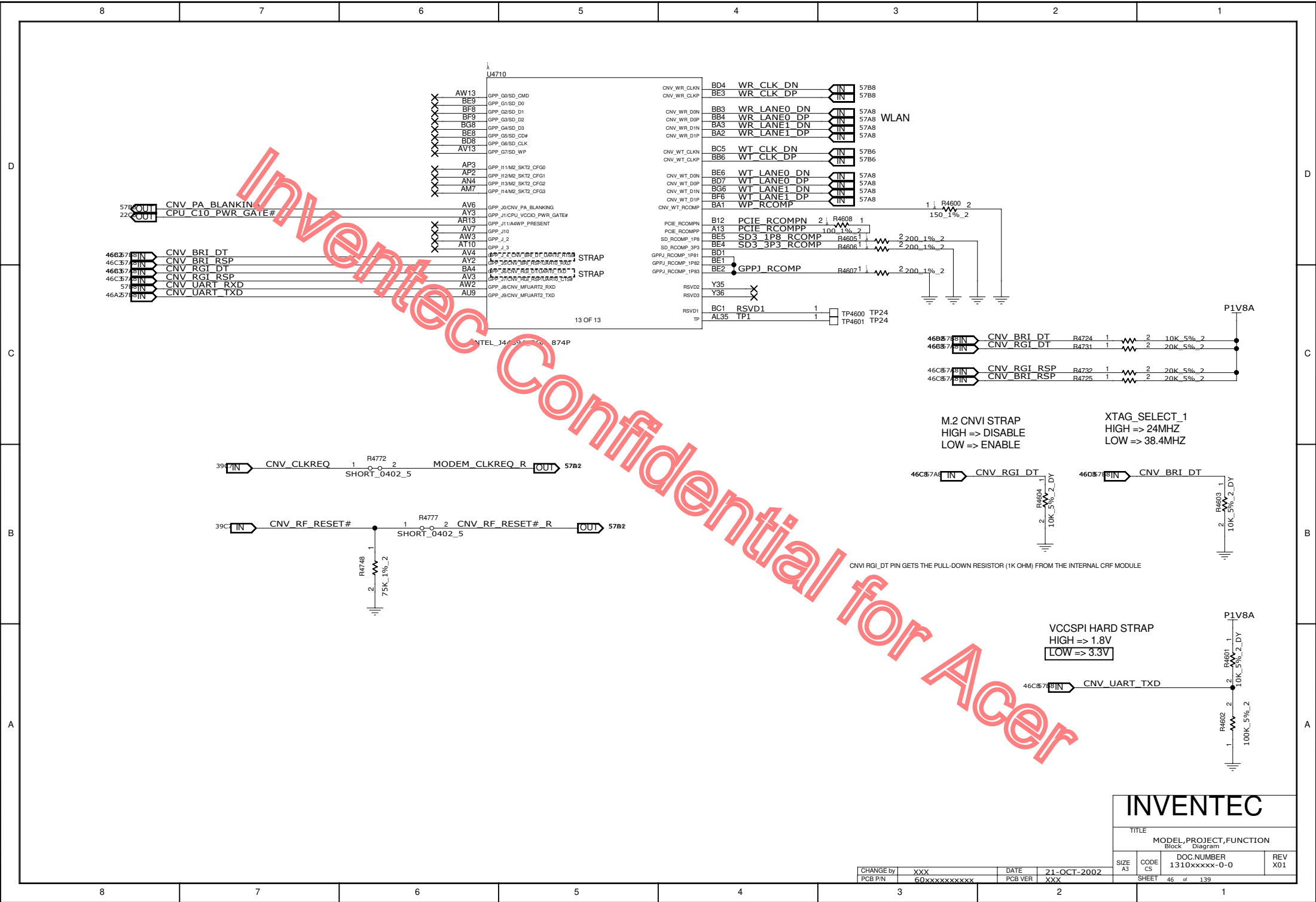
	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	1	1
D build	1	0	1	0
	1	0		
Pre-MP	1	1	0	
MP	1	1	0	

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
 - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
 - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs



INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
PCH-GPP,CLKOUT			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		45 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC NUMBER

1310xxxxx-0-0

REV

X01

CHANGE by

XXX

DATE

21-OCT-2002

PCB P/N

60xxxxxxx

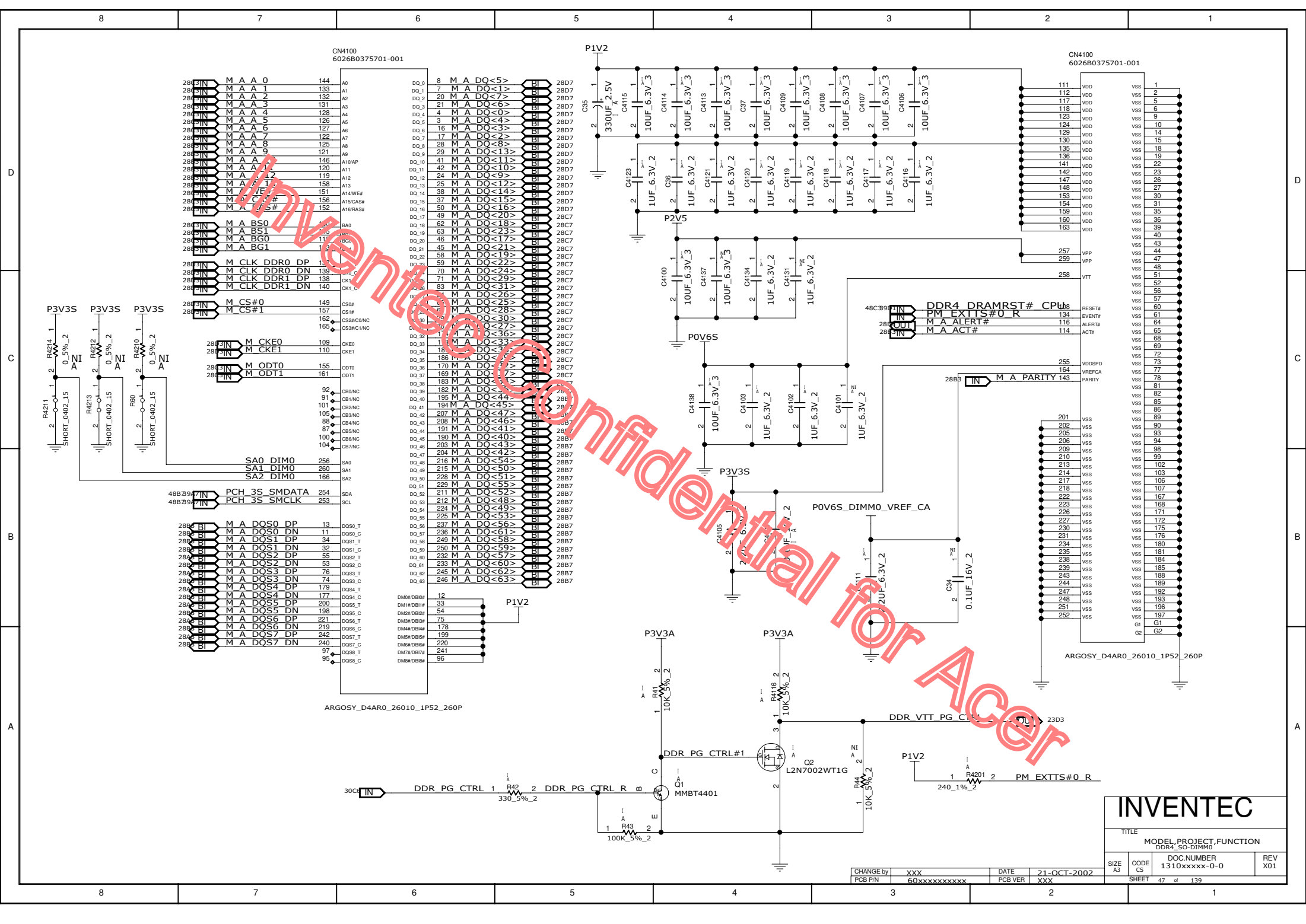
PCB VER

XXX

SHEET

46 of 139

1



INVENTEC

TITLE

MODEL PROJECT FUNCTION

DOC NUMBER

REV

SIZE

CODE

SHEET

CHANGE by XXX

PCB P/N 60xxxxxxxxxx

DATE

PCB VER

21-OCT-2002

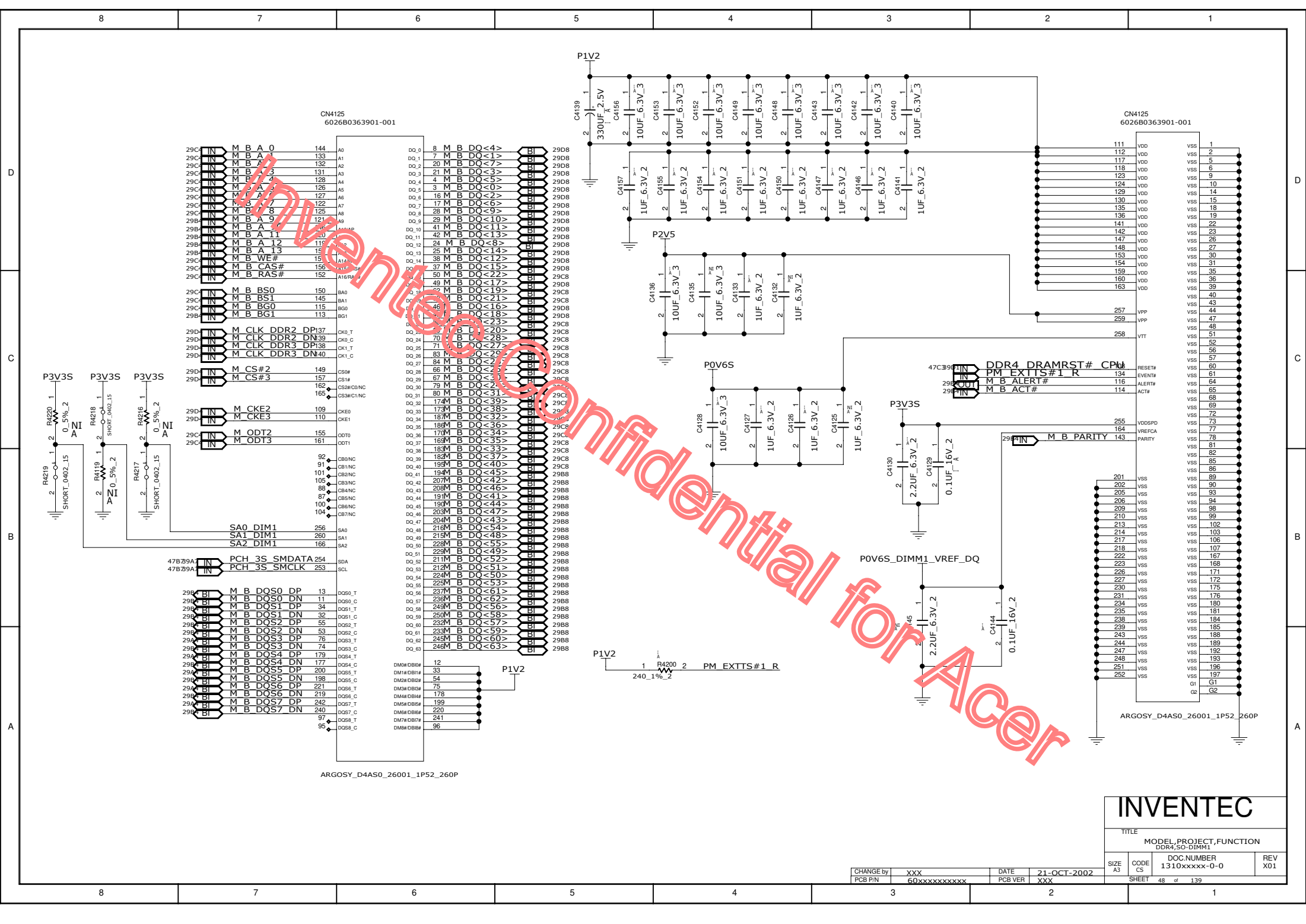
XXX

1310xxxxx-0-0

X01

47 of 139

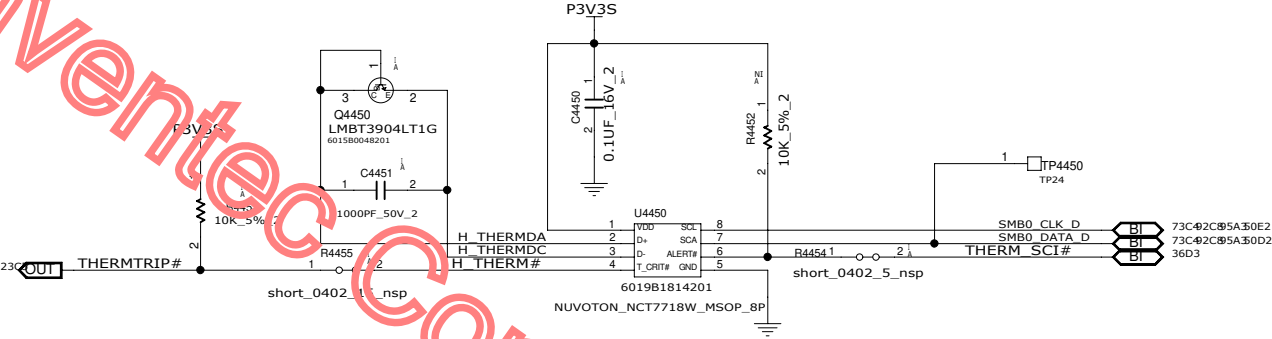
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INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
DDR4 SO DIMM1			
SIZE A3		DOC NUMBER	REV
CODE CS		1310xxxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		48 of 139	1

REFERENCE NUMBER:4450~4499

THERM SENSOR



INVENTEC

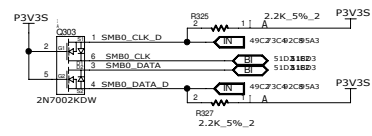
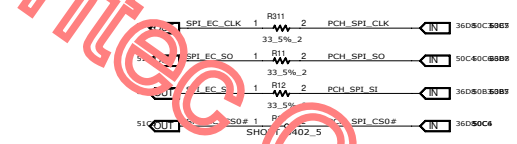
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

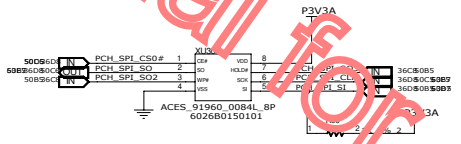
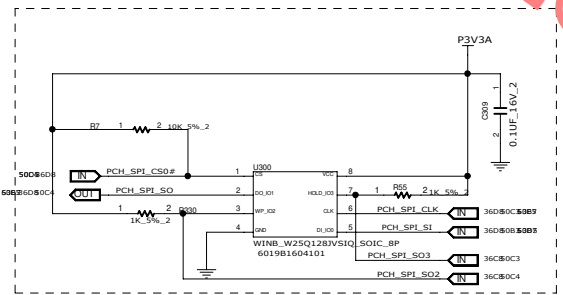
CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 49 of 139

REFERENCE 300~389(KBC)



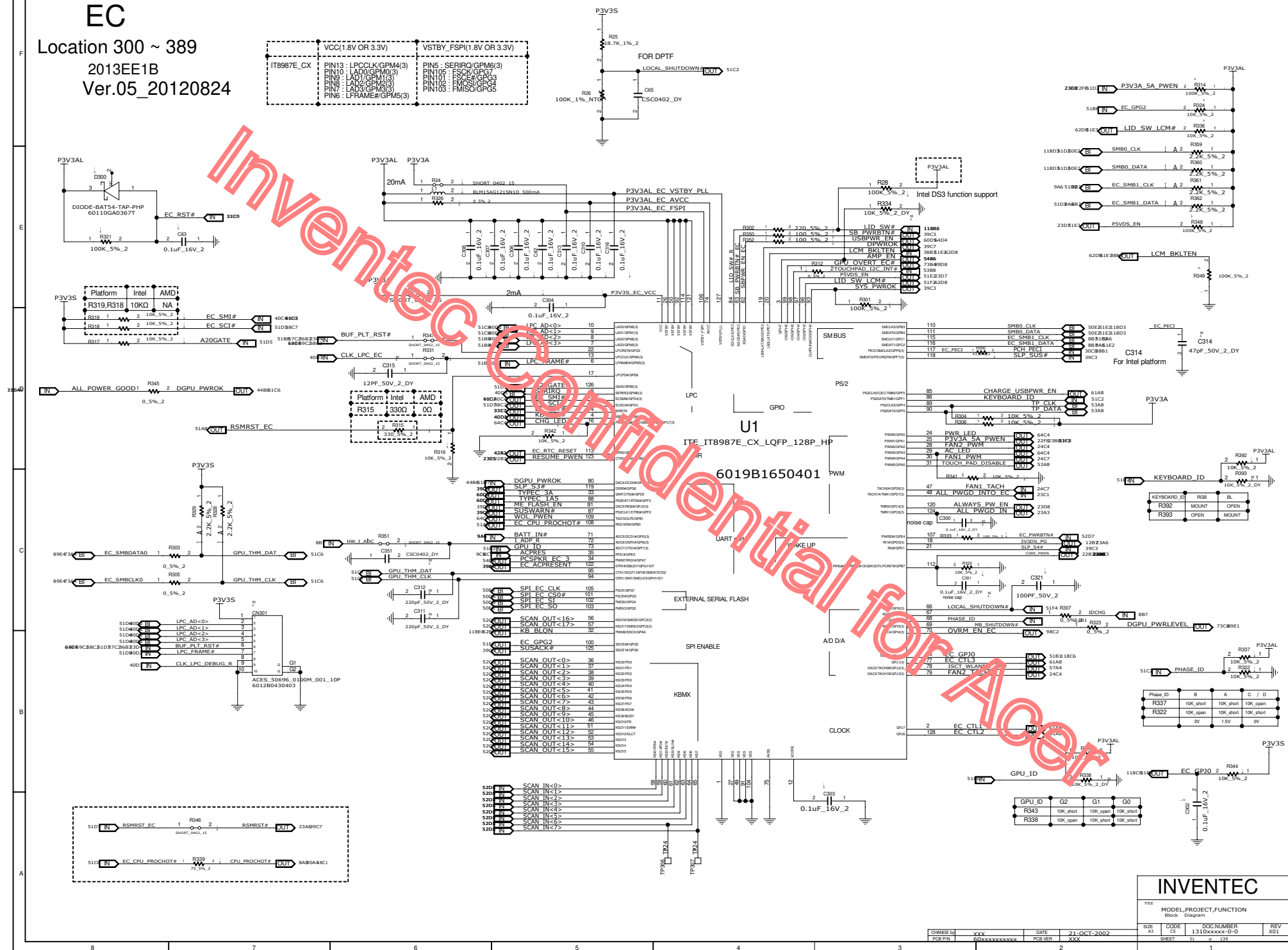
THERMAL SENSOR
HDMI
DP



R390 FOR INTEL DEBUG

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
CHANGE D	xxx	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	xxx
SIZE A3	CODE CS	DOC NUMBER	1310xxxxx-0-0
SHEET	50	of	139
REV	X01		

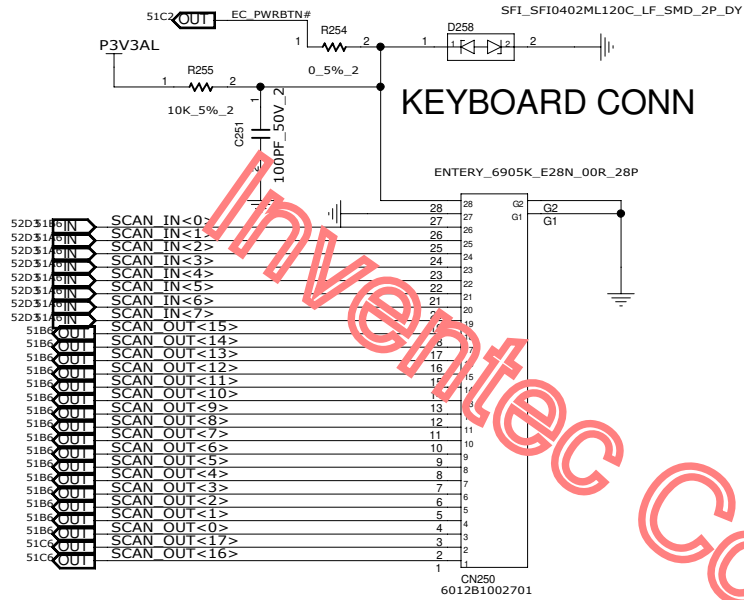
Location 300 ~ 389
2013EE1B
Ver.05 20120824



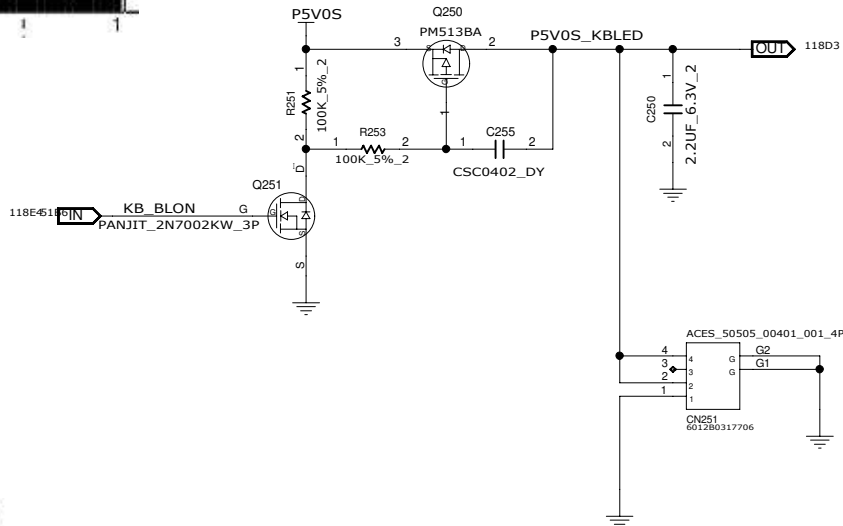
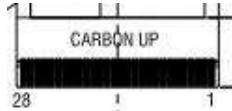
TITLE	MODEL,PROJECT,FUNCTION
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CHANGE by	xxx	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX	SHEET		51	of		139		

REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



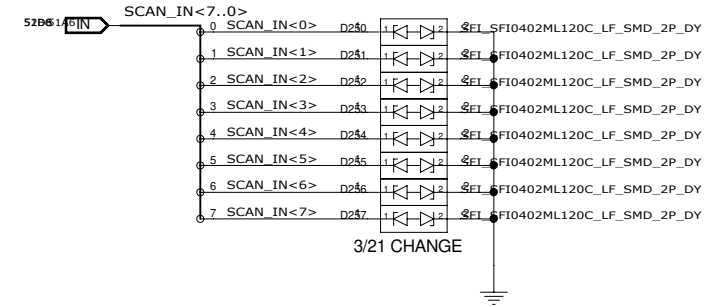
NEE TO CHANGE 6012B1002701
5/2 REVERSE



VCC : 45V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

	14*
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE

INVENTEC

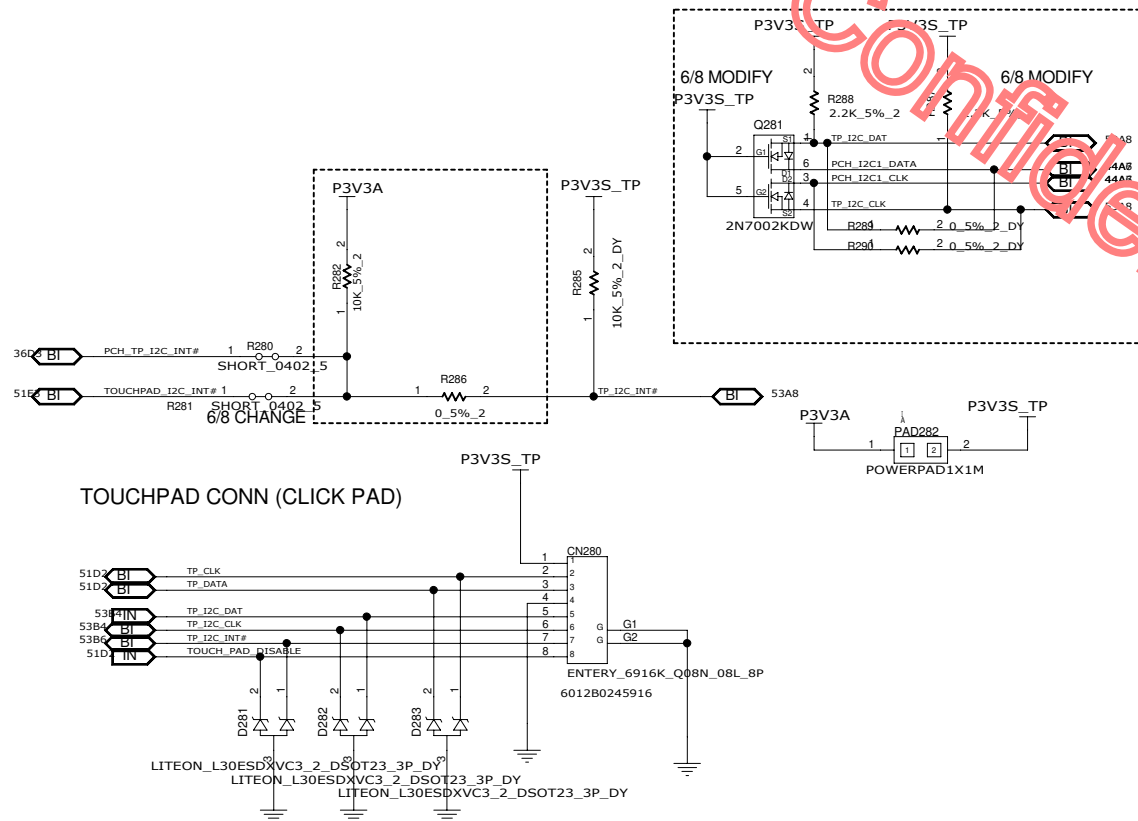
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 52 of 139

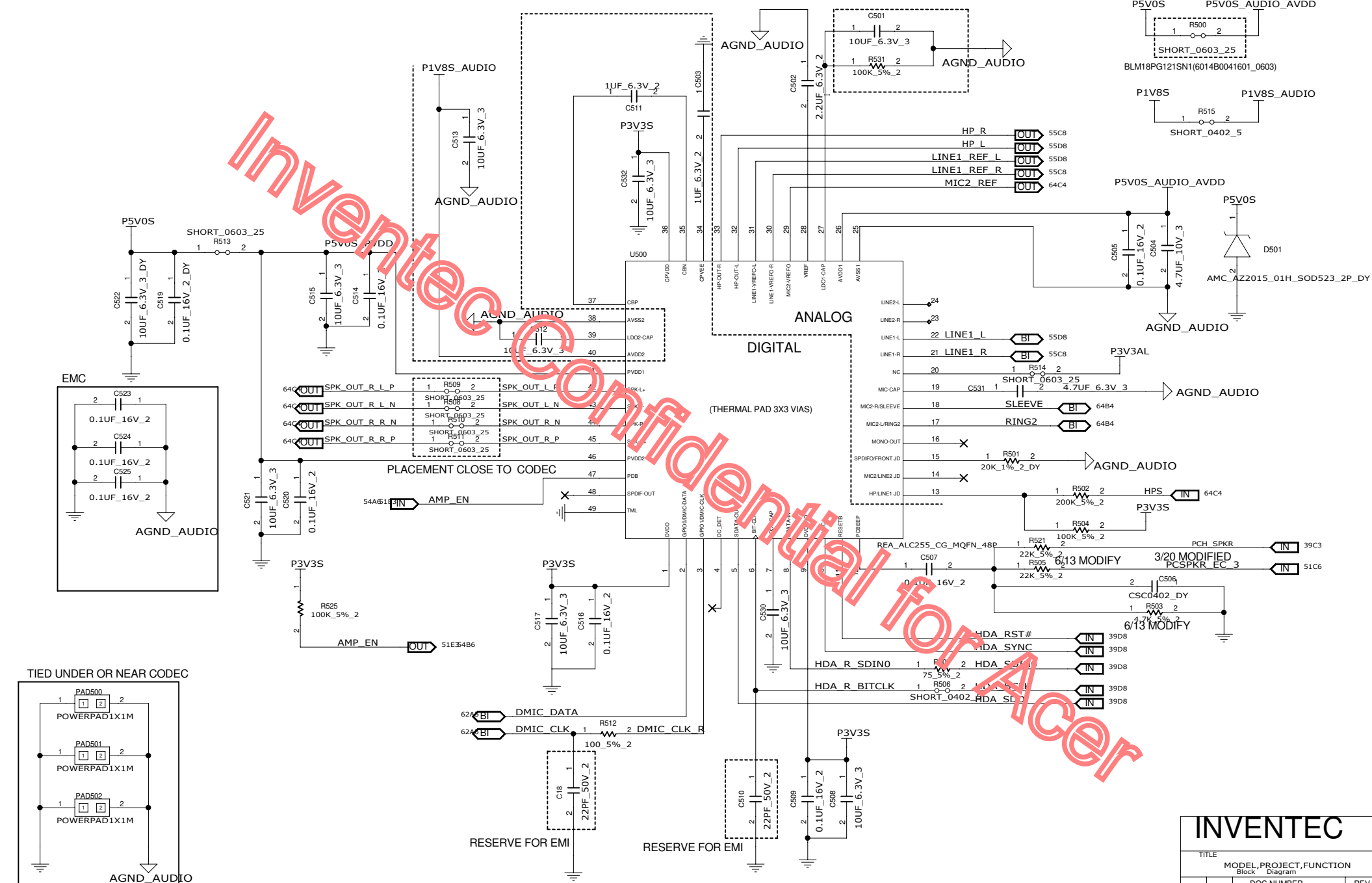
Inventec Confidential for Acer



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 53	of 139		

REFERENCE 500~549(AUDIO CODEC)

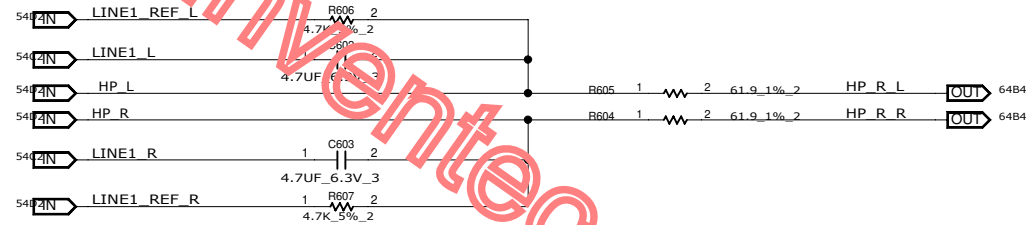


INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 54 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

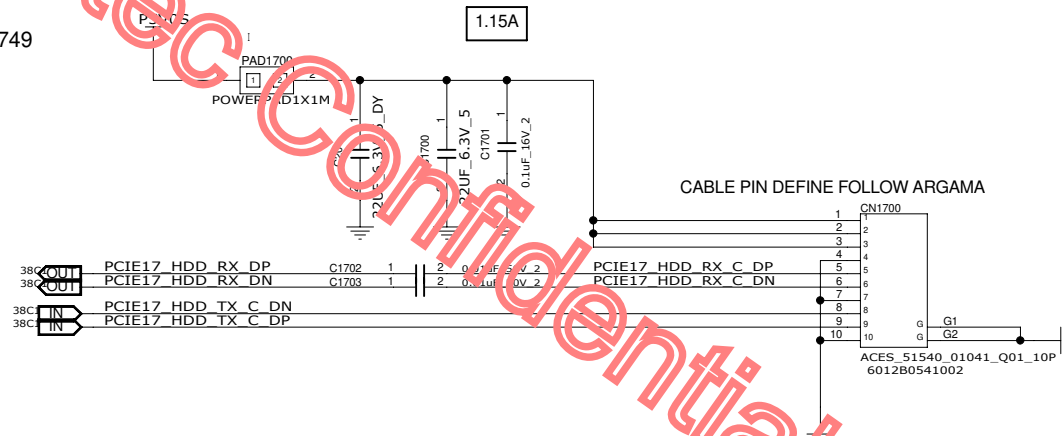
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 55 of 139

SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749



INVENTEC

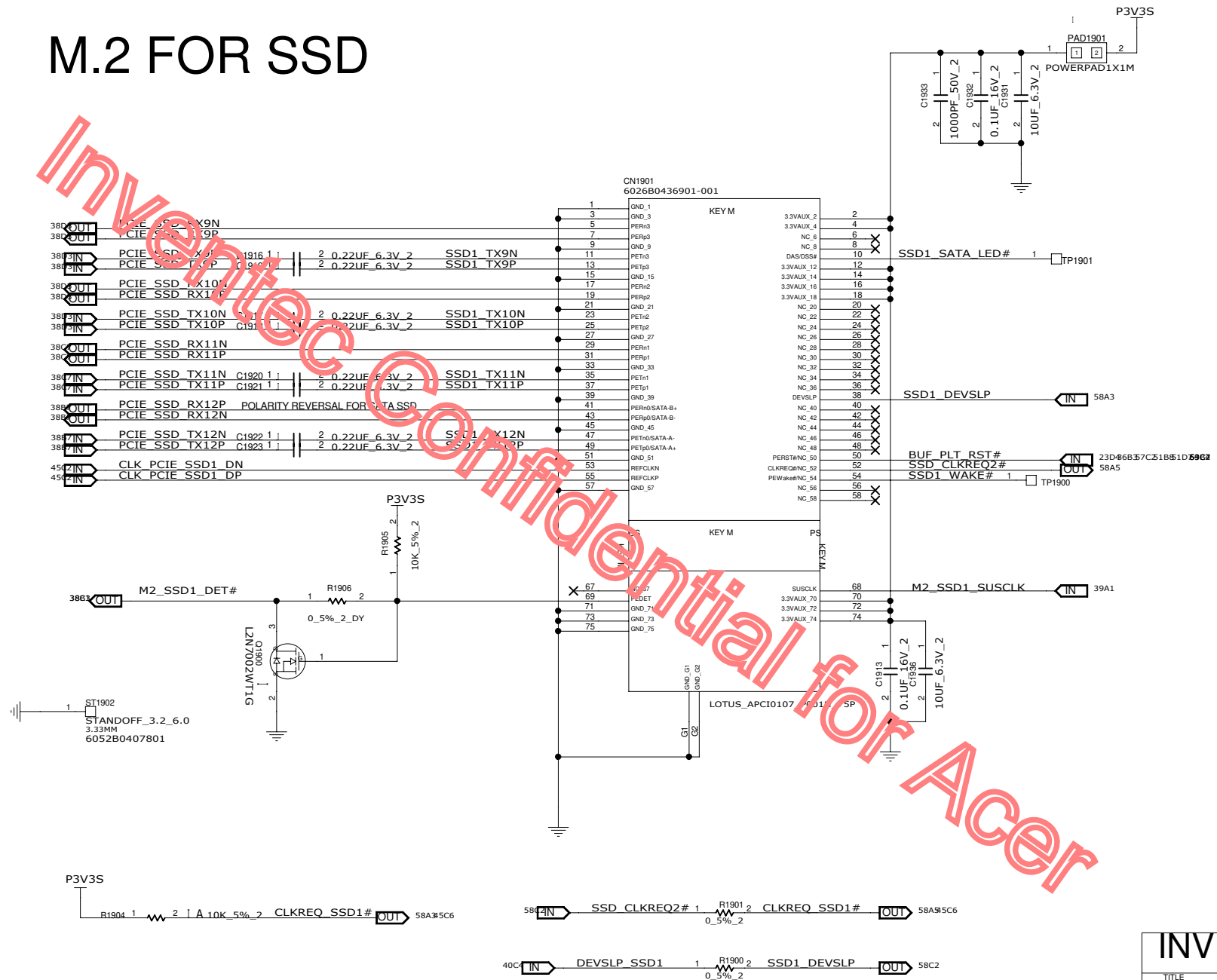
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	Block Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET 56 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

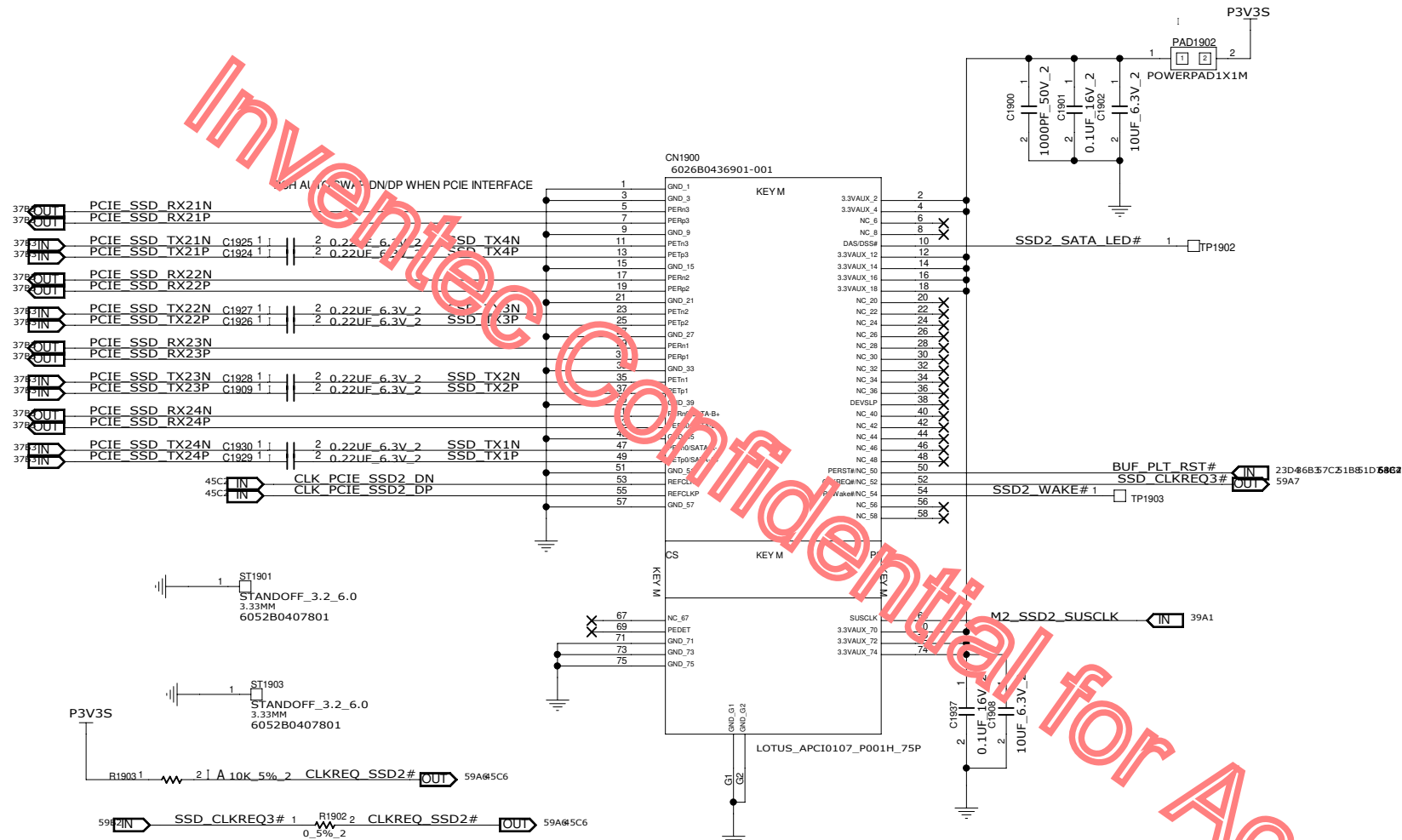
D	C	B	A
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[illegible]

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	REV X01
SHEET		58 of 139	

NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

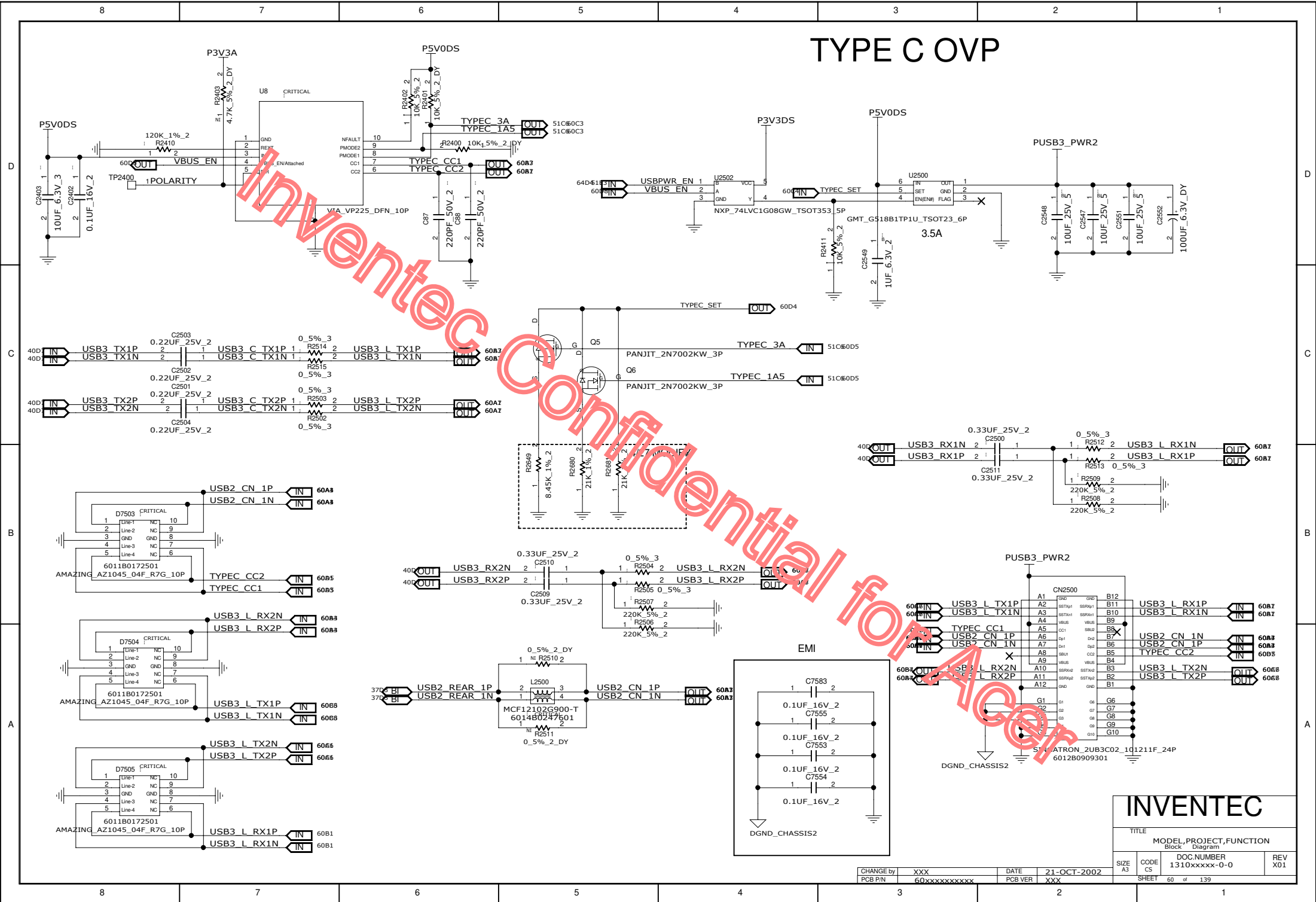
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
SATA HDD CONN.			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET	59	of	139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TYPE C OVP

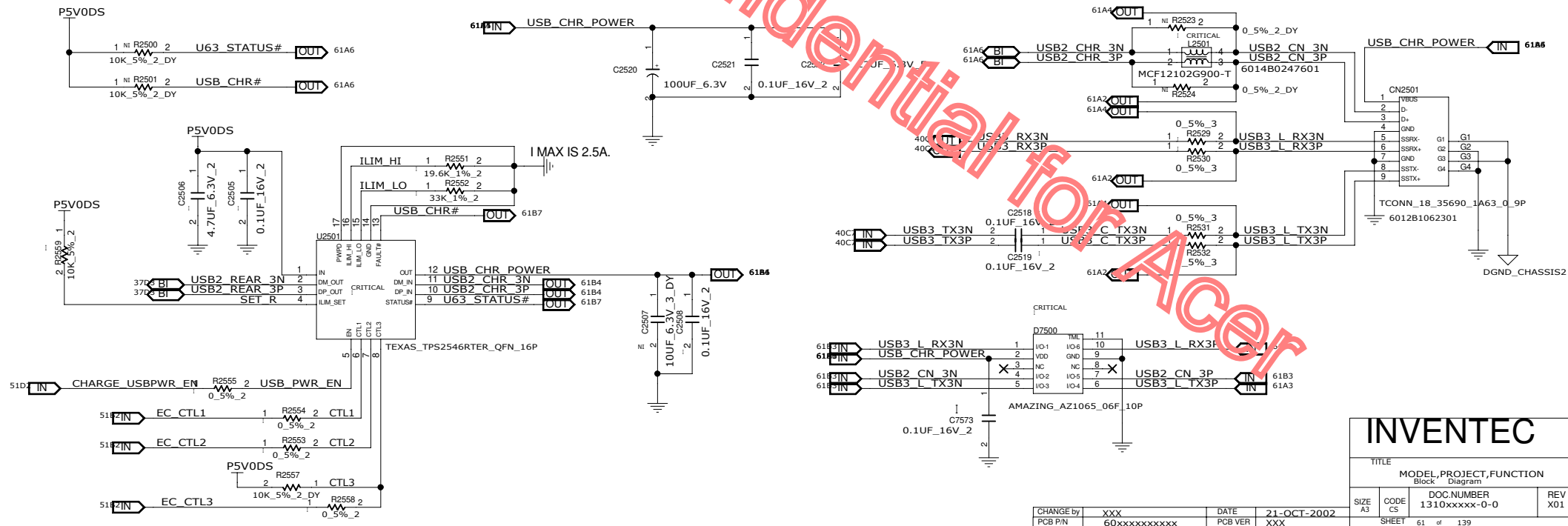


INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		60 of 139	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

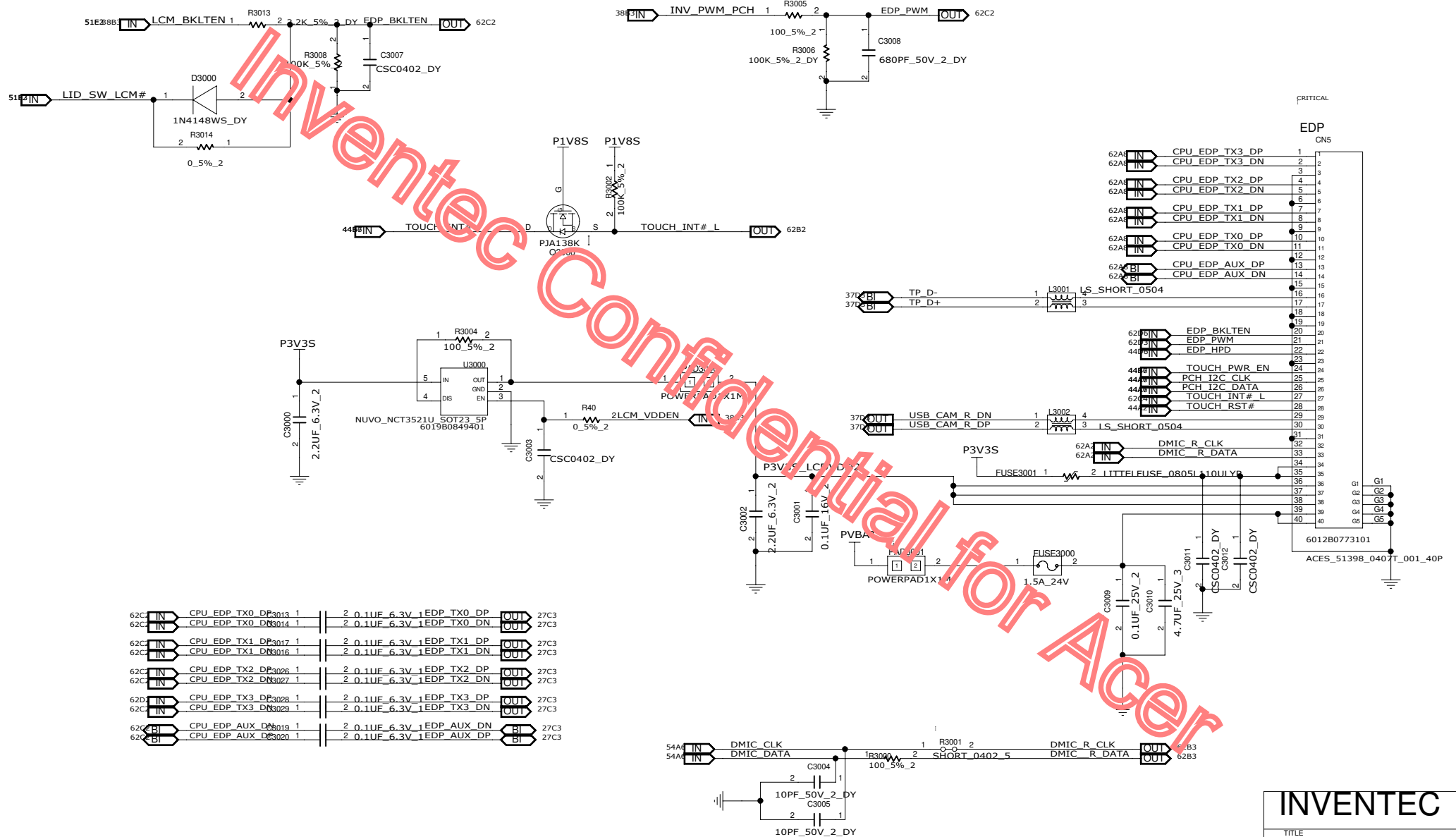
USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl.Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



REFERENCE 3000~3049(LCM)

EDP CONN



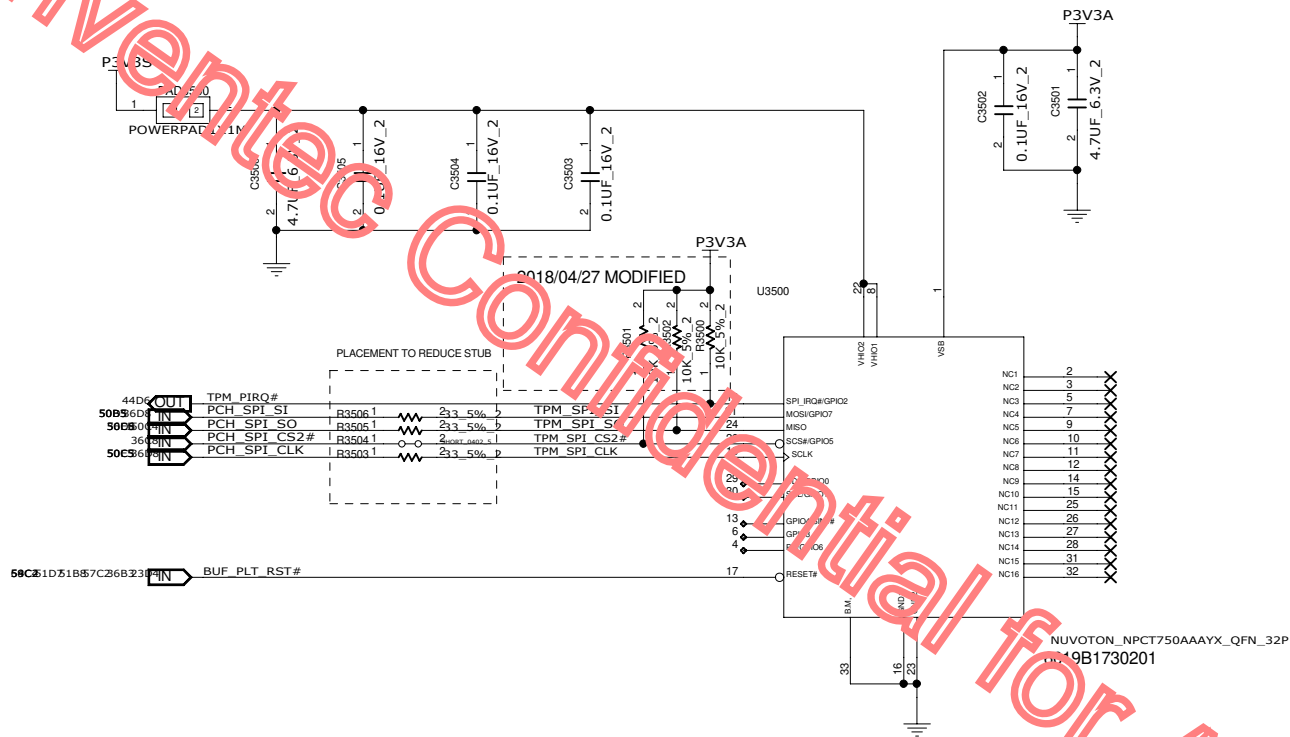
INVENTEC

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MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

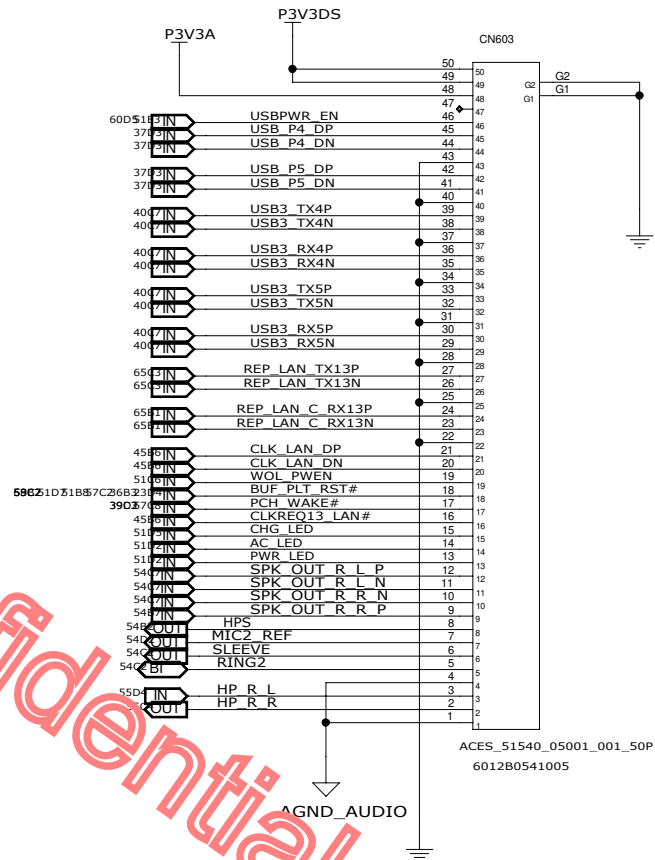
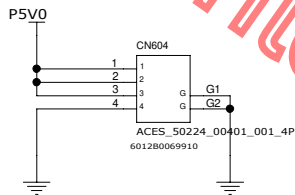
SHEET 62 of 139

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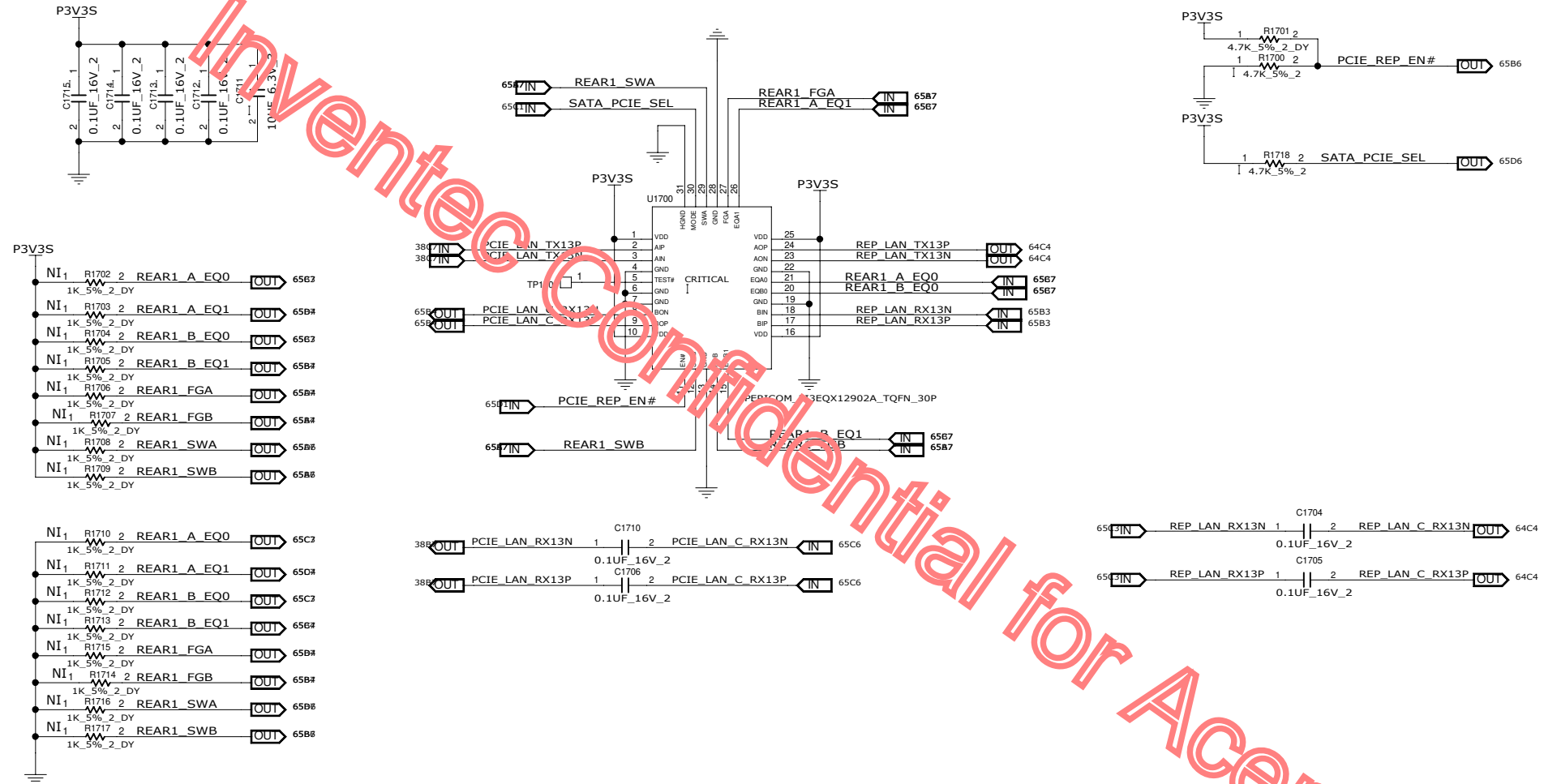
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TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		63 of 139	1	

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INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		64 of 139		

PCIE REPEATER



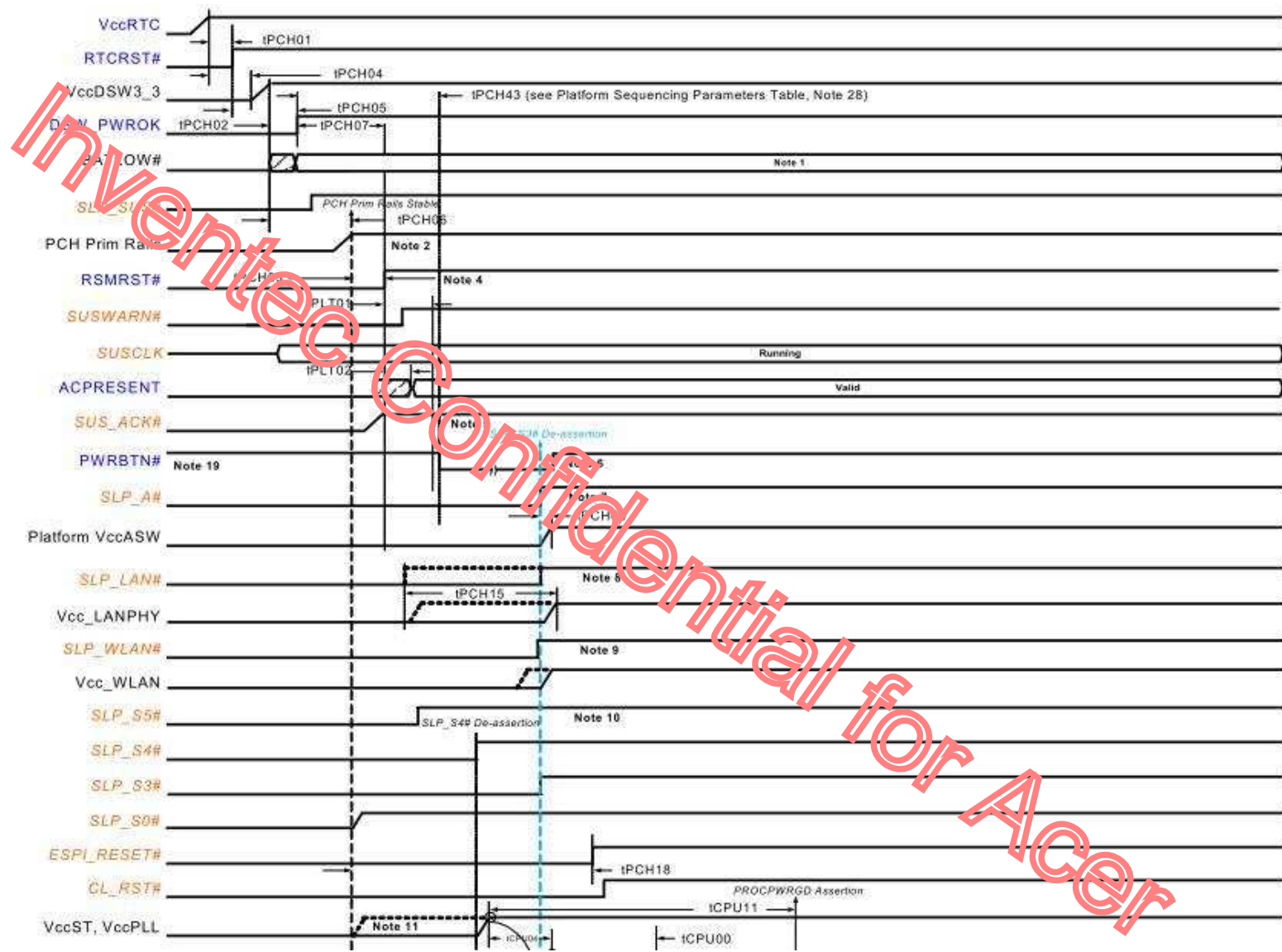
INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

SHEET 65 of 139



INVENTEC			
TITLE MODEL PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
60xxxxxxxxxx		SHEET 66 of 139	

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 68 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 69 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 70 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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N18E-G0
N18E-G1
N18E-G2 MAX-Q
8GB DDR5 256M X 16 X 2 X6

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 71 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

PCA CODE NAME : N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001

G1 : 6019B1849201

G2 MAXQ:6019B1849301

PCB VERSION : X01

BOARD SIZE:

SCH P/N:

PCB P/N:

PCA P/N:

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL

NI: NON-INSTALL

DY: NON-INSTALL

MP: PRODUCTION

PROTO: PRE-PRODUCTION

CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847701

MICRON MT61K256M32JE-14:A
6019B1847701

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MONITOR BOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (MP86941_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (MP86941_1P)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (R18158A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
88	GPU VBIOS, STRAPS	118	
89	GPU GPIOs	119	
90	GPU IFP_AB	120	
91	GPU DP IFP_CD	121	
92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
93	GPU DP CONNECTOR	123	
94	GPU HDMI IFP_EF	124	
95	GPU HDMI RETIMER IT66317	125	
96	GPU HDMI CONNECTOR	126	
97	GPU NVHS	127	
98	OV-R	128	
99	GPU NVDD	129	
100	GPU FBVDD	130	

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	72	of	139				

CONNECTION TO MAINBOARD

D

C

B

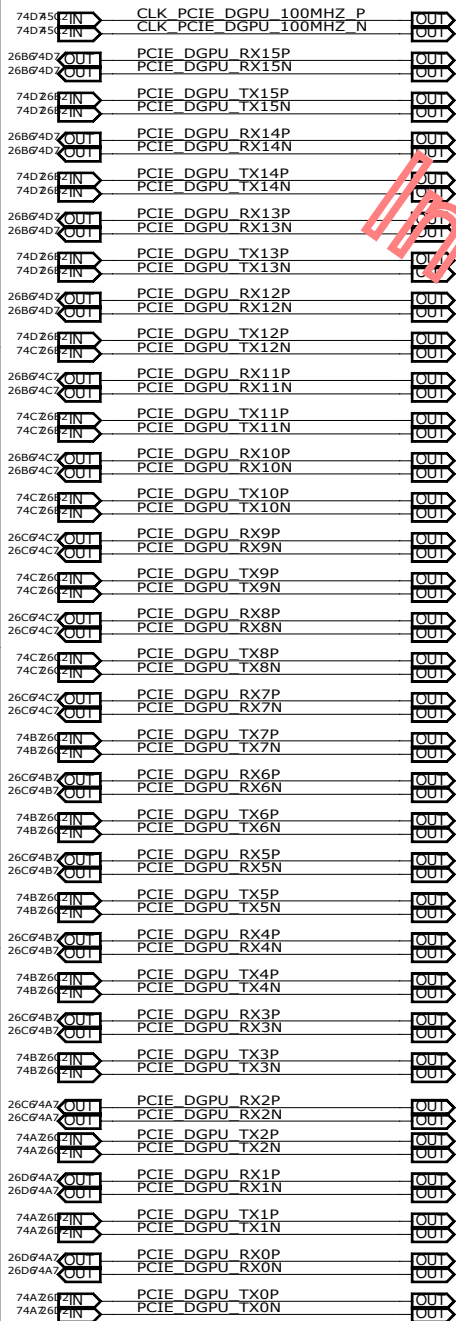
A

D

C

B

A



105B403D41D84D 2IN DGPU_PWR_EN 2OUT

GPU_PWR_ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

74F86B 2IN PCH_PLTRST#_BUF 2OUT

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

74F814A 2IN IRMT_HOLD_RST# 2OUT

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

74C268 2IN GPU_EVENT_PCH# 2OUT

GPU EVENT FOR GPU WILL EXIT GC6 MODS

89E51C 2IN DGPU_PWRLE 2OUT

15.3.2 PWR_LEVEL* (GPIO12)

The **PWR_LEVEL** input signal triggers an immediate low-to-high or slow-to-high transition followed by the driver capping the GPU power state to the appropriate limit. There are a few events that can trigger this signal assertion: AC to battery power transition, total system power overdraw event.

45C64E8 2OUT PEX_CLKREQ# 2IN

PCIE CLK REQUESTD#

51D8 105A 2OUT ALL_POWER_GOOD 2IN

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

93A54A 2OUT DP_MA_HPD# 2IN

DP HPD TO MAINBOARD

MAKE SURE 10K P3V3S PULL UP

50D295A32C873C49C 2BI SMB0_DATA_D 2BI

50E295A32C873C49C 2BI SMB0_CLK_D 2BI

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

95A54A 2OUT HDMI_MB_HPD# 2IN

HDMI HPD TO MB

98B 2BI SMB0_DATA_D 2BI

50E295A32C873C49C 2BI SMB0_CLK_D 2BI

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

93A54A 2OUT GPU_OVERT_EC# 2IN

GPU OVERT
OVER TEMPERATURE TO PCH OR EC

105B414C89B 2OUT GC6_EN_PCH 2IN

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

89E51C 2BI EC_SMBDATA0 2BI

89E51C 2BI EC_SMBCLK0 2BI

GPU I2C, COMMUNICATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

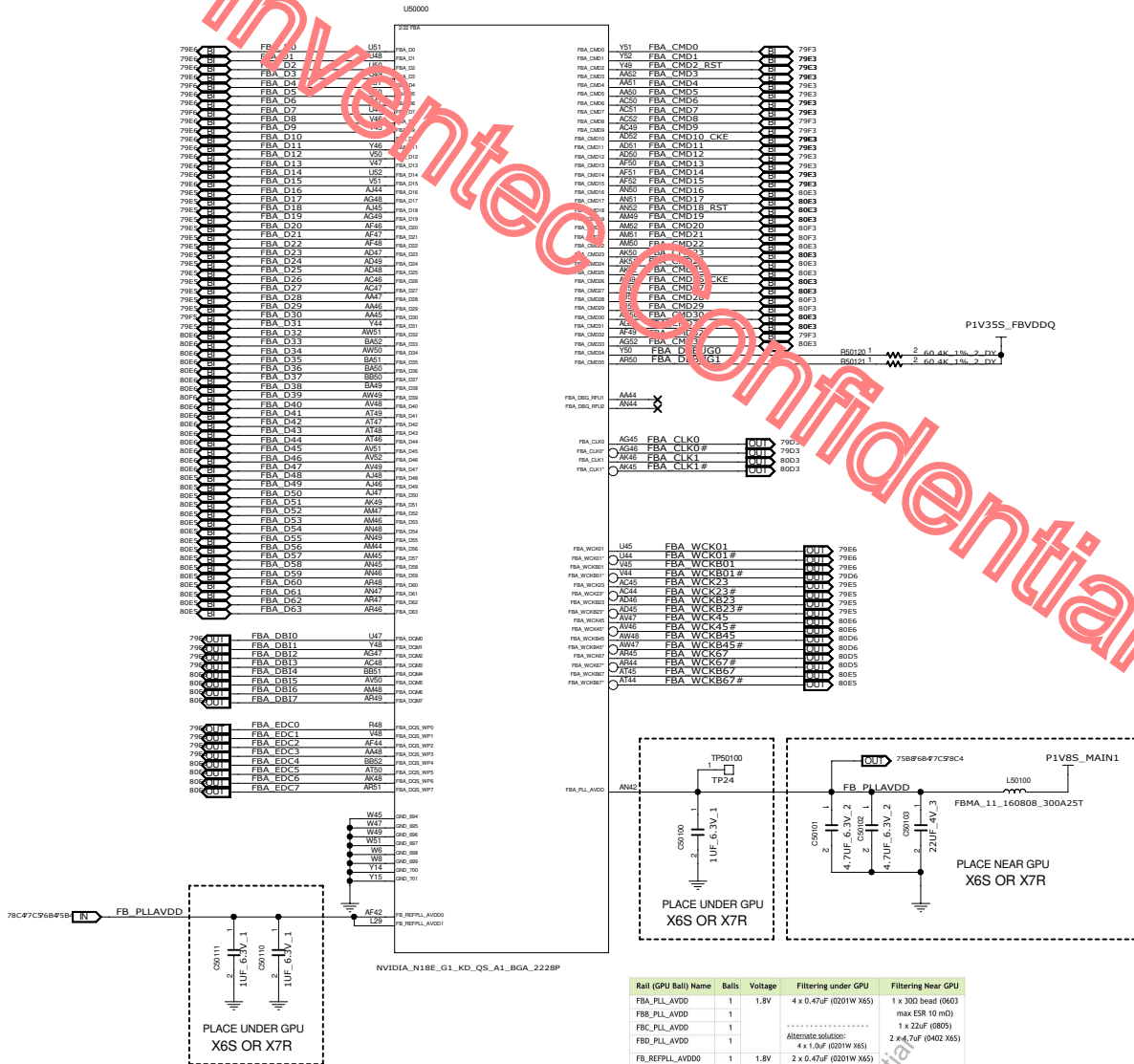
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 73 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1			2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1			2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	

50100 - 50199

INVENTEC

MODEL, PROJECT, FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	C5	1310xxxxx-0-0	X01
SHEET	75	of 139	

CHANGE ID	XXXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxx	PCB VER	XXX

[illegible]

TP50200
1
TP24
FB PLLAVDD
IN 7550F58P2C5
2
5000
100µF 3.3V 1
X6S OR X7R
PLACE UNDER GPU

F
E
D
C
E
F



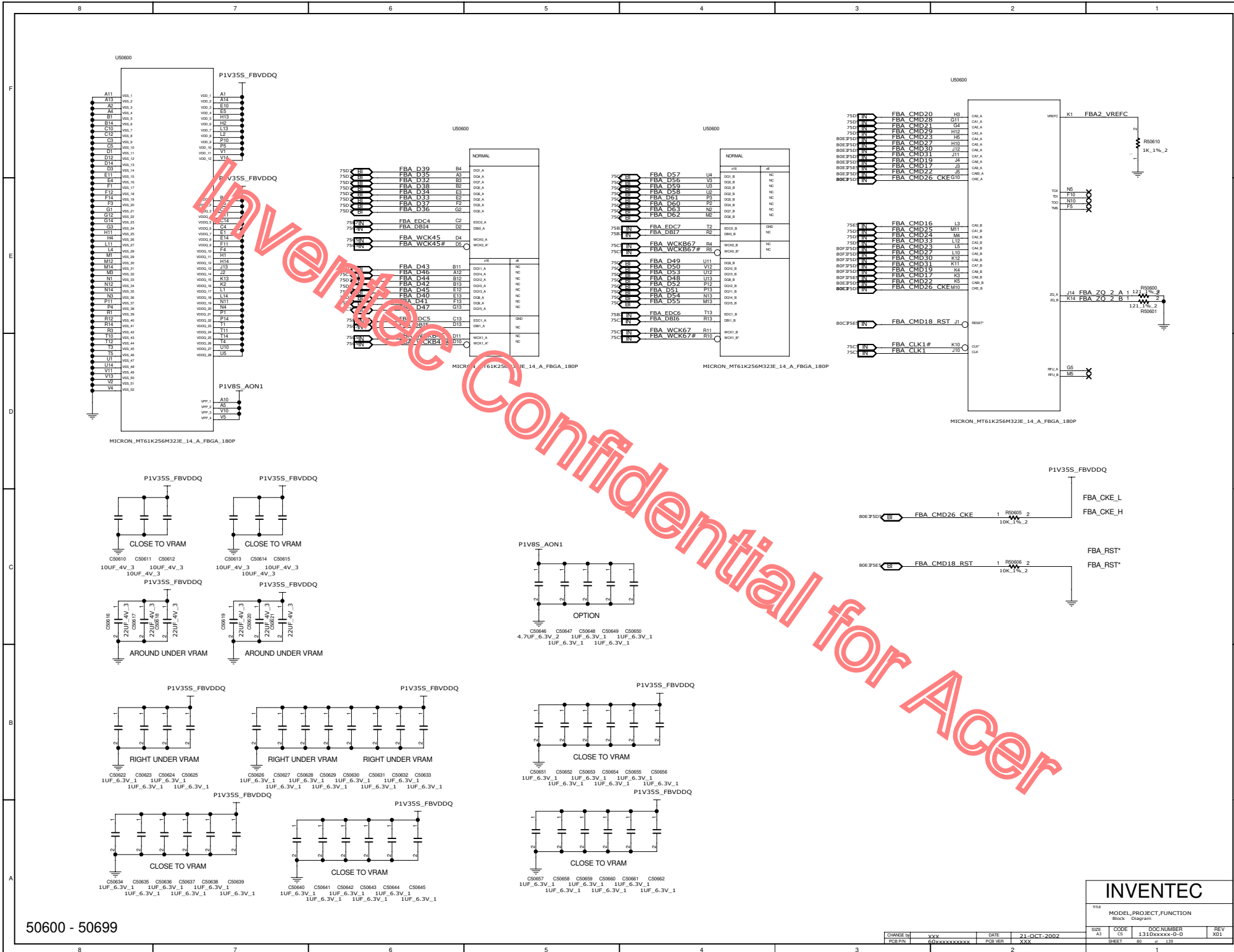
50300 - 50399

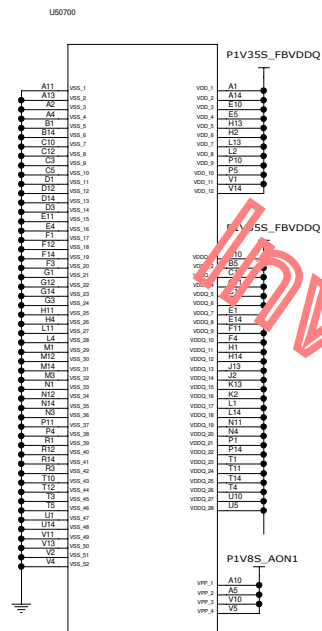
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50400 - 50499										INVENTEC <table border="1"> <tr> <td colspan="4">TITLE</td> </tr> <tr> <td colspan="4">MODEL, PROJECT, FUNCTION</td> </tr> <tr> <td colspan="4">Block Diagram</td> </tr> <tr> <td>SIZE</td> <td>CODE</td> <td>DOC NUMBER</td> <td>REV</td> </tr> <tr> <td>A1</td> <td>C3</td> <td>133 D000000-0-0</td> <td>201</td> </tr> </table>				TITLE				MODEL, PROJECT, FUNCTION				Block Diagram				SIZE	CODE	DOC NUMBER	REV	A1	C3	133 D000000-0-0	201
TITLE																																	
MODEL, PROJECT, FUNCTION																																	
Block Diagram																																	
SIZE	CODE	DOC NUMBER	REV																														
A1	C3	133 D000000-0-0	201																														
CHANGE IN		xxx	DATE	21-OCT-2002		SIZE		CODE		DOC NUMBER		REV																					
PCB PIN		60xxxxxxxxxx		PCB VER		XXX		SHEET		78		# 132																					
8		7		6		5		4		3		2																					

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 78		of 139	
1			

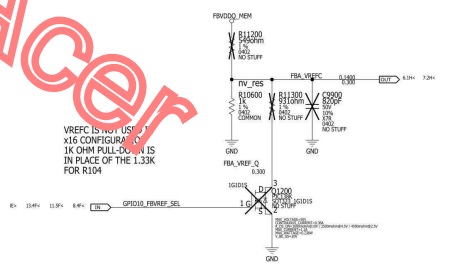
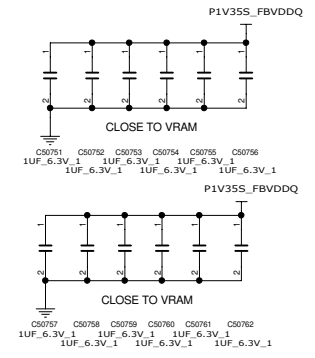
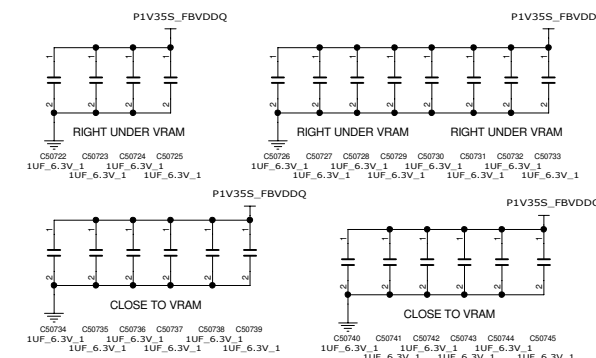
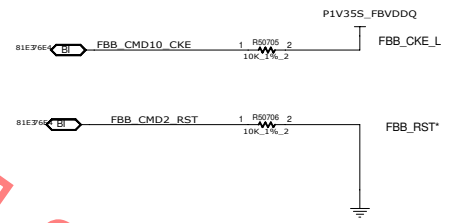
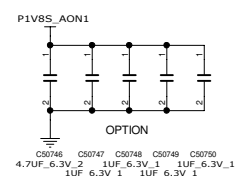
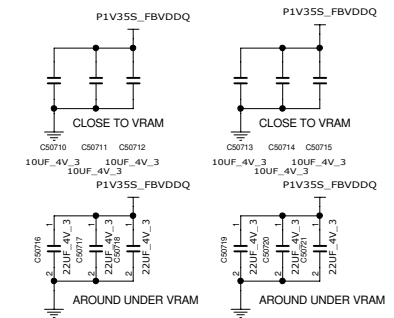
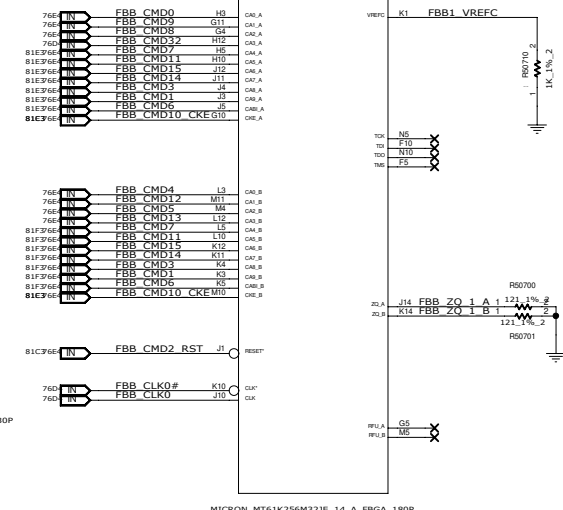
CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 78 of 139			
2				1			





NORMAL			
76E2	IN	FBB D1	B4
76E2	IN	FBB D6	A3
76E2	IN	FBB D2	B3
76E2	IN	FBB D5	E9
76E2	IN	FBB D3	E2
76E2	IN	FBB D0	F2
76E2	IN	FBB D7	D2
76E2	IN	FBB D4	D3
76E2	IN	FBB D10	C2
76E2	IN	FBB D8	D0
76E2	IN	FBB D9	D1
76E2	IN	FBB D11	B11
76E2	IN	FBB D12	B12
76E2	IN	FBB D13	B13
76E2	IN	FBB D14	A12
76E2	IN	FBB D15	E12
76E2	IN	FBB D16	E13
76E2	IN	FBB D17	D13
76E2	IN	FBB D18	D14
76E2	IN	FBB D19	M13
76E2	IN	FBB D20	M12
76E2	IN	FBB D21	U11
76E2	IN	FBB D22	P13
76E2	IN	FBB D23	M13
76E2	IN	FBB D24	U4
76E2	IN	FBB D25	U3
76E2	IN	FBB D26	U2
76E2	IN	FBB D27	P2
76E2	IN	FBB D28	M2
76E2	IN	FBB D29	U3
76E2	IN	FBB D30	U2
76E2	IN	FBB D31	U2
76E2	IN	FBB D32	U2
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76E2	IN	FBB D36	U2
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76E2	IN	FBB D41	U2
76E2	IN	FBB D42	U2
76E2	IN	FBB D43	U2
76E2	IN	FBB D44	U2
76E2	IN	FBB D45	U2
76E2	IN	FBB D46	U2
76E2	IN	FBB D47	U2
76E2	IN	FBB D48	U2
76E2	IN	FBB D49	U2
76E2	IN	FBB D50	U2
76E2	IN	FBB D51	U2
76E2	IN	FBB D52	U2
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76E2	IN	FBB D55	U2
76E2	IN	FBB D56	U2
76E2	IN	FBB D57	U2
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76E2	IN	FBB D59	U2
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76E2	IN	FBB D67	U2
76E2	IN	FBB D68	U2
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76E2	IN	FBB D70	U2
76E2	IN	FBB D71	U2
76E2	IN	FBB D72	U2
76E2	IN	FBB D73	U2
76E2	IN	FBB D74	U2
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76E2	IN	FBB D76	U2
76E2	IN	FBB D77	U2
76E2	IN	FBB D78	U2
76E2	IN	FBB D79	U2
76E2	IN	FBB D80	U2
76E2	IN	FBB D81	U2
76E2	IN	FBB D82	U2
76E2	IN	FBB D83	U2
76E2	IN	FBB D84	U2
76E2	IN	FBB D85	U2
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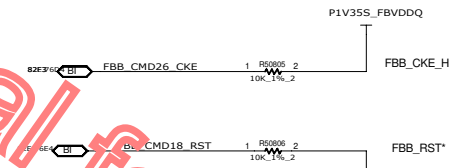
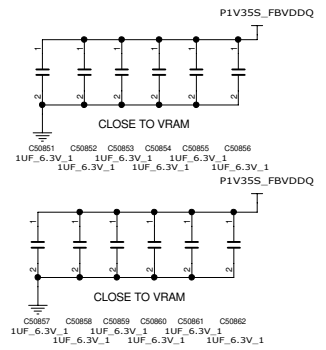
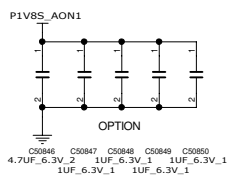
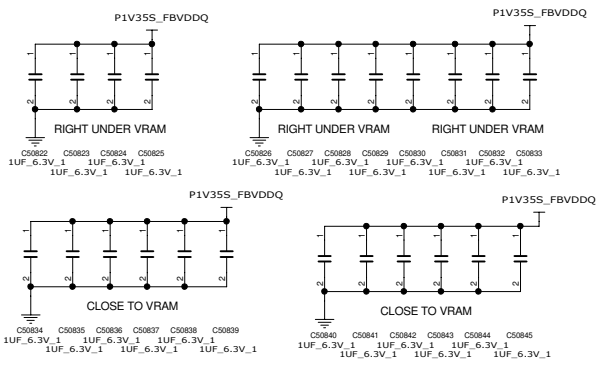
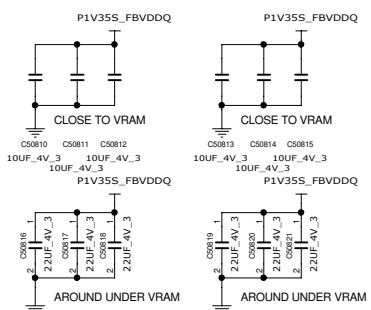
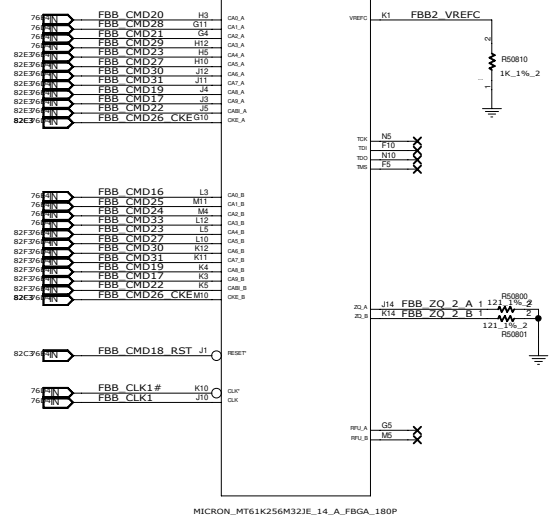
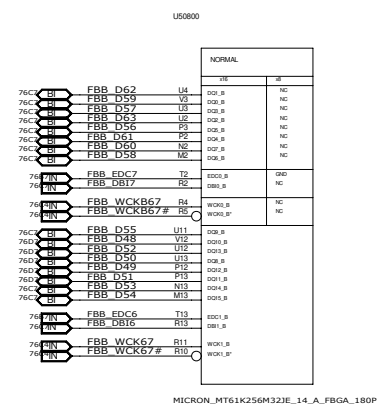
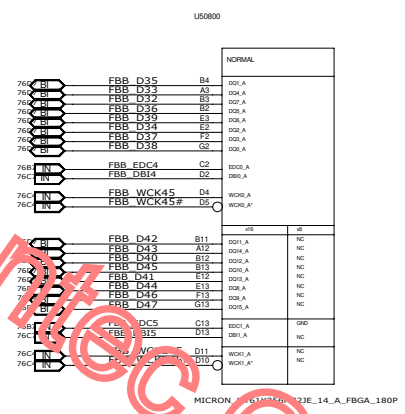
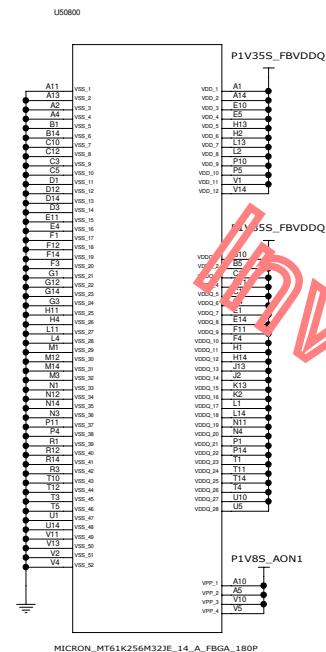
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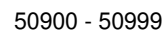
50700 - 50799

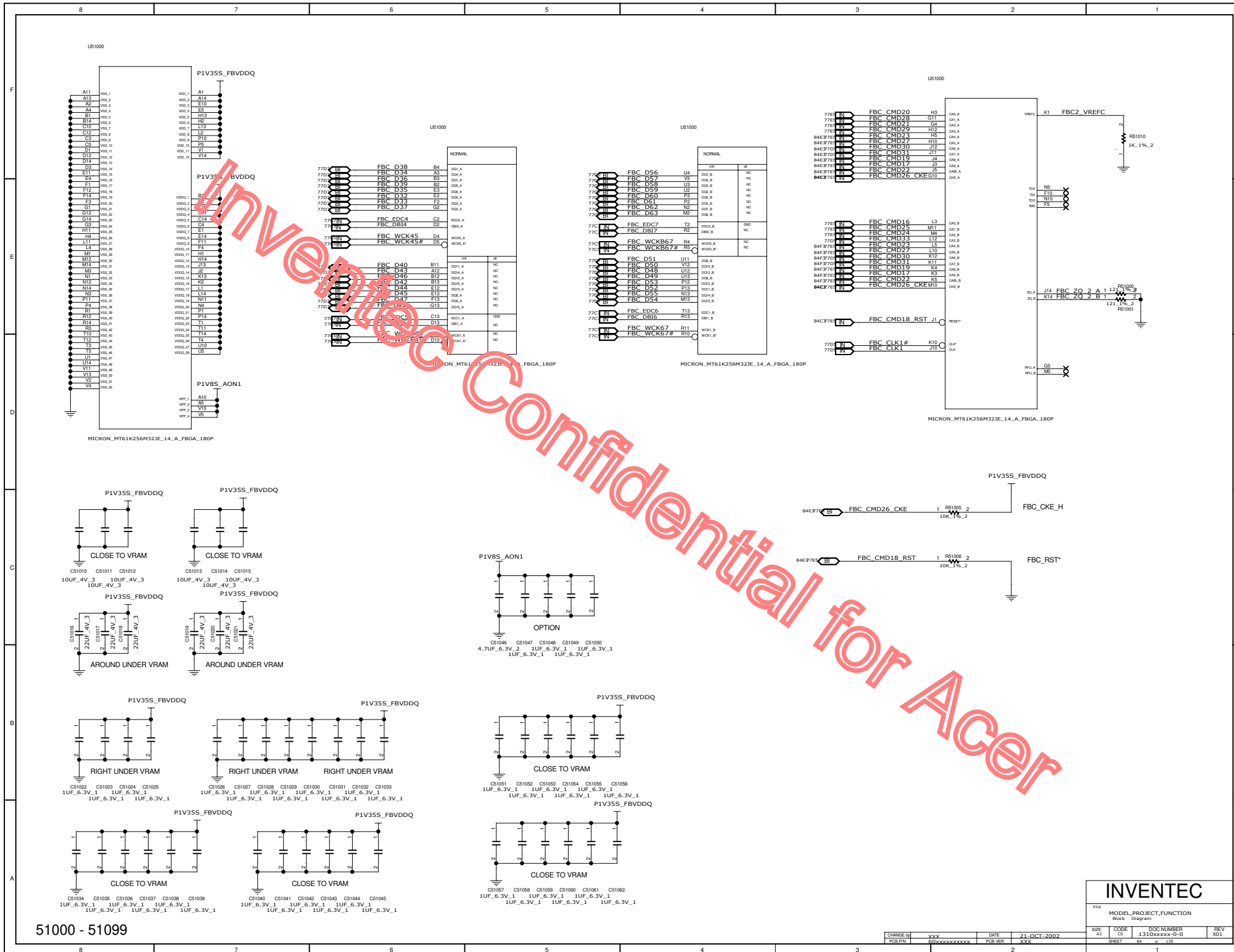
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MODEL, PROJECT, FUNCTION			
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SHEET		1	

CHANGE D1	XXXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX



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$$CL = 2 \cdot 10 - (5 + 3) = 12$$
$$CL_{trim} = 2 \times C_{Load} - (C_{stray} + C_i)$$

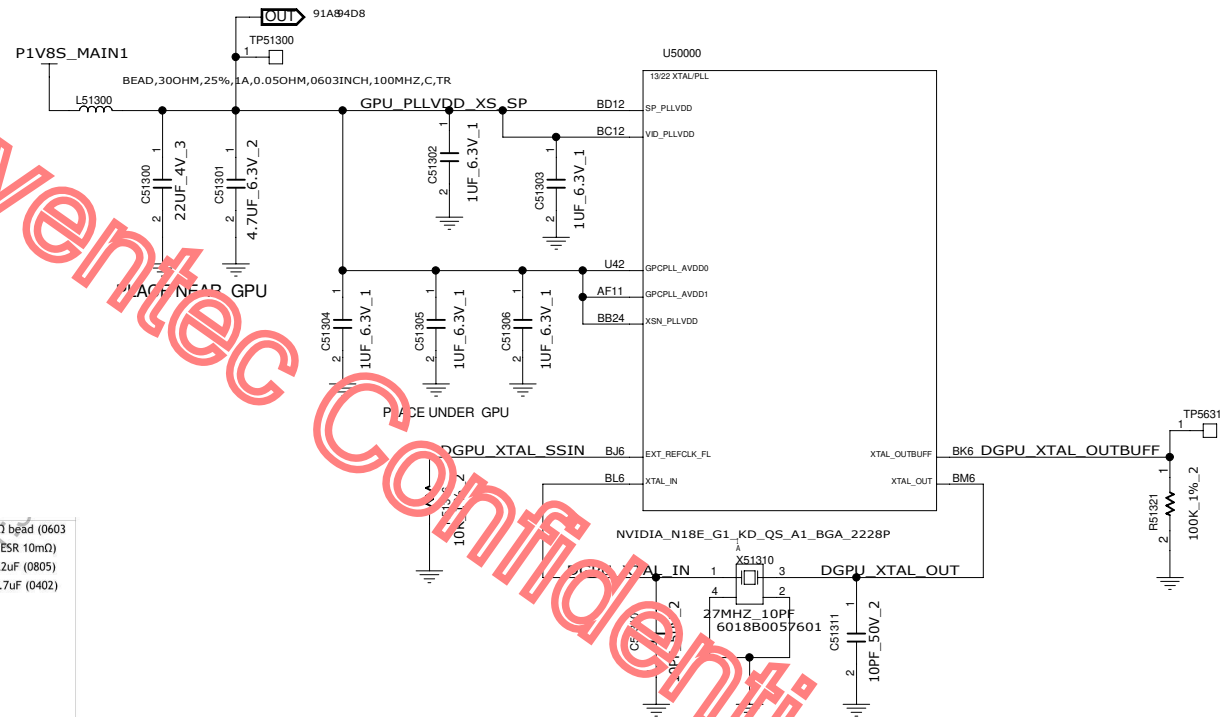
Where:

- ▶ C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- ▶ C_{Stray} is $\sim 3\text{pF}$ (Stray capacitance of XTAL pads and any significant trace routing)
- ▶ C_i is pin capacitance (5pF)

Typical CL_{trim} = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X65)	1 x 300 bead (0603)
IFPCD_PLLVDD	1			max ESR 10mΩ
IFPEF_PLLVDD	1		Alternate solution: 3 x 1.0uF (0201W X65)	1 x 22uF (0805)
				1 x 4.7uF (0402)
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X65)	
			Alternate solution: 3 x 1.0uF (0201W X65)	
SP_PLLVDD	1		1 x 0.47uF (0201W X65)	
			Alternate solution: 1 x 1.0uF (0201W X65)	
VID_PLLVDD	1		1 x 0.47uF (0201W X65)	
			Alternate solution: 1 x 1.0uF (0201W X65)	

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GPU VBIOS, EXTERNAL STRAPS

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

Strap Pins, See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	L	1	0	0	0
L	L	H	1	0	0	1
L	H	L	1	0	1	0
L	H	H	1	0	1	1

Table 12.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE						
Strap Pins see Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	L	1	0	0	0
H	L	H	1	0	0	1
H	H	L	1	0	1	0
H	H	H	1	0	1	1
L	L	L	1	0	1	0
L	L	H	1	0	1	1
L	H	L	1	0	1	0
L	H	H	1	0	1	1
M	M	M	1	0	0	0
M	M	M	1	0	0	1
M	M	M	1	0	1	0
M	M	M	1	0	1	1
M	M	M	1	0	1	1
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M	M	M	1	0</		

DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14

MICRON MT61K256M32JE-14-A

6019B1847601

6019B1847701

STRAP 0X0=000

STRAP 0X1=001

SAMSUNG-R51431 STUFF

MICRON-R51430 STUFF

R51430 NOT STUFF

R51431 NOT STUFF

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBW/DQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Alert	Qual Plan	Status
8 Gb	2Chx256Mb16	1.23V	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
	and 1.35V		Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:

1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.

2. DQS is required. WCK: TBD

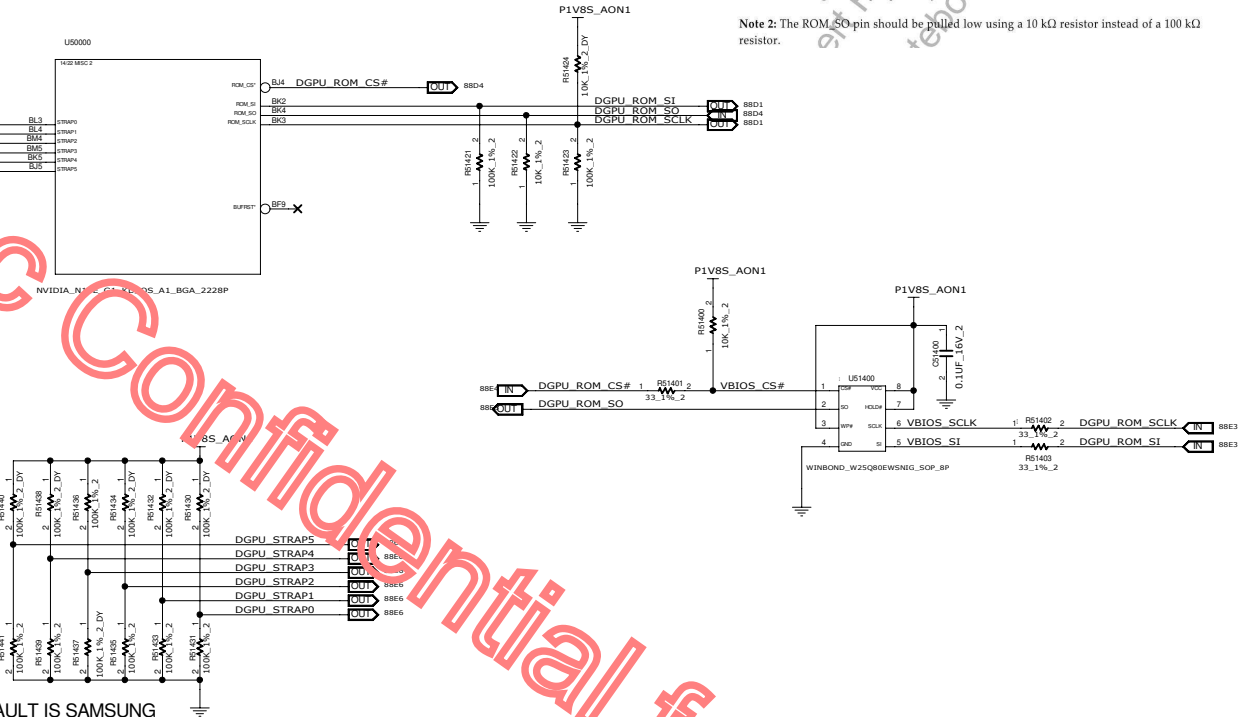


Table 7. Thermal Specifications

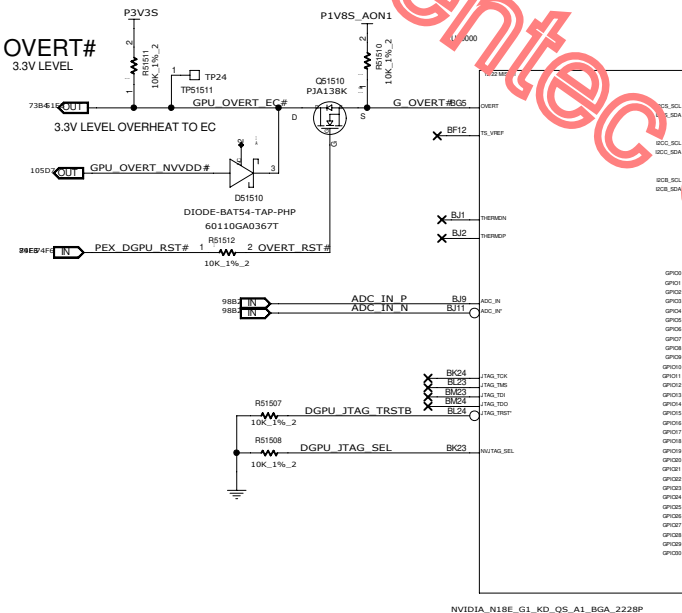
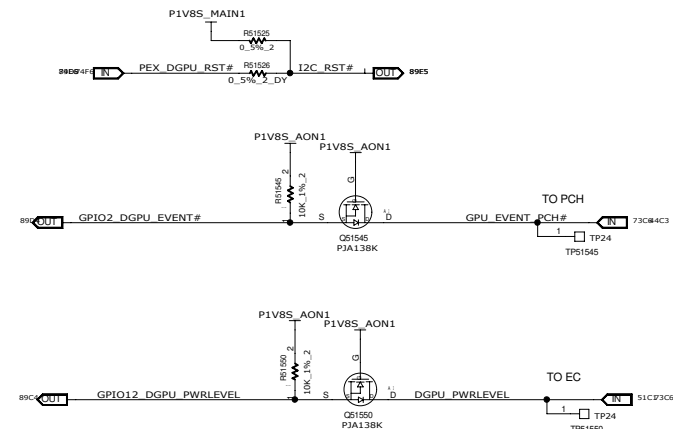
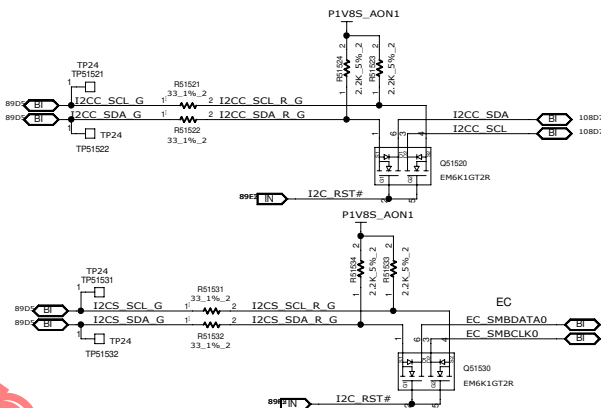
Table 7. Thermal Specifications

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, R_{JC})	0.014	0.017	0.017	TBD	°C/W
Thermal Resistance (Junction to PCB Board, R_{JA})	0.64	0.96	0.96	TBD	°C/W
GPU Shutdown Temperature (OVERT) ¹	99	99	99	TBD	°C
GPU Slowdown Temperature (THERM_ALERT) ²	94	94	94	TBD	°C

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature ¹	89	89	89	TBD	°C
GPU Target Temperature	87 (Default) 75 (Min)	87 (Default) 75 (Min)	87 (Default) 75 (Min)	TBD	°C

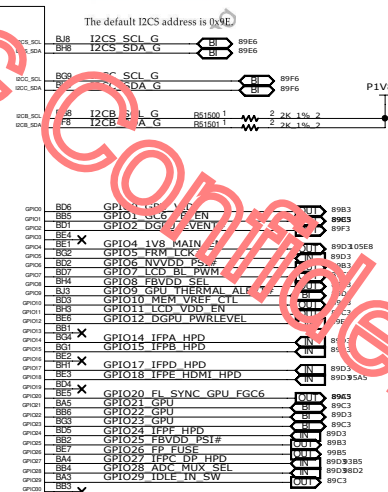
Notes:

1. OVERT results in an 87.5% (18) hardware clock slowdown.
2. THERM_ALERT results in a 50% (12) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clock) under the total board power level.

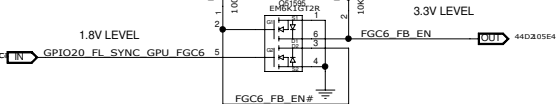
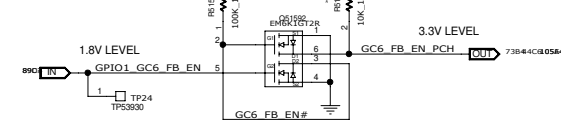


13.3.2.1 I2CS Slave Address

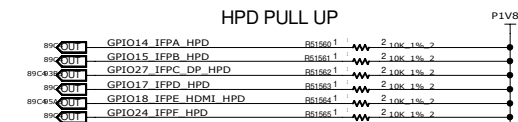
100% 90% 80% 70% 60% 50% 40% 30% 20% 10% 0%



NVIDIA_N18E_G1_KD_QS_A1_BGA_2228



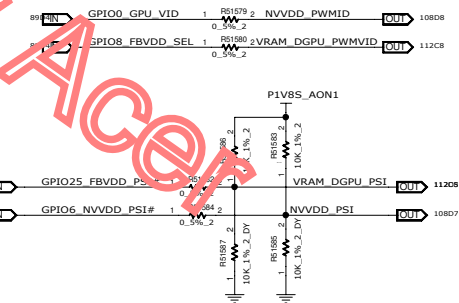
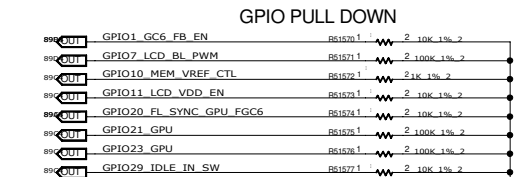
HPD PULL UP



GPIO PULL UP



GPIO PULL DOWN

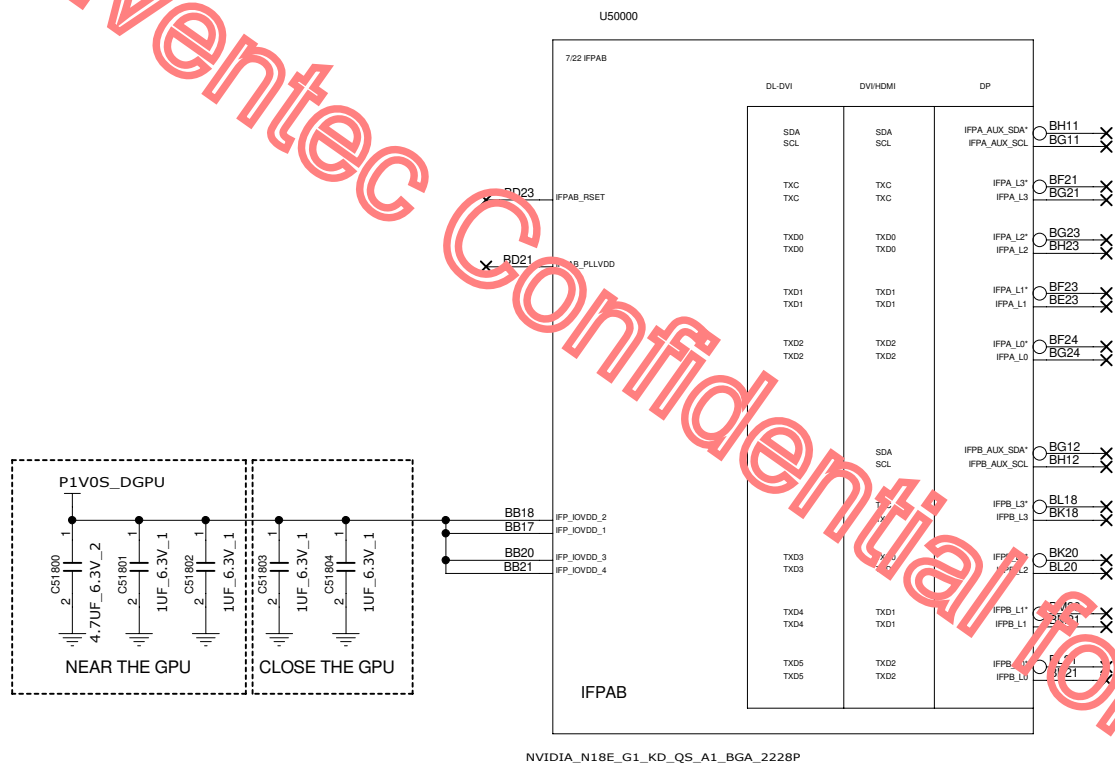


53900 - 54199
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INVENTEC

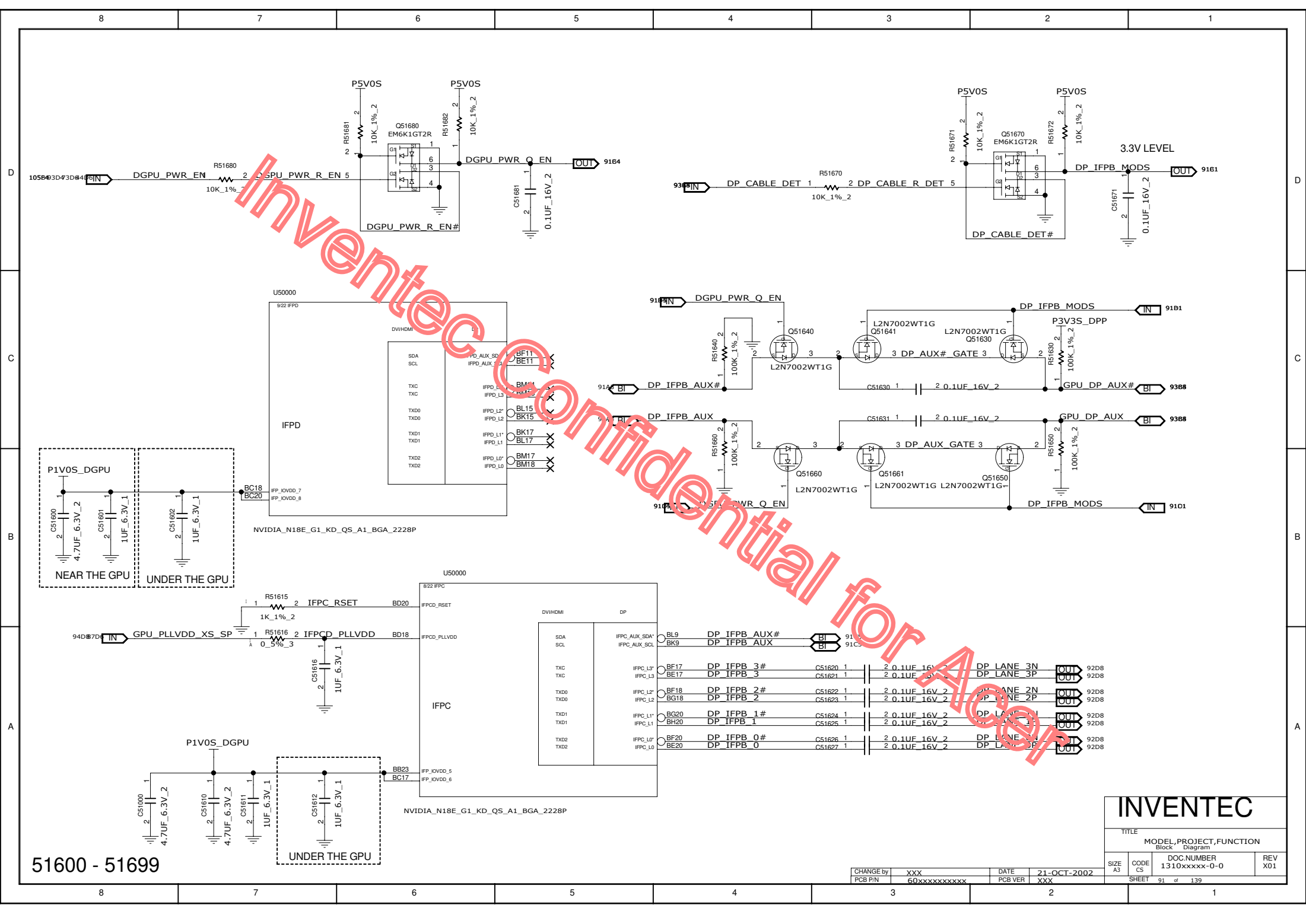
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Inventec Confidential for Acer



51800 - 51899

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
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PCB P/N		PCB VER	XXX	
SHEET		90 of	139	

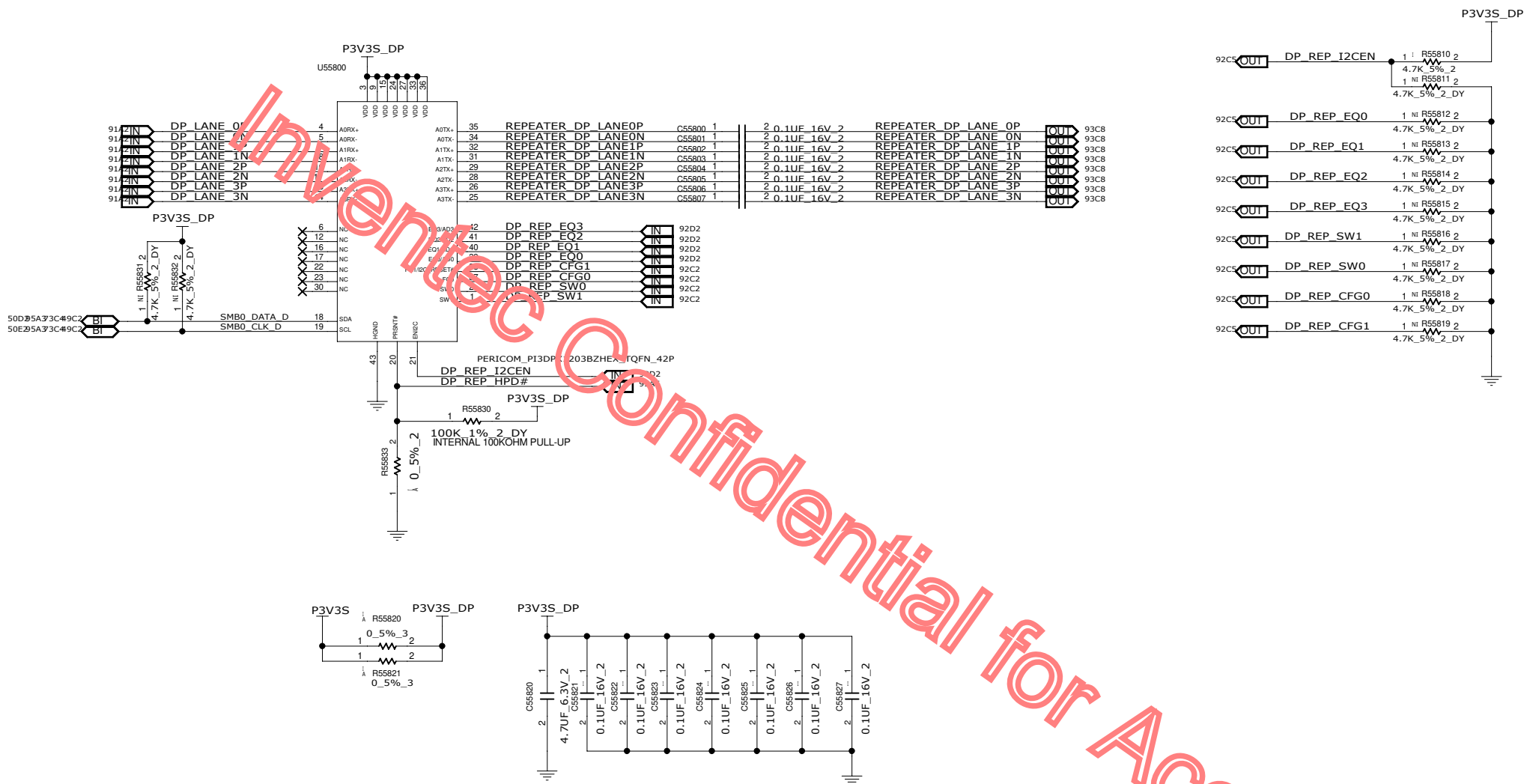


51600 - 51699

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC. NUMBER		REV
A3	CS	1310xxxx-0-0		
SHEET		91 of 139		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

DP REDRIVER



55800 - 55999 56000 - 56199

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET	92 of 139		

INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

SIZE	CODE	DOC.NUMBER 1310xxxxx-0-0	REV X01
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A3	CS	10/10/2010		
SHEET		92	of	139

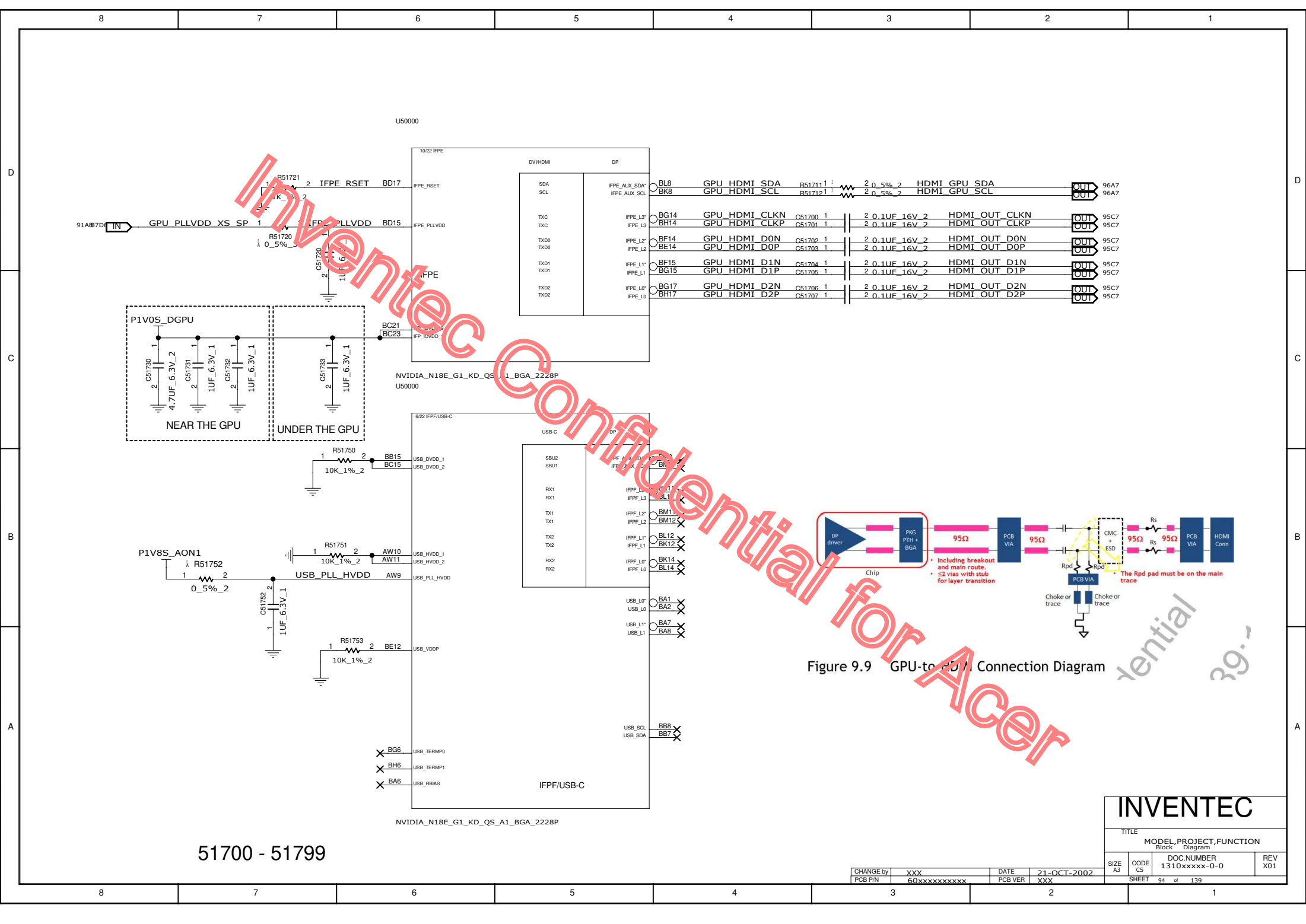
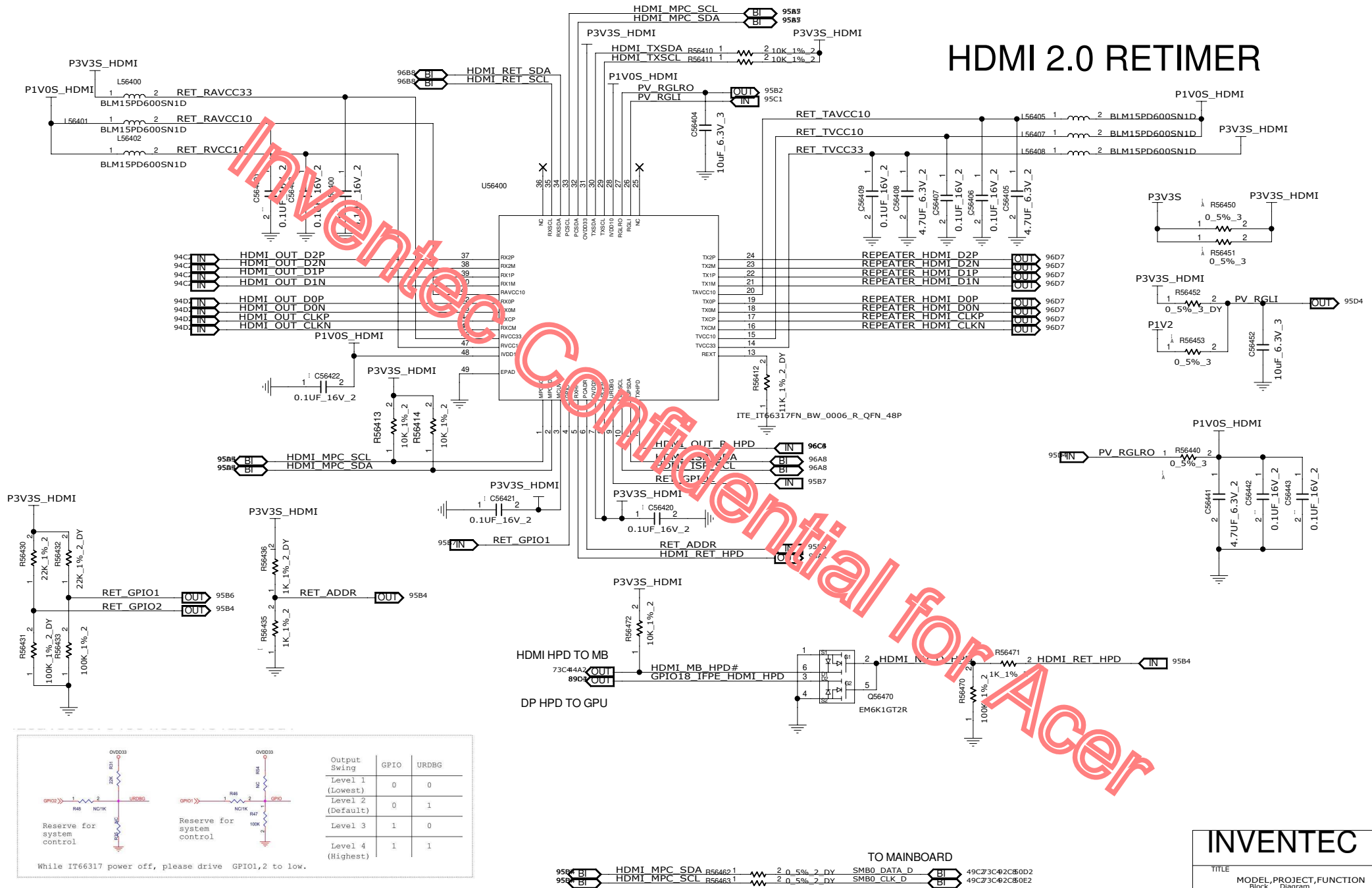


Figure 9.9 GPU-to-PD/A Connection Diagram

51700 - 51799

INVENTEC				
TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX	SHEET 94 of 139

HDMI 2.0 RETIMER



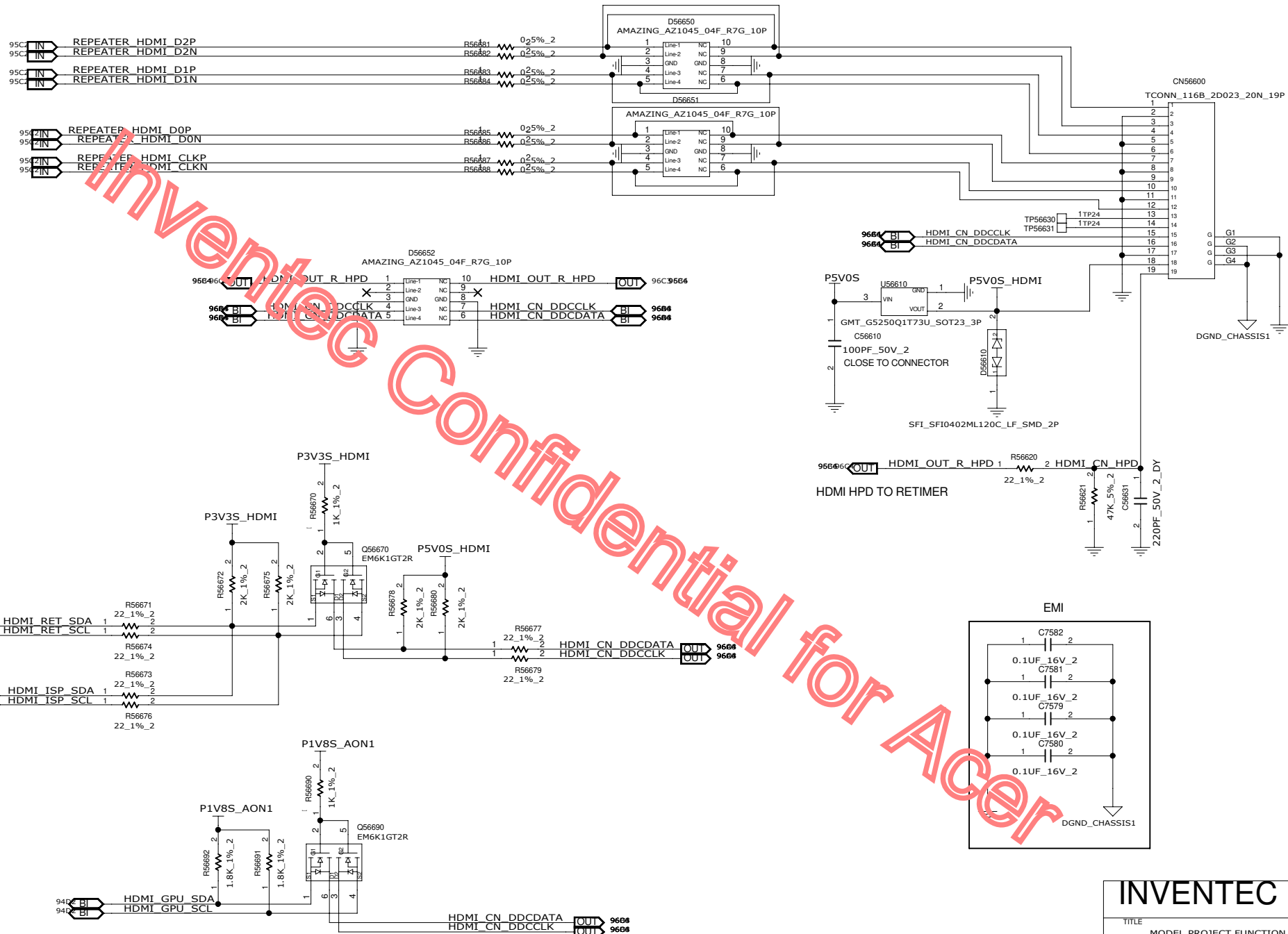
56400 - 56599

TO MAINBOARD

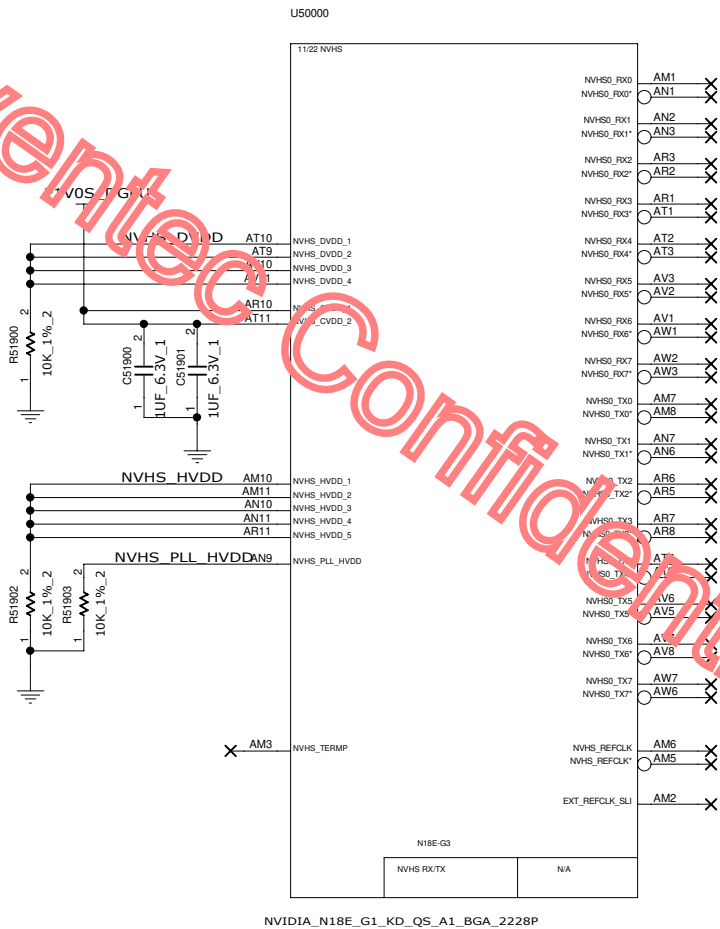
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 95 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



Inventec Confidential for Acer

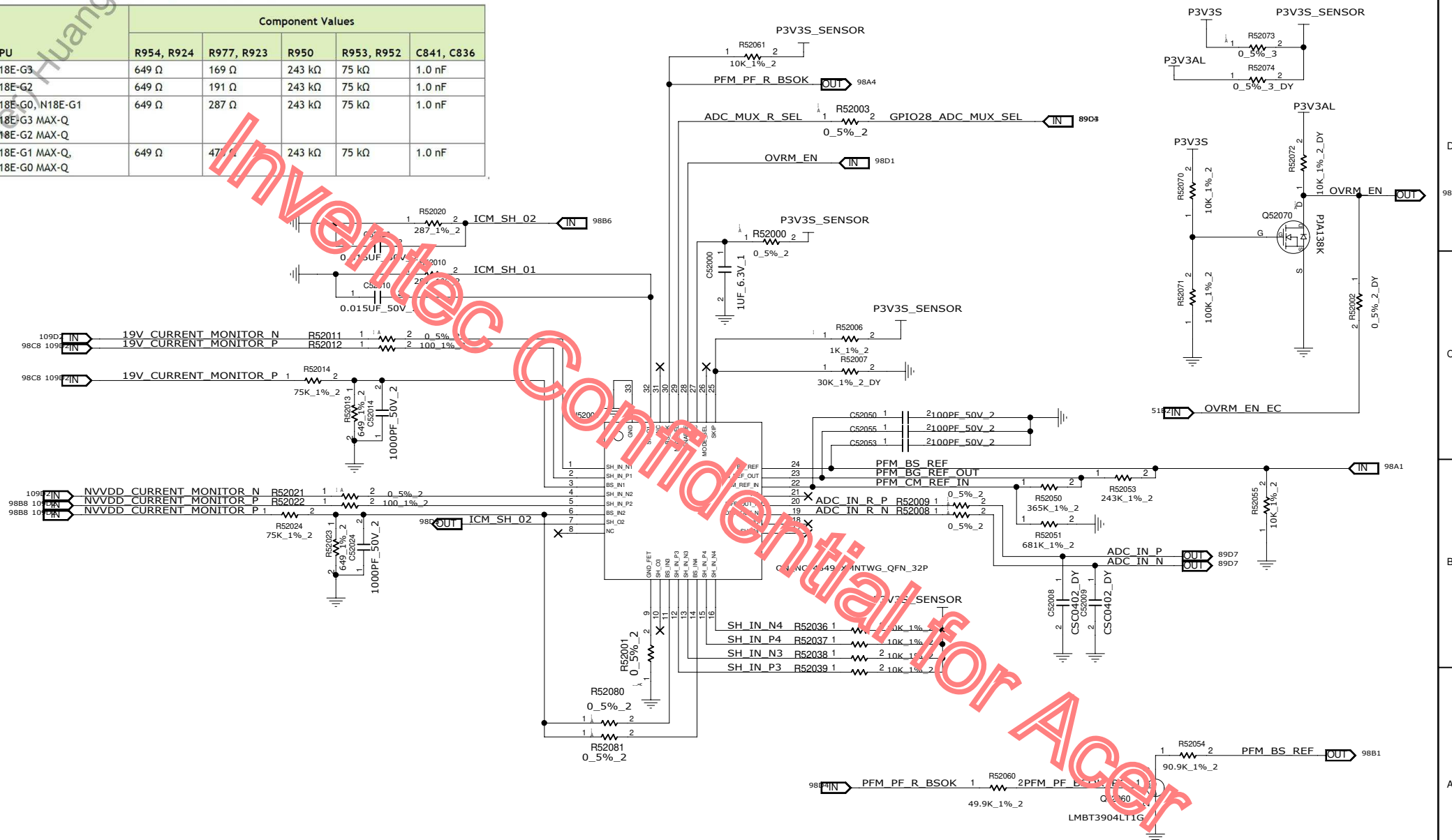


51900 - 51999

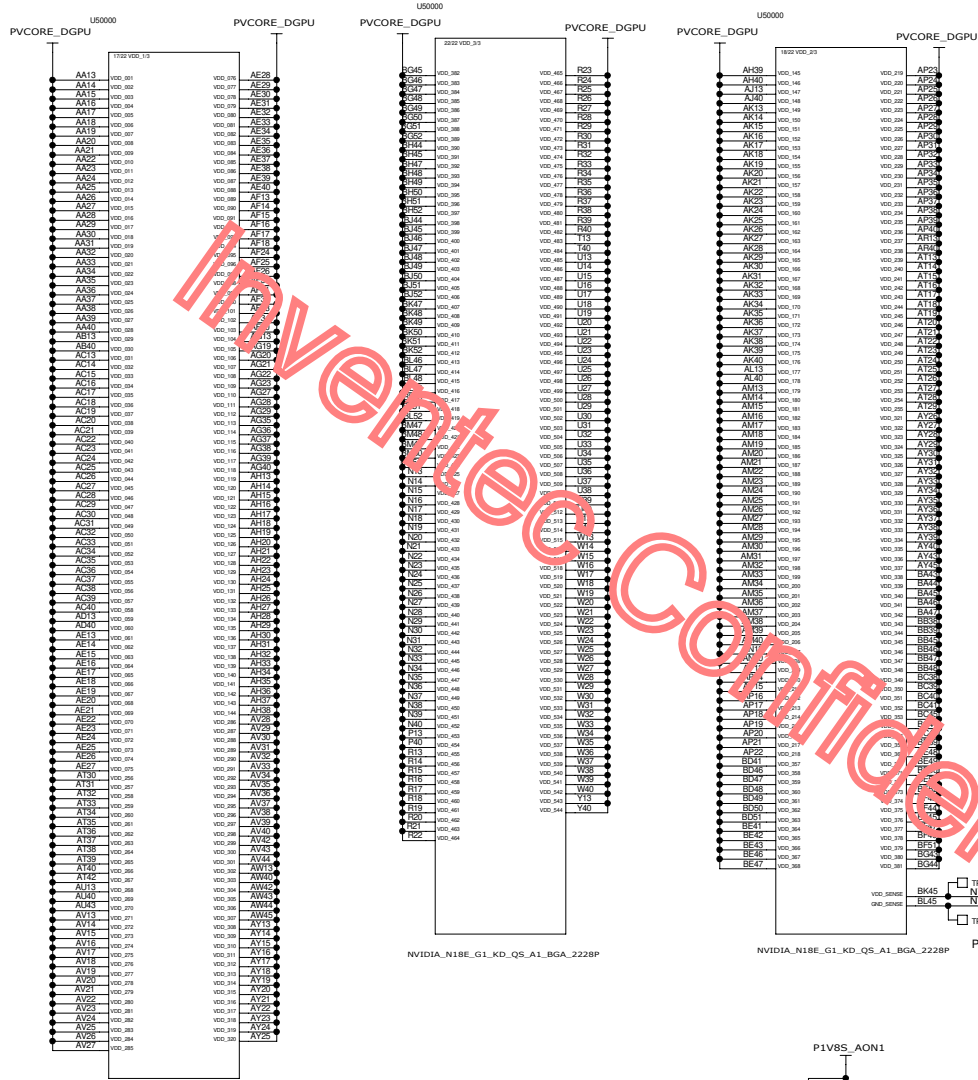
INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC. NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
SHEET 97 of 139				

Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G3 MAX-Q					
N18E-G2 MAX-Q					
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF



52000 - 52099



The required subcircuit is shown in detail in Figure 15.6.

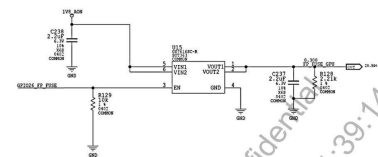
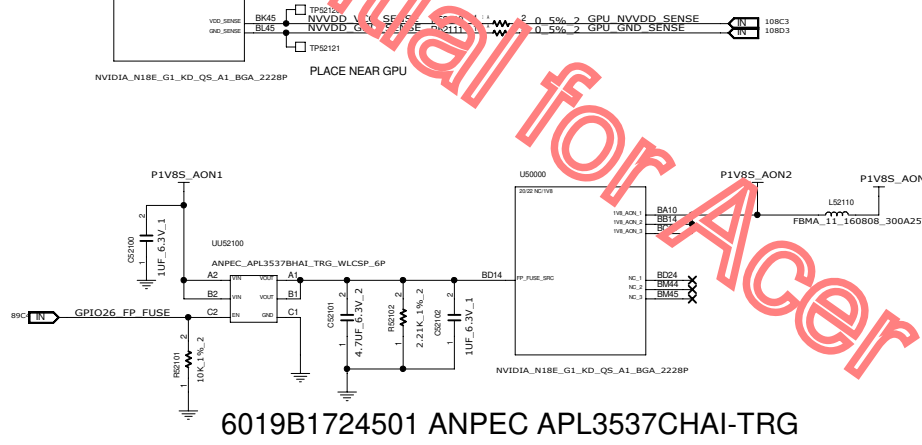
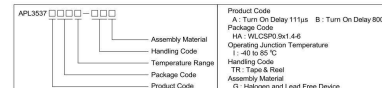


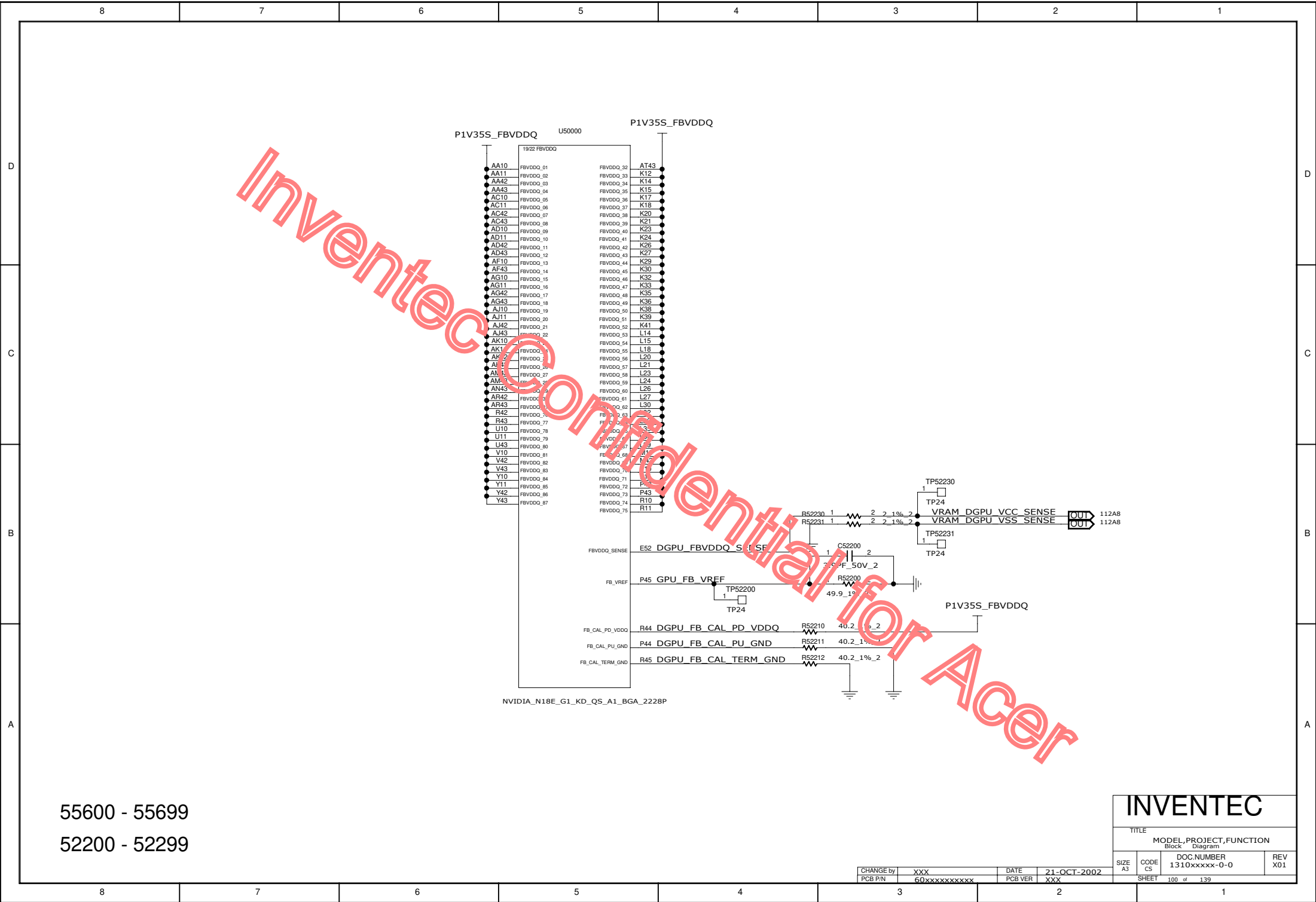
Figure 15.6 Subcircuit Schematic

- In Figure 15.6, the component labeled "U15" is an active switch; devices equivalent to the GS7165C-R are acceptable as long as they meet the following requirements:
- ▶ The active switch must be capable of driving 100mA or more.
 - ▶ The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100ms or less.
 - ▶ There must be no glitch during power up or GPGCC-Off entry or exit.
 - ▶ The FP_FUSE_GPU output trace width must be 0.25 mm (10 mil) or greater.

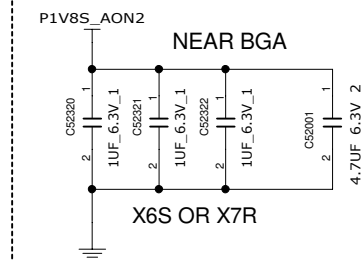
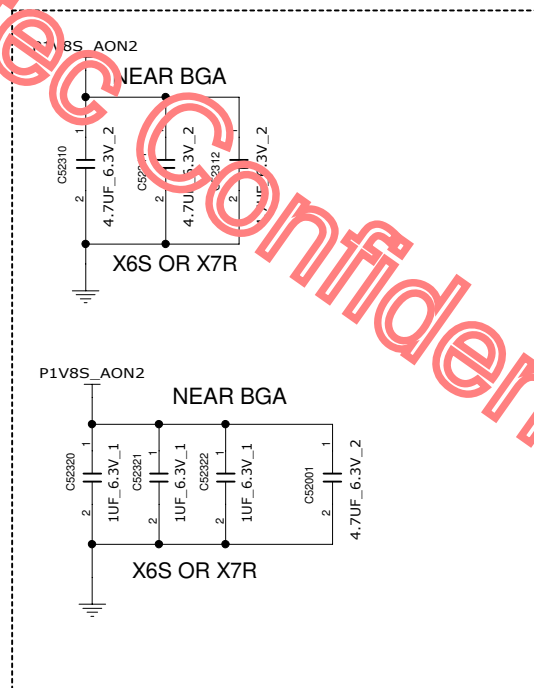
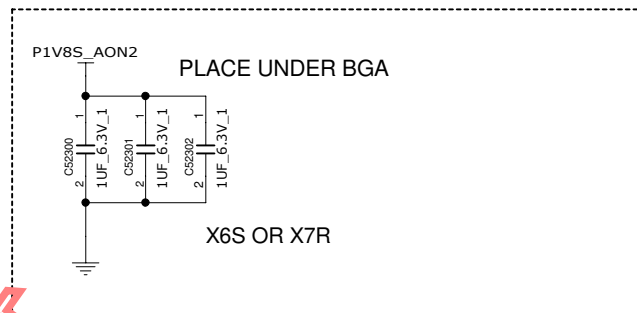


6019B1724501 ANPEC APL3537CHAI-TRG





GPU 1V8_AON DECOUPLING



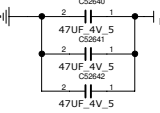
1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S)	3 x 1uF (0402 X6S)
			Alternate solution:	3 x 4.7uF (0603 X6S)
			3 x 1.0uF (0201W X6S)	

52300 - 52399

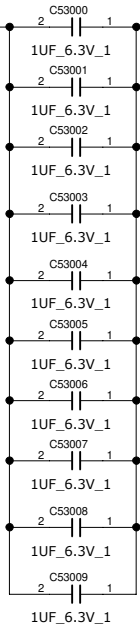
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

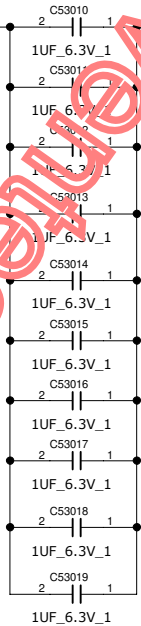
SHEET	101 of 139
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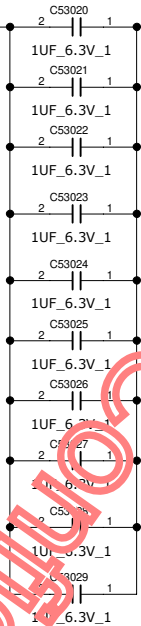
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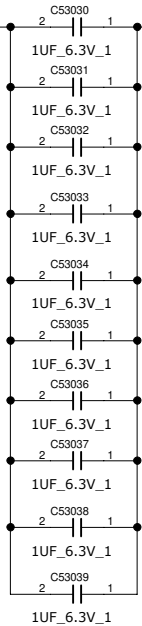
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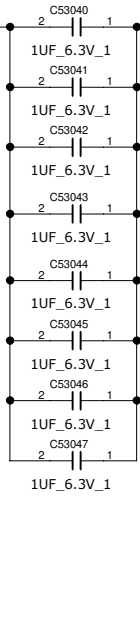
P1V35S_FBVDQ



P1V35S_FBVDQ

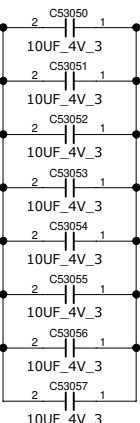


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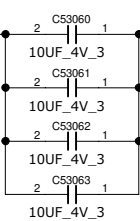
PLACE UNDER GPU

P1V35S_FBVDQ



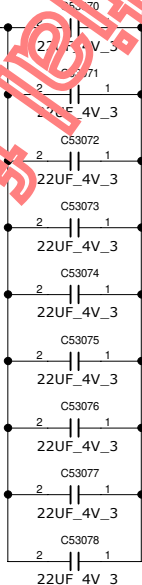
PLACE UNDER GPU

P1V35S_FBVDQ



PLACE NEAR GPU

P1V35S_FBVDQ



Herbert
tec Net

FBVDQ (GPU side)
25V
48 x 0.47uF (0201W X65)
8 x 10uF (0603 X65)
4 x 10uF (0603 X65)
9 x 22uF (0603 X65)
Generate solution:
24 x 1.0uF (0201W X65) 2
8 x 10uF (0603 X65)

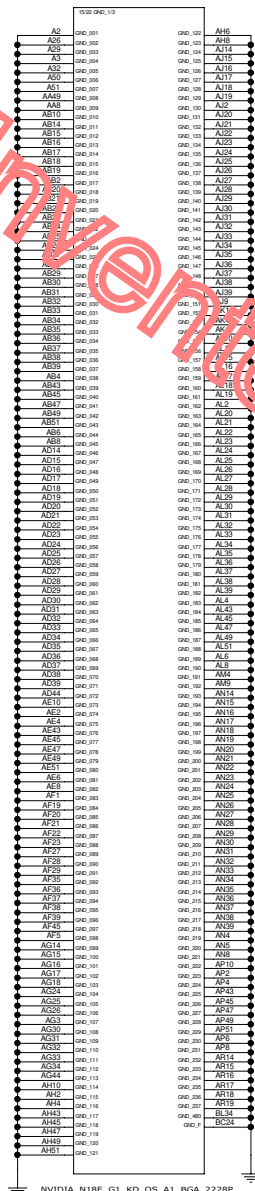
INVENTEC

INVENTEC									
TITLE									
MODEL, PROJECT, FUNCTION									
Block Diagram									
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SHEET		102 of		139					
CHANGE BY		XXX		DATE		21-OCT-2002			
PCB P/N		60XXXXXXXXXX		PCB VER		XXX			

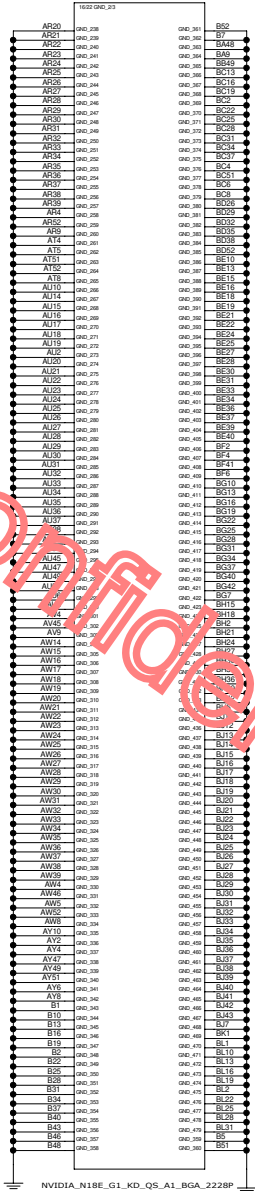
53000 - 53299

GND

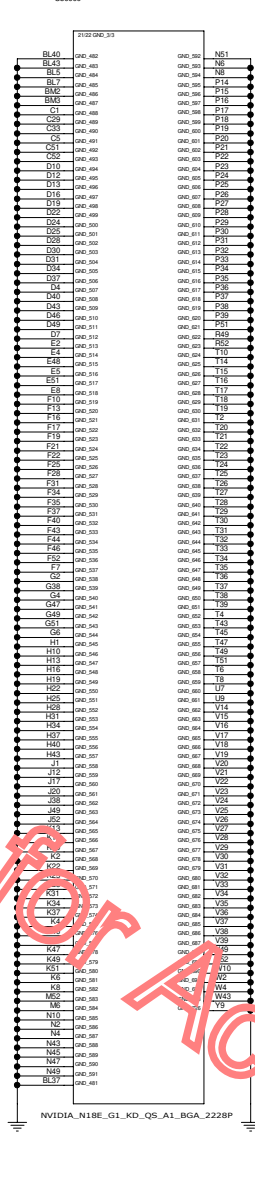
U50000



U50000



U50000



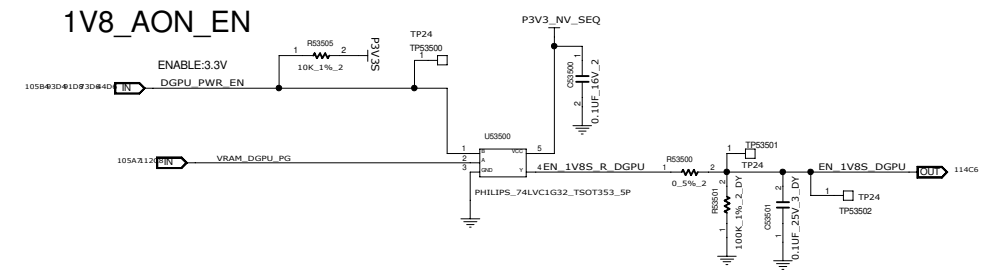
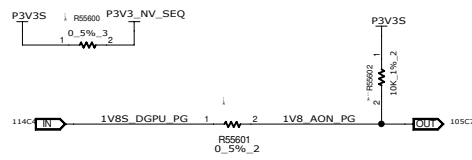
NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

53300 - 53499

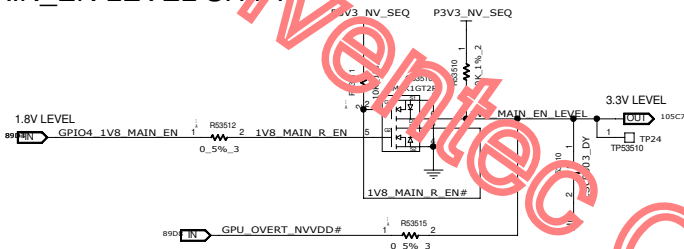
INVENTEC

MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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SHEET	104 of 130		

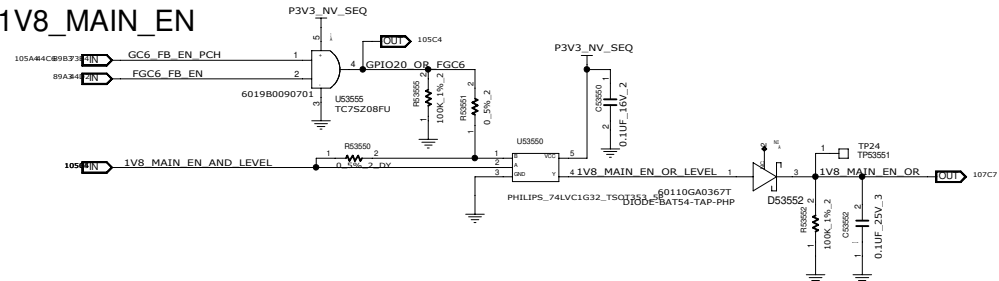
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PCB P/N	60xxxxxxxxxx	PCB VER	xxx



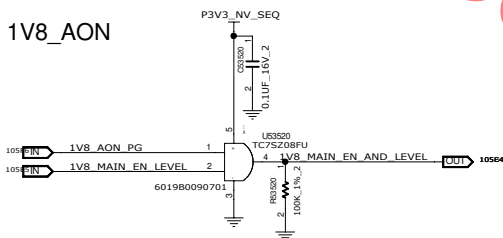
1V8_MAIN_EN LEVEL SHIFT



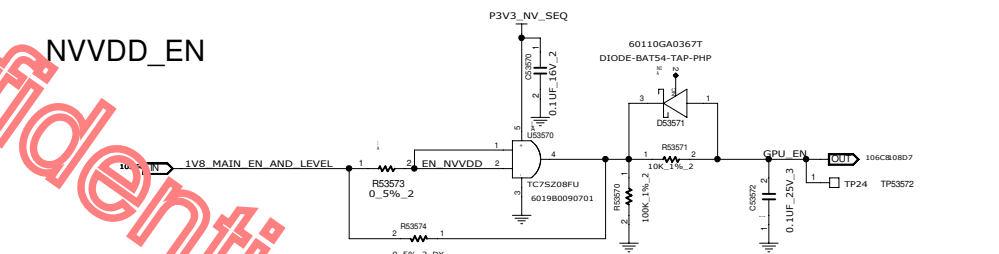
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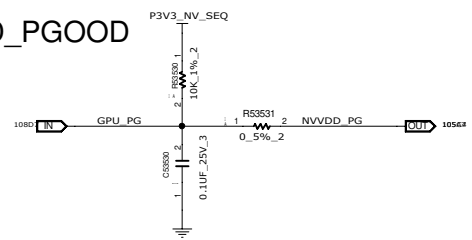
1V8_MAIN_EN AND WITH 1V8_AON



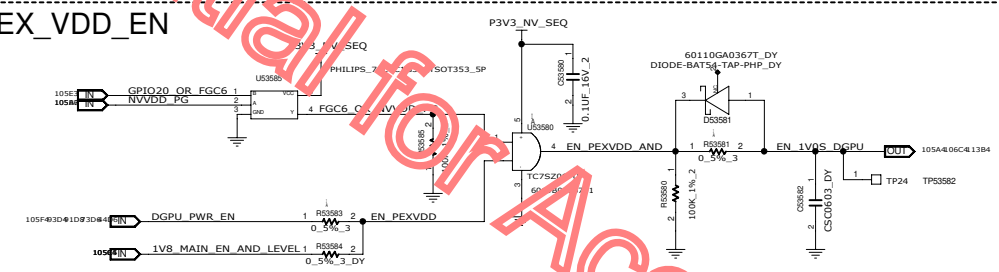
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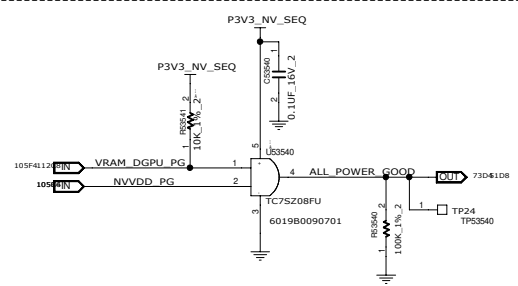
NVVD_PGOOD



PEX_VDD_EN

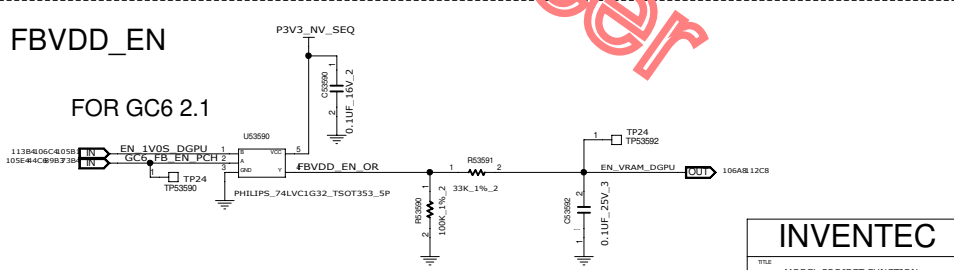


ALL POWER GOOD



FBVDD_EN

FOR GC6 2.1

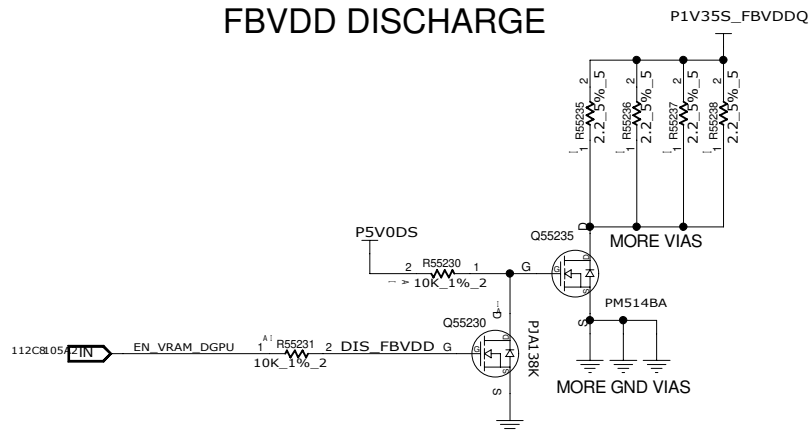
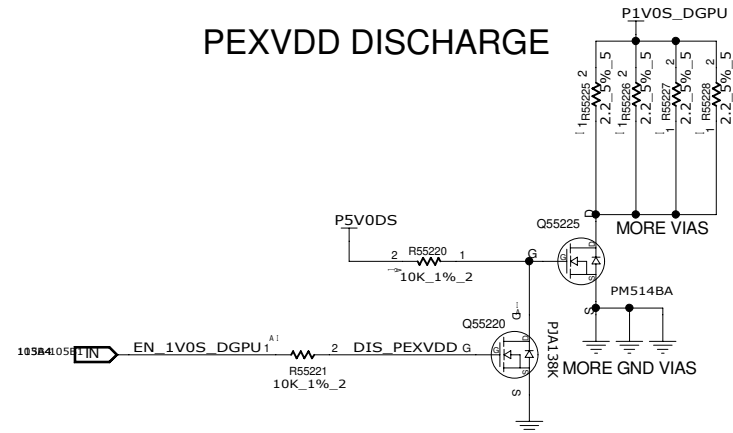
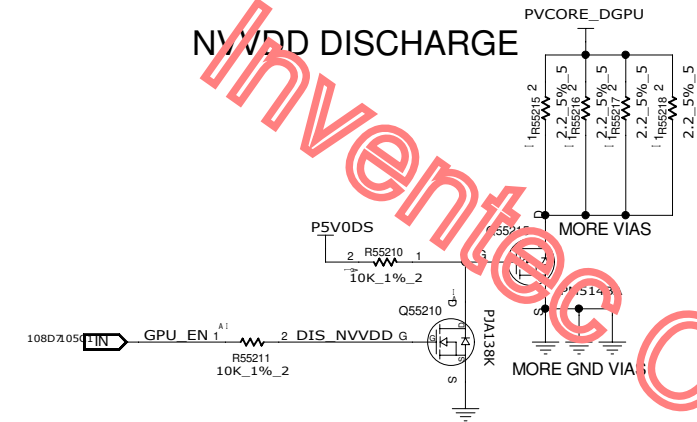


55600 - 55699
53500 - 53899

INVENTEC				
MODEL PROJECT FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	C5	1310xxxxx-0-0	X01	
SHEET 105 of 139				

CHANGE ID	DATE	21-OCT-2002
PCB PIN	PCB VER	XXX

A



55200 - 55299

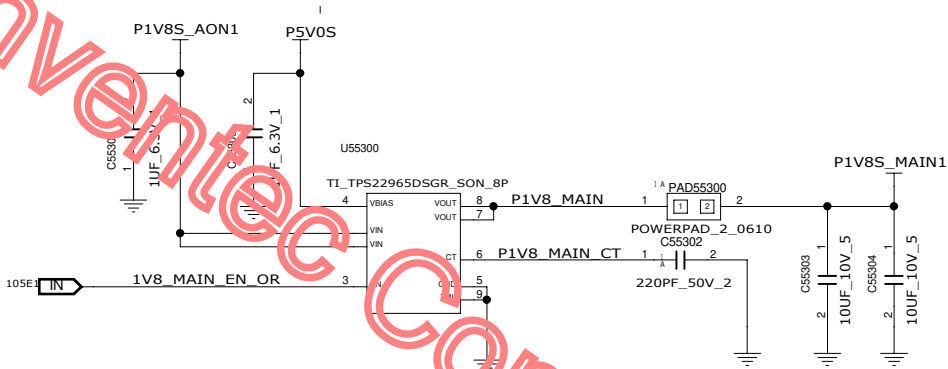
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	106	of	139		

INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		106 of 139	

1V8_MAIN



55300 - 55399

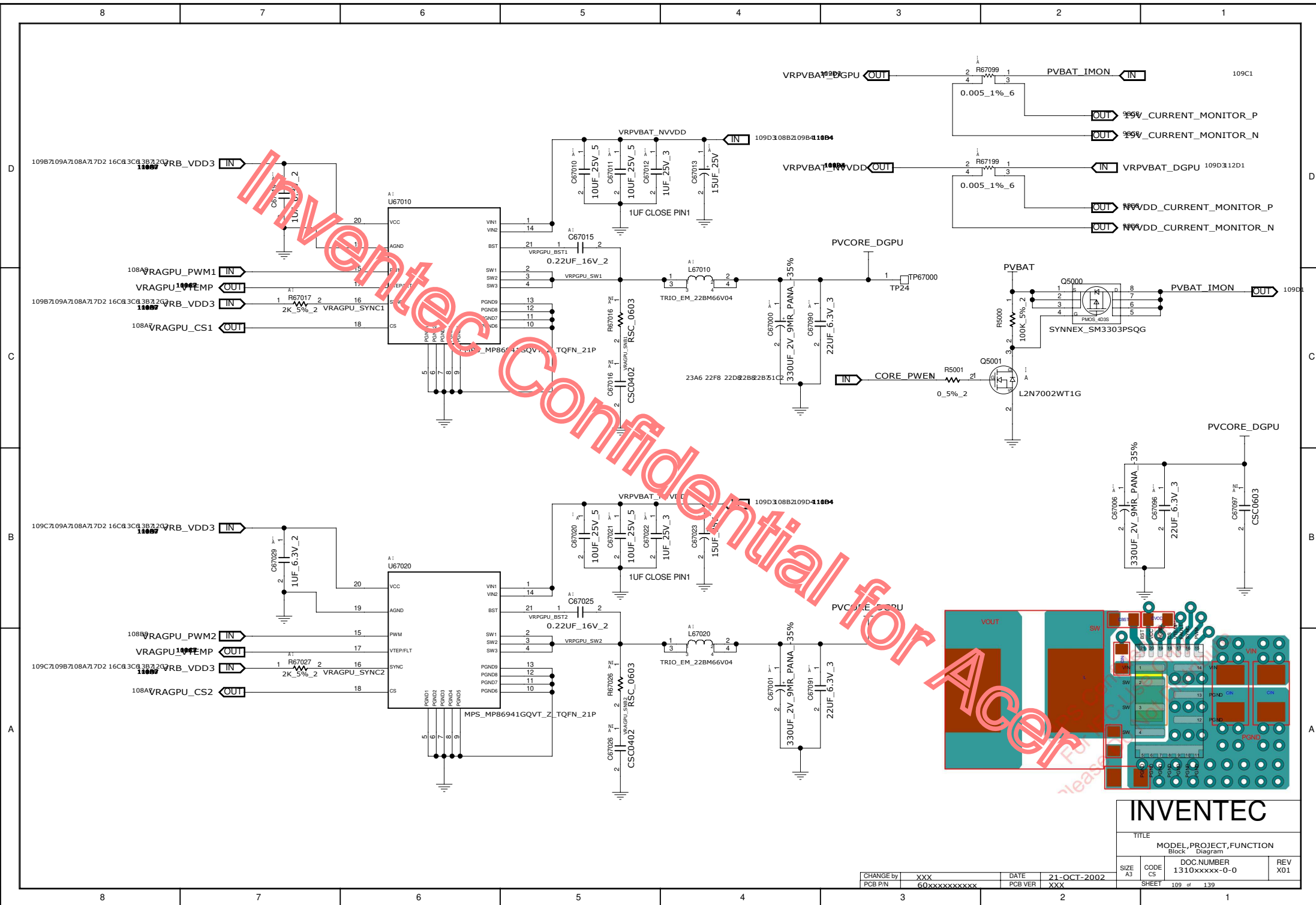
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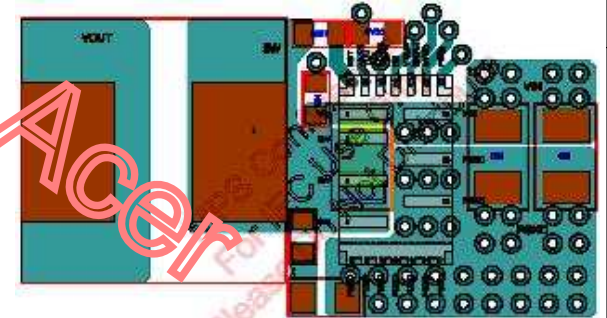
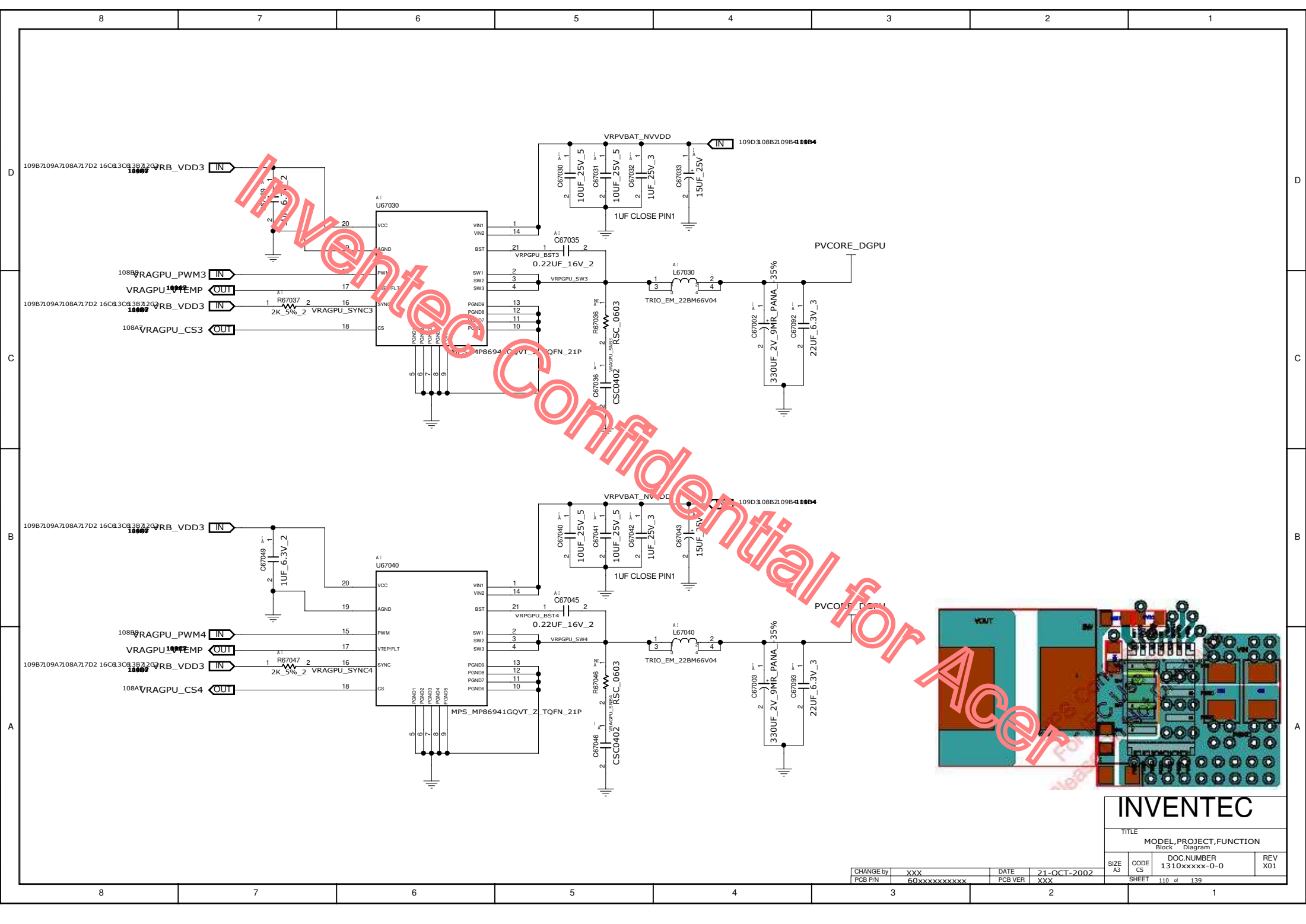
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

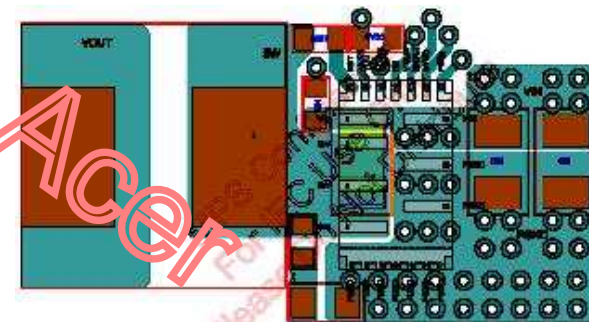
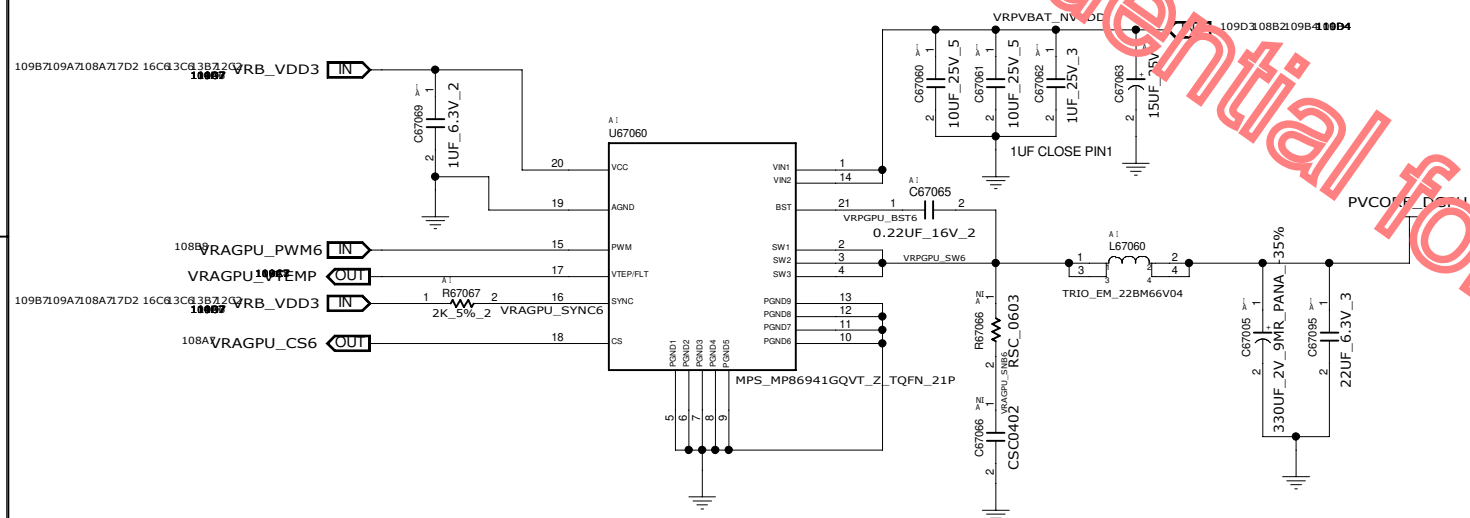
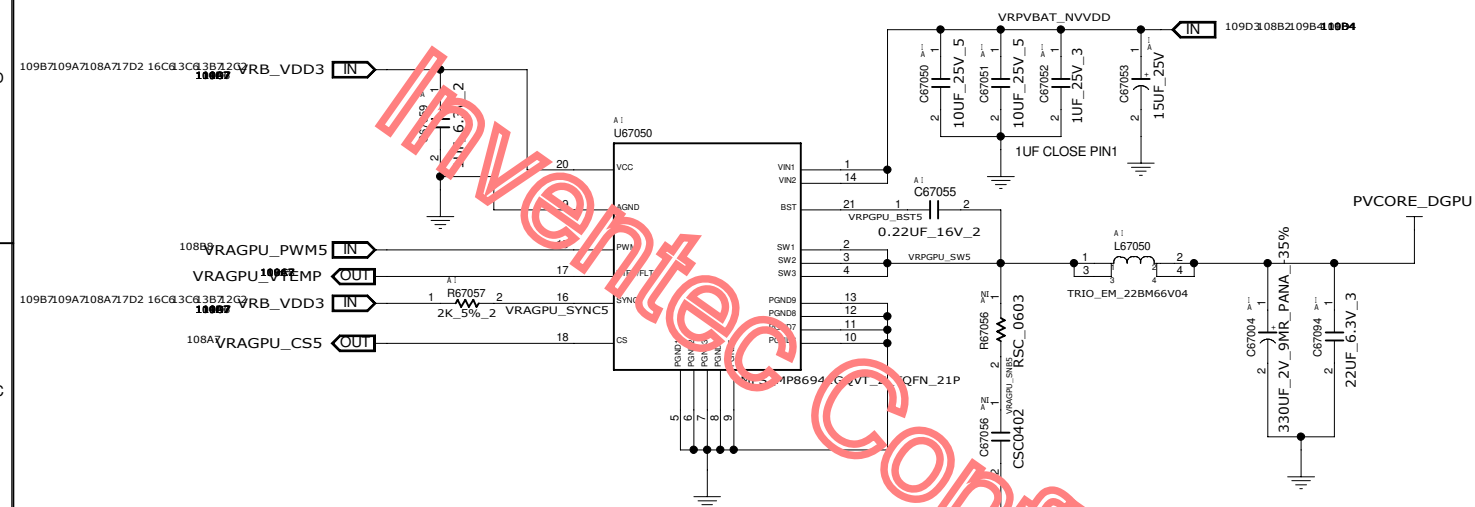
SHEET 107 of 139





INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		110 of	139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

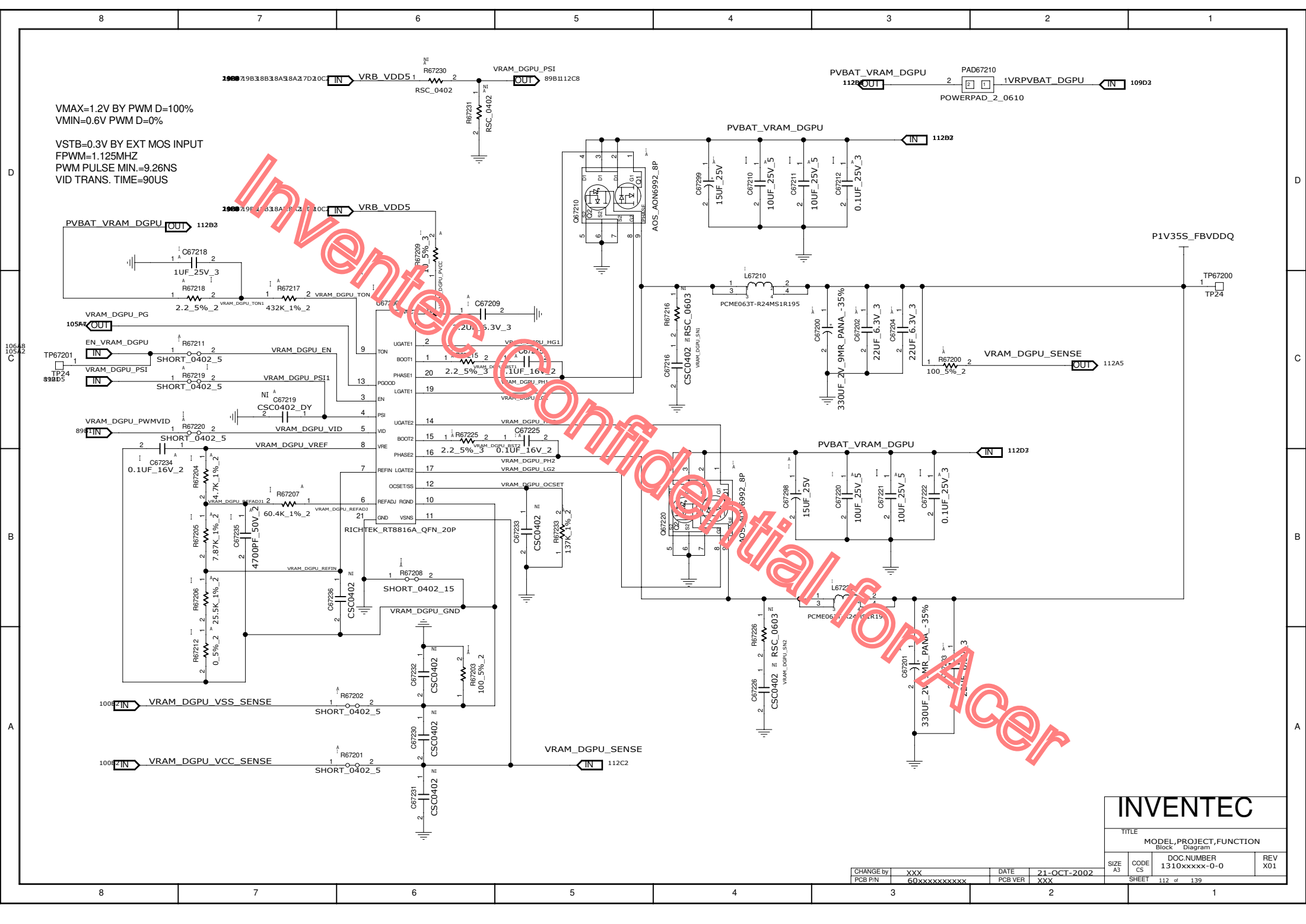


INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
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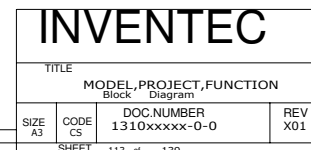
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 111 of 139			

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

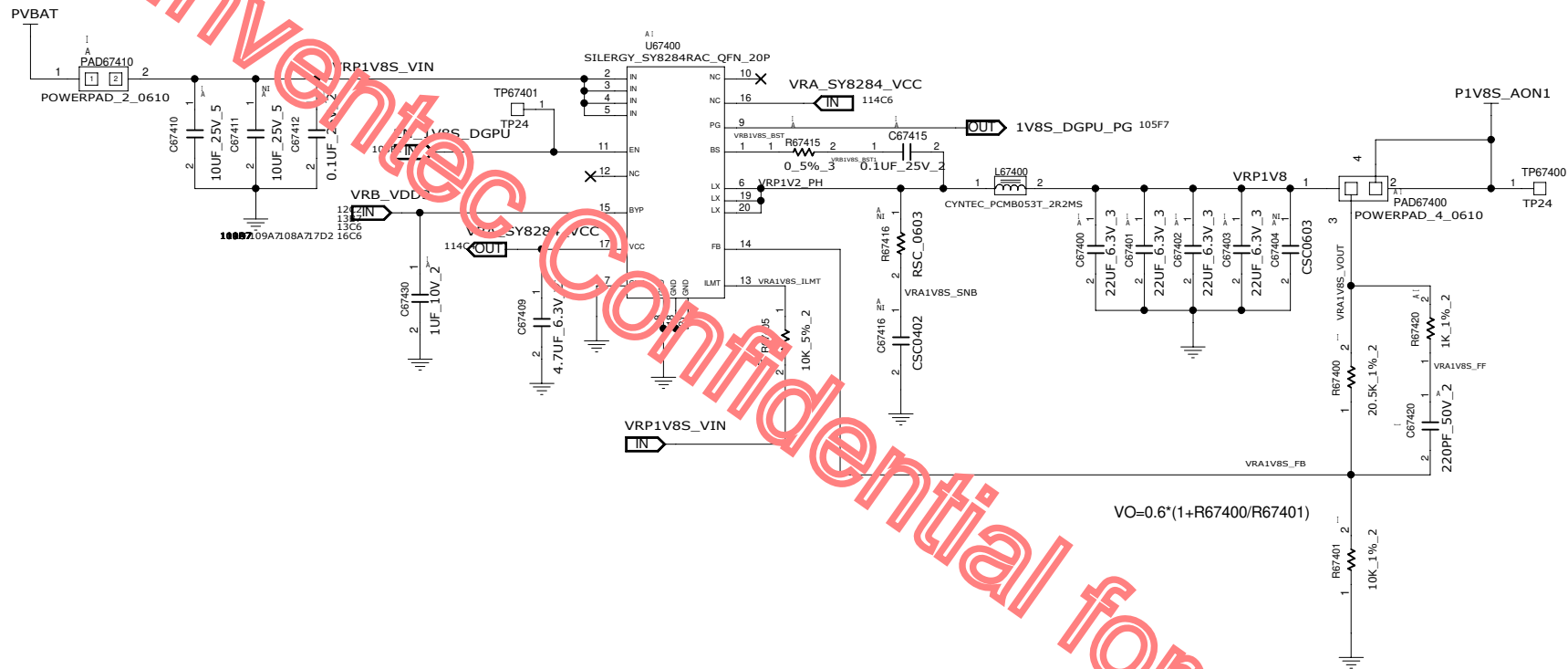


VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D=0%
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US

INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		112 of	139	



CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		SHEET	113 of 139	



$$VO=0.6*(1+R67400/R67401)$$

INVENTEC

TITLE
Block Diagram

MODEL, PROJECT, FUNCTION
1310xxxxx-0-0

SIZE A3 CODE CS REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 114 of 139

Table 12. Output EDP-Continuous

		NVVD	FB TOTAL ⁵	1.0V Total ¹	1.8V Total ²
Product	TGP (W)	(A)	(A)	(A)	(A)
N18E-G3	150	142	46	1.6	2.3
	160	152			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

		NVVD	FB TOTAL ⁴	1.0V Total ¹	1.8V Total ²
Product	TGP (W)	(A)	(A)	(A)	(A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms) ² (A)	Input EDPp (5ms) ² (A)	Input EDPc (1sec) ¹ (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$\text{Input EDPc Current (A)} = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$\text{Input EDPp (A) at } V_{\text{new}} = \text{Input EDPp (A) at } 19V \times \frac{19V}{V_{\text{new}}(V)}$$

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

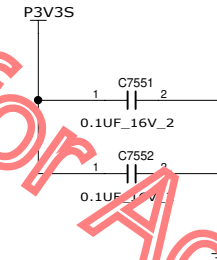
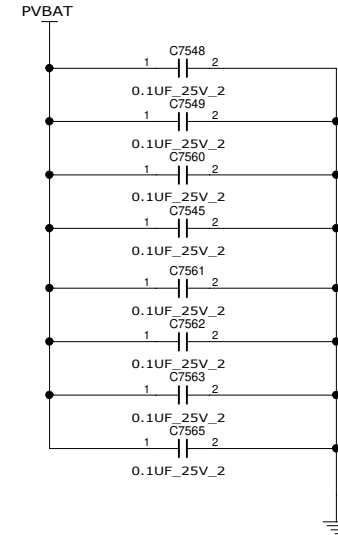
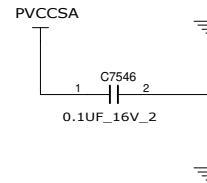
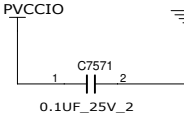
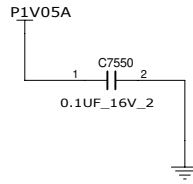
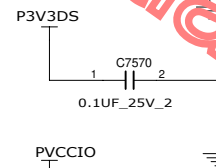
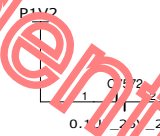
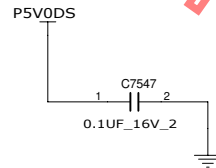
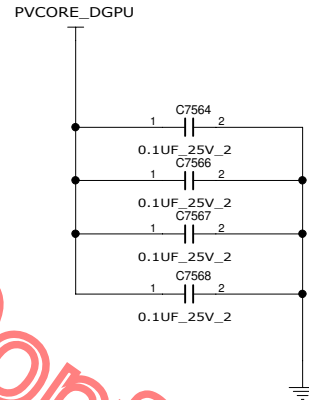
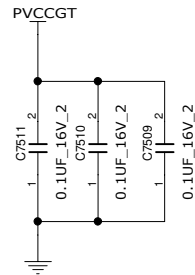
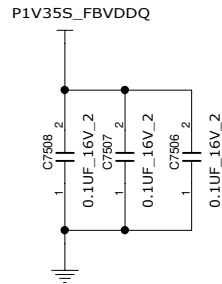
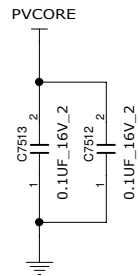
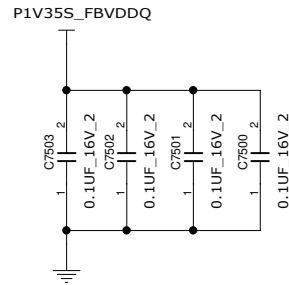
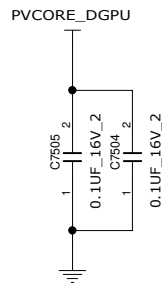
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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8	7	6	5	4	3	2	1
HISTORY							
SCHEMATIC MODIFY HISTORY							
Inventec Confidential for Acer							
INVENTEC							
TITLE							
MODEL, PROJECT, FUNCTION							
Block Diagram							
CHANGE by		XXX		DATE		21-OCT-2002	
PCB P/N		60xxxxxxxxxx		PCB VER		XXX	
SIZE		A3		CODE		CS	
SHEET		116 of		139		REV	
8		7		6		5	
3		2		1			

EMI



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
NFC_CNNL			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 117 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

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TURBO# BOARD

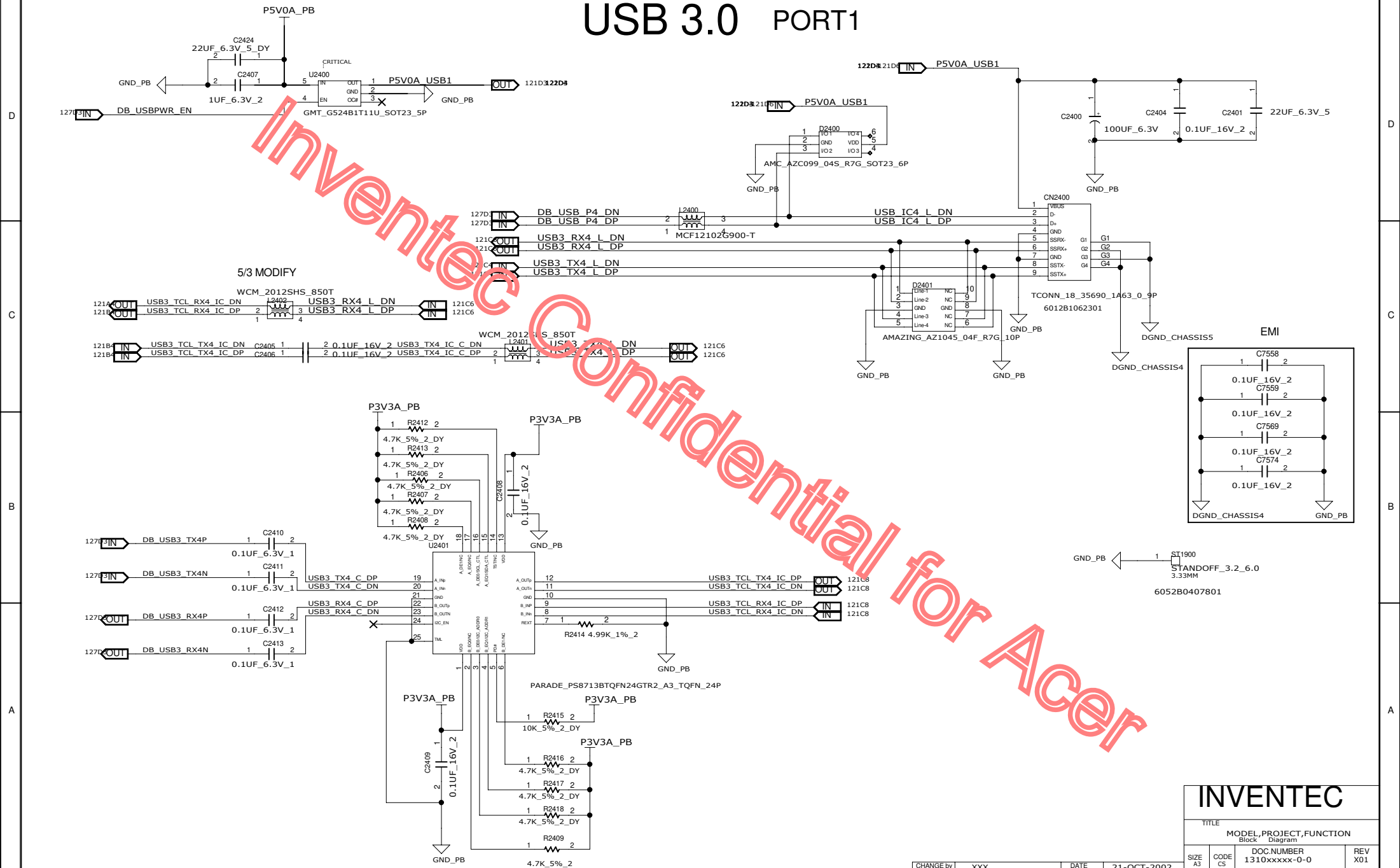
INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET

XXX	21-OCT-2002
60xxxxxxxxxx	XXX

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		SHEET	120 of 139	

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC NUMBER

1310xxxxx-0-0

REV

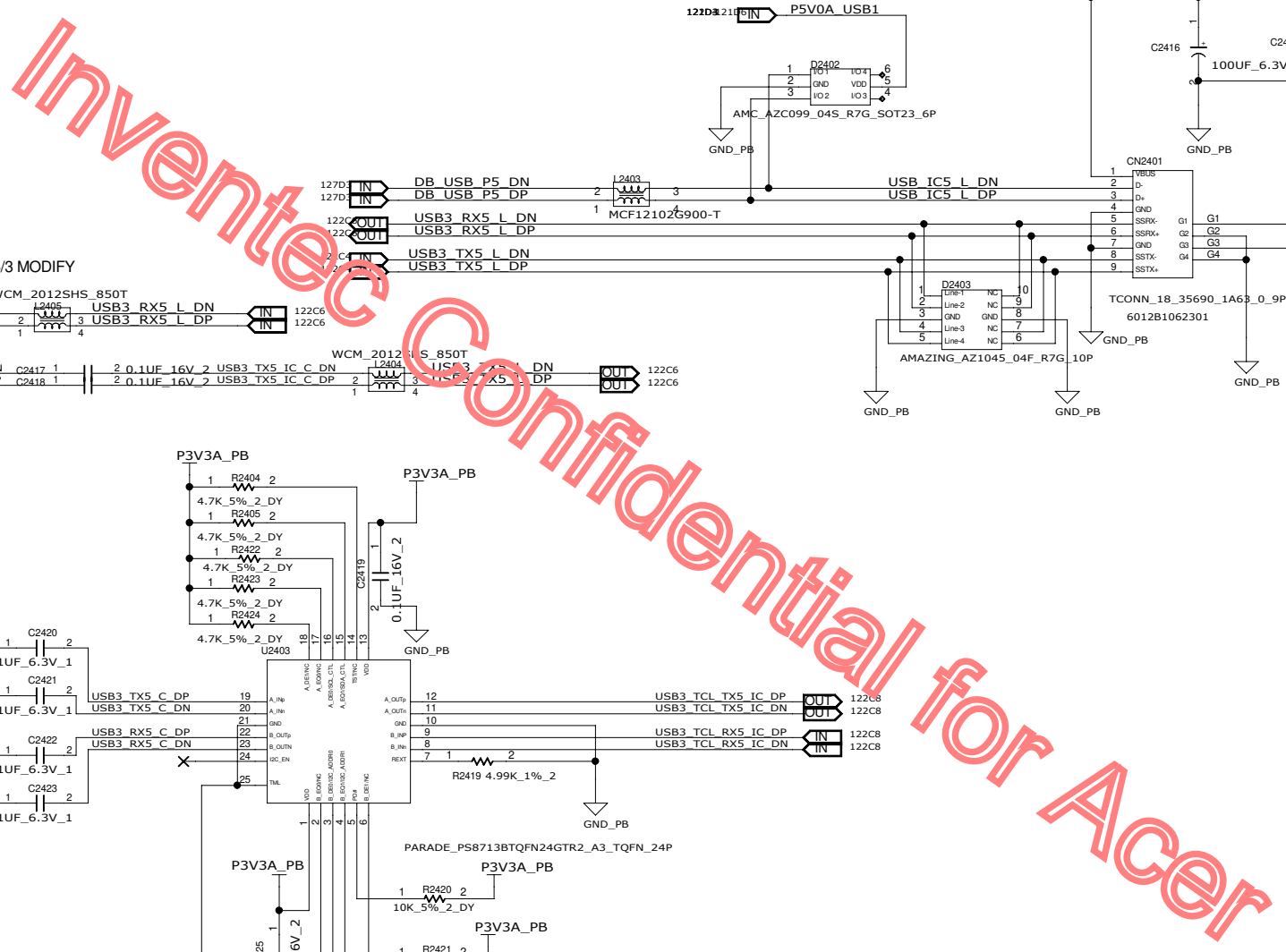
X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

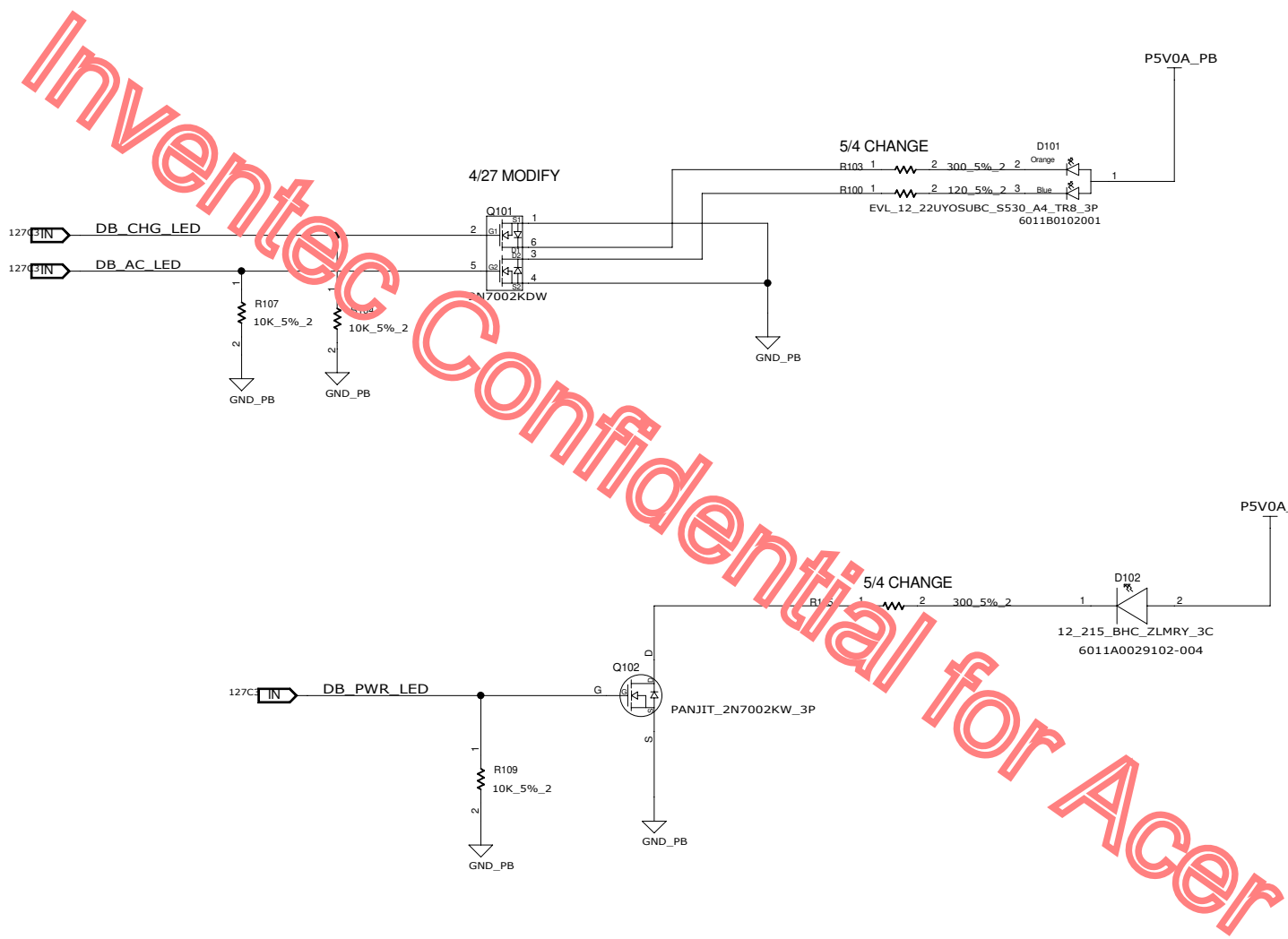
DATE 21-OCT-2002
PCB VER XXX

SHEET 121 of 139

8	7	6	5	4	3	2	1
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



INVENTEC				
TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 123 of 139

A



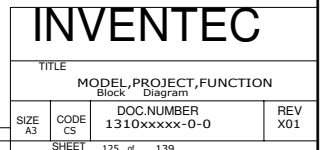
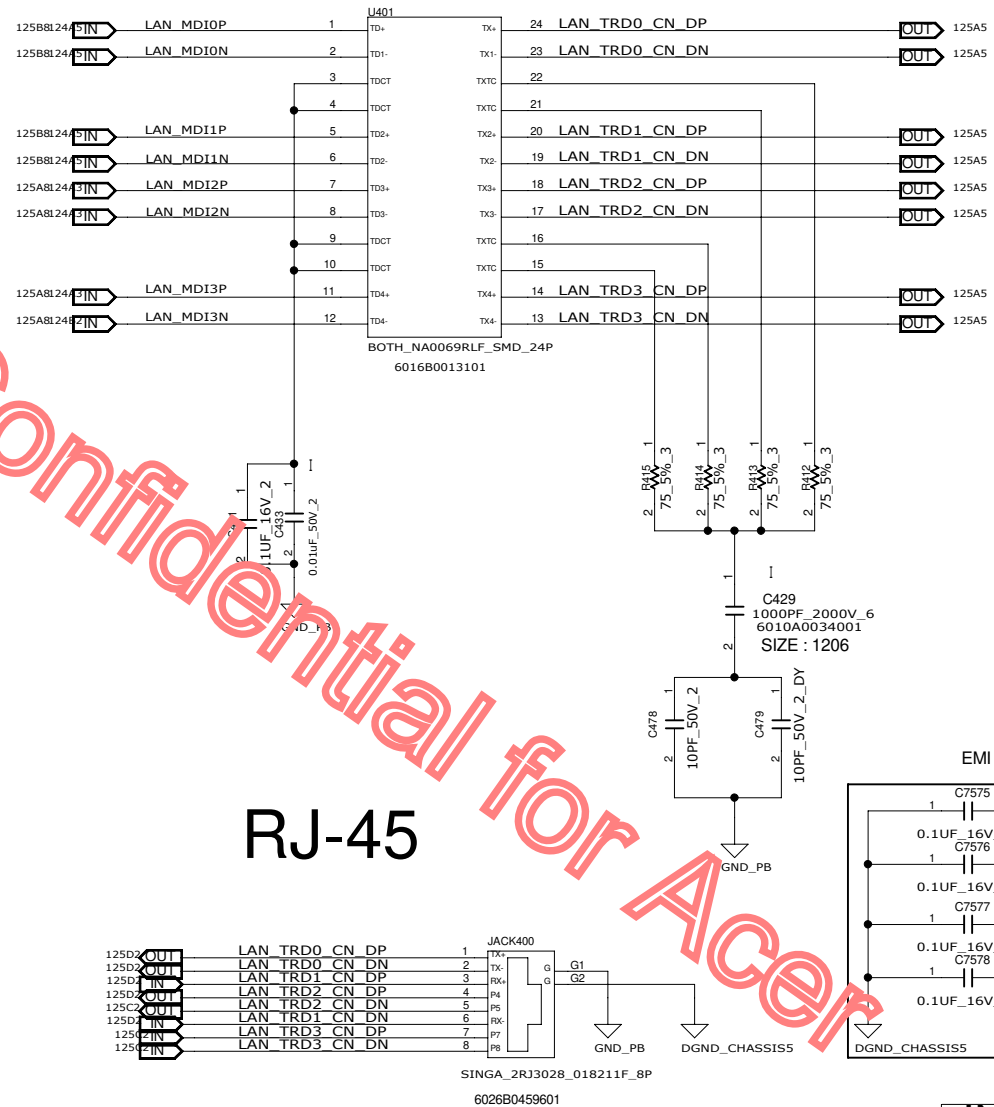
	1
--	---

2

	1
--	---

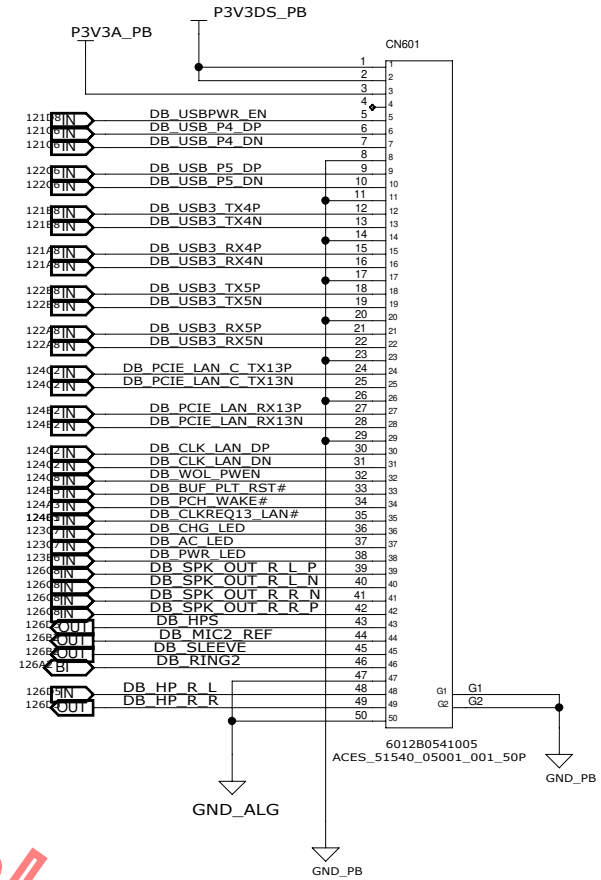
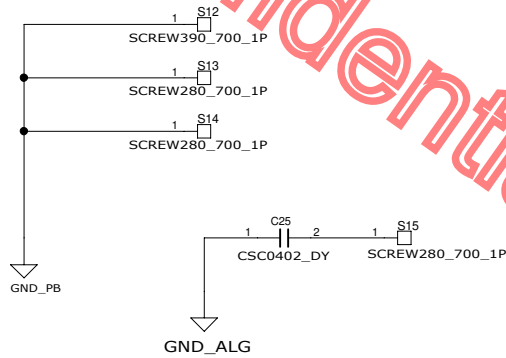
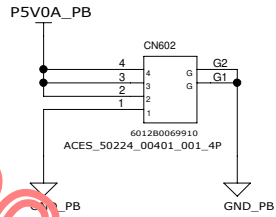
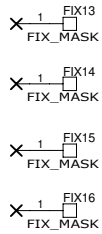
ESD

RJ-45



CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 125 of 139			

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INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 127 of 139

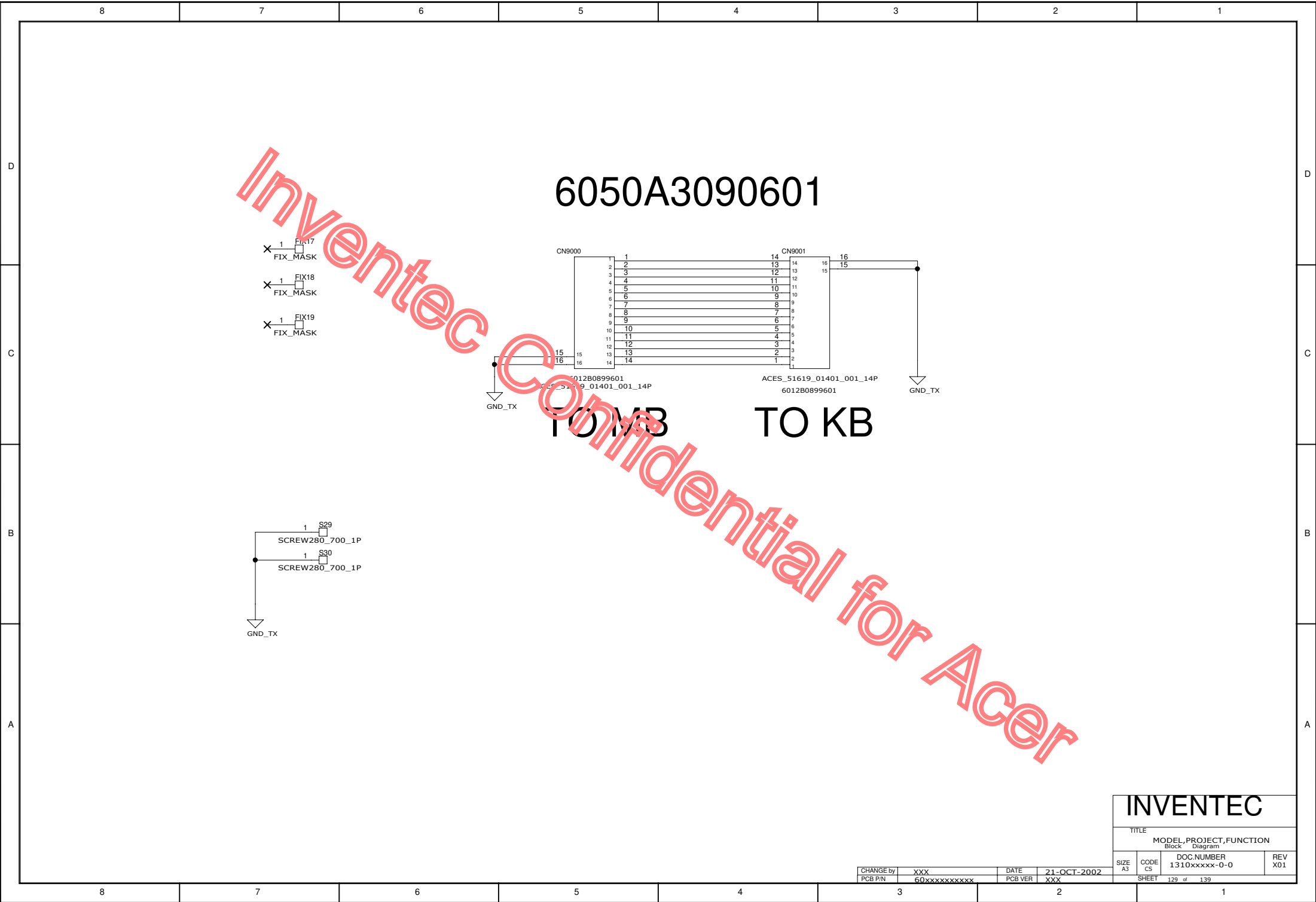
8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

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FOR 17 SMALL BOARD

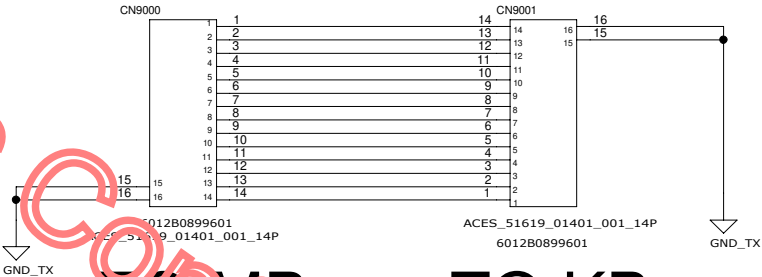
INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 128 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



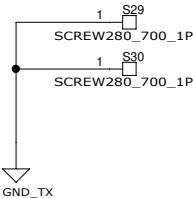
6050A3090601

X 1 FIX17
FIX_MASK
X 1 FIX18
FIX_MASK
X 1 FIX19
FIX_MASK



TO MB

TO KB



INVENTEC

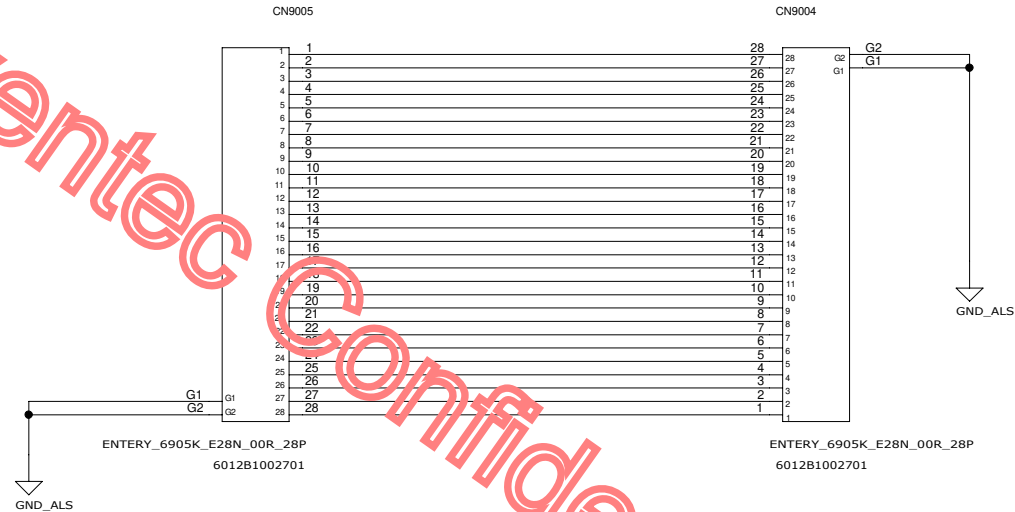
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE CODE
A3 CS
DOC NUMBER
1310xxxxx-0-0
REV
X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

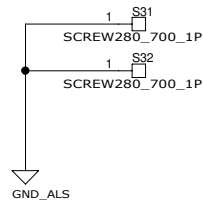
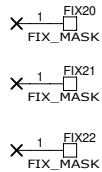
SHEET 129 of 139

6050A3090501



TO MB

TO KB



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE CODE
A3 CS
DOC NUMBER
1310xxxxx-0-0
REV
X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

SHEET 130 of 139

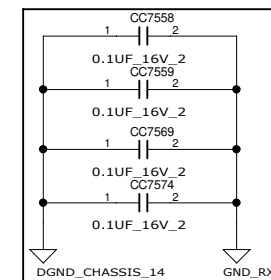
8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

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FOR '15 AUDIO BOARD

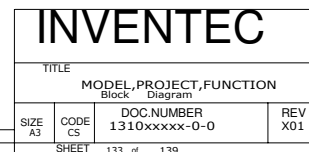
INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 131 of 139			

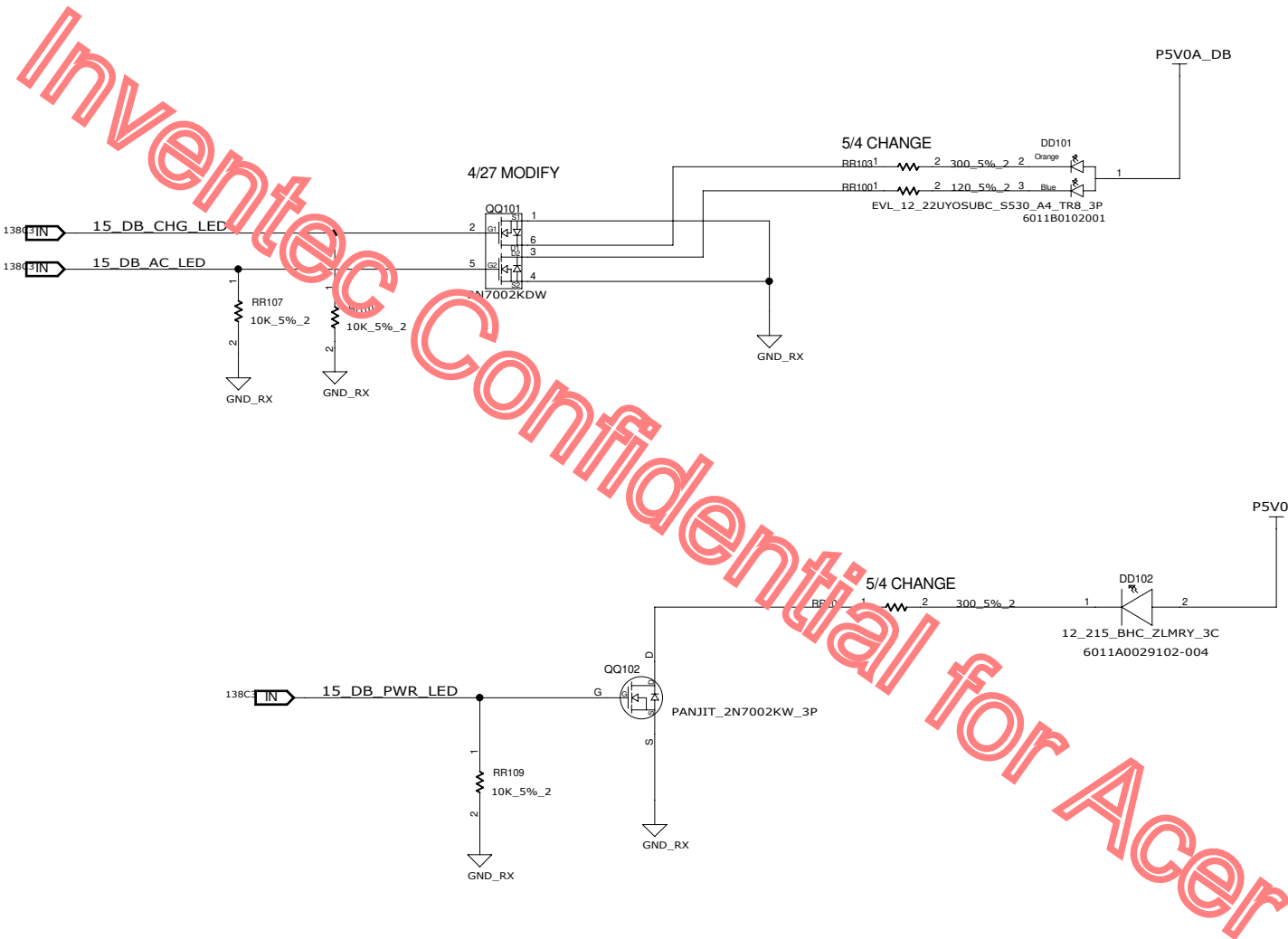
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



GND_RX 

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 132 of 130			



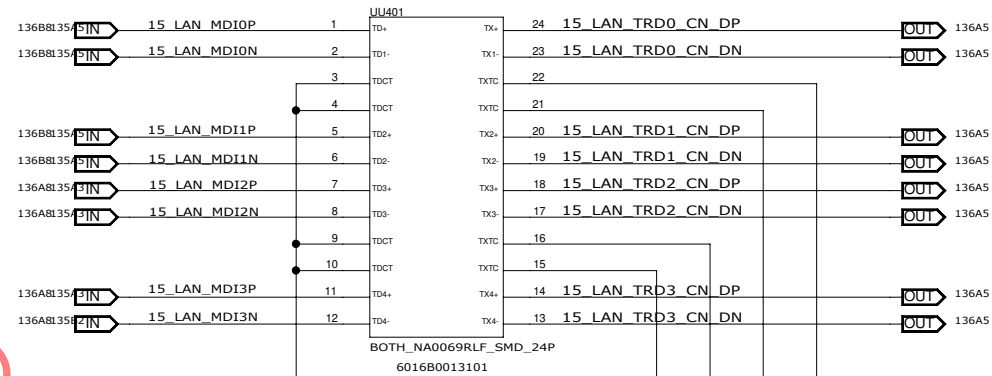


INVENTEC				
TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 134 of 139

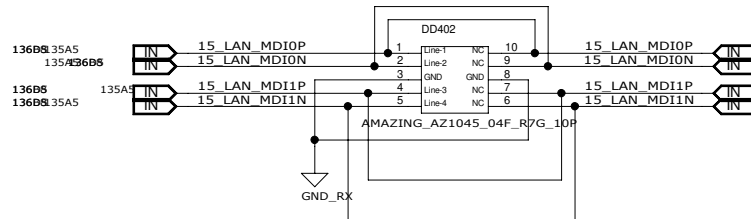


CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		SHEET	135 of 139	

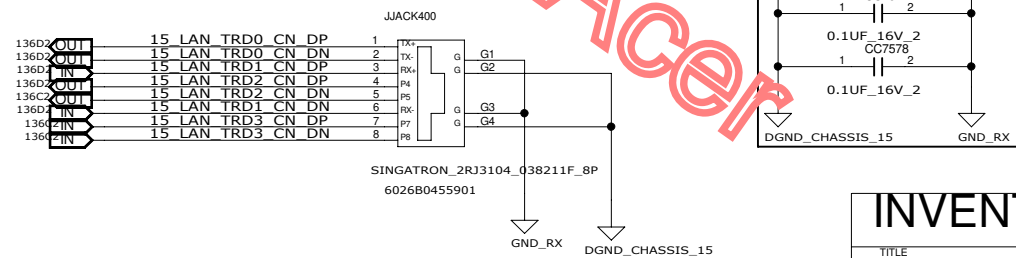
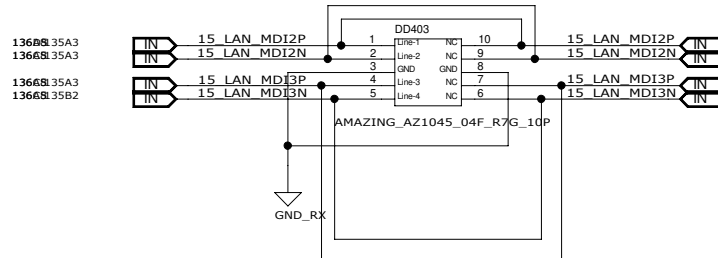
TRANSFORMER



ESD



RJ-45



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

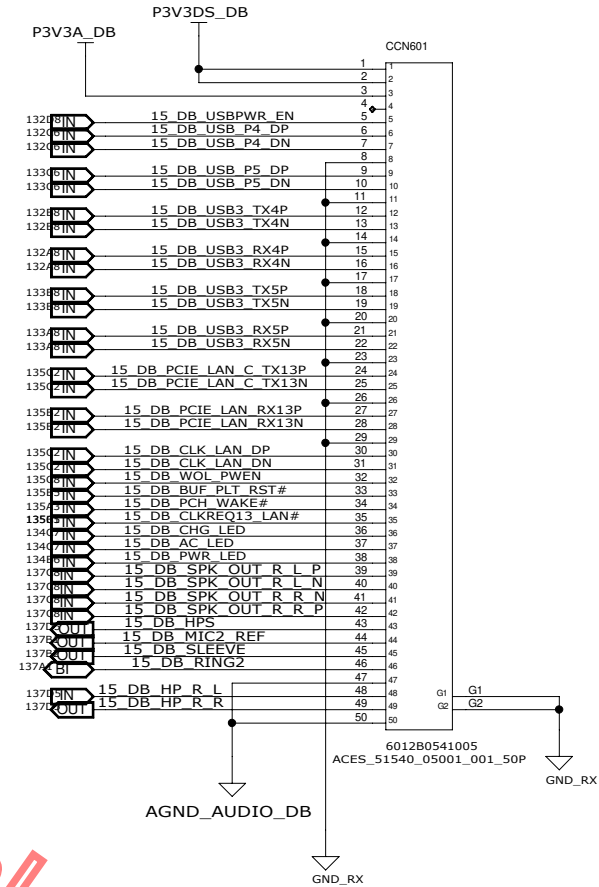
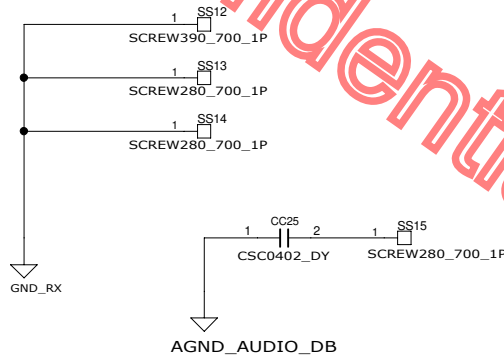
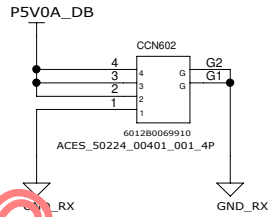
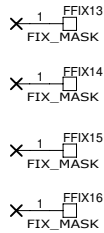
SIZE A3 CODE CS
DOC NUMBER 1310xxxxx-0-0
REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

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INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 138 of 139

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

Inventec Confidential for Acer

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 139 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX