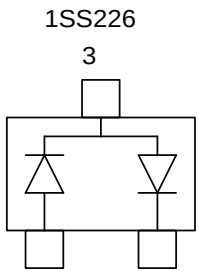
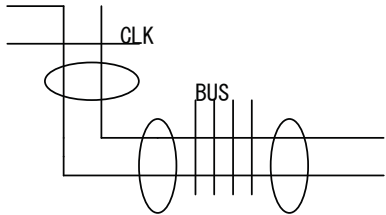
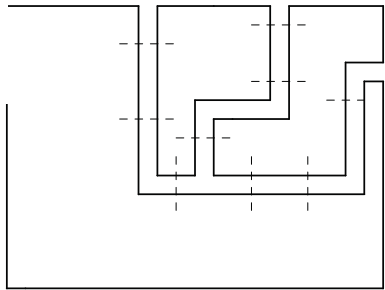
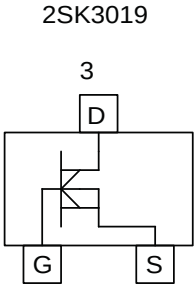


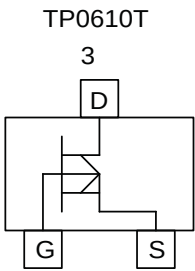
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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
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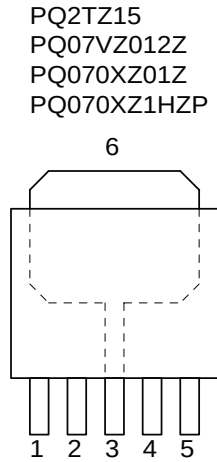
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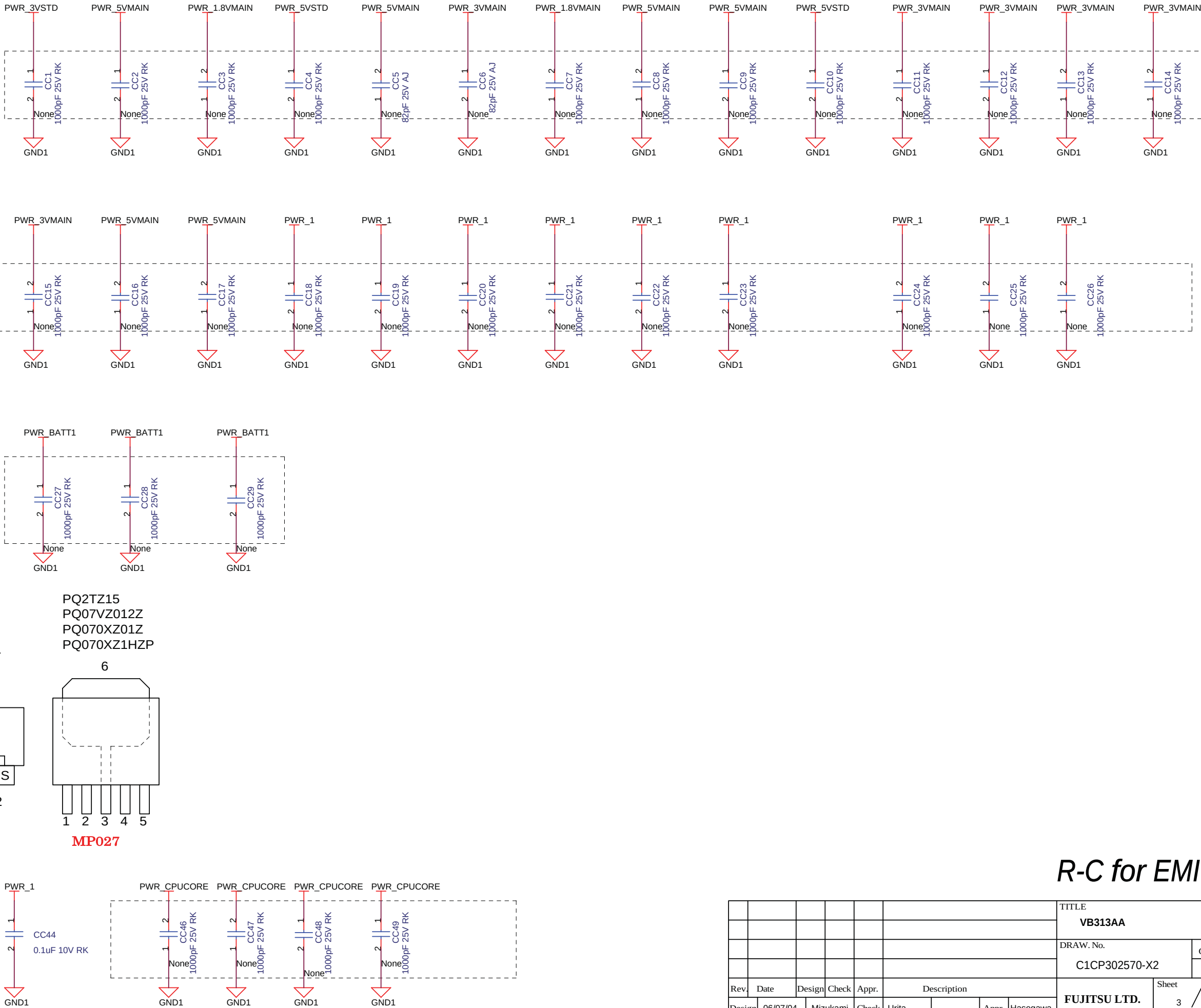
MP010



MP009



MP027

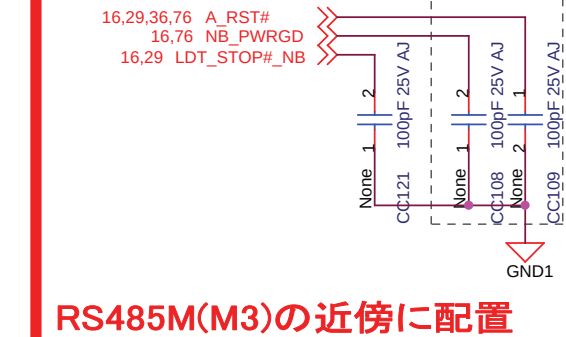
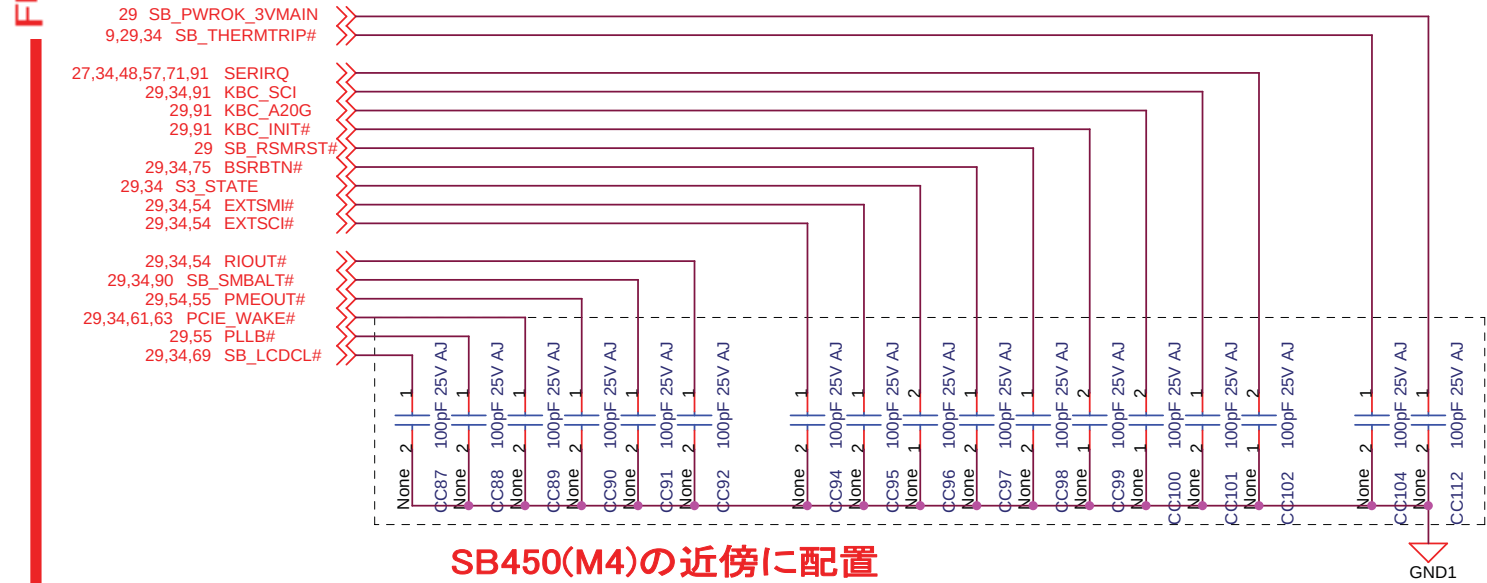


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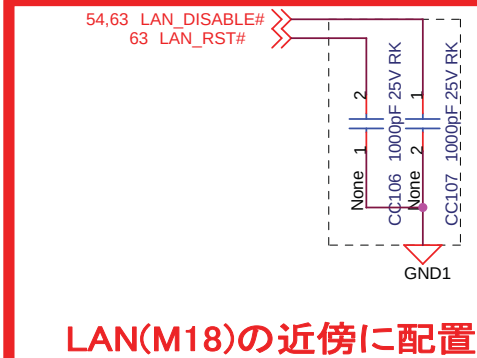
R-C for EMI

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Design	06/07/04	Mizukami	Check	Urita		3	/	93
						Fujitsu Ltd.		

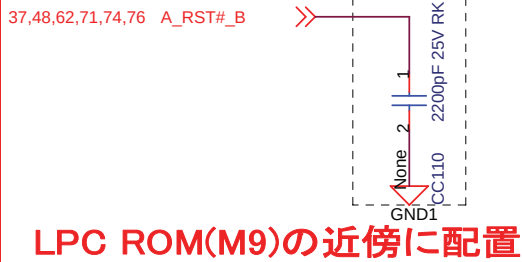
CPU(CN1)の近傍に配置



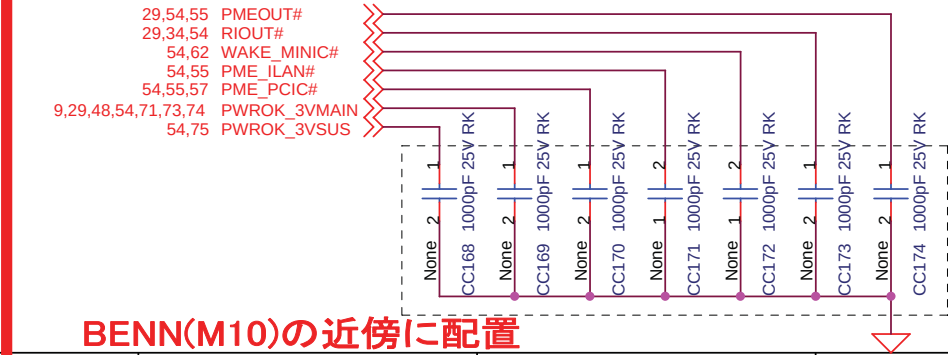
RS485M(M3)の近傍に配置



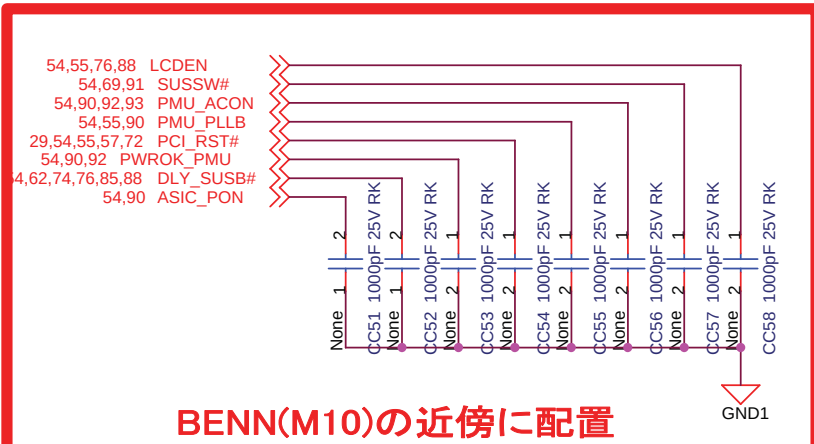
LAN(M18)の近傍に配置



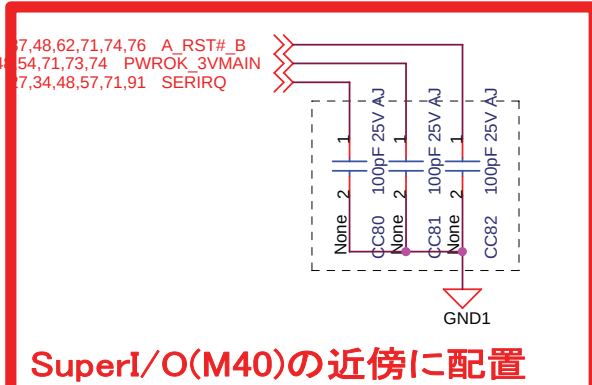
LPC ROM(M9)の近傍に配置



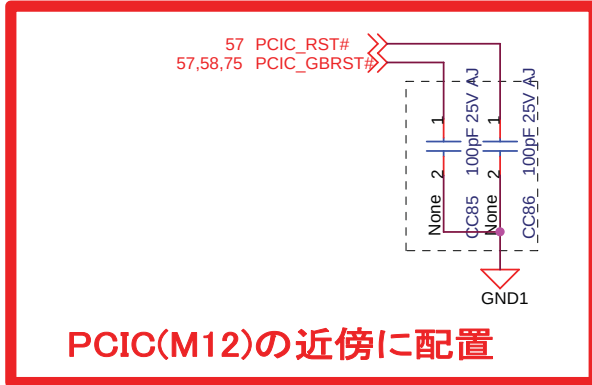
BENN(M10)の近傍に配置



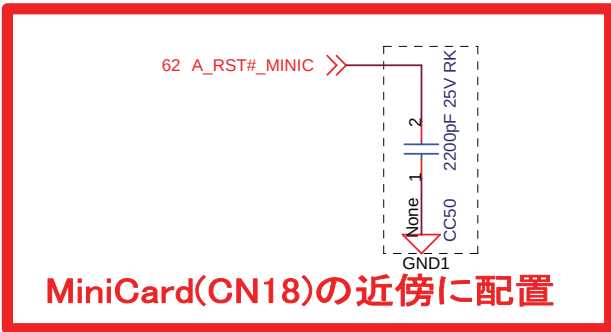
BENN(M10)の近傍に配置



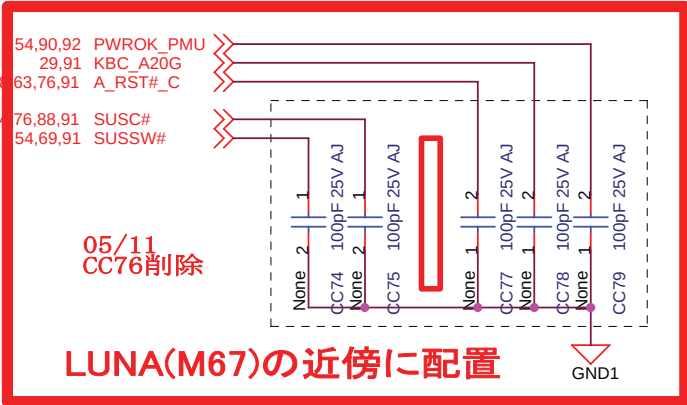
SuperI/O(M40)の近傍に配置



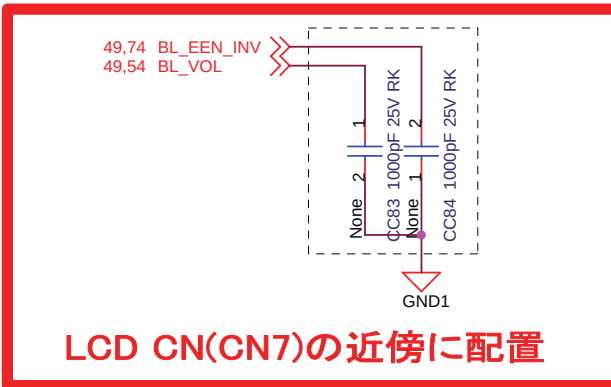
PCIC(M12)の近傍に配置



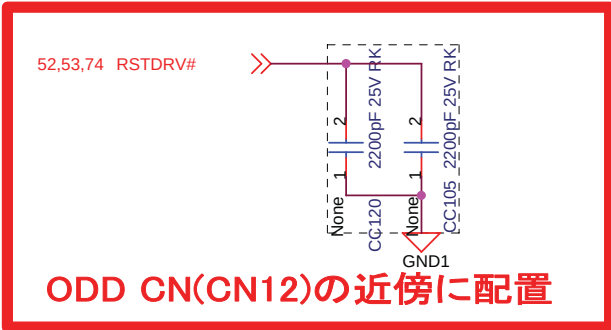
MiniCard(CN18)の近傍に配置



LUNA(M67)の近傍に配置



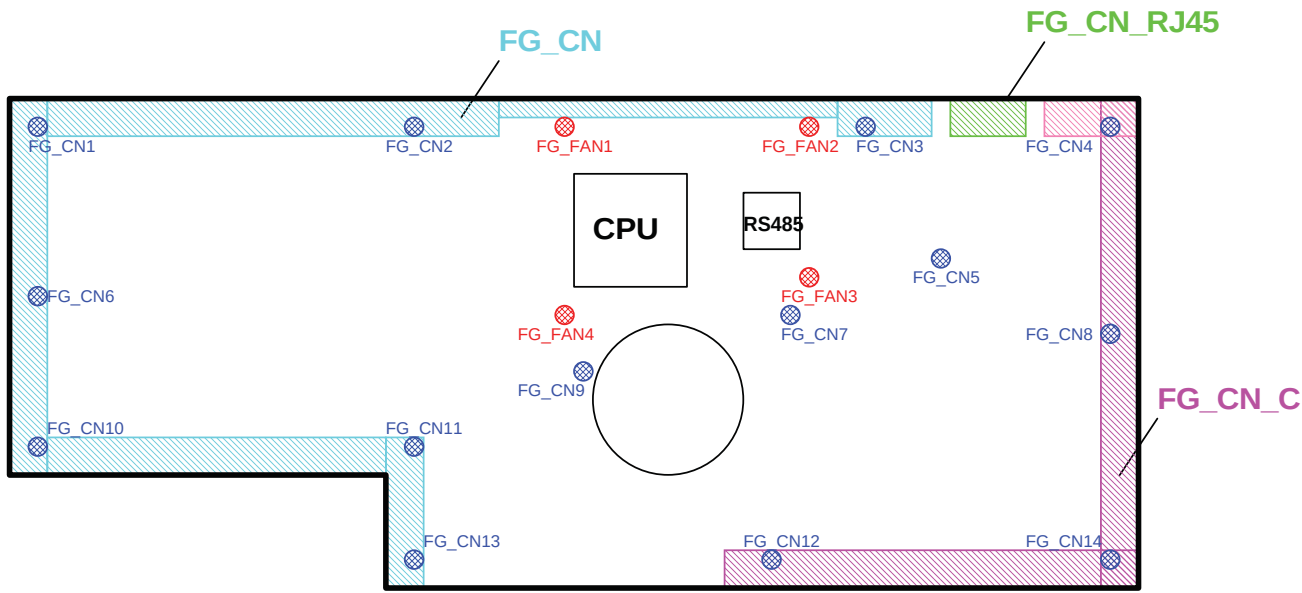
LCD CN(CN7)の近傍に配置



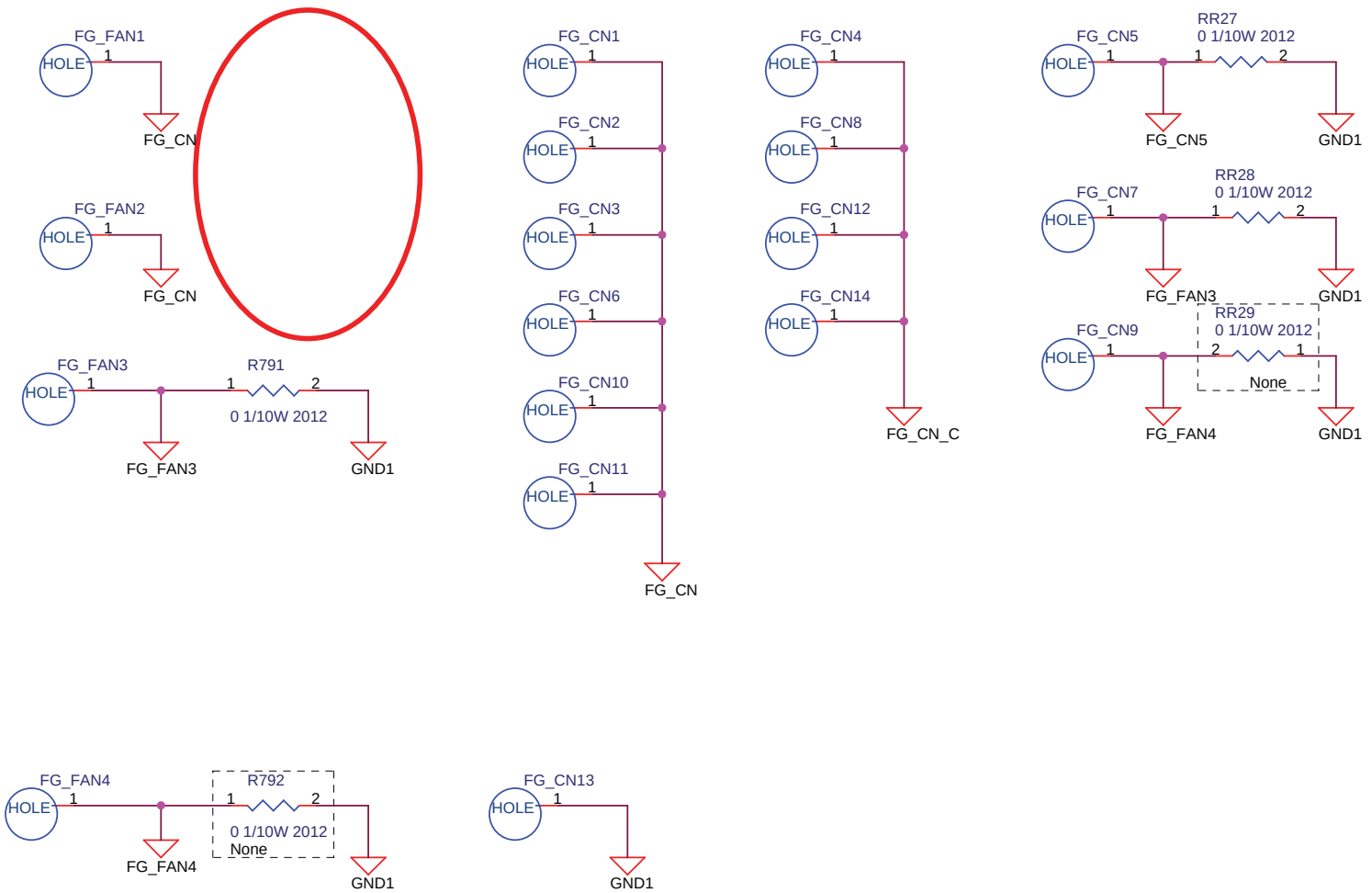
ODD CN(CN12)の近傍に配置

R-C for ESD

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						Appr. Hasegawa		



2006.7.4
02版: R721, R1

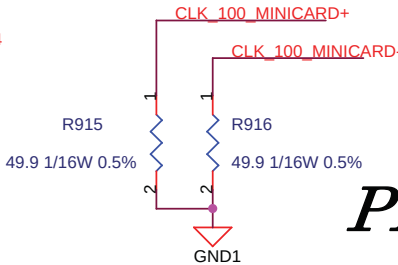
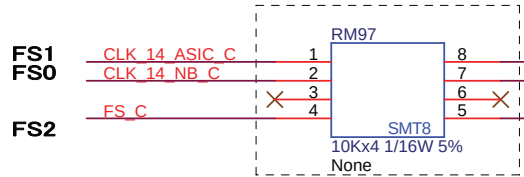


FG-CN

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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	5 / 93

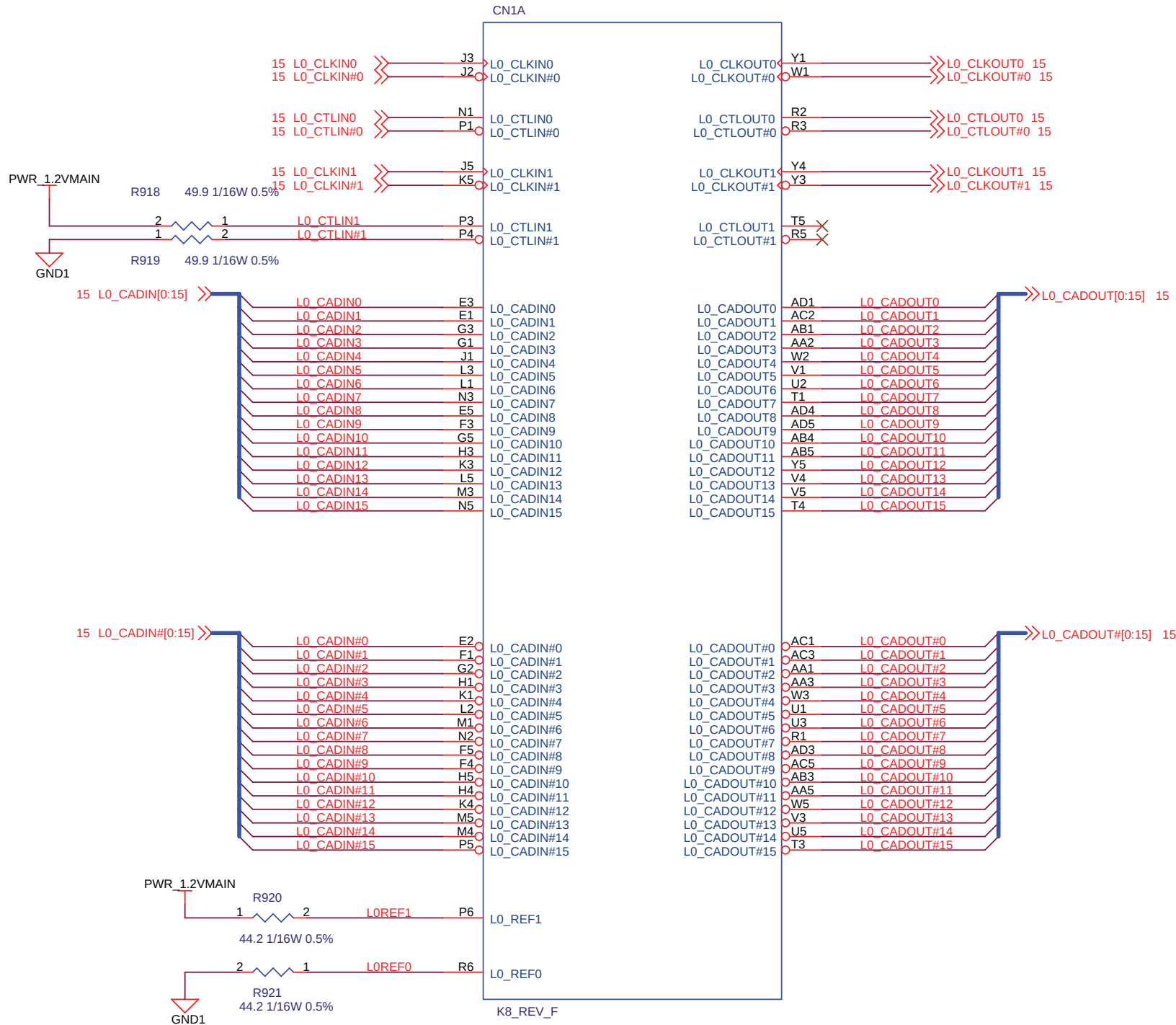
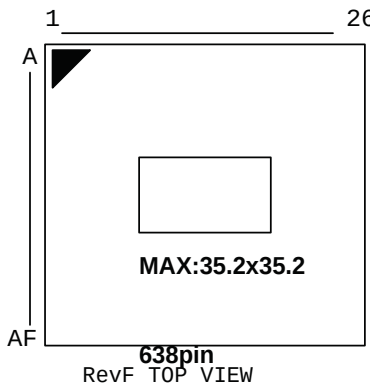
FS2	FS1	FS0	CPU(MHz)	HTT(MHz)	PCI(MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	36.56	73.12
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

CV137 does not have strap option



									TITLE	
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									DRAW. No.	CAST
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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	6 / 93		

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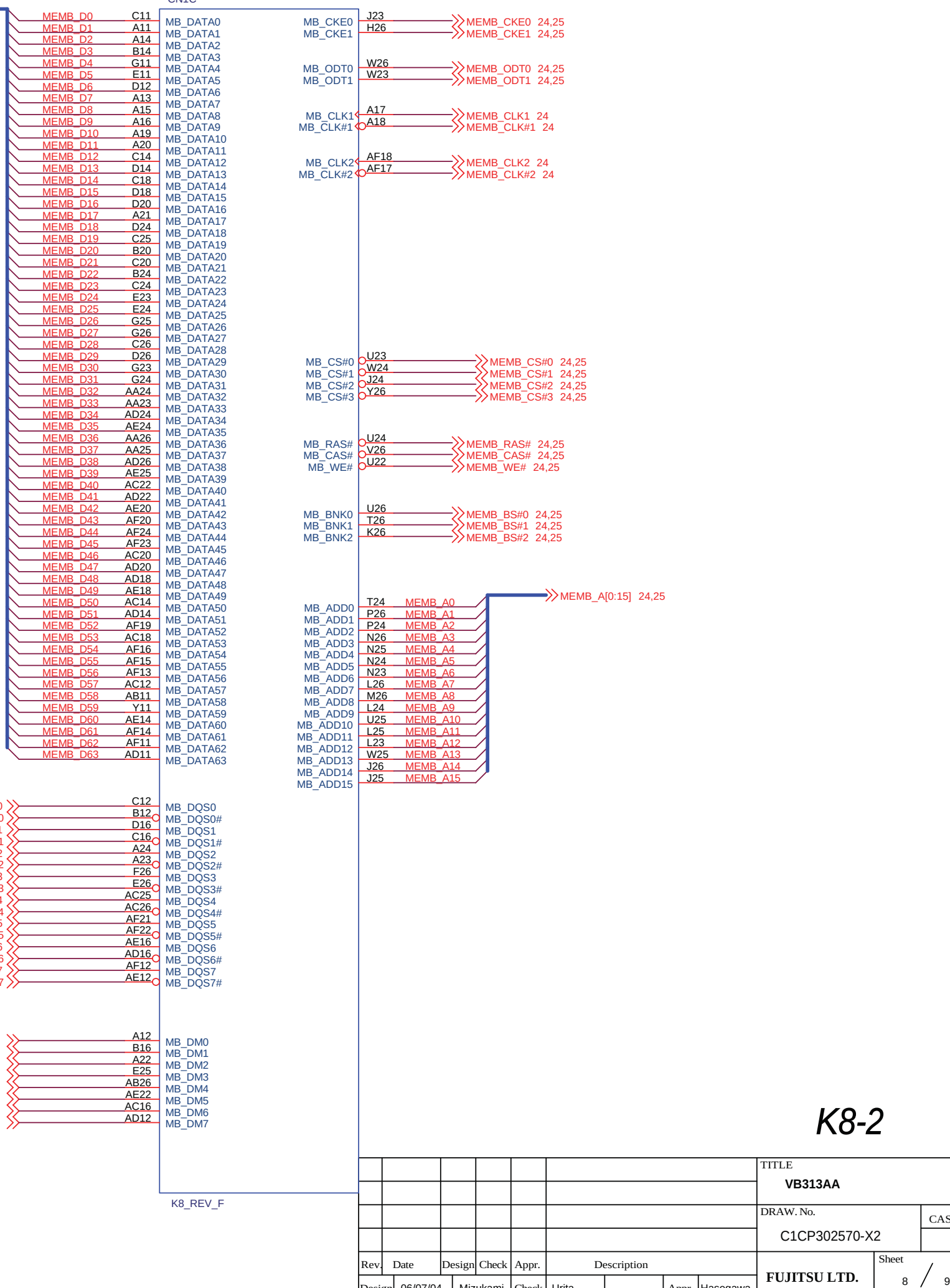
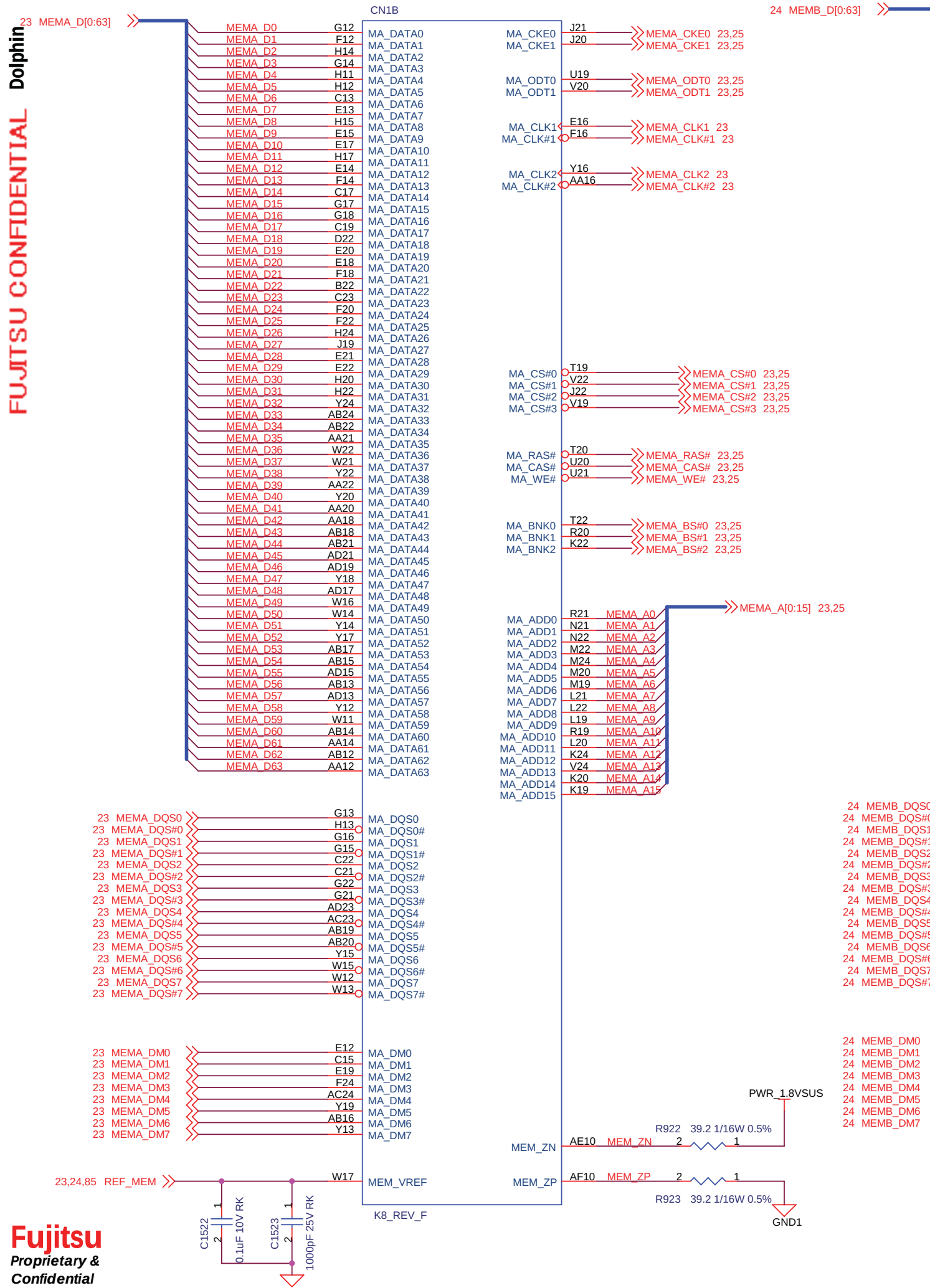


K8-1

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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	7 / 93

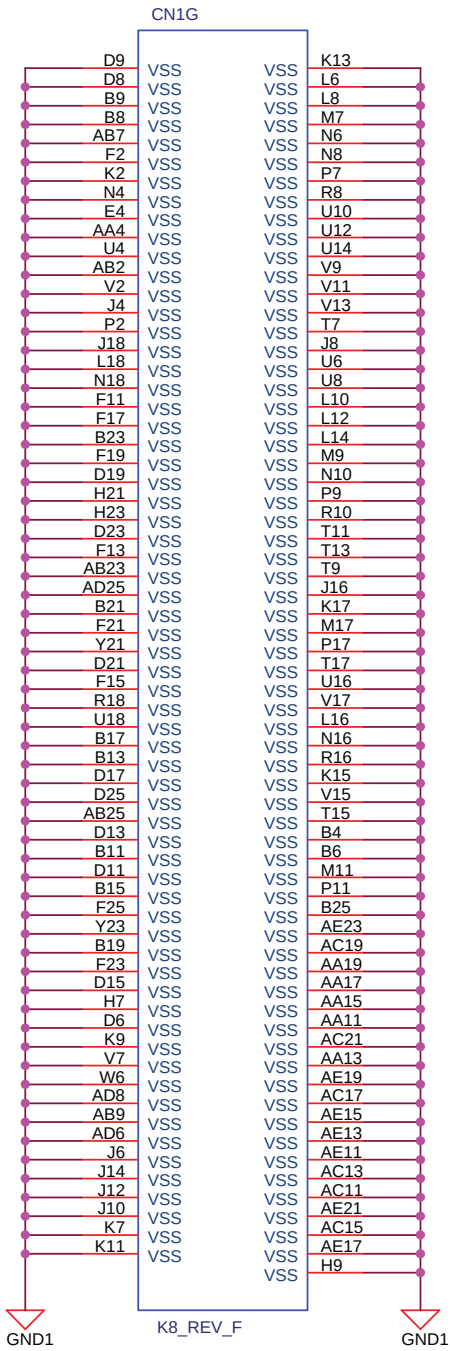
Dolphin
FUJITSU CONFIDENTIAL



K8-2

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					Appr.	Hasegawa	FUJITSU LTD.	

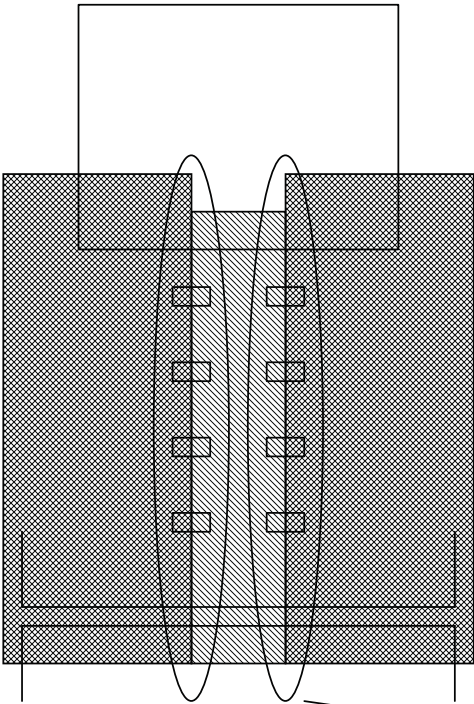
FUJITSU CONFIDENTIAL Dolphin



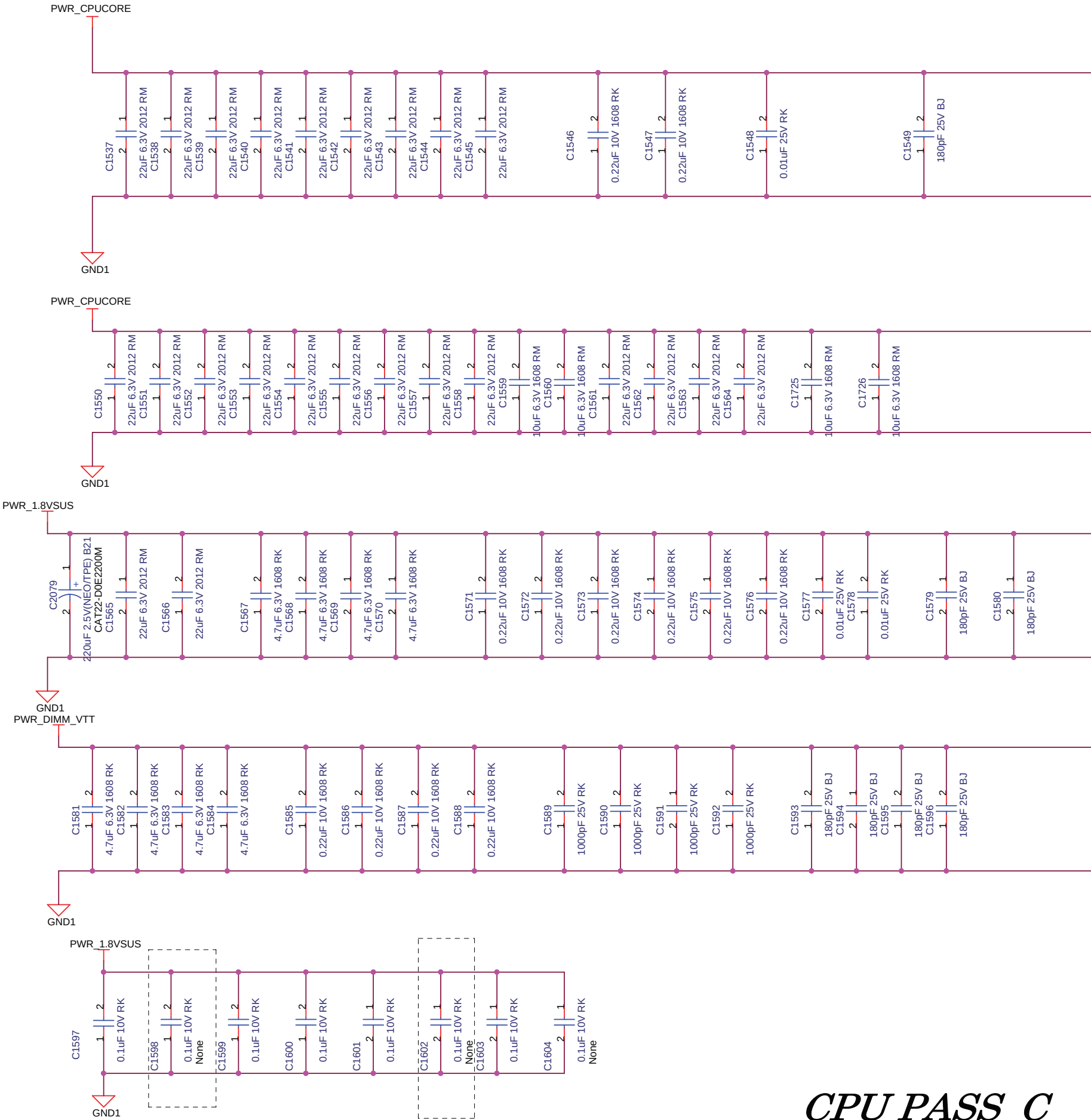
K8-5

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Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 11 / 93



これらのコンデンサC1597～C1604は、図のように
PWR_1.8VSUS, GND1のプレーンの間に
約1インチ間隔で配置すること。

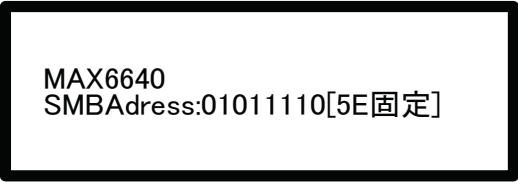


K8_CPU

CPU PASS_C

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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
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G		Fujitsu Proprietary & Confidential														G	

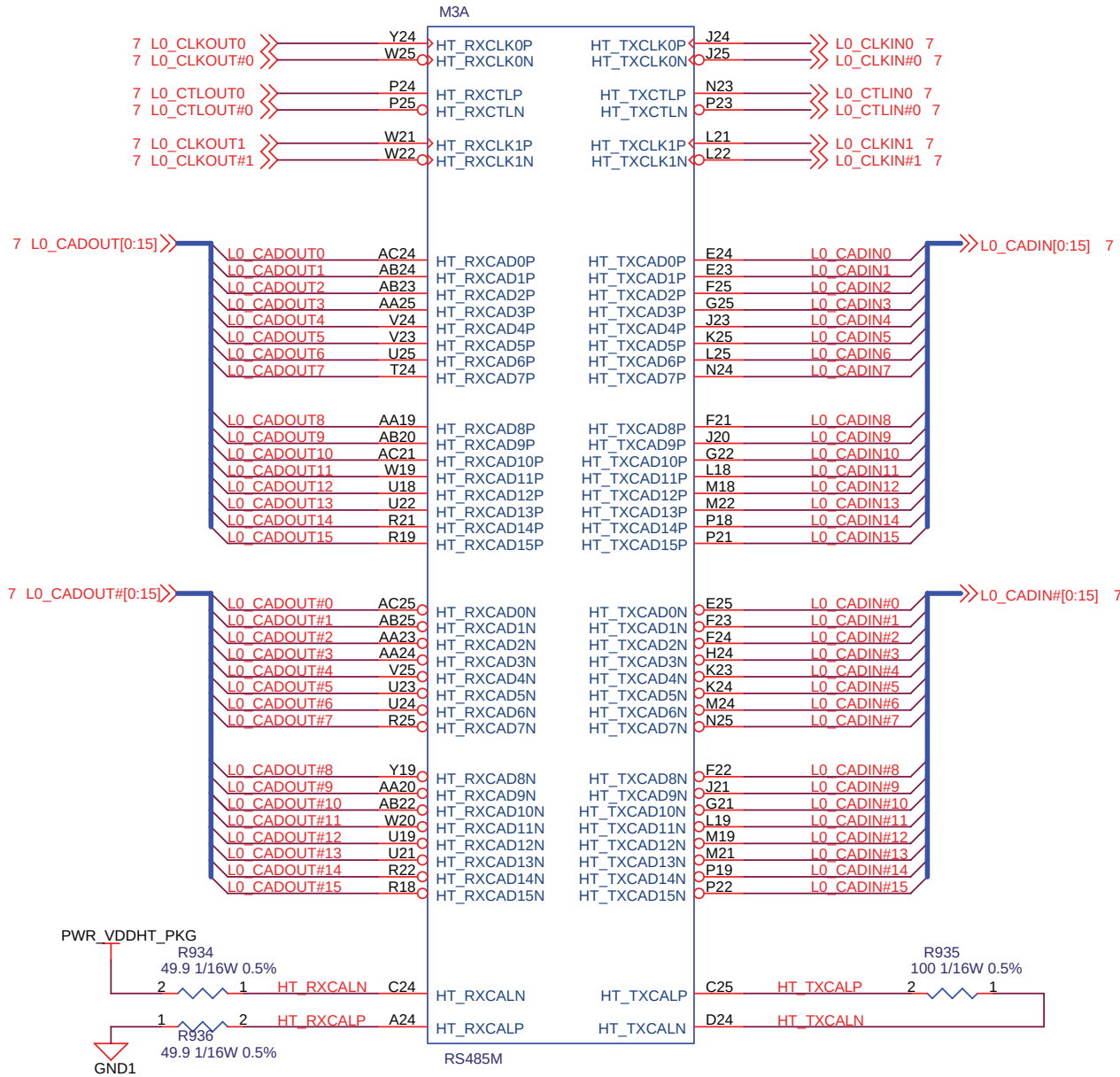
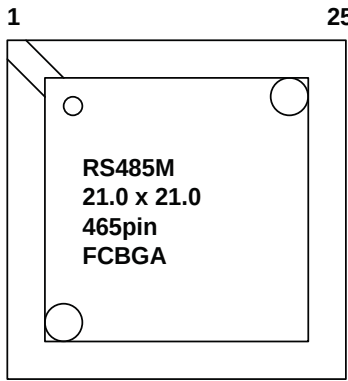


04/24 NET名修正：
TEMP_TACH_CPU -> TEMP_TACH

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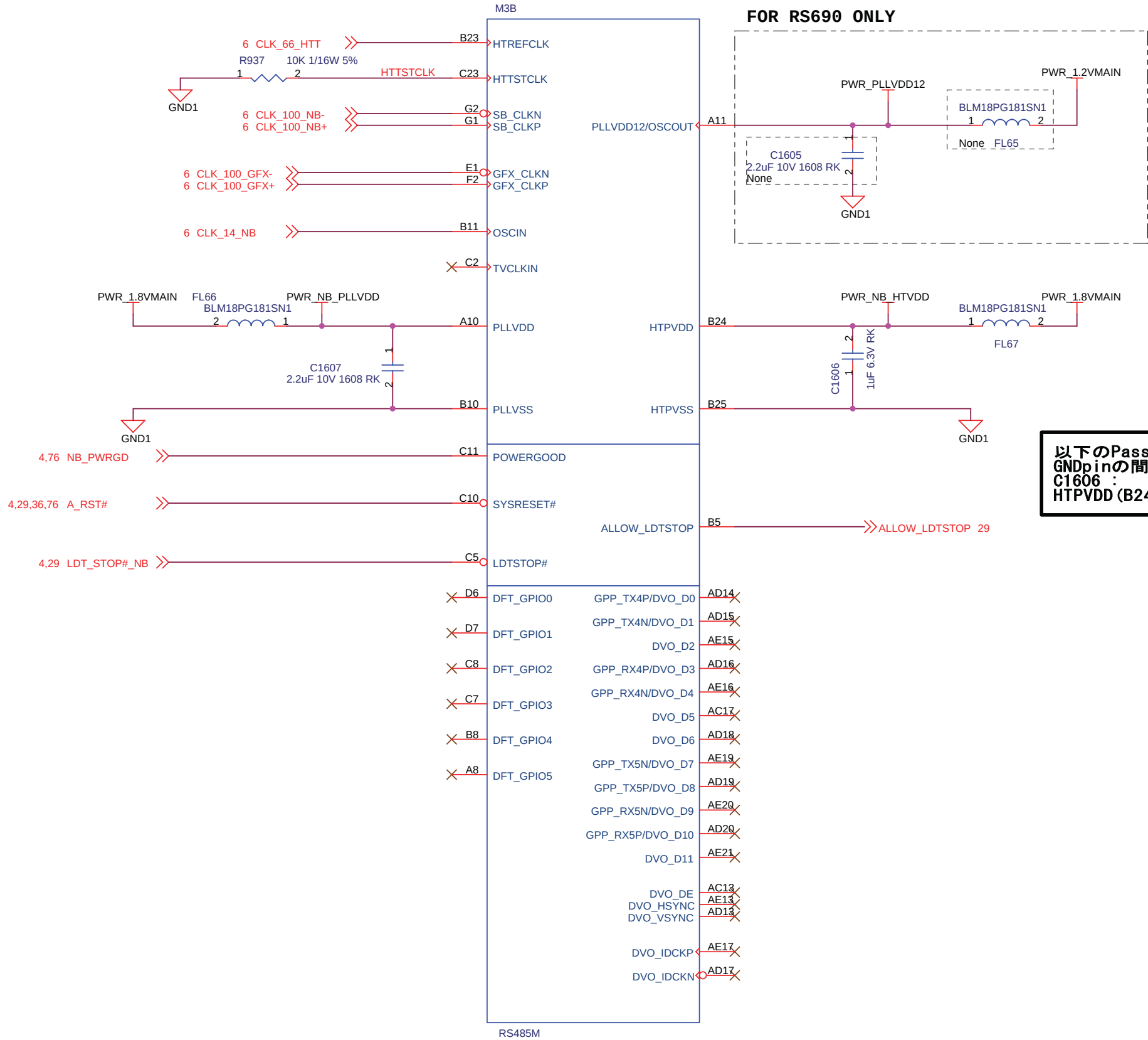
Dolphin



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RS485-1

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以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1606 :
HTPVDD (B24pin) とHTPVSS (B25pin) の間

RS485-2

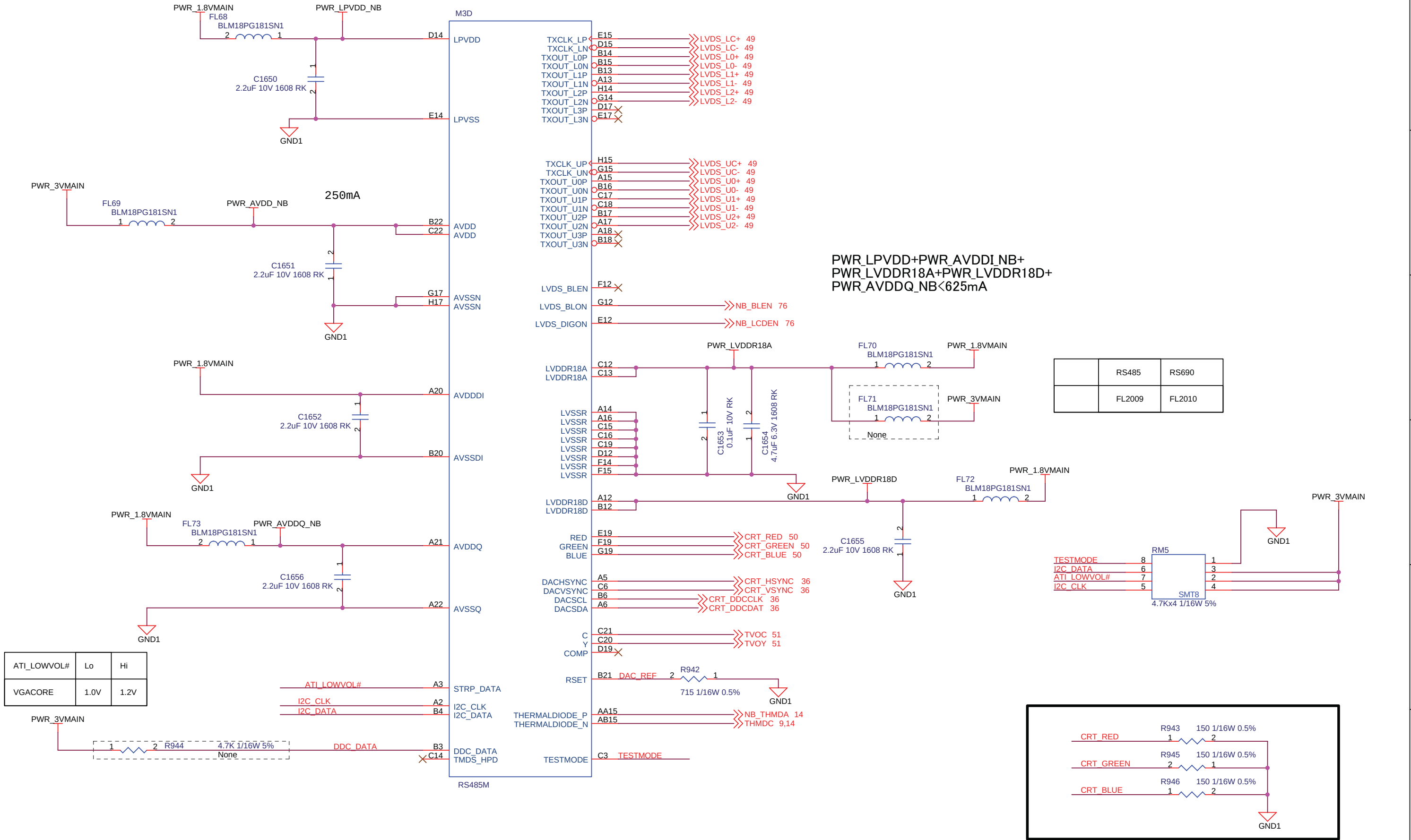
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita				16 / 93



	RS485	RS690
R939	8.2Kohm 0.5%	None
R941	10Kohm 5%	1.47Kohm 5%

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						VB313AA			
						DRAW. No.		CAST	
						C1CP302570-X2			
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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		

RS485-3



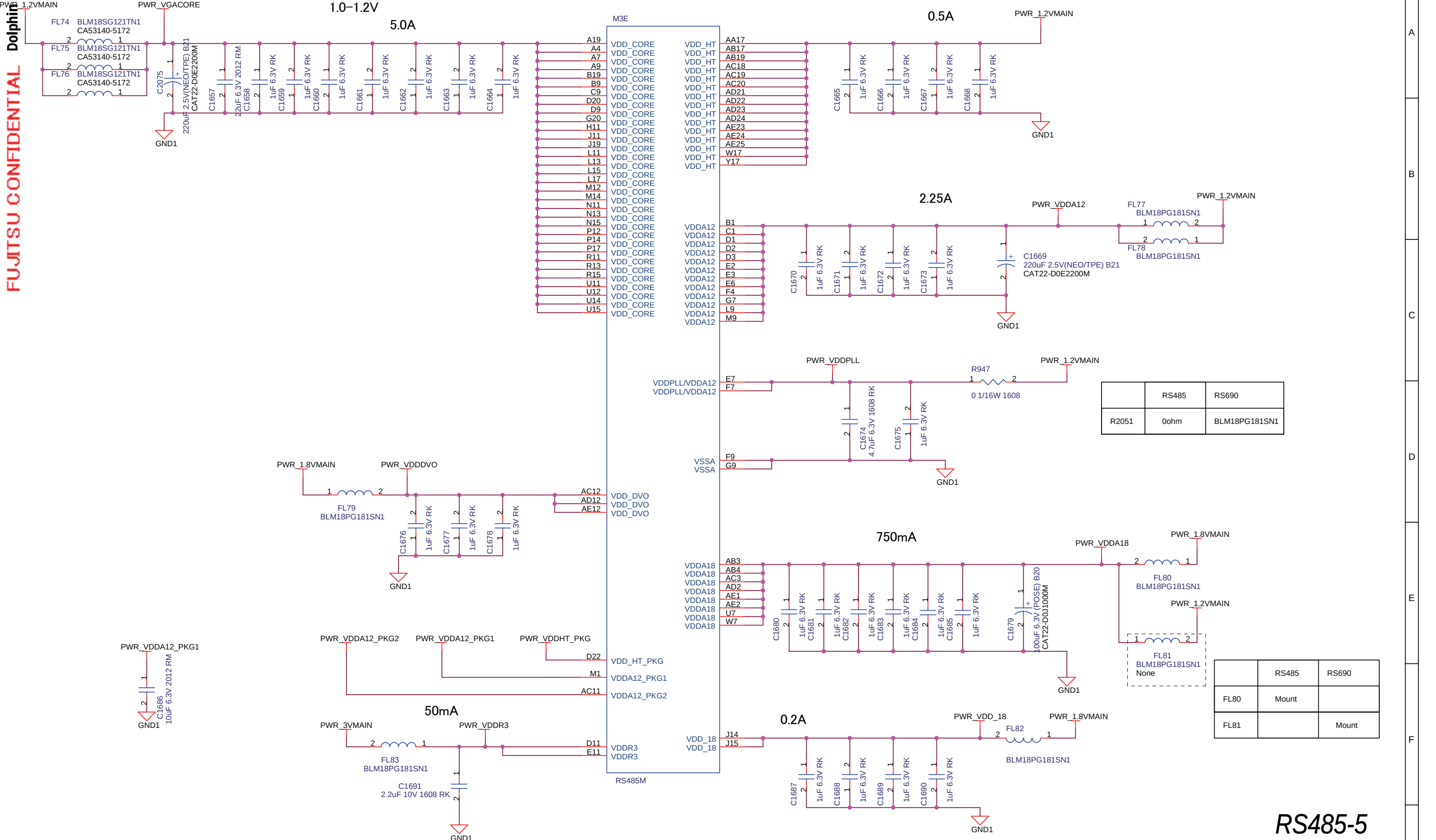
以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
LPVSS(E14pin)
LVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)
AVSSN(G17,H17pin)
AVSSDI(B20pin)
AVSSQ(A22pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1650 : LPVDD(D14pin)とLPVSS(E14pin)の間
C1653, C1654 : LVDDR18A(C12,C13pin)とLVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)の間
C1651 : AVDD(B22,C22pin)とAVSSN(G17,H17pin)の間
C1652 : AVDDI(A20pin)とAVSSDI(B20pin)の間
C1656 : AVDDQ(A21pin)とAVSSQ(A22pin)の間

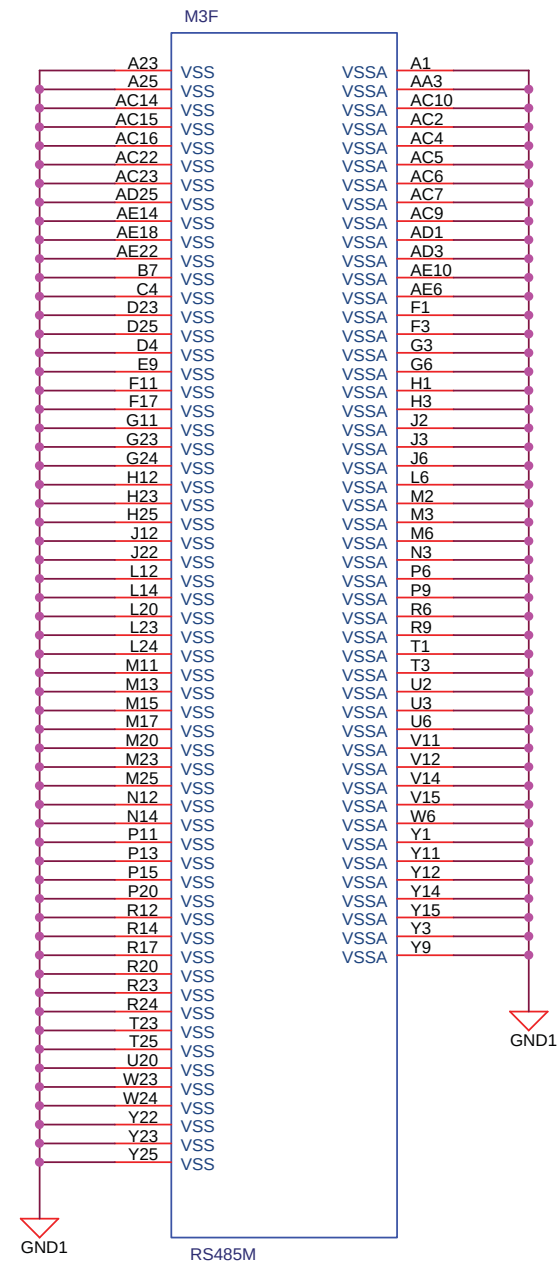
R943,R945,R946は、M3(RS485M)の直近に配置すること

RS485-4

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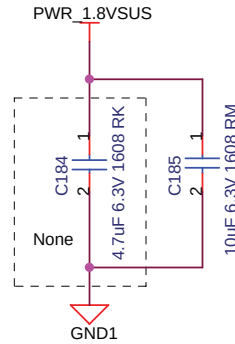
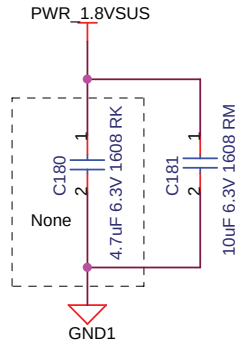
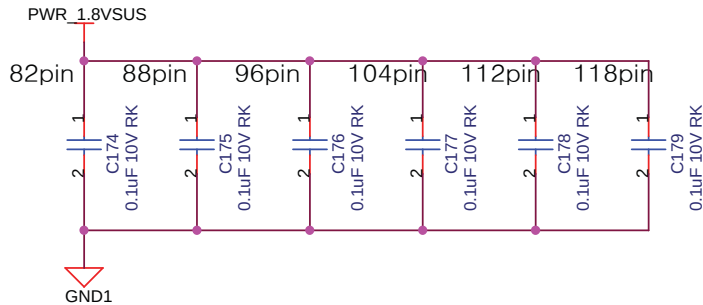
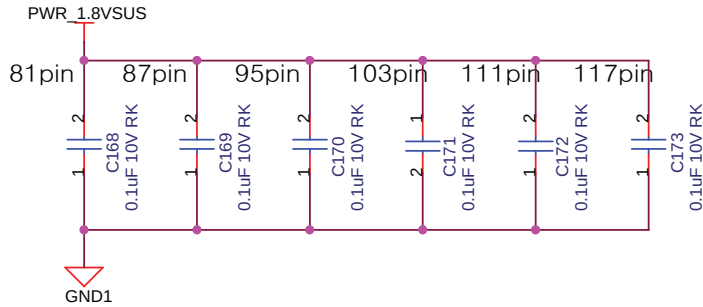
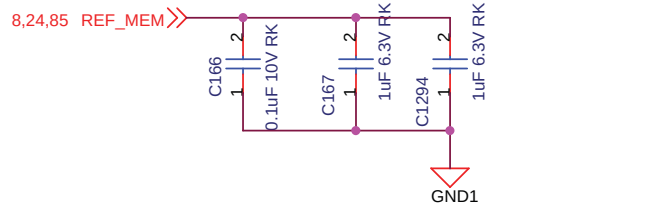
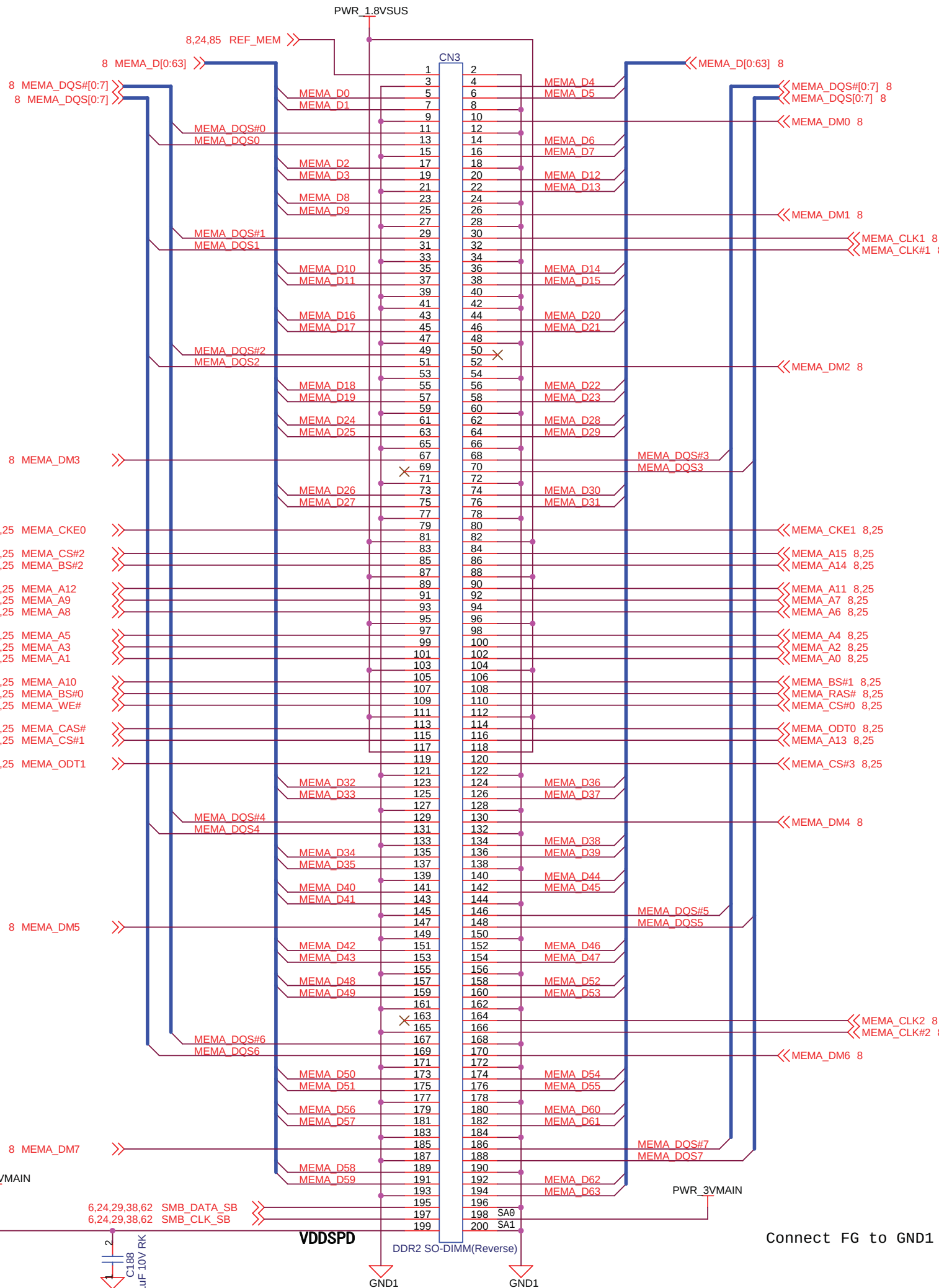
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RS485-6

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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		20 / 93

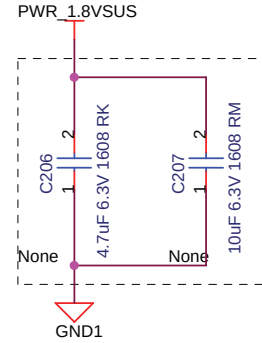
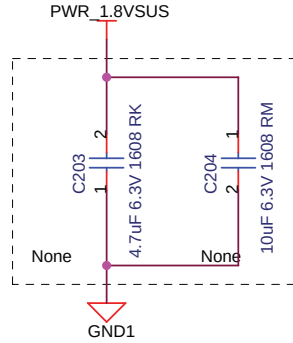
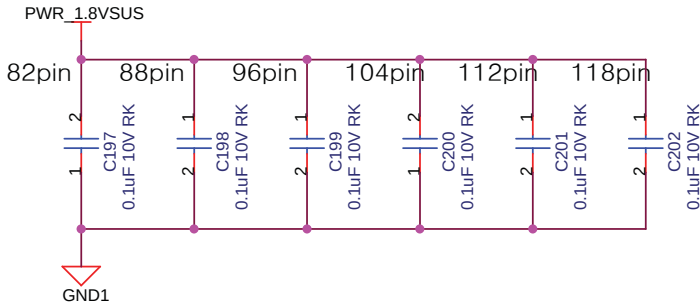
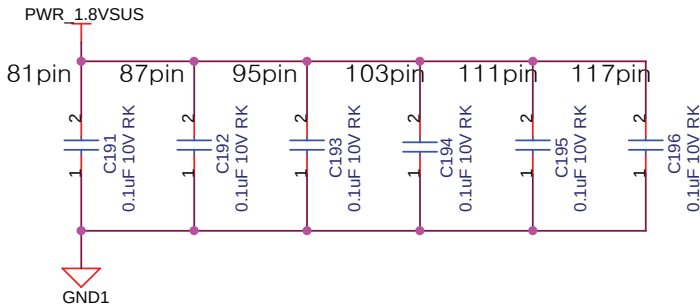
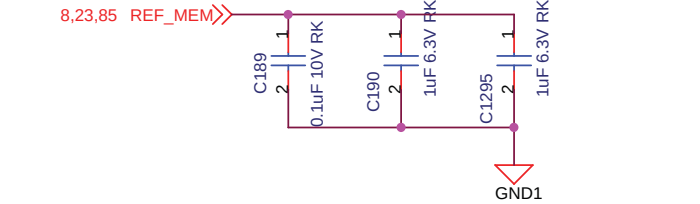
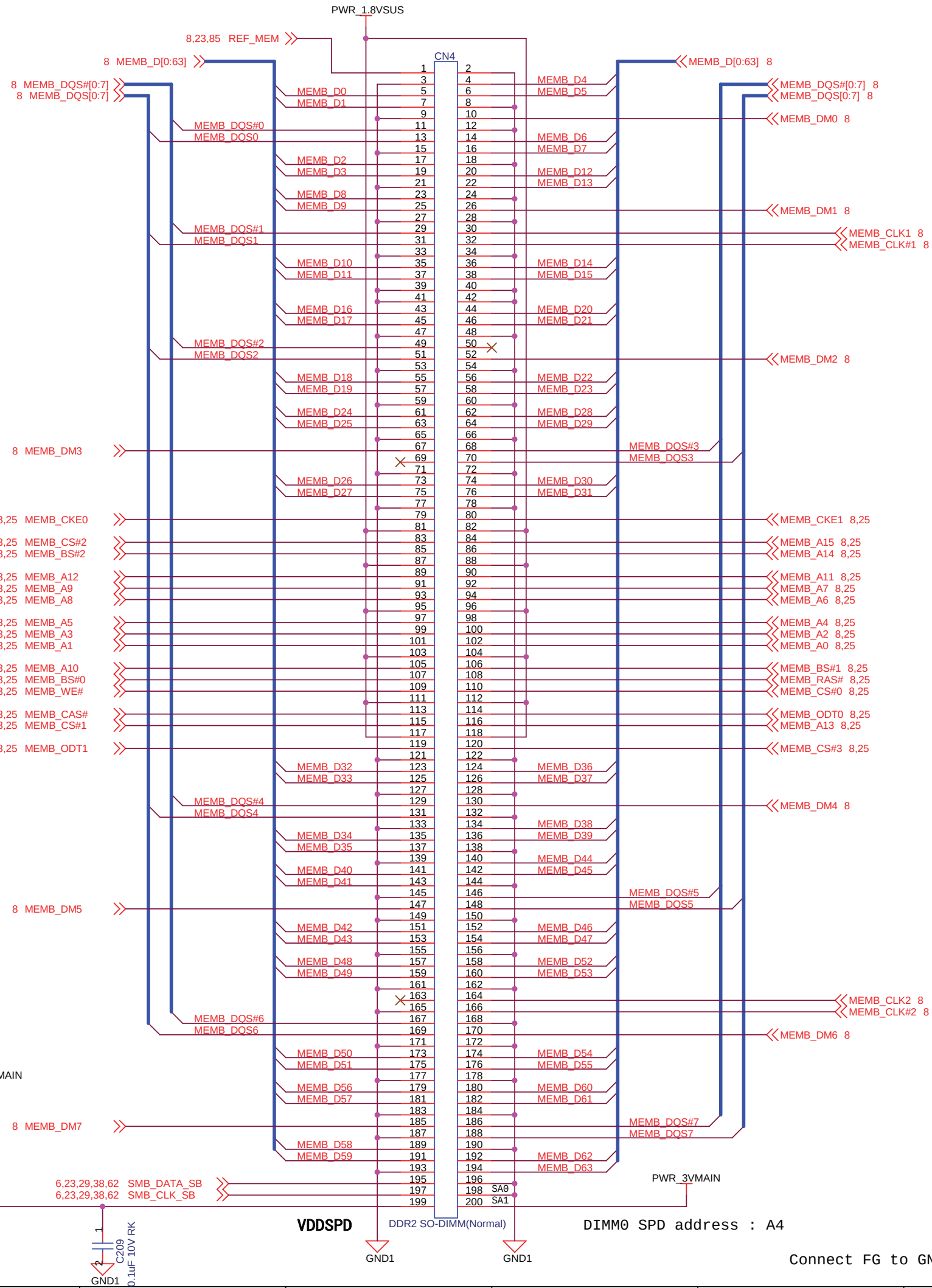
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Fujitsu Proprietary & Confidential <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">TITLE</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">VB313AA</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">DRAW. No.</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">C1CP302570-X2</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2"></td></tr><tr><td>Rev.</td><td>Date</td><td>Design</td><td>Check</td><td>Appr.</td><td colspan="3">Description</td><td></td></tr><tr><td>Design</td><td>06/07/04</td><td>Mizukami</td><td>Check</td><td>Urita</td><td></td><td>Appr.</td><td>Hasegawa</td><td></td></tr></table>																							TITLE								VB313AA								DRAW. No.								C1CP302570-X2										Rev.	Date	Design	Check	Appr.	Description				Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		22 / 93
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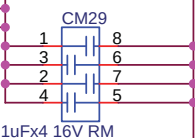
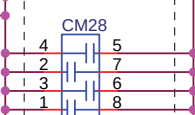
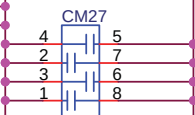
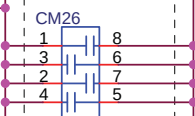
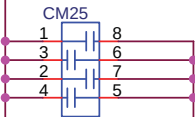
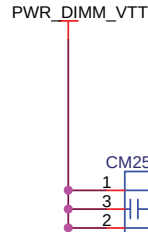
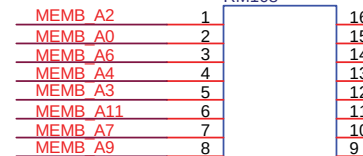
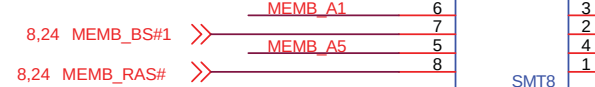
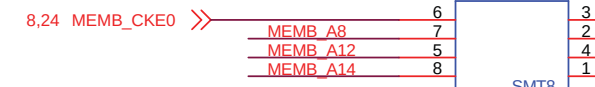
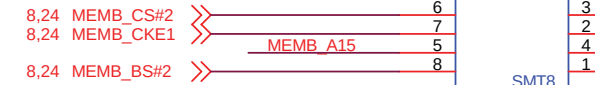
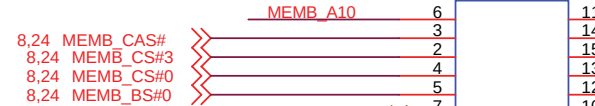
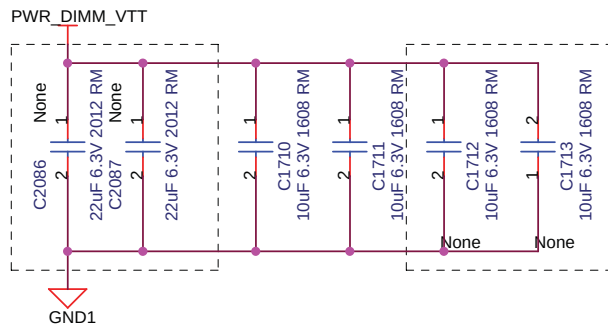
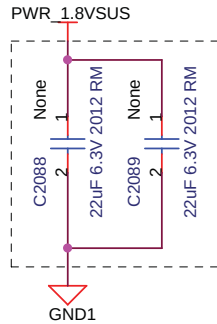
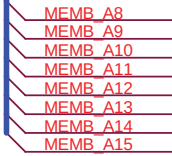
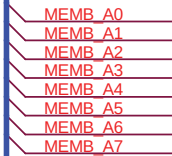
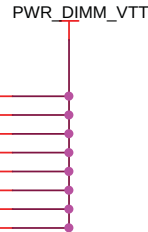
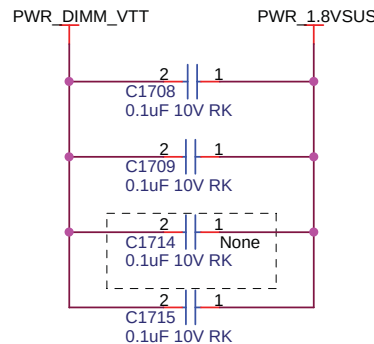
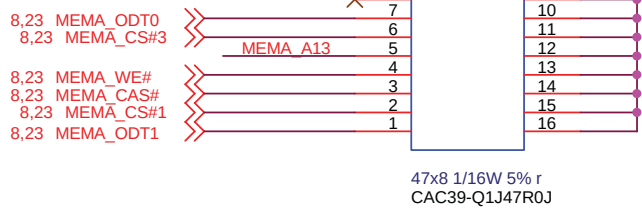
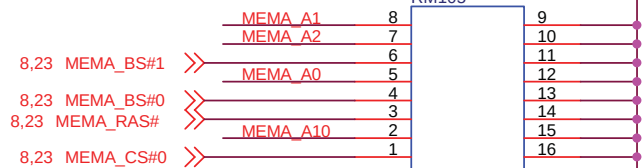
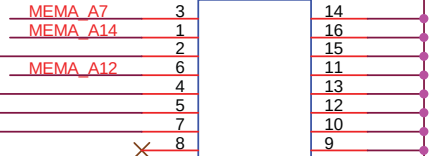
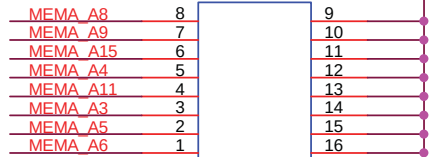
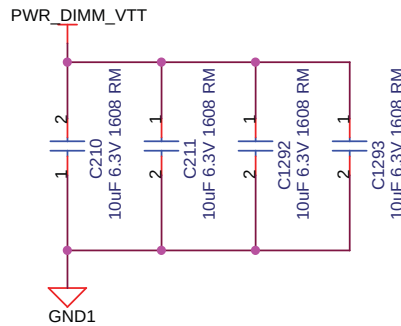
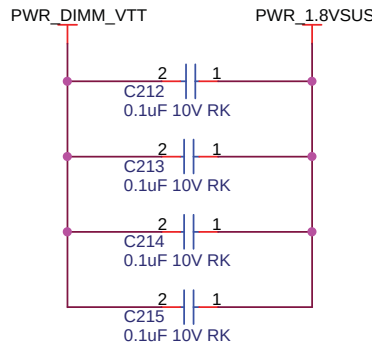
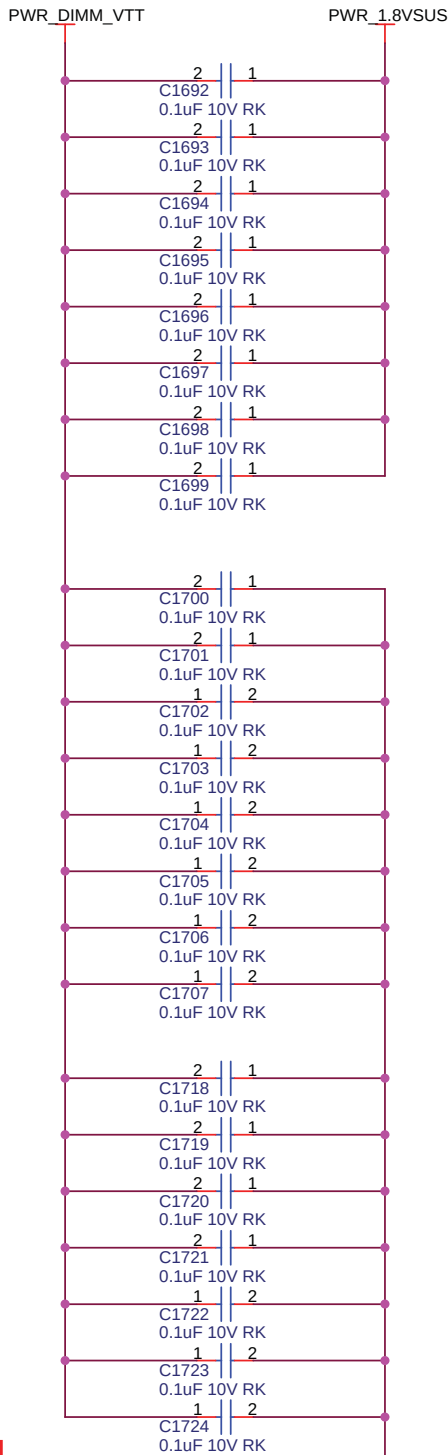
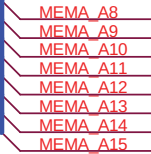
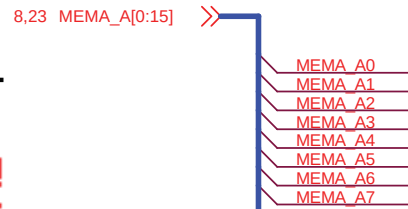
Memory Slot1

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					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	23 / 93
					FUJITSU LTD.			



Memory Slot2

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						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita				
						Sheet	24 / 93	

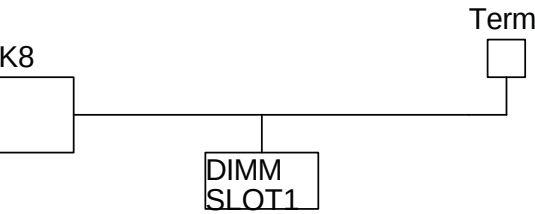


Memory Termination

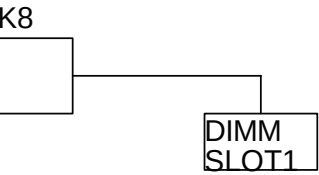
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	Sheet 25 / 93

Channel A

DIMM Address/Command Topology

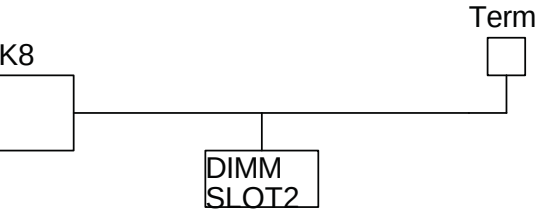


DIMM Data Bus Topology

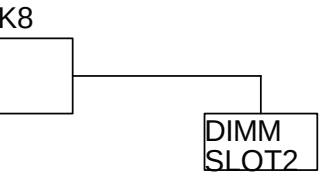


Channel B

DIMM Address/Command Topology

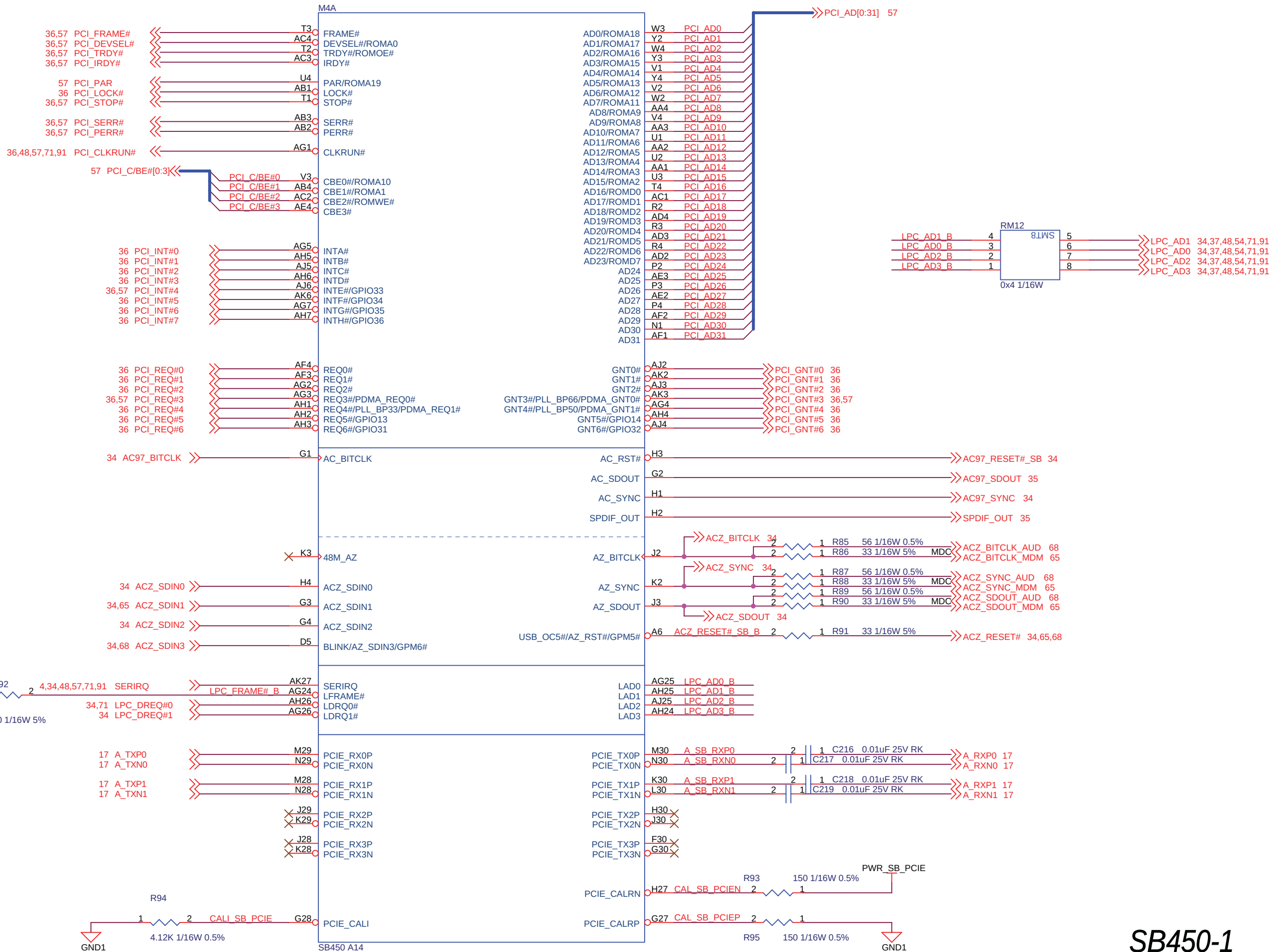
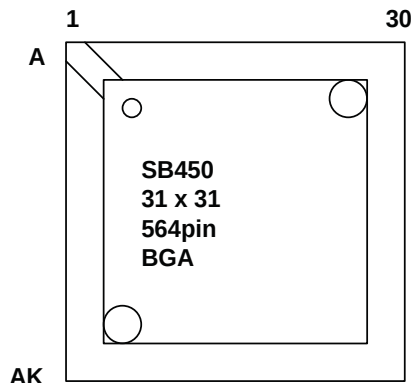


DIMM Data Bus Topology



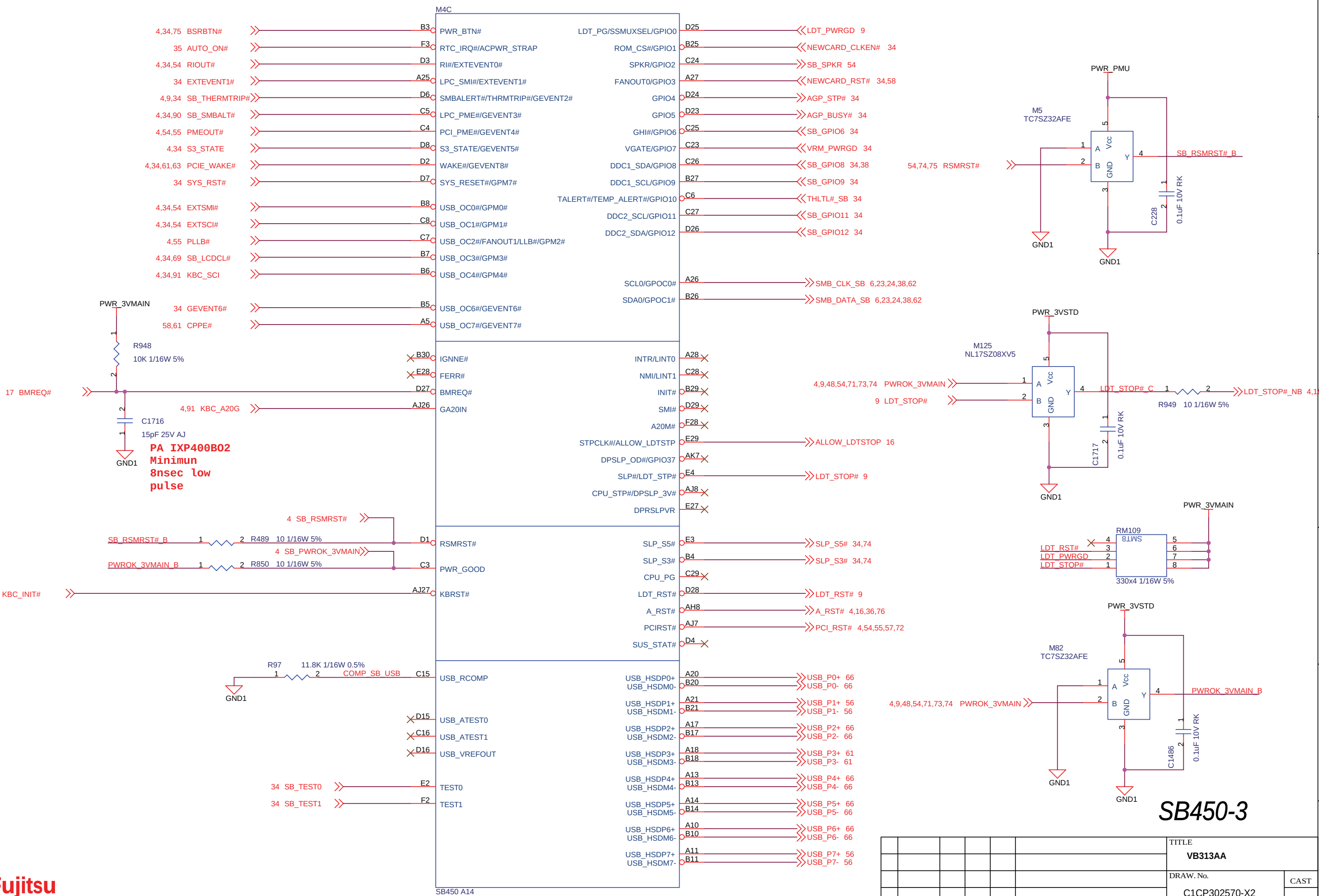
Topology

						TITLE			
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						DRAW. No.			CAST
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Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.	26 / 93

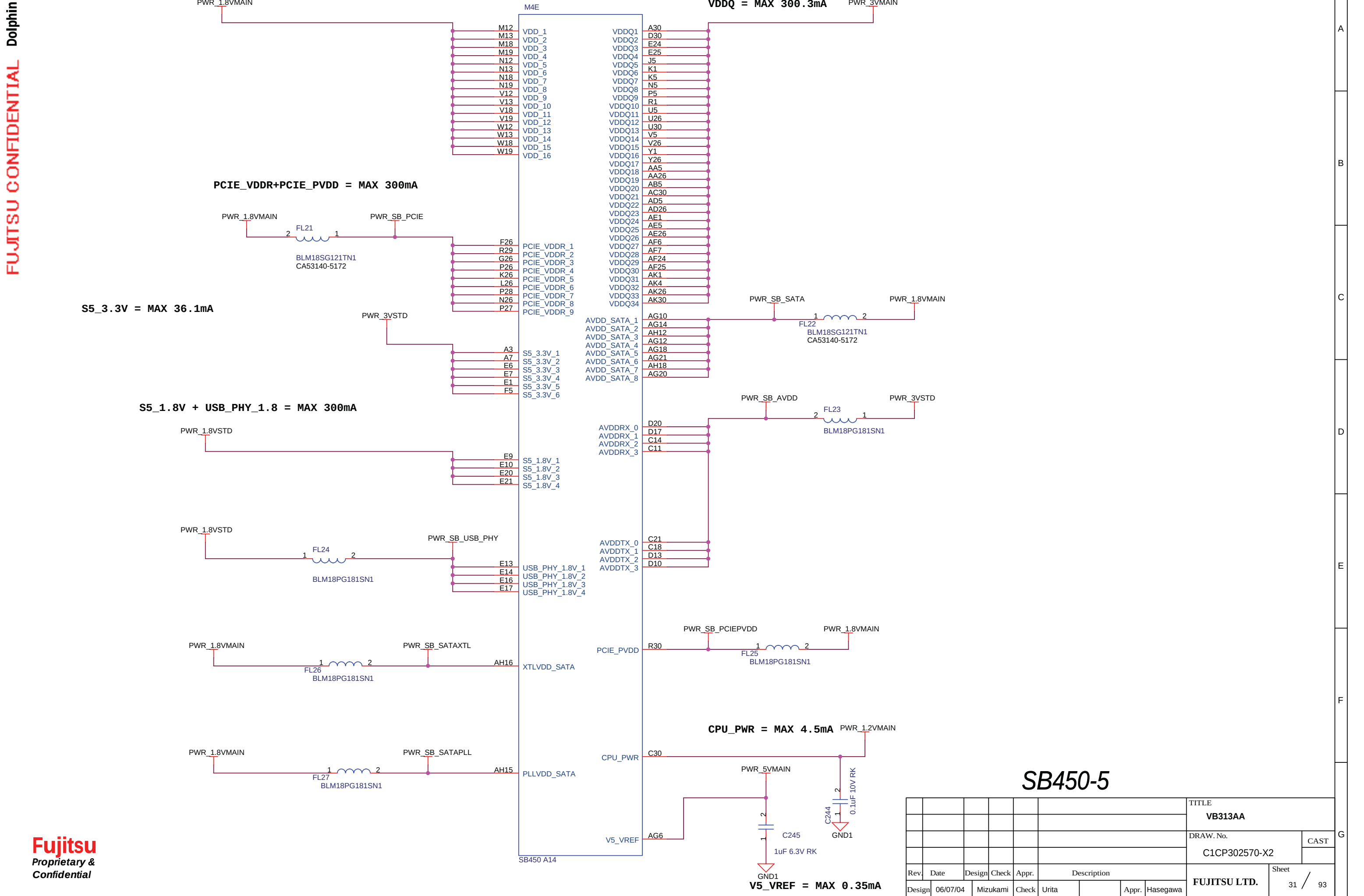


SB450-1

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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		27 / 93



									TITLE VB313AA	
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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		29 / 93

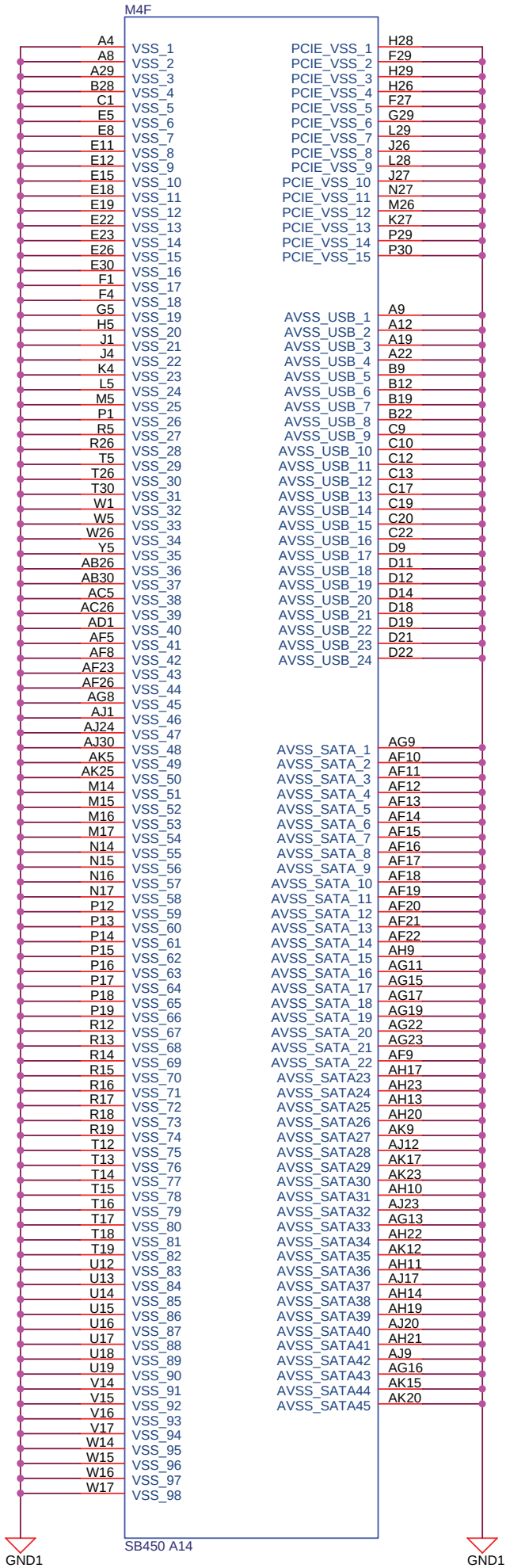


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Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		31 / 93		
						FUJITSU LTD.		

Dolphin

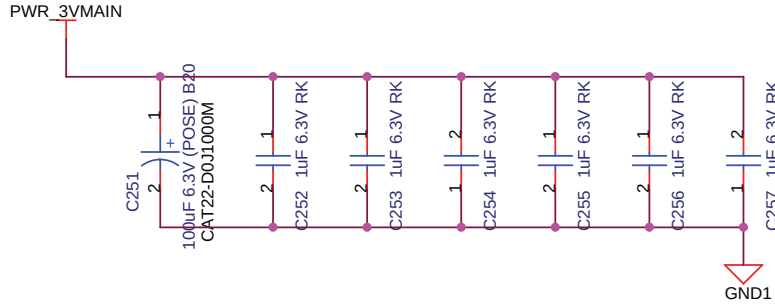
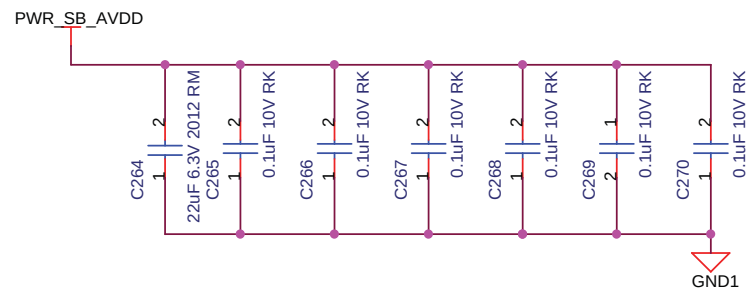
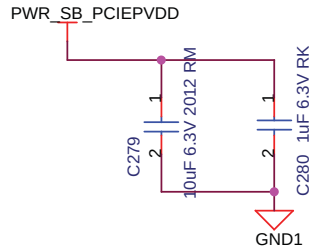
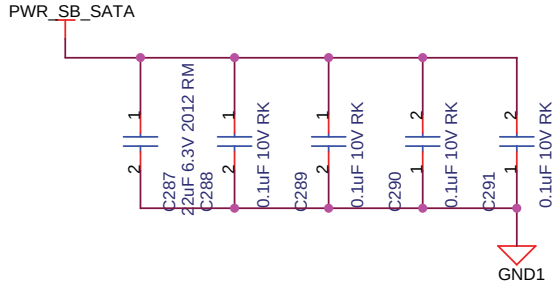
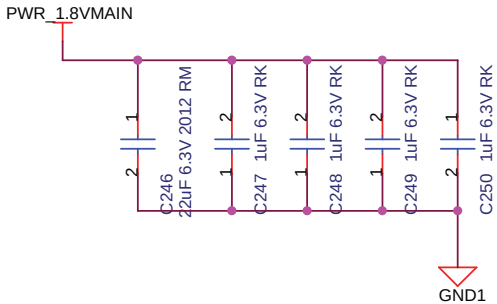
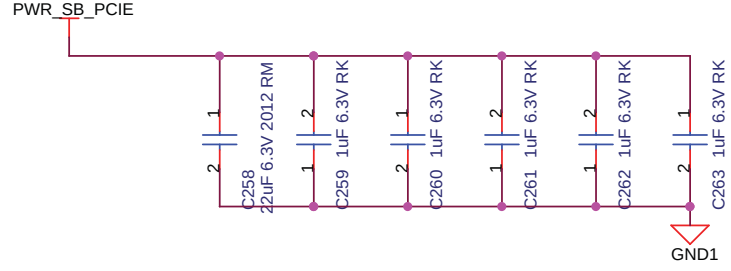
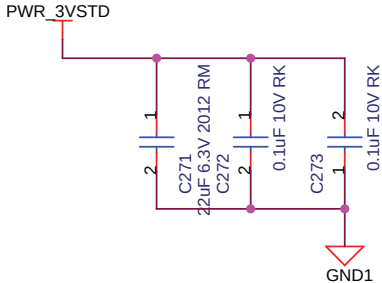
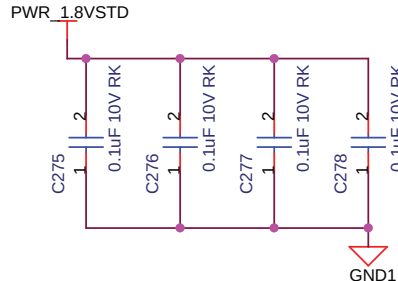
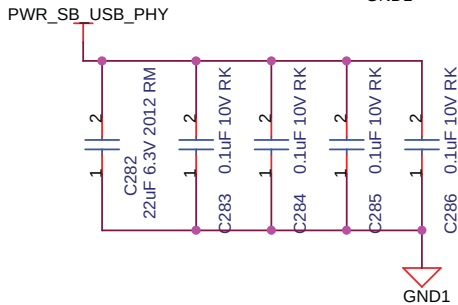
FUJITSU CONFIDENTIAL

Fujitsu
Proprietary &
Confidential



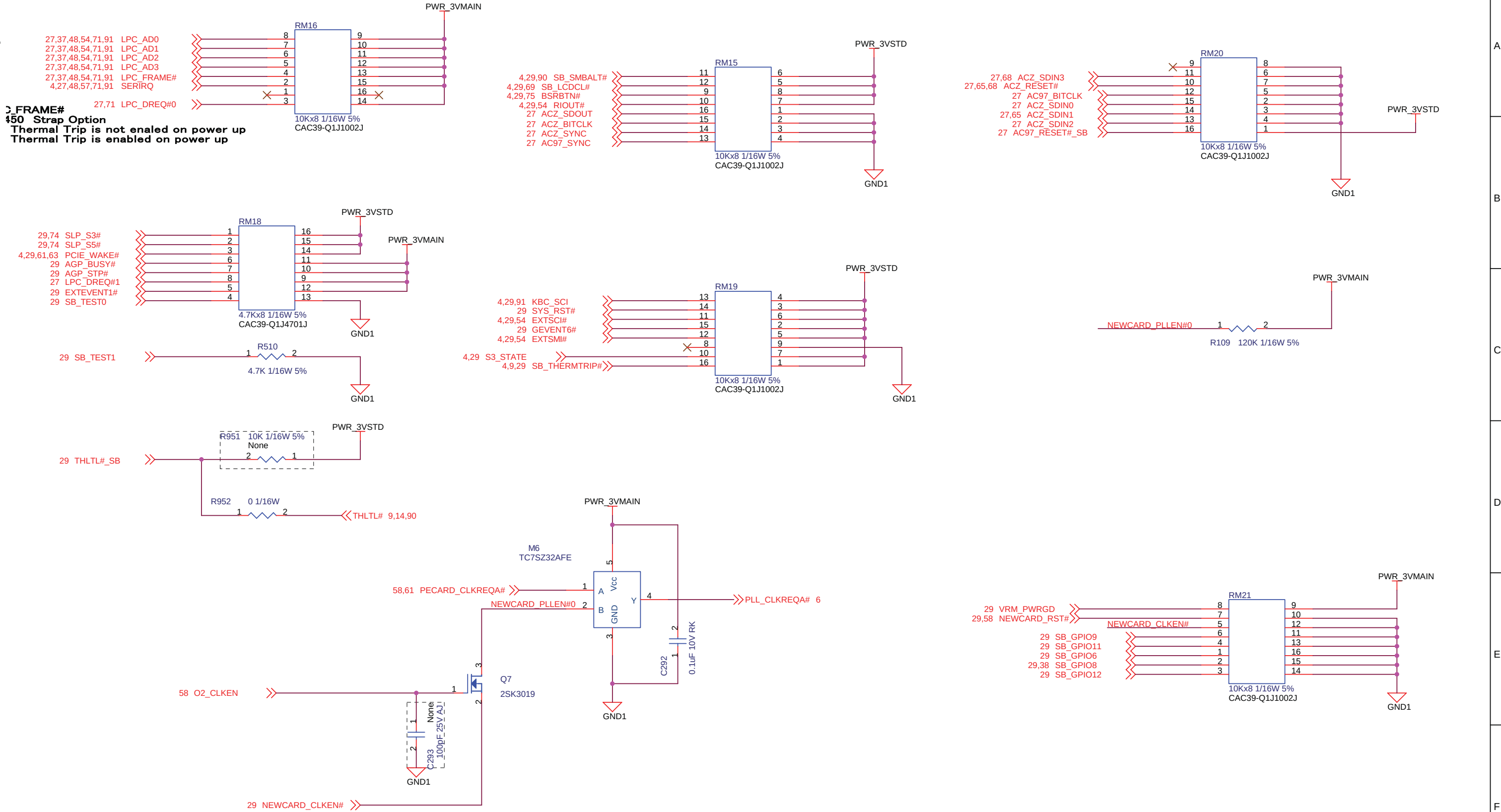
SB450-6

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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	



SB450-7

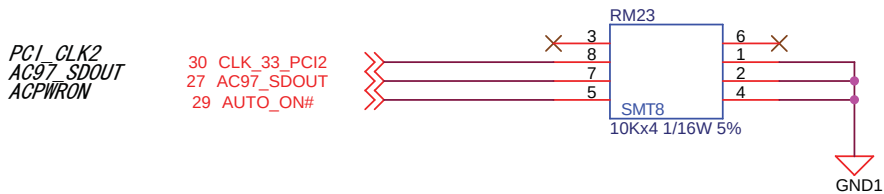
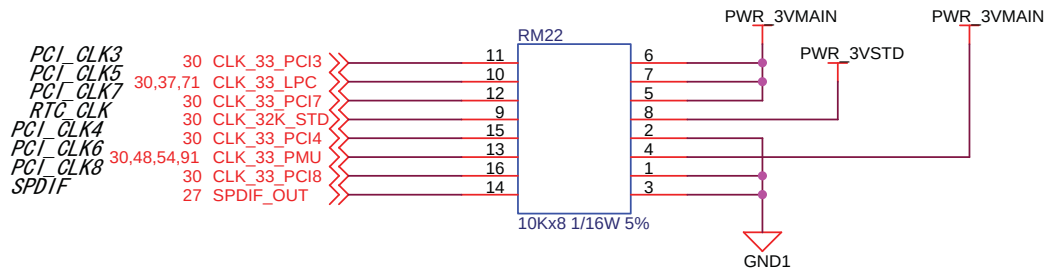
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Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			33 / 93



04/28
部品削除 : R494, R495, R787, R788

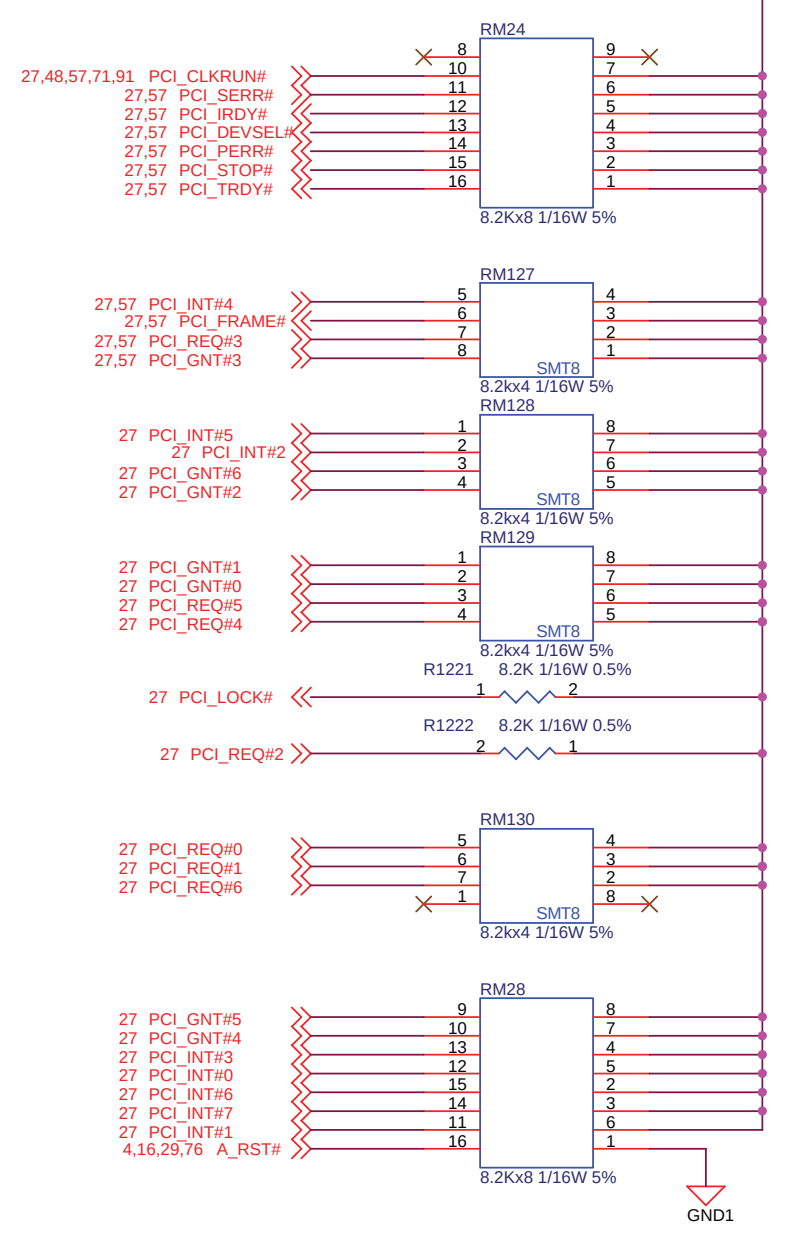
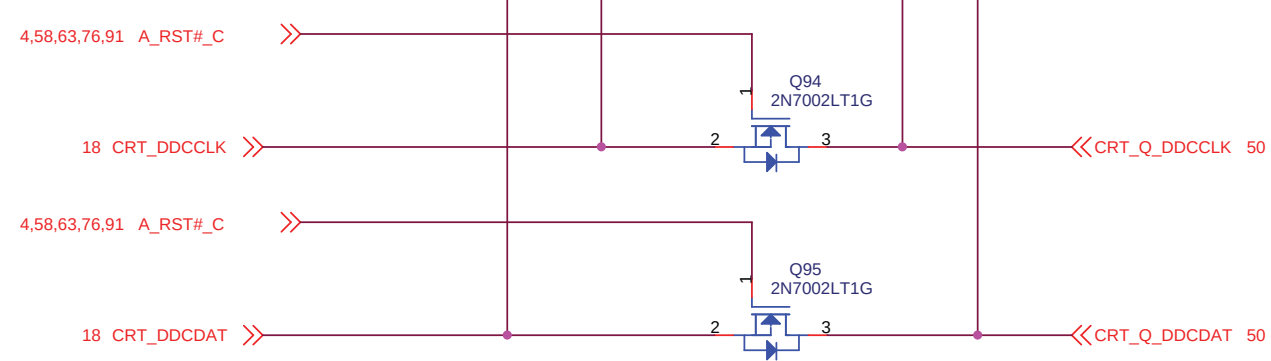
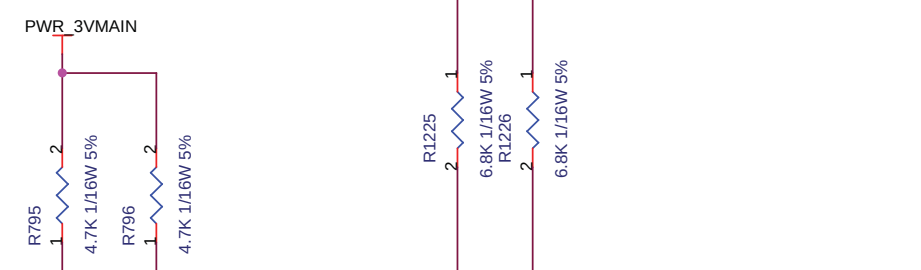
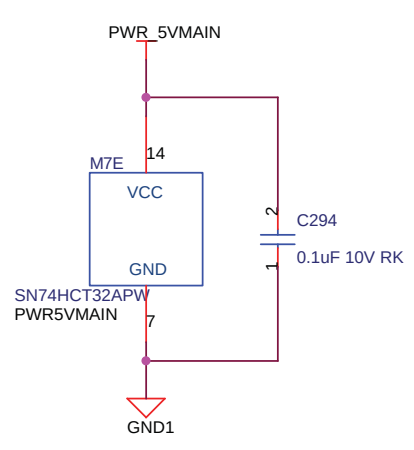
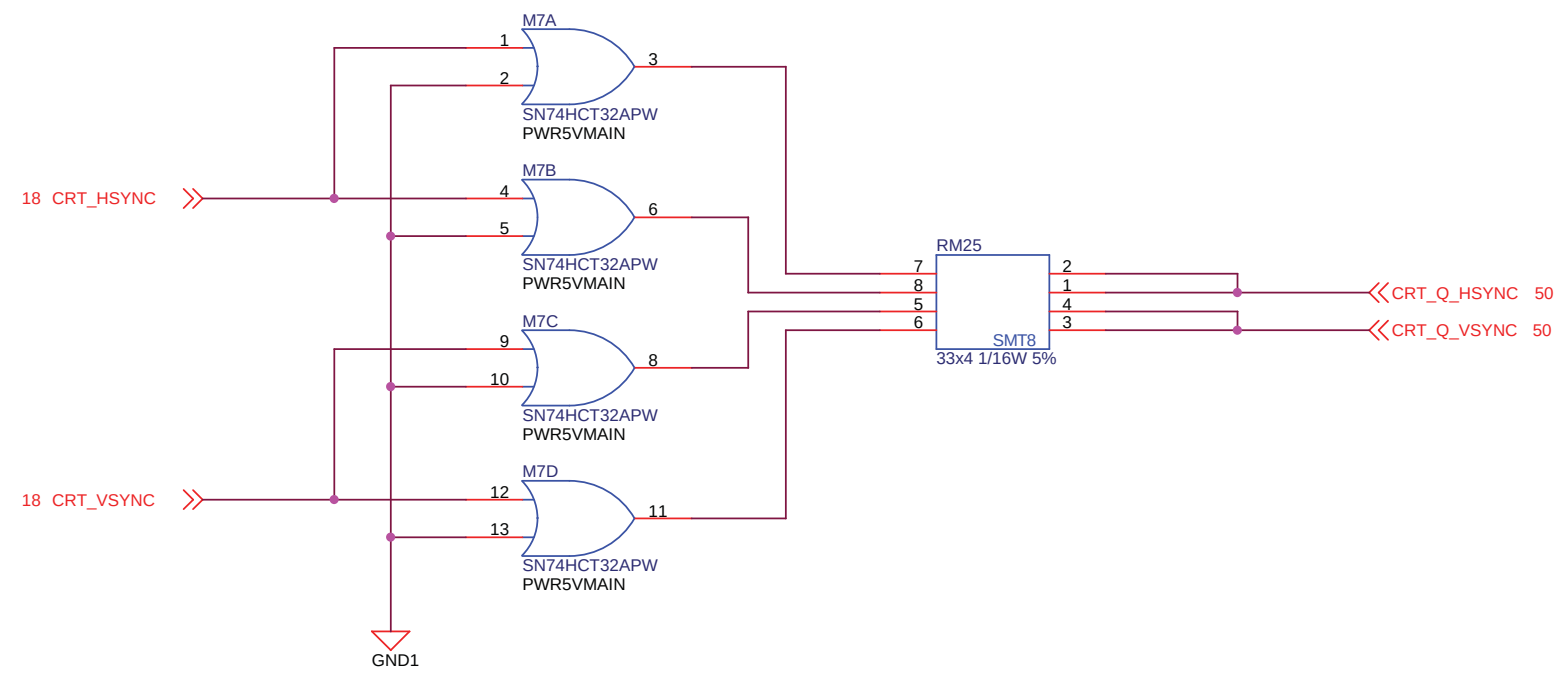
SB450 Pull Up/Down

									TITLE
									VB313AA
									DRAW. No.
									C1CP302570-X2
									CAST
Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr. Hasegawa	34 / 93	FUJITSU LTD.



Pin Name	Description					Post-Beira Setting
ACPWRON	Active Manual Power On. 0 : Automatic Power On 1 : Manual Power On					0
AC97SDOUT	Enable/Disable additional straps for Debugging. 0 : Use Hardcoded defaults for Debug straps 1 : Enable additional Debug Strap					0
SPDIF	Select Speed for Super I/O. 0 : SIO Speed is 48MHz 1 : SIO Speed is 24MHz					0
PCICLK7 PCICLK8	ROM Type Select					1
	PCICLK7	1	1	0	0	
	PCICLK8	0	1	0	1	0
		ROM Type	LPC ROM (256K)	BIOS ROM (X-bus)	FWH	LPC ROM (512K/1M)
PCICLK6	Define Type of CPU 0 : Intel Processors 1 : AMD K8					1
PCICLK5	48MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer					1
PCICLK4	Bypsd USB PLL 0 : use external 48MHz 1 : use internal USB					0
PCICLK3	USB PLL Down 0 : Enable 1 : Disable					1
PCICLK2	48MHz Clock Pad Select 0 : Clock Input Buffer 1 : Ctystal Pad					0
RTC_CLK	RTC Select 0 : External RTC 1 : Internal RTC					1
LFRAME#	Thermal Trip Strap 0 : Thermal Trip is not enabled on power up 1 : Thermal Trip is enabled on power up (default)					1

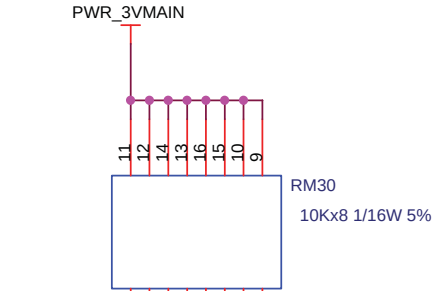
Pin Name	Description	
IDEPDack	Generate Short Reset 0 : Use Short Reset 1 : Use Long Reset	
PCI_AD31 PCI_AD30	Overcharge Pump control Bit	
PCI_AD29 PCI_AD28	PLL VCO control bits	
PCI_AD27	Bypass PCI PLL 0 : Use internal IDE PLL. Generated PCI CLK 1 : Bypass internal PCI PLL	
PCI_AD26	Bypass ACPI BCLK 0 : Use internal ACPI_BCLK 1 : Bypass ACPI_BCLK	
PCI_AD25	Bypass IDE Clock 0 : Use Internal IDE CLK 1 : Bypass Internal IDE	
PCI_AD24	BLK core strap from I2ROM enable 0 : Use default Value 1 : getting the value from I2C	
PCI_AD23	EPROM Reserved	



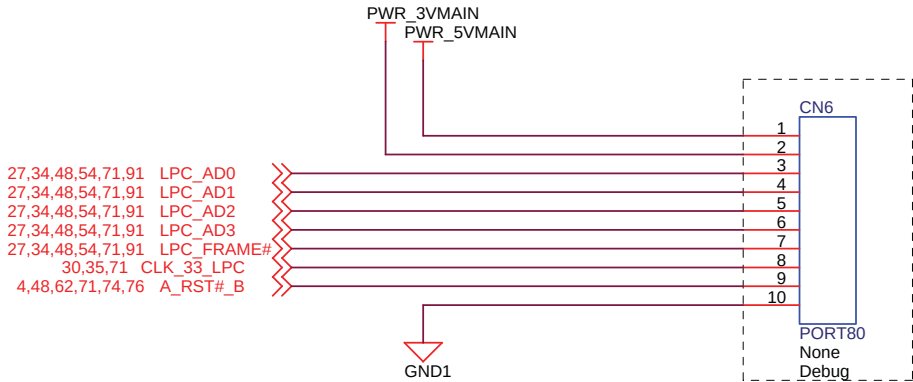
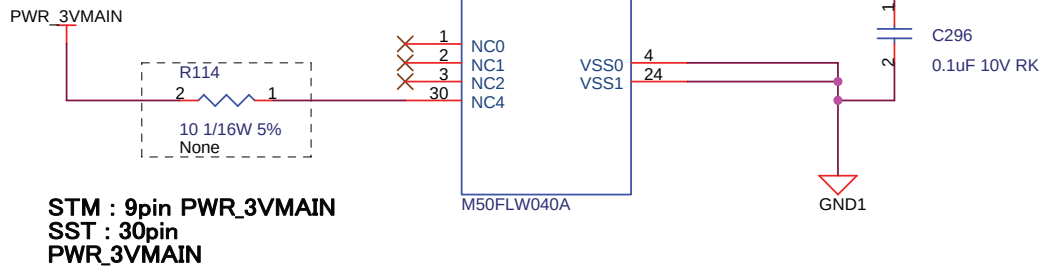
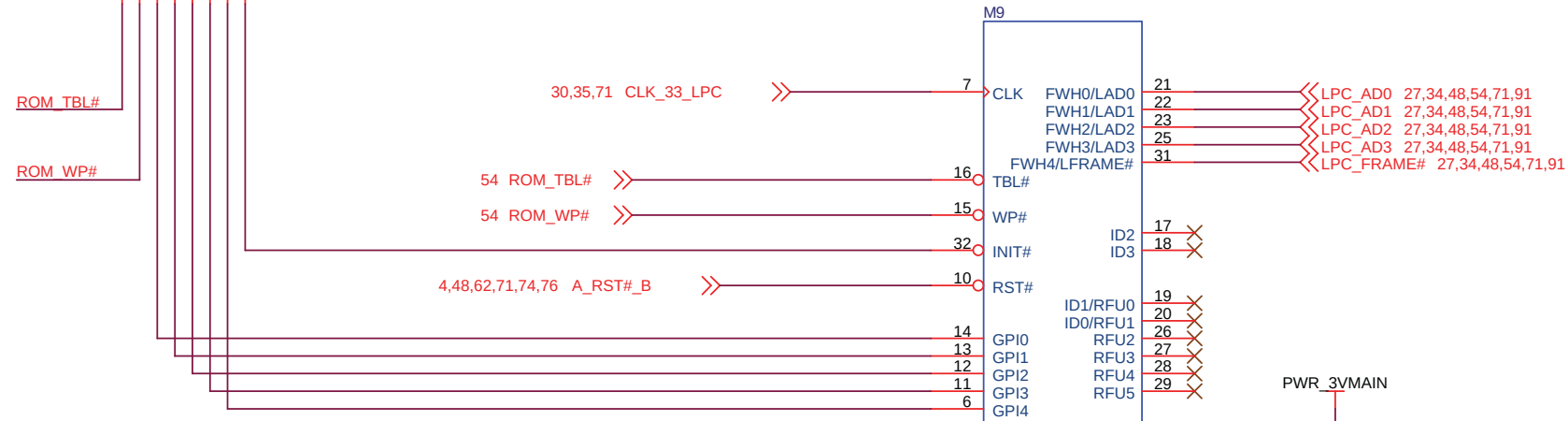
上記多連部品(8.2Kx4)については
配線しやすいようにピンスワップ可能。

Pullup for
AGP,PCI,LPC

					TITLE			
					VB313AA			
					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
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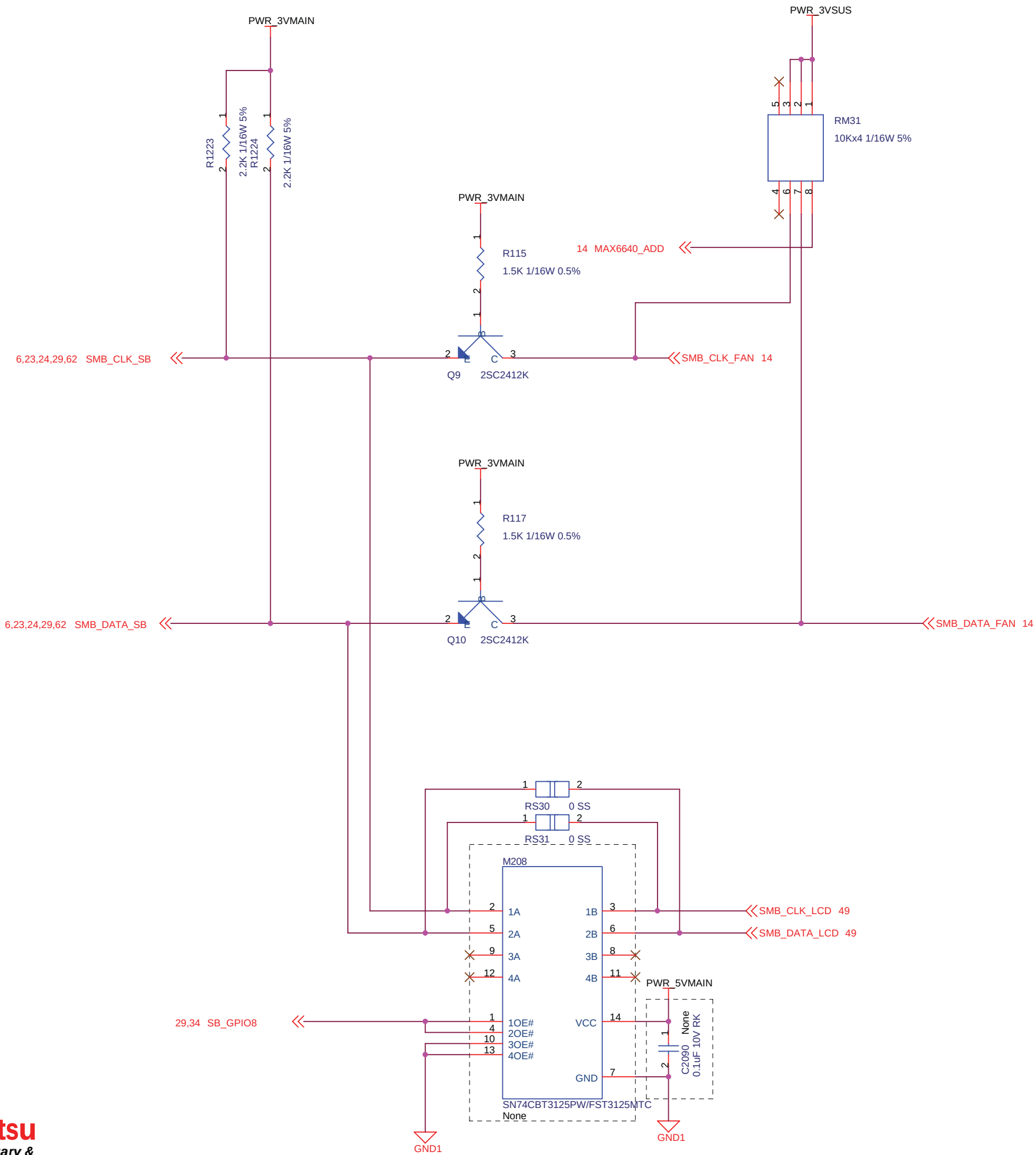


Socket for LPC ROM.
※LPC ROMはソケットを実装可能なパターンにすること。



LPC ROM

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						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description		Sheet
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Device	Hex	Address
MAX6640	5Eh	0101 111x b
MEM slot0	A2h	1010 001x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b

BUS	Device	address
	DIMM1	A2h
	DIMM2	A4h
	MAX6640	5Eh
	LCD	A0h
PLL	PLL	D2h
PMU	PMU	32h

SMBus

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
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FUJITSU CONFIDENTIAL

Dolphin

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Reserve

					TITLE		
					VB313AA		
					DRAW. No.		CAST
					C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa

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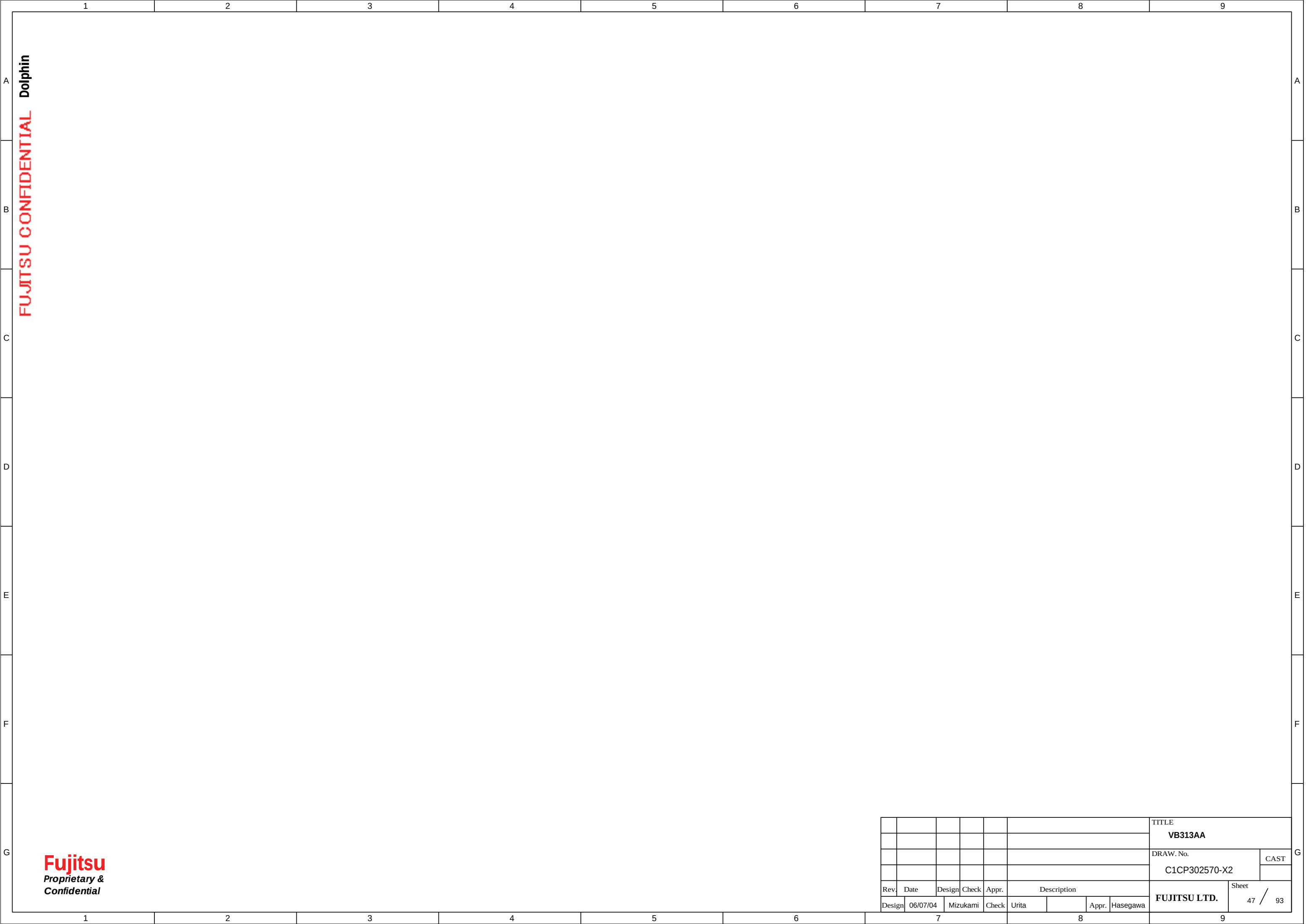
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Rev.		Date		Design		Check		Appr.		Description				FUJITSU LTD.		Sheet	
Design		06/07/04		Mizukami		Check		Urita				Appr.		Hasegawa		46 / 93	
1		2		3		4		5		6		7		8		9	



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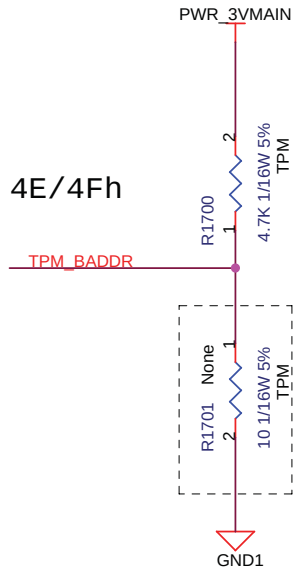
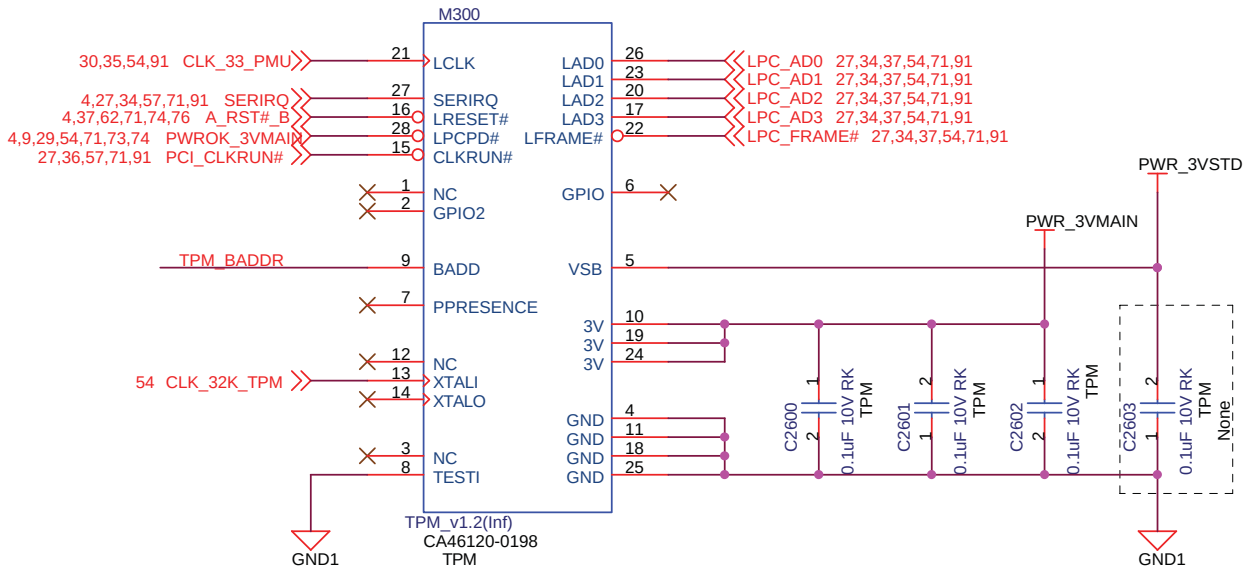
Dolphin

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Proprietary &
Confidential

						TITLE			
						VB313AA			
						DRAW. No.			CAST
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Fujitsu Ltd.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	47 /	93

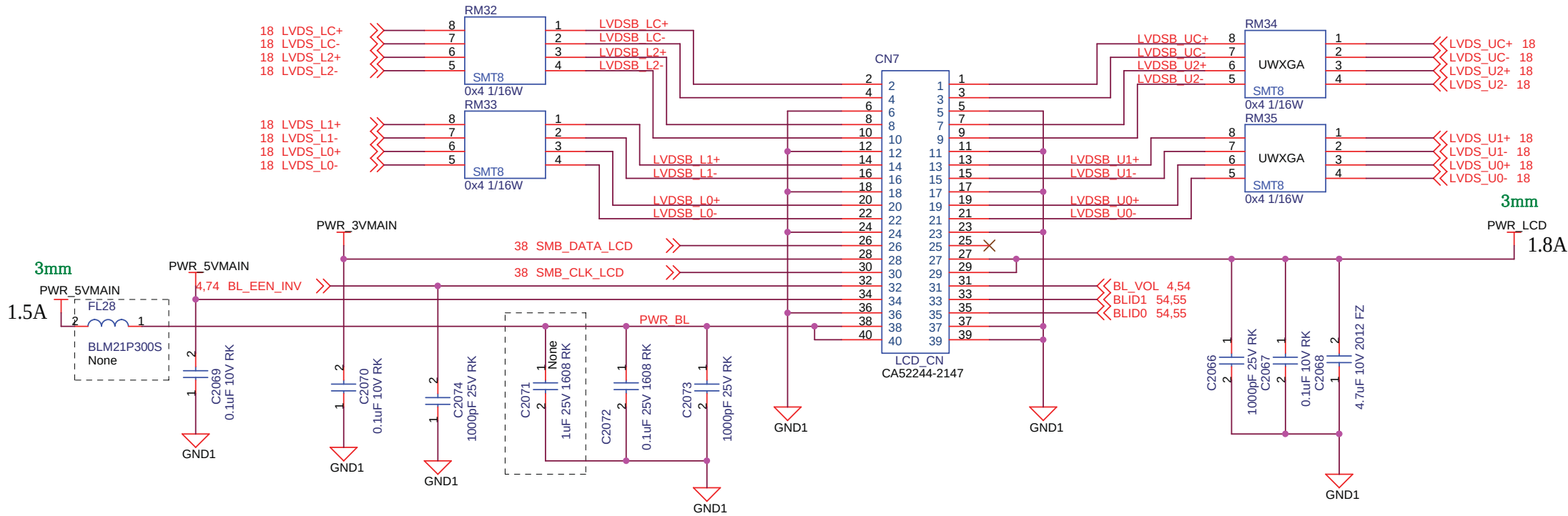
TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh



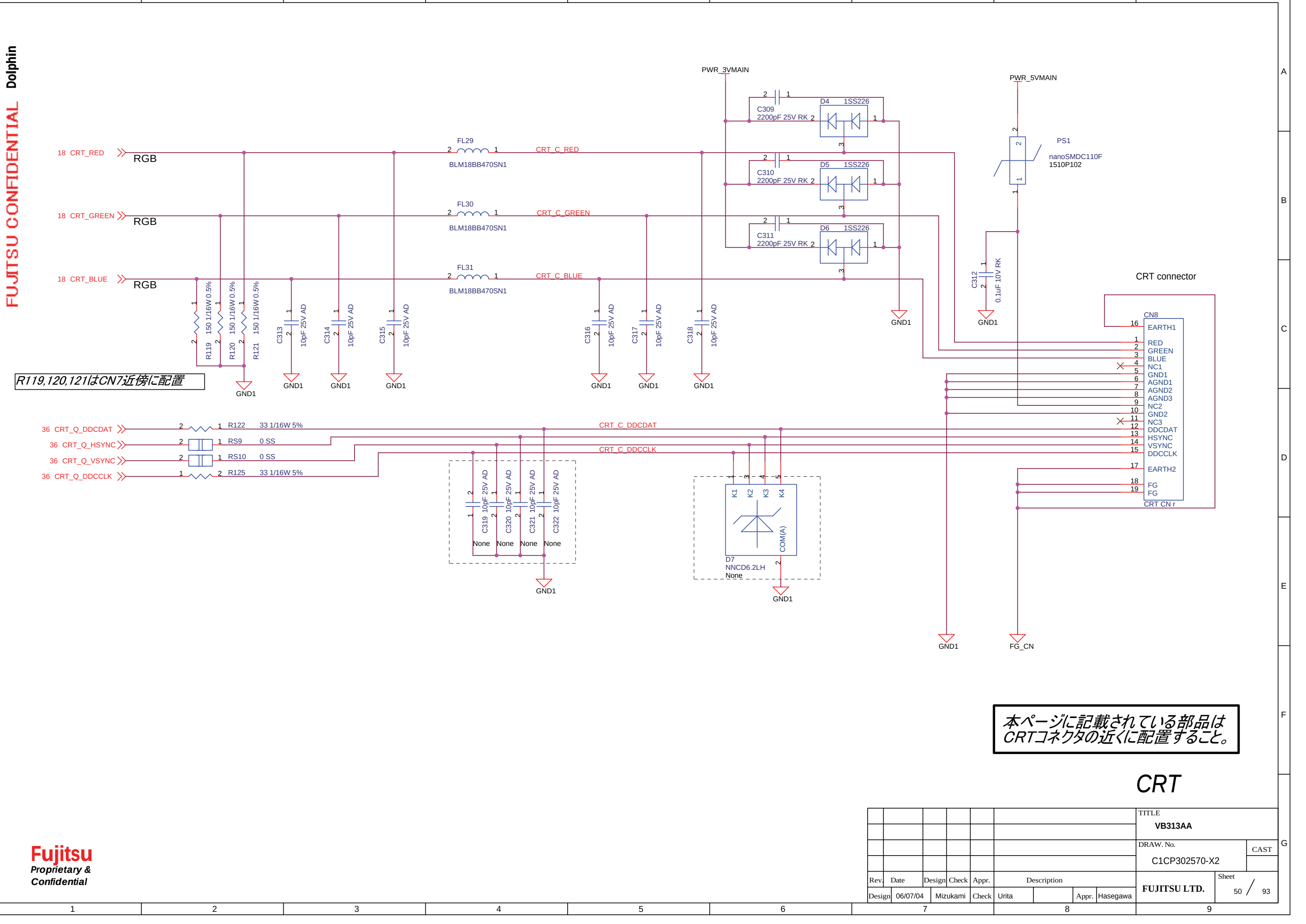
TPM

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	48 / 93



Stab of LVDS is shortest.

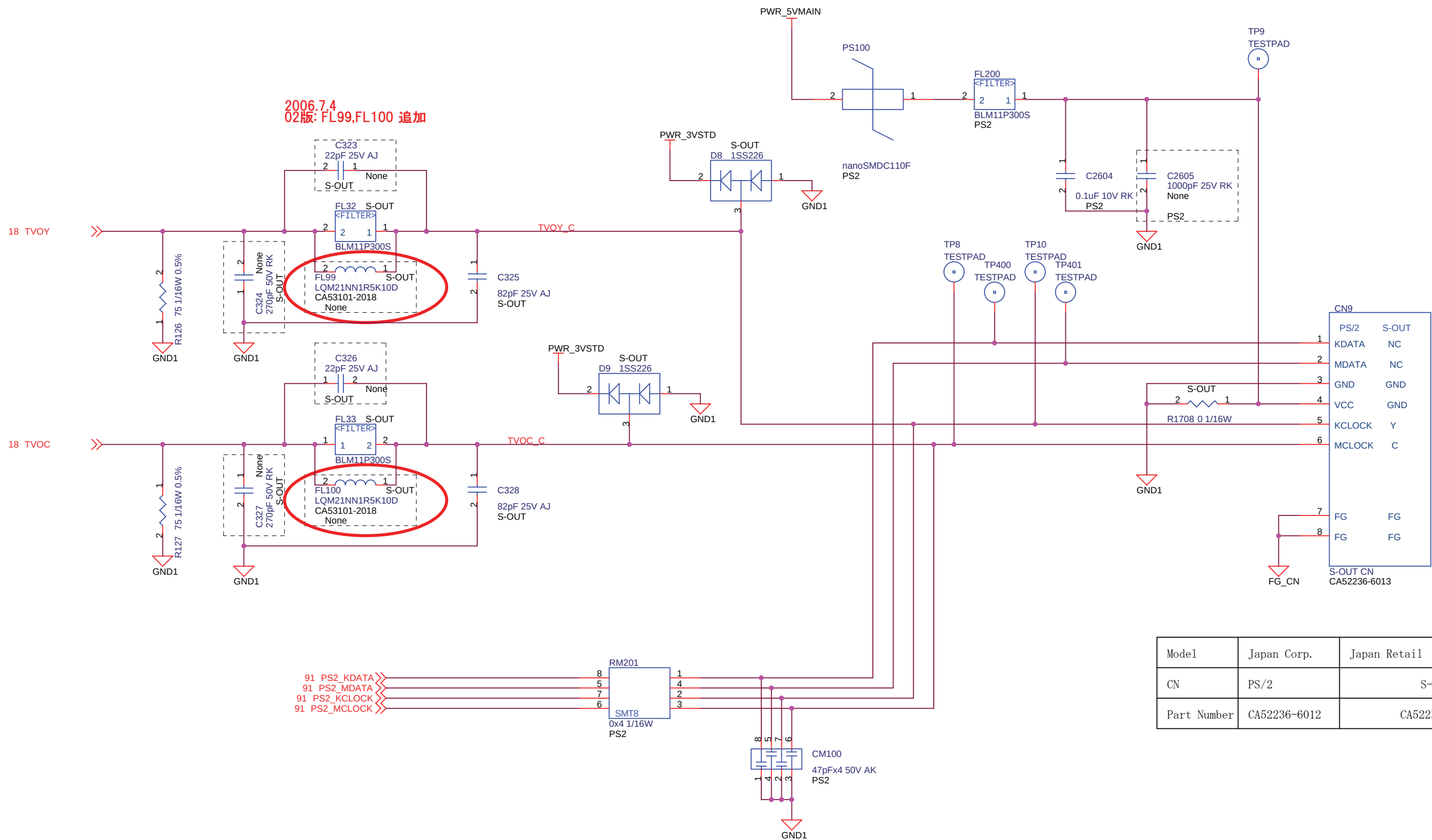
					TITLE			
					VB313AA			
					DRAW. No.			CAST
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 49 / 93



本ページに記載されている部品は
CRTコネクタの近くに配置すること。

CRT

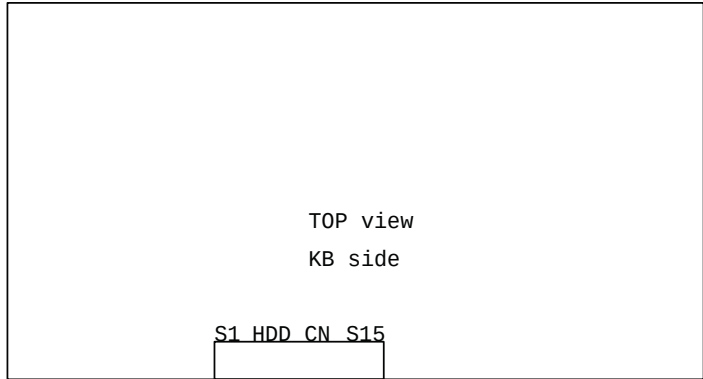
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					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							50 / 93	



Model	Japan Corp.	Japan Retail Oversea
CN	PS/2	S-OUT
Part Number	CA52236-6012	CA52236-6013

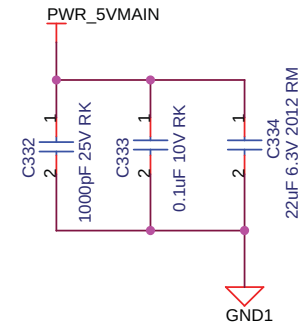
S-OUT/PS2

								TITLE	
								VB313AA	
								DRAW. No.	
								C1CP302570-X2	
								CAST	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	Sheet 51 / 93	

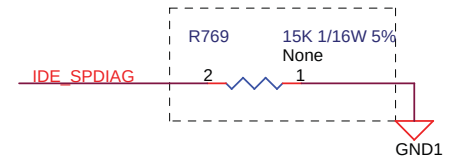
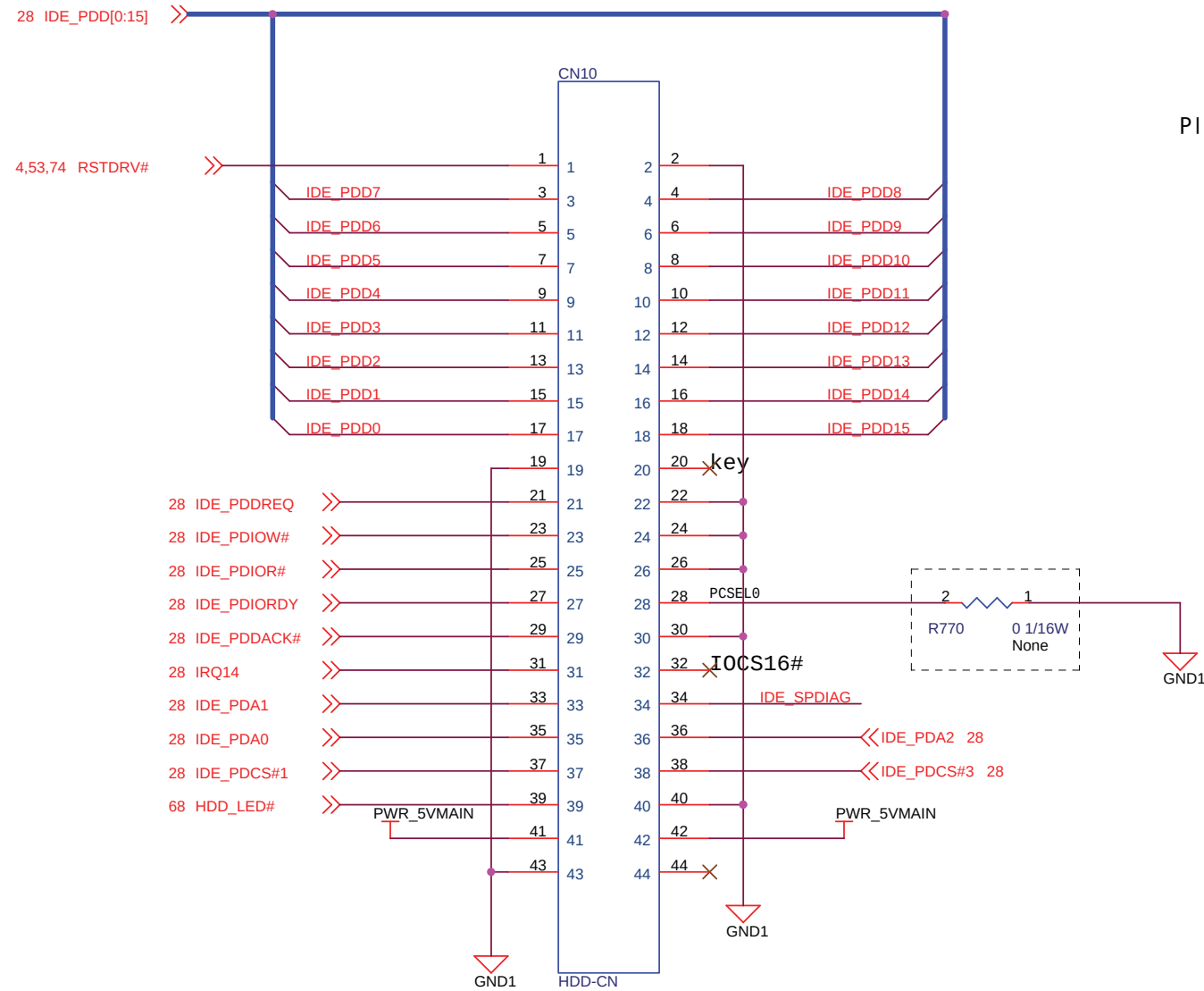


Max:2A

Supply enough current volume.
Need tie to GND1 fully.

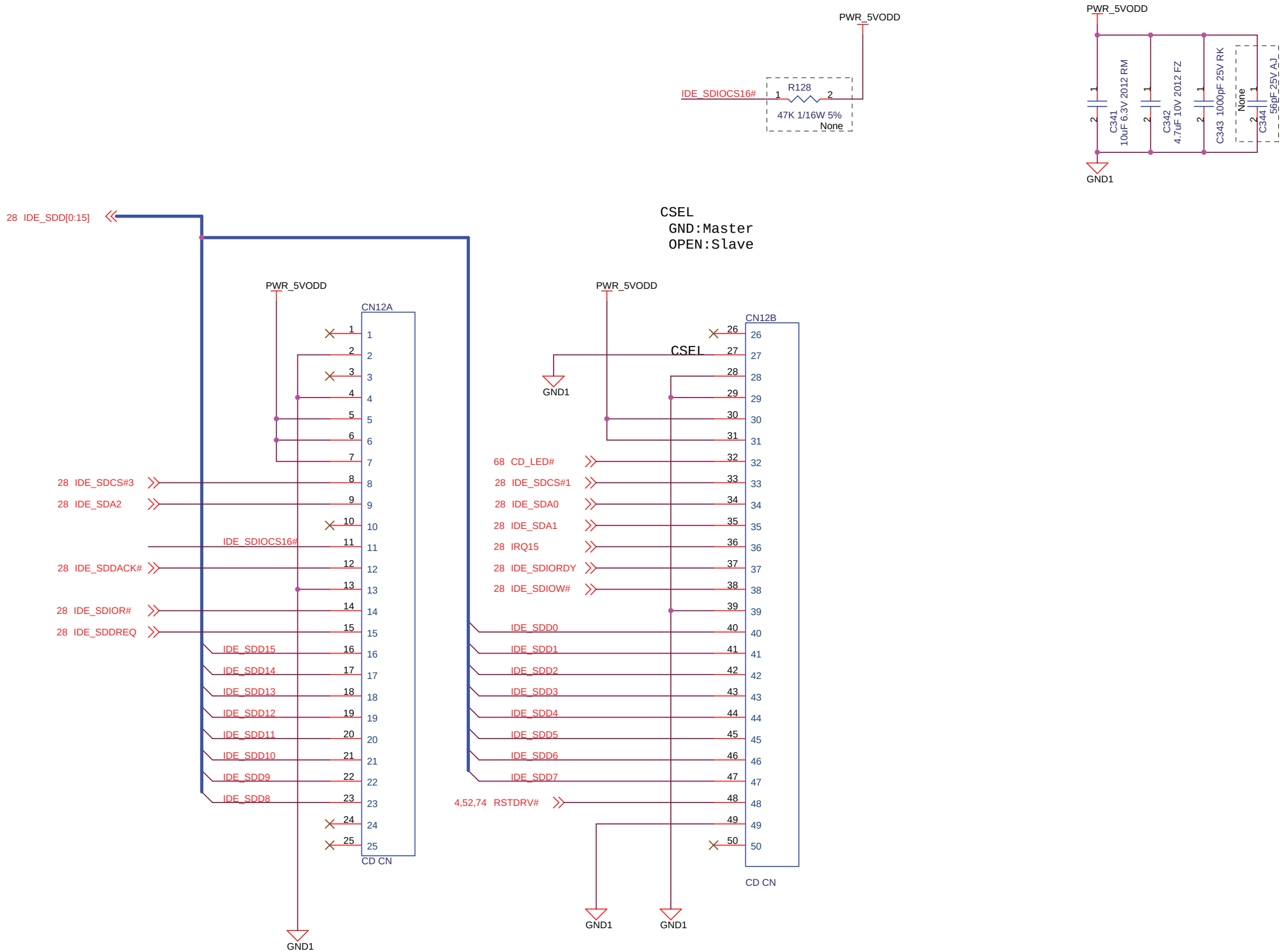


Place the capacitors near power pin of HDD CN



1st HDD CN

						TITLE VB313AA DRAW. No. C1CP302570-X2 CAST	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD. Sheet 52 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	



ODD-CN

						TITLE VB313AA					
									DRAW. No.		
									C1CP302570-X2		
								CAST			
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		53 / 93		

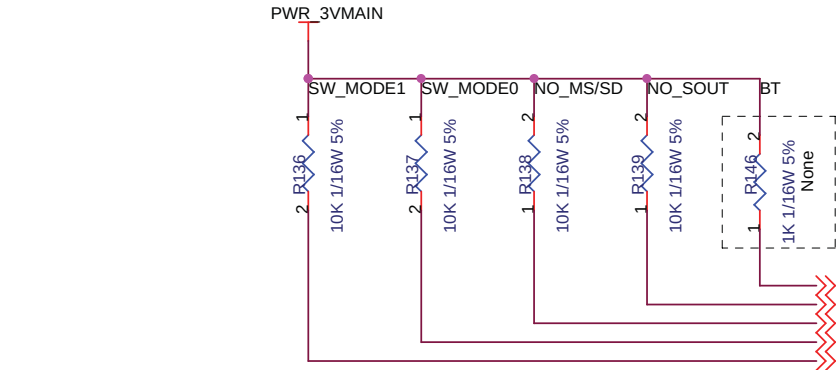
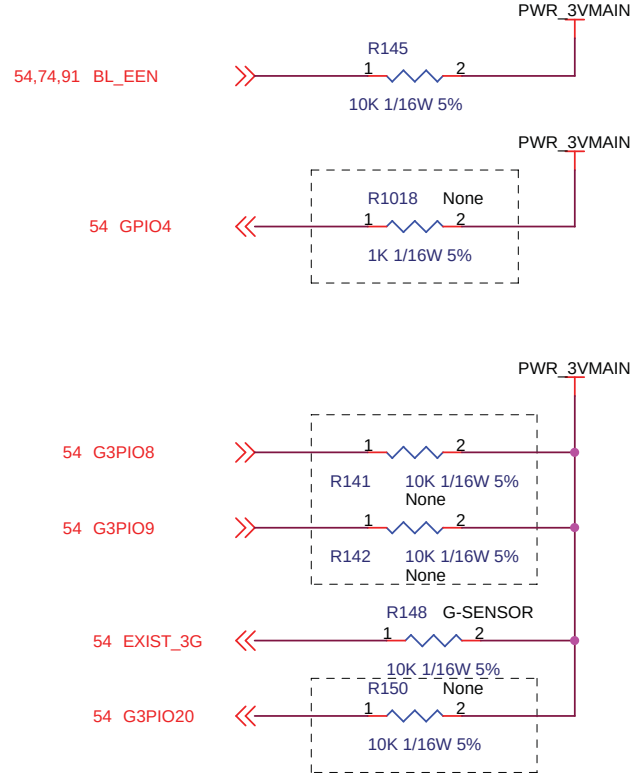
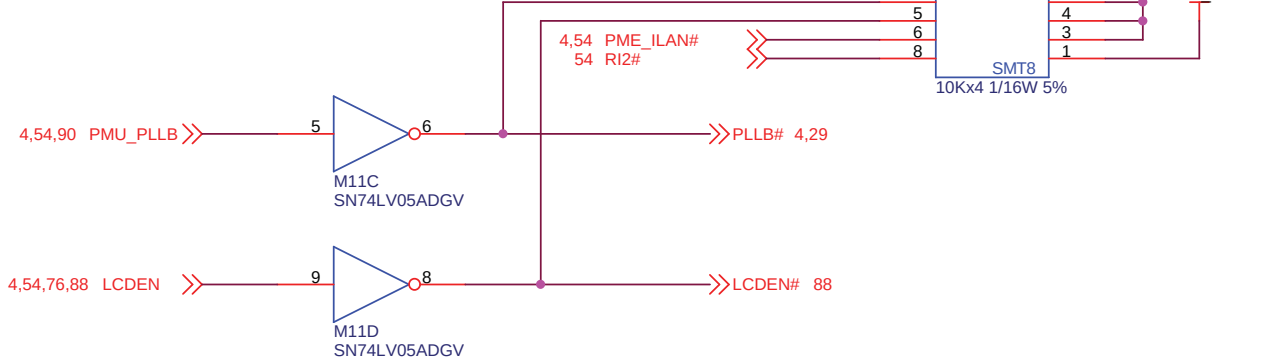
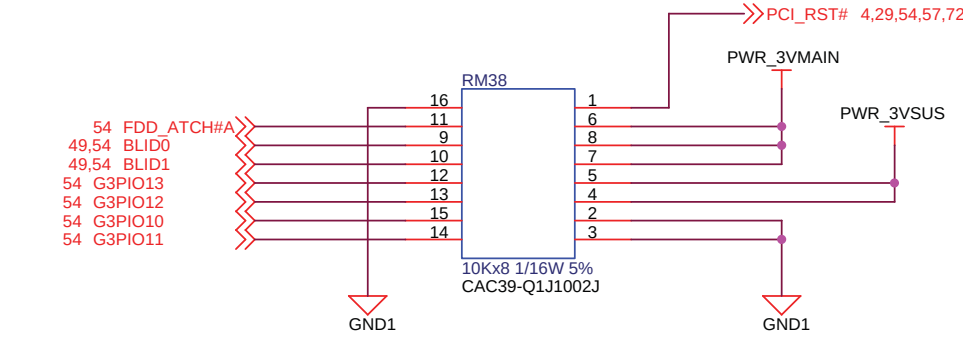
(Wireless LAN)

(Marvel LAN)

(RS232C)

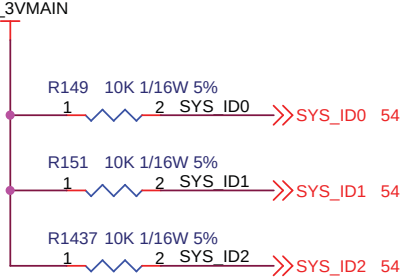
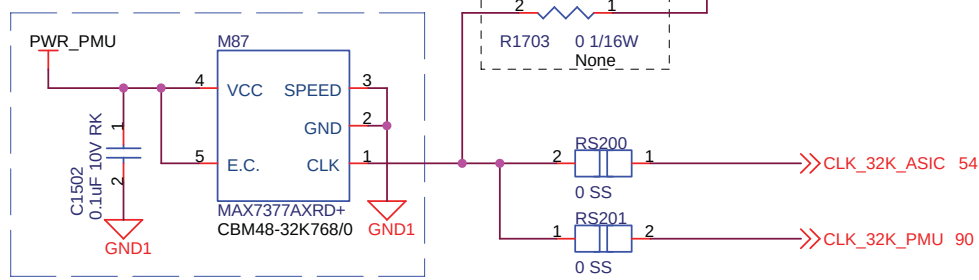
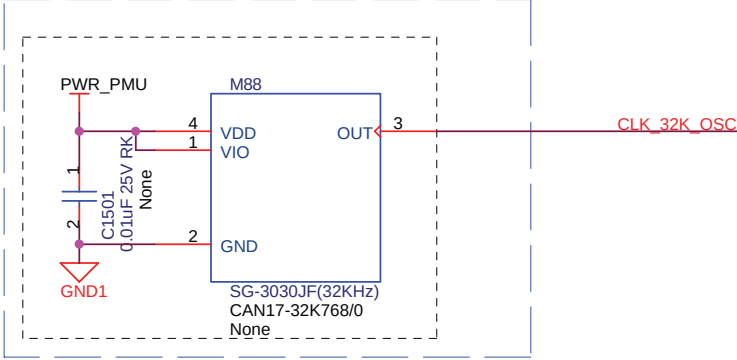
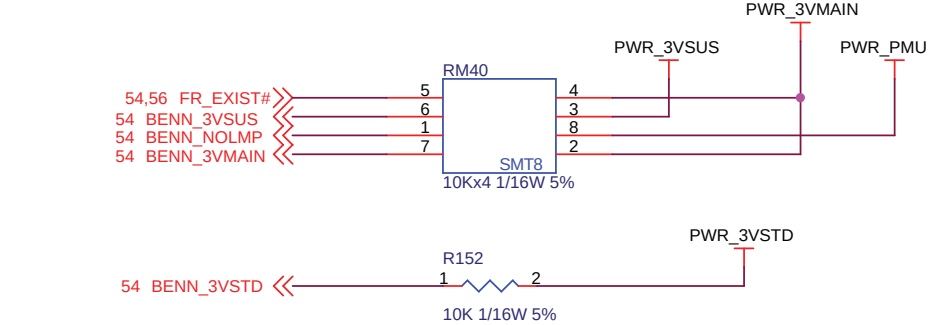
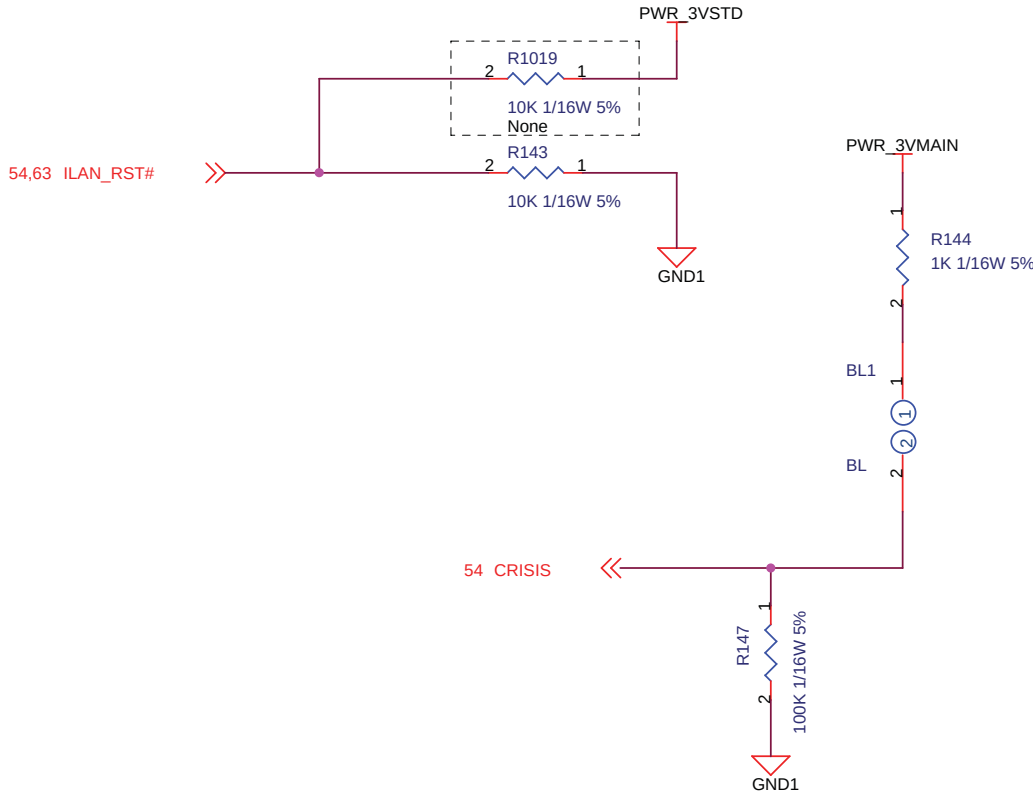
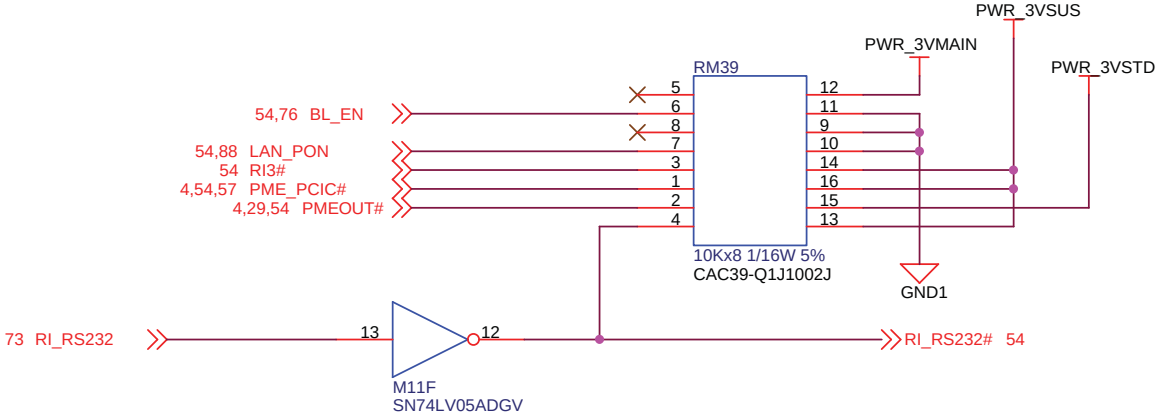
BENN

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	54 / 93



SW_MODE[1:0]
00 : 4ボタン(店頭/FCS)
[Appli], [Appli], [VolumeDown], [VolumeUp]
01 : 4ボタンモデル(FKL/FPC)
[Appli], [Appli], [Appli], [Appli]
10 : クラサバモデル
(T.B.D)
11 : 6ボタンモデル(仕向け先は未定。06秋冬はなし)
[Internet], [Mail], [A], [B], [VolumeDown], [VolumeUp]

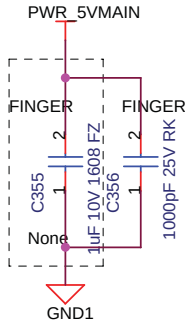
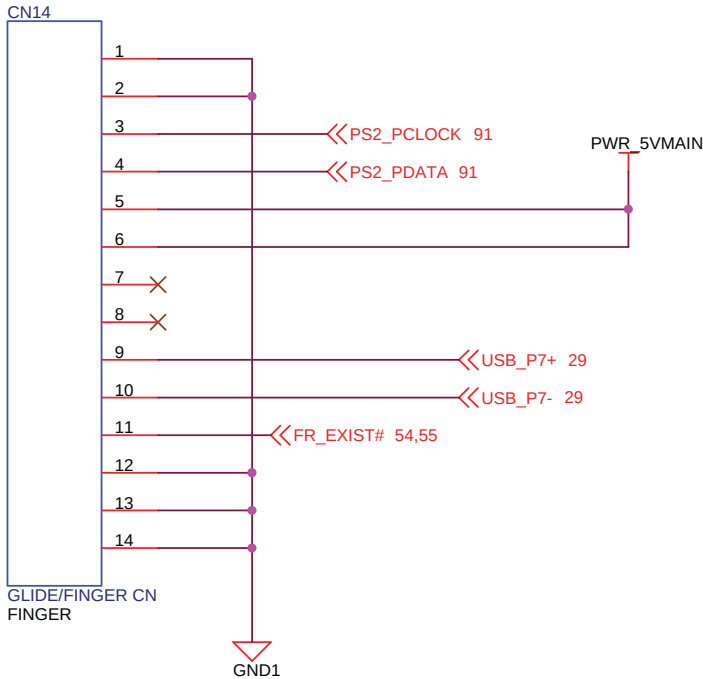
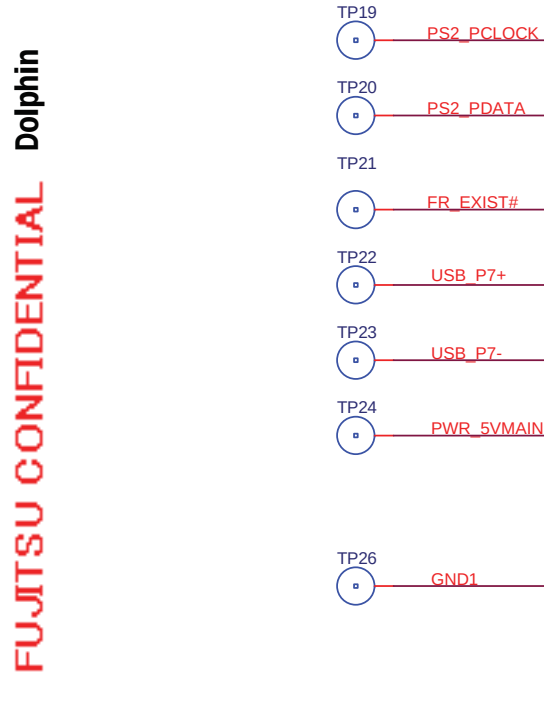
※IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。



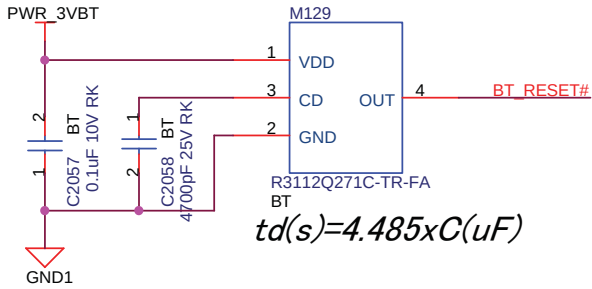
SYS_ID[2:0]
000 : 国内店頭
001 : 海外
010 : クラサバ
011 - 111 : Reserve

*Pullup/down
for BENN*

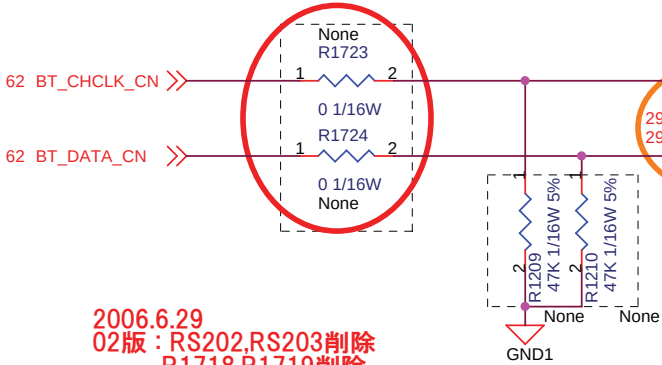
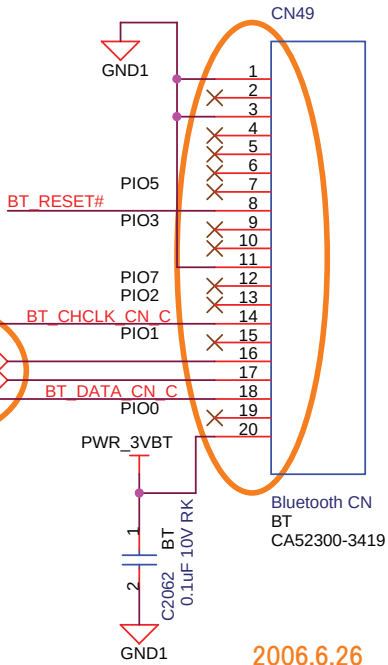
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									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet 55 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			



Target 20ms



$td(s)=4.485 \times C(uF)$



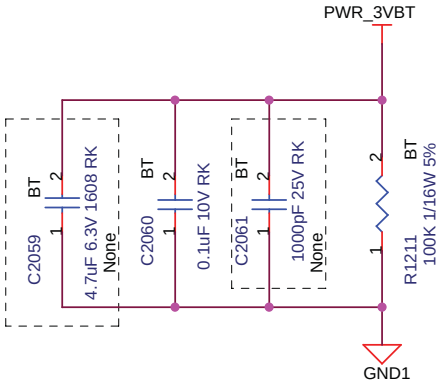
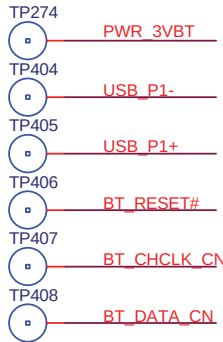
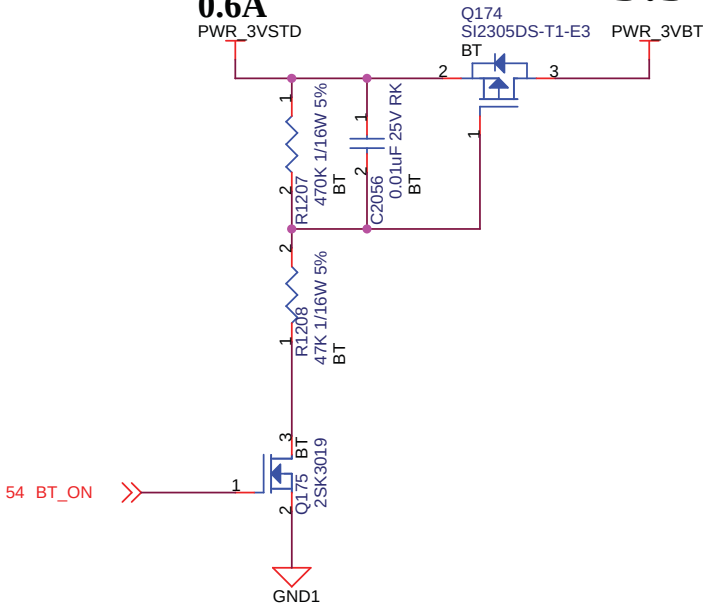
2006.6.29
02版 : RS202,RS203削除
R1718,R1719削除

2006.6.26
02版 : USB_P1+とUSB_P1-入れ替え

2006.6.26
02版 :
CN49のピンアサインを逆に変更

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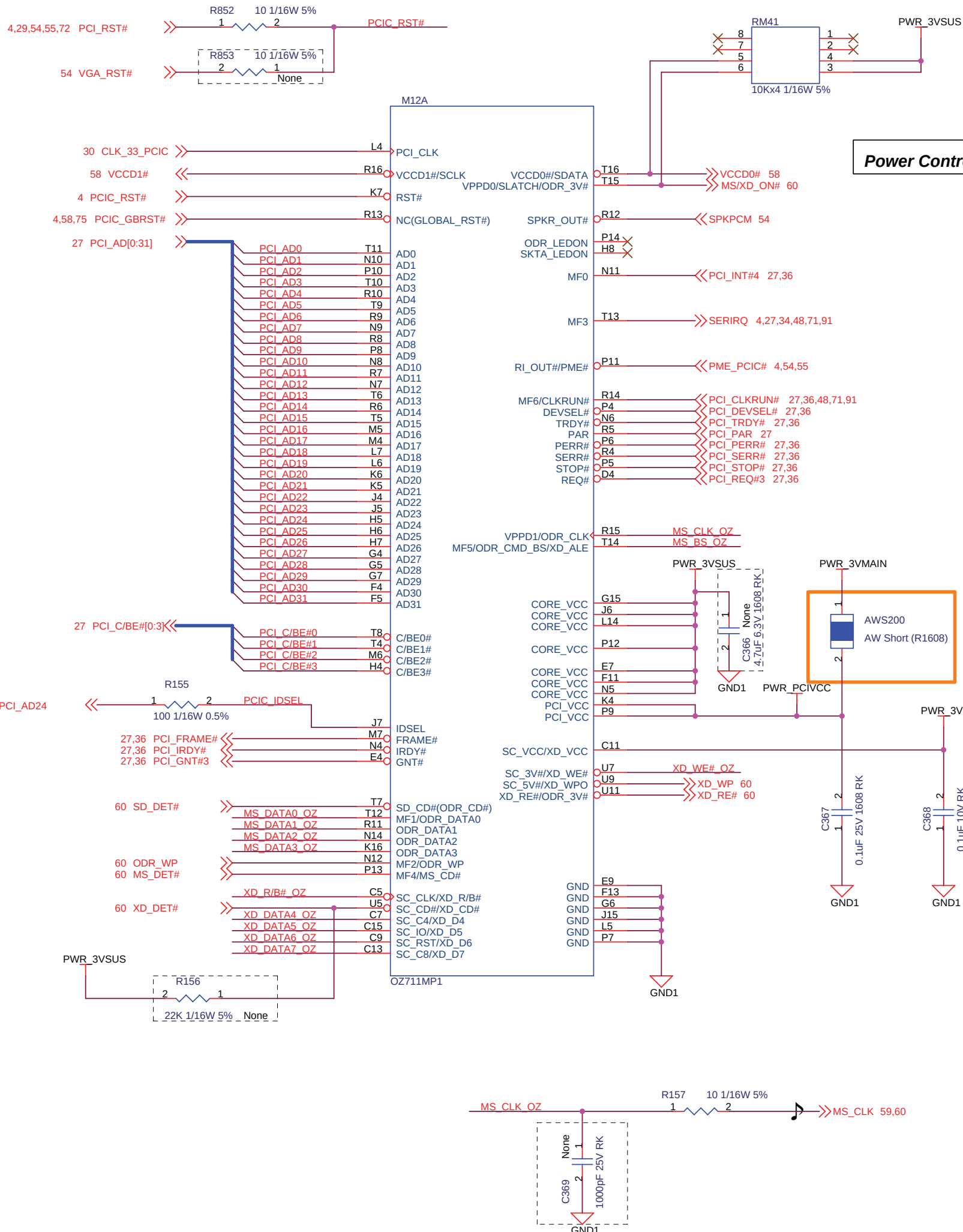
2mm
0.6A
3mm
3.3V/0.6A



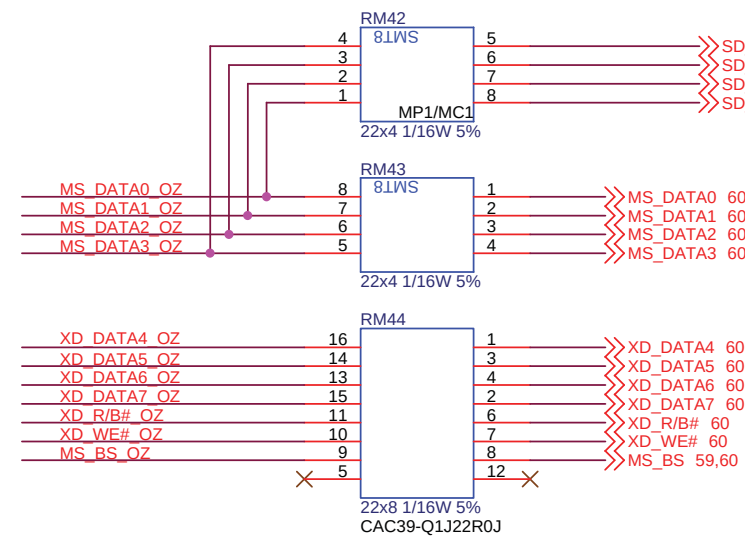
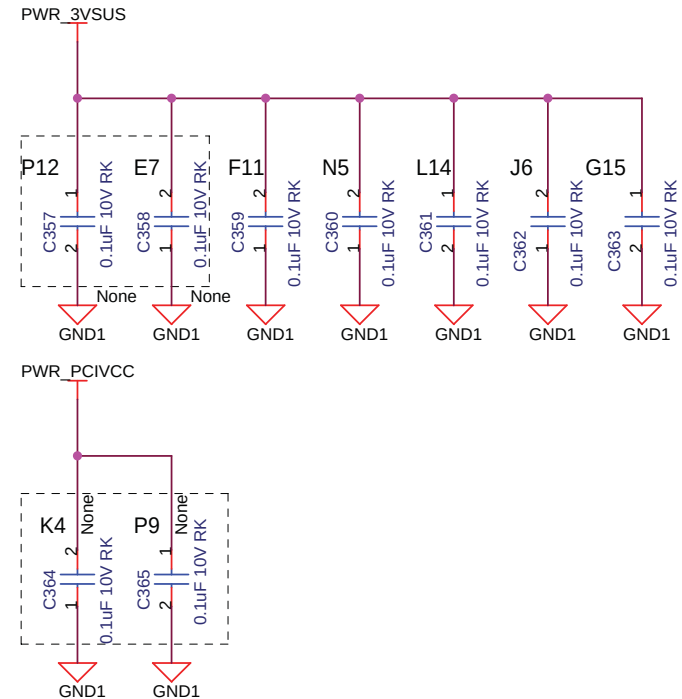
FINGER_CN

									TITLE
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									DRAW. No.
									C1CP302570-X2
									CAST
Rev.	Date	Design	Check	Appr.	Description				Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	56 / 93

FUJITSU LTD.



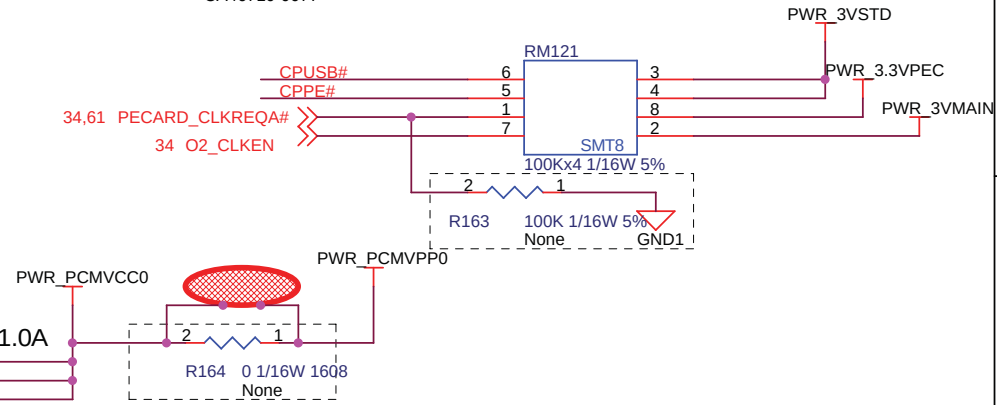
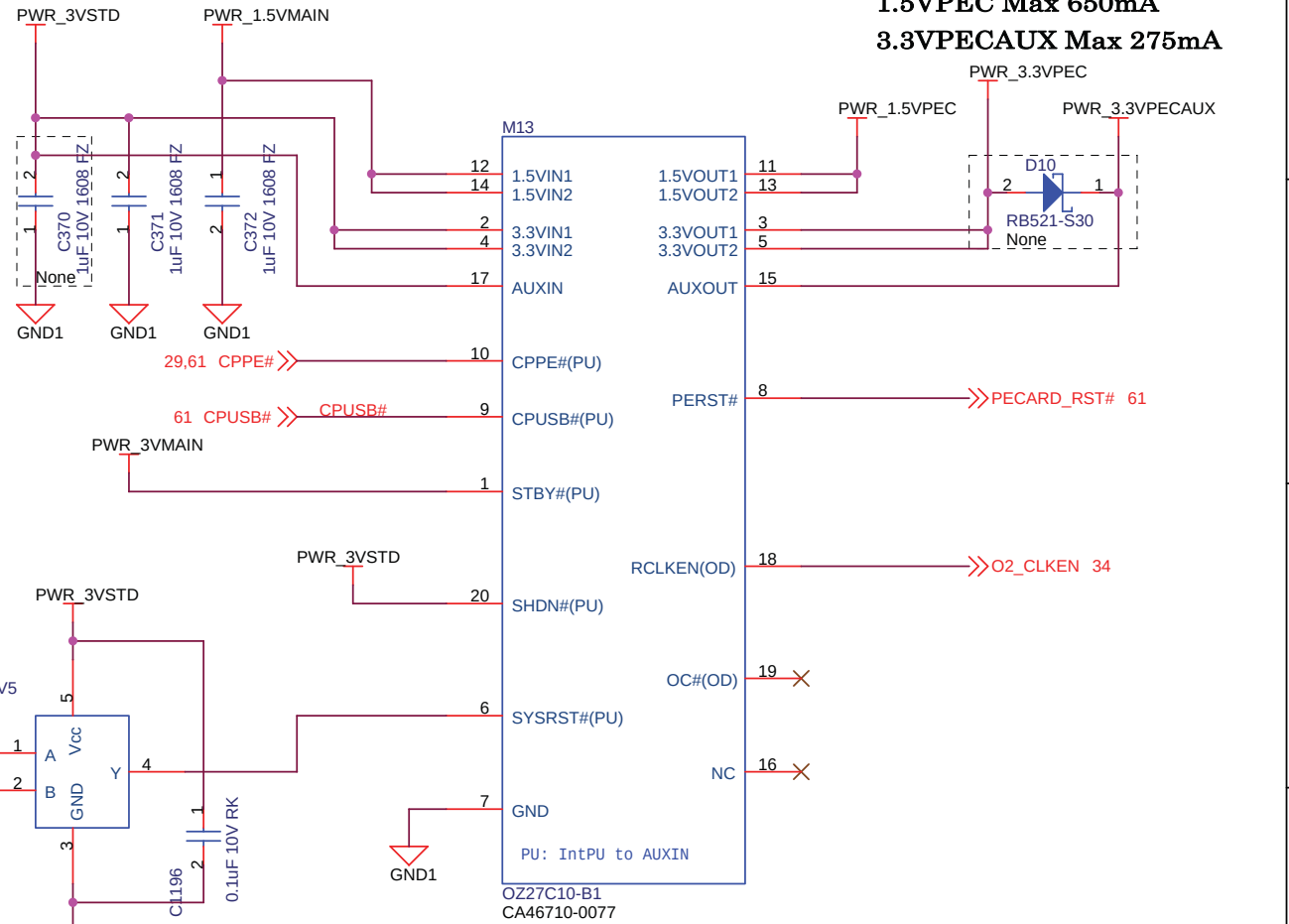
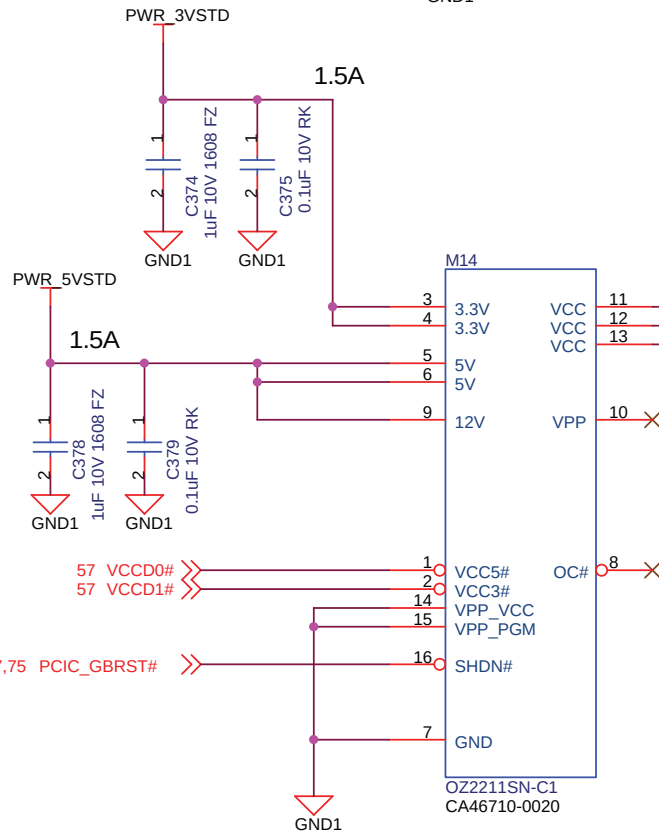
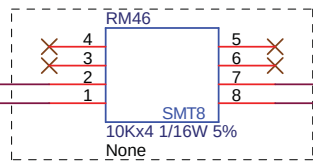
下記コンデンサは各電源PINの直近に配置すること。



PCIC-1

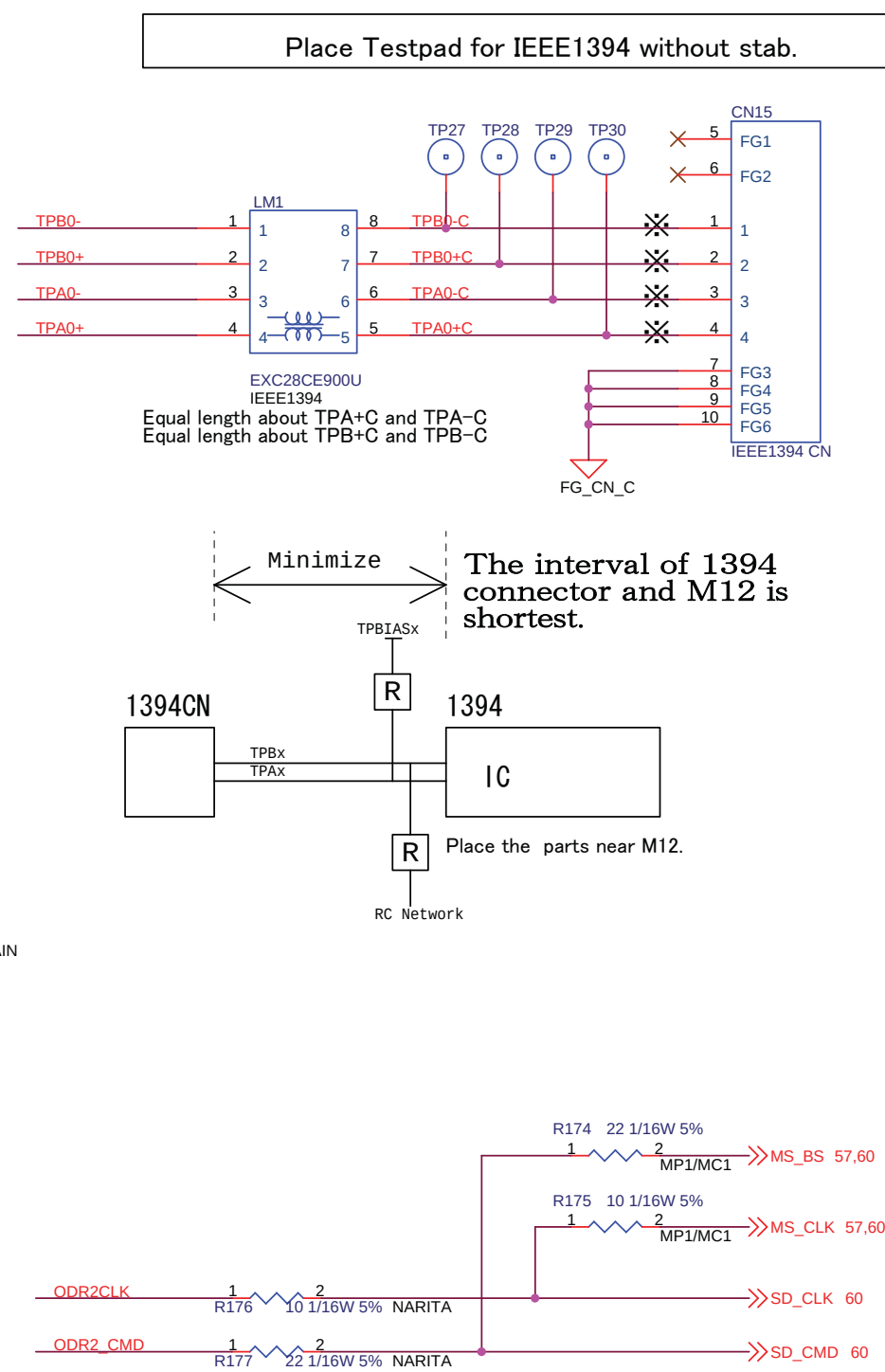
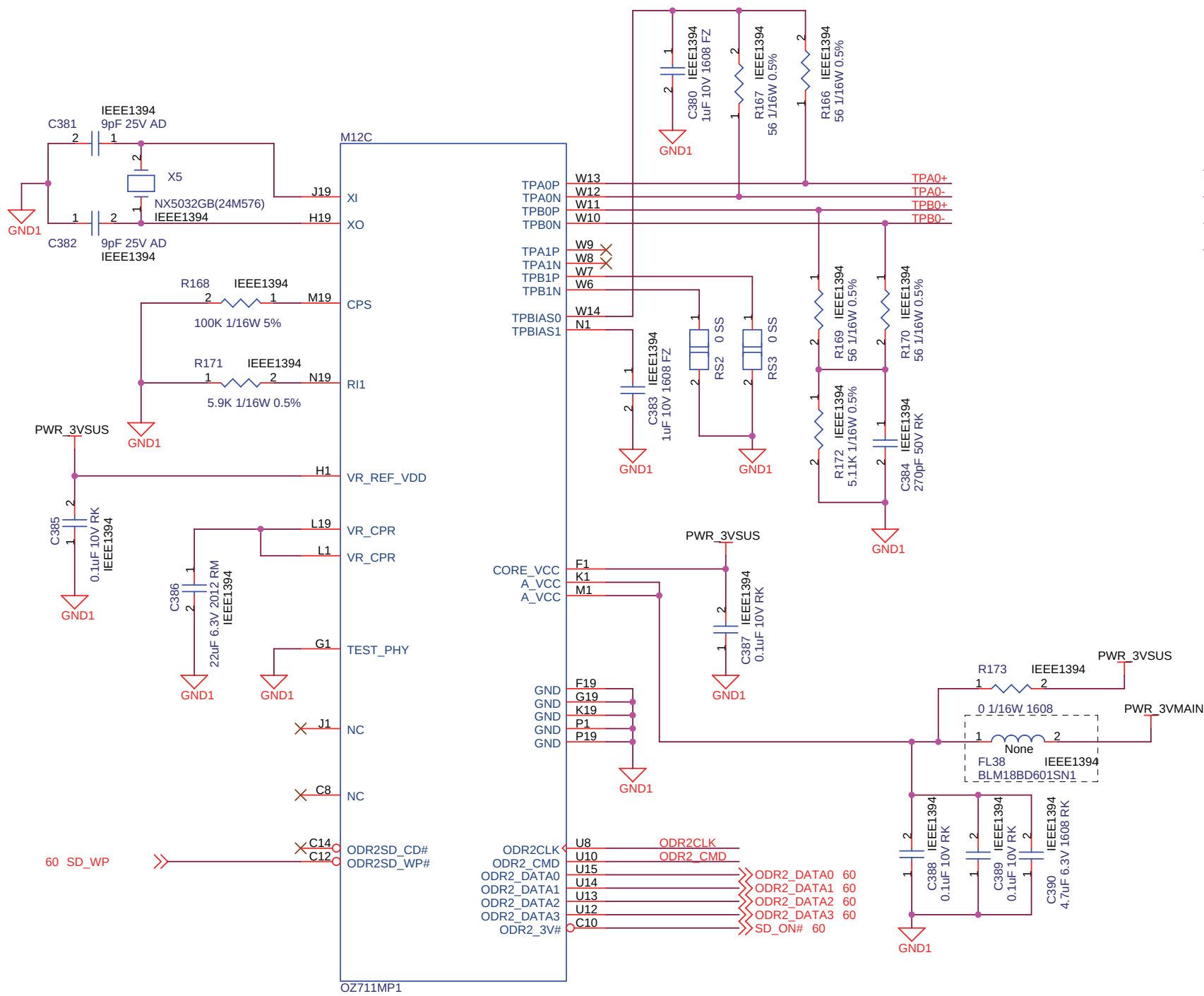
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						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		57 / 93		
						Fujitsu LTD.		

Place this clock dumping register near PCIC.



PCIC-2

									TITLE	
									VB313AA	
									DRAW. No.	
									C1CP302570-X2	
									CAST	
Rev.	Date	Design	Check	Appr.	Description					
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD.	
									Sheet 58 / 93	



IEEE1394 CN

						TITLE				
						VB313AA				
						DRAW. No.			CAST	
						C1CP302570-X2				
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			59 / 93

Dolphin

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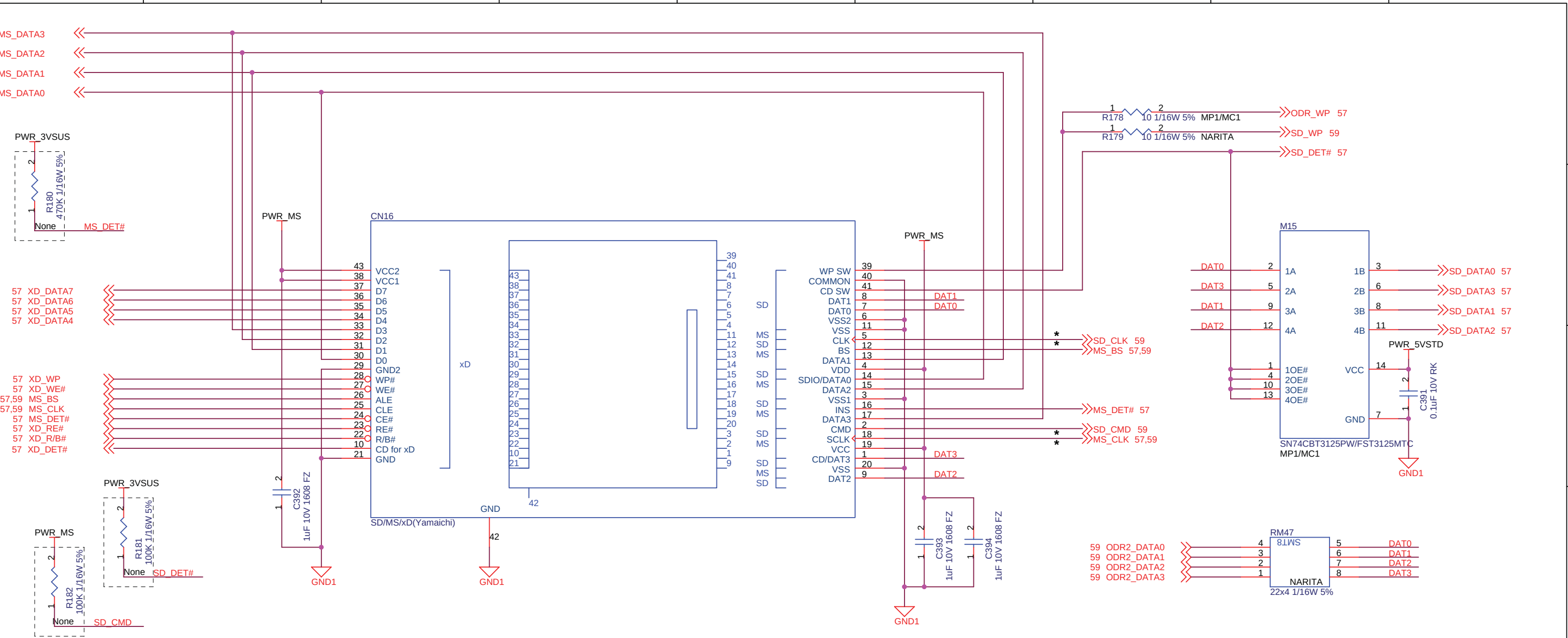
C

D

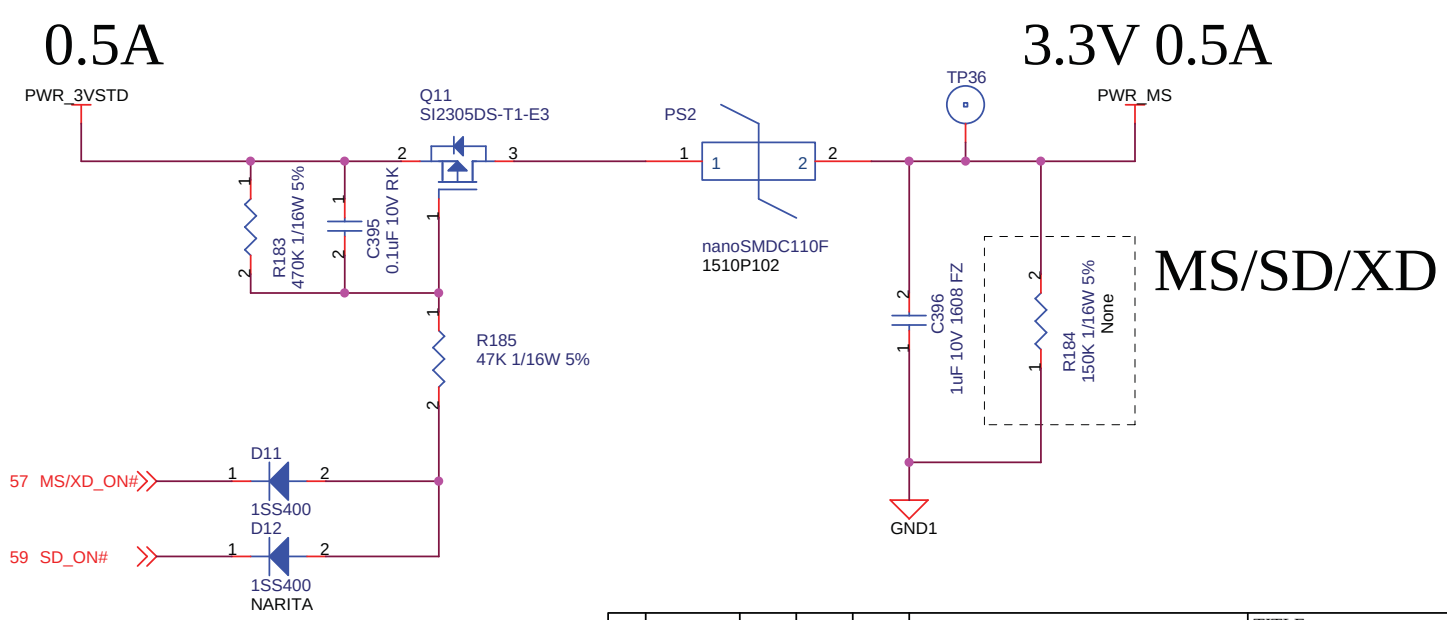
E

F

G

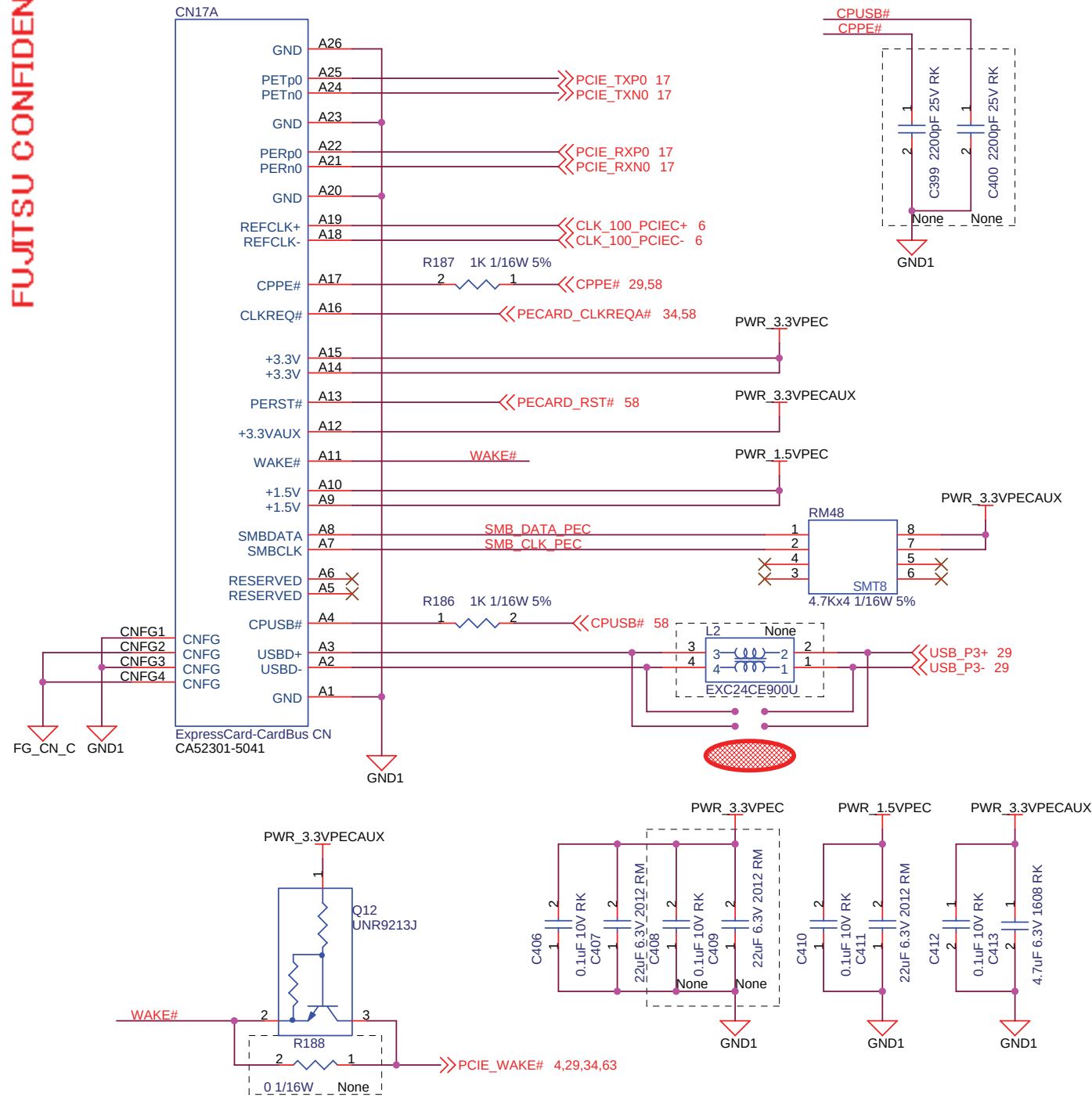


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Confidential



									TITLE VB313AA	
									DRAW. No.	
									CAST	
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD. Sheet 60 / 93	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		

SLOT #1

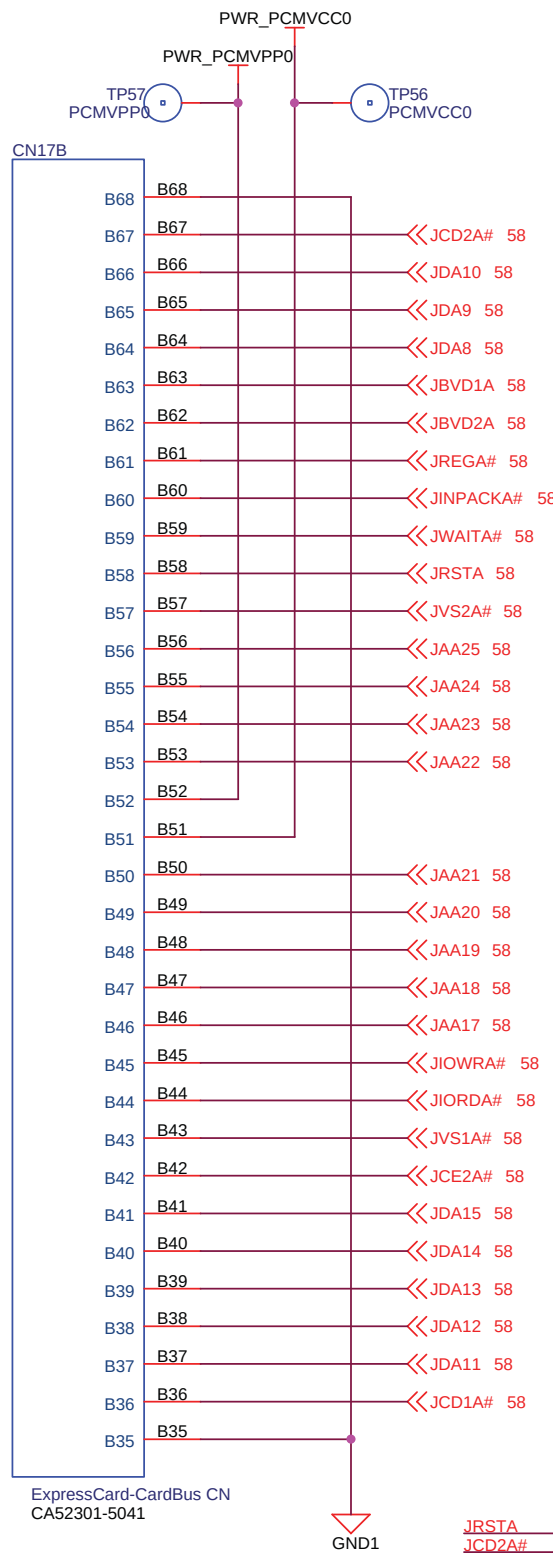


05/11
部品変更
Q12 : DTC144EE (CA47001-0312) -->
DTC144EETL (CA471005016)

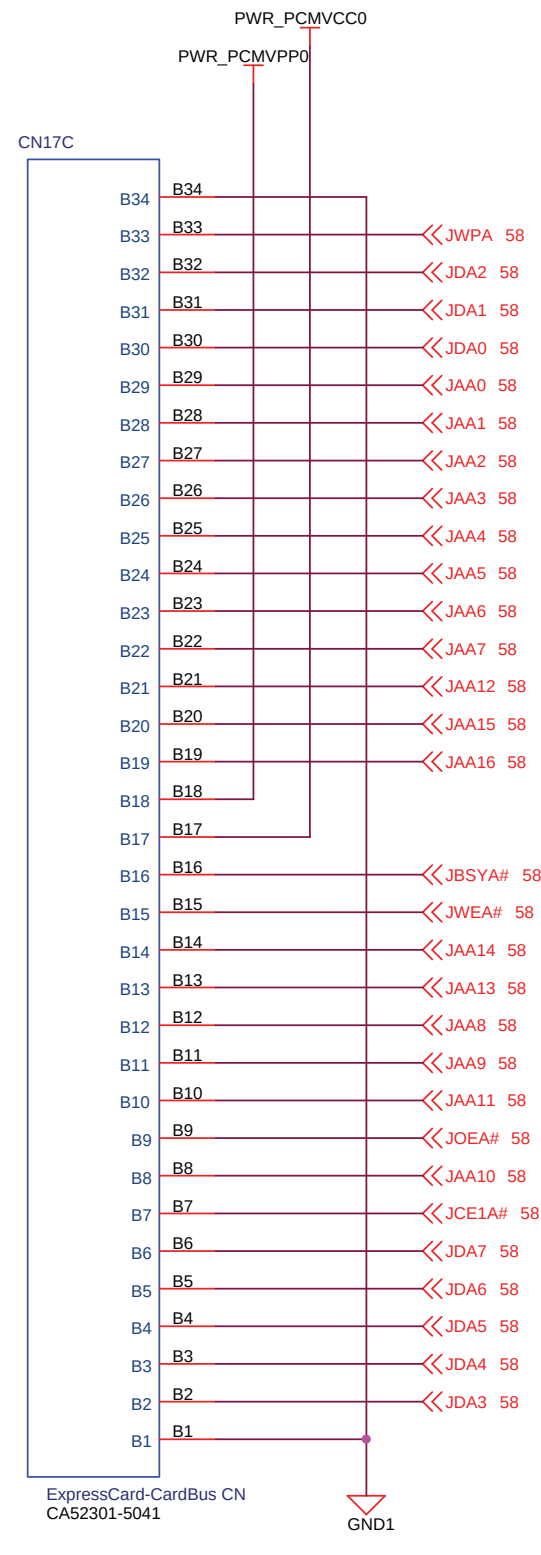
Fujitsu
Proprietary &
Confidential

Express Card SLOT
PCMCIA SLOT
PCB

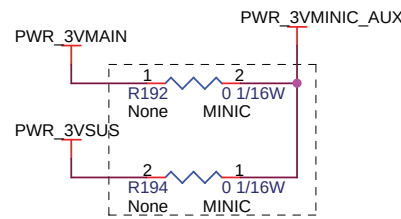
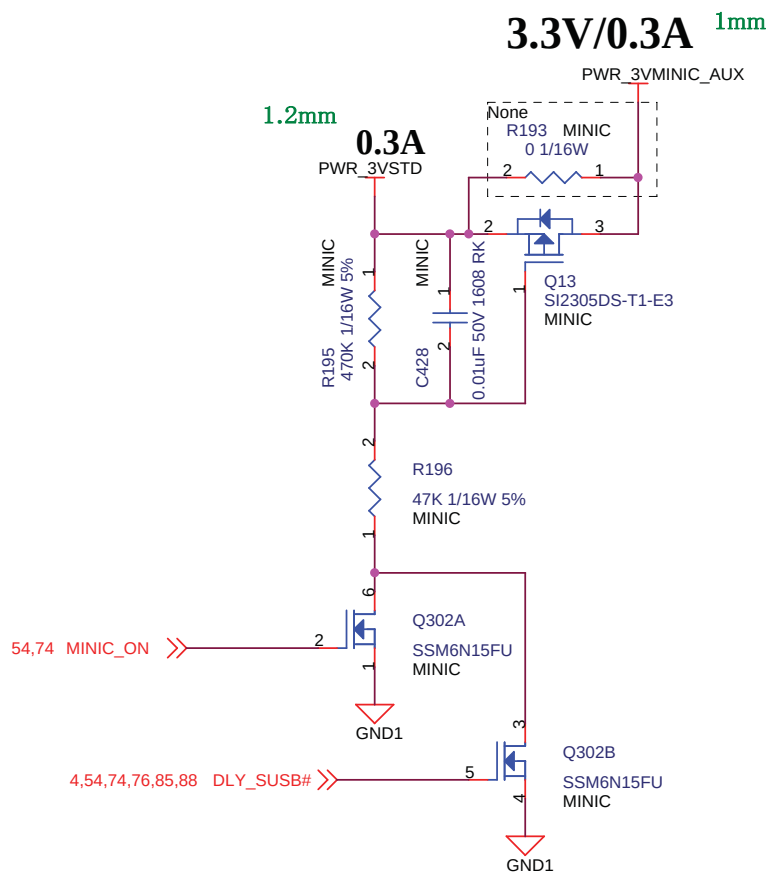
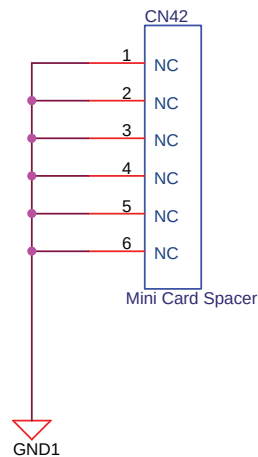
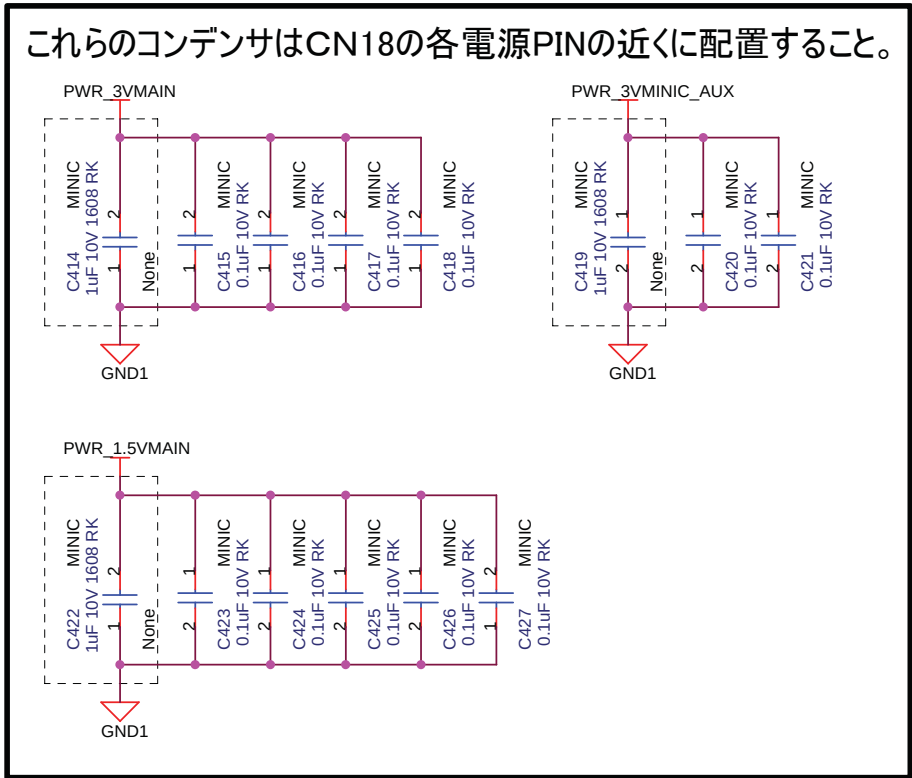
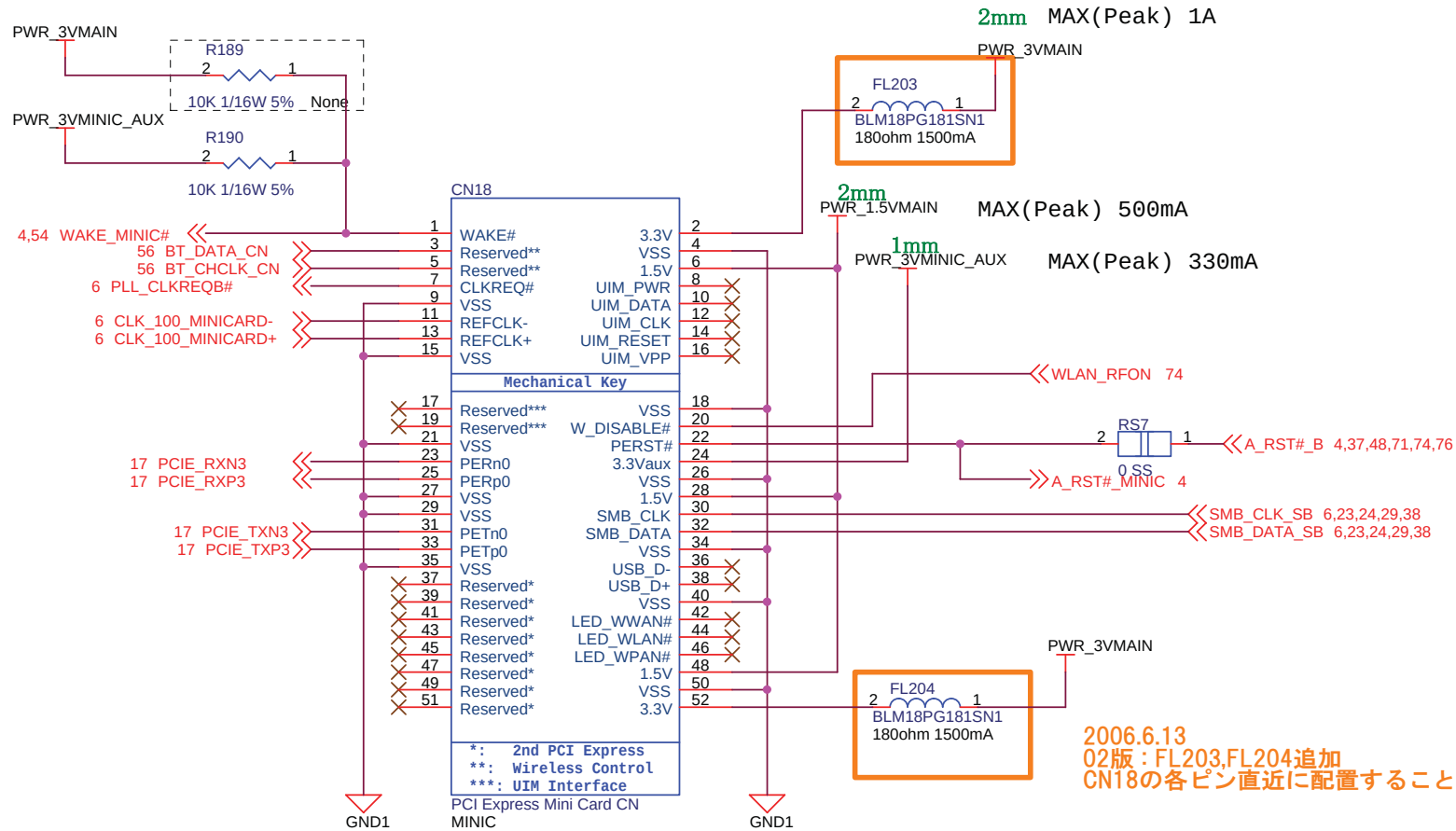
SLOT #0



PCMCIA SLOT

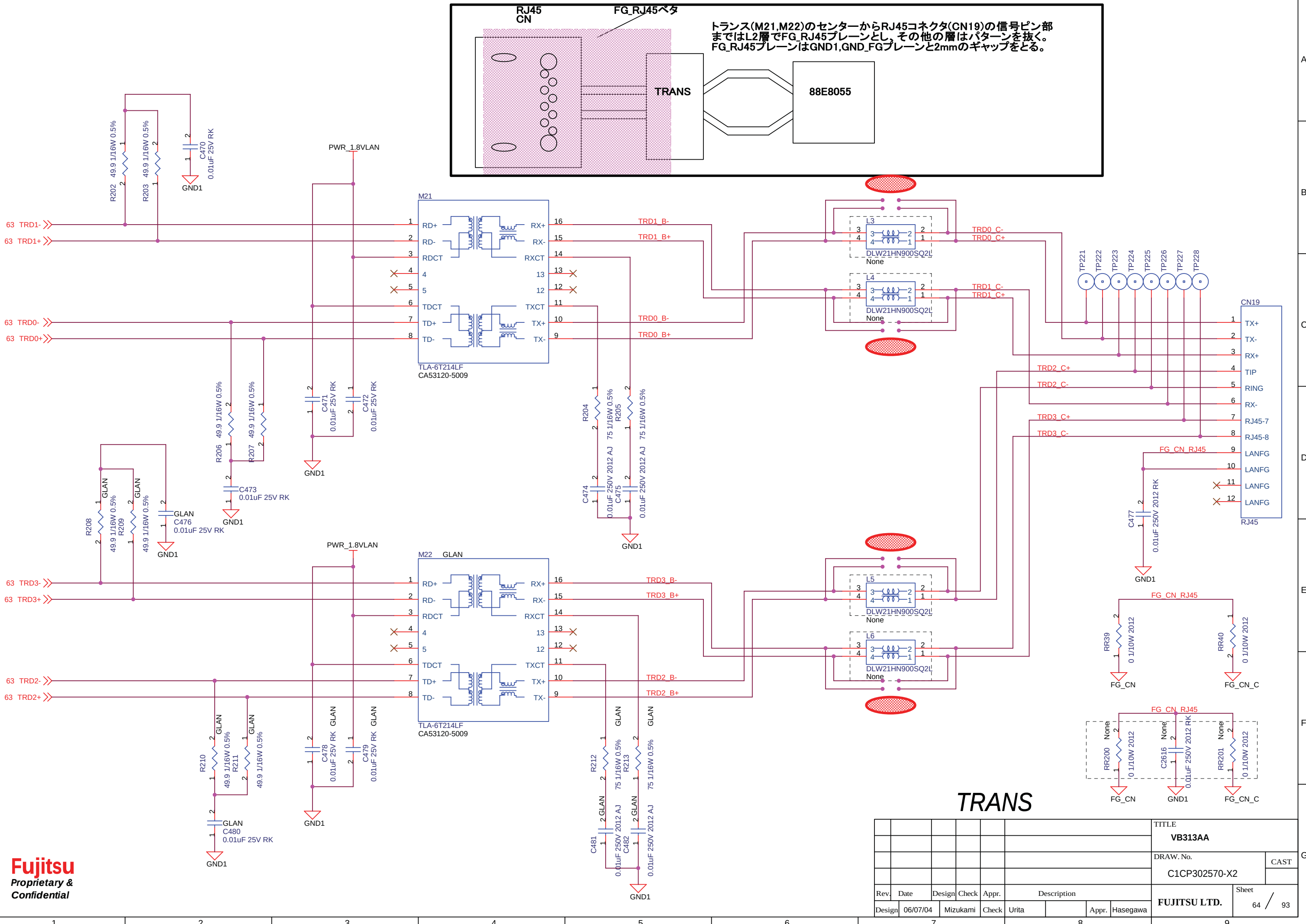


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							DRAW. No.		C1CP302570-X2
									CAST
Rev.	Date	Design	Check	Appr.	Description		Sheet		
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.		61 / 93



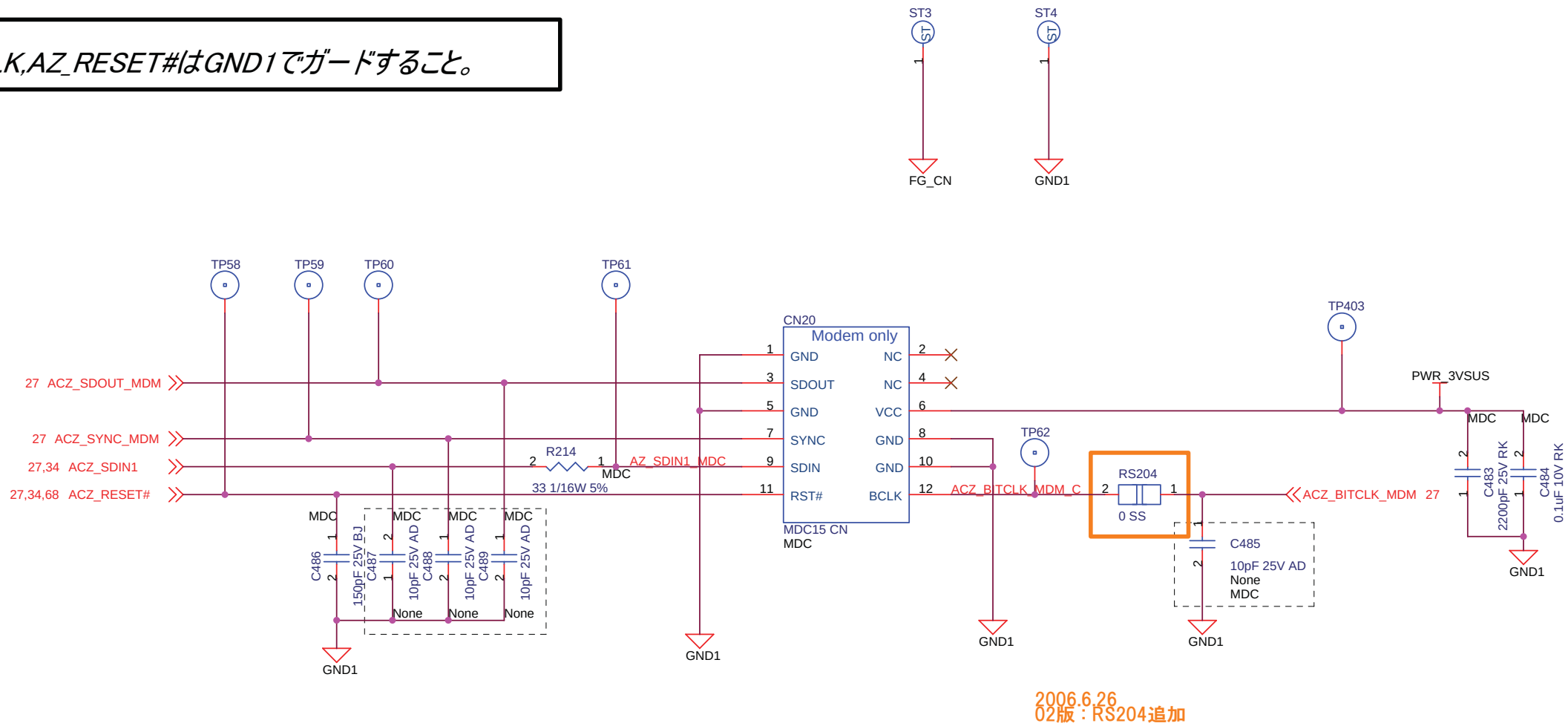
MiniCard CN

						TITLE		
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						DRAW. No.		CAST
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	62 / 93



									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	64 / 93		

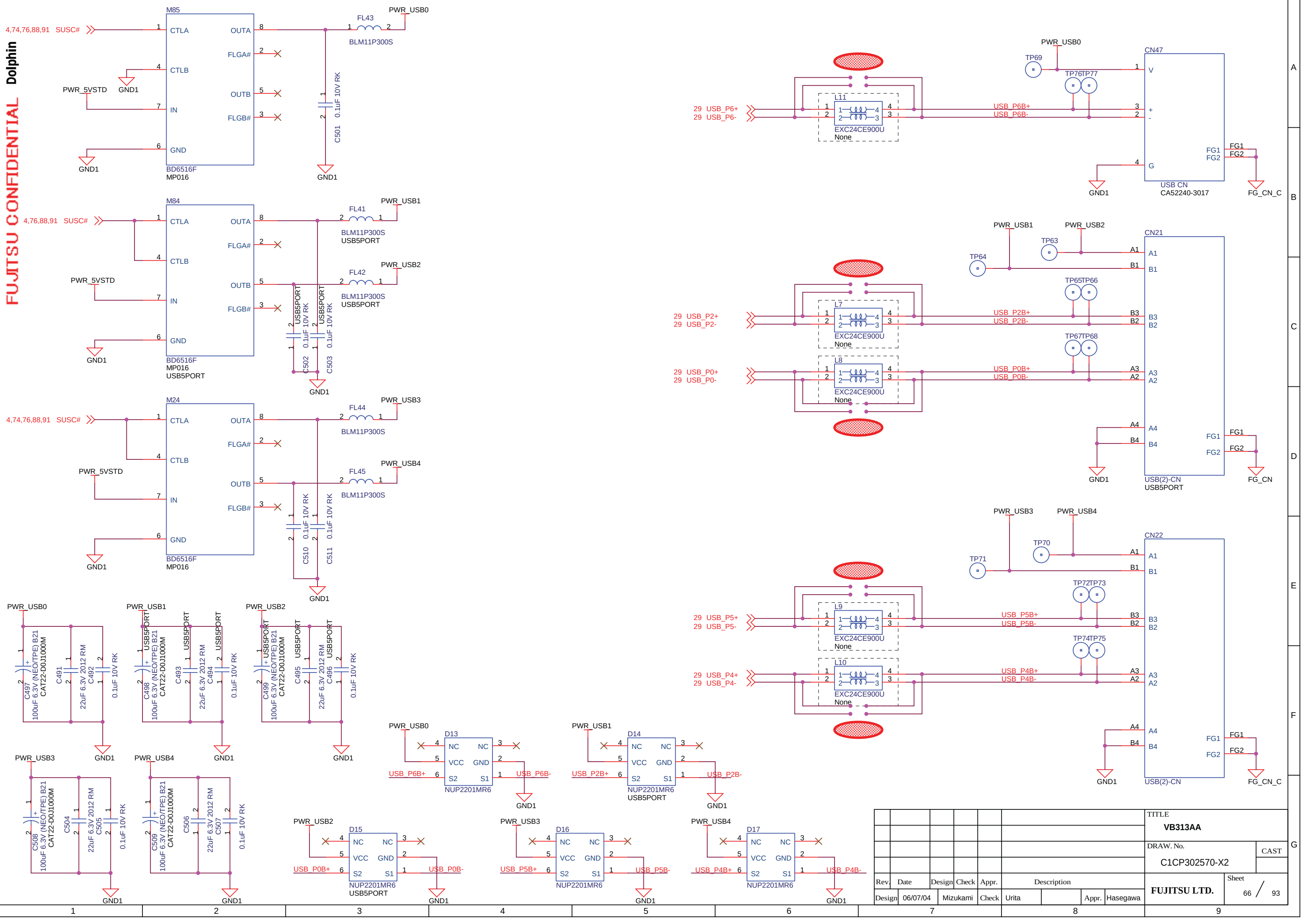
AZ_BITCLK,AZ_RESET#はGND1でガードすること。



MDC Modem

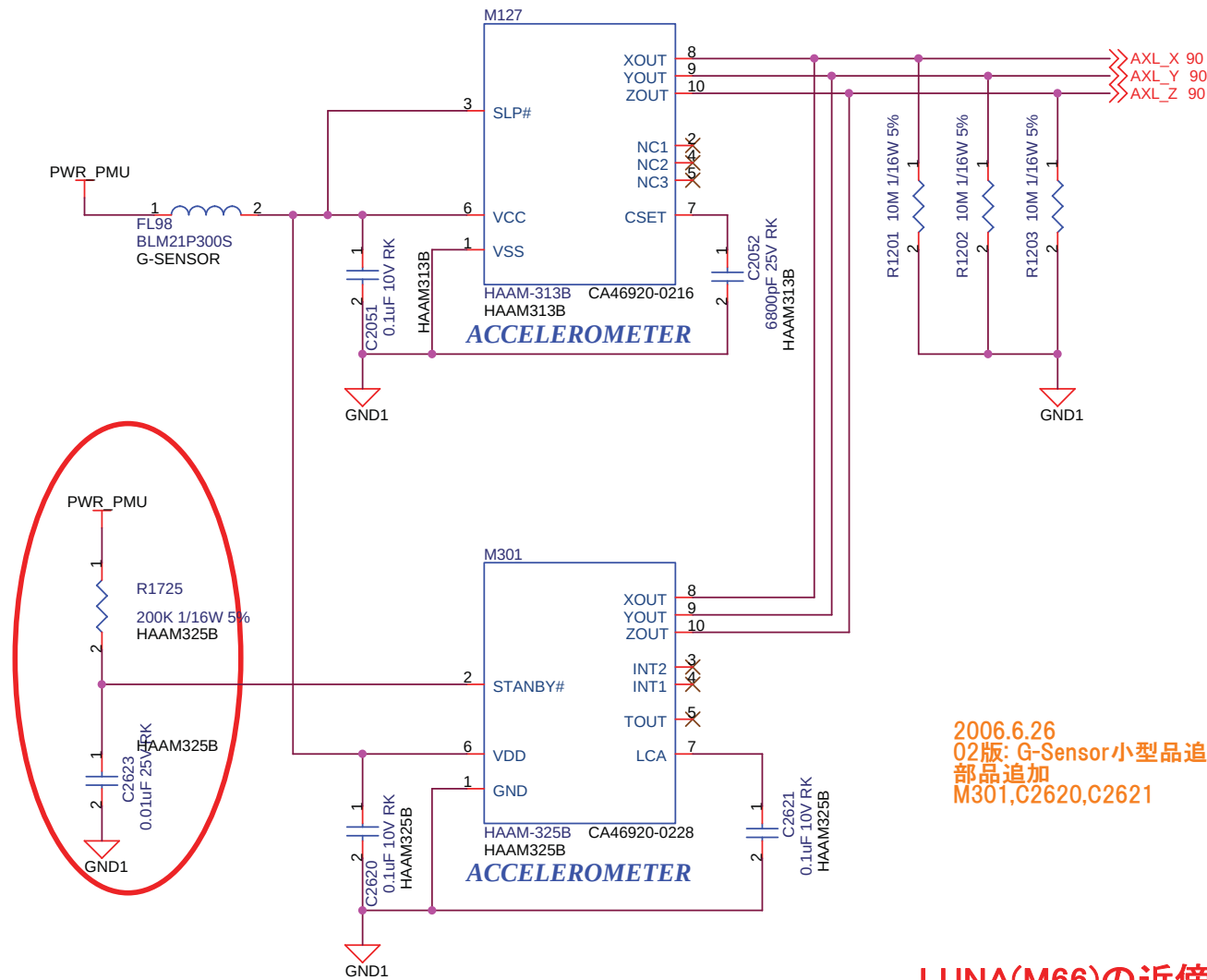


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						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		65 /	93
						FUJITSU LTD.	



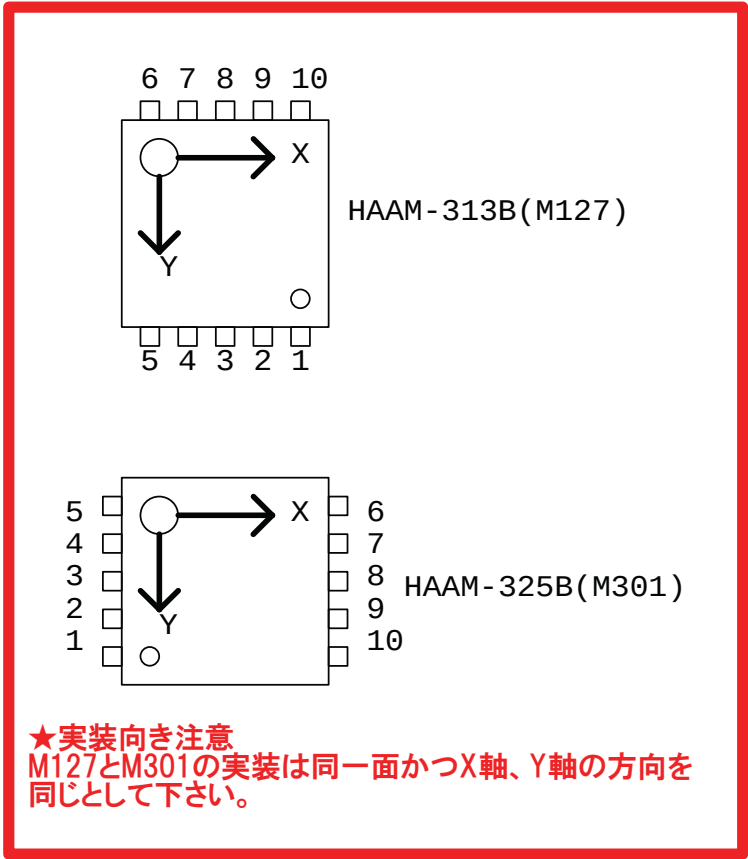
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						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		66 / 93		
						Fujitsu Ltd.		

2006.7.4
02版: R1725、C2623追加

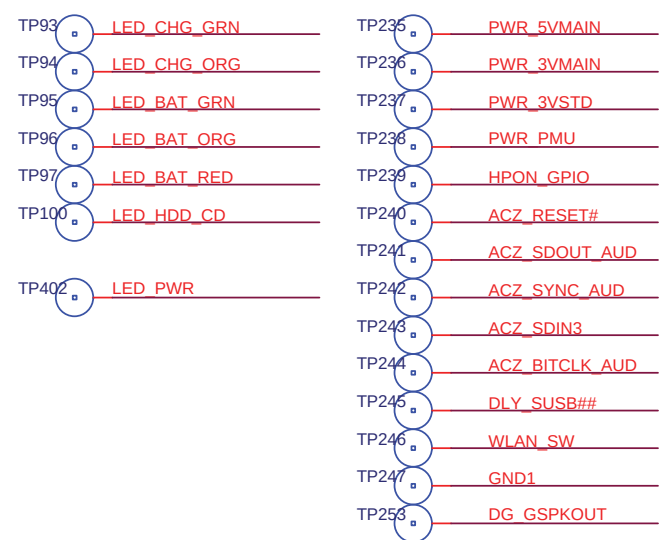
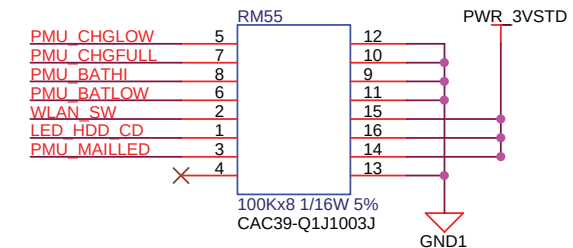
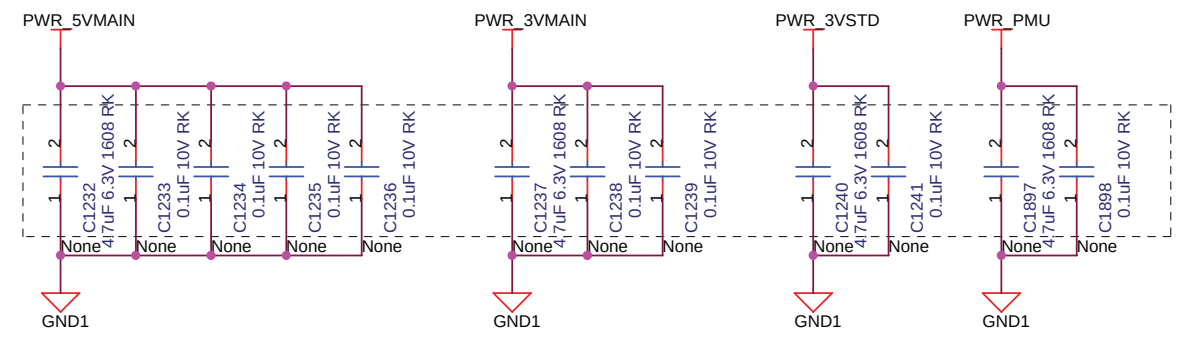
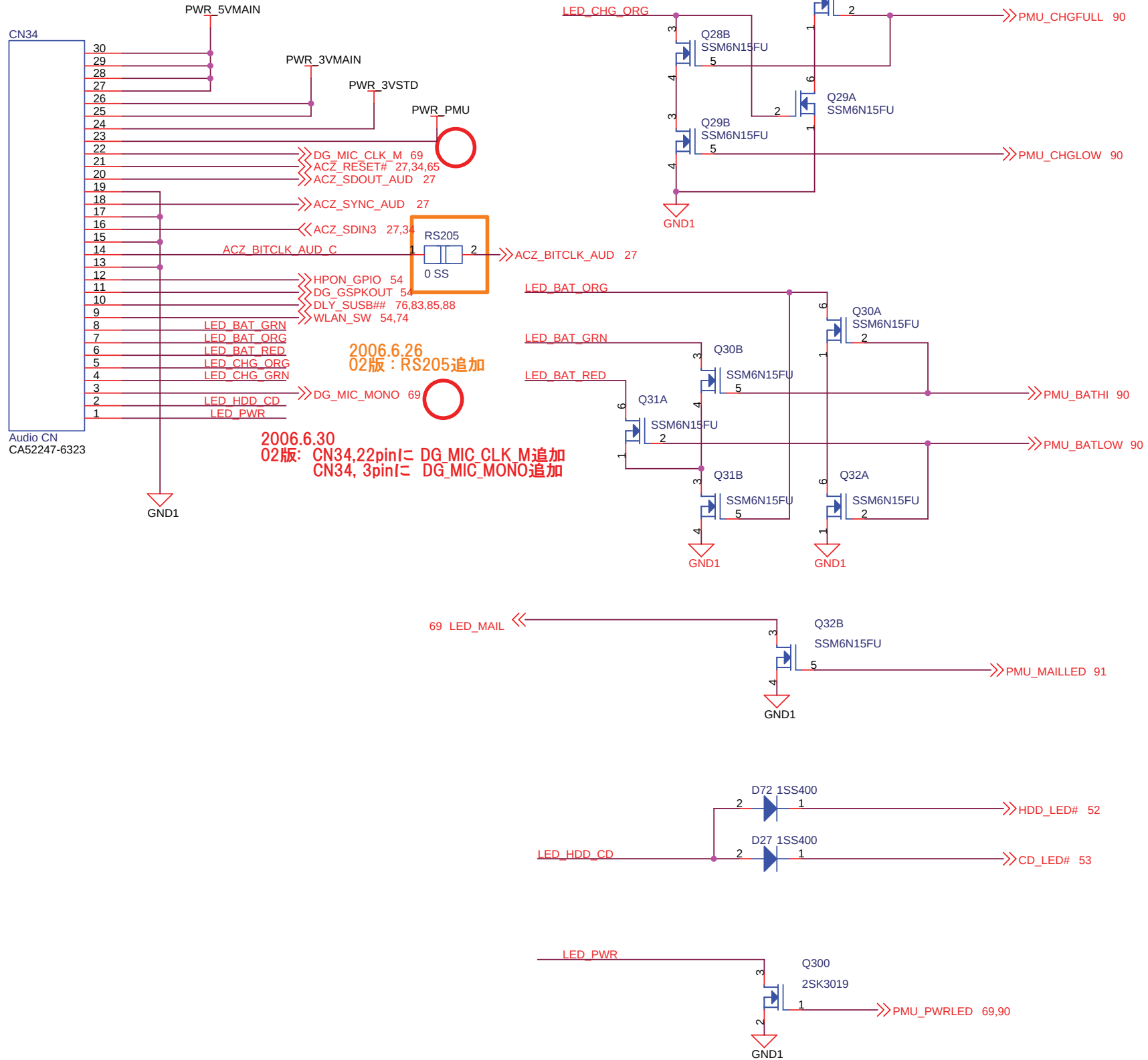


2006.6.26
02版: G-Sensor小型品追加
部品追加
M301,C2620,C2621

LUNA(M66)の近傍に配置

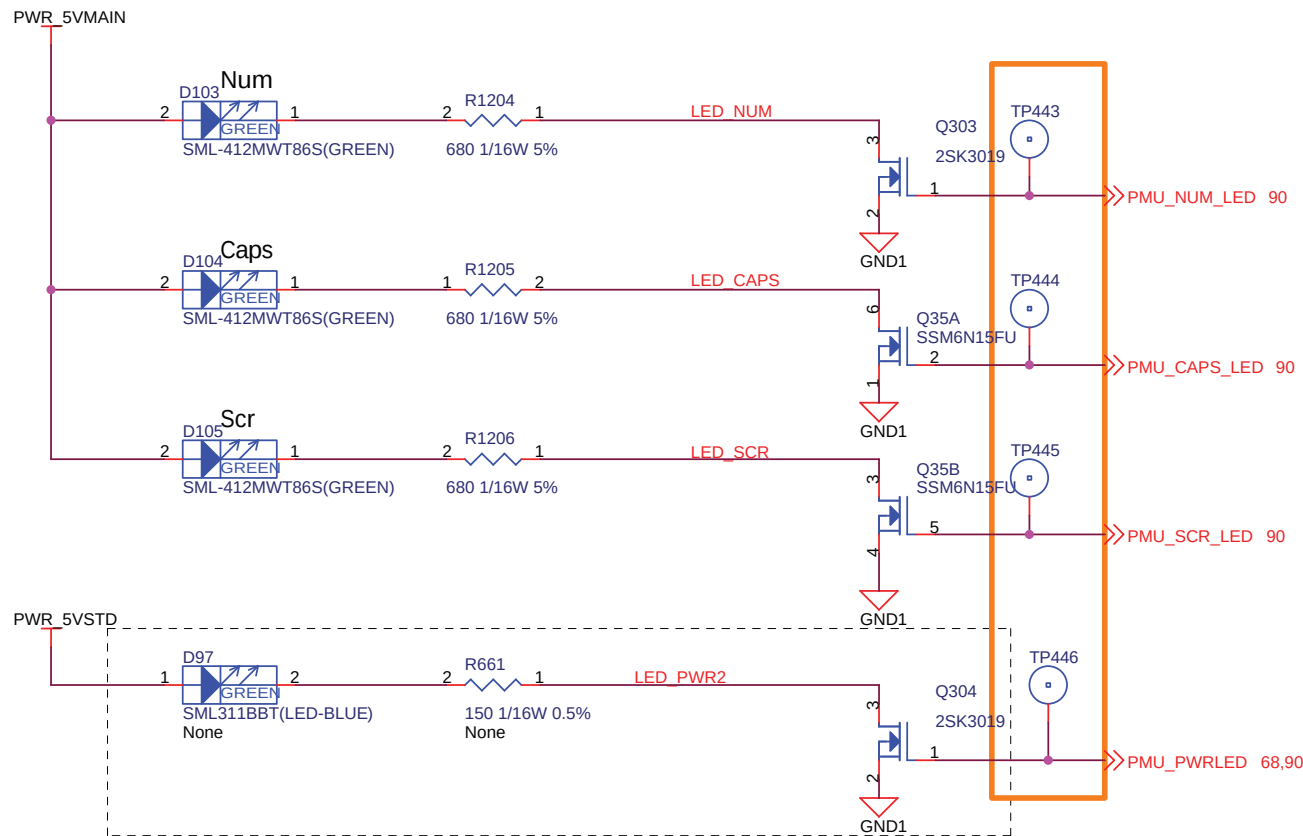


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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	67 / 93

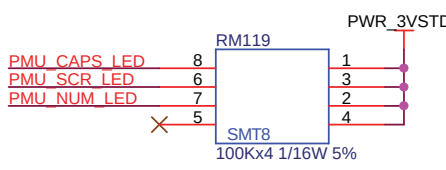


Audio/Statsu CN

						TITLE		
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						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	68 / 93



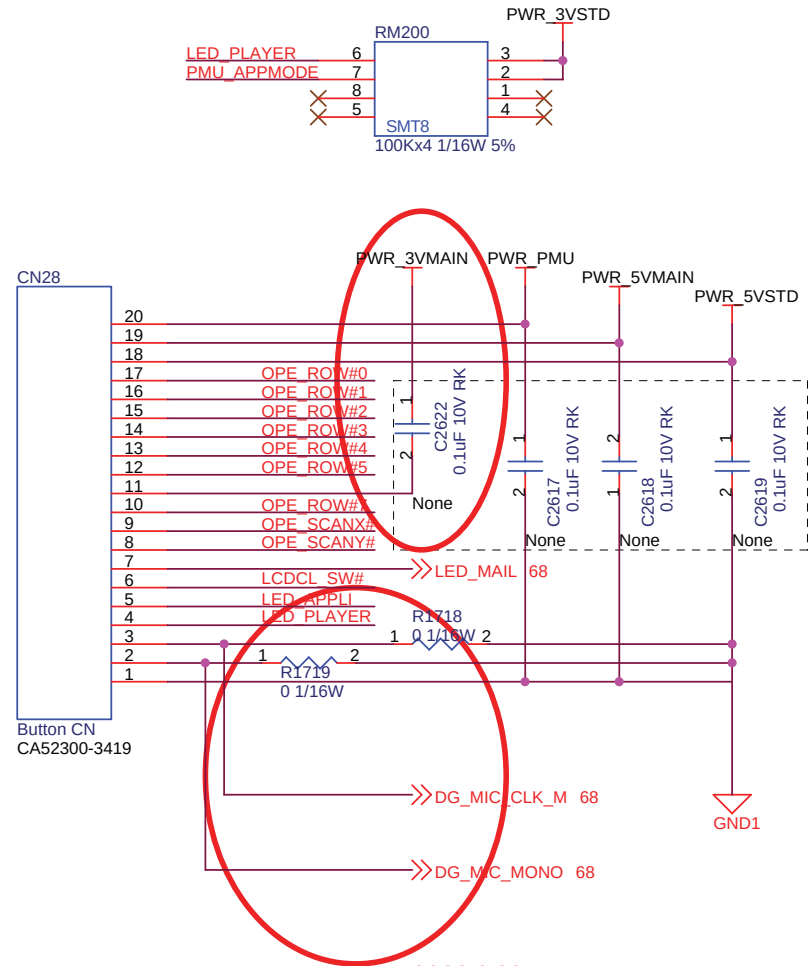
2006.6.26
02版:
LEDにTP追加。TP443,TP444,TP445,TP446
(Fennecと配置の共通化をお願い致します)



2006.6.26
02版: 電源ボタンにTP追加
(Fennecと配置の共通化をお願い致します)

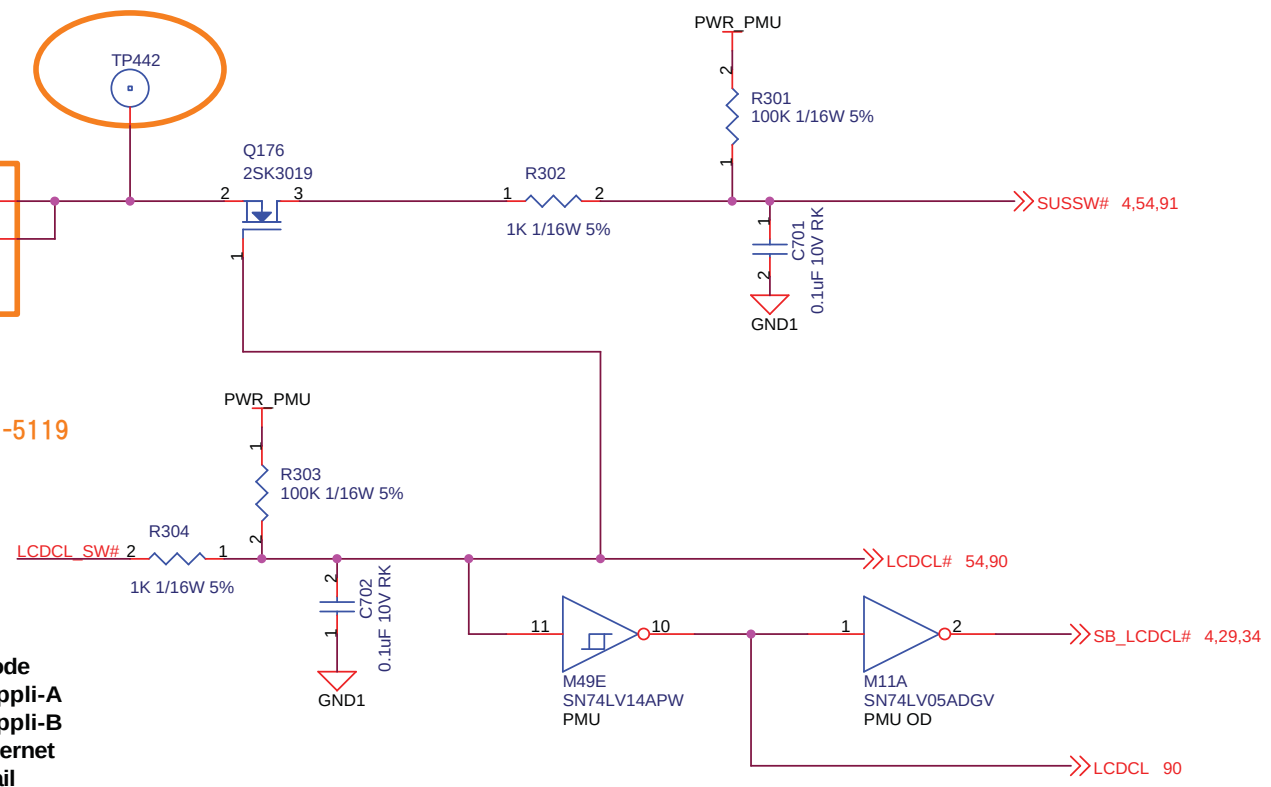
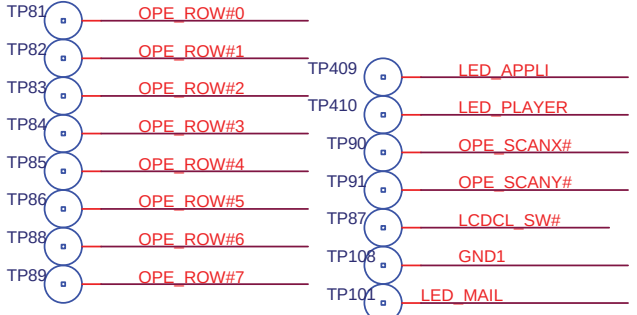
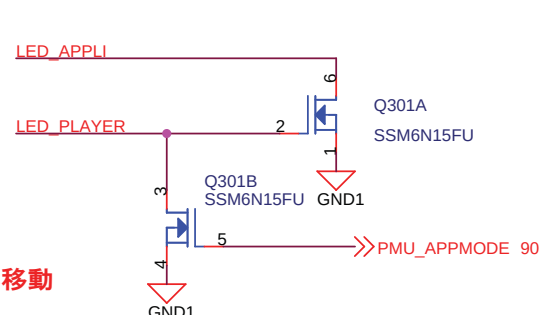
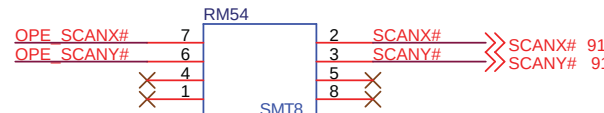
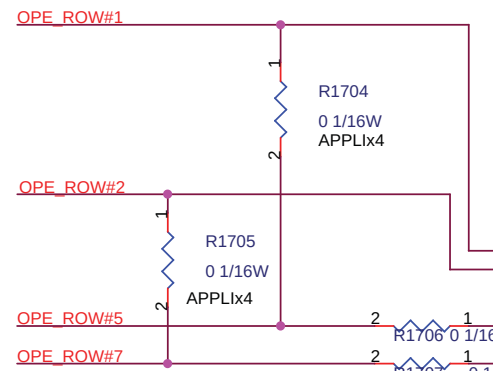
2006.6.26
02版: 電源ボタン変更
CA49001-5370 --> CA49001-5119

- ROW#0 SW_Mode
- ROW#1 SW_Appli-A
- ROW#2 SW_Appli-B
- ROW#3 SW_Internet
- ROW#4 SW_Mail
- ROW#5 SW_Vol_Down
- ROW#6 Unused
- ROW#7 SW_Vol_up



2006.6.30
02版: R1718-1721,C2622追加

2006.7.04
R1720,R1721をMainボードからAudioボードへ移動



[Button CN]

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
						FUJITSU LTD.		Sheet
Rev.	Date	Design	Check	Appr.	Description			69 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

Dolphin

FUJITSU CONFIDENTIAL

C

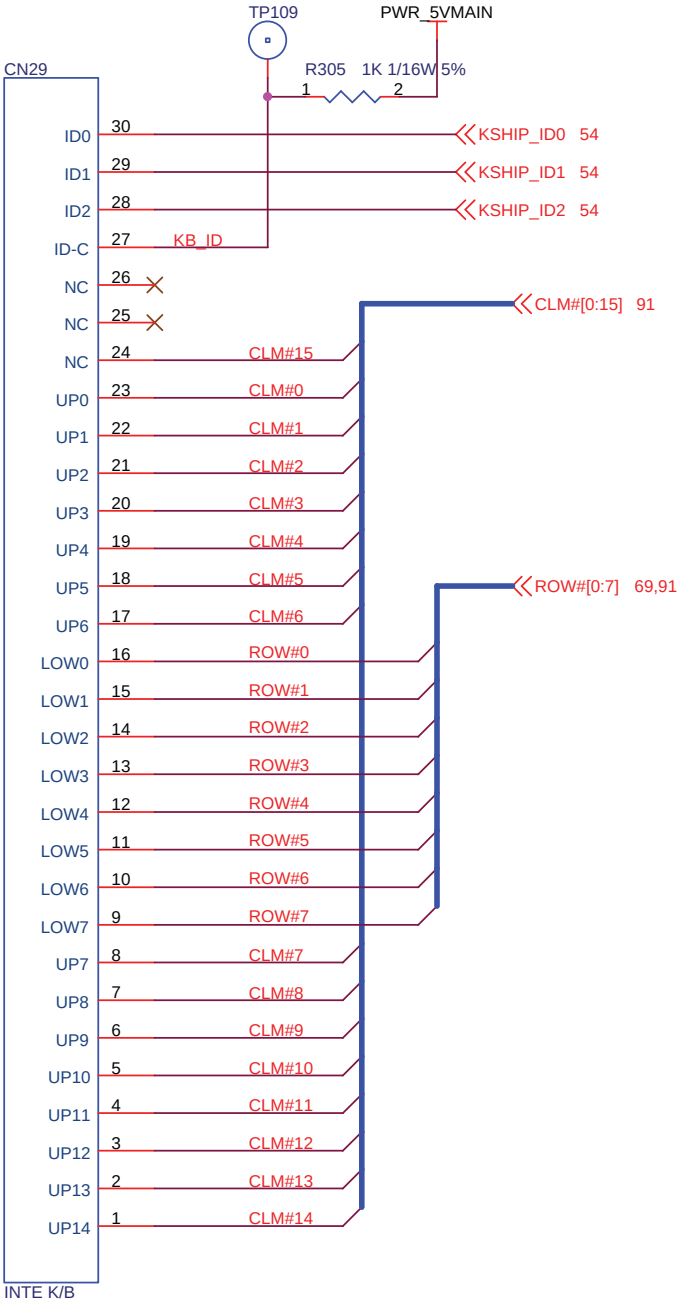
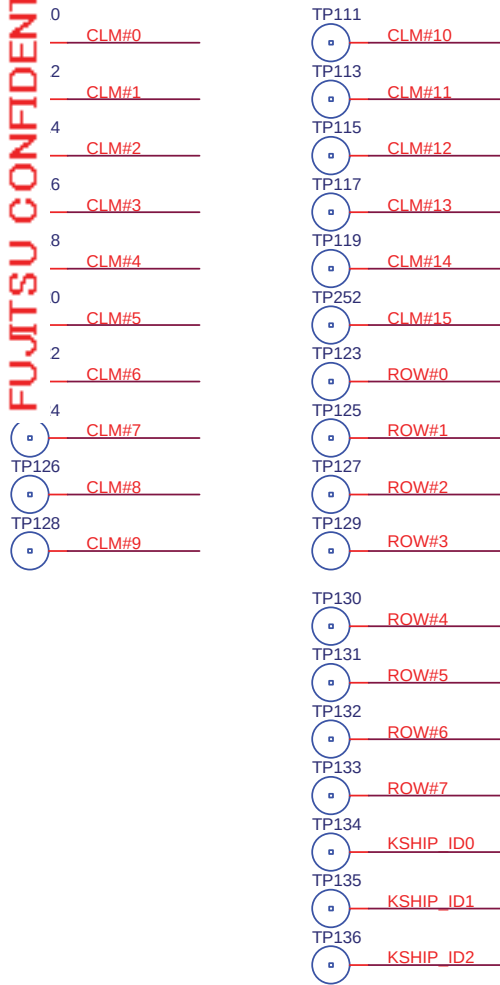
D

E

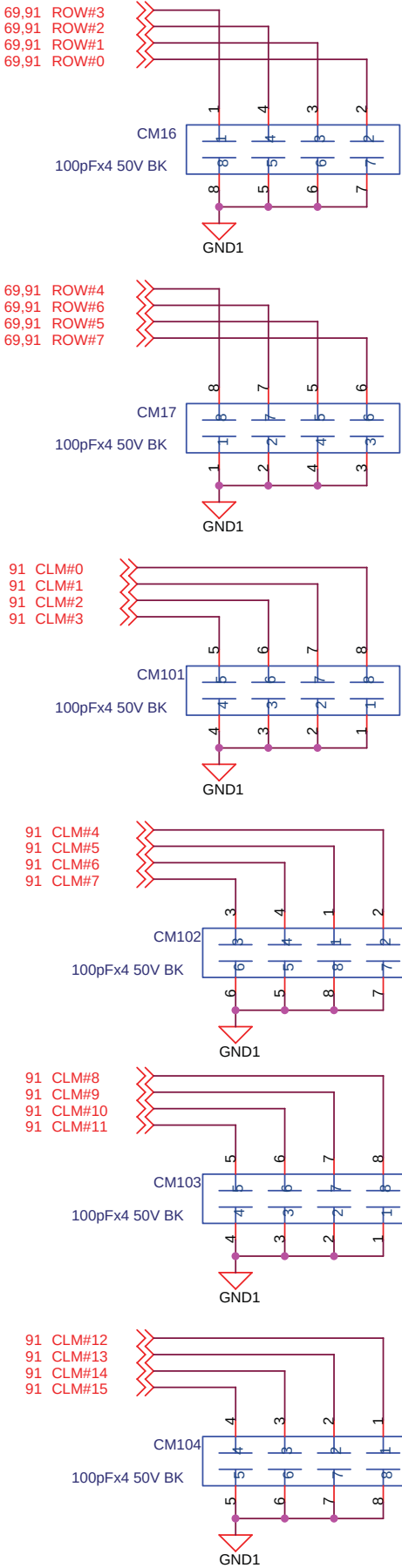
F

G

Fujitsu
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Confidential

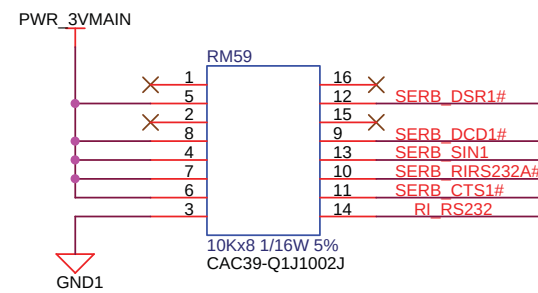
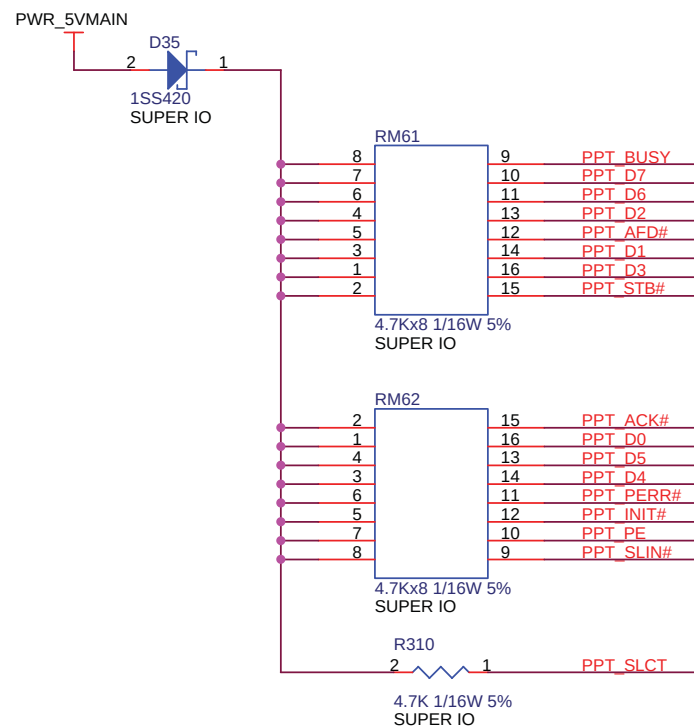
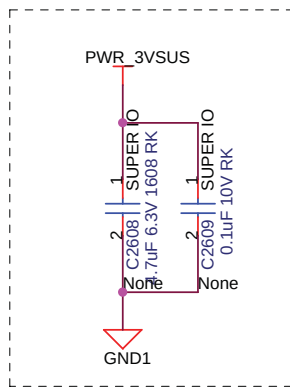
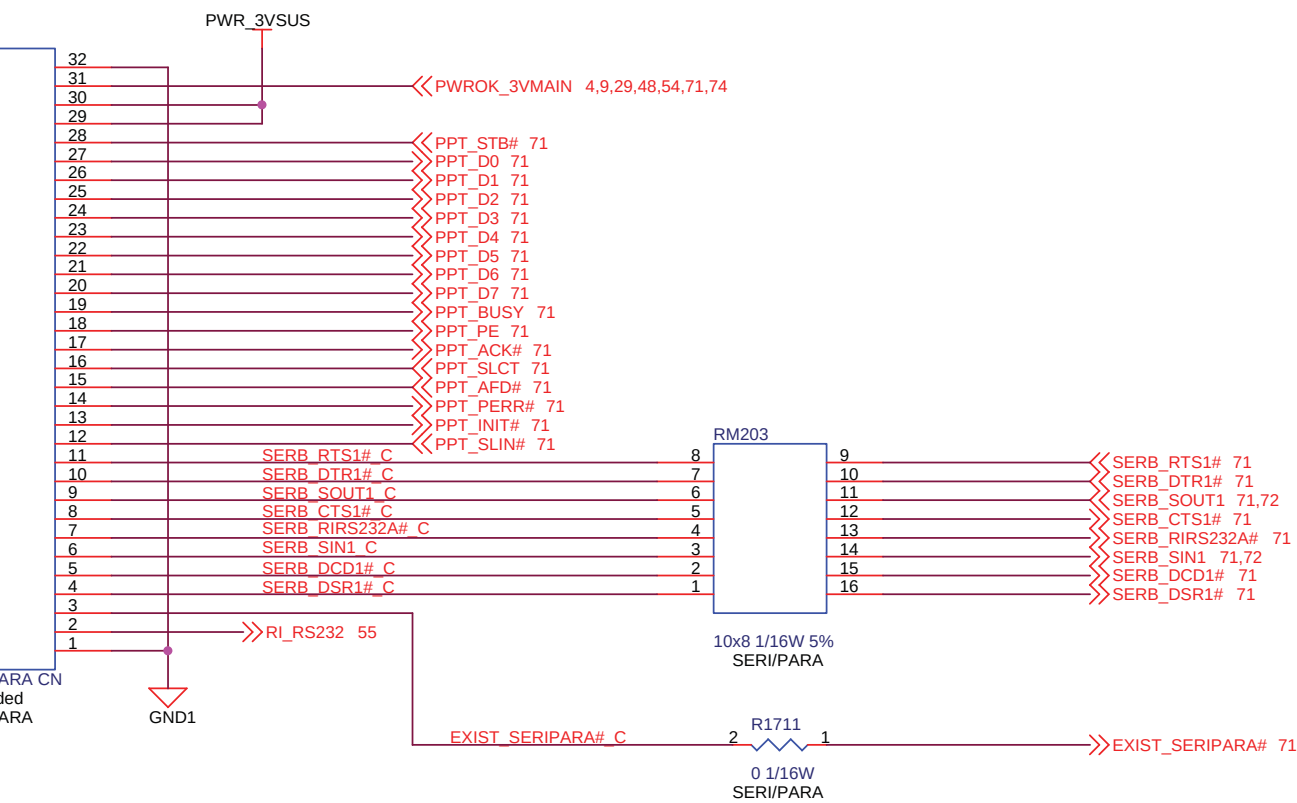
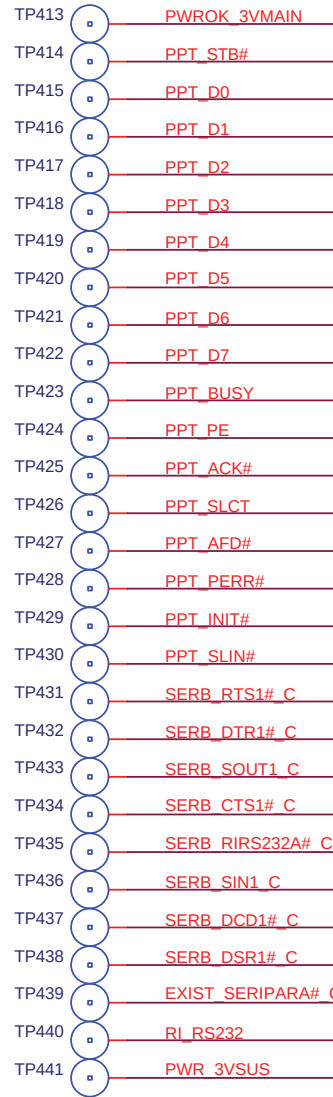


	SHIPID		
	ID0	ID1	ID2
OYA	0	0	0
UK	0	0	1
US	0	1	0
JP	0	1	1



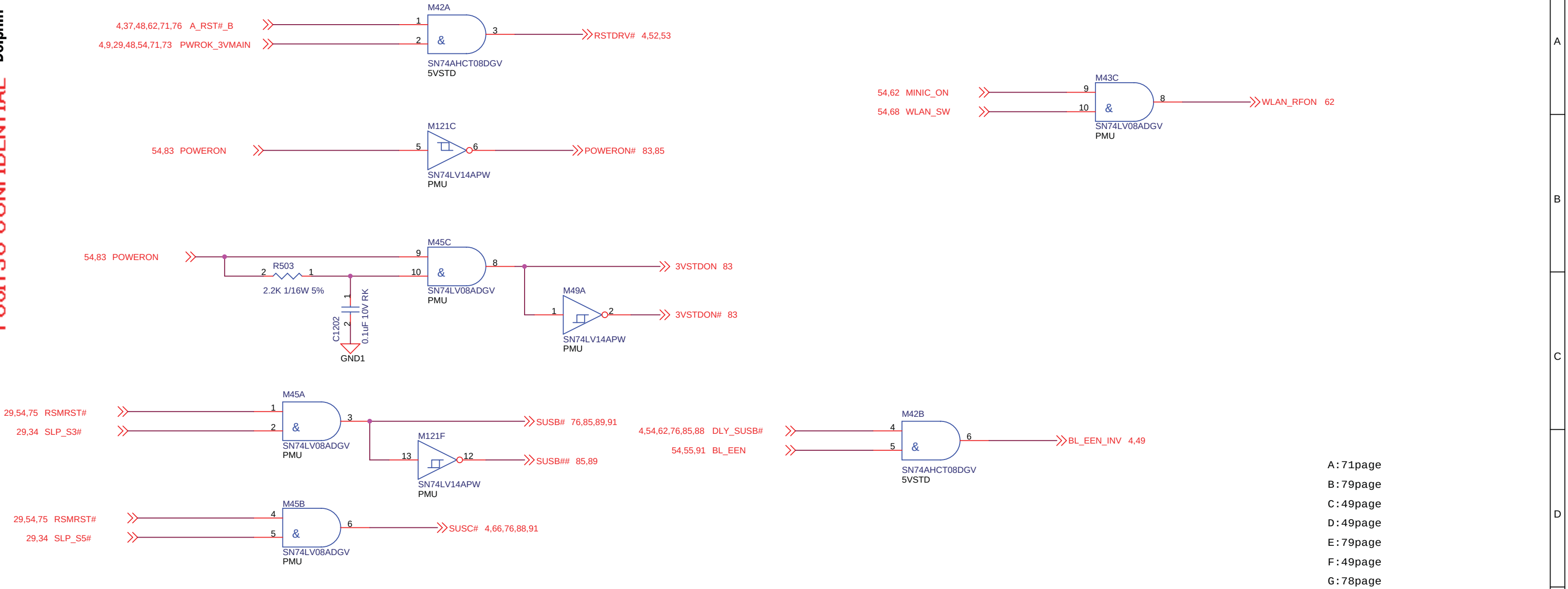
KB/Pointing-CN

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								DRAW. No.	CAST
								C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		70 / 93

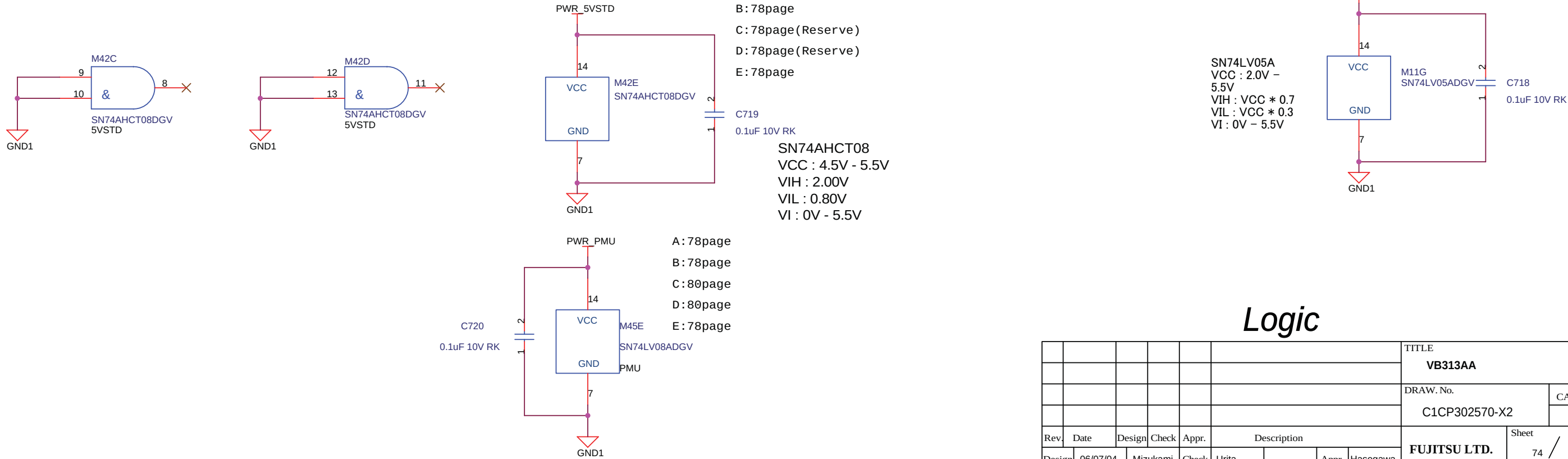


PARALLEL/SERIAL CN

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									DRAW. No.	
									C1CP302570-X2	
									CAST	
Rev.	Date	Design	Check	Appr.	Description				Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD. 73 / 93	



SLP_S3, SLP_S5#に3VSTDでPull-Upがあるためマスク回路追加



A: 71page
B: 79page
C: 49page
D: 49page
E: 79page
F: 49page
G: 78page

A: 78page
B: 78page
C: 78page(Reserve)
D: 78page(Reserve)
E: 78page

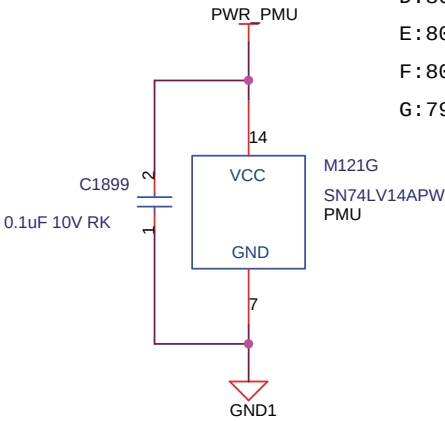
A: 78page
B: 78page
C: 80page
D: 80page
E: 78page

Logic

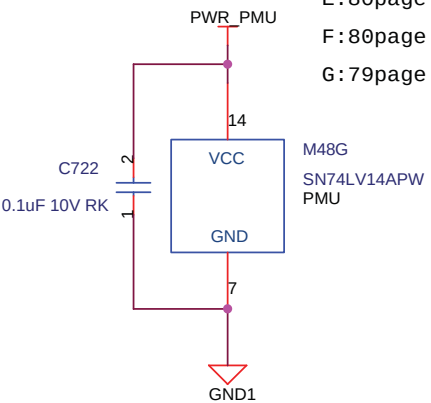
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						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 74 / 93

PWR_3VSUS to BENN_SUSOK
Default 50ms

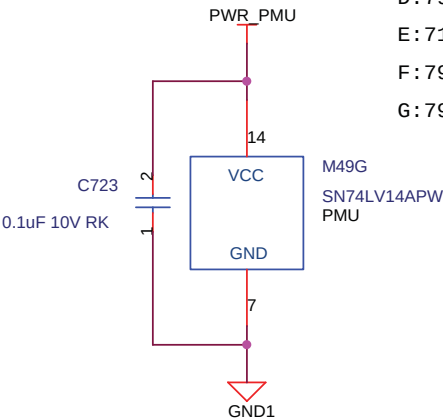
PWR_3VMAIN to BENN_MAINOK
Default 170ms



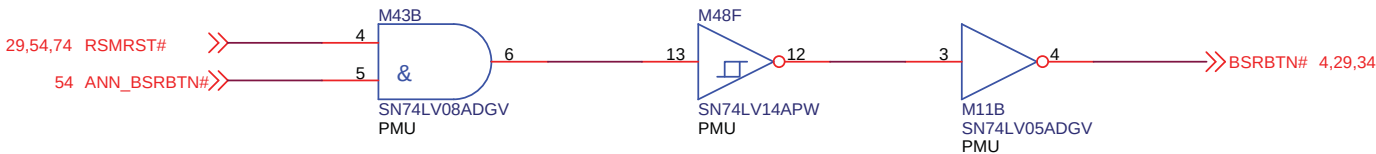
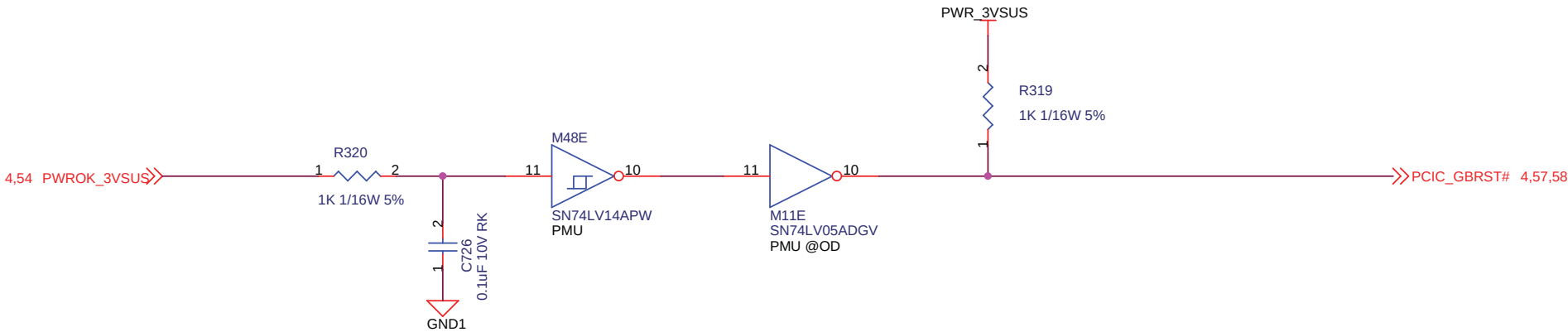
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C: 80page
D: 80page
E: 80page
F: 80page
G: 79page



A: 80page
B: 80page
C: 80page
D: 80page
E: 80page
F: 80page
G: 79page



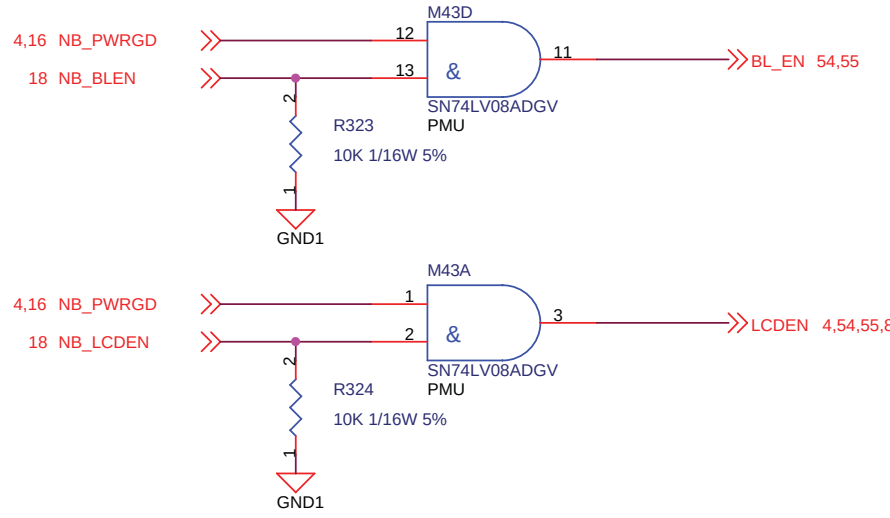
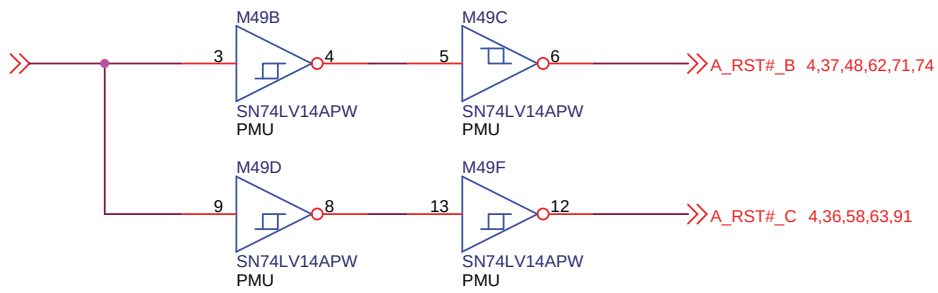
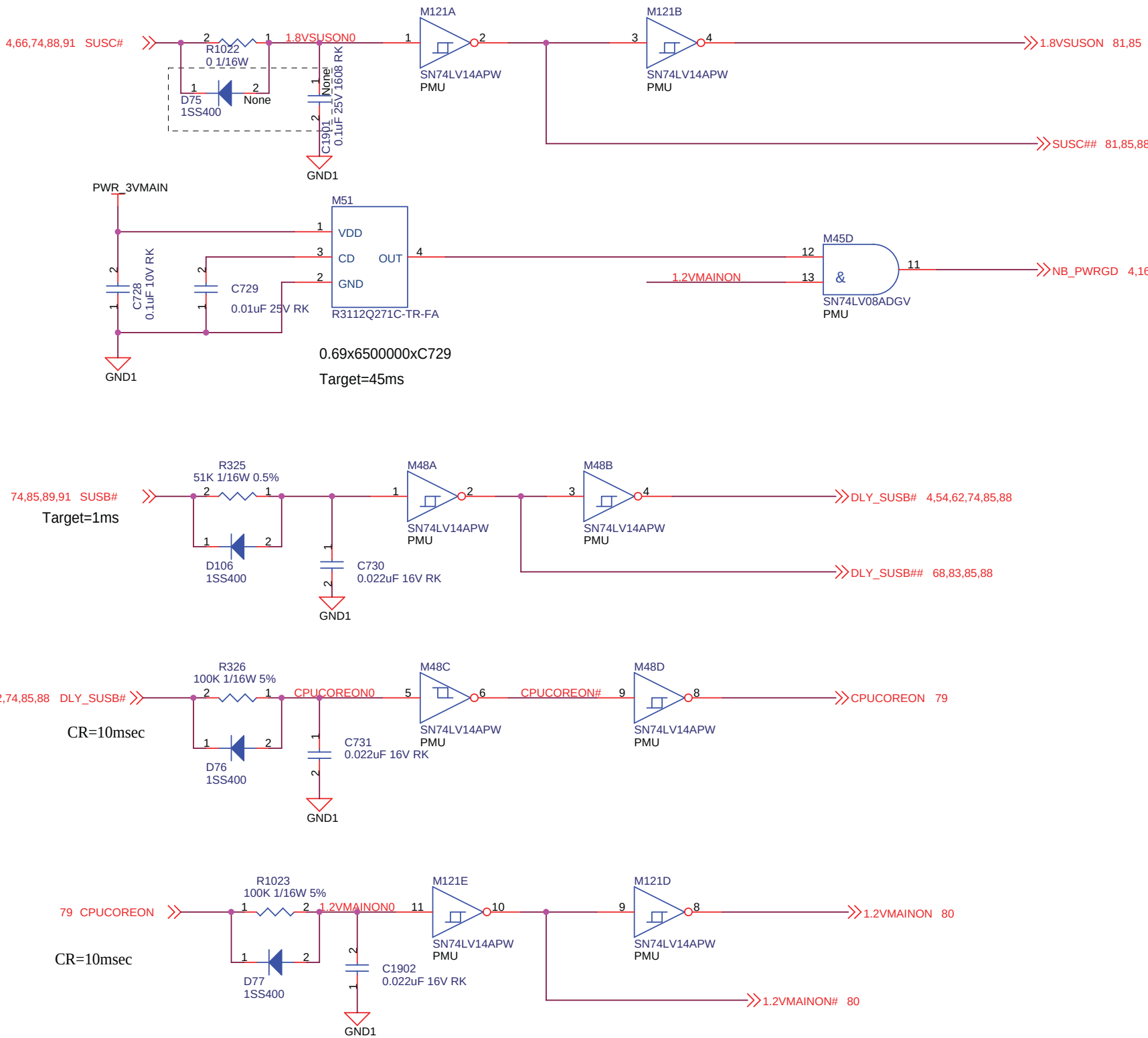
A: 80page
B: 80page
C: 80page
D: 79page
E: 71page
F: 79page
G: 79page



遅延ターゲット
BD5327G:
 $T_{plh}(s) = 0.69(TYP) \times 9(M\Omega) \times CT(F)$

RESET IC

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 75 / 93



SEQUENCE

						TITLE	
						VB313AA	
						DRAW. No.	
						C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	76 / 93

Falcon Power Supply

Caution

Features

- 1/ Voltage Regulator for AMD K8 Rev.F Processor
- 2/ ATI RS480M Chipset
- 3/ DDR2 Memory
- 4/ Internal VGA (PowerPlay is not supported)
- 5/ Normal Speed Charger
- 6/ 19V AC Adaptor
- 7/ A circuit reducing a rush current from AC adaptor
- 8/ Internal Battery with 4 or 3 Seirial cells and Digital Interface

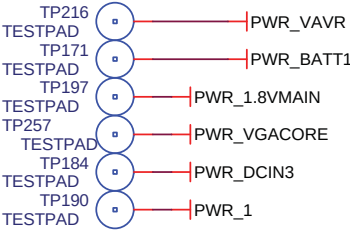
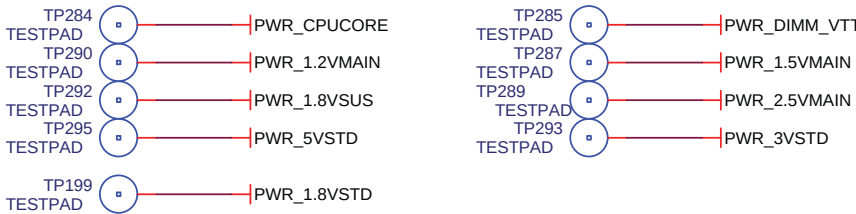
Voltage Regulator Spec.

DDC	CPUCore	TBD	35A	typ/peak
	1.2VMain	1.200V +/-5% (1.140V-1.260V)	6A	typ / 8Apeak
	1.8VSus	1.800V +/-5% (1.710V-1.890V)	6A	typ / 8Apeak
	3VStd	3.300V +/-5% (3.135V-3.465V)	6A	typ / 8Apeak
	5VStd	5.000V +/-4% (4.800V-5.200V)	6A	typ / 8Apeak
Charger	CV 3-serial 12.60V +/-1.2% (12.45V-12.75V)CC 1.33A			
	CV 4-serial 16.80V +/-1.2% (16.60V-17.00V)CC 1.33A			
LDO	DimmVtt	0.900V +/-100mV (0.800-1.000V)	+0.25A	typ / +-1Apeak
	1.5VMain	1.500V +/-5% (1.425V-1.575V)	1A	
	1.8VStd	1.800V +/-5% (1.710V-1.890V)	0.3A	
	2.5VMain	2.500V +/-5% (2.375V-2.625V)	40mA	
	VAVR	3.300V +/-2% (3.234V-3.366V)	30mA	

Power Contents

Contents		Page#	Contents		Page#
DDC	TopPage	82	Node	DCIn,Battery	91
	Delivery	83		Switch1	92
				Switch2	93
	CPUCore	84	PMU	LUNA1 (PMU part)	94
	(reserved)	85		LUNA2 (KBC part)	95
LDO	1.05V/1.8V	86		Etc0 (Common)	96
	3.3V/5V	87		Etc1 (Battery1)	97
	(reserved)	88			
	Charger	89			
		90			

TestPad (for SFJ)

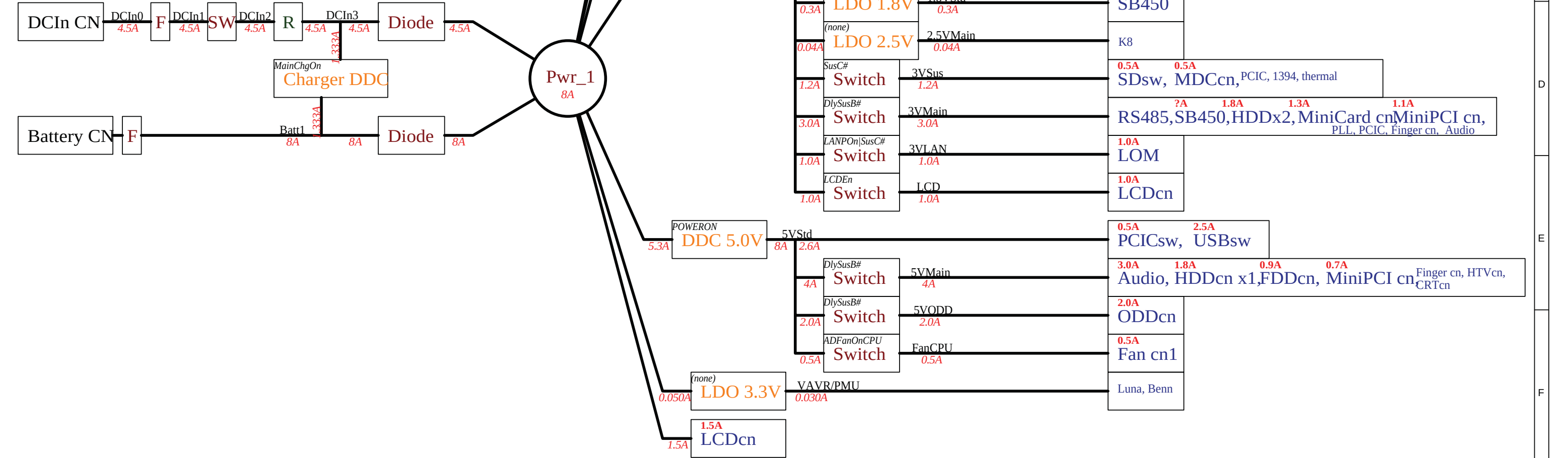


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						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet 77 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

Dolphin

Power Delivery

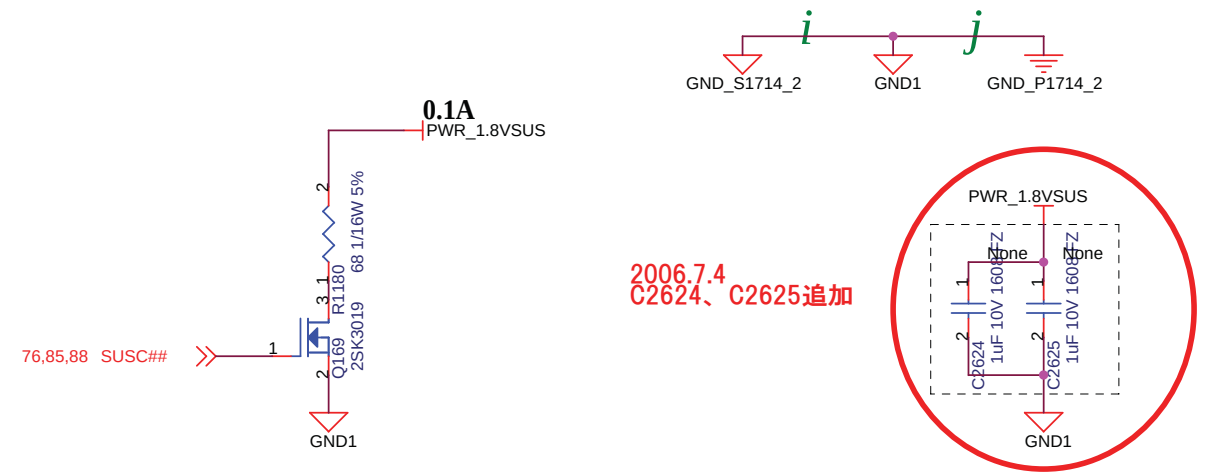
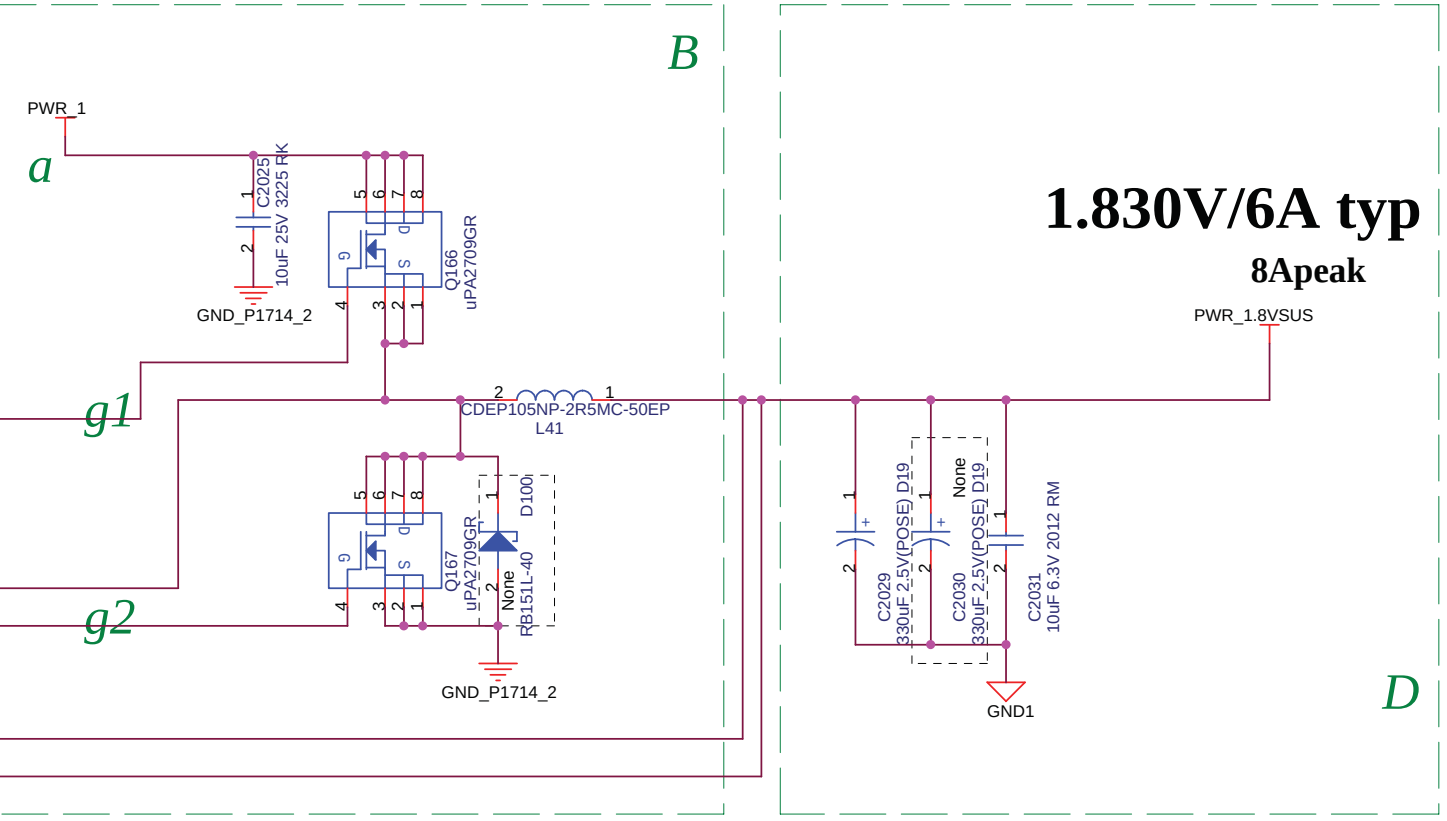
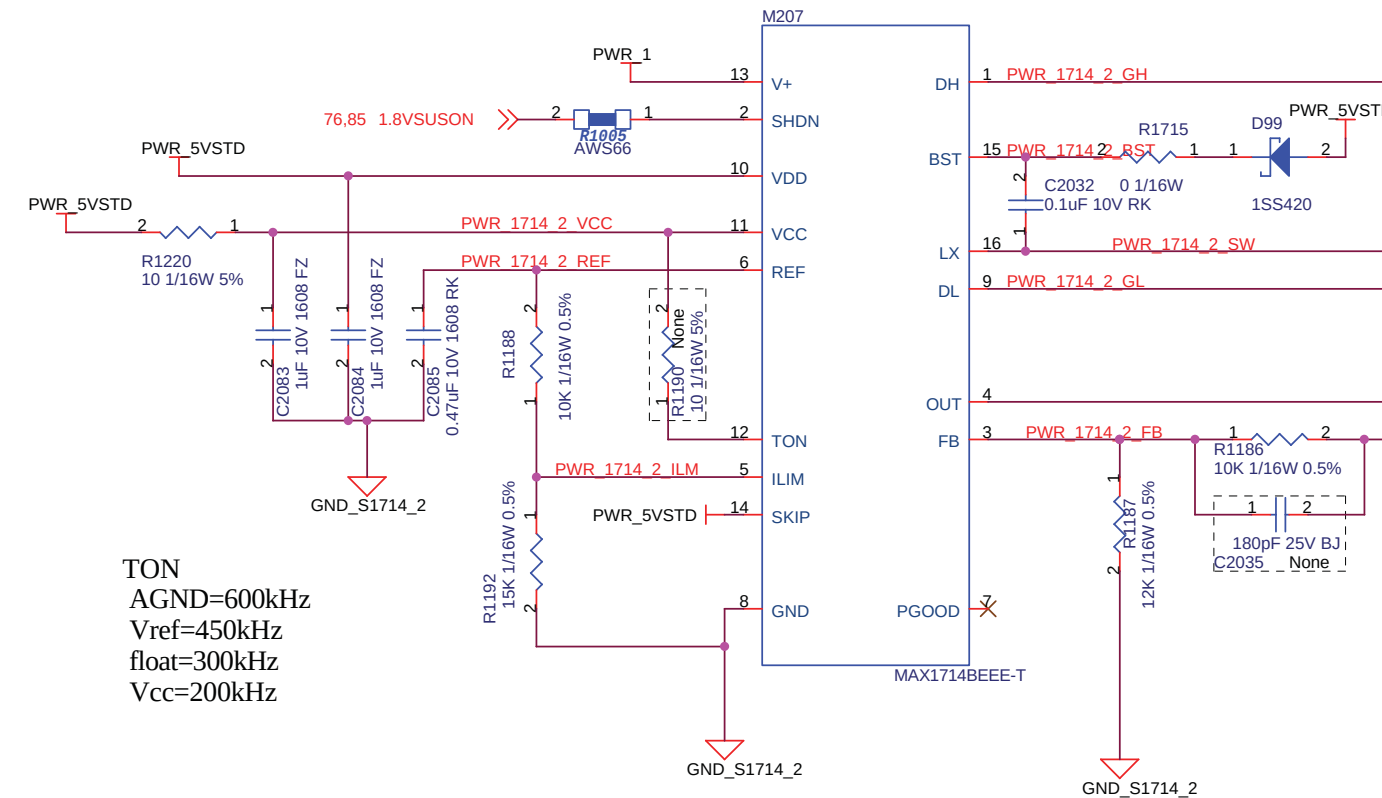
FUJITSU CONFIDENTIAL



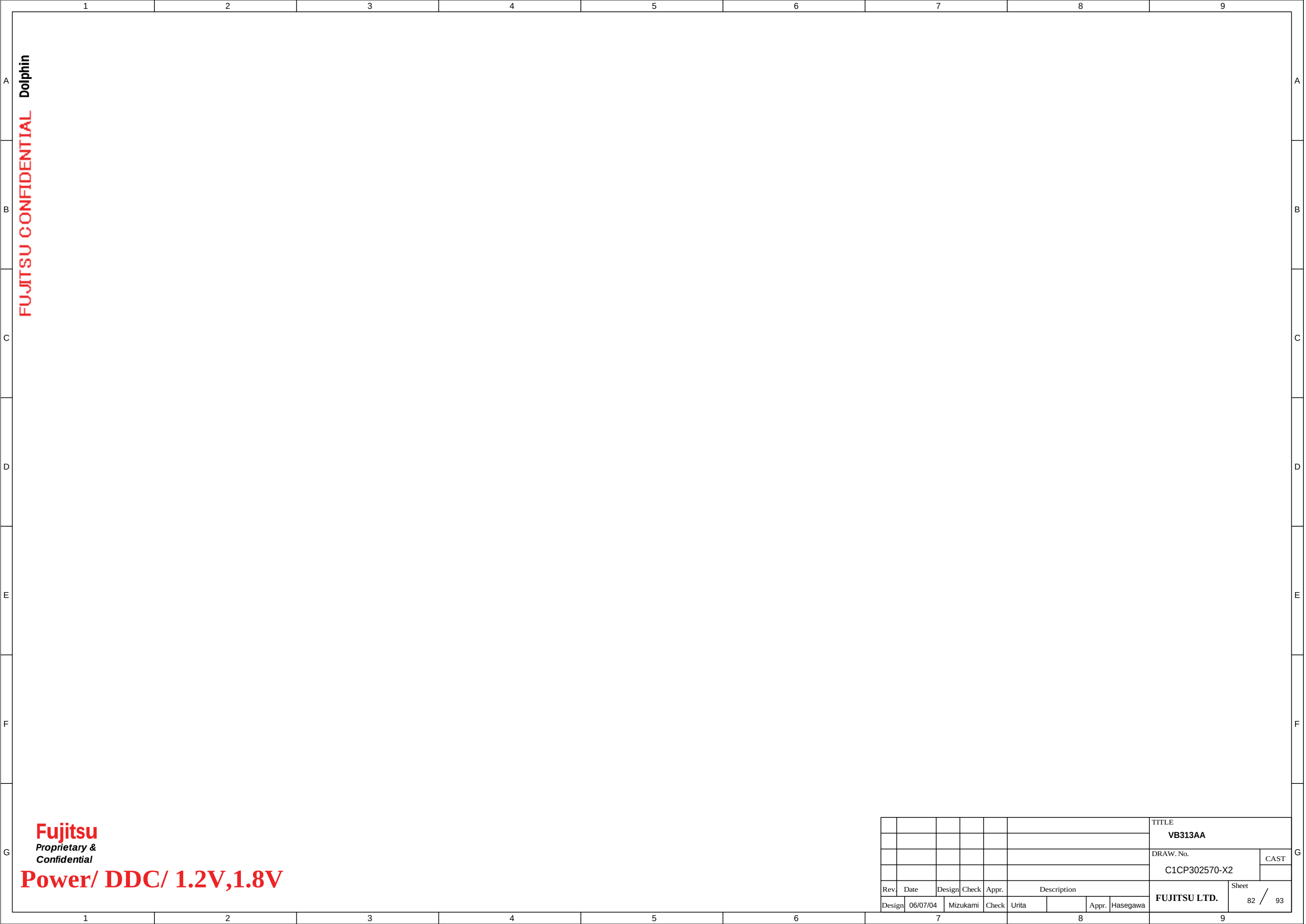
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Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	Sheet 78 / 93



									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	80 / 93		



					TITLE		
					VB313AA		
					DRAW. No.		CAST
					C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
					FUJITSU LTD.		Sheet 81 / 93

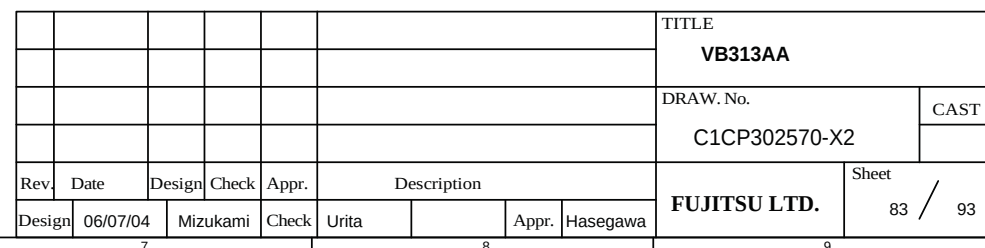


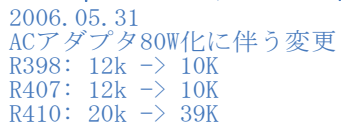
FUJITSU CONFIDENTIAL

Dolphin

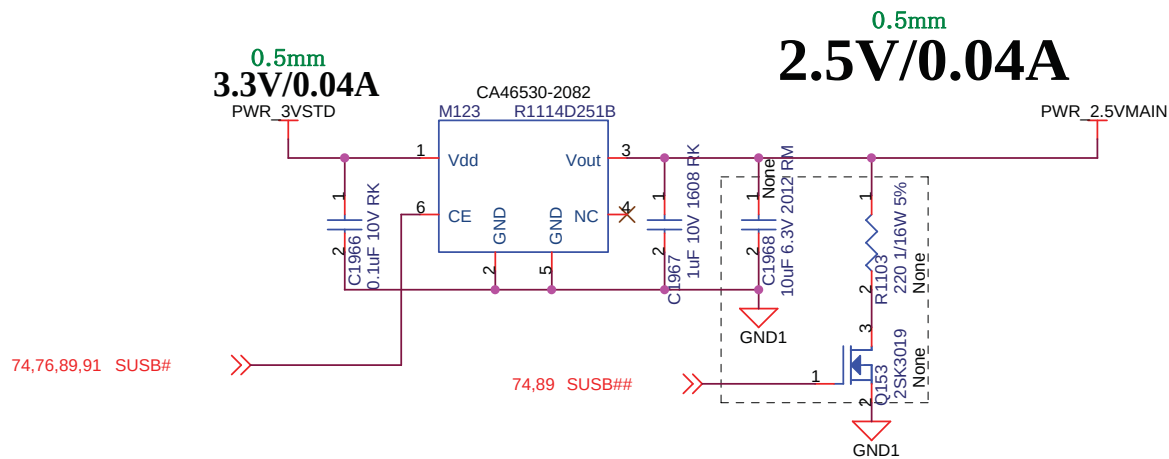
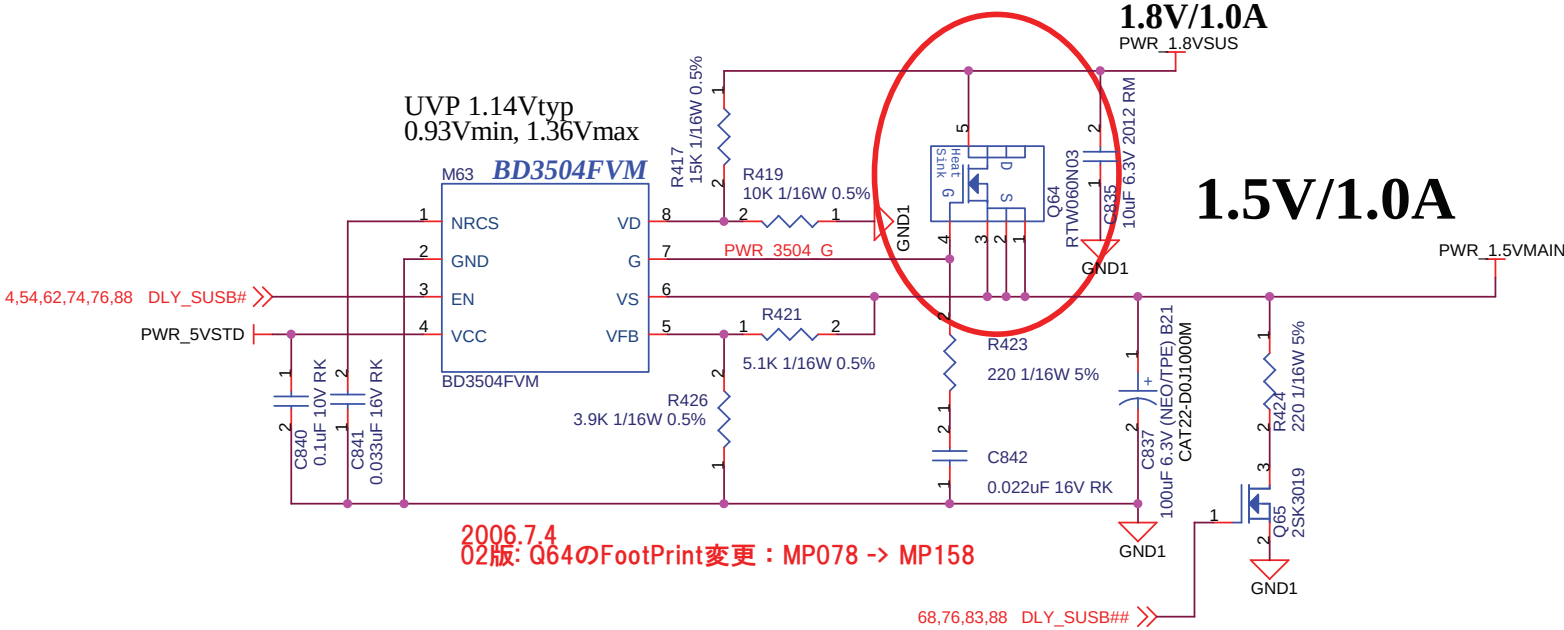
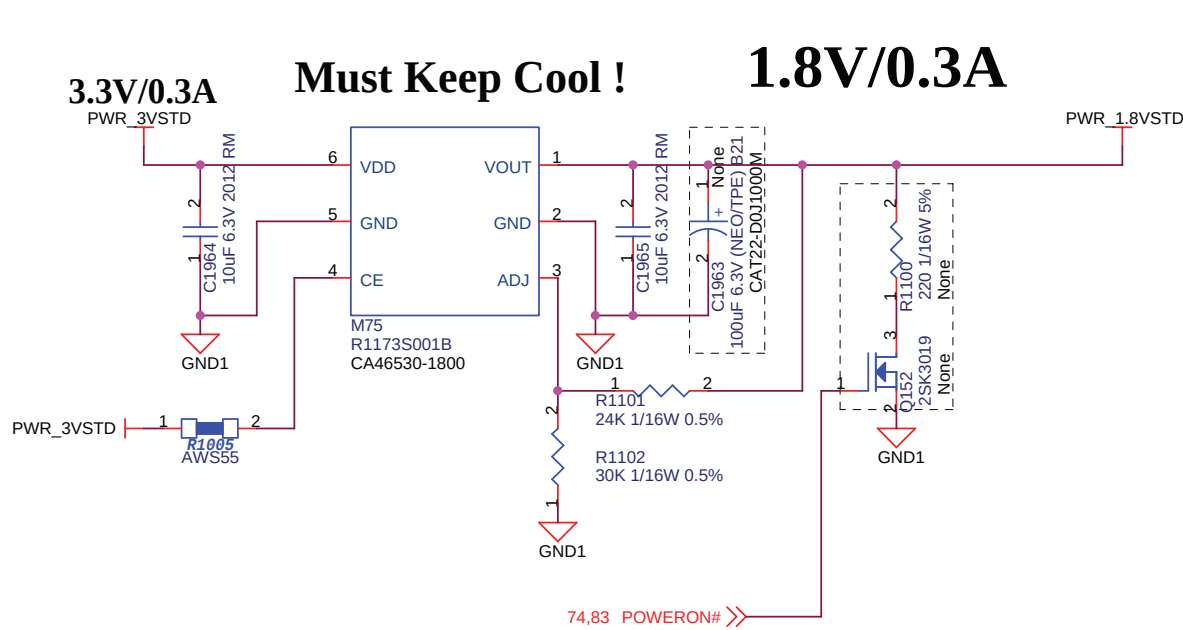
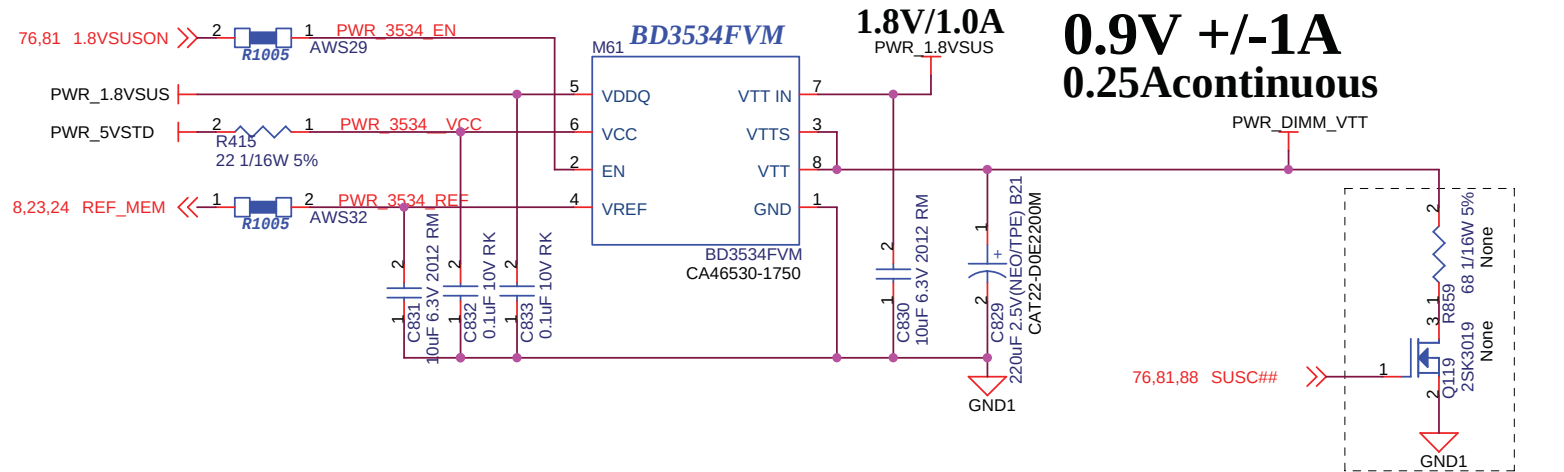
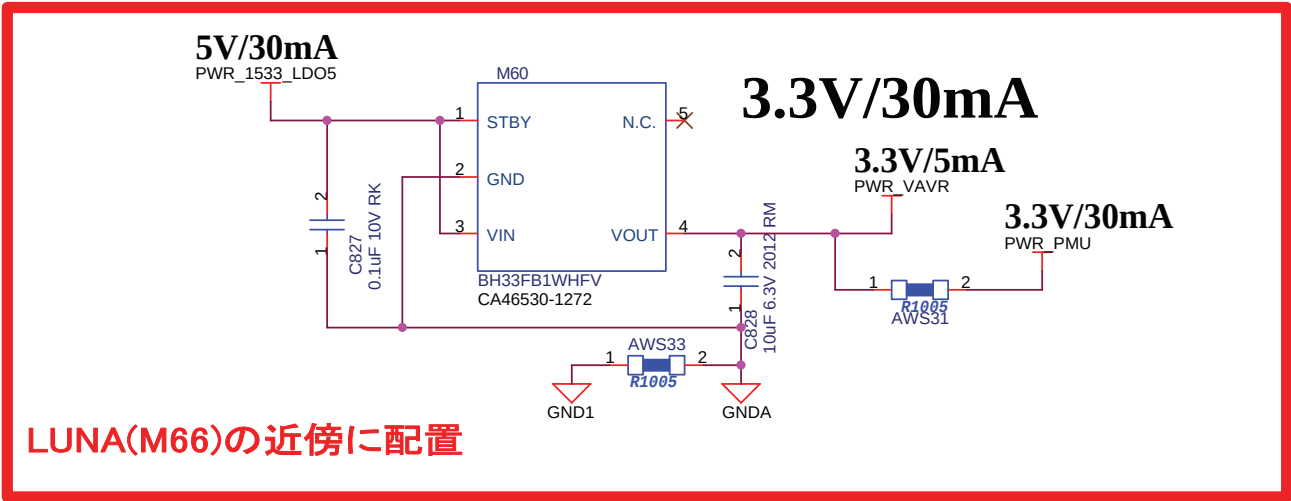
Fujitsu
Proprietary & Confidential
Power/ DDC/ 1.2V,1.8V

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						DRAW. No.			CAST
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Rev.	Date	Design	Check	Appr.	Description		Fujitsu Ltd.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	82 /	93

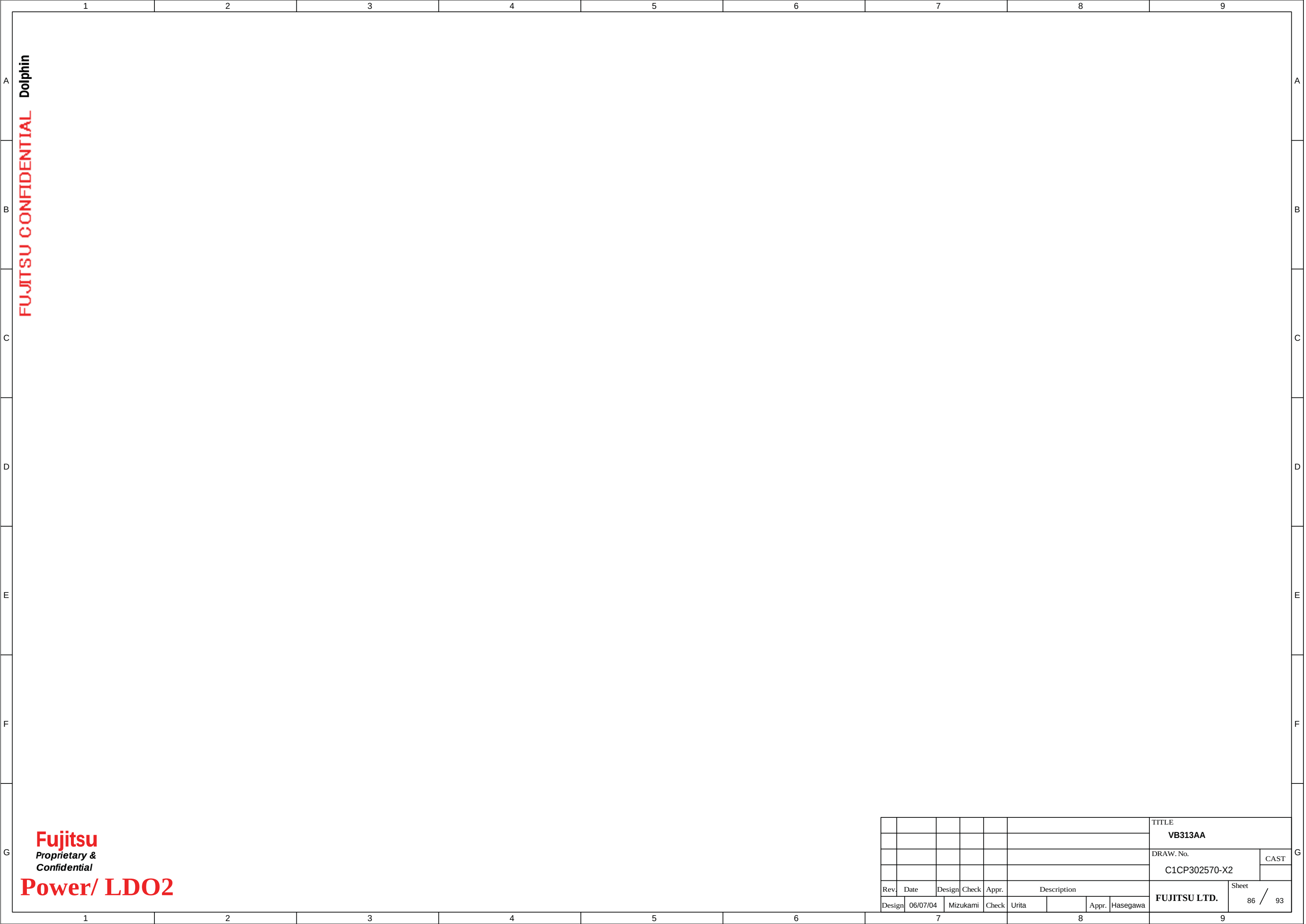




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Rev.	Date	Design	Check	Appr.	Description			Sheet 84 / 93		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			
7					8			9		



					TITLE			
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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							85 / 93	

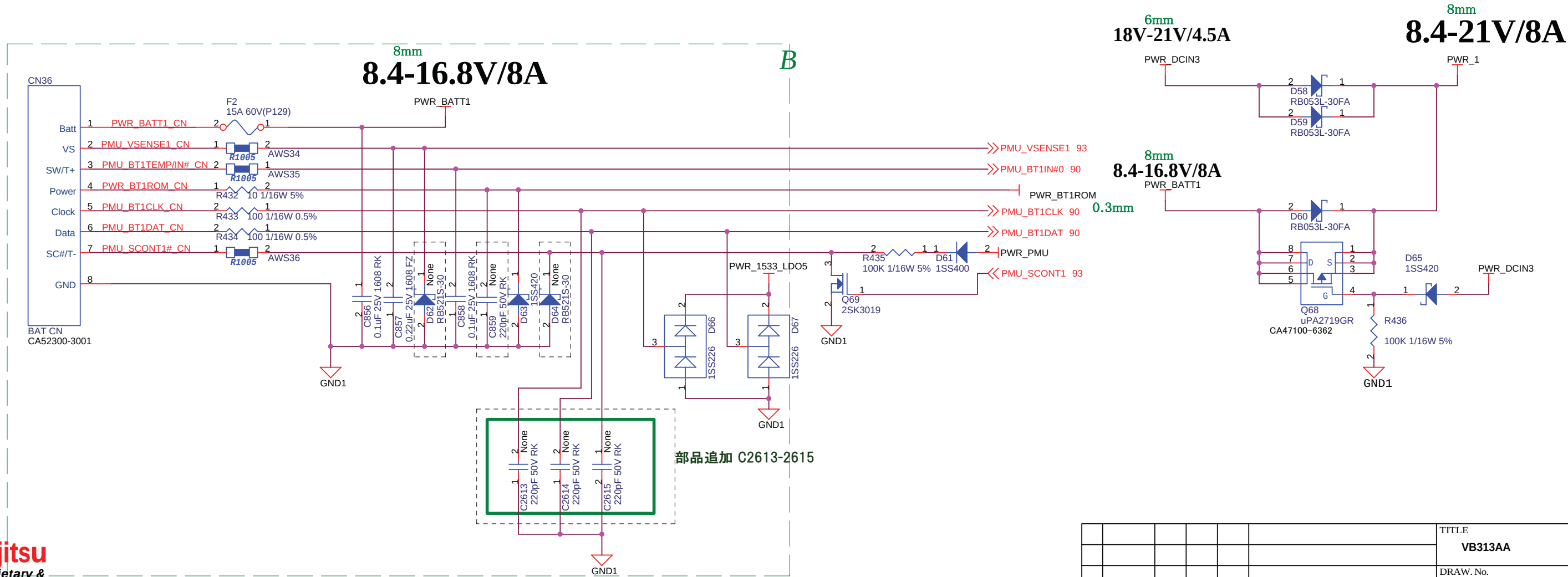
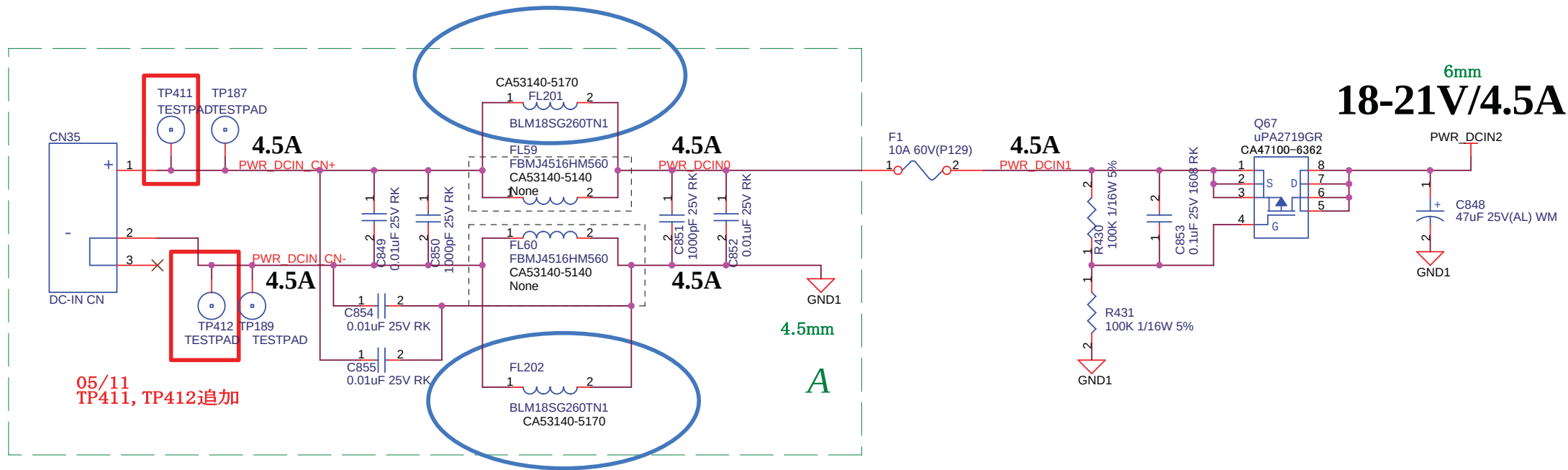


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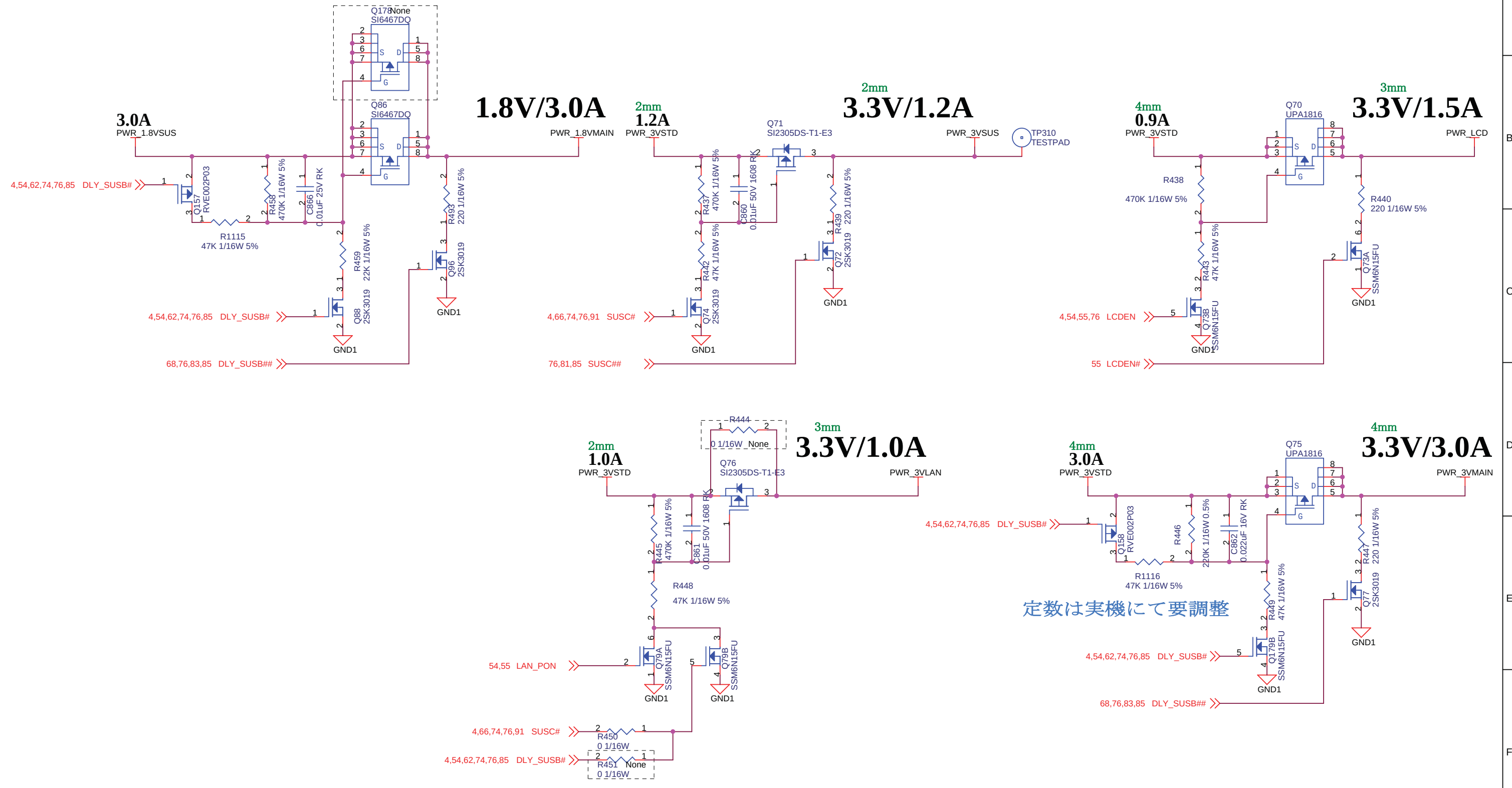
Dolphin

Fujitsu
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Confidential*
Power/ LDO2

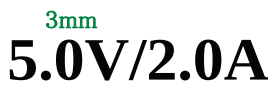
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Rev.	Date	Design	Check	Appr.	Description		Fujitsu Ltd.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	86 /	93



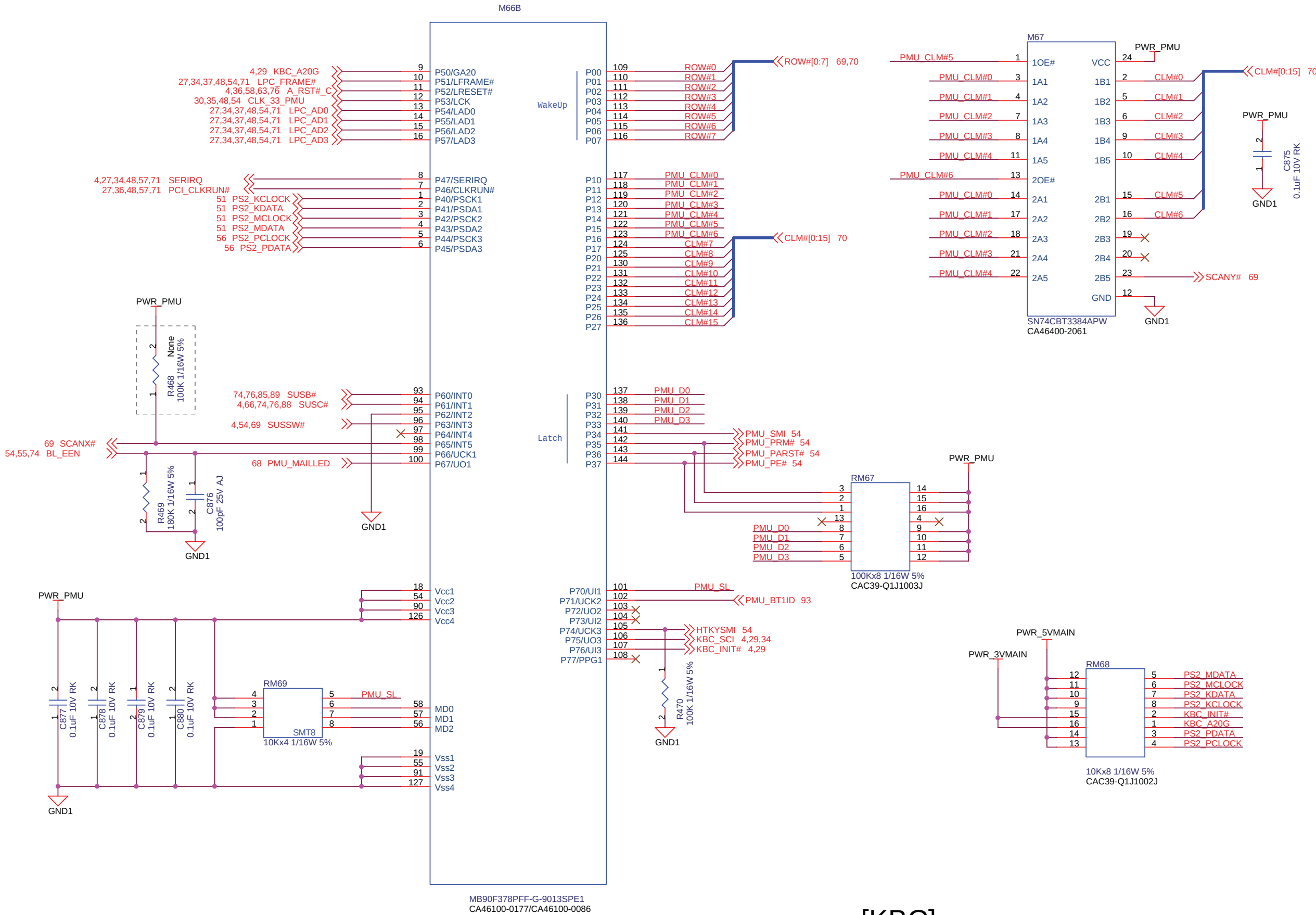
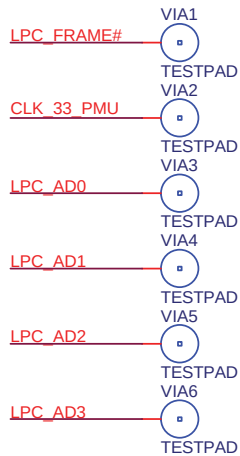
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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	87 / 93



						TITLE	
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						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		88	93
						FUJITSU LTD.	



TITLE	
VB313AA	
DRAW. No.	CAST
C1CP302570-X2	
FUJITSU LTD.	Sheet 89 / 93

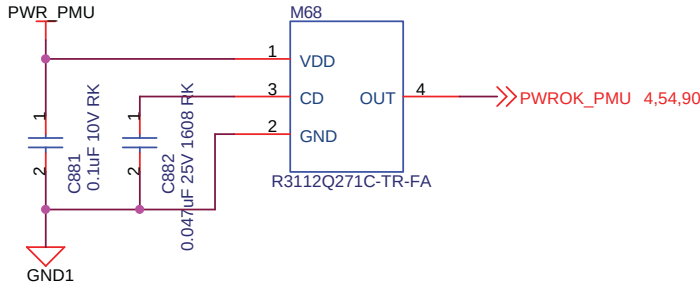
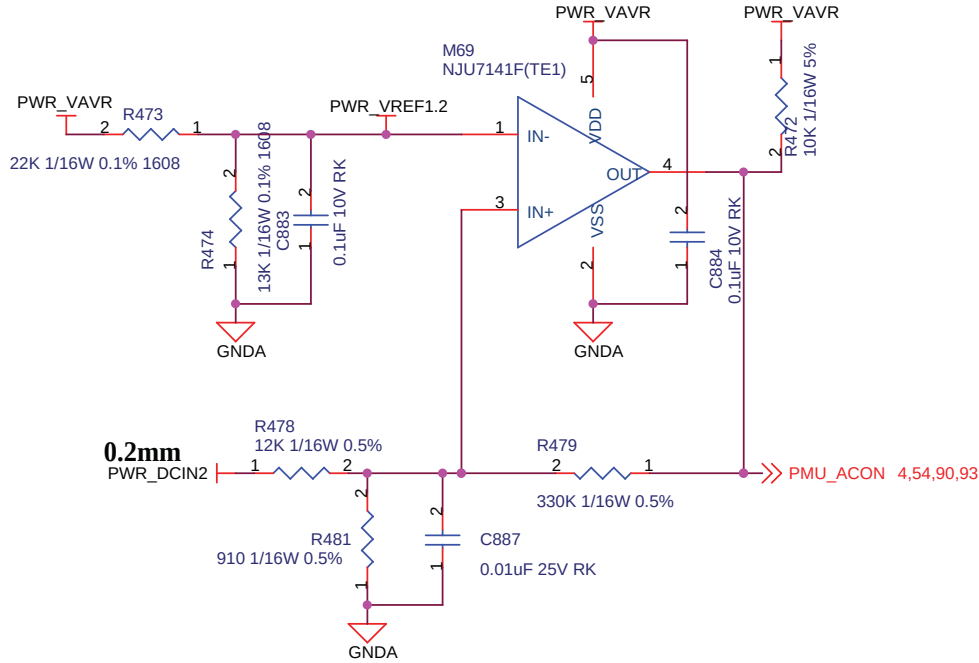


本ページの抵抗・コンデンサはM38867付近に配置すること。
パソコンについてはM38867の電源ピンに対して均等になるように配置分散し、
電源ピンまでのリード長を最大限短くなるようレイアウトすること。

[KBC]

					TITLE			
					VB313AA			
					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							91 / 93	

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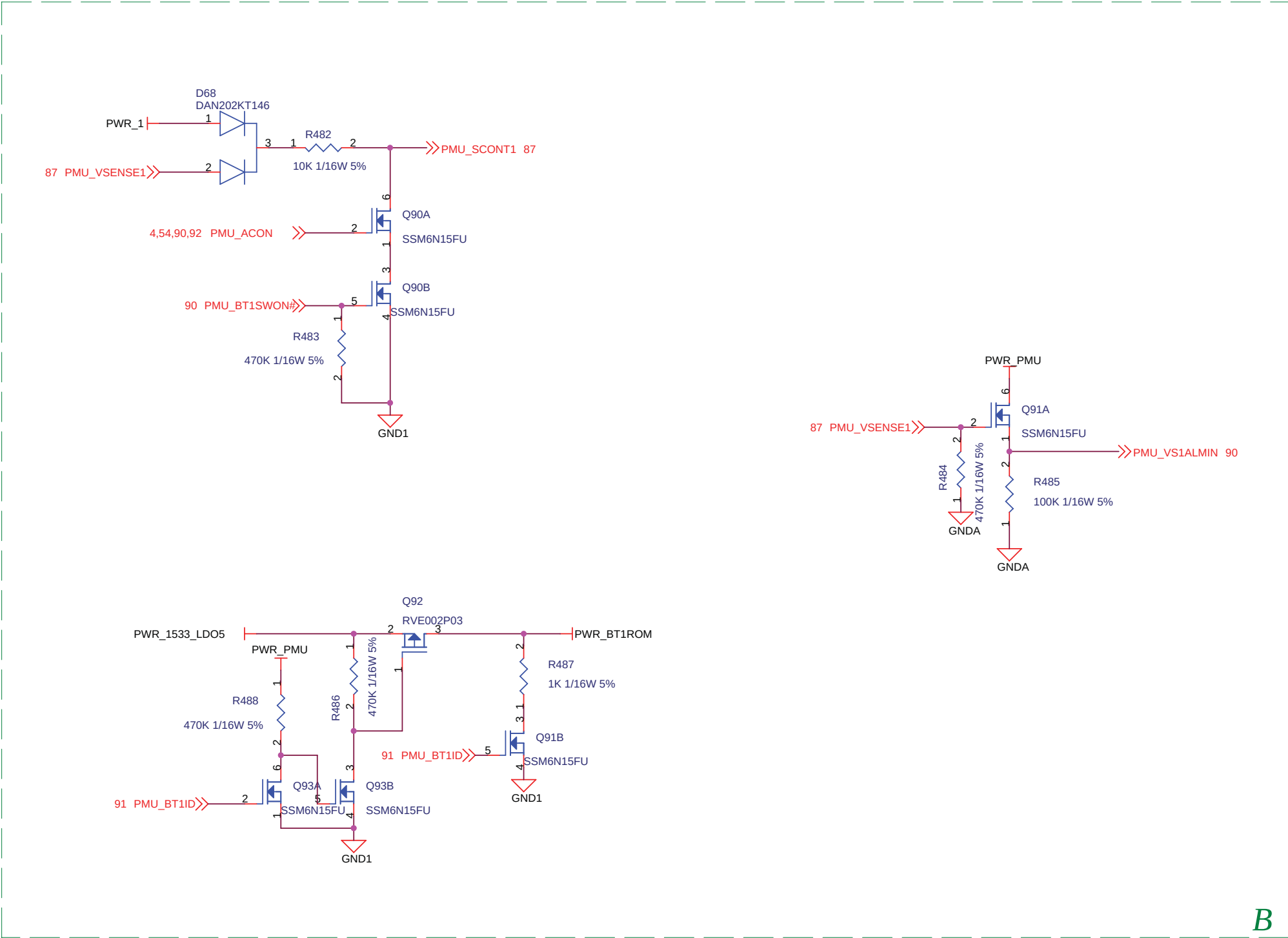
Target 200ms

遅延ターゲット
R3112N271C-TR:
 $T_{plh}(s) = 0.69(TYP) \times 6.5(M\Omega) \times CT(F)$

A

LUNA近傍に配置

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
FUJITSU LTD.						92 /	93



B

Luna近傍に配置

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 93 / 93