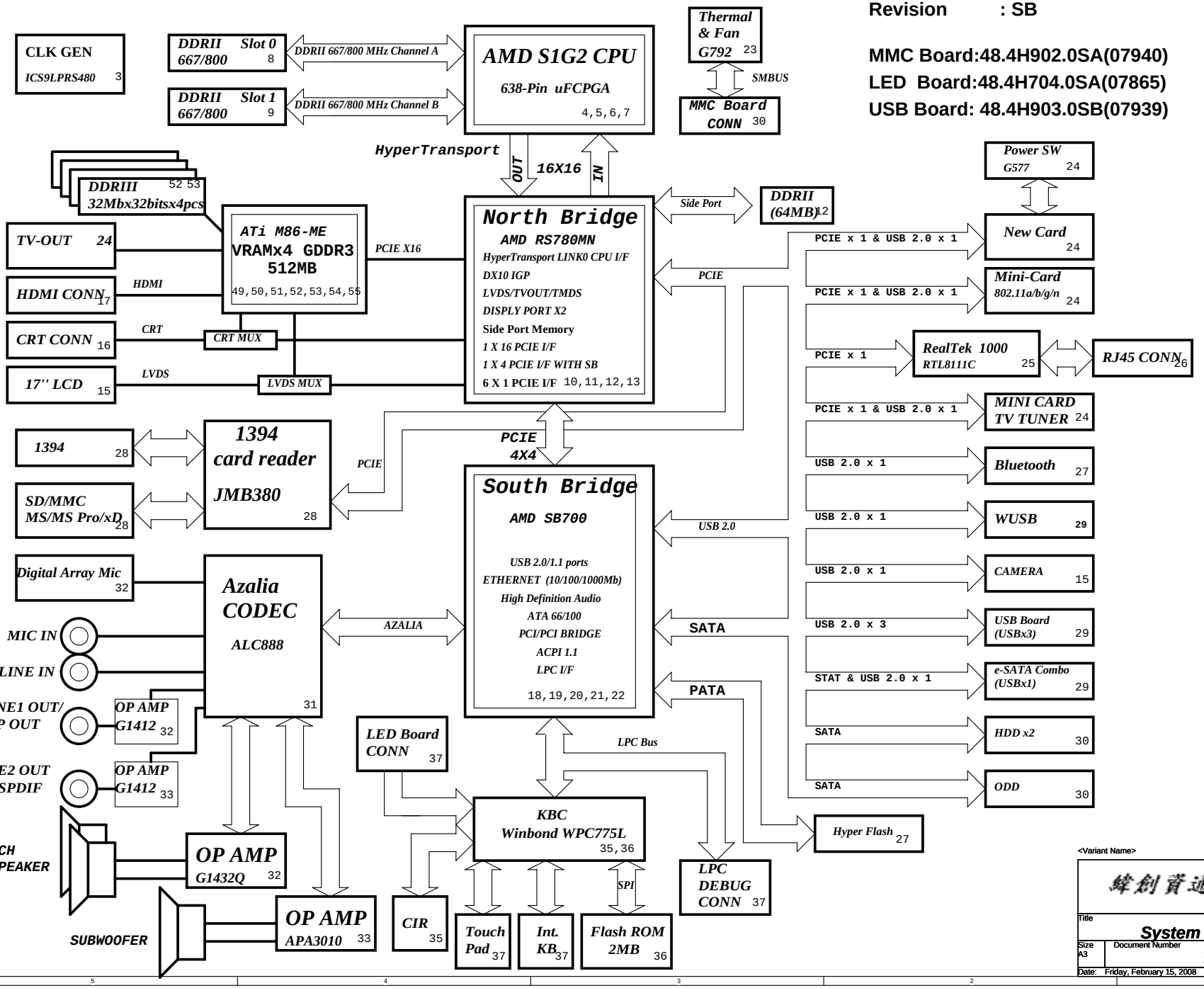
X17 Block Diagram

Project code : 91.4H901.001
PCB Number : 07256
Revision : SB

MMC Board:48.4H902.0SA(07940)
LED Board:48.4H704.0SA(07865)
USB Board: 48.4H903.0SB(07939)



CPU V_CORE	
ISL6265 40,41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC	
TPS51125 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC	
LDO 45	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC	
LDO 45	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC	
TPS51125 42	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **System Block Diagram**

Size	Document Number	Rev
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Date: Friday, February 15, 2008 Sheet 1 of 56

SB700 Functional Strap Definitions

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

		USB PORT#	DESTINATION
SB700	2.0	0	Combo(ESATA/USB)
		1	USB1
		2	USB2
		3	CAMERA
		4	Bluetooth
		5	NEW CARD
		6	USB3
		7	WLAN
		8	TV TUNER
		9	WUSB
		10	NC
		11	NC
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER &1394
Lane 4	TV tuner
Lane 5	NC

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX XX	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED, IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

Release BOM need modify

Page	Location	Schematic	BOM	2nd Source	Main source	3rd source
P3	U41(CLK GEN)	71.09480.003	71.09480.003	71.08628.003		
P10	U65(RS780MN)	71.RS780.M02	71.RS780.M07			
P18	U74(SB700)	71.SB700.M02	71.SB700.M06			
P41	U57,U11,U52,U51,(CPU power) U56,U53	ZZ.COMBO.001	84.04634.037			
P46	U62(GPU power)	ZZ.COMBO.001	84.07686.037			
P12	U17 (Side Port)	72.18512.M0U		72.18512.M0U(Qimonda)	72.55162.00U(HYNIX)	72.45116.A0U(Samsung)
P53 P54	U68~U71 (Vram)	72.18321.00U(Qimonda 700M)		72.18321.A0U(Qimonda 900M)	72.18321.00U(Qimonda 700M)	72.41032.B0U(Samsung)

<Variant Name>

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Title: ***Table of Content***

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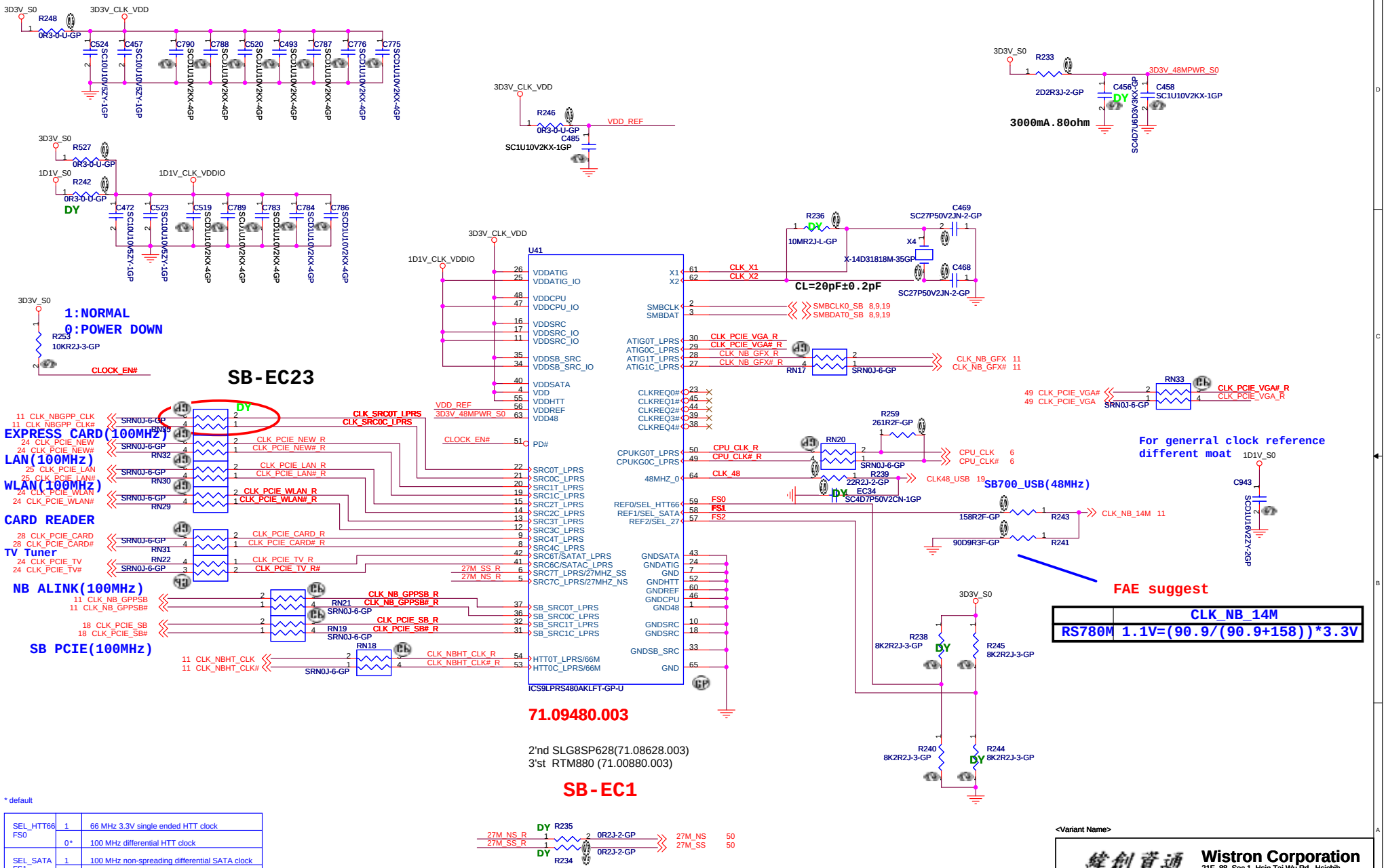

* default

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1	100 MHz non-spreading differential SATA clock
	0 *	100 MHz spreading differential SRC clock
SEL_27 FS2	1 *	27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
	0	100MHz differential spreading SRC clock

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Gen-ICS 9LPR480

Size	Document Number	Rev
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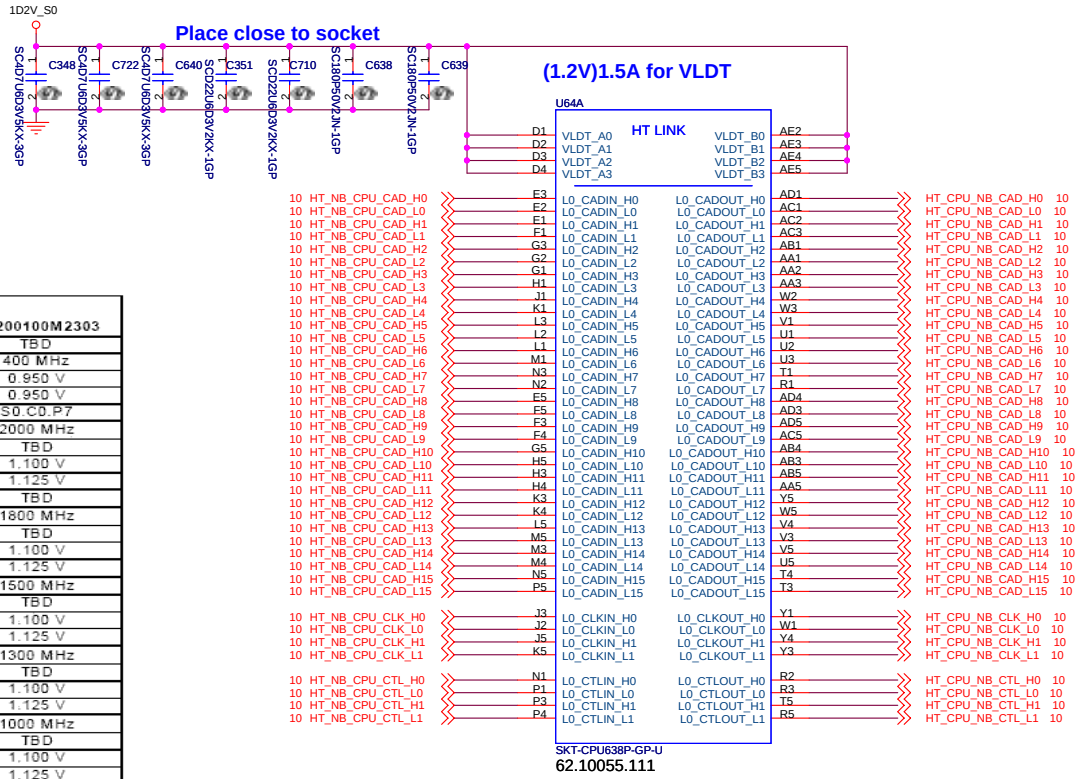
Date: Tuesday, February 19, 2008 Sheet 3 of 56

CPU / HT3.0

SSID = CPU



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: X17 | Rev: SA

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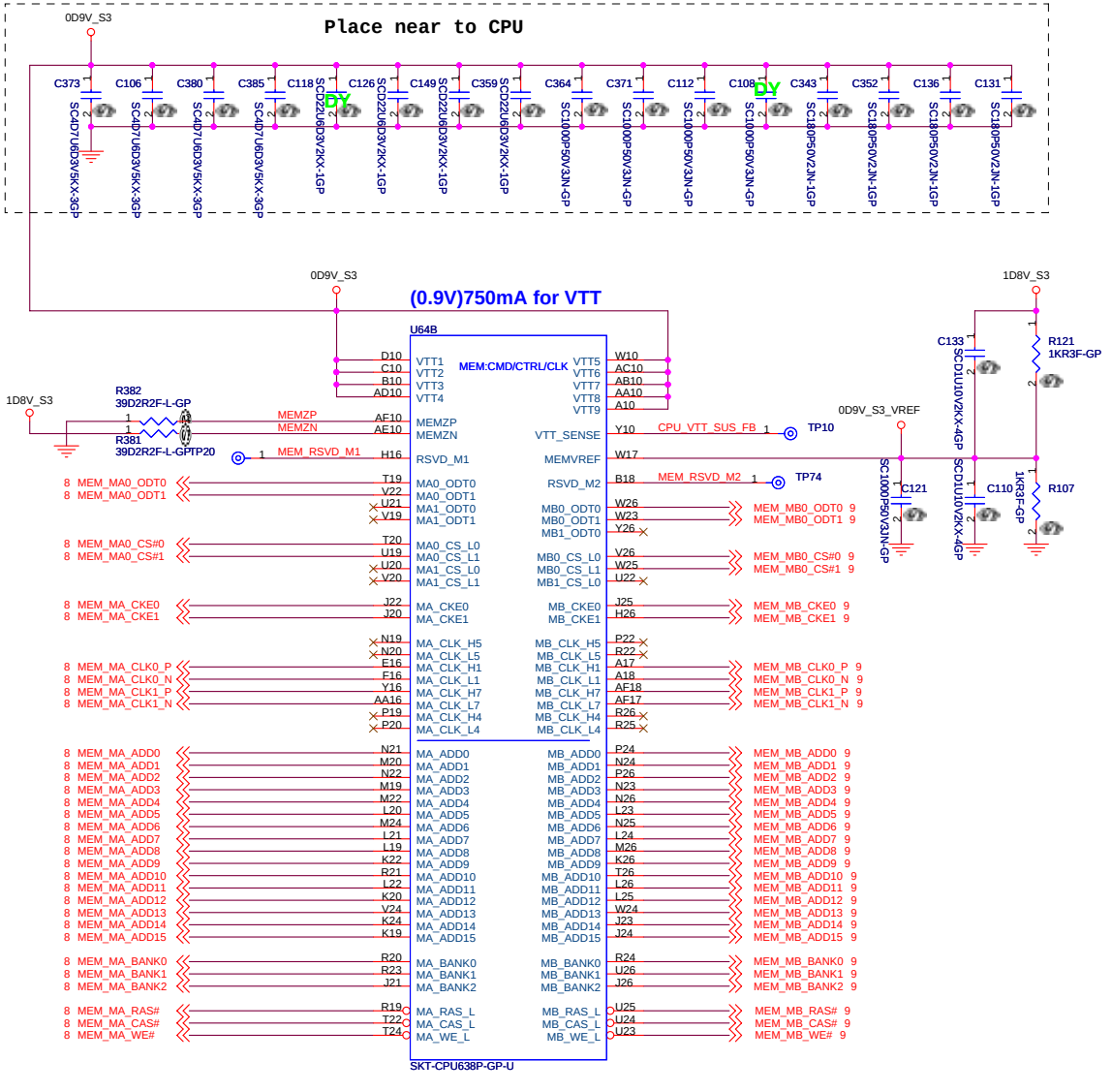
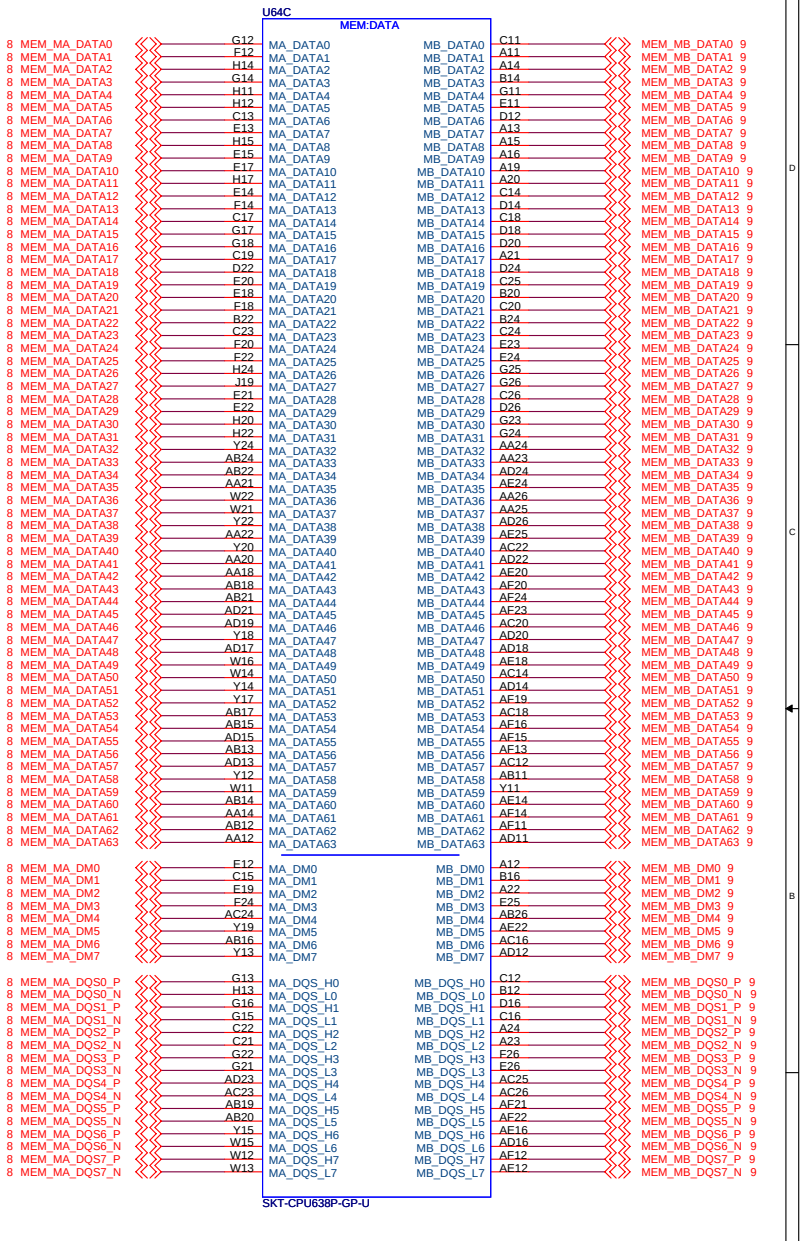
CPU / DDR2





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CPU_DDR_(2/4)

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LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

(2.5V)250mA for VDDA

Cloce To CPU

CPU_CLK(200MHz)

For HDT DBG

near cpu

Sideband temperature

CPU temperature sensor
driver INT event to EC

CPU exceeds to 125℃

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

SB-EC63

HDT Connectors

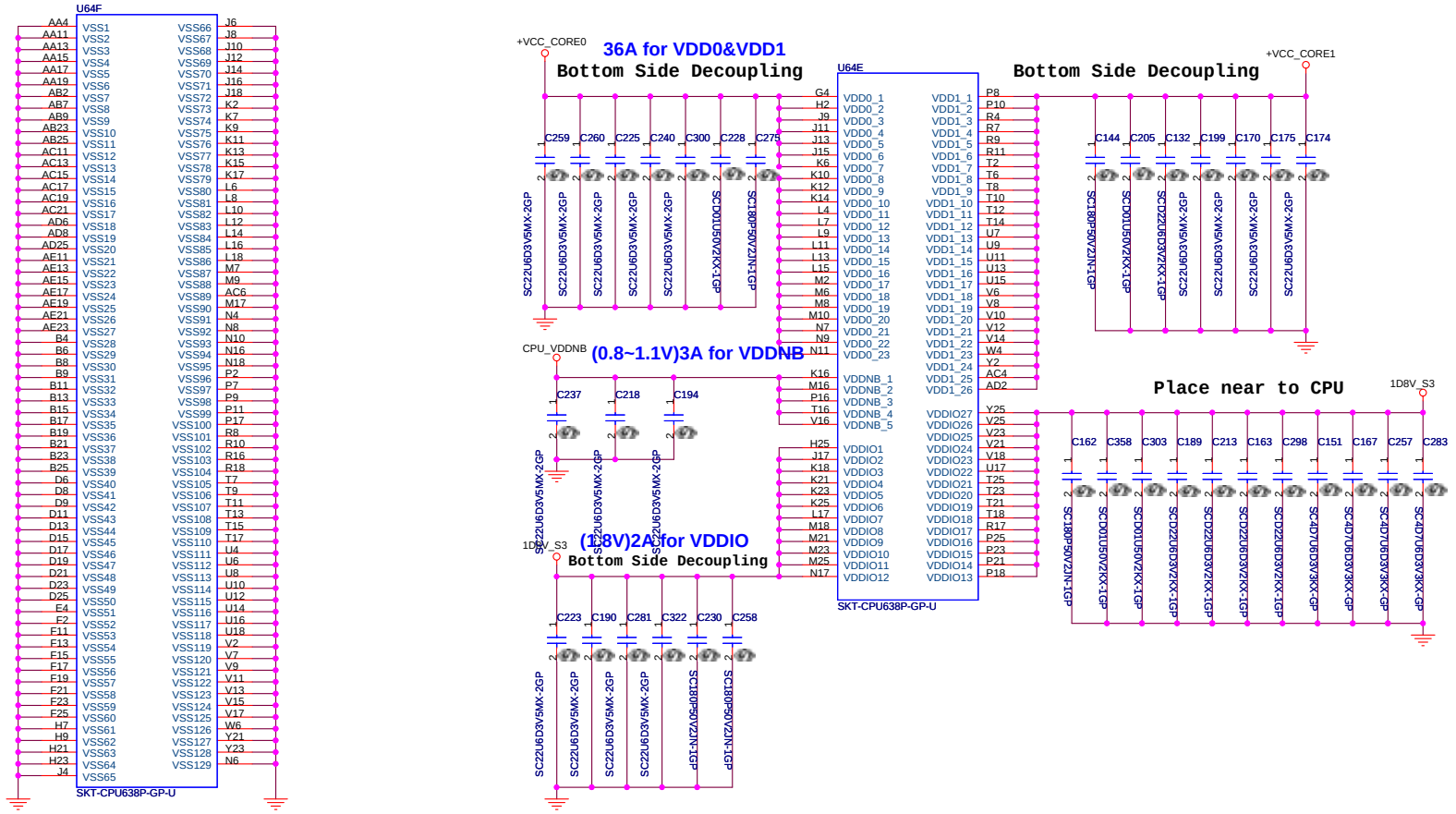
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: X17 | Rev: SA

Date: Friday, February 15, 2008 | Sheet 6 of 56

SSID = CPU



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
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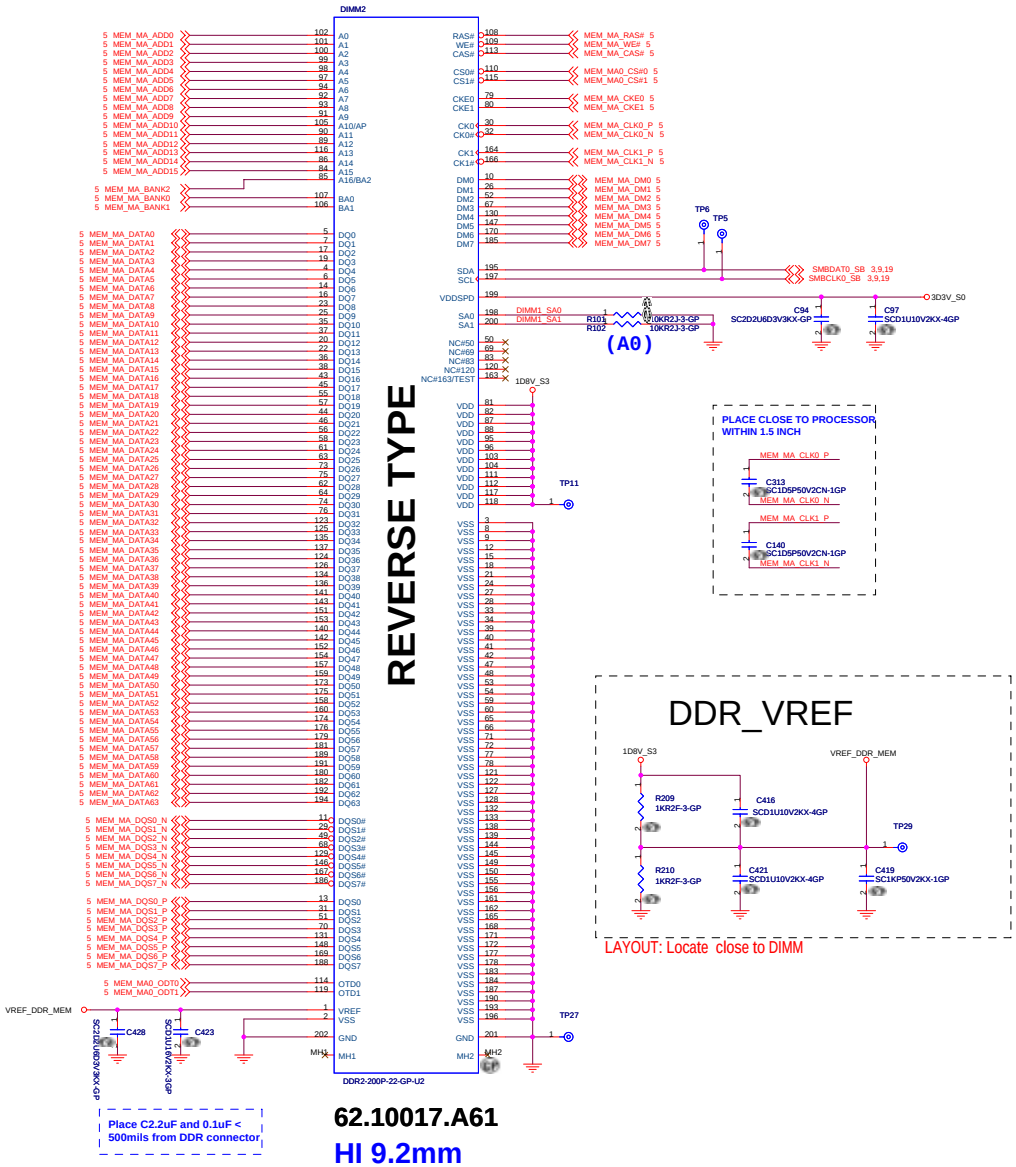
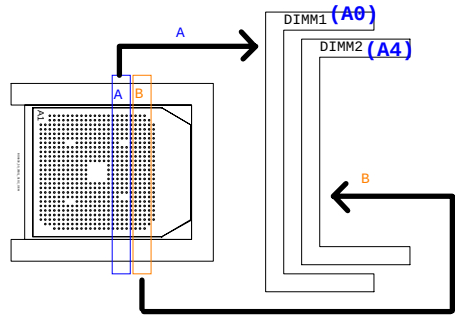
Date: Friday, February 15, 2008 Sheet 7 of 56

SSID = MEMORY



62.10017.A61

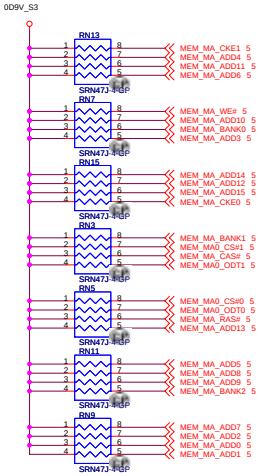
HI 9.2mm



PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

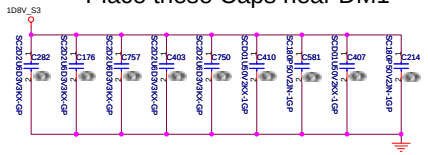


DDR_VREF

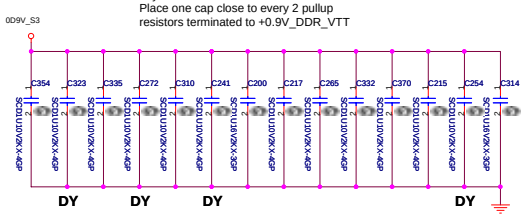
LAYOUT: Locate close to DIMM

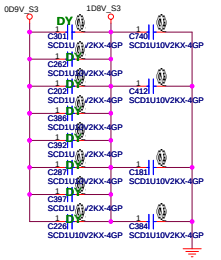
Decoupling Capacitor

Place these Caps near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_DIMM1

Size: A2 | Document Number: X17 | Rev: SA

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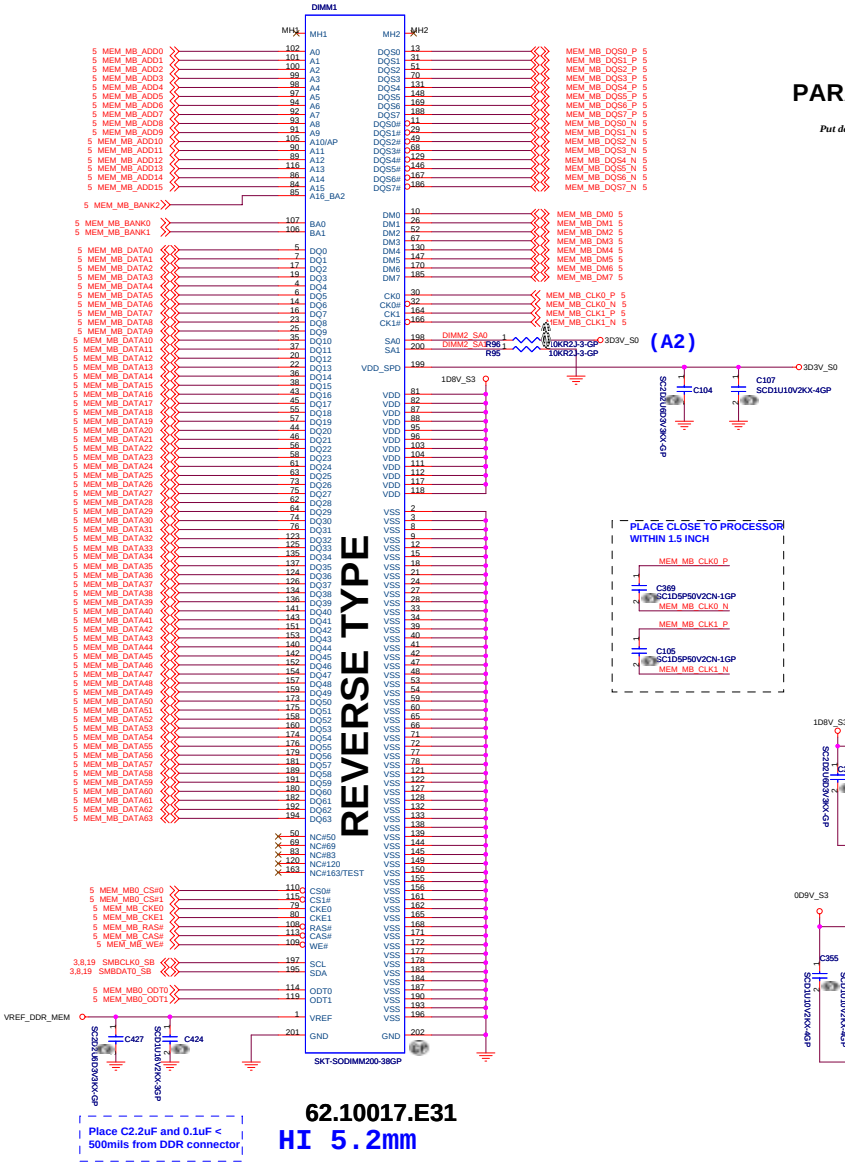
SSID = MEMORY



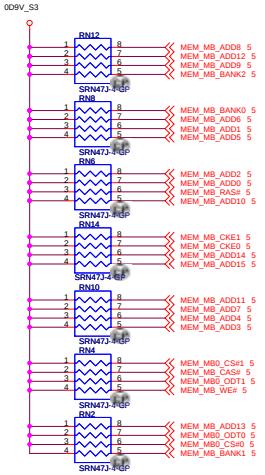
62.10017.E31

HI 5.2mm

PARALLEL TERMINATION

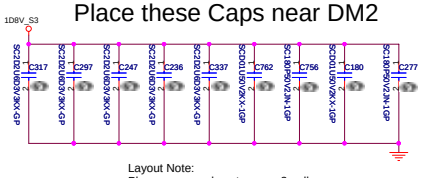
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

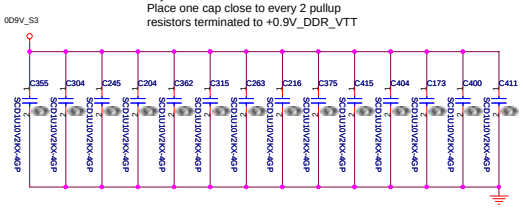


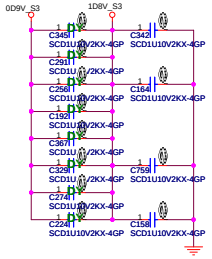
Decoupling Capacitor

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





<Variant Name>

Wistron Corporation
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Title: DDR_DIMM2

Size: A2 | Document Number: X17 | Rev: SA

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SSID = N.B

SB-EC13

U65A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U1

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

U65B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780M-GP-U1

Placement: close RS780 Placement: close RS780

For A-Link reference different moat

NEW
WLAN
LAN
CARD
TV

A-LINK

Symbol use (71.RS780.002)
BOM use AMD RS780 (71.RS780.007)

Place < 100mils from pin AC8 and AB8

<Variant Name>

蜂創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M HT LINK&PCIE(1/4)

Size: A3 | Document Number: X17 | Rev: SA

Date: Tuesday, February 19, 2008 | Sheet 10 of 56

SSID = N.B

SB-EC-81

STRAP_DEBUG_BUS_GPIO_ENABLE
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)
*0 : Enable 1 : Disable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

close NB within 1000 mil

Close to NB ball

ENABLE External CLK GEN

pull up form SB

SB-EC6

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

15mil width

15mil width

U65C — RS780M-GP-U1 — PART 3 OF 6

CRT/TVOUT: AVDD1, AVDD2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, C_Pr, Y, COMP_Pb, RED, REDb, GREEN, GREENb, BLUE, BLUEb, DAC_HSYNC, DAC_VSYNC, DAC_SCL, DAC_SDA, DAC_RSET

PLL/PWR/LVTM: PLLVDD, PLLVDD18, PLLVSS, VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2, SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP

CLOCKs PM: HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN, REFCLK_N, GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP, GPPSB_REFCLKN

MIS.: I2C_CLK, I2C_DATA, DDC_CLK0/AUX0P, DDC_DATA0/AUX0N, DDC_DATA0/AUX0N, DDC_CLK0/AUX0P, DDC_CLK1/AUX1P, DDC_DATA1/AUX1N, STRP_DATA, RESERVED, AUX_CAL

TXOUT_L0P/N, TXOUT_L1P/N, TXOUT_L2P/N, TXOUT_L3P/N, TXCLK_LP/LN, TXCLK_UP/UN, TXOUT_U0P/N, TXOUT_U1P/N, TXOUT_U2P/N, TXOUT_U3P/N

VDDLTP18, VSSLTP18, VDDLT18_1, VDDLT18_2, VDDLT33_1, VDDLT33_2, VSSLT1–VSSLT7

LVDS_DIGON, LVDS_BLON, LVDS_ENA_BL

TMDS_HPD, HPD, SUS_STAT#, THERMALDIODE_P, THERMALDIODE_N, TESTMODE

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_LVDS&CRT_(2/4)

Size: A3 | Document Number: X17 | Rev: SA

Date: Tuesday, February 19, 2008 | Sheet 11 of 56

SSID = N.B

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

15mil width

15mil width

SB-EC-78
ATI DY

DY

Layout Note: 50 mil for VSSDL

Main source: 72.55162.00U(HYNIX)

2'nd source : 72.18512.M0U(Qimonda)

3'rd source : 72.45116.A0U(Samsung)

72.18512.M0U

<Variant Name>

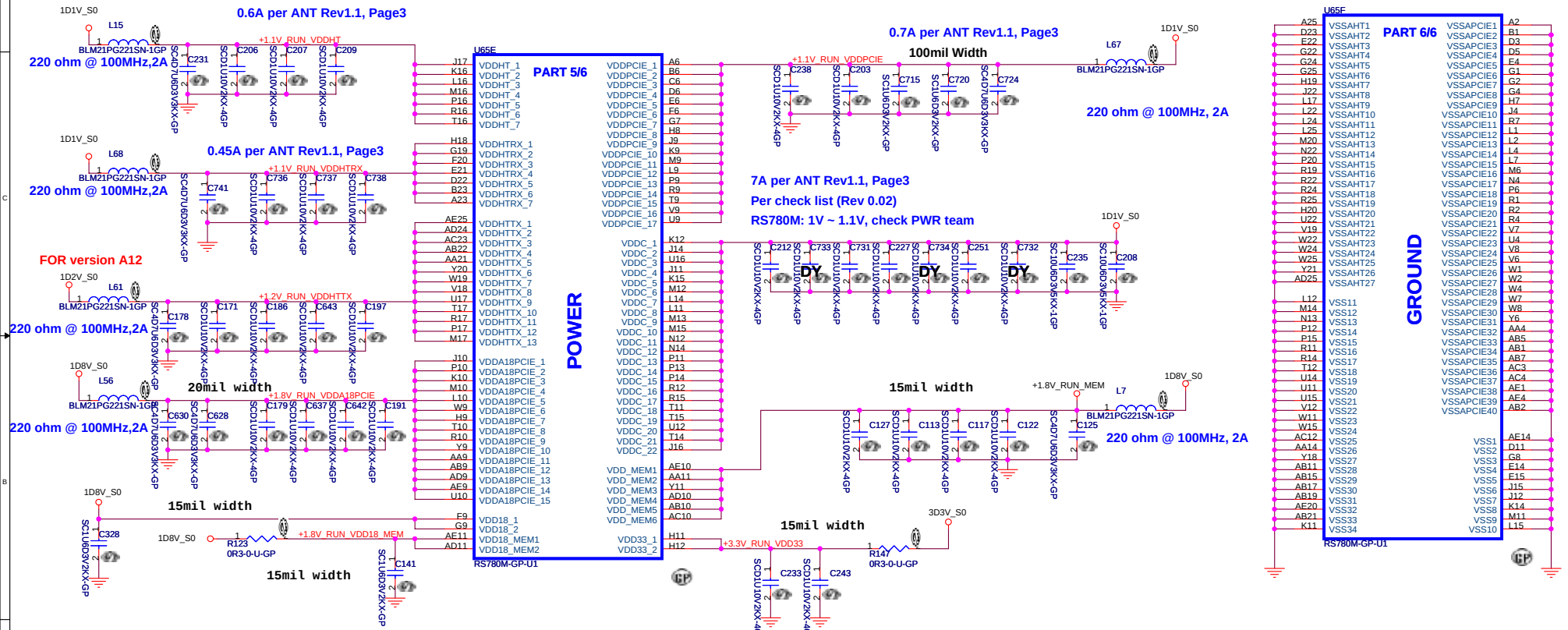
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_SidePort_(3/4)

Size	Document Number	Rev
A3	X17	SA

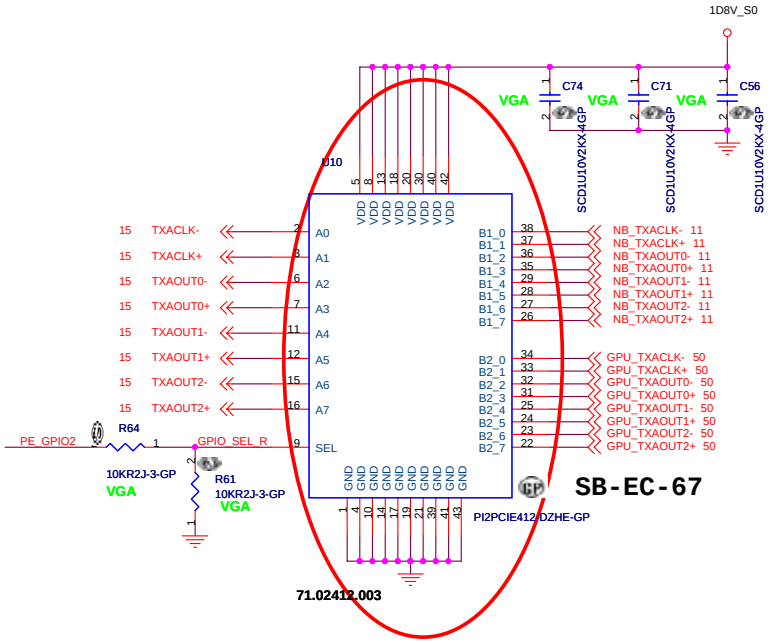
Date: Tuesday, February 19, 2008 Sheet 12 of 56

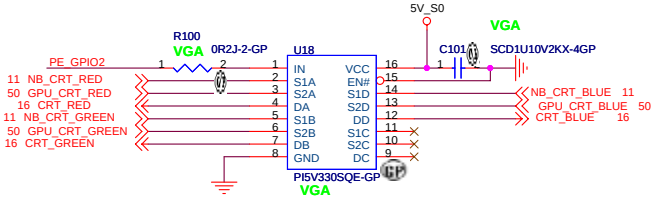
SSID = N.B

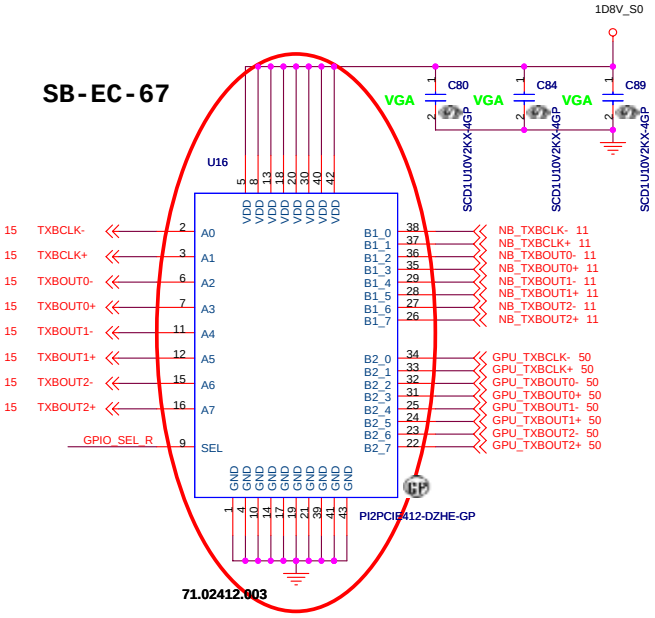


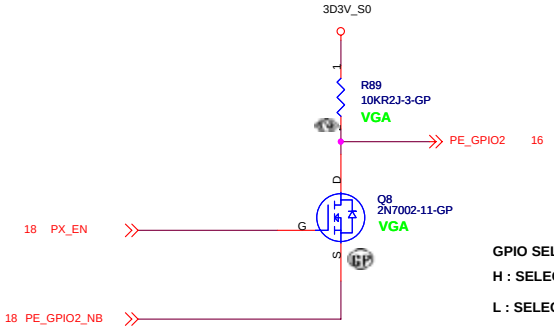
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ATi-RS780M_PWR&GD_(4/4)***	
Size A3	Document Number **X17**	Rev **SA**
Date: Friday, February 15, 2008	Sheet 13 of 56	





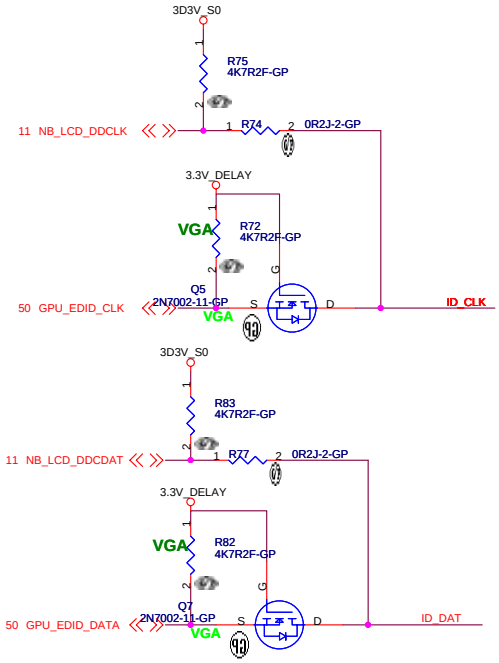


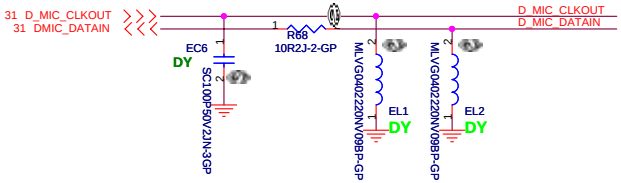


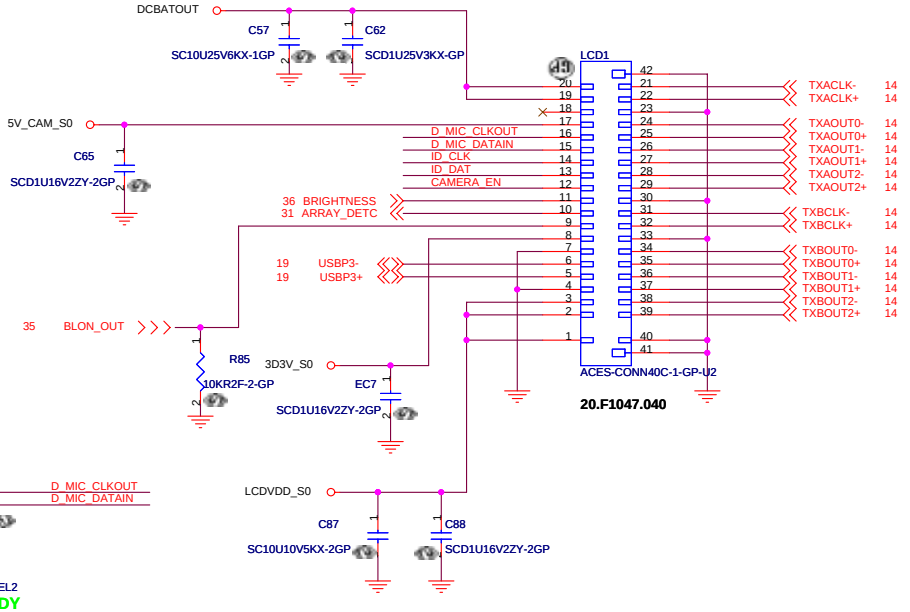
<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT / LVDS MUX***	
Size A3	Document Number **X17**	Rev **SA**
Date: Tuesday, February 19, 2008	Sheet 14 of 56	

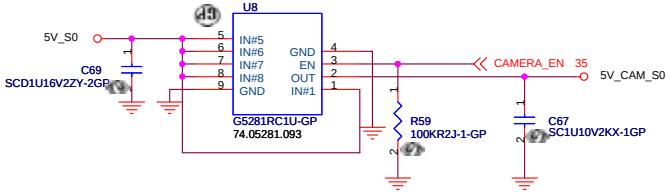
LCD CONNECTOR

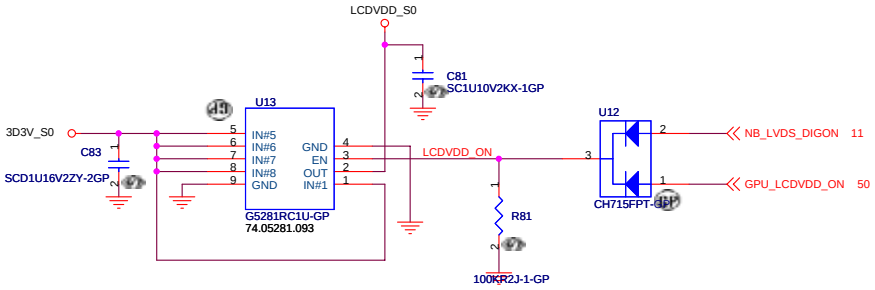




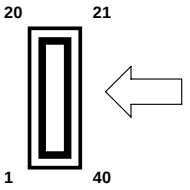


CAMERA POWER





TOP VIEW



<Variant Name>

蜂創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN/CAMERA**

Size	Document Number	Rev
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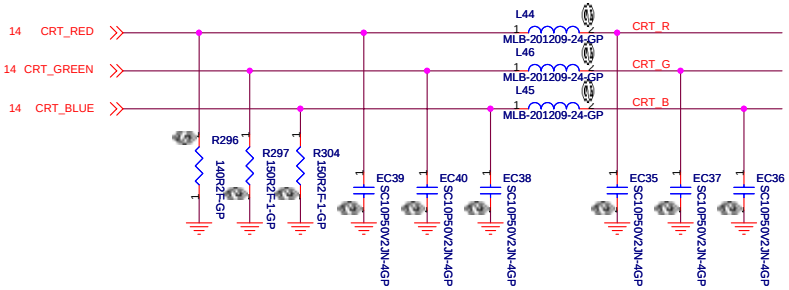
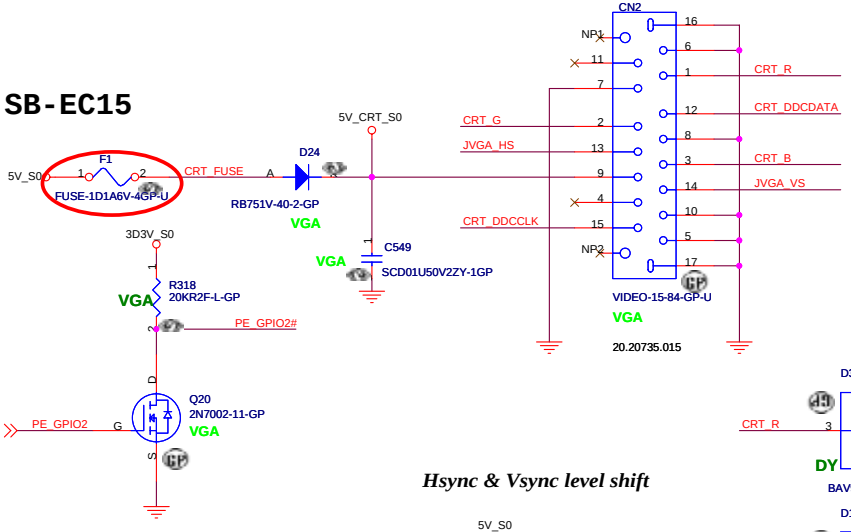
CRT I/F & CONNECTOR

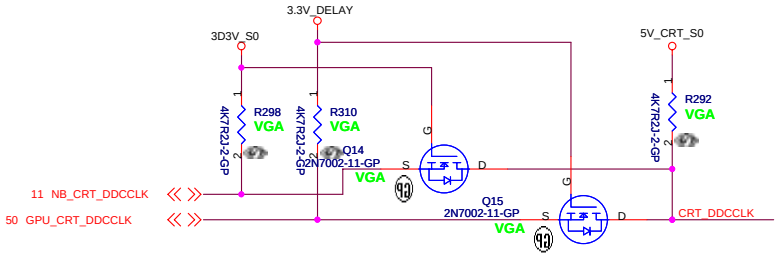
Layout Note:
Place these resistors close to the CRT-out connector

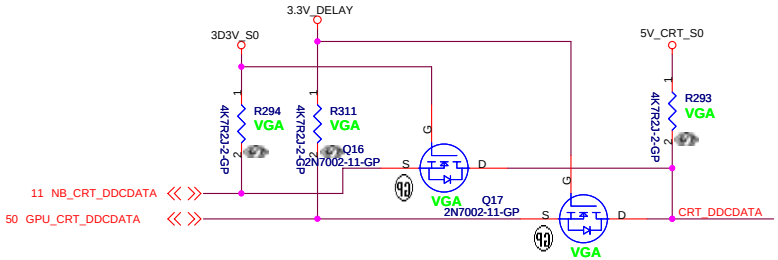


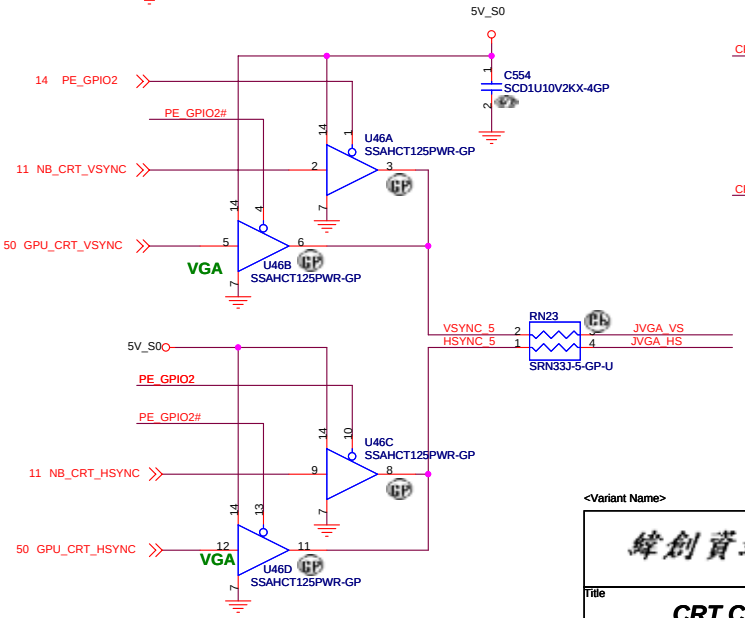
SB-EC15

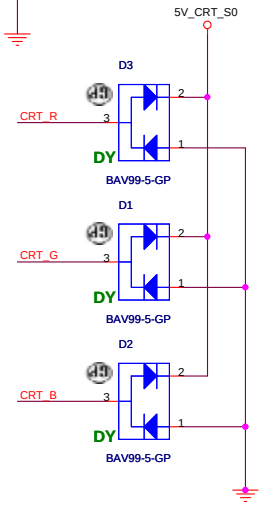


Hsync & Vsync level shift









<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN

Size	Document Number	Rev
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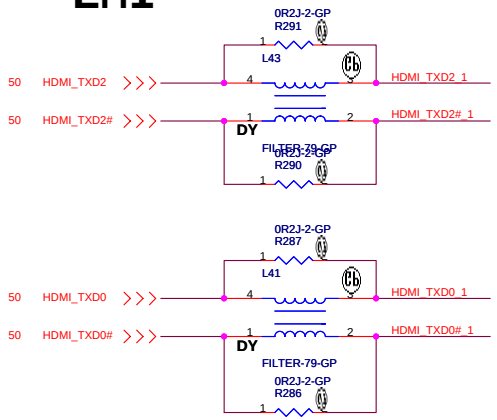
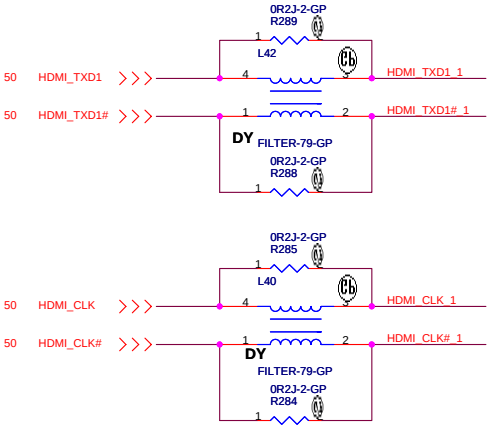
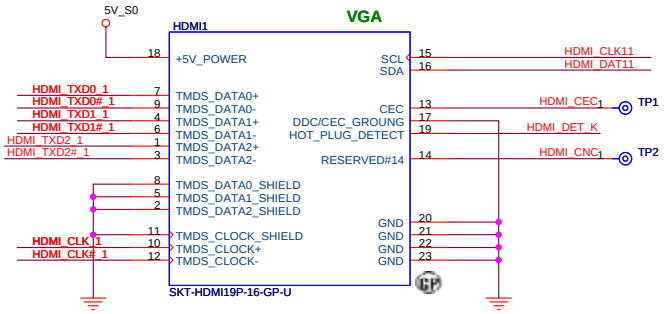
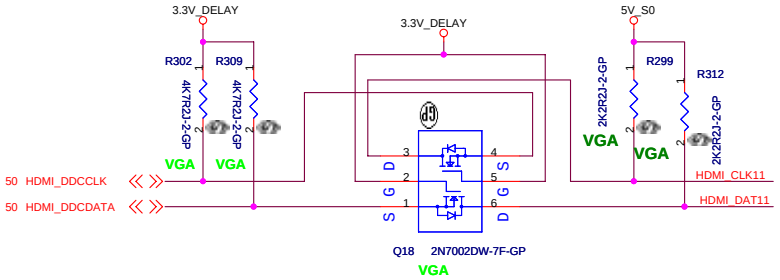
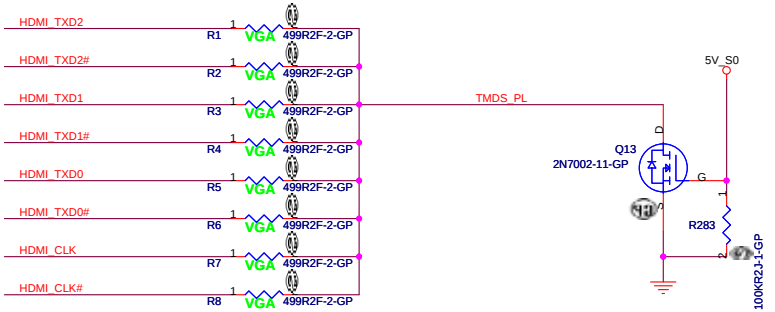
EMI

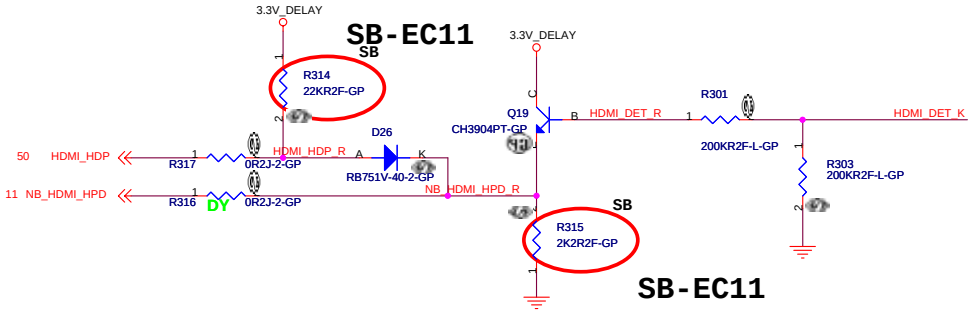












<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DVI & HDMI CONN

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SSID = S.B

SB700 Part 1 of 5

U74A

SB700-1-GP-U

SB-EC14

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET

PE_GPIO1 MXM POWER ENABLE H: Enable

PE_GPIO2 MODE SWITCH H: Enable

TMDS_HPD0 MXM HOT PLUG

20mil Width

Place R <100mils form pins T25,T24

200 ohm 2A

Symbol use (71.SB700.002)

BOM use AMD SB700 (71.SB700.006)

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_PCIE&PCI_(1/5)

Size: A3 | Document Number: X17 | Rev: SA

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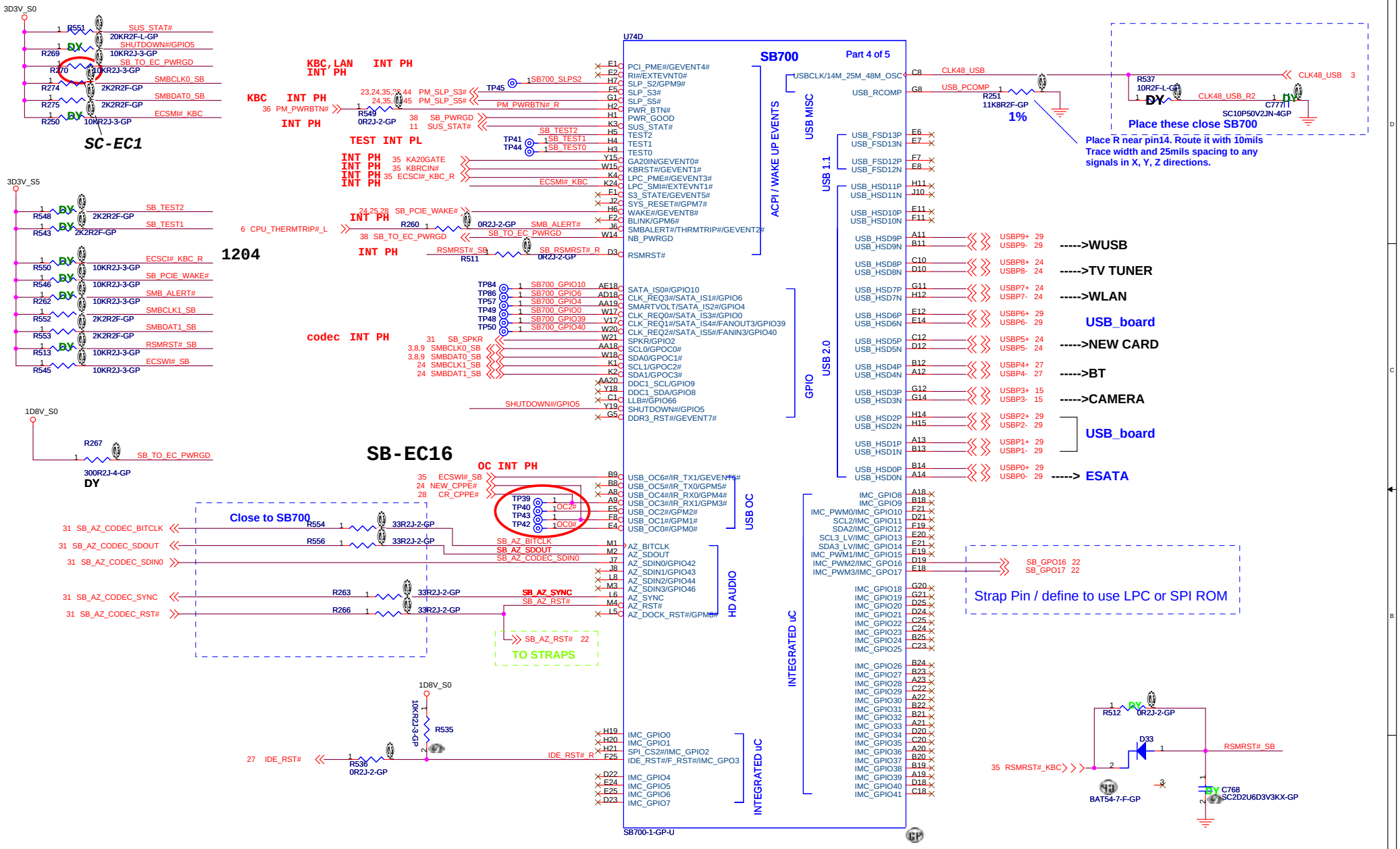
SC-EC1
SB-EC16
1204
SB700
Part 4 of 5
U74D
SB700-1-GP-U
KBC INT PH
INT PH
TEST INT PL
codec INT PH
OC INT PH
Close to SB700
TO STRAPS
Place these close SB700
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
----->WUSB
----->TV TUNER
----->WLAN
USB_board
----->NEW CARD
----->BT
----->CAMERA
USB_board
-----> ESATA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_USB&GPIO_(2/5)
X17
SA
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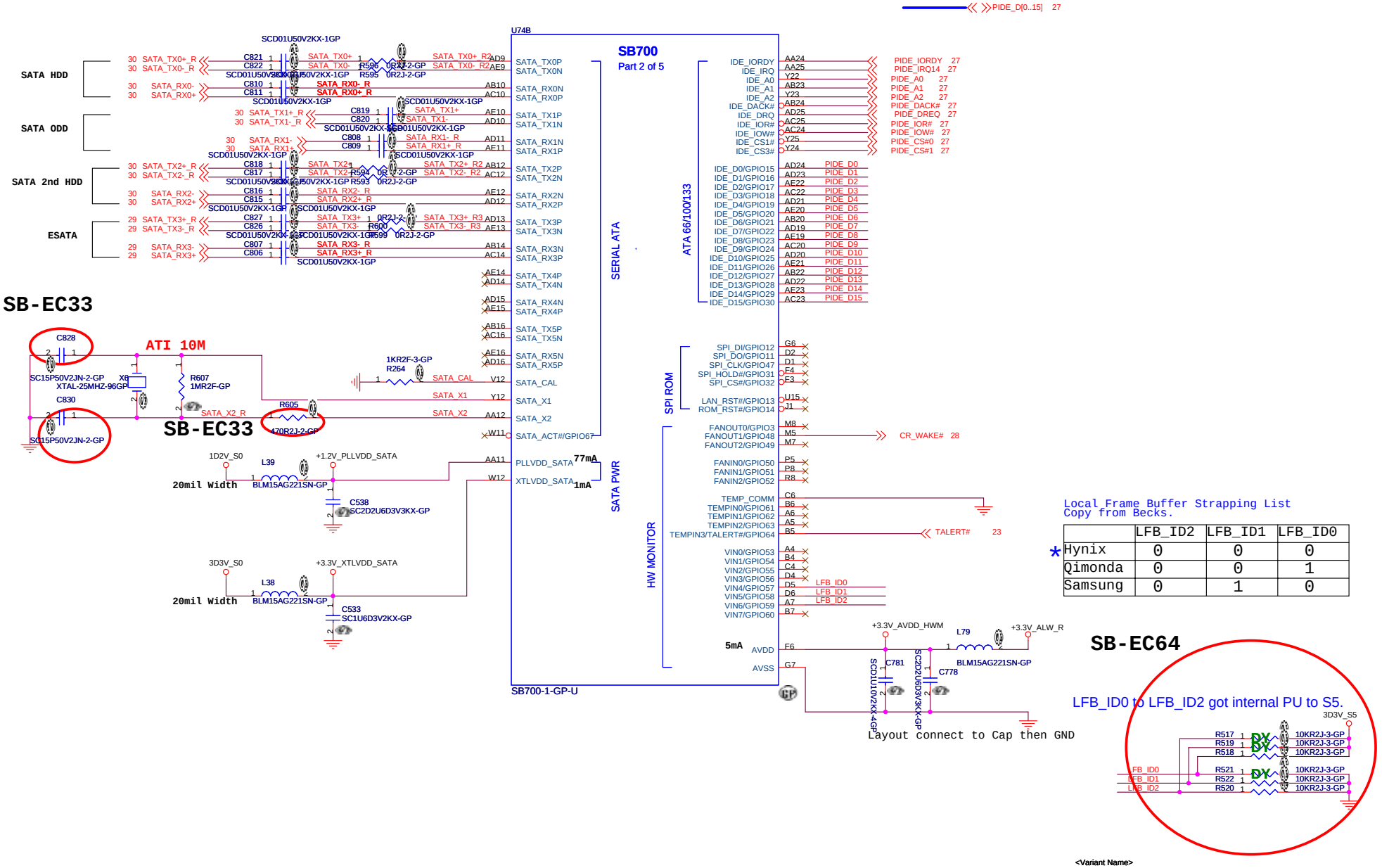
SB700
Part 2 of 5
U74B
SB700-1-GP-U
SERIAL ATA
SATA PWR
HW MONITOR
SPI ROM
ATA 66/100/133
SATA HDD
SATA ODD
SATA 2nd HDD
ESATA
SB-EC33
ATI 10M
SB-EC33
SB-EC64
PIDE_D[0..15] 27
Local Frame Buffer Strapping List
Copy from Becks.
LFB_ID2 LFB_ID1 LFB_ID0
Hynix 0 0 0
Qimonda 0 0 1
Samsung 0 1 0
LFB_ID0 to LFB_ID2 got internal PU to S5.
Layout connect to Cap then GND
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_SATA-IDE_(3/5)
X17
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SSID = S.B

U74C — SB700 Part 3 of 5

Use Flash I/O:+1.8V / IDE:+3.3V

POWER

Use Plane Shape for +3.3V_AVDD_USB

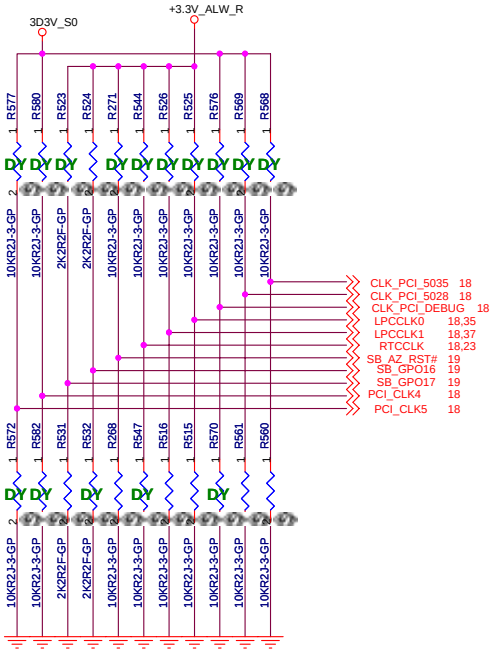
U74E — SB700 Part 5 of 5

GROUND

SB700-1-GP-U

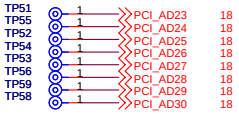
SSID = S.B

REQUIRED STRAPS



REQUIRED SYSTEM STRAPS

DEBUG STRAPS



	CLK_PCI_5035	CLK_PCI_5028	CLK_PCI_DEBUG	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ATi-SB700_STRAPPING_(5/5)*

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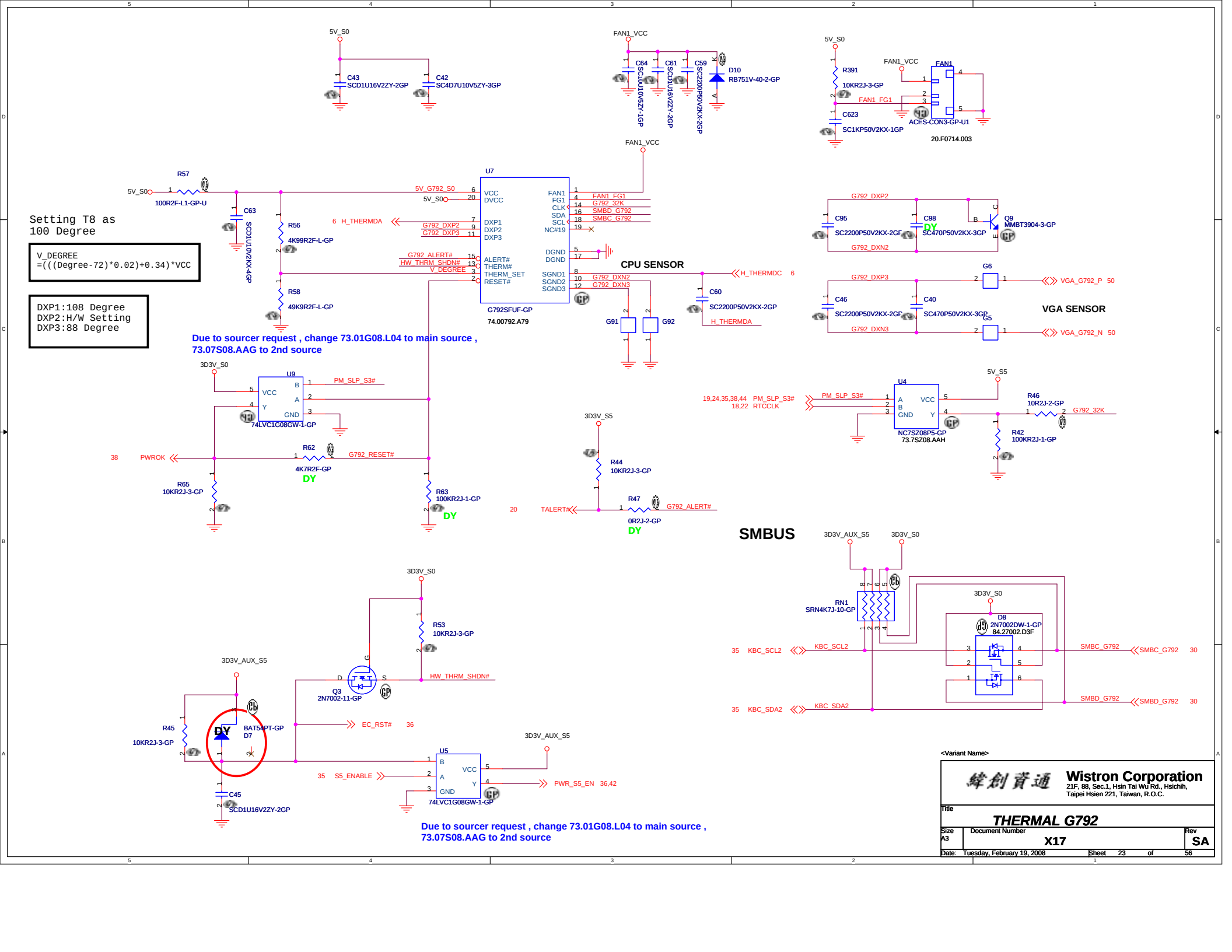
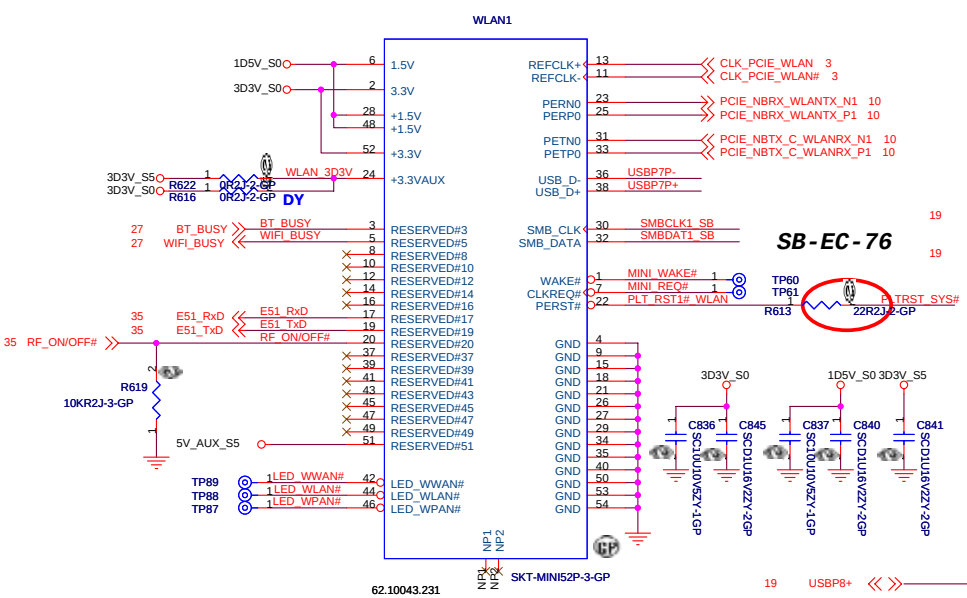
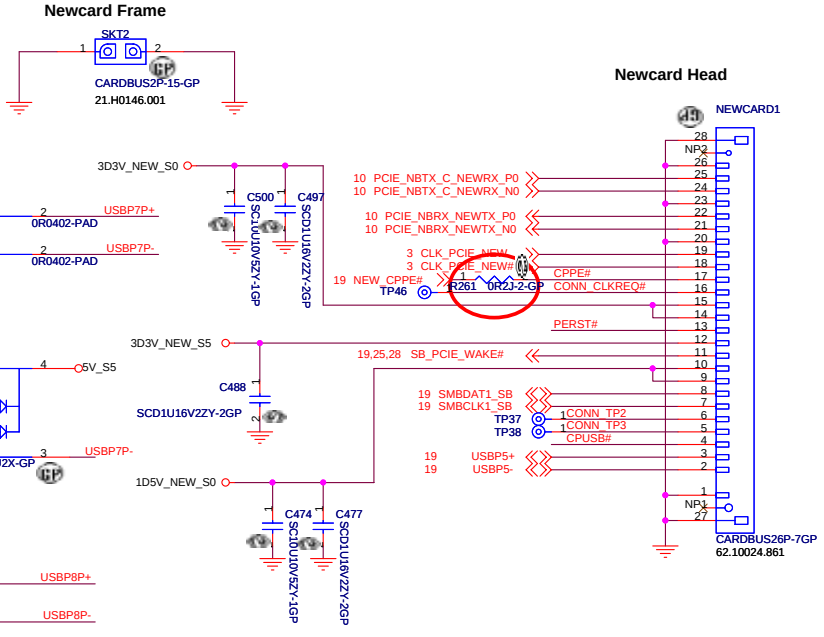

Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
CPU SENSOR
VGA SENSOR
SMBUS
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
THERMAL G792
X17
SA
Tuesday, February 19, 2008

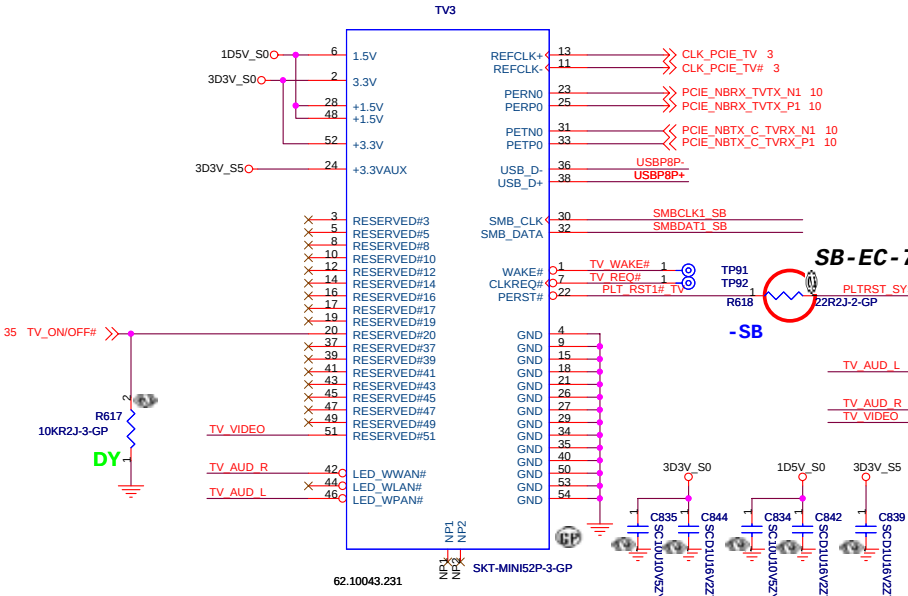
WLAN Connector

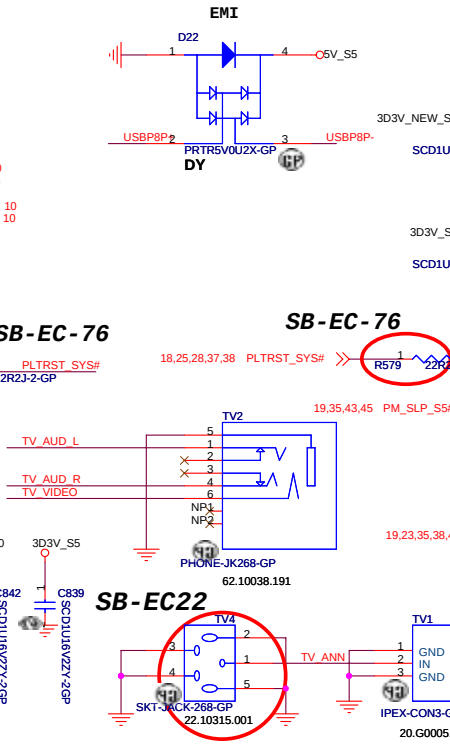


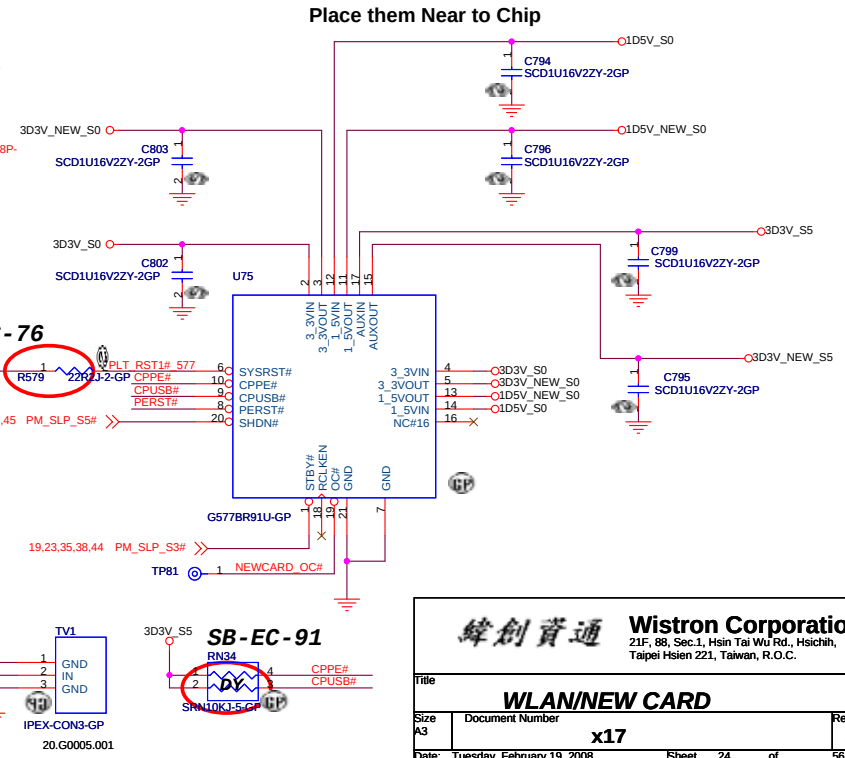
NEWCARD Connector



TV TUNER Connector







蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WLAN/NEW CARD**

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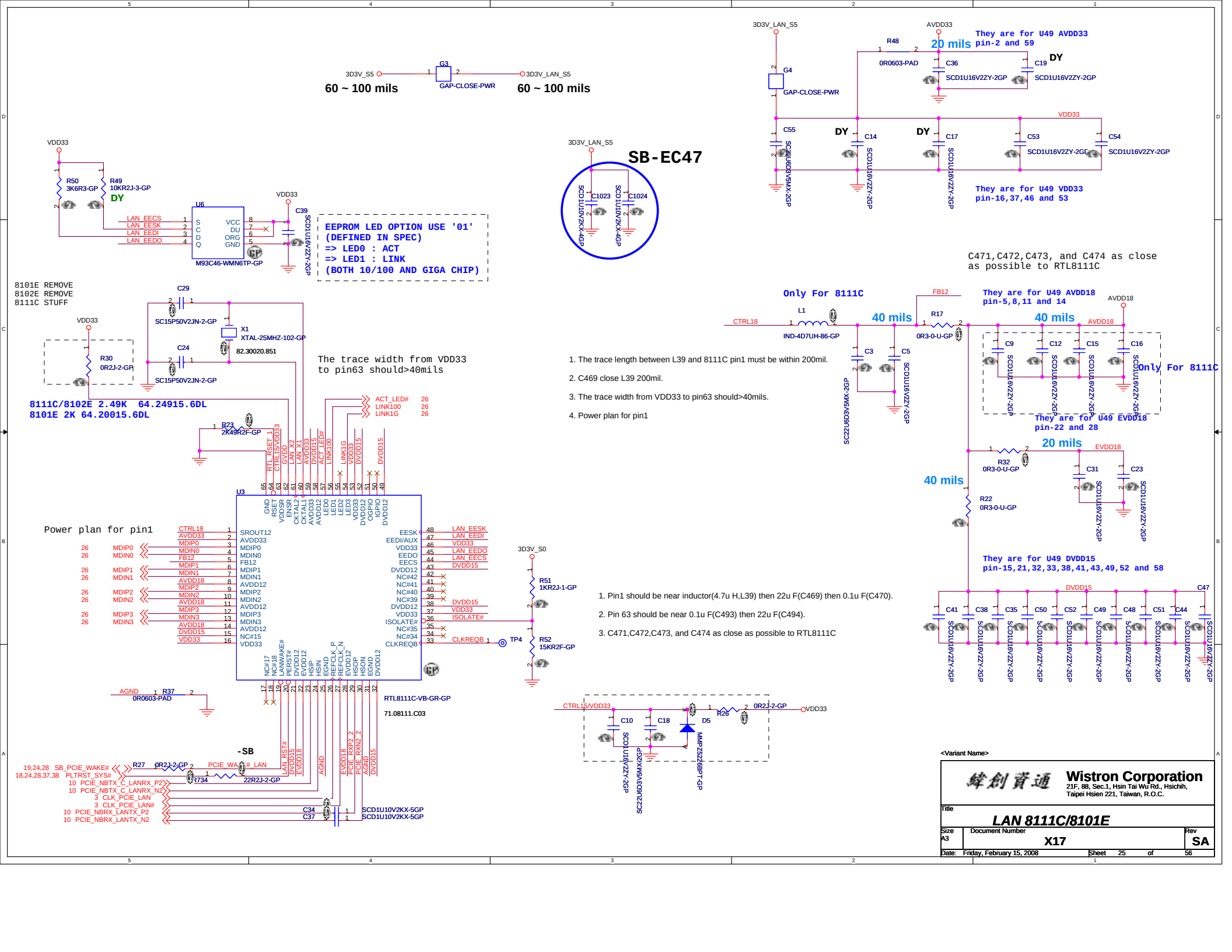
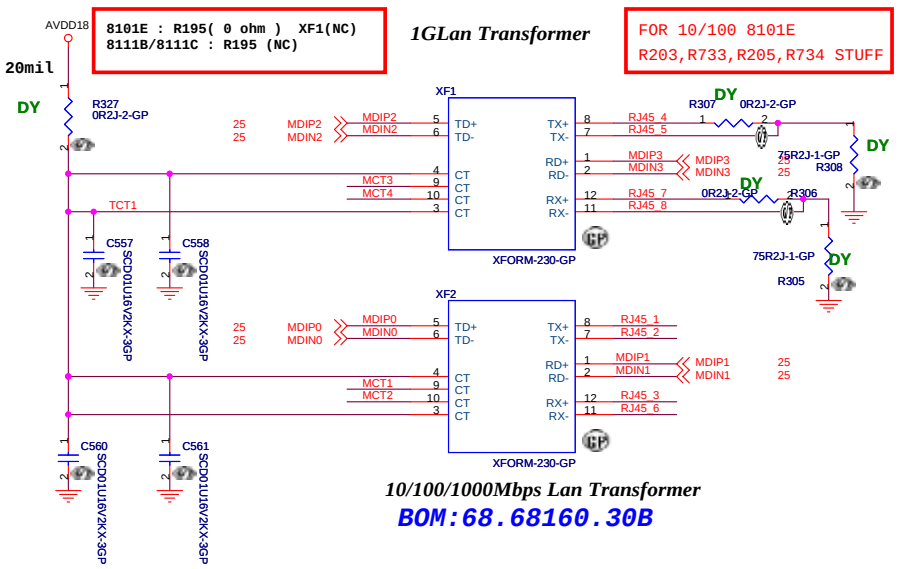

3D3V_S5
G3
3D3V_LAN_S5
60 ~ 100 mils
GAP-CLOSE-PWR
60 ~ 100 mils
3D3V_LAN_S5
AVDD33
They are for U49 AVDD33
pin-2 and 59
20 mils
R48
0R0603-PAD
C36
SCD1U16V2ZY-2GP
C19
DY
SCD1U16V2ZY-2GP
G4
GAP-CLOSE-PWR
VDD33
C55
SCD1U6D3V5MX-2GP
DY
C14
SCD1U16V2ZY-2GP
DY
C17
SCD1U16V2ZY-2GP
C53
SCD1U16V2ZY-2GP
C54
SCD1U16V2ZY-2GP
They are for U49 VDD33
pin-16,37,46 and 53
VDD33
R50
3K6R3-GP
R49
10KR2J-3-GP
DY
LAN_EECS
LAN_EESK
LAN_EEDI
LAN_EEDO
U6
S
C
D
Q
VCC
DU
ORG
GND
M93C46-WMN6TP-GP
VDD33
C39
SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
3D3V_LAN_S5
SB-EC47
C1023
SCD1U10V2KX-4GP
C1024
SCD1U10V2KX-4GP
C471,C472,C473, and C474 as close
as possible to RTL8111C
8101E REMOVE
8102E REMOVE
8111C STUFF
C29
SC15P50V2JN-2GP
VDD33
X1
XTAL-25MHZ-102-GP
82.30020.851
C24
SC15P50V2JN-2GP
R30
0R2J-2-GP
The trace width from VDD33
to pin63 should>40mils
8111C/8102E 2.49K 64.24915.6DL
8101E 2K 64.20015.6DL
R23
2K49R2F-GP
ACT_LED#
LINK100
LINK1G
RTL_RESET_1
CTRL15/VDD33
GVDD
LAN_X2
LAN_X1
AVDD33
DVDD15
ACT_LED#
LINK100
LINK1G
VDD33
DVDD15
DVDD15
U3
GND
RSET
VDDSR
ENSR
CKTAL2
CKTAL1
AVDD33
AVDD12
LED0
LED1
LED2
LED3
VDD33
DVDD12
OGPIO
IGPIO
DVDD12
Power plan for pin1
CTRL18
AVDD33
MDIP0
MDIN0
FB12
MDIP1
MDIN1
AVDD18
MDIP2
MDIN2
AVDD18
MDIP3
MDIN3
AVDD18
DVDD15
VDD33
SROUT12
AVDD33
MDIP0
MDIN0
FB12
MDIP1
MDIN1
AVDD12
MDIP2
MDIN2
AVDD12
MDIP3
MDIN3
AVDD12
NC#15
VDD33
EESK
EEDI/AUX
VDD33
EEDO
EECS
DVDD12
NC#42
NC#41
NC#40
NC#39
DVDD12
VDD33
ISOLATE#
NC#35
NC#34
CLKREQB
LAN_EESK
LAN_EEDI
VDD33
LAN_EEDO
LAN_EECS
DVDD15
DVDD15
VDD33
ISOLATE#
CLKREQB
TP4
3D3V_S0
R51
1KR2J-1-GP
R52
15KR2F-GP
NC#17
NC#18
LANWAKE#
PERST#
DVDD12
EVDD12
HSIP
HSIN
EGND
REFCLK_P
REFCLK_N
EVDD12
HSOP
HSON
EGND
DVDD12
AGND
R37
0R0603-PAD
RTL8111C-VB-GR-GP
71.08111.C03
-SB
19,24,28 SB_PCIE_WAKE#
18,24,28,37,38 PLTRST_SYS#
10 PCIE_NBTX_C_LANRX_P2
10 PCIE_NBTX_C_LANRX_N2
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
10 PCIE_NBRX_LANTX_P2
10 PCIE_NBRX_LANTX_N2
R27
0R2J-2-GP
PCIE_WAKE#_LAN
2734
22R2J-2-GP
LAN_RST#
DVDD15
EVDD18
AGND
EVDD18
PCIE_RXP2_2
PCIE_RXN2_2
AGND
DVDD15
C34
C37
SCD1U10V2KX-5GP
SCD1U10V2KX-5GP
1. The trace length between L39 and 8111C pin1 must be within 200mil.
2. C469 close L39 200mil.
3. The trace width from VDD33 to pin63 should>40mils.
4. Power plan for pin1
1. Pin1 should be near inductor(4.7u H,L39) then 22u F(C469) then 0.1u F(C470).
2. Pin 63 should be near 0.1u F(C493) then 22u F(C494).
3. C471,C472,C473, and C474 as close as possible to RTL8111C
Only For 8111C
CTRL18
L1
IND-4D7UH-86-GP
40 mils
FB12
R17
0R3-0-U-GP
They are for U49 AVDD18
pin-5,8,11 and 14
AVDD18
40 mils
AVDD18
C9
SCD1U16V2ZY-2GP
C12
SCD1U16V2ZY-2GP
C15
SCD1U16V2ZY-2GP
C16
SCD1U16V2ZY-2GP
Only For 8111C
C3
SC22U6D3V5MX-2GP
C5
SCD1U16V2ZY-2GP
They are for U49 EVDD18
pin-22 and 28
20 mils
EVDD18
R32
0R3-0-U-GP
C31
SCD1U16V2ZY-2GP
C23
SCD1U16V2ZY-2GP
40 mils
R22
0R3-0-U-GP
They are for U49 DVDD15
pin-15,21,32,33,38,41,43,49,52 and 58
DVDD15
C47
C41
C38
C35
C50
C52
C49
C48
C51
C44
SCD1U16V2ZY-2GP
CTRL15/VDD33
C10
SCD1U16V2ZY-2GP
C18
SC22U6D3V5MX-2GP
D5
MMPZ5226BPT-GP
R26
0R2J-2-GP
VDD33
<Variant Name>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN 8111C/8101E
Size
A3
Document Number
X17
Rev
SA
Date: Friday, February 15, 2008
Sheet 25 of 56

8101E : R195(0 ohm) XF1(NC)
8111B/8111C : R195 (NC)

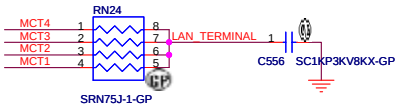
1GLan Transformer

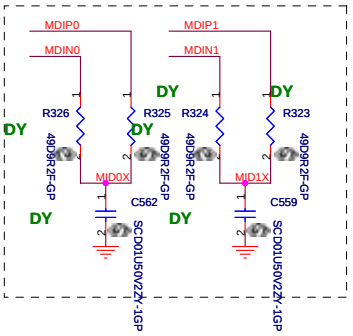
FOR 10/100 8101E
R203,R733,R205,R734 STUFF



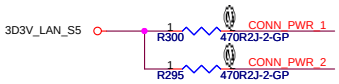
10/100/1000Mbps Lan Transformer

BOM:68.68160.30B

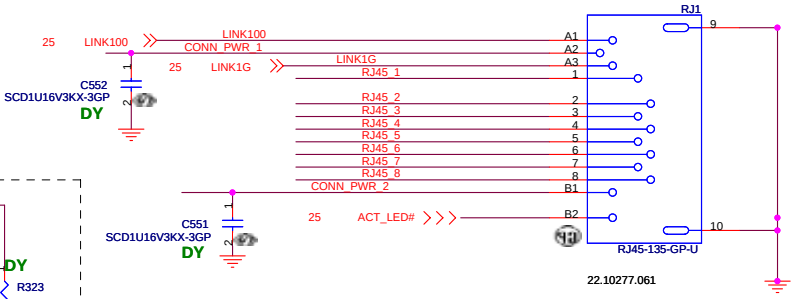




GIGA no need it at all , 10/100 keep



Off : Link 10 Mbps
Green : Link 100 Mbps
Orange : Link 1000 Mbps



Green : Link up
Blinking : TX/RX activity

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN Connector***

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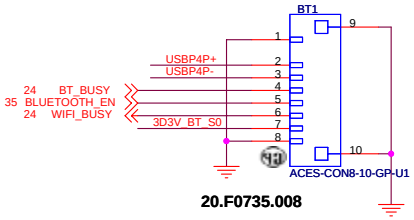
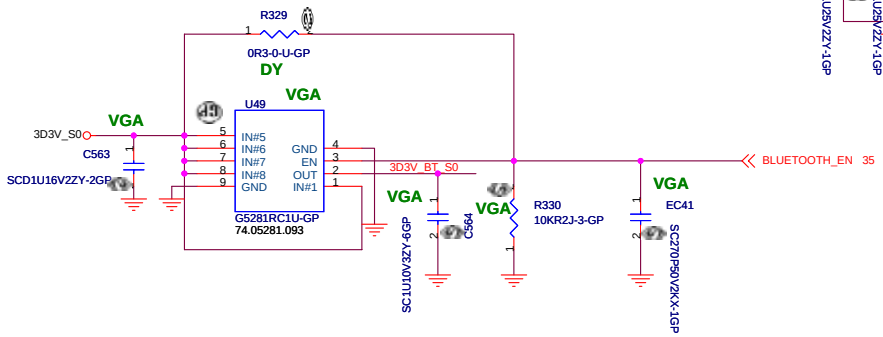
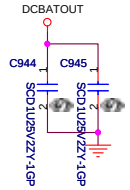
HYPER FLASH

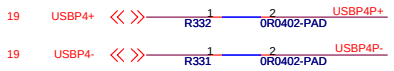
Bluetooth

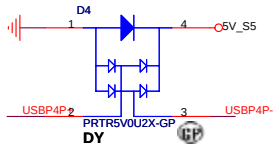




For HF reference different moat

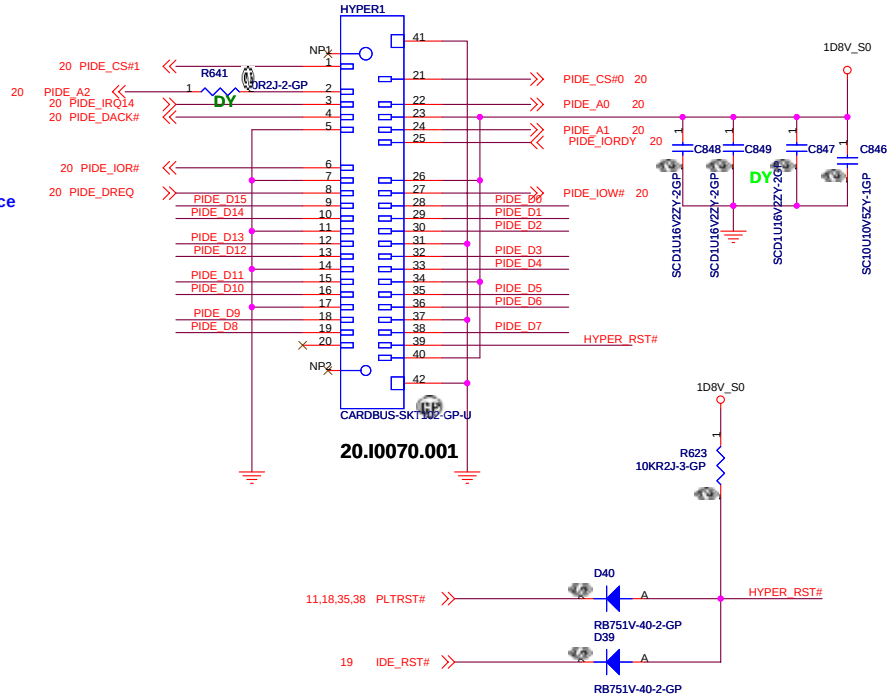






EMI

20 PIDE_D[0..15]



<Variant Name>

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HYPER FLASH/BT

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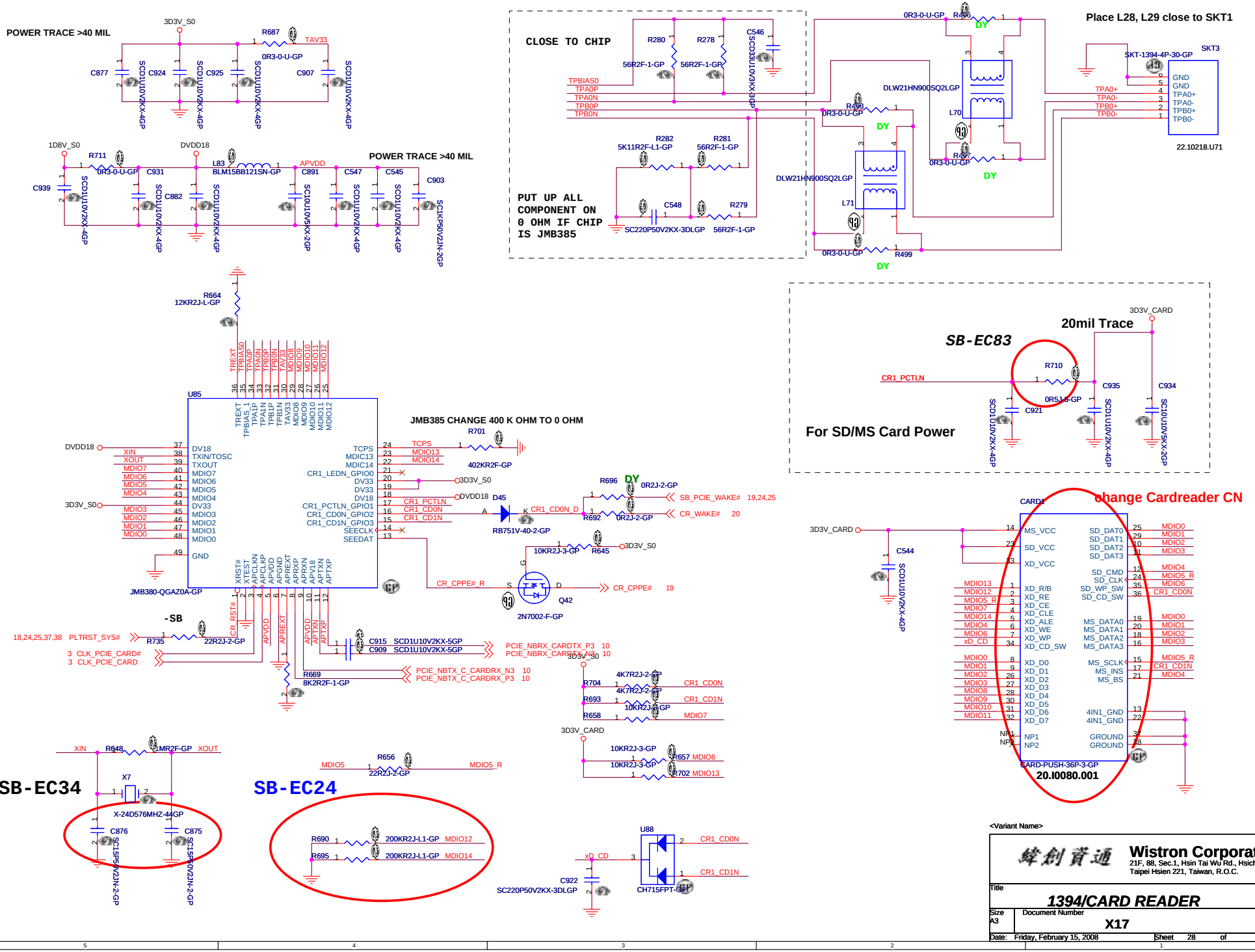
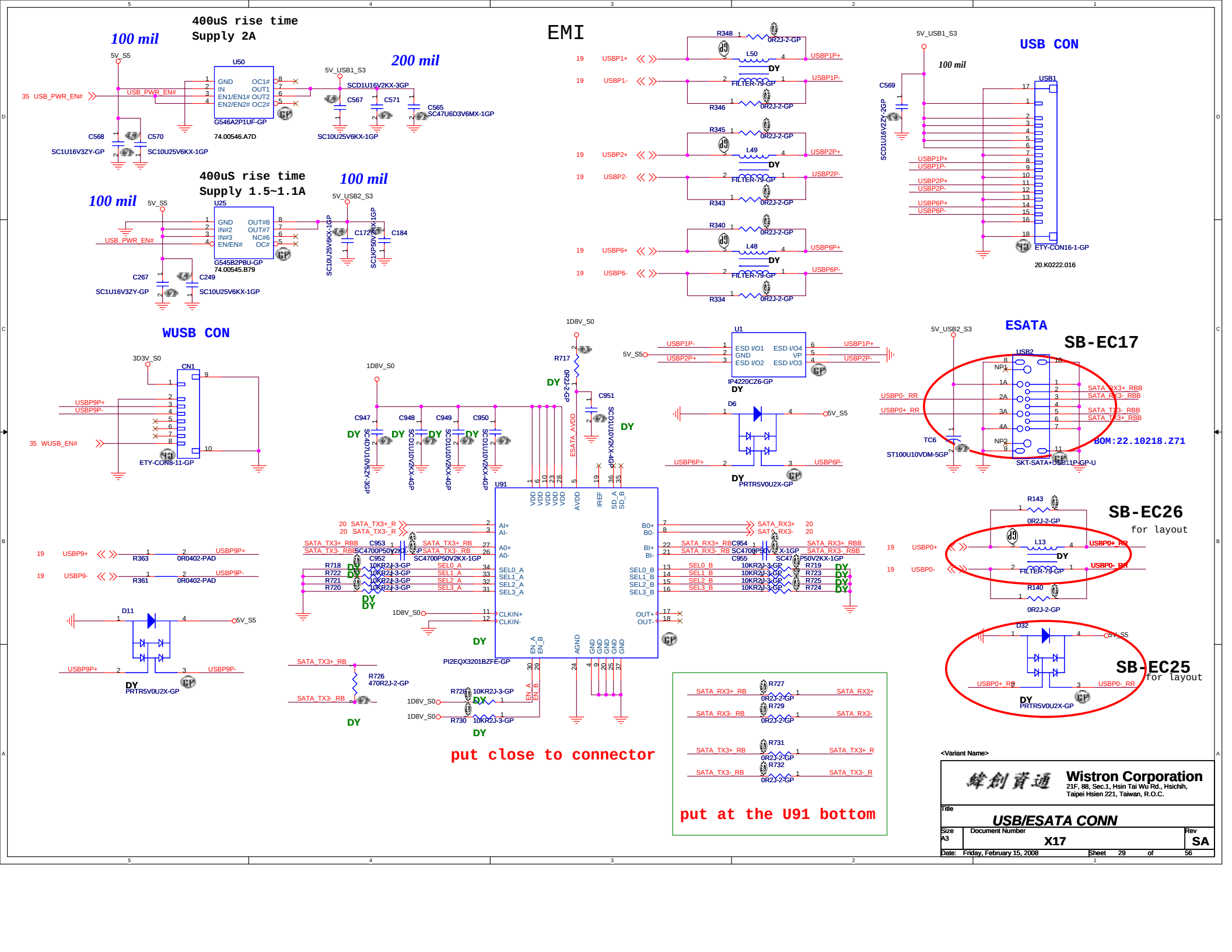
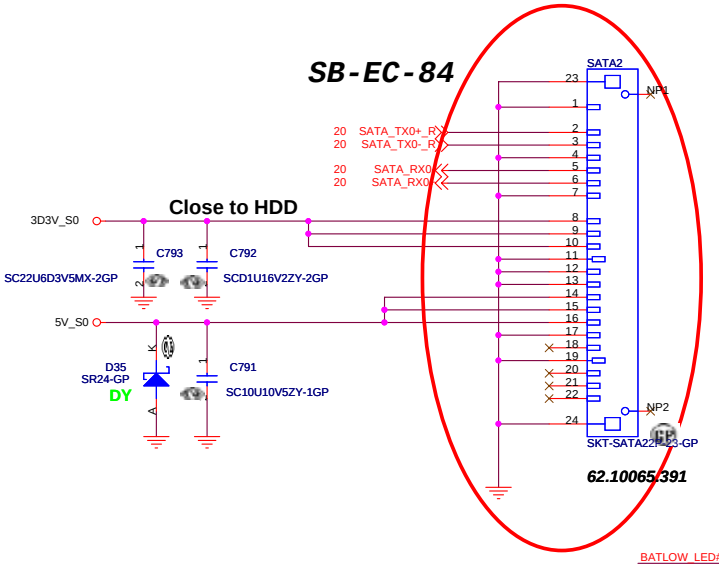
Date: Friday, February 15, 2008 Sheet 27 of 56

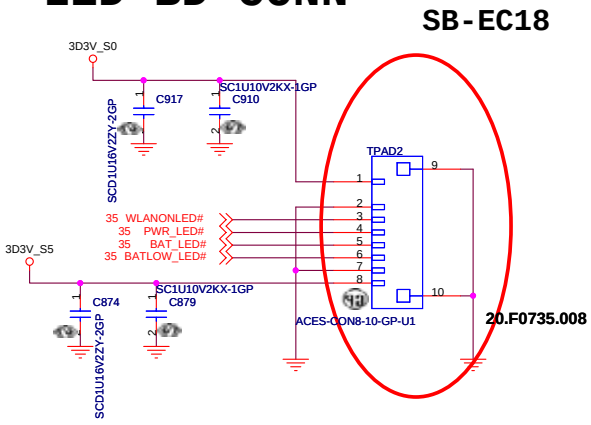

POWER TRACE >40 MIL
3D3V_S0
R687
0R3-0-U-GP
TAV33
C877
C924
C925
C907
SCD1U10V2KX-4GP
1D8V_S0
DVDD18
R711
0R3-0-U-GP
L83
BLM15BB121SN-GP
APVDD
C939
C931
C882
C891
C547
C545
C903
SC10U10V5KX-2GP
SCK150P50V2JN-2GP
CLOSE TO CHIP
R280
R278
C546
56R2F-1-GP
SCD33U10V3KX-3GP
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
R282
5K11R2F-L1-GP
R281
56R2F-1-GP
C548
R279
SC220P50V2KX-3DLGP
PUT UP ALL COMPONENT ON 0 OHM IF CHIP IS JMB385
0R3-0-U-GP
R496
DY
R498
R497
R499
DLW21HN900SQ2LGP
L70
L71
Place L28, L29 close to SKT1
SKT-1394-4P-30-GP
SKT3
GND
TPA0+
TPA0-
TPB0+
TPB0-
22.10218.U71
R664
12KR2J-L-GP
U85
JMB380-QGAZ0A-GP
JMB385 CHANGE 400 K OHM TO 0 OHM
R701
402KR2F-GP
DV18
TXIN/TOSC
TXOUT
MDIO7
MDIO6
MDIO5
MDIO4
MDIO3
MDIO2
MDIO1
MDIO0
GND
TCPS
MDIC13
MDIC14
CR1_LEDN_GPIO0
CR1_PCTLN_GPIO1
CR1_CD0N_GPIO2
CR1_CD1N_GPIO3
SEECLK
SEEDAT
CR1_PCTLN
CR1_CD0N
CR1_CD1N
D45
RB751V-40-2-GP
R696
0R2J-2-GP
R692
SB_PCIE_WAKE# 19,24,25
CR_WAKE# 20
R645
10KR2J-3-GP
Q42
2N7002-F-GP
CR_CPPE# 19
CR_CPPE#_R
-SB
18,24,25,37,38 PLTRST_SYS#
R735
22R2J-2-GP
3 CLK_PCIE_CARD#
3 CLK_PCIE_CARD
C915 SCD1U10V2KX-5GP
C909 SCD1U10V2KX-5GP
PCIE_NBRX_CARDTX_P3 10
PCIE_NBRX_CARDTX_N3 10
R669
8K2R2F-1-GP
PCIE_NBTX_C_CARDRX_N3 10
PCIE_NBTX_C_CARDRX_P3 10
R704
4K7R2J-2-GP
R693
4K7R2J-2-GP
R658
10KR2J-3-GP
CR1_CD0N
CR1_CD1N
MDIO7
3D3V_CARD
10KR2J-3-GP
R657 MDIO6
R702 MDIO13
SB-EC34
XIN
R648
2MR2F-GP
XOUT
X7
X-24D576MHZ-44GP
C876
C875
SC15P50V2JN-2GP
SB-EC24
MDIO5
R656
22R2J-2-GP
MDIO5_R
R690
200KR2J-L1-GP
MDIO12
R695
200KR2J-L1-GP
MDIO14
U88
xD_CD
C922
SC220P50V2KX-3DLGP
CH715FPT-GP
SB-EC83
20mil Trace
3D3V_CARD
CR1_PCTLN
R710
0R5J-5-GP
C921
C935
C934
SCD1U10V2KX-4GP
SC10U10V5KX-2GP
For SD/MS Card Power
change Cardreader CN
CARD1
C544
MS_VCC
SD_VCC
XD_VCC
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_CD_SW
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
NP1
NP2
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_WP_SW
SD_CD_SW
MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3
MS_SCLK
MS_INS
MS_BS
4IN1_GND
GROUND
CARD-PUSH-36P-3-GP
20.I0080.001
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1394/CARD READER
Size A3
Document Number
X17
Rev SA
Date: Friday, February 15, 2008
Sheet 28 of 56


400uS rise time
Supply 2A
100 mil
200 mil
5V_S5
U50
GND
IN
EN1/EN1#
EN2/EN2#
OC1#
OUT1
OUT2
OC2#
USB_PWR_EN#
35 USB_PWR_EN#
G546A2P1UF-GP
74.00546.A7D
5V_USB1_S3
SCD1U16V2KX-3GP
C567
C571
C565
SC47U6D3V6MX-1GP
SC10U25V6KX-1GP
C568
C570
SC1U16V3ZY-GP
SC10U25V6KX-1GP
400uS rise time
Supply 1.5~1.1A
100 mil
100 mil
5V_S5
U25
GND
IN#2
IN#3
EN/EN#
OUT#8
OUT#7
NC#6
OC#
USB_PWR_EN#
G545B2P8U-GP
74.00545.B79
5V_USB2_S3
SC10U25V6KX-1GP
C172
SC1K250V2KX-1GP
C184
C267
C249
SC1U16V3ZY-GP
SC10U25V6KX-1GP
EMI
R348
0R2J-2-GP
L50
DY
FILTER-79-GP
R346
R345
L49
R343
R340
L48
R334
19 USBP1+
19 USBP1-
19 USBP2+
19 USBP2-
19 USBP6+
19 USBP6-
USBP1P+
USBP1P-
USBP2P+
USBP2P-
USBP6P+
USBP6-
USB CON
5V_USB1_S3
100 mil
C569
SCD1U16V2ZY-2GP
USB1
USBP1P+
USBP1P-
USBP2P+
USBP2P-
USBP6P+
USBP6P-
ETY-CON16-1-GP
20.K0222.016
WUSB CON
3D3V_S0
CN1
USBP9P+
USBP9P-
35 WUSB_EN#
ETY-CON8-11-GP
1D8V_S0
R717
0R2J-2-GP
DY
C947
C948
C949
C950
C951
SCD1U10V2KX-4GP
SC1U10V2ZY-3GP
ESATA_AVDD
U91
VDD
AVDD
IREF
SD_A
SD_B
AI+
AI-
A0+
A0-
BI+
BI-
B0+
B0-
SEL0_A
SEL1_A
SEL2_A
SEL3_A
SEL0_B
SEL1_B
SEL2_B
SEL3_B
CLKIN+
CLKIN-
OUT+
OUT-
EN_A
EN_B
AGND
GND
PI2EQX3201BZFE-GP
SATA_TX3+_R
SATA_TX3-_R
SATA_TX3+_RBB
SATA_TX3-_RBB
SATA_RX3+_RBB
SATA_RX3-_RBB
SC4700P50V2KX-1GP
C952
C953
C954
C955
10KR2J-3-GP
R718
R722
R721
R720
R719
R723
R725
R724
R726
470R2J-2-GP
R728
R730
10KR2J-3-GP
1D8V_S0
USBP1P-
USBP2P-
5V_S5
U1
ESD I/O1
ESD I/O2
GND
ESD I/O4
ESD I/O3
VP
USBP1P+
USBP2P-
IP4220CZ6-GP
D6
USBP6P+
USBP6P-
PRTR5V0U2X-GP
ESATA
SB-EC17
5V_USB2_S3
USB2
NP1
NP2
1A
2A
3A
4A
USBP0- RR
USBP0+ RR
SATA_TX3+_RBB
SATA_TX3-_RBB
SATA_TX3-_RBB
SATA_TX3+_RBB
TC6
ST100U10VDM-5GP
SKT-SATA+USB11P-GP-U
BOM:22.10218.Z71
SB-EC26
for layout
R143
0R2J-2-GP
L13
FILTER-79-GP
R140
0R2J-2-GP
19 USBP0+
19 USBP0-
USBP0+_RR
USBP0-_RR
SB-EC25
for layout
D32
SATA_RX3+_RB
SATA_RX3-_RB
SATA_TX3+_RB
SATA_TX3-_RB
R727
R729
R731
R732
SATA_RX3+
SATA_RX3-
SATA_TX3+_R
SATA_TX3-_R
put close to connector
put at the U91 bottom
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB/ESATA CONN
Size
A3
Document Number
X17
Rev
SA
Date: Friday, February 15, 2008
Sheet 29 of 56

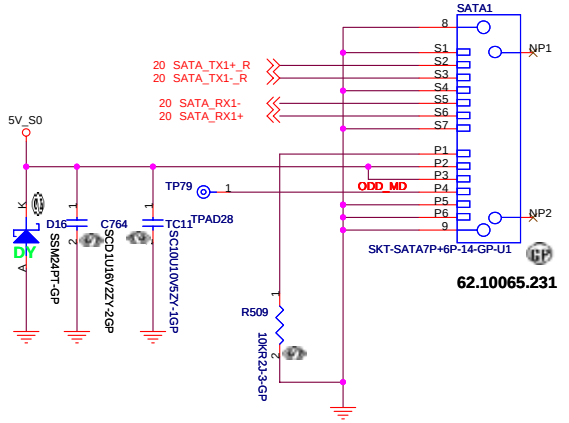
SATA HDD Connector

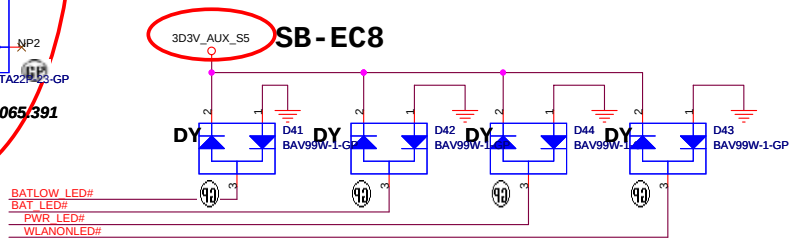


LED BD CONN

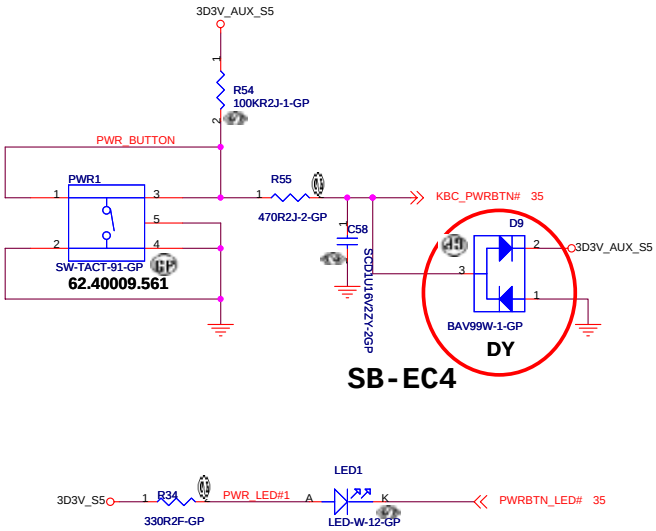


SATA ODD Connector

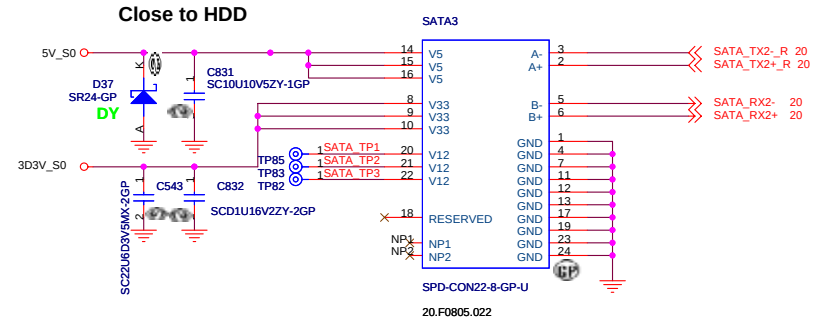




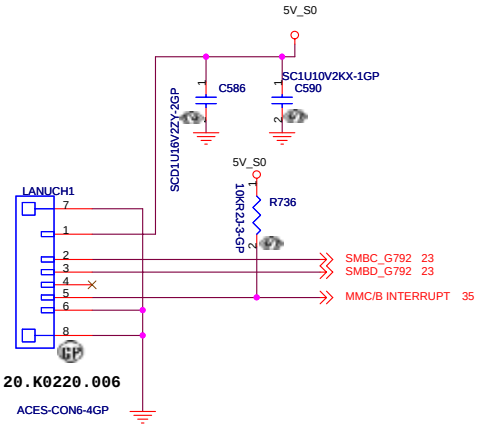
POWER BUTTON



SATA HDD2 Connector



MMC BD CONN



<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CDROM/LED/LAUNCH**

Size	Document Number	Rev
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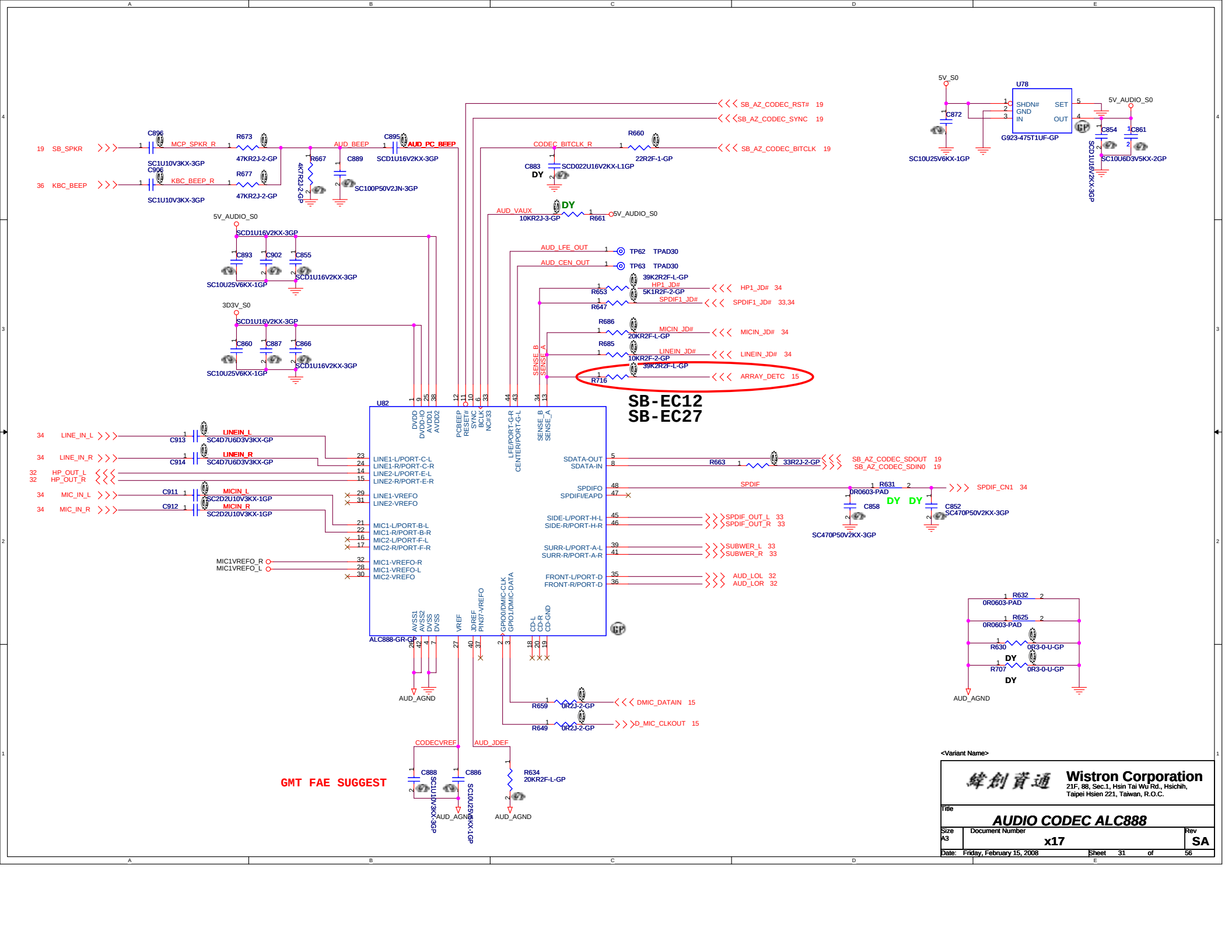
SB-EC12
SB-EC27
GMT FAE SUGGEST
U82
ALC888-GR-GP
U78
G923-475T1UF-GP
SB_AZ_CODEC_RST# 19
SB_AZ_CODEC_SYNC 19
SB_AZ_CODEC_BITCLK 19
SB_AZ_CODEC_SDOUT 19
SB_AZ_CODEC_SDIN0 19
HP1_JD# 34
SPDIF1_JD# 33,34
MICIN_JD# 34
LINEIN_JD# 34
ARRAY_DETC 15
SPDIF_CN1 34
DMIC_DATAIN 15
D_MIC_CLKOUT 15
5V_S0
5V_AUDIO_S0
3D3V_S0
AUD_AGND
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC ALC888
Size A3
Document Number x17
Rev SA
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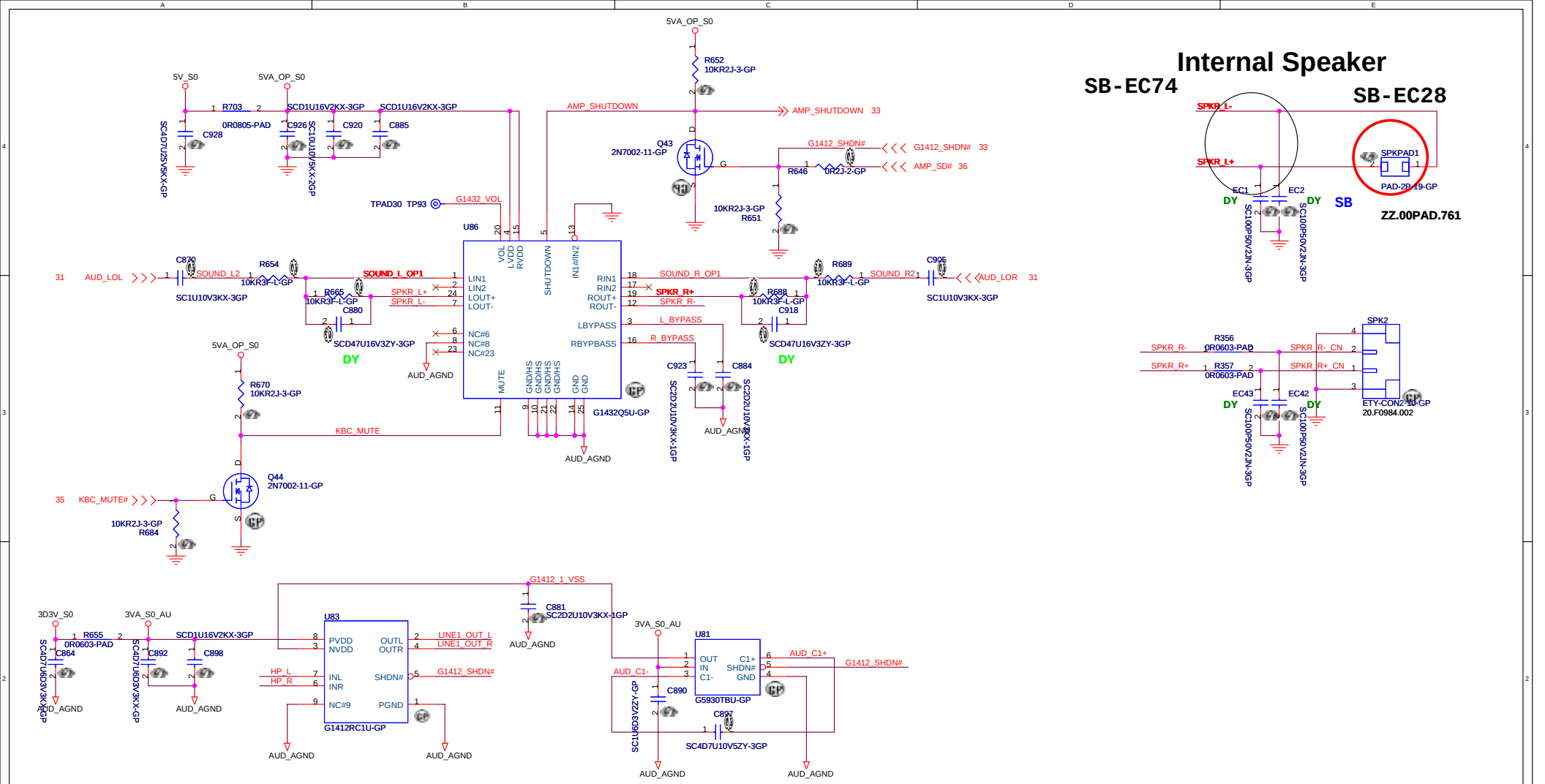
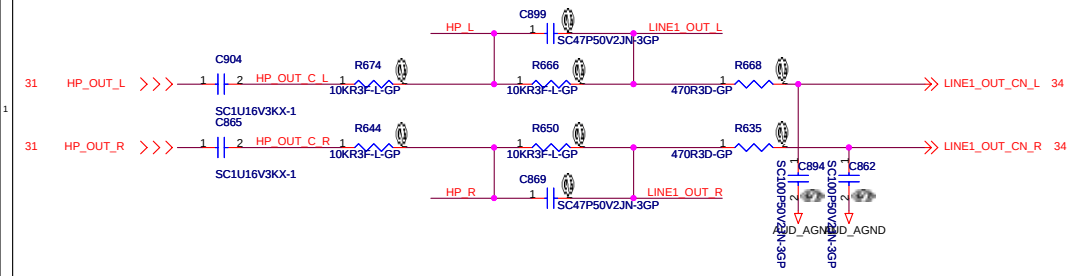


LINE Out



<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/Speaker**

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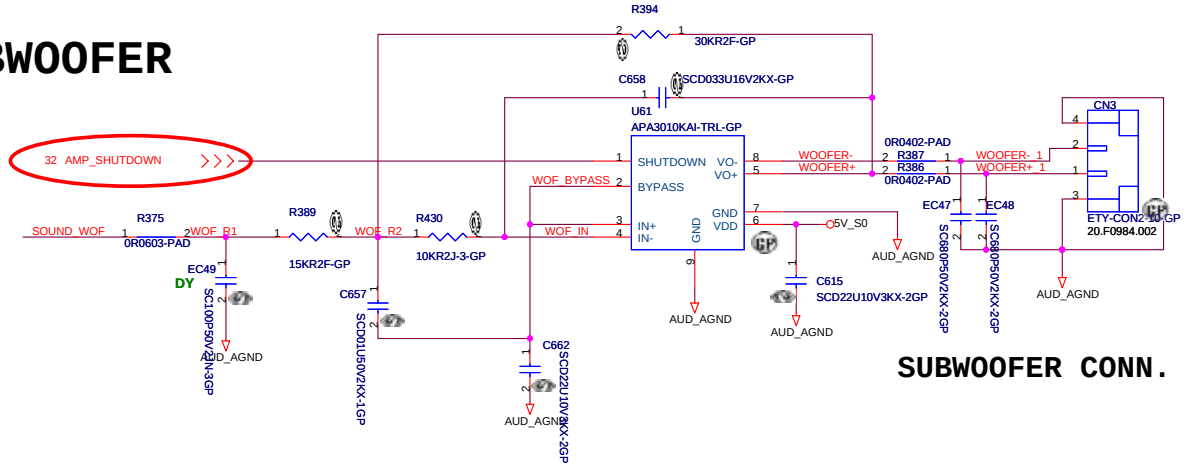
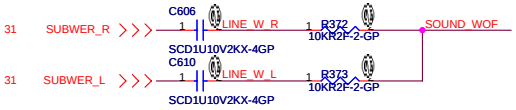
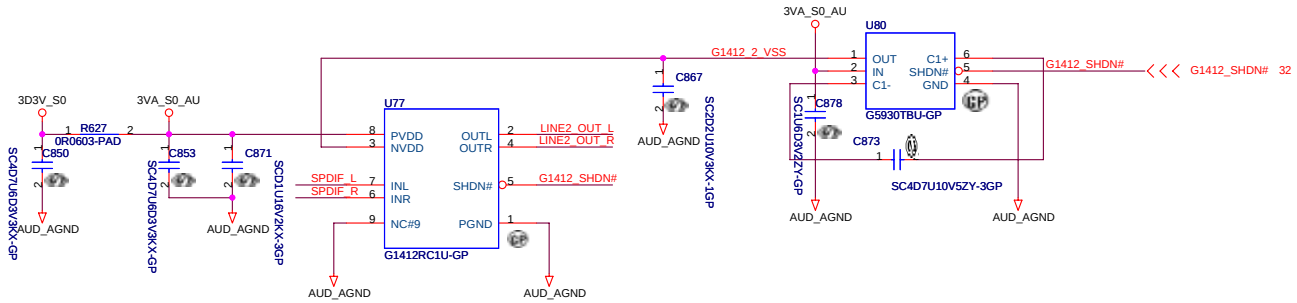
SUBWOOFER

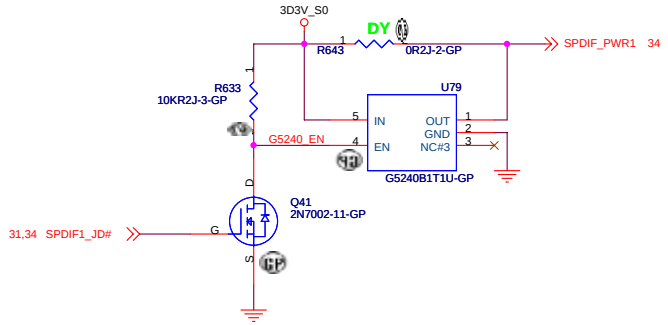
SB-EC10



SUBWOOFER CONN.

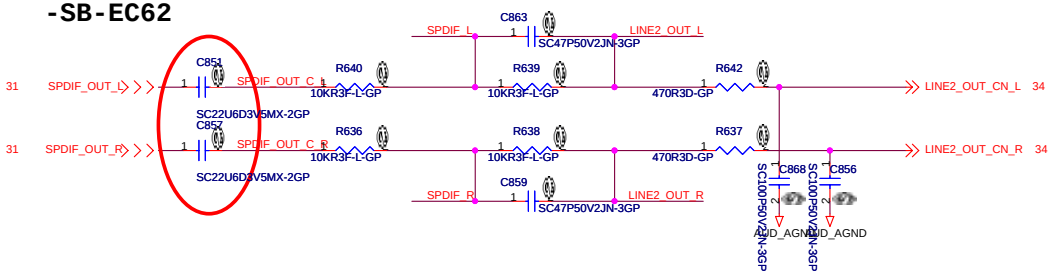






LINE2 Out

-SB-EC62



蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/Subwoofer**

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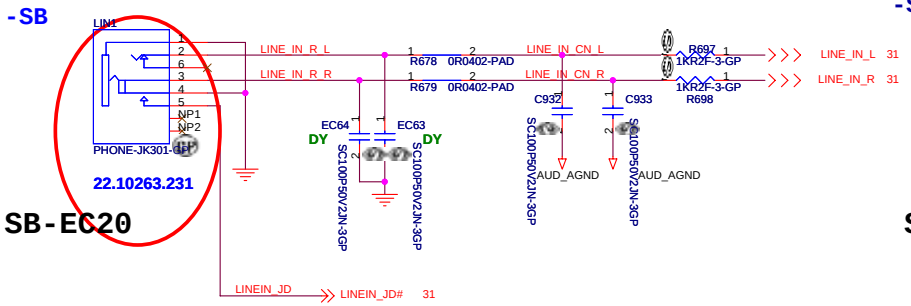
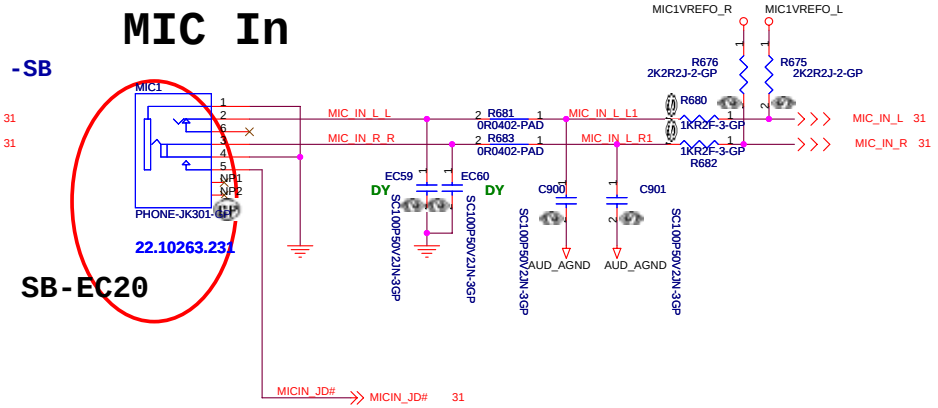
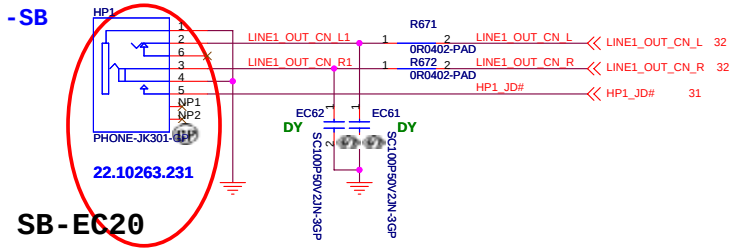
LINE In



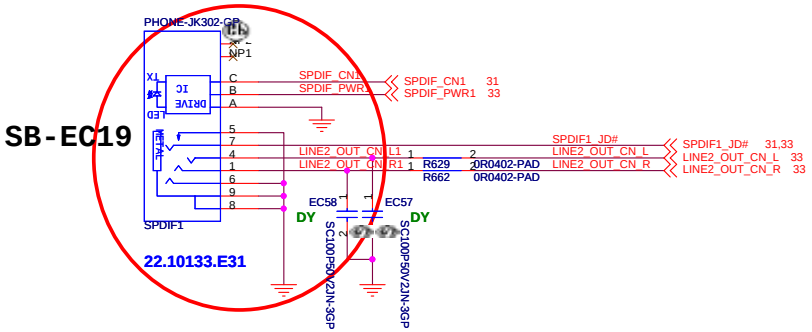
MIC In



Headphone / LINE1 OUT



SPDIF OUT / LINE2 OUT



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CONN/SUBWOOFER**

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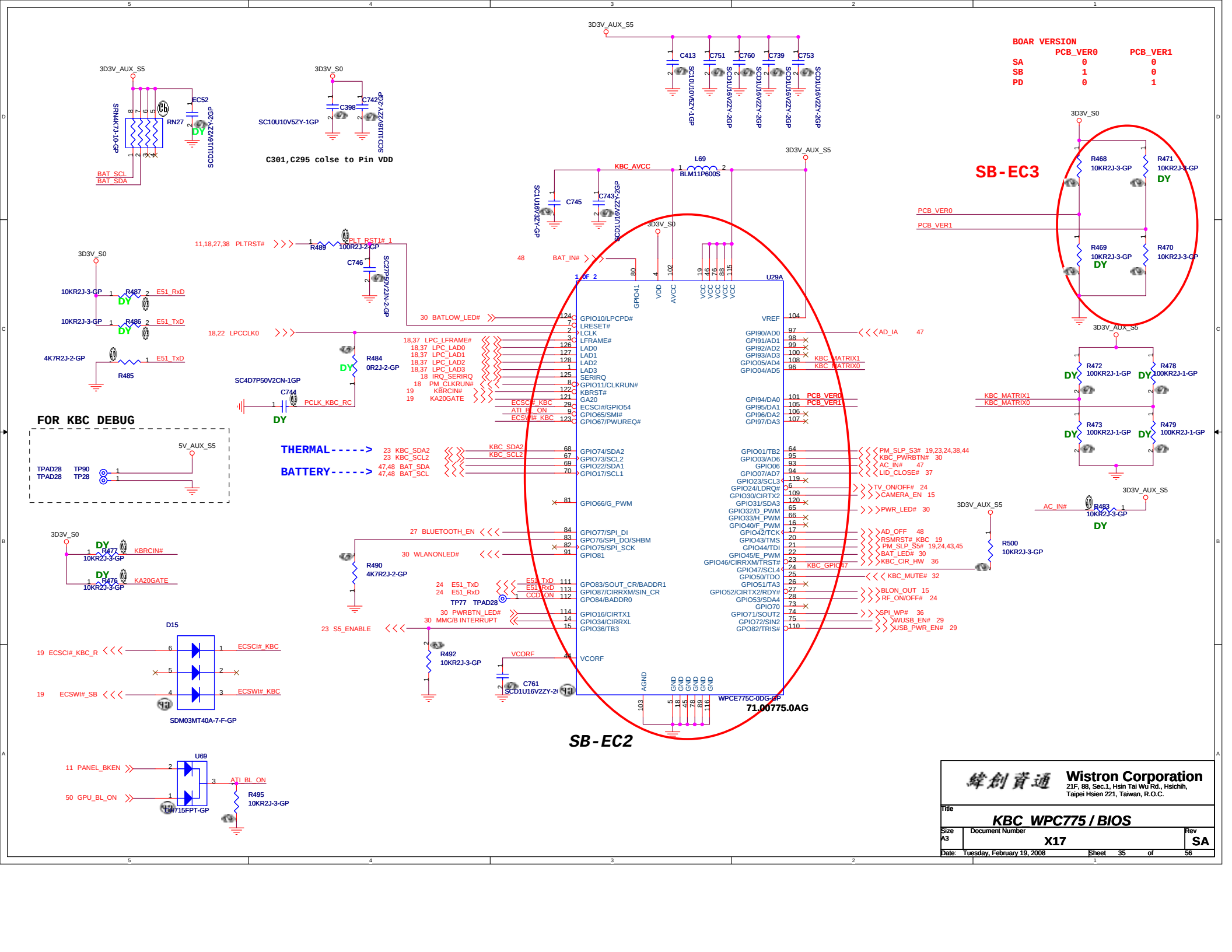
BOAR VERSION
PCB_VER0 PCB_VER1
SA 0 0
SB 1 0
PD 0 1
SB-EC3
SB-EC2
FOR KBC DEBUG
C301,C295 colse to Pin VDD
THERMAL-----> 23 KBC_SDA2
BATTERY-----> 47,48 BAT_SDA
U29A
WPCE775C-0DG-GP
71.00775.0AG
SDM03MT40A-7-F-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_WPC775 / BIOS
X17
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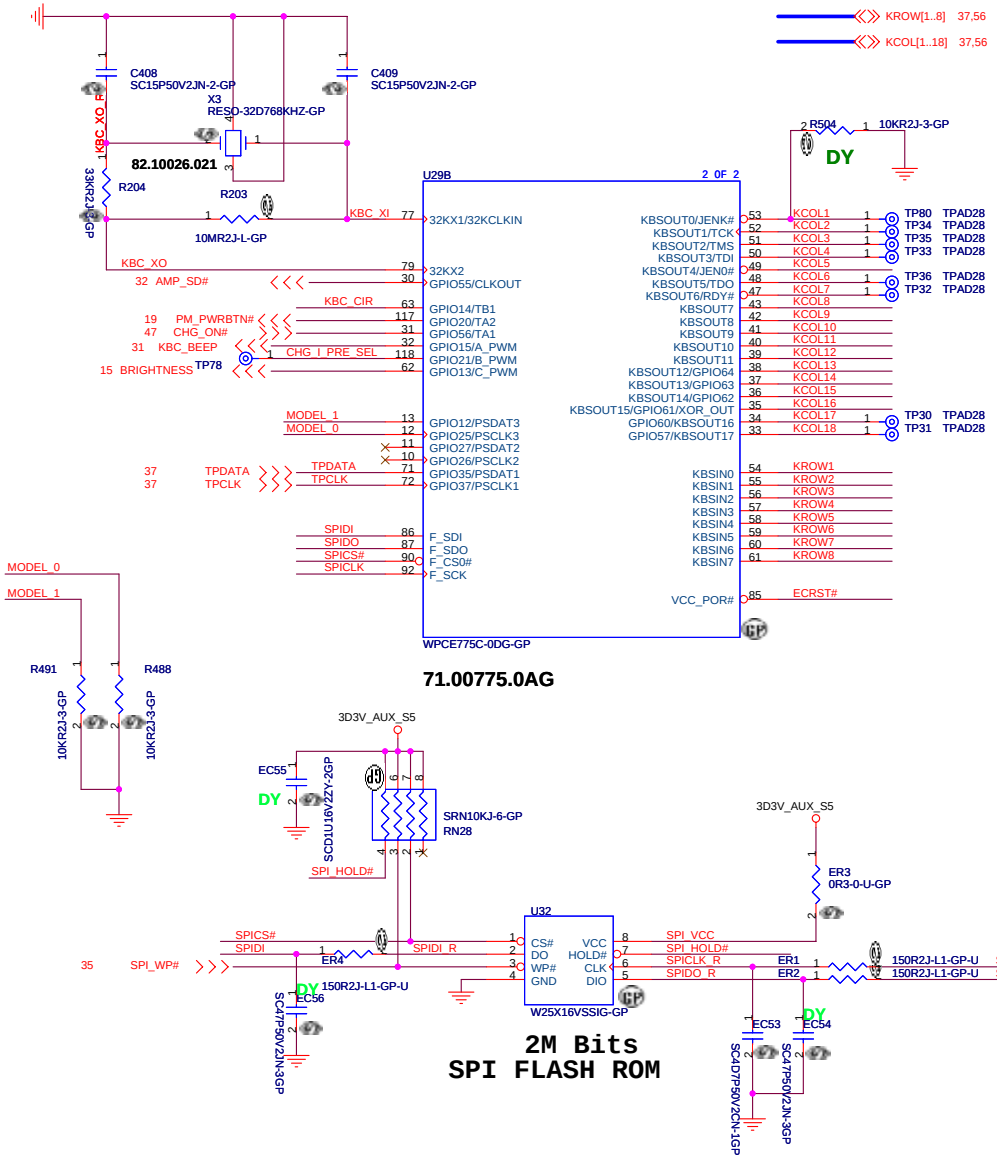
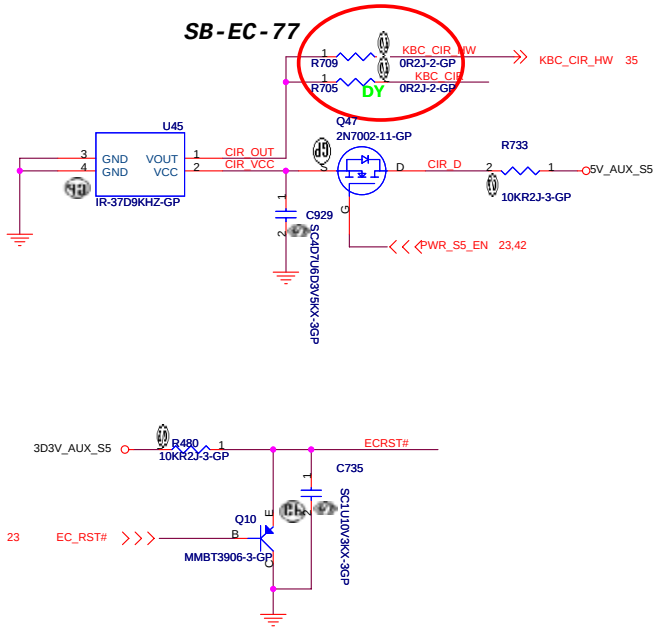


CIR



<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***KBC_WPC775 / BIOS(2/2)***

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Internal KeyBoard Connector

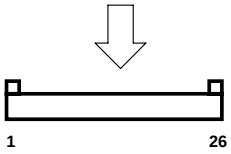
KROW[1..8] 36,56

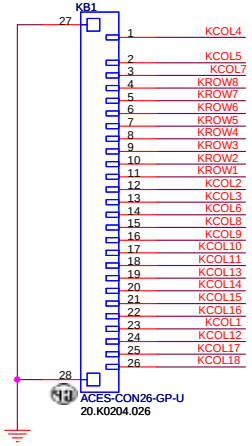
KCOL[1..18] 36,56

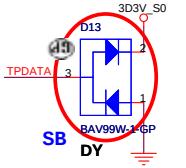
KEYBOARD MARTIX the same as Y40/Y41/Y45/Y46

Keyboard matrix (from vendor)

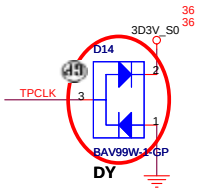
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



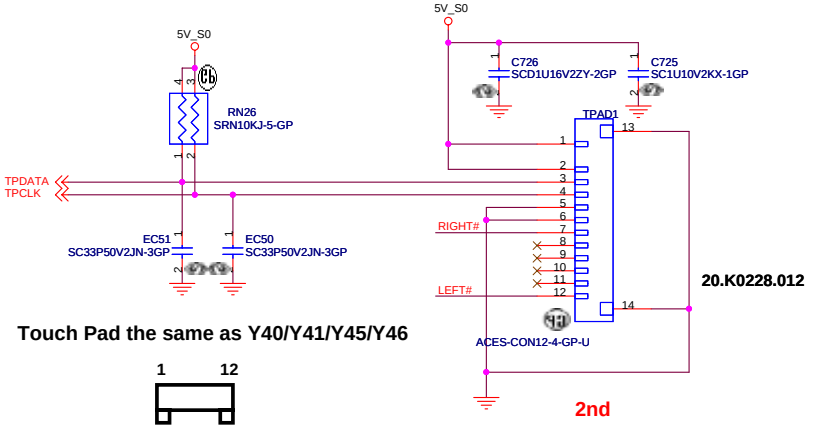




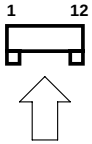
SB-EC29



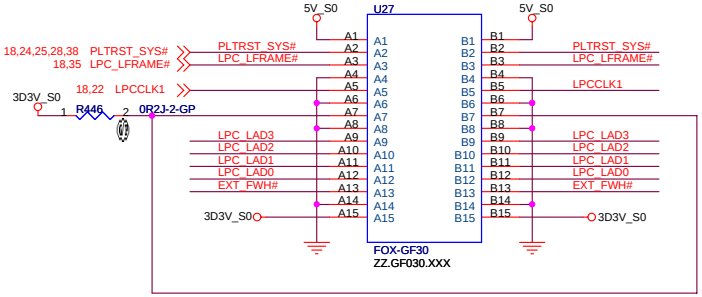
TouchPad Connector

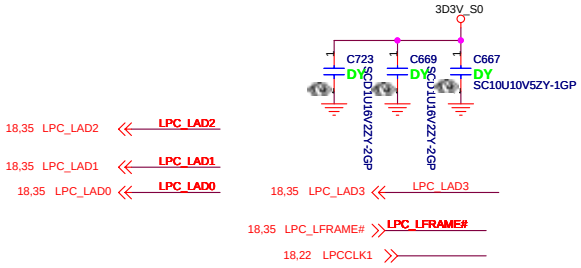


Touch Pad the same as Y40/Y41/Y45/Y46



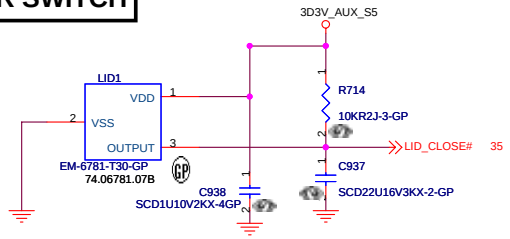
GOLDEN FINGER FOR DEBUG BOARD





COVER SWITCH

SB

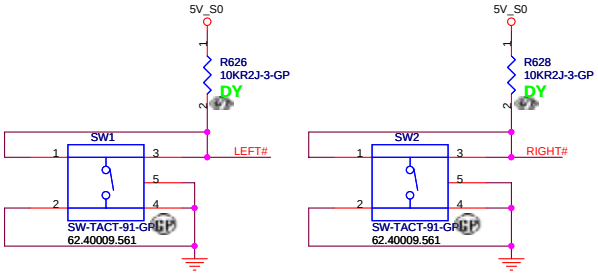


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

17" TOUCHPAD BUTTON SWITCH



蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TPAD/DEBUG/LID

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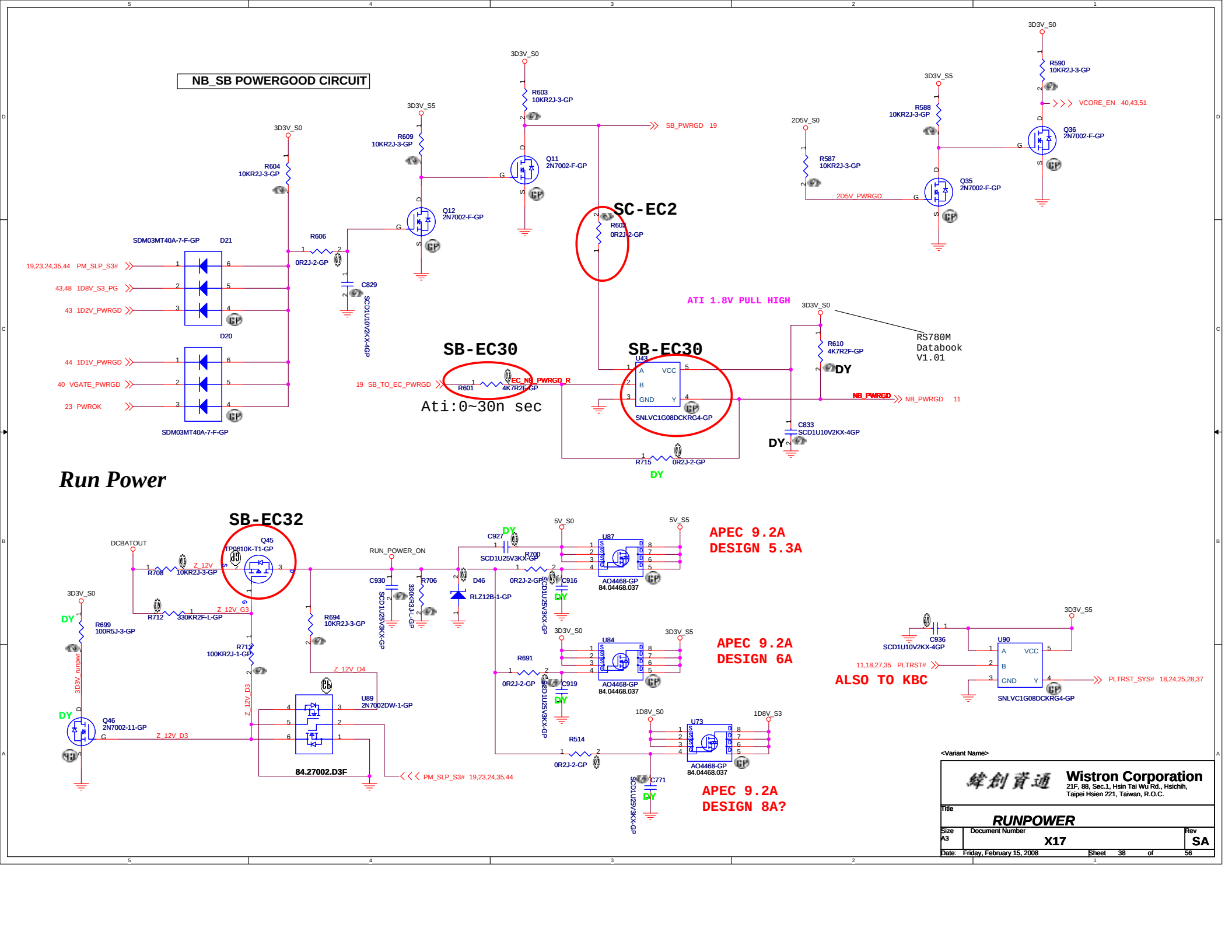
NB_SB POWERGOOD CIRCUIT
SC-EC2
SB-EC30
SB-EC30
ATI 1.8V PULL HIGH
RS780M
Databook
V1.01
Ati:0~30n sec
Run Power
SB-EC32
APEC 9.2A
DESIGN 5.3A
APEC 9.2A
DESIGN 6A
APEC 9.2A
DESIGN 8A?
ALSO TO KBC
SDM03MT40A-7-F-GP
D21
D20
SDM03MT40A-7-F-GP
19,23,24,35,44 PM_SLP_S3#
43,48 1D8V_S3_PG
43 1D2V_PWRGD
44 1D1V_PWRGD
40 VGATE_PWRGD
23 PWROK
R604 10KR2J-3-GP
R606 0R2J-2-GP
C829 SCD1U10V2KX-4GP
R609 10KR2J-3-GP
Q12 2N7002-F-GP
R603 10KR2J-3-GP
Q11 2N7002-F-GP
SB_PWRGD 19
R602 0R2J-2-GP
19 SB_TO_EC_PWRGD
R601 4K7R2F-GP
EC_NB_PWRGD_R
U43
SNLVC1G08DCKRG4-GP
R610 4K7R2F-GP
DY
NB_PWRGD
NB_PWRGD 11
C833 SCD1U10V2KX-4GP
R715 0R2J-2-GP
R590 10KR2J-3-GP
VCORE_EN 40,43,51
Q36 2N7002-F-GP
R588 10KR2J-3-GP
Q35 2N7002-F-GP
R587 10KR2J-3-GP
2D5V_PWRGD
DCBATOUT
Q45 TP0610K-T1-GP
R708 10KR2J-3-GP
Z_12V
R712 330KR2F-L-GP
Z_12V_G3
R699 100R5J-3-GP
3D3V_runpwr
Q46 2N7002-11-GP
Z_12V_D3
R713 100KR2J-1-GP
Z_12V_D3
R694 10KR2J-3-GP
Z_12V_D4
U89 2N7002DW-1-GP
84.27002.D3F
PM_SLP_S3# 19,23,24,35,44
RUN_POWER_ON
C930 SCD1U25V3KX-GP
R706 330KR3J-1-GP
D46 RLZ12B-1-GP
C927 SCD1U25V3KX-GP
R700 0R2J-2-GP
C916 SCD1U25V3KX-GP
U87 AO4468-GP 84.04468.037
R691 0R2J-2-GP
C919 SCD1U25V3KX-GP
U84 AO4468-GP 84.04468.037
R514 0R2J-2-GP
C771 SCD1U25V3KX-GP
U73 AO4468-GP 84.04468.037
C936 SCD1U10V2KX-4GP
U90 SNLVC1G08DCKRG4-GP
11,18,27,35 PLTRST#
PLTRST_SYS# 18,24,25,28,37
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RUNPOWER
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Rev SA
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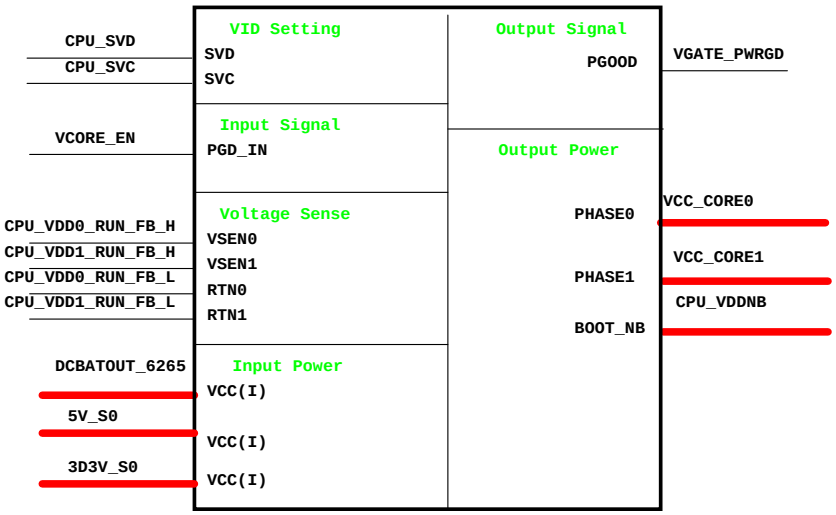
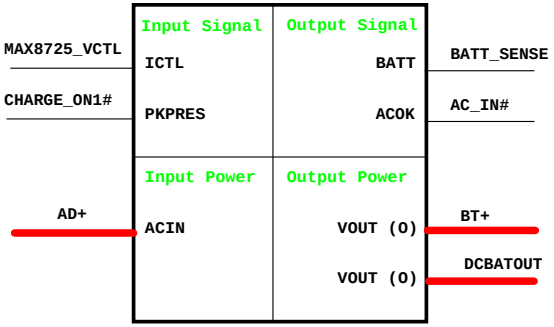
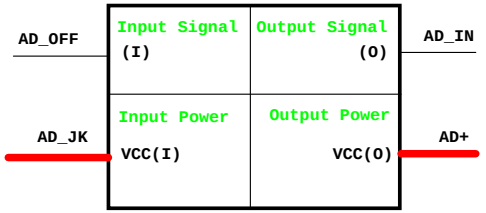
CPU_CORE
Intersil ISL6265



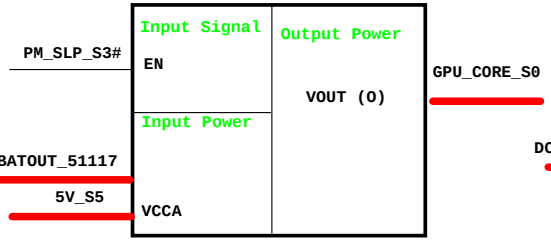
Charger Max8725



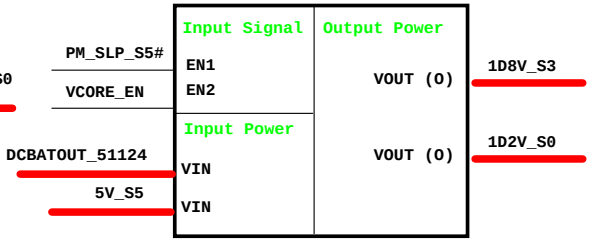
Adapter



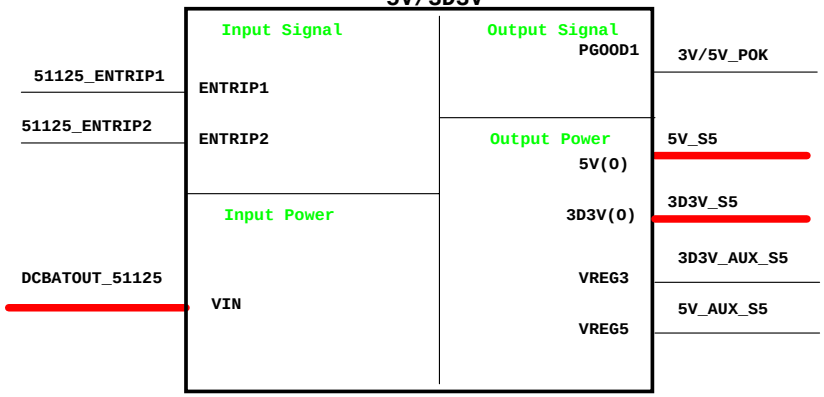
TPS51117
GPU_CORE



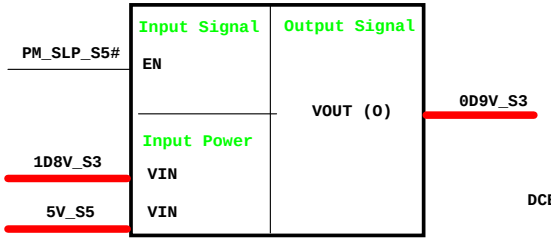
TPS51124
1D8V_S3
1D2V_S0



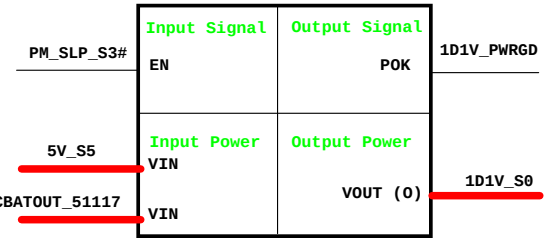
TPS51125
5V/3D3V



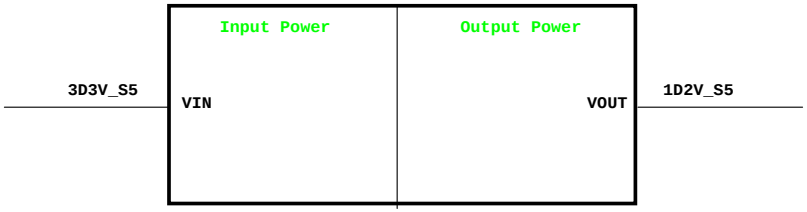
RT9026PFP
0D9V_S3



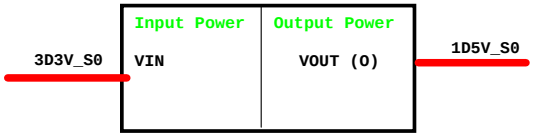
TPS51117
1D1V_S0



G9161
1D2V_S5



G957
1D5V_S0



<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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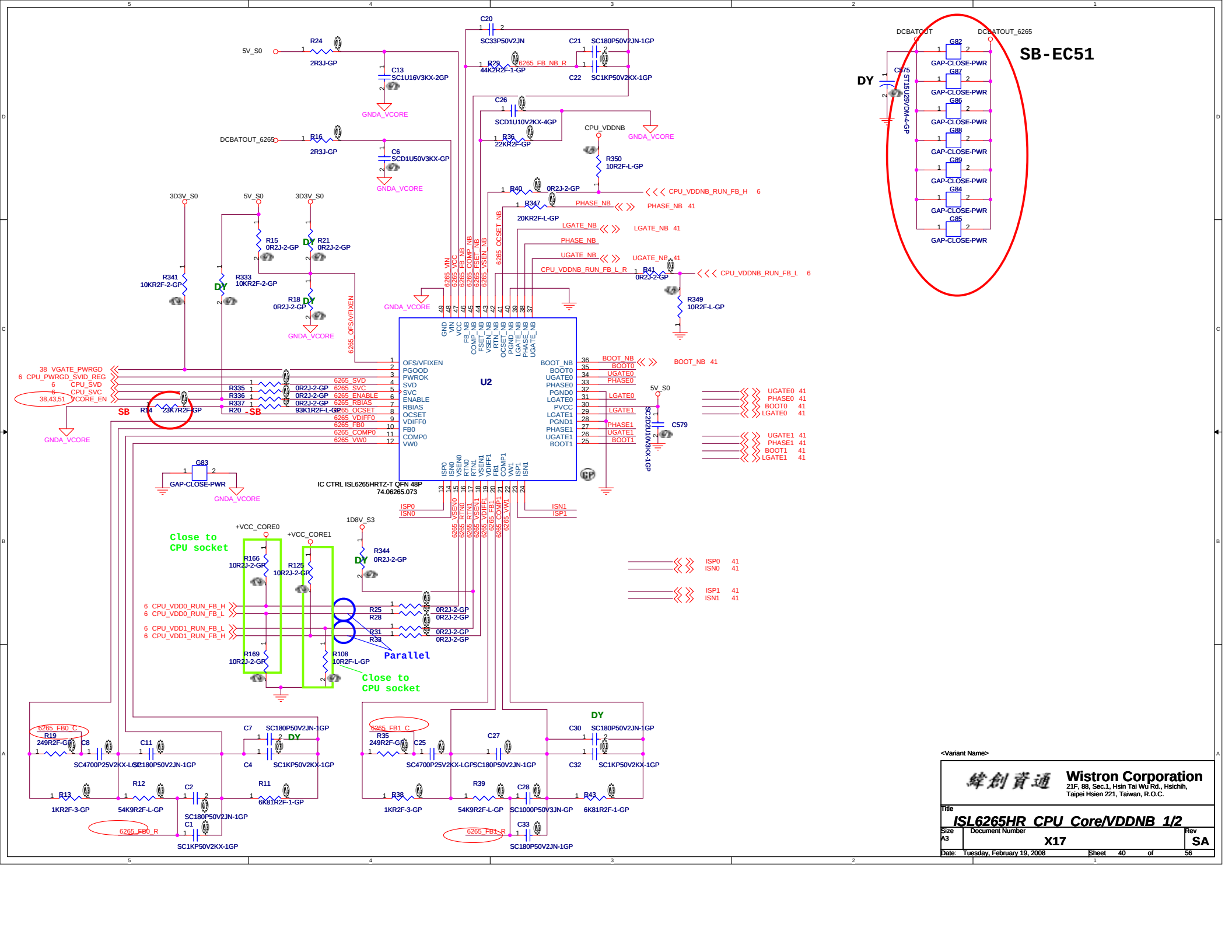
SB-EC51
DCBATOUT
DCBATOUT_6265
DY
C575
ST15U25V0M4-4GP
G82
G87
G86
G88
G89
G84
G85
GAP-CLOSE-PWR
U2
IC CTRL ISL6265HRTZ-T QFN 48P
74.06265.073
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISP0
ISN0
VSEN0
RTN0
RTN1
VSEN1
VDIFF1
FB1
COMP1
VW1
ISP1
ISN1
GND
VIN
VCC
FB_NB
COMP_NB
FSET_NB
VSEN_NB
RTN_NB
OCSET_NB
PGND_NB
LGATE_NB
PHASE_NB
UGATE_NB
Close to CPU socket
Parallel
Close to CPU socket
SB
-SB
DY
GNDA_VCORE
5V_S0
3D3V_S0
1D8V_S3
+VCC_CORE0
+VCC_CORE1
CPU_VDDNB
CPU_VDDNB_RUN_FB_H 6
CPU_VDDNB_RUN_FB_L 6
PHASE_NB 41
LGATE_NB 41
UGATE_NB 41
BOOT_NB 41
ISP0 41
ISN0 41
ISP1 41
ISN1 41
6 CPU_VDD0_RUN_FB_H
6 CPU_VDD0_RUN_FB_L
6 CPU_VDD1_RUN_FB_L
6 CPU_VDD1_RUN_FB_H
38 VGATE_PWRGD
6 CPU_PWRGD_SVID_REG
6 CPU_SVD
6 CPU_SVC
38,43,51 VCORE_EN
6265_SVD
6265_SVC
6265_ENABLE
6265_RBIAS
6265_OCSET
6265_VDIFF0
6265_FB0
6265_COMP0
6265_VW0
6265_OFS/VFIXEN
6265_FB0_C
6265_FB0_R
6265_FB1_C
6265_FB1_R
R24 2R3J-GP
R29 44K2R2F-1-GP
R16 2R3J-GP
R36 22KR2F-GP
R350 10R2F-L-GP
R40 0R2J-2-GP
R347 20KR2F-L-GP
R41 0R2J-2-GP
R349 10R2F-L-GP
R15 0R2J-2-GP
R21 0R2J-2-GP
R341 10KR2F-2-GP
R333 10KR2F-2-GP
R18 0R2J-2-GP
R335 0R2J-2-GP
R336 0R2J-2-GP
R337 0R2J-2-GP
R14 23K7R2F-GP
R20 93K1R2F-L-GP
R344 0R2J-2-GP
R166 10R2J-2-GP
R125 10R2J-2-GP
R169 10R2J-2-GP
R108 10R2F-L-GP
R25 0R2J-2-GP
R28 0R2J-2-GP
R31 0R2J-2-GP
R33 0R2J-2-GP
R19 249R2F-GP
R35 249R2F-GP
R13 1KR2F-3-GP
R12 54K9R2F-L-GP
R11 6K81R2F-1-GP
R38 1KR2F-3-GP
R39 54K9R2F-L-GP
R43 6K81R2F-1-GP
C20 SC33P50V2JN
C21 SC180P50V2JN-1GP
C22 SC1KP50V2KX-1GP
C13 SC1U16V3KX-2GP
C26 SCD1U10V2KX-4GP
C6 SCD1U50V3KX-GP
C579 SC2D2U10V3KX-1GP
C8 SC4700P25V2KX-LGP
C11 SC180P50V2JN-1GP
C4 SC1KP50V2KX-1GP
C7 SC180P50V2JN-1GP
C2 SC180P50V2JN-1GP
C1 SC1KP50V2KX-1GP
C25 SC4700P25V2KX-LGP
C27 SC180P50V2JN-1GP
C30 SC180P50V2JN-1GP
C32 SC1KP50V2KX-1GP
C28 SC1000P50V3JN-GP
C33 SC180P50V2JN-1GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6265HR_CPU_Core/VDDNB_1/2
Size A3
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Sheet 40 of 56

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037

SB-EC-69

+VCC_CORE0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A

+VCC_CORE1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A

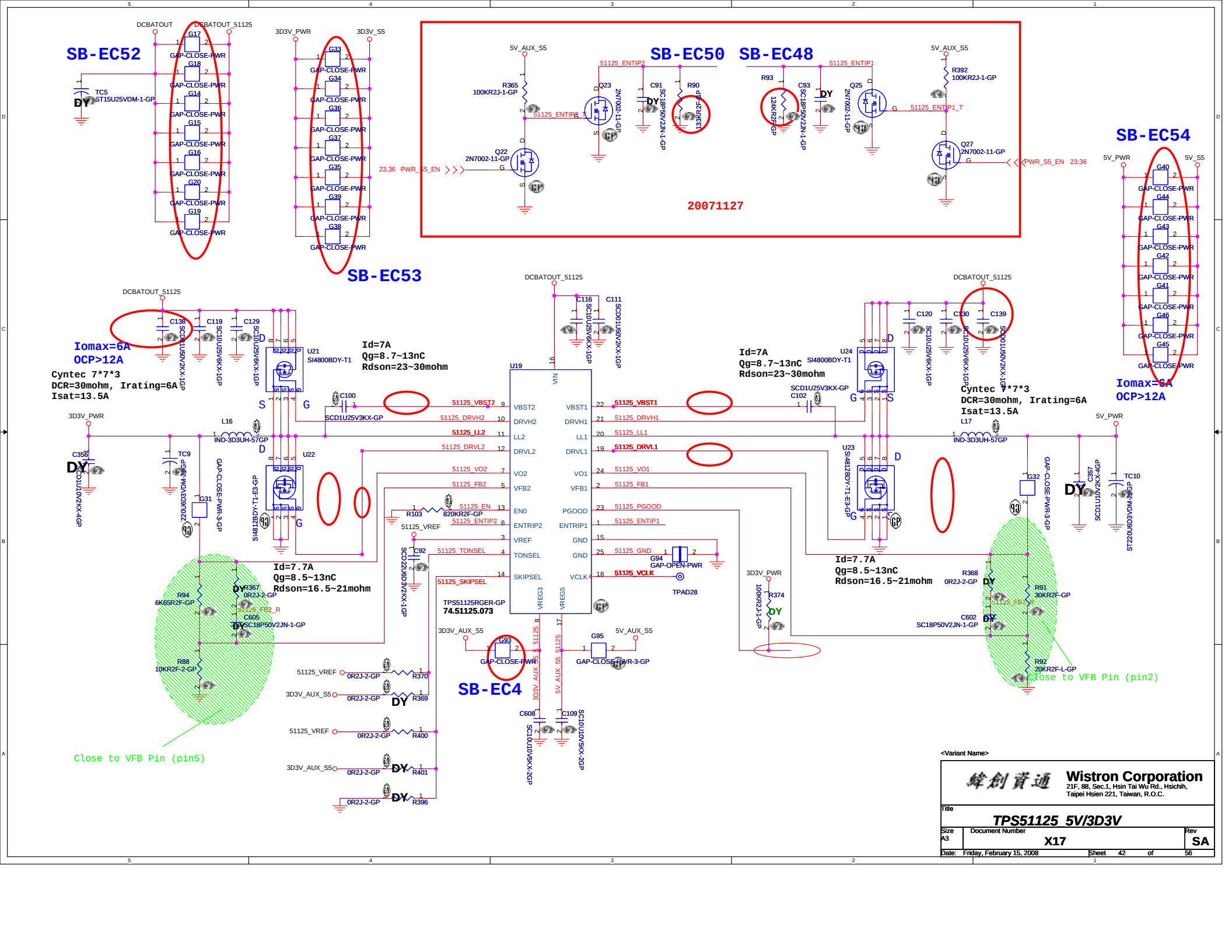
Iomax=3A
OCP>6A

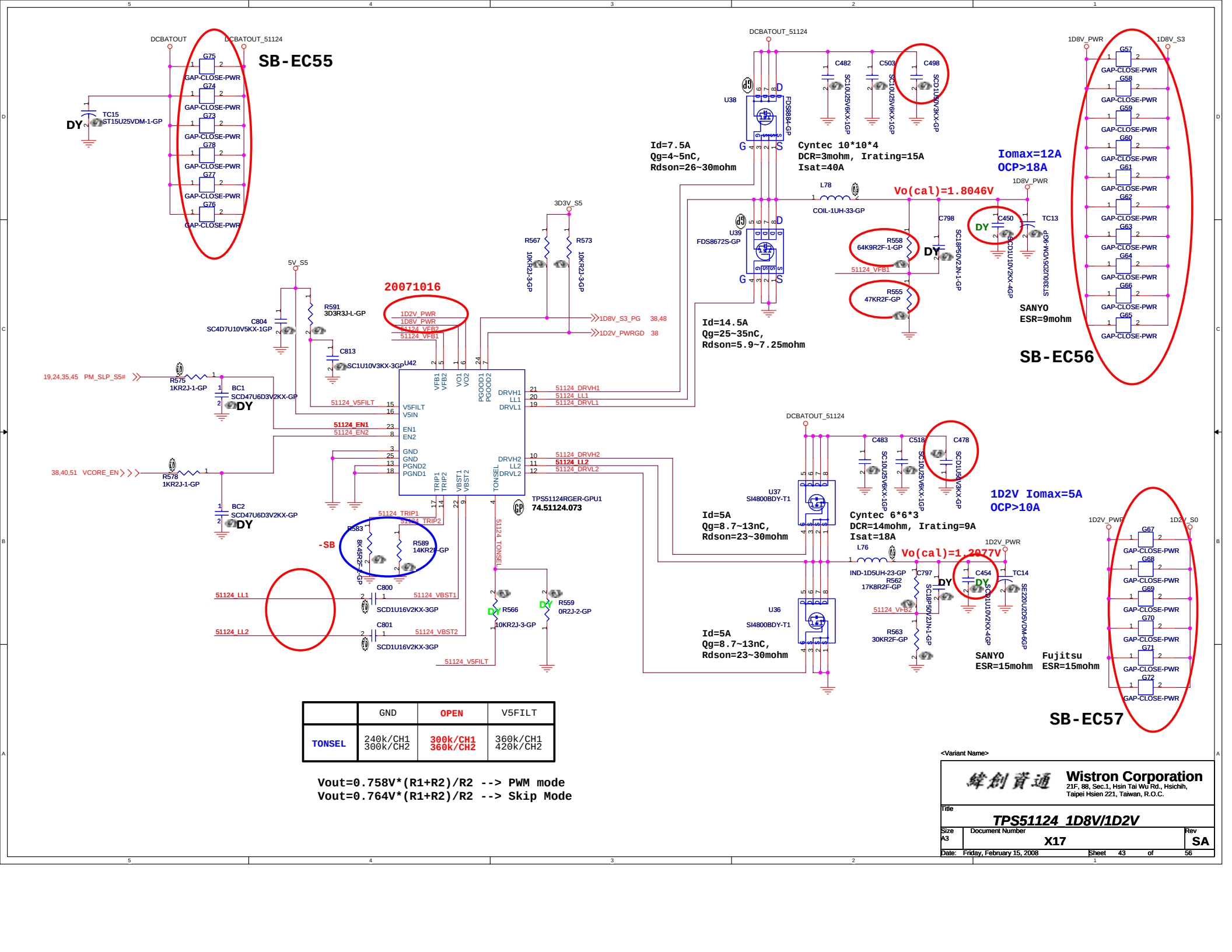
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6265HR_CPU_Core/VDDNB_2/2
Size: A3 | Document Number: X17 | Rev: SA
Date: Friday, February 15, 2008 | Sheet 41 of 56


SB-EC52
SB-EC53
SB-EC50
SB-EC48
SB-EC54
SB-EC4
20071127
Iomax=6A
OCP>12A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
PWR_S5_EN 23,36
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51125_5V/3D3V
X17
SA
Friday, February 15, 2008
Sheet 42 of 56



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

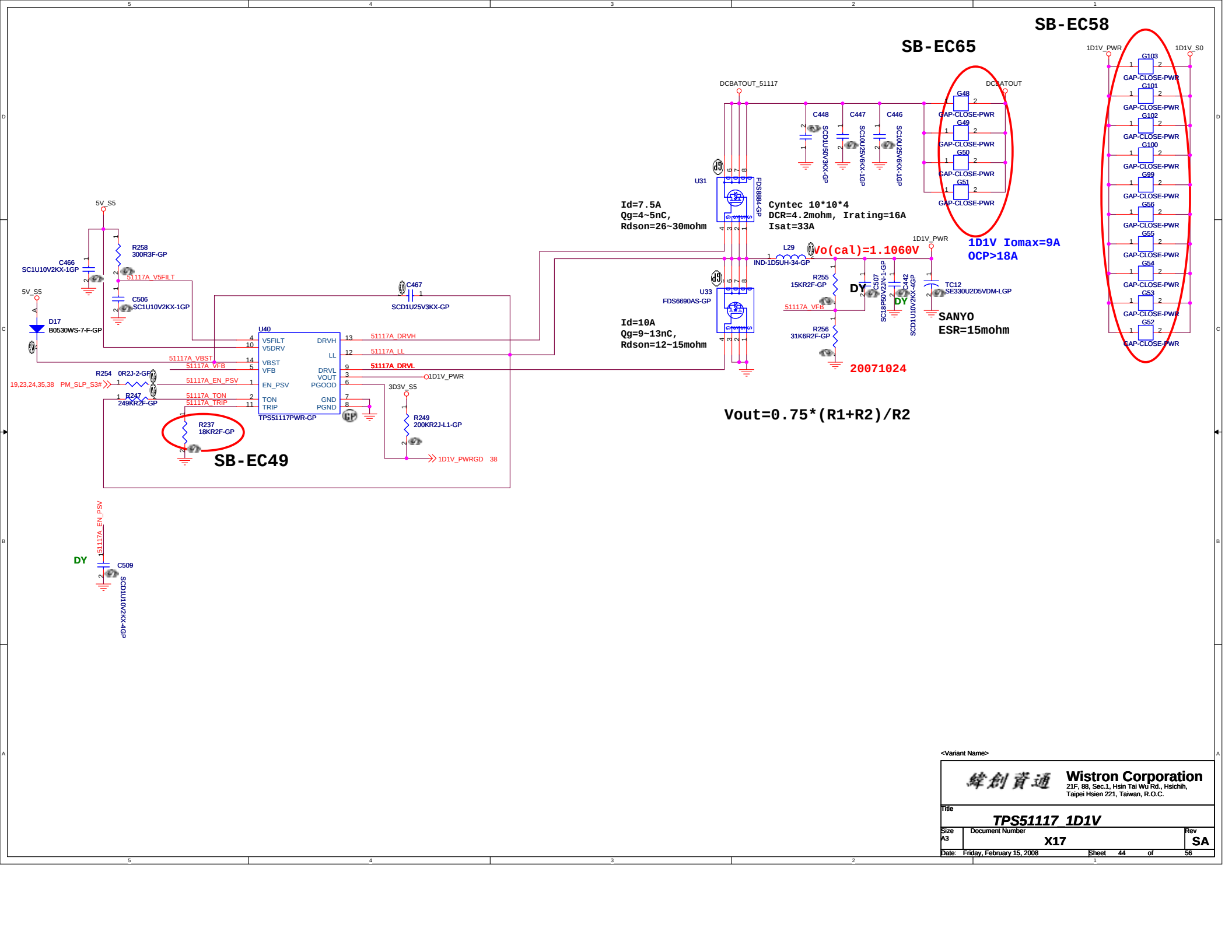
<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51124_1D8V/1D2V*

Size	Document Number	Rev
A3	X17	SA

Date: Friday, February 15, 2008 Sheet 43 of 56



<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117_1D1V***

Size	Document Number	Rev
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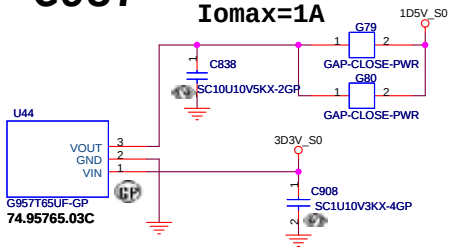
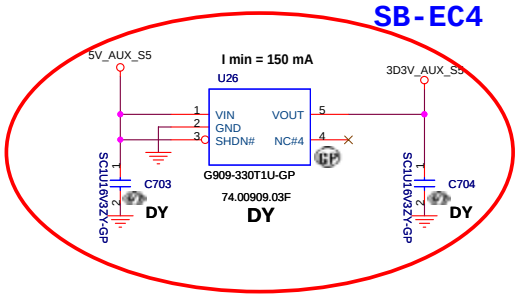
Date: Friday, February 15, 2008 Sheet 44 of 56

G957

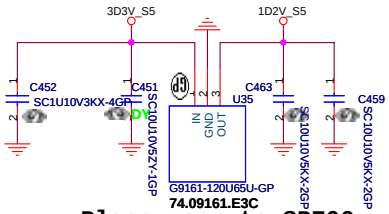
1D5V_S0
Iomax=1A



SB-EC4

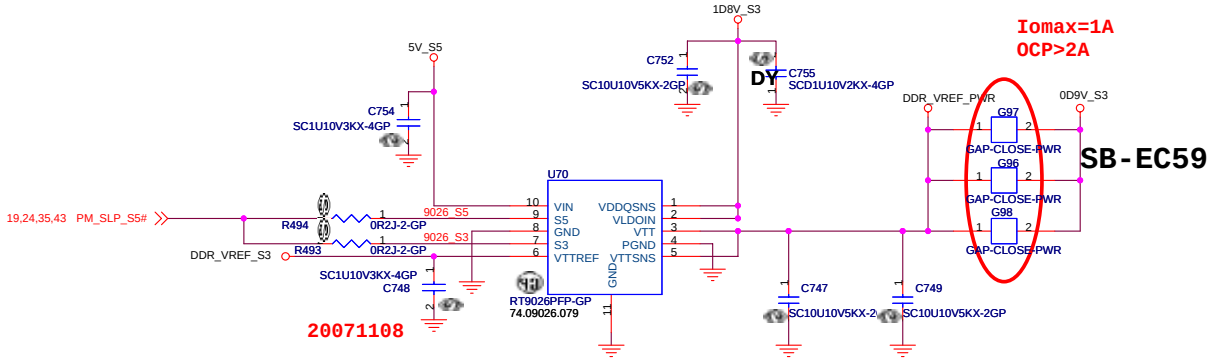


1D2V_S5
Iomax=400mA



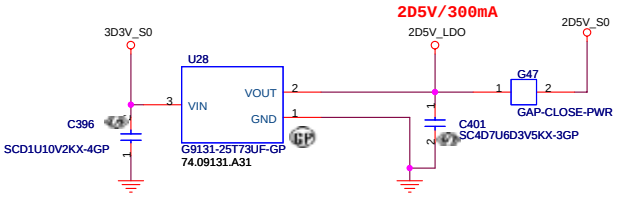
Place near to SB700

SB-EC59



20071108

2D5V_S0
Iomax=0.3A



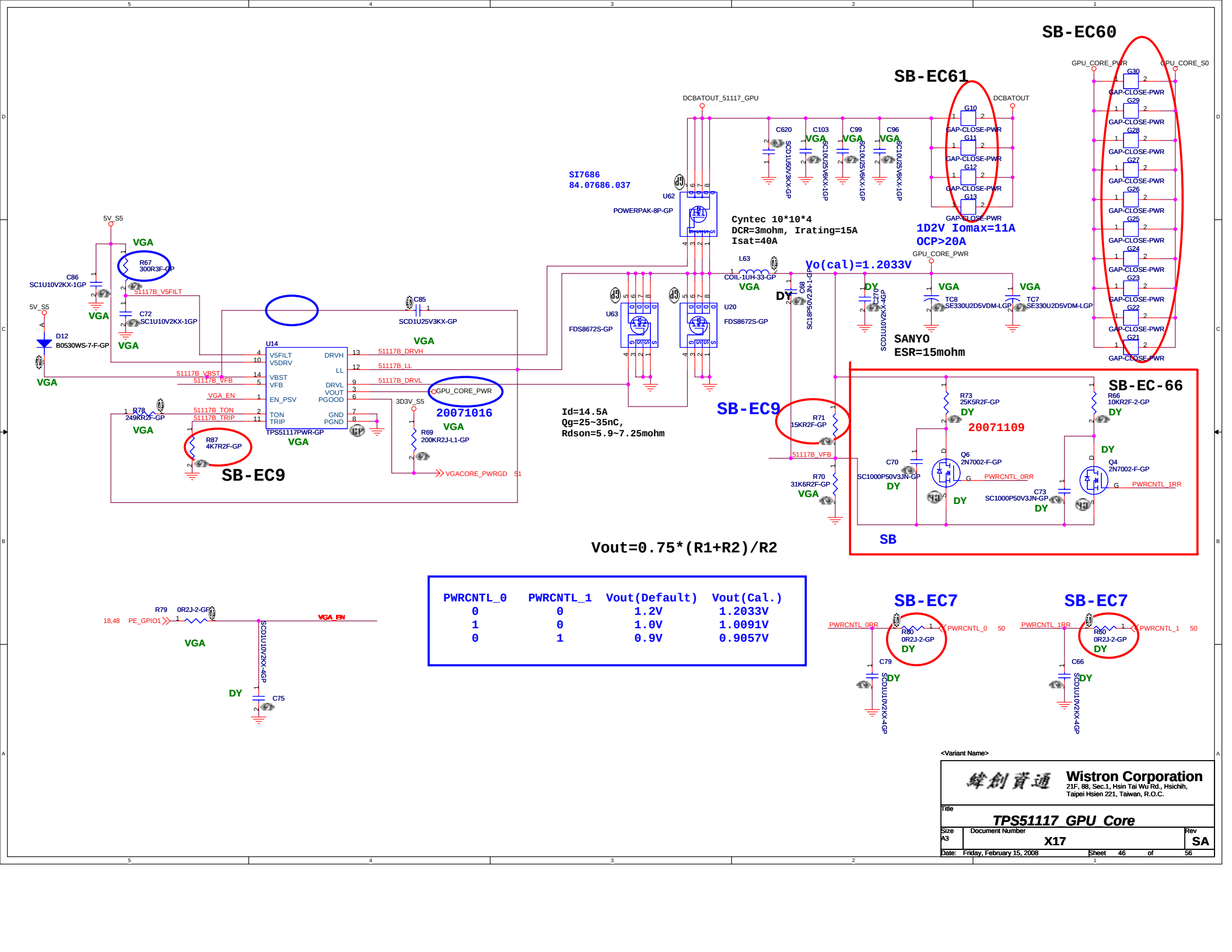
<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***0D9V&2D5V&1D25V&1D5V***

Size	Document Number	Rev
A3	X17	SA

Date: Friday, February 15, 2008 Sheet 45 of 56



PWRCNTL_0	PWRCNTL_1	Vout(Default)	Vout(Cal.)
0	0	1.2V	1.2033V
1	0	1.0V	1.0091V
0	1	0.9V	0.9057V

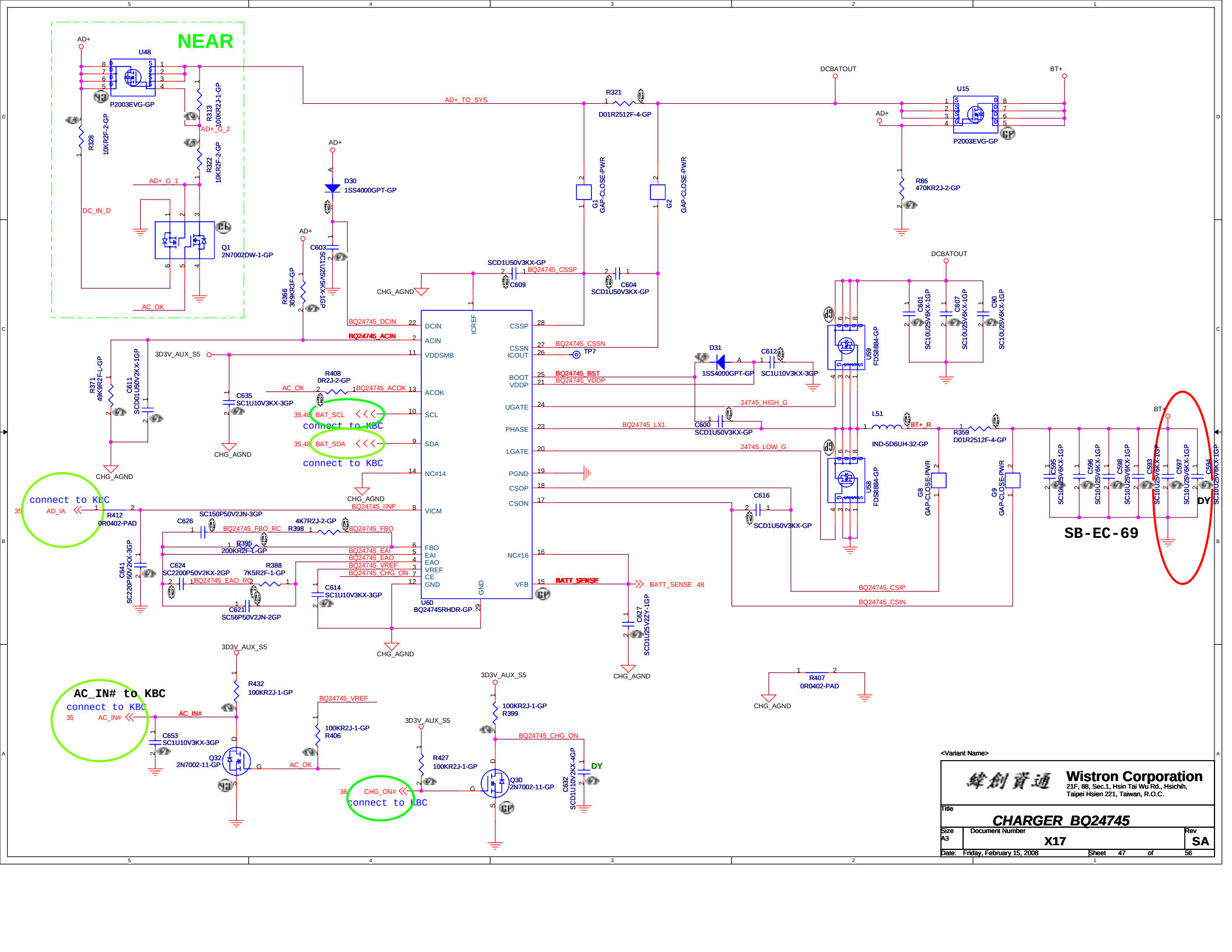
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117_GPU_Core

Size: A3 | Document Number: X17 | Rev: SA

Date: Friday, February 15, 2008 | Sheet 46 of 56


NEAR
U48
P2003EVG-GP
R328 10KR2F-2-GP
R313 100KR2J-1-GP
R322 10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q1 2N7002DW-1-GP
AC_OK
AD+
D30 1SS4000GPT-GP
C603 SC1U25V5KX-1GP
R366 309KR3F-GP
AD+_TO_SYS
R321 D01R2512F-4-GP
DCBATOUT
BT+
U15
P2003EVG-GP
R86 470KR2J-2-GP
G1 GAP-CLOSE-PWR
G2 GAP-CLOSE-PWR
SCD1U50V3KX-GP
C609
C604 SCD1U50V3KX-GP
CHG_AGND
ICREF
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R371 49K9R2F-L-GP
C611 SCD01U50V2KX-1GP
C635 SC1U10V3KX-3GP
R408 0R2J-2-GP
AC_OK
BQ24745_ACOK
35,48 BAT_SCL
35,48 BAT_SDA
connect to KBC
connect to KBC
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U60
BQ24745RHDR-GP
BQ24745_CSSP
BQ24745_CSSN
TP7
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BATT_SENSE
BATT_SENSE 48
D31 1SS4000GPT-GP
C612 SC1U10V3KX-3GP
C600 SCD1U50V3KX-GP
L51 IND-5D6UH-32-GP
BT+_R
R359 D01R2512F-4-GP
U59 FDS8884-GP
U58 FDS8884-GP
C601 SC10U25V6KX-1GP
C607 SC10U25V6KX-1GP
C90 SC10U25V6KX-1GP
G8 GAP-CLOSE-PWR
G9 GAP-CLOSE-PWR
C595 SC10U25V6KX-1GP
C596 SC10U25V6KX-1GP
C598 SC10U25V6KX-1GP
C593 SC10U25V6KX-1GP
C597 SC10U25V6KX-1GP
C594 SC10U25V6KX-1GP
DY
SB-EC-69
C616 SCD1U50V3KX-GP
BQ24745_CSIP
BQ24745_CSIN
C627 SCD1U25V2ZY-1GP
R407 0R0402-PAD
R412 0R0402-PAD
AD_IA
SC150P50V2JN-3GP
C626
BQ24745_FBO_RC
4K7R2J-2-GP
R398
BQ24745_FBO
R395 200KR2F-1-GP
C641 SC220P50V2KX-3GP
C624 SC2200P50V2KX-2GP
BQ24745_EAO_RC
R388 7K5R2F-1-GP
C621 SC56P50V2JN-2GP
C614 SC1U10V3KX-3GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
AC_IN# to KBC
connect to KBC
AC_IN#
R432 100KR2J-1-GP
C653 SC1U10V3KX-3GP
Q32 2N7002-11-GP
AC_OK
BQ24745_VREF
R406 100KR2J-1-GP
CHG_ON#
connect to KBC
R427 100KR2J-1-GP
R399 100KR2J-1-GP
BQ24745_CHG_ON
Q30 2N7002-11-GP
C632 SCD1U10V2KX-4GP
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER_BQ24745
Size A3
Document Number X17
Rev SA
Date: Friday, February 15, 2008
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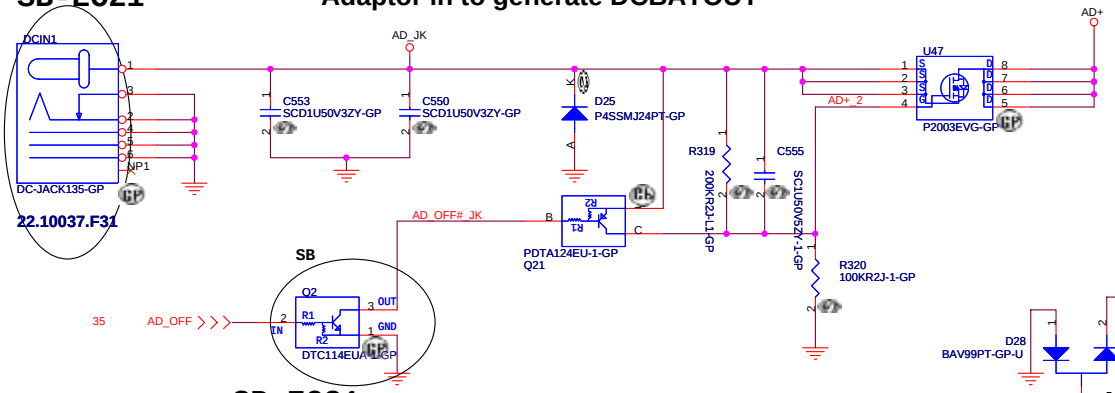
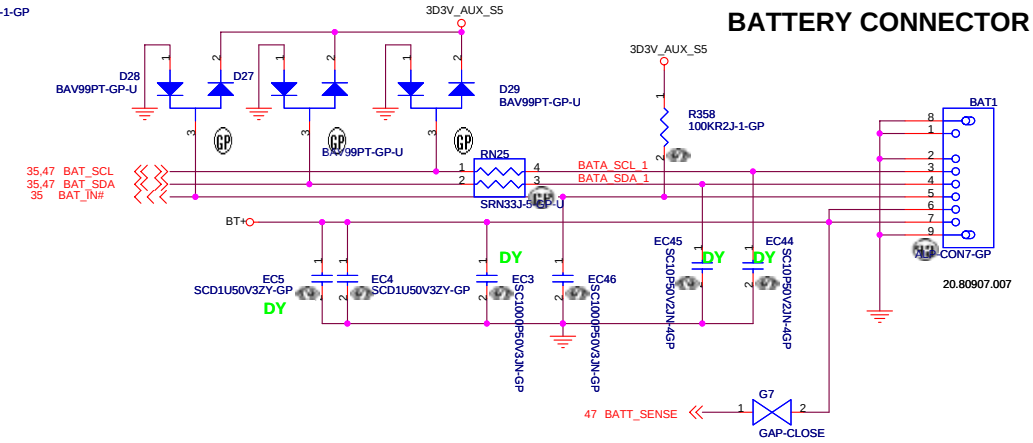
SB-EC21

Adaptor in to generate DCBATOUT

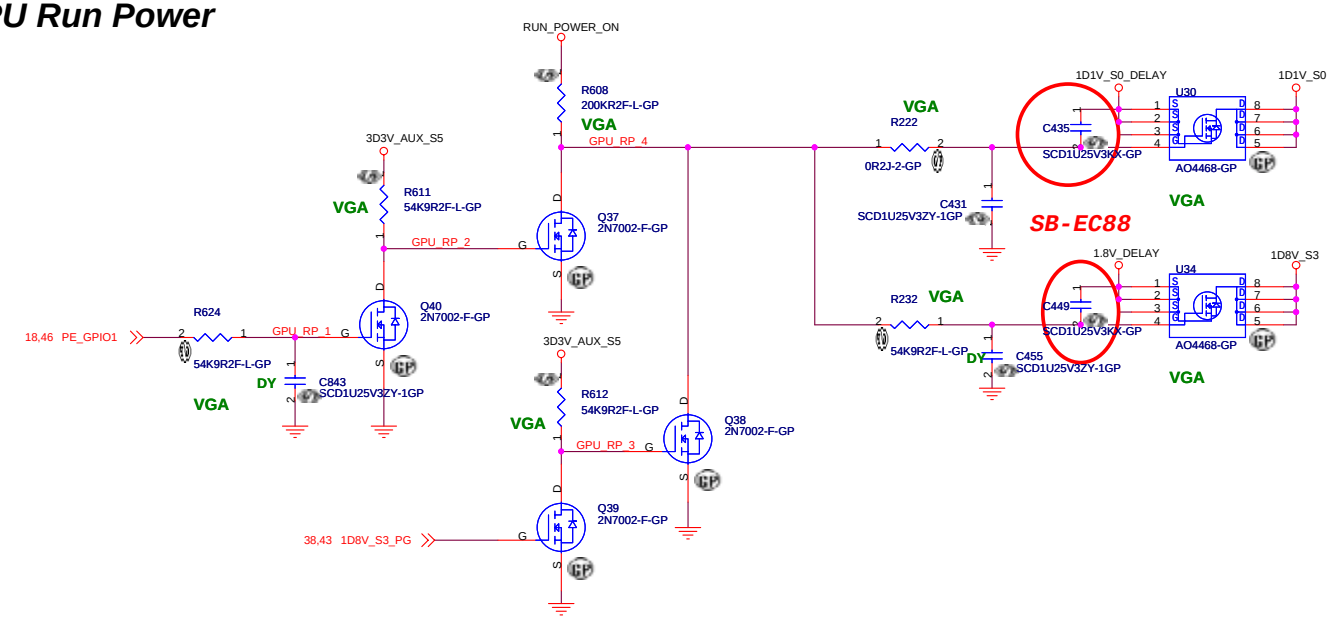


SB-EC31

BATTERY CONNECTOR



GPU Run Power



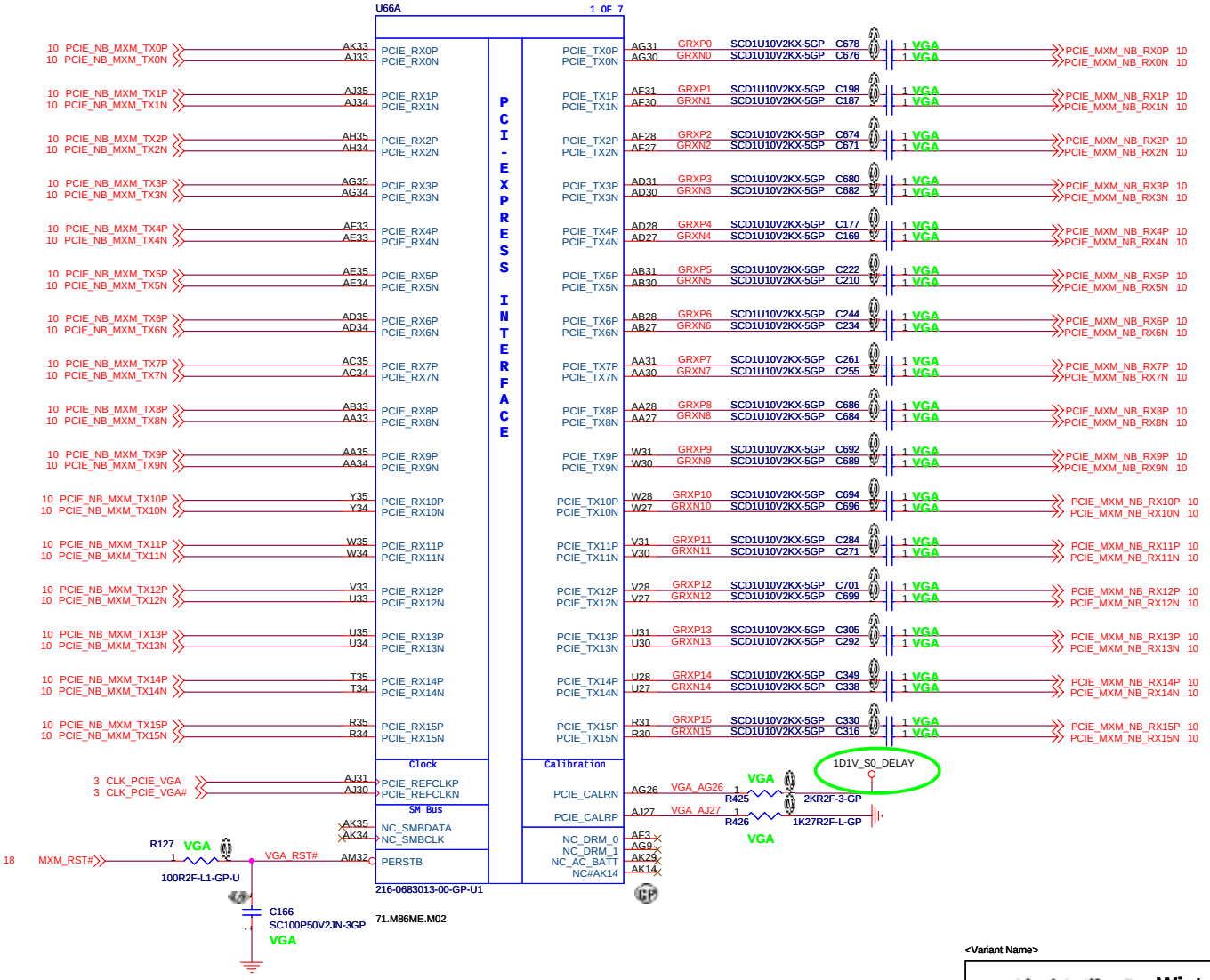
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD_IN/ BTY SWITCH/GPURUN

Size	Document Number	Rev
A3	X17	SA

Date: Friday, February 15, 2008 Sheet 48 of 56



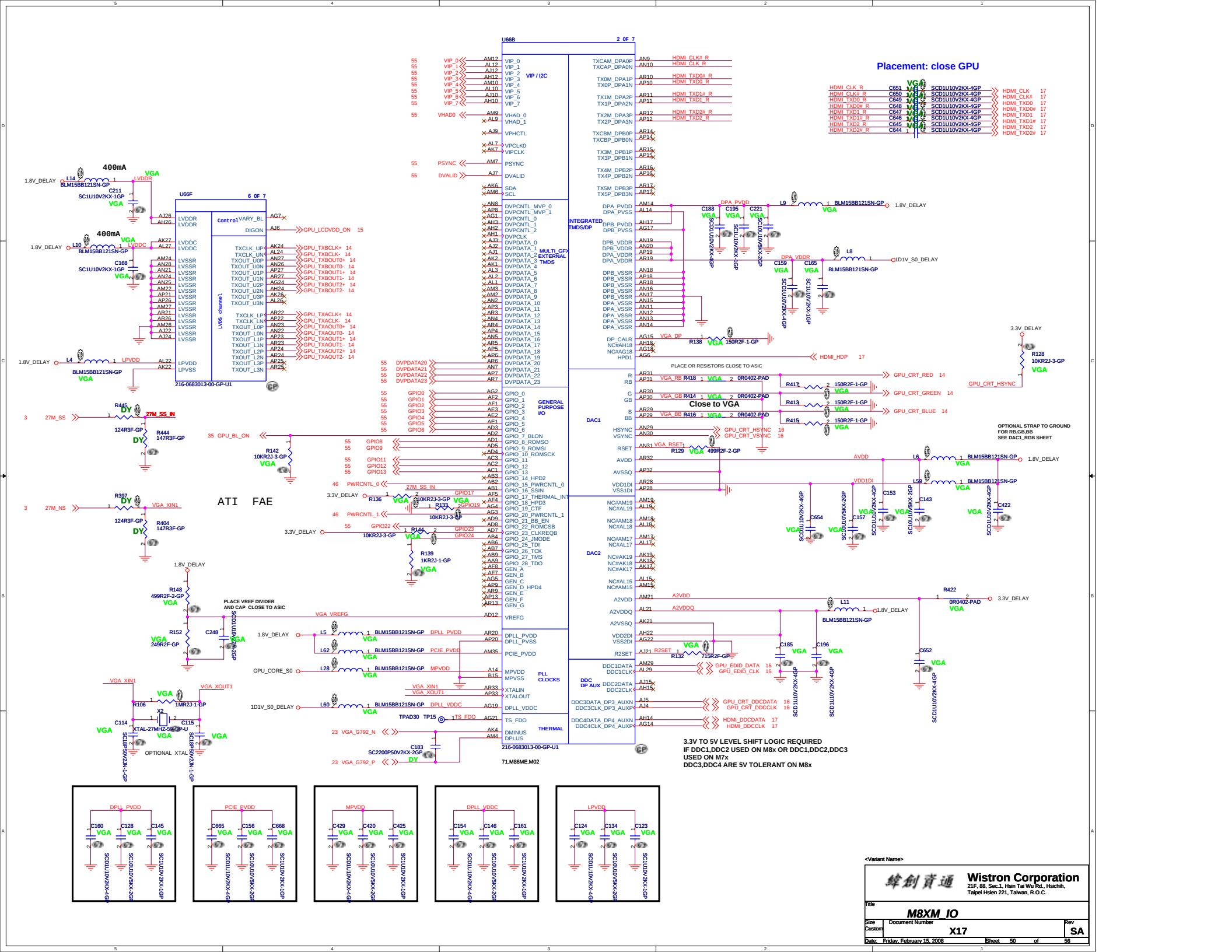
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **M8XM_PCIE**

Size	Document Number	Rev
A3	X17	SA

Date: Friday, February 15, 2008 Sheet 49 of 56



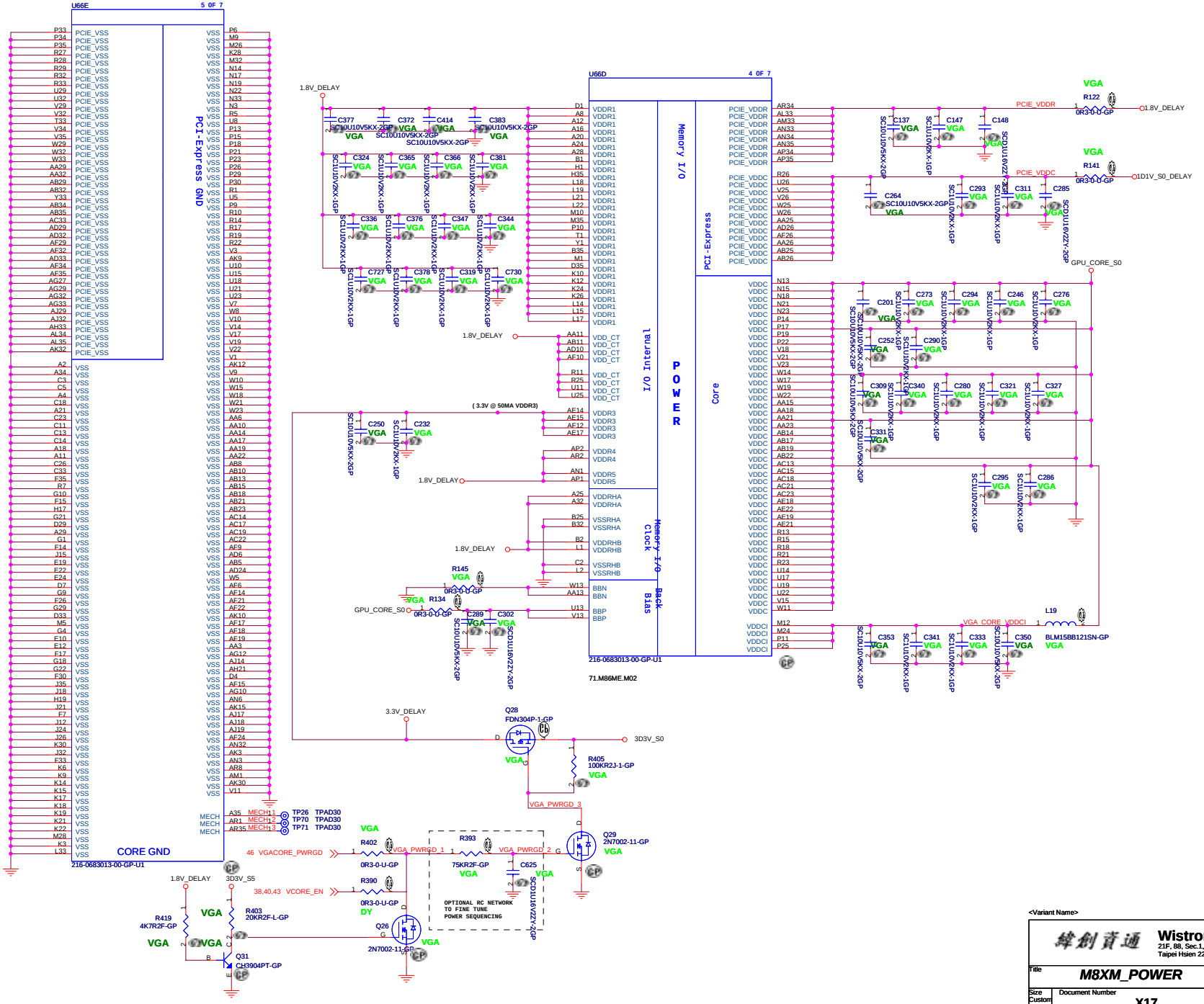
<Variant Name>

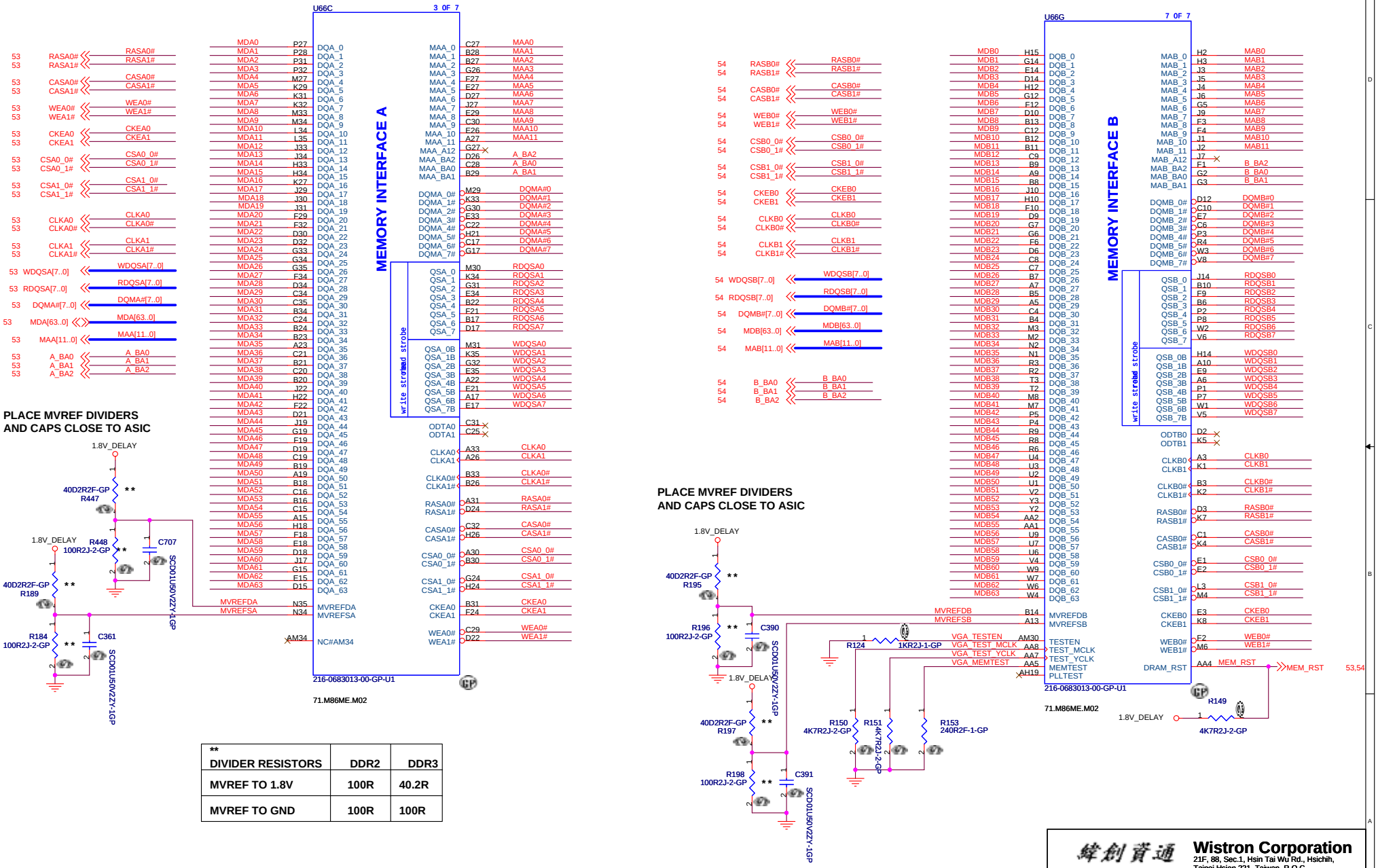
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M8XM_IO

Size: Custom | Document Number: X17 | Rev: SA

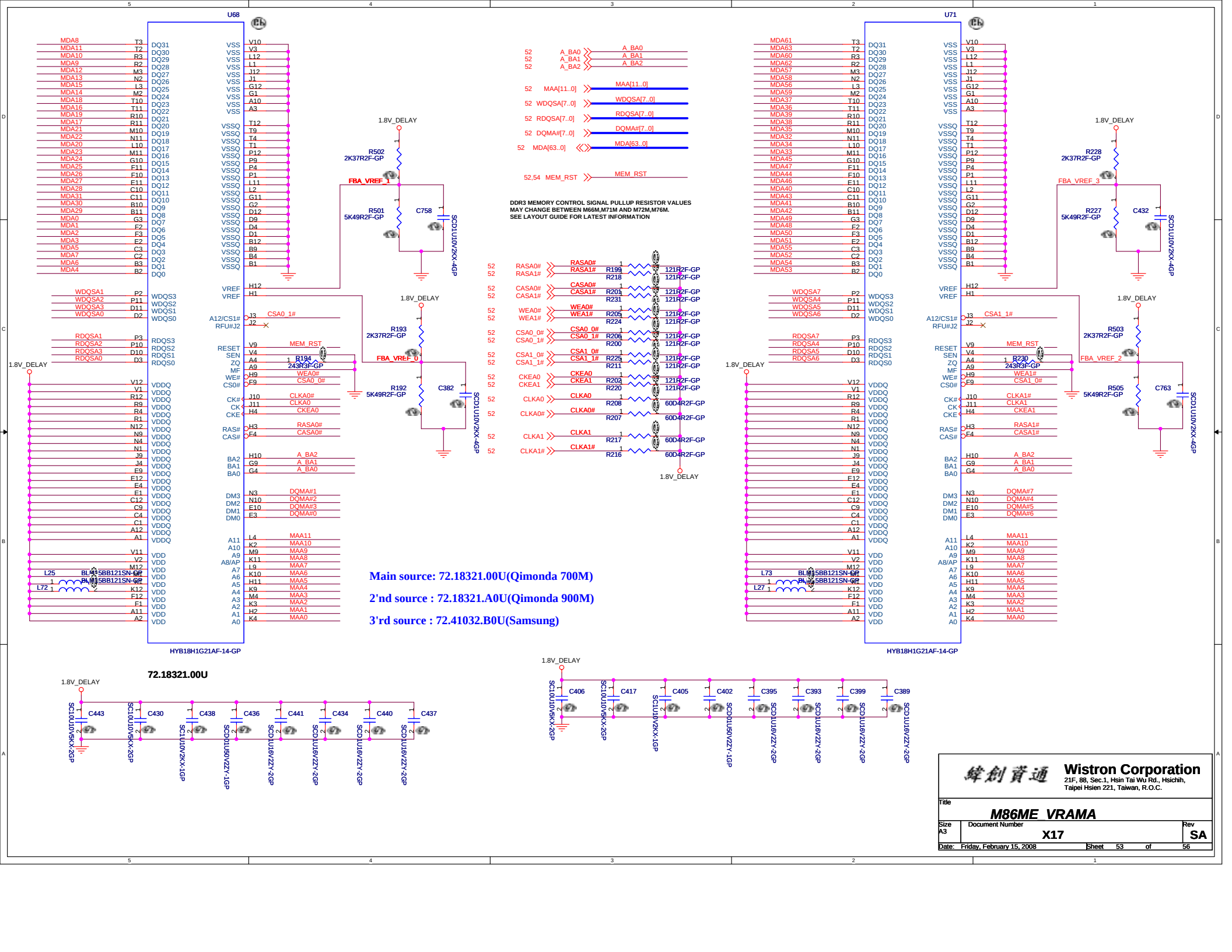
Date: Friday, February 15, 2008 | Sheet 50 of 56


U66E
5 OF 7
PCI-Express GND
CORE GND
216-0683013-00-GP-U1
U66D
4 OF 7
Memory I/O
I/O Internal
POWER
Core
PCI-Express
Memory I/O Clock
Bias
216-0683013-00-GP-U1
71.M86ME.M02
1.8V_DELAY
3.3V_DELAY
3D3V_S0
GPU_CORE_S0
VGA_CORE_VDDCI
1D1V_S0_DELAY
(3.3V @ 50MA VDDR3)
VGACORE_PWRGD
VCORE_EN
VGA_PWRGD_1
VGA_PWRGD_2
VGA_PWRGD_3
OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING
Q28 FDN304P-1-GP
Q29 2N7002-11-GP
Q26 2N7002-11-GP
Q31 CH3904PT-GP
R405 100KR2J-1-GP
R402 0R3-0-U-GP
R390 0R3-0-U-GP
R393 75KR2F-GP
R403 20KR2F-L-GP
R419 4K7R2F-GP
R145 0R3-0-U-GP
R134 0R3-0-U-GP
R122 0R3-0-U-GP
R141 0R3-0-U-GP
L19 BLM15BB121SN-GP
TP26 TPAD30
TP70 TPAD30
TP71 TPAD30
VGA
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M8XM_POWER
Size Custom
Document Number
X17
Rev
SA
Date: Friday, February 15, 2008
Sheet 51 of 56



** DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M8XM_MEMORY
Size A3	Document Number X17
Rev	SA
Date: Friday, February 15, 2008	Sheet 52 of 56


U68
U71
HYB18H1G21AF-14-GP
DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M66M,M71M AND M72M,M76M.
SEE LAYOUT GUIDE FOR LATEST INFORMATION
Main source: 72.18321.00U(Qimonda 700M)
2'nd source : 72.18321.A0U(Qimonda 900M)
3'rd source : 72.41032.B0U(Samsung)
72.18321.00U
1.8V_DELAY
FBA_VREF_1
FBA_VREF_0
FBA_VREF_3
FBA_VREF_2
MEM_RST
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
M86ME_VRAMA
X17
SA
Friday, February 15, 2008
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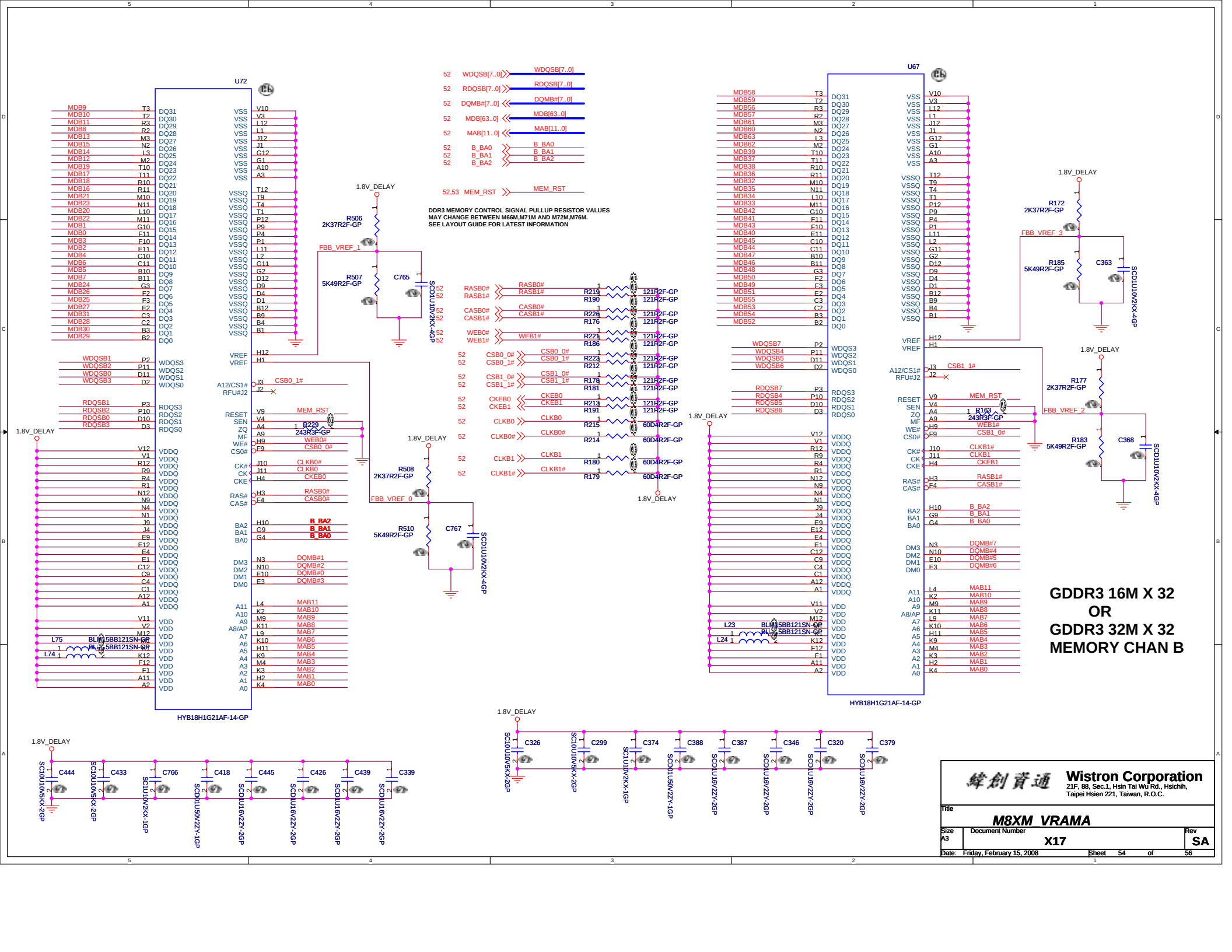
56


U72
HYB18H1G21AF-14-GP
U67
HYB18H1G21AF-14-GP
DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M66M,M71M AND M72M,M76M.
SEE LAYOUT GUIDE FOR LATEST INFORMATION
GDDR3 16M X 32
OR
GDDR3 32M X 32
MEMORY CHAN B
1.8V_DELAY
FBB_VREF_1
FBB_VREF_2
FBB_VREF_3
FBB_VREF_0
R506 2K37R2F-GP
R507 5K49R2F-GP
R508 2K37R2F-GP
R510 5K49R2F-GP
R172 2K37R2F-GP
R185 5K49R2F-GP
R177 2K37R2F-GP
R183 5K49R2F-GP
R163 243R3F-GP
R229 243R3F-GP
C765
C767
C363
C368
L75 BLM15BB121SN-GP
L74 BLM15BB121SN-GP
L23 BLM15BB121SN-GP
L24 BLM15BB121SN-GP
C444
C433
C766
C418
C445
C426
C439
C339
C326
C299
C374
C388
C387
C346
C320
C379
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
M8XM_VRAMA
X17
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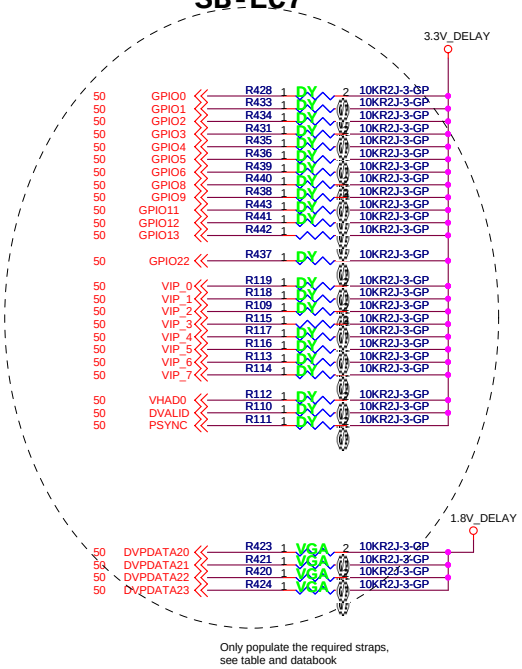
Friday, February 15, 2008
54
56

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

SB-EC7



Only populate the required straps, see table and databook

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **STRAPS**

Size: A3 | Document Number: **X17** | Rev: **SA**

Date: Friday, February 15, 2008 | Sheet 55 of 56

H1 HOLE H2 HOLE H3 HOLE H4 HOLE H5 HOLE

H10 HOLE H6 HOLE H7 HOLE H8 HOLE H9 HOLE

H15 HOLE H11 HOLE H12 HOLE H13 HOLE H14 HOLE

H20 HOLE H16 HOLE H17 HOLE H18 HOLE H19 HOLE

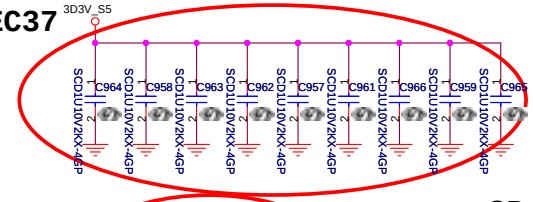
H25 HOLE H21 HOLE H22 HOLE H24 HOLE

H27 HOLE H26 HOLE H28 HOLE H29 HOLE

SB-EC35

EMI Power

SB-EC37



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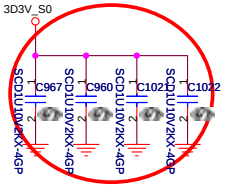

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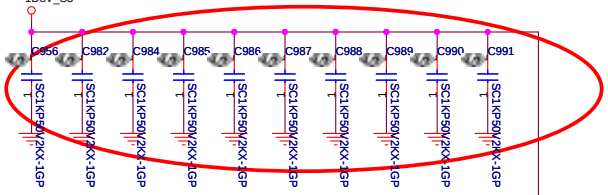

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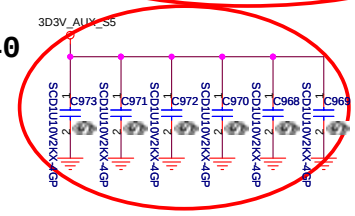

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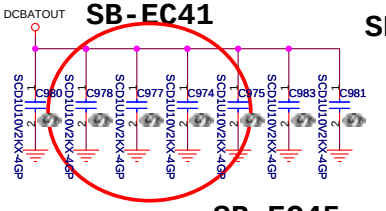

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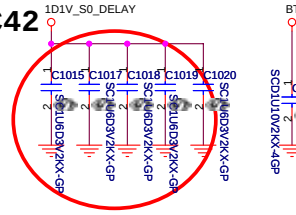

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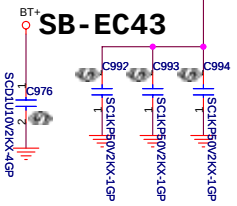

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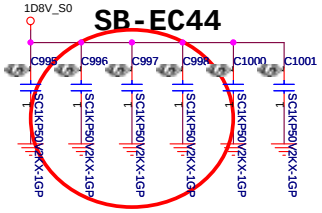

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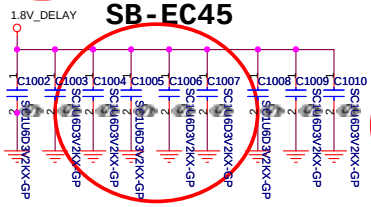

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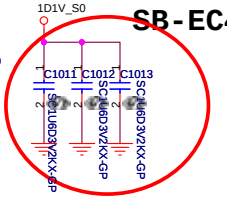

SB-EC36

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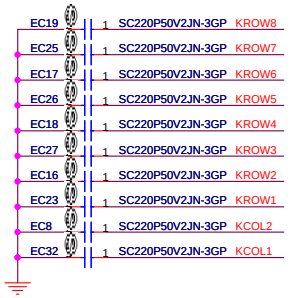
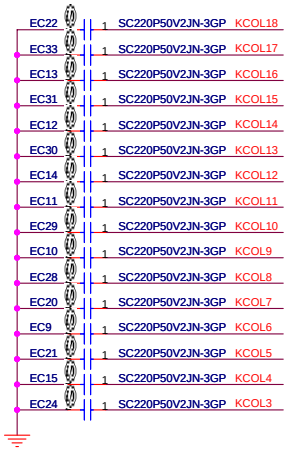
34.39S07.001 34.49T19.001 34.4B312.002 34.39S07.001

-SB ME

Keyboard EMI Caps





36,37 KROW[1..8]

36,37 KCOL[1..18]

<Variant Name>

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Title: **EMI**

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