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03	Change List	1A	
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05	HSW MCP(MEMORY/GND)	1A	
06	HSW MCP(CFG/PwrMGT)	1A	
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10	HSW PCH(CLK/LPC/SPI/SMB)	1A	
11	HSW PCH(GPIO/LPIO/MISC)	1A	
12	HSW PCH(POWER)	1A	
13	DDR3L MEMORY x 16(CHA)	1A	
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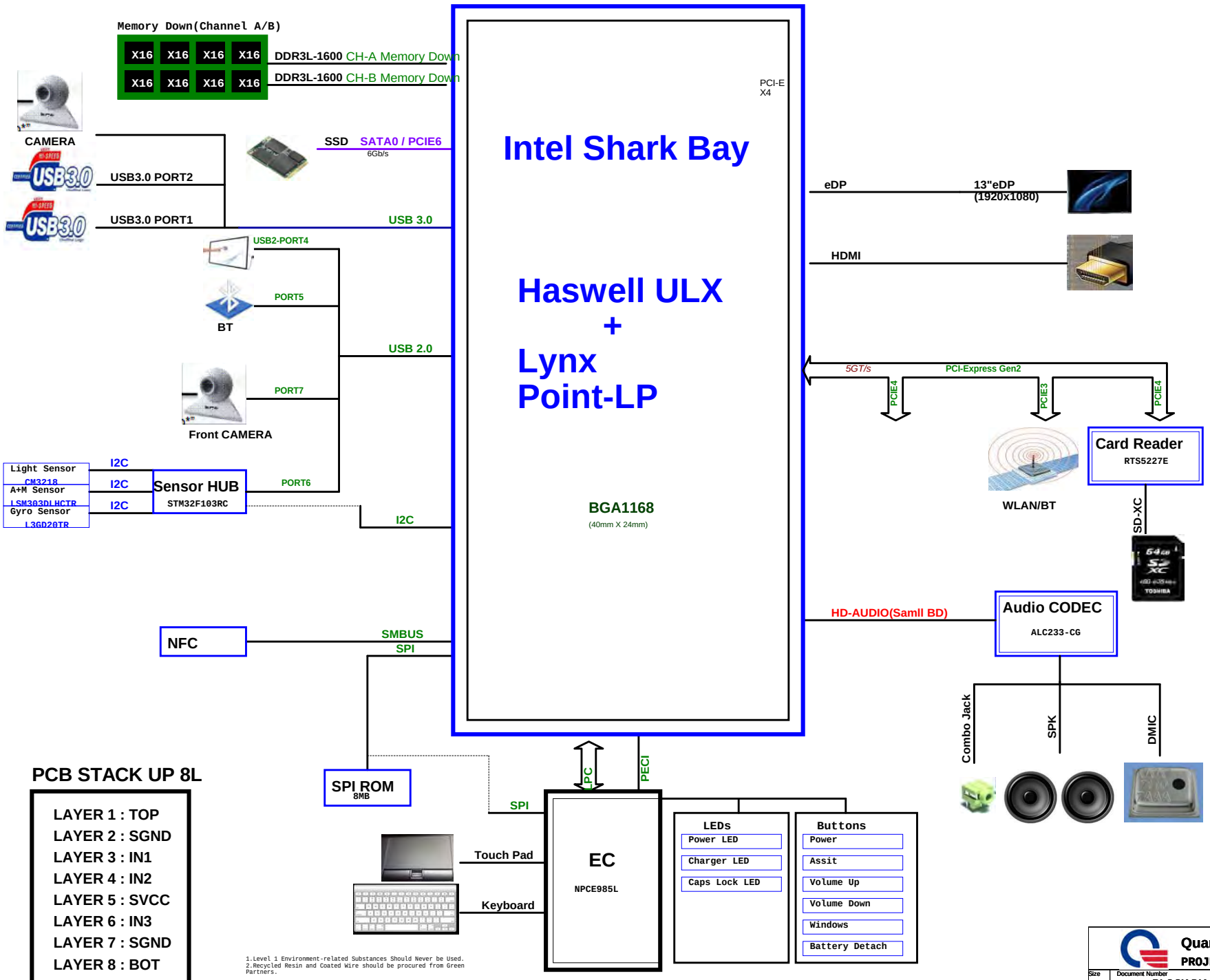
21	Rear Camera	1A	
22	NGFF WLAN/KB-BL	1A	
23	NGFF SSD/TP/FAN	1A	
24	Audio ALC233-CG CON	1A	
25	SWITCH/LED	1A	
26	POWER +VCC_CORE (NCP81101)	1A	
27	POWER 3VPCU&RVCC5(TPS51427)	1A	
28	POWER 1.35VSUS/VTT_MEM	1A	
29	POWER +1.05V(G5602R41U)	1A	
30	POWER(BAT IN / ADA IN/ UL)	1A	
31	POWER CHARGER (ISL88732)	1A	
32	BLANK	1A	
33	TPM CON	1A	
34	BLANK	1A	
35	BLANK	1A	
36	Sensors Hub & Sensors	1A	
37	BLANK	1A	
38	SMBUS	1A	
39	Power Table	1A	

Page	Title of schematic page	Rev.	Date
40	Power Design Diagram	1A	
		1A	
		1A	
		1A	

1

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

Mule BLOCK DIAGRAM



PCB STACK UP 8L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

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Change List

DVT-2013-05-05

P15 Add serial resistor RP11~RP16 on K/B matrix

Reason :For ESD protection
Possible Risk: no

DVT-2013-05-05

P4 Change netname of GPIO 78 from EC_A20GATE to GPIO78

P16 Remove EC_A20GATE

Reason : EC_A20GATE is not necessary

DVT-2013-05-05

P9 PCH GPIO29 use for WLAN_PW_EN
Reason :Change the power well of WLAN_PW_EN from sus to DSW. .

DVT-2013-05-05
P20 Add R24460 without mount for TPS2543 .
Reason :Reserve for TPS2543 .

DVT-2013-05-05
P22 remove R671,R673 for cost down .

DVT-2013-05-05
P22 change R2442 from unmout to mount
P22 change R656 from mout to unmount
Reason :Change PLTRST#_WLAN instead of PLTRST for RTD3

DVT-2013-05-05
P22 Add a AND gate U30 for WLAN power enable
P16 add GPIO84 for EC_WLAN_PWR_EN

DVT-2013-05-05
P22 Change WLAN_WAKE# PU power well from +3V_S5 to +3V_S5_DSW .

Reason :The signal is belong to" DSW " power well

DVT-2013-05-06

P15 unmount KB 220P (C184~C207)

DVT-2013-05-08

P9 Add TP150 for ME

DVT-2013-05-10

P23 Add U54 for SATA & PCIE Detect

P23 Add +3.3V PU R24461 10Kohm

DVT-2013-05-10
P12 Add C302 0.47uf capacitor for inrush current.(VCCDSW3_3)

DVT-2013-05-10

P17 Add mode_lid-2# signal

P16 Add KR28 PU and change EC GPIO32 from IMVP_PWRGD to MODE_LID-2#

DVT-2013-05-10

P25 remove CN2 and add SW3 ,SW4

DVT-2013-05-10

P18 MR2,MR3 mount

DVT-2013-05-11

P19 R200,R202 change from 2.2k to 4.7k for VEVS 7-1 DDC 130ohm test item

DVT-2013-05-13

P16 Change EC GPIO55 from DRAM_VOLTAGE_SET to SIO_WAKE_GPIO27#

P11 GPIO27 add SIO_WAKE_GPIO27# From EC

DVT-2013-05-13

P8 Change Y1 package for Broadwell requirement

DVT-2013-05-13

P8 Change Y1 package for Broadwell requirement

DVT-2013-05-13
P16 Add KC16 150 pF for EC_PECI

DVT-2013-05-14

P11 Add R24462 100K pull down for CR_PW_EN and unmount R297

DVT-2013-05-14

P36 Change U29 to AL000527000 and power source from +5V_WAKE to +3V_WAKE

P36 Add R24470 ,R24469 to PD,R2449 mount, remove R2450

P36 Add R24471 to PD

P36 Remove R2384 and mount R2451

P36 Add R24472 for SH_ALS_INT# PU

DVT-2013-05-14

P21 mount L2007,L2008,L2009

DVT-2013-05-14

P18 Change MR12,MR13,MR14,MR15,MR16,MR17 from 43ohm to 20 ohm

DVT-2013-05-15
P15 remove H19

DVT-2013-05-16
P17 Change U51 as AL000527000
P17 Change R2413 as 40.2K ohm and mount;Change R24455 as 100Kohm
P17 remove R258,R259,R2436,R2435

DVT-2013-05-16

P11 Change R2433,R304,R310,R308,R297,R306 from mount to un-mount .

DVT-2013-05-16

P4 Change the netname of GPIO77 from EC_EXT_SMI# to GPIO77
P8 Change the netname of GPIO35 from GPIO35 to EC_EXT_SMI#

DVT-2013-05-16

P16 Add KD5 for EC_PWROK

DVT-2013-05-16

P17 Change U52 from G5254T11U to G527ATP11U

P17 mount R258 40.2k ohm and change R24456 as 100k ohm

P17 Change U26 from G5254T11U to G527ATP11U

P17 mount R2436 40.2k ohm and change R24454 as 100k ohm

DVT-2013-05-19

P21 Change U53 from G5254T11U to G527ATP11U

P21 Change R2431 to 40.2Kohm and Add R24473 as 100K ohm

DVT-2013-05-19

P22 Change U27 to G547E1P81U

P22 Delete R2454

DVT-2013-05-19

P4 Change R271,R272,R273,R274,R275,R276,R277 to 100Kohm

DVT-2013-05-19

P7 Change R42 as 100Kohm

DVT-2013-05-19

P8 R278,R279,R280,R281 change to 100Kohm, and remove R2048

DVT-2013-05-19
P9 Change R73, R282 from 10k ohm to 100k ohm

DVT-2013-05-19
P10 Change R24474(no mount), R24475, R86 from 10k ohm to 100k ohm,and remove RP4

P11 Change R283, R285, R300, R315, R313, R317,
R311, R296, R290, R291, R301, R303, R305, R307, R309, R312,
R314, R316(no mount), R318, R319, R320, R2433(no mount), R298,
R299, R304(no mount), R295, R310(no mount), R308(no mount),
R284, R112, R24448, R115, R292, R287, R294, R116, R117, R118, R119,
R286, R289, R297(no mount), R128(unmount),R114, R122, R306(no mount),
R125, R126(unmount), R127, R129(no mount), R130,
R131(no mount), R132, R133(no mount), R134, R135(unmount),R293
from 10k ohm to 100k ohm

P16 Change KR2, KR4, KR19, KR26, KR27, KR28 from 10k ohm to 100k ohm
P22 Change R24445,R2446 from 10k ohm to 100k ohm
P4 Change R14,R15 from 10k ohm to 100k ohm

DVT-2013-05-21

P36 U29 PIN1 change +3V_SENSORHUB for optional non CS design
P36 R2451 change +3V_S5 for optional non CS design
P36 change U29 ,C2337,R24469,R2449,R24470 to un-mout

DVT-2013-05-21

P22 Add R24476 0 ohm
P22 Mount R656
P22 Un-mount R2446,R24442,Q34,Q35,R2447,U28,R2442,R2443,U30,C2336

DVT-2013-05-21
P8 Change R62 as 330ohm,change CON1 P/N

DVT-2013-05-22
P20 Add C2432,C2433 0.22uF CAP

DVT-2013-05-22
P23 :TP function mount D8,D9,D10,D11,D12 for ESD

DVT-2013-05-22
P25 :Change SW1 as DHP00XJ1J01

DVT-2013-05-23
P23:change Q8 as BAM34040001

DVT-2013-05-28
P36:Mount R2359,R2361,R2364,R2365,R2367,R2369

DVT-2013-05-23
P24: Add R24477 for EMI

DVT-2013-05-23
P21: Change U45 as AL000918000,U46,U47 as AL000916007
P21: Change R2149,R2147;R786,R790;R2152,R2148

DVT-2013-05-25
P11: Mount R310

DVT-2013-05-25
P17: Change CON6 FP(P/N: DFHS40FS104)

DVT-2013-05-25
P23: Change SW2,SW3,SW4 FP, and reserve D45,D46,D47,D48,C2435,C2436,C2437

DVT-2013-05-25
P4:Add R24480 and Reserve R24478,R24479

DVT-2013-05-25
P8:R24451 change to 15Kohm

DVT-2013-05-25
P18:unmount MC21,MC24,MU2,MC23,MR20,MU3,MR22,MR23,ML4
P18:mount ML2,MR24

DVT-2013-05-27
P19: R186,R187,R189,R190,R192,R193,R195,R196 change to 470 ohm

DVT-2013-05-27
P19: R186,R187,R189,R190,R192,R193,R195,R196 change to 470 ohm

DVT-2013-05-27
P22: Remove R236,Q17,U28,R2442,R2443,U30,R24442,R2446,Q35,R2447,C2336,Q34,R24445,Q36

DVT-2013-05-27
P11:R315 unmount

DVT-2013-05-28
P22:Con14 Change to DFFC04FR066

DVT-2013-05-29
P33:add R24481 33ohm and reserve C2438

DVT-2013-05-29
P17:L10 mount

DVT-2013-05-30
P23:Delete R2407,R2408

DVT-2013-05-30
P7:mount C49 680P

DVT-2013-05-30
P7:mount C49 680P

DVT-2013-05-30
P21:unmount U53,R24473,C2415,R2431,R219 and add R24484 and R24482

DVT-2013-05-31
P19:unmount R185,R188,R191,R194

DVT-2013-05-31
P17:Add U56,R24485

DVT-2013-06-01
P23: remove R342

DVT-2013-06-01
P22: ADD C303,R24486

DVT-2013-06-03
P24: Change F10,F12 footprint

DVT-2013-06-03
P20: Add R24488,R24489,R24490,R24491,R24492,R24493,R24494,R24495

DVT-2013-06-04
P16: Add KR29

DVT-2013-06-04
P19: Add TU3,TC2,TR3,TR4,TQ2

DVT-2013-06-04
P25: Add R24496, R24497

DVT-2013-06-07
P8: Unmount R59,R60,R61,R64,R65,R66

DVT-2013-06-12
P16: Unmount KC16

DVT-2013-06-13
P19: mount R185,R188,R191,R194

DVT-2013-06-19
P25: Change Q25,Q26 PN BA001240Z11

DVT-2013-05-16 (Power Portion)

P27 POWER 3VPCU&RVCC5(TPS51427)
Removed PG1,PG2,+5V_WAKE-1 and +3V_WAKE-1
Reason : DVT is not necessary.

P28 POWER 1.35VSUS/VTT_MEM
Change PCB footprint of PU4 from 21P to 26P
Reason : 21P is incorrect componet.
Removed PC75
Reason : PC75 will lead to delay DDR_PG signal.
Possible : DDR_PG signal will be unstable.
Removed PG3 and +1.35V_SUS-1
Reason : DVT is not necessary.

P29 POWER +1.05V/+1.5V/Thermal
Change PC81 from CH6104K9A00 to CH6104M9901.
Reason : To decrease the temperature of PQ34 and PQ35.
Removed PG4 and +1.05V_M-1
Reason : DVT is not necessary.

P30 POWER(BAT IN / ADAIN /UL)
Change “One-Shot 10ms POCHOT# For ADP/BAT” circuit to “One-Shot 10ms POCHOT# For ADP”.
Reason : Order to fine-tune for new 45W adapter.
Change System OVP for VEDS from “+5V_WAKE-1 ,+3V_WAKE-1, +1.35V_SUS-1 and +1.05V_M-1” to “+5V_WAKE ,+3V_WAKE, +1.35V_SUS and +1.05V”
Reason : +5V_WAKE-1 ,+3V_WAKE-1, +1.35V_SUS-1 and +1.05V_M-1 are removed

P31 POWER CHARGER (ISL88732)
Change PR215 from 95.3K to 140K.
Change PR217 from 34.8K to 31.6K.
Change charge current from 2.81A to 2.688A
Reason : Modify Max Charge Current Limit from 4.5A to 3.2A.

DVT-2013-05-23 (Power Portion)
To change PSW P/N from DHP0TJ42600 to DHP00XJ1J01.
Reason : To change the swich component.
To change PU0 P/N P/N from AL088732000 to AL088732001.
Reason : IC version update.
To add PR196 and to change PC141 P/N from CH21006KB16 to CH5102K9B06.
Reason : To reserve a RC delay time filter in ISENSE_IN route.

DVT-2013-05-29 (Power Portion)
To change PR23 value from 24Kohm to 24.9K.
Reason : To modify the Vhcore Loadline.

To use PC10 1200pF and to close PC9 1000pF.
Reason : To modify the Vhcore load transient.

To use PC21~PC23.
Reason : To modify the Vhcore load transient overshoot.

To correct PU107A into PU104A.
Reason :PU104A and PU104B is a group IC.

DVT-2013-06-05 (Power Portion)

Change PR23 from 24.9K to 23.7K
Change PC170 from 470PF to 220PF
Reason : modify Vhcore’s Dynamic Iout accury.

DVT-2013-06-06 (Power Portion)

Update FI1 Power portion DVT 0606 schematics
To add PR145 430K and PR141 in parallel.
Change PR141 from 470K NTC to 680K NTC
Change PR146 from 6.98K to 0 ohm.
Reason : The minimum temp of PQ36 trigger point will be increased from 86C to 98C

DVT-2013-06-07 (Power Portion)

FI1 power portion 0607 update(for DVT building BOM)
Change PR141,PR146 and PR145 from DVT value to EVT value.
Reason : PR141 680K lack parts.

PVT-2013-07-18 (Power Portion)

P26,P27,P29
Change to Short pad PR7,PR15,PR25,PR27,PR838,PR54,
PR45,PR53,PR55,PR37,PR231,PR96,PR116,PR193
Reason : PVT stage do not need to reserve 0 ohm.

P27 POWER 3VPCU&RVCC5(TPS51427)
Change PC44,PC46 from CH7221M8601 to CH7221MT603
Reason : NEO assign Cap P/N.
Add +1.35V_SUS discharge circuit (PR64,PR65,PR67,PR69,PQ16,PQ17)
Reason : +1.35V_SUS discharge

P29 POWER +1.05V/+1.5V/Thermal
Add PC 151 parallel with the PR220

P30 POWER(BAT IN / ADAIN /UL)
Change PG5 PCB foot print from short pad jumper to RC 0603

P31 POWER CHARGER (ISL88732)
Add PC54 parallel with the P161
Reason : Avoid BAT over voltage.

PVT-2013-07-18

P8: reserve Q46 , R24498 for no power issue

P16:EC GPIO85 add EC_RTC_RST for workaround solution

P12:R138,R139 change to short pad.

P13:DR1,DR2 change to short pad.

P14:DR50,DR53 change to short pad.

P16 KL1,KR25,KR18 change to short pad.

P17 add U58,R24499,R24501,R24500,C2444, remove F6

P22 R619 change to short pad.

PVT-2013-07-19

P17 change F2 footprint

PVT-2013-07-19

P22 Add R24507,R24508 and unmount R24486

PVT-2013-07-19 (Power Portion)

modified 1.35V_SUS discharge ciruit
Reason: change PQ17 from dual package to single package.

PVT-2013-07-21

P10 change R95,R96,R97,R98 to shortpad

P17 change R329 to shortpad

P36 change R2374 to shortpad

P21 delete L2008,L2009

PVT-2013-07-22 (Power Portion)

P31 POWER CHARGER
Added EC176 0.1U/25V/Y5V_4
Reason: EMI suggestion
P30 POWER(BATIN/ADAIN/UL)
Added EC11 0.1U/50V/X7R_6
Reason: EMI suggestion

PVT-2013-07-22

P4 change R24480 to shortpad

P17 change R2437 to shortpad

P17 unmount R24455,R24454 ,C294,C295

P21 change R219 to shortpad

P11 mount R308,R306

P25 Change R226 as 120 ohm,R264 as 300 ohm;
R263 as 680ohm,F18 unmount
P25 Add R24509,R24510 and Q47

PVT-2013-07-23

P17 reserve D24

PVT-2013-07-27

P17 Change the R185,R188,R191,R194 as 330 ohm

PVT-2013-07-29
P17 unmount R24455,R24454 ,C294,C295,R243B,R2448,
mount R24512,R24511

PVT-2013-07-30
P36 Change U20 AR6W08D0000(FW26)

PVT-2013-07-31
P17 R24512 change to 0 ohm

PVT-2013-08-01
P17 change C2331,C2332,C2333 to 2.2u

PVT-2013-08-01
P19 change R208 to 57.6k,R212 to 23.7k
P19 change R206 to 100k,R211 to 42.2k

MP-2013-08-09

P21: Change C932 as 1u
P21: add D49,R24517 , C2446

MP-2013-08-10

P10: Add R24518,R24519,R24520,R24521,R24522

P23: Change C330,C317,C319 and reserve C2447

MP-2013-08-11
P19: remove R185,R188,R191,R194 as 330 ohm,
add C2448,C2449,C2450,C2451

MP-2013-08-16
P21: R804, R2145 change to 0 ohm
P17: Change F2

03

Quanta Computer Inc.
PROJECT : FI1

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	Change List	1A
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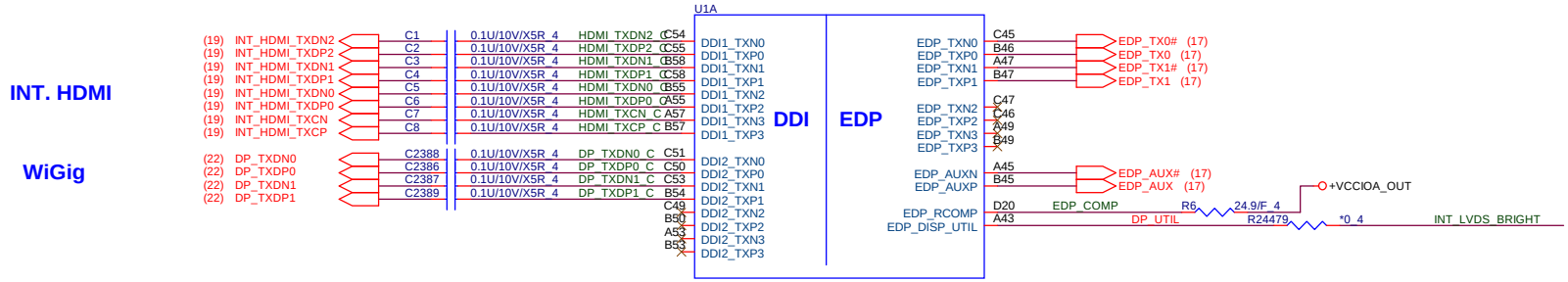
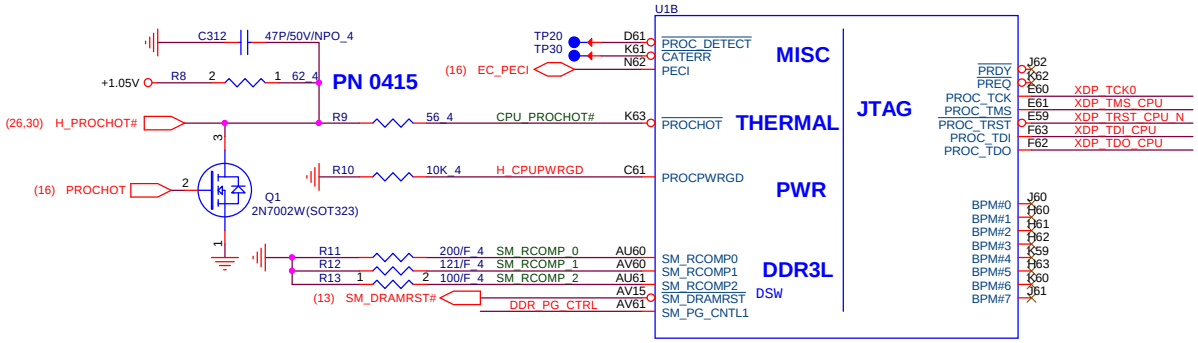
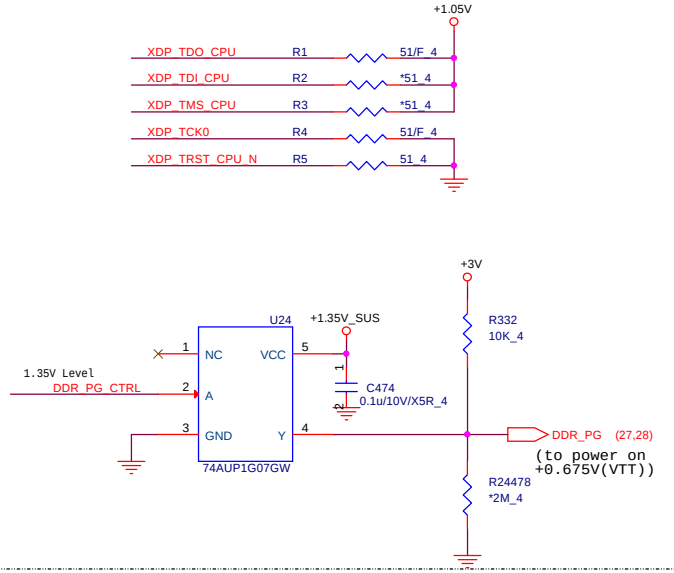
Haswell ULT (DISPLAY)

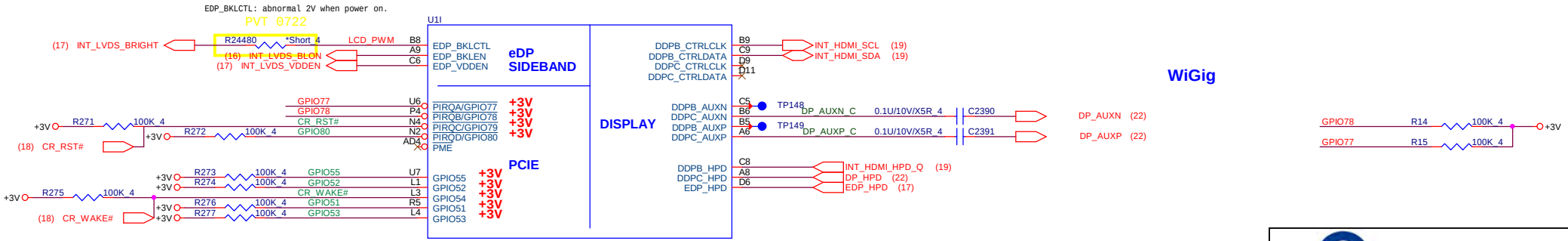
INT. HDMI

WiGig









WiGig

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Quanta Computer Inc.

PROJECT : FI1

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	HSW MCP(Display/eDP)	1A
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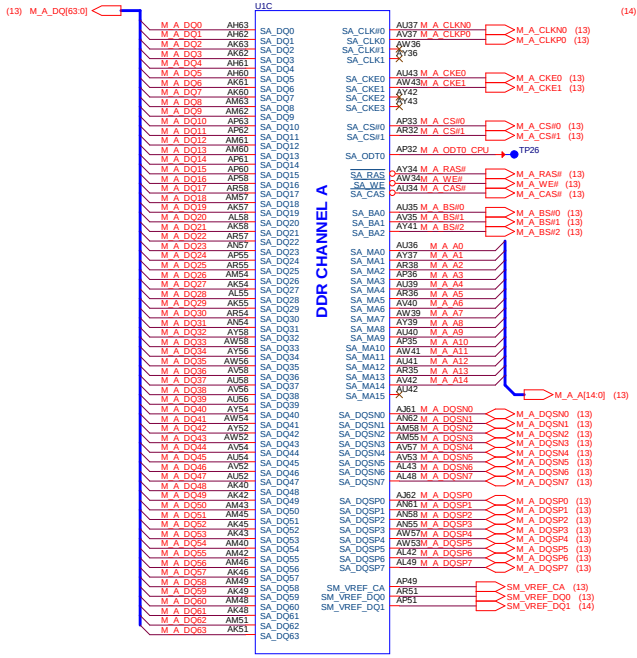
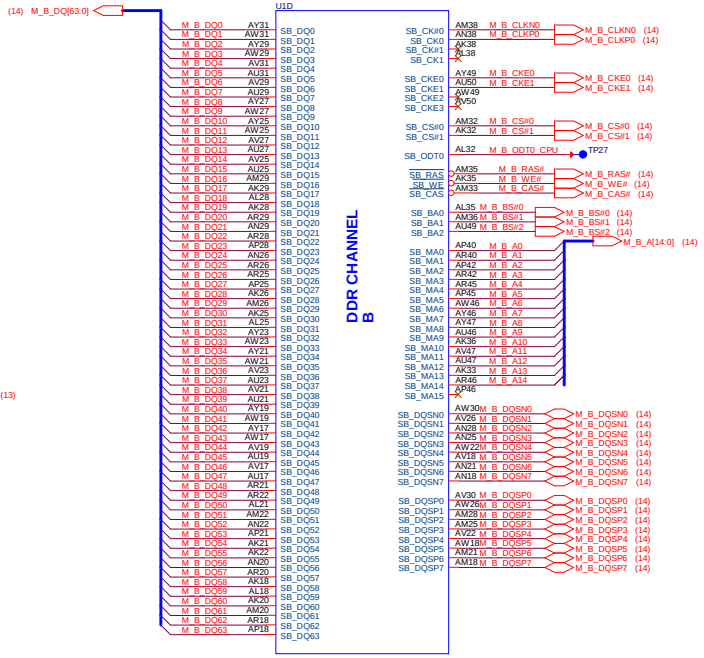
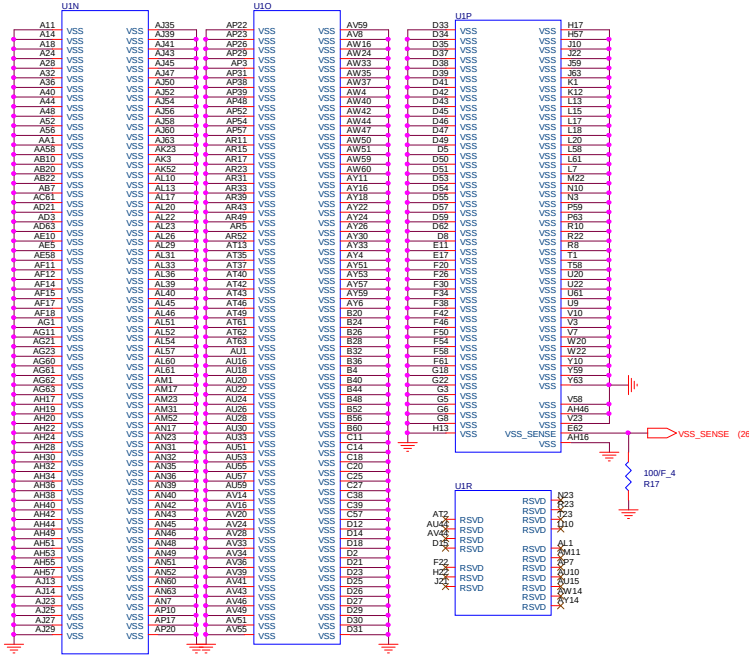
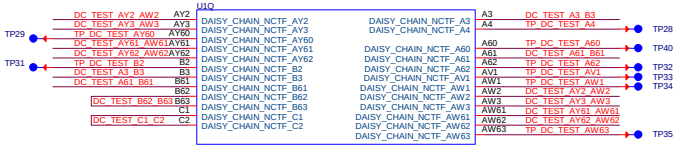
Haswell ULT (DDR3L)





HSW ULT(GND)





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Quanta Computer Inc.
PROJECT :FI1

Size	Document Number	Rev
	HSW MCP(Memory)	1A
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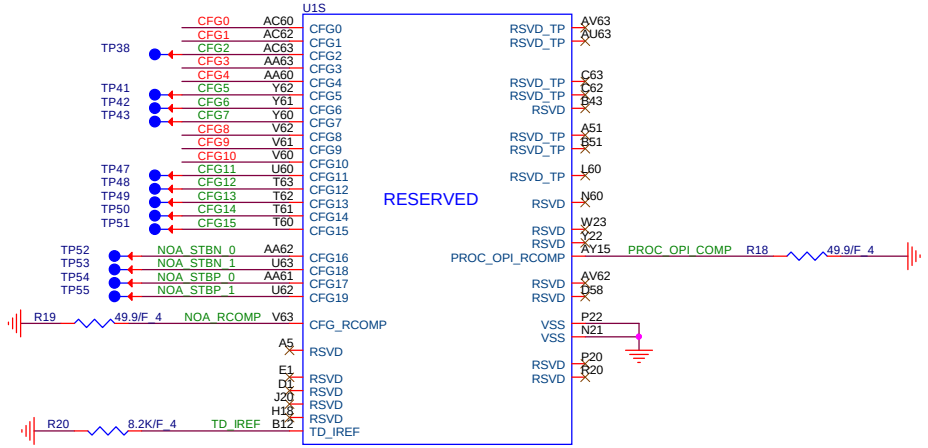

Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R21 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R22 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R23 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG4 R24 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG8 R25 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R26 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R27 *1K_4

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Haswell ULT MCP(POWER)

+1.35V_SUS

C2420 3.3P/50V/NPO_4
2.2uF *4
10uF *6

C11 10/u/6.3V/X5R_6
C13 10/u/6.3V/X5R_6
C15 10/u/6.3V/X5R_6
C17 10/u/6.3V/X5R_6
C19 10/u/6.3V/X5R_6
C21 10/u/6.3V/X5R_6

C24 2.2u/6.3V/X5R_4
C26 2.2u/6.3V/X5R_4
C28 2.2u/6.3V/X5R_4
C30 2.2u/6.3V/X5R_4

+VCC_CORE

Haswell ULT 15W : 32A

C9 22u/6.3V/X5R_6
C10 22u/6.3V/X5R_6
C12 22u/6.3V/X5R_6
C14 22u/6.3V/X5R_6
C16 *22u/6.3V/X5R_6
C18 22u/6.3V/X5R_6
C20 22u/6.3V/X5R_6
C22 22u/6.3V/X5R_6
C23 *22u/6.3V/X5R_6
C25 22u/6.3V/X5R_6
C27 22u/6.3V/X5R_6
C29 22u/6.3V/X5R_6
C31 22u/6.3V/X5R_6
C32 22u/6.3V/X5R_6
C33 *22u/6.3V/X5R_6
C34 22u/6.3V/X5R_6
C35 *22u/6.3V/X5R_6
C36 *22u/6.3V/X5R_6
C37 22u/6.3V/X5R_6
C38 22u/6.3V/X5R_6
C39 22u/6.3V/X5R_6
C40 22u/6.3V/X5R_6
C41 22u/6.3V/X5R_6
C42 22u/6.3V/X5R_6
C43 *22u/6.3V/X5R_6
C44 22u/6.3V/X5R_6
C45 22u/6.3V/X5R_6
C46 22u/6.3V/X5R_6
C47 22u/6.3V/X5R_6
C48 *22u/6.3V/X5R_6

U1L

+1.35V_SUS (VDDQ : 4.2A)

AH26 AJ31 AJ33 AJ37 AN33 AP43 AR48 AY35 AY40 AY44 AY50 — VDDQ

+VCC_CORE

F59 N58 AC58 — VCC RSVD RSVD

+VCC_CORE R35 100/F_4 (26) VCC_SENSE

E63 AB23 A59 — VCC_SENSE RSVD VCCIO_OUT

TP90

+VCCIO_OUT E20 — VCCIO_OUT

+VCCIOA_OUT AD23 AA23 AE59 — VCCIOA_OUT RSVD RSVD RSVD

HSW ULT POWER

VR_EN(1.05V): Output to disable VR in C10
VR_Ready(1.05v):

H_CPU_SVIDALRT_N L62 — VIDALERT
VR_SVID_CLK N63 — VIDSCLK
VR_SVID_DATA L63 — VIDSOUT
VCCST_PWRGD B59 — VCCST_PWRGD

(26) H_VR_ENABLE_MCP R36 10K_4 VR_READY C59 — VR_EN VR_READY

F60 — VSS

+V1.05S_VCCST R39 150/F_4 FIVR_EN_BUF H59 — PWR_DEBUG

D63 P62 P60 P61 N59 N61 T59 AD60 AD59 AA59 AE60 AC59 AG58 U59 V59 — VSS RSVD_TP RSVD_TP RSVD_TP RSVD_TP RSVD RSVD RSVD RSVD RSVD RSVD RSVD RSVD RSVD

VCCST_PWRGD(O/D Input):
VCC/VDDQ/CLK stable

+V1.05S_VCCST
+1.05V R40 1 2 0_6

AC22 AE22 AE23 — VCCST VCCST VCCST

AB57 AD57 AG57 C24 C28 C32 — VCC VCC VCC VCC VCC VCC

+VCC_CORE

VCC: C36 C40 C44 C48 C52 C56 E23 E25 E27 E29 E31 E33 E35 E37 E39 E41 E43 E45 E47 E49 E51 E53 E55 E57 F24 F28 F32 F36 F40 F44 F48 F52 F56 G23 G25 G27 G29 G31 G33 G35 G37 G39 G41 G43 G45 G47 G49 G51 G53 G55 G57 H23 J23 K23 K57 L22 M23 M57 P57 U57 W57

23 X 22UF(0805 MLCC)

SVID ALERT

+1.05V
close to CPU
R28 75_4
H_CPU_SVIDALRT_N R30 43_4 VR_SVID_ALERT# (26)

SVID DATA

close to CPU
+1.05V
R31 130_4

close to VR
+1.05V
R33 130_4

VR_SVID_DATA VR_SVID_DATA (26)

close to VR
+1.05V
R37 54.9_4
VR_SVID_CLK VR_SVID_CLK (26)

+3V_S5 +V1.05S_VCCST

R41 100K_4
R42 100K_4

(9,16) EC_PWROK

VCCST_PWRGD

Q2 2N7002DW

C49 680p/50V/X5R_4

+3V +3V_S5

R43 100K_4
R44 100K_4

(26) IMVP_PWRGD

VR_READY

Q3 2N7002DW

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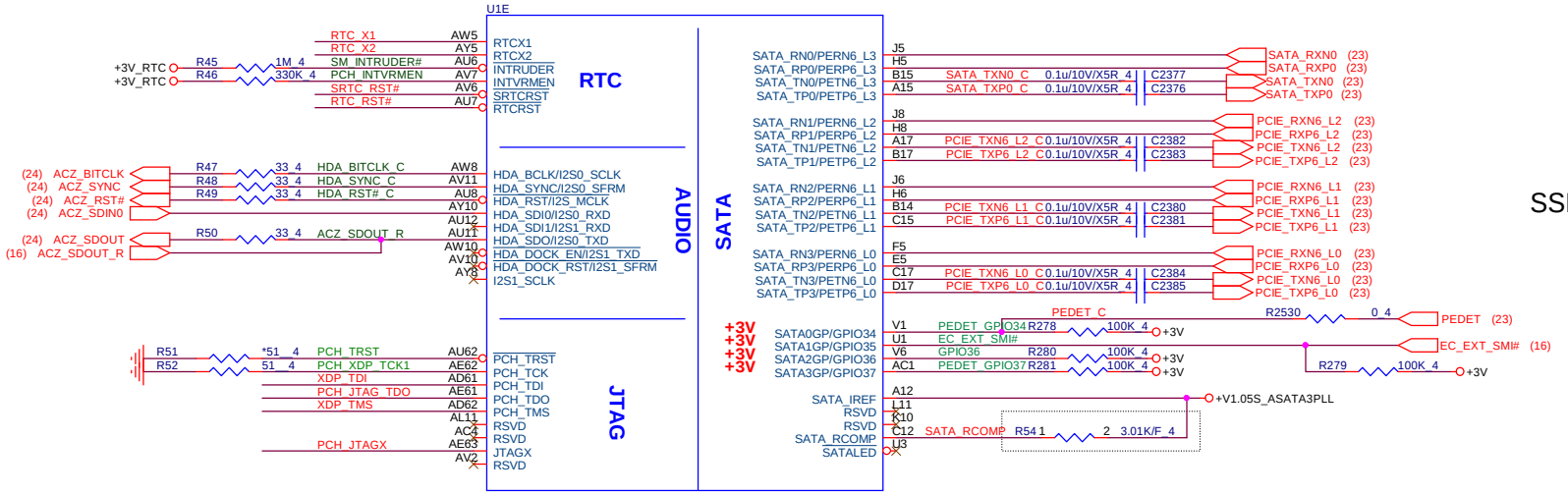
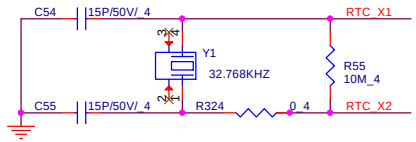
Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW MCP(Power)	1A
Date: Monday, August 19, 2013	Sheet 7 of 40	

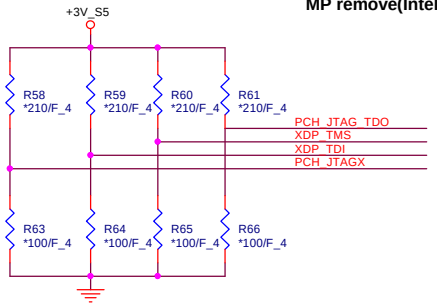
Haswell ULT (RTC, HDA, JTAG, SATA)

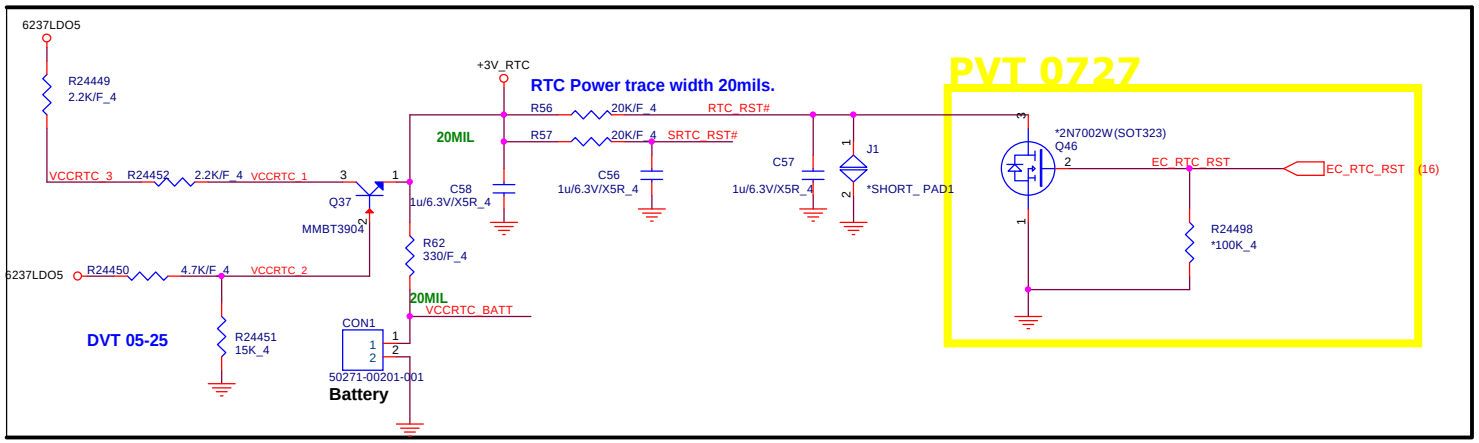




PCH JTAG Debug (CLG)

MP remove(Intel)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R67 *1K_4 SPKR (11,24)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(RTC/HDA/SATA)	1A

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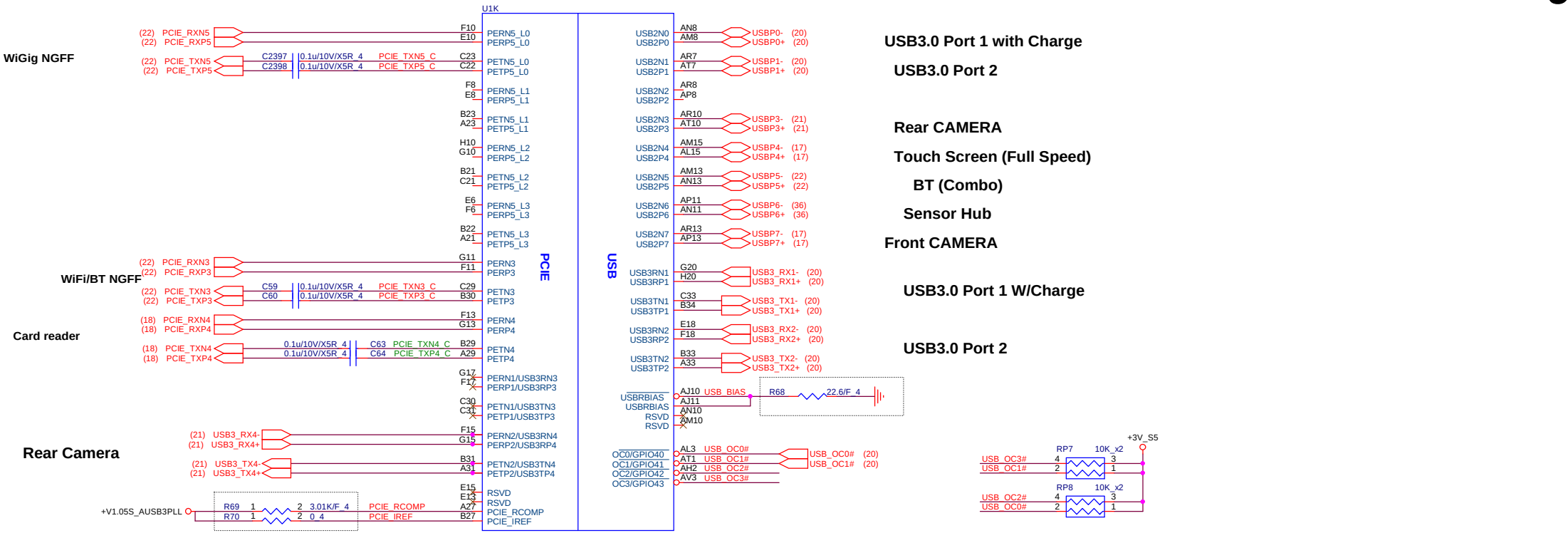
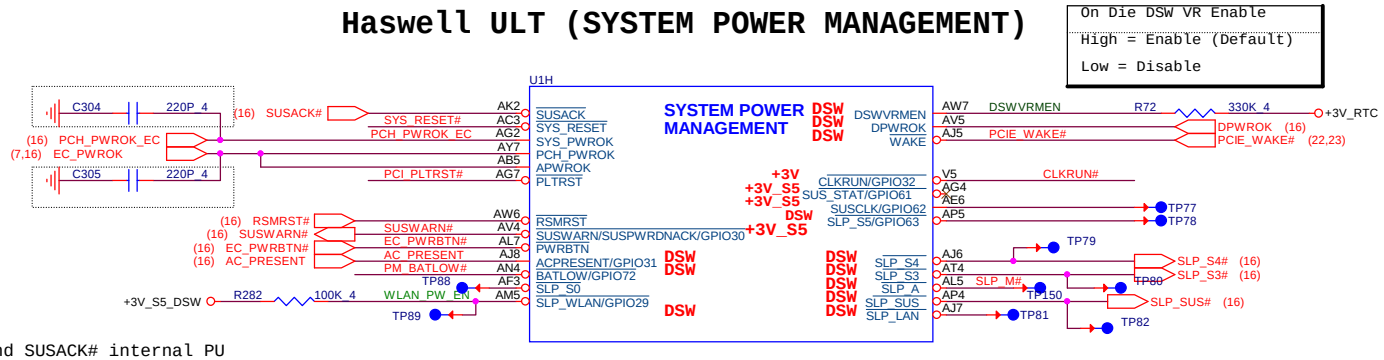
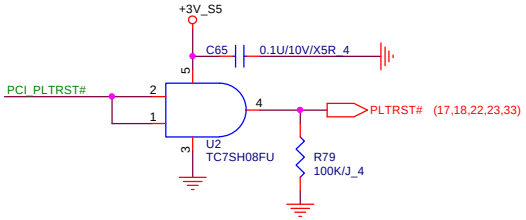
Haswell ULT (PCIE,USB)



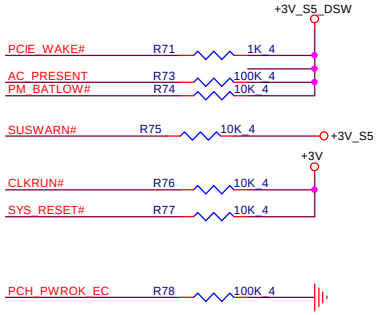
Haswell ULT (SYSTEM POWER MANAGEMENT)



PWRBTN# and SUSACK# internal PU



PCH Pull-high/low(CLG)



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Quanta Computer Inc.		
PROJECT : FI1		
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	HSW PCH(PCIE/USB)	1A
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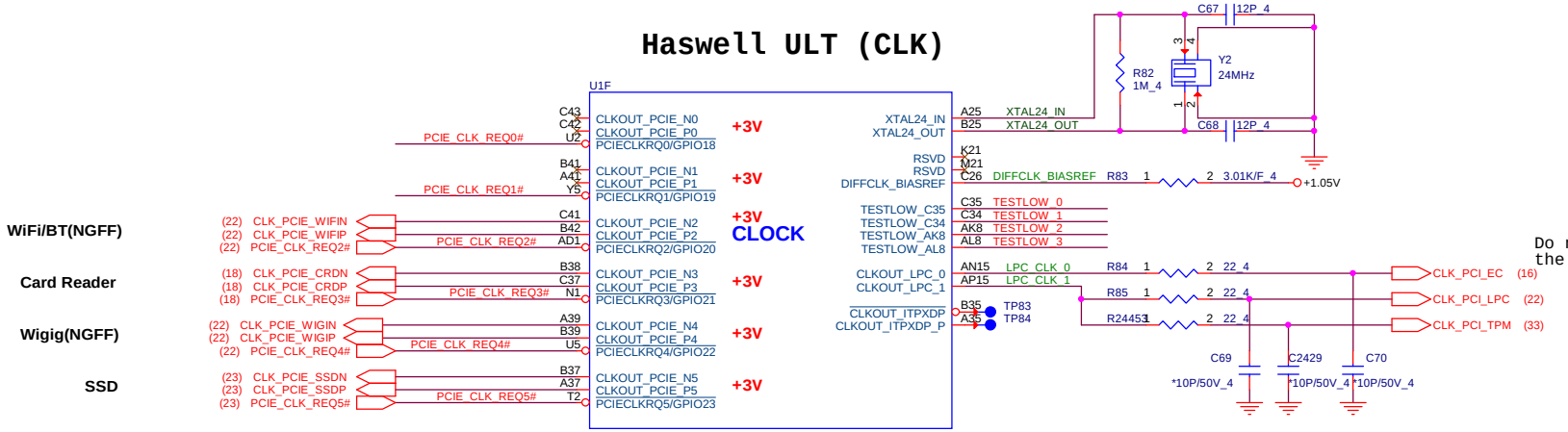
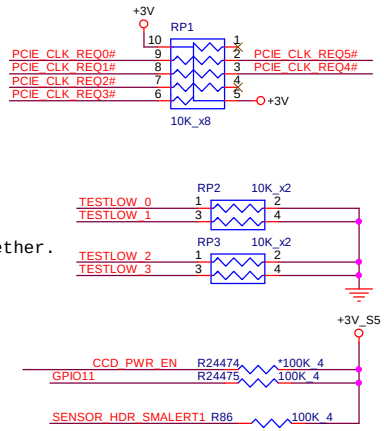
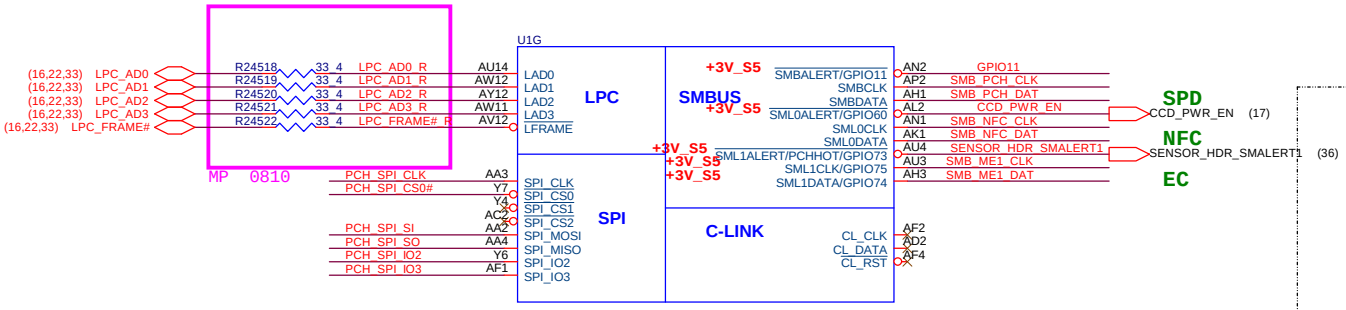
Haswell ULT (CLK)



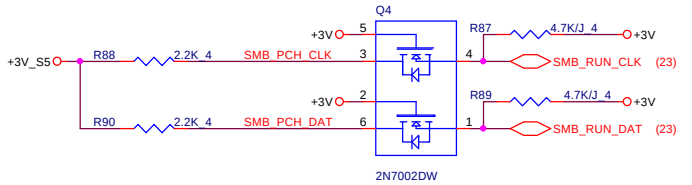
Do not short
the testlow pins together.

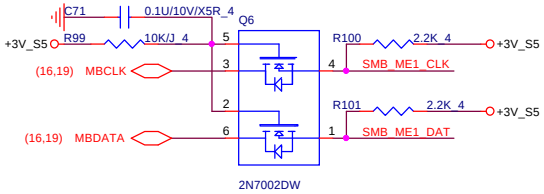


Haswell ULT (LPC/SPI/SMB/CLINK)

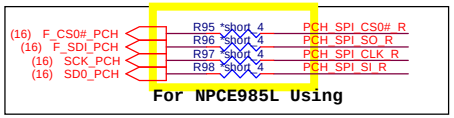


SMBus/Pull-up(CLG)

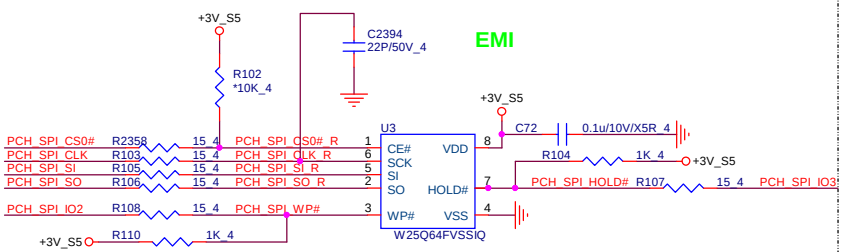




PVT 0721



SPI FLASH



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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	1A
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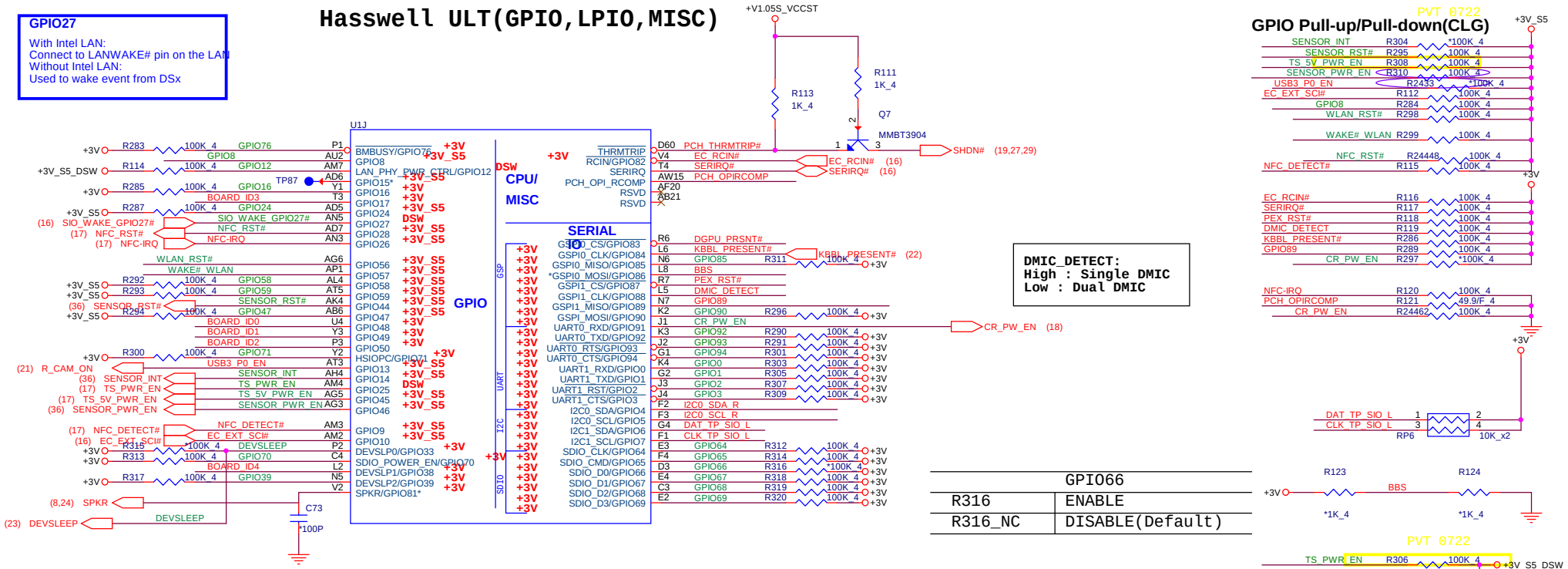
Hasswell ULT(GPIO,LPIO,MISC)

GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



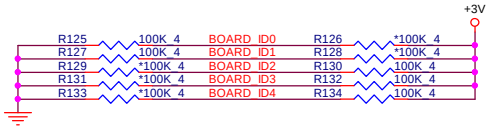
	GPIO66
R316	ENABLE
R316_NC	DISABLE(Default)

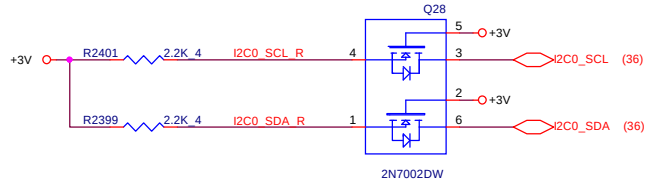
PVT 0722

GPIO Pull-up/Pull-down(CLG)

PVT 0722

Vendor	Vendor Part Number	BOARD_ID2	BOARD_ID3	BOARD_ID4
Elpida(4G)	EDJ4216EFBG-GN-F	0	0	0
Samsung(4G)	K4B4G1646B-HYK0	0	0	1
Hynix(4G)	H5TC4G63AFR-PBA	0	1	0
Elpida(8G)	EDJ8416E6MB-GN-F	0	1	1
Samsung(8G)	K4B8G1646B-MYK0	1	0	0
Hynix(8G)	H5TC8G63AMR-PBA	1	0	1
		1	1	0
		1	1	1





	R127(Low) R128(High) Board ID1	R125(Low) R126(High) Board ID0
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(GPIO/MISC)	1A
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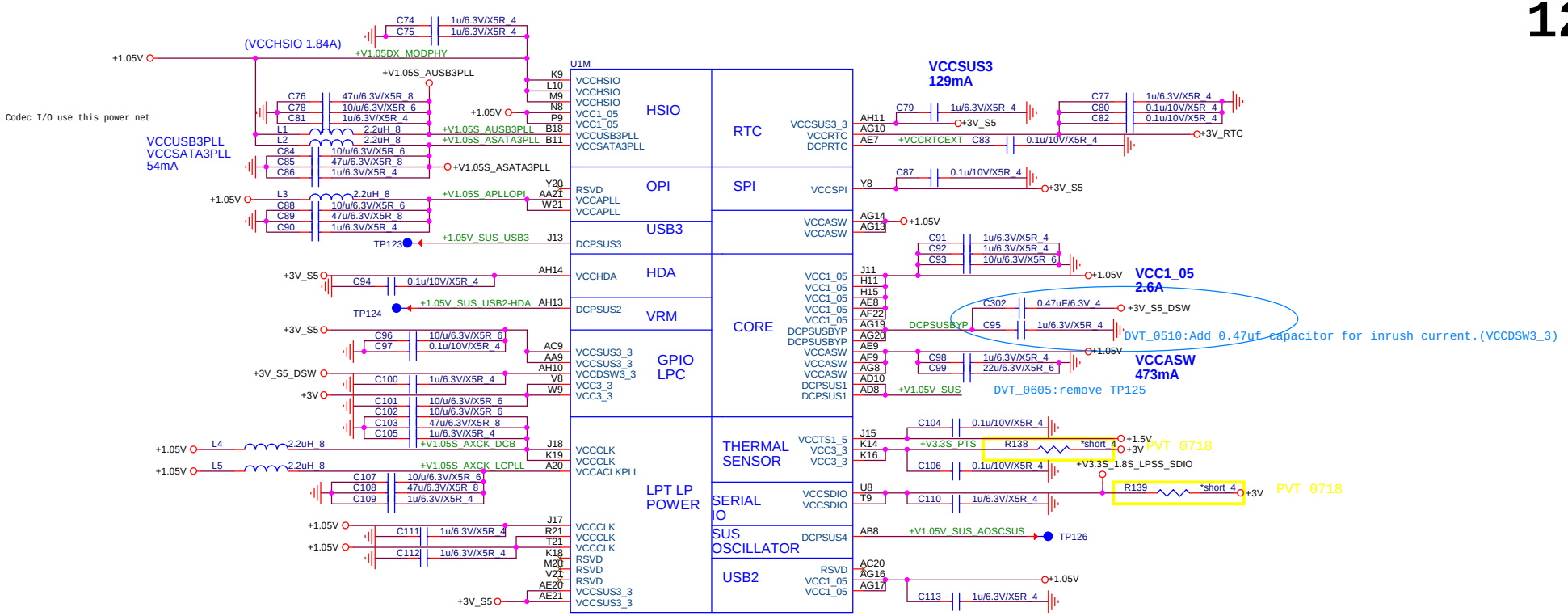
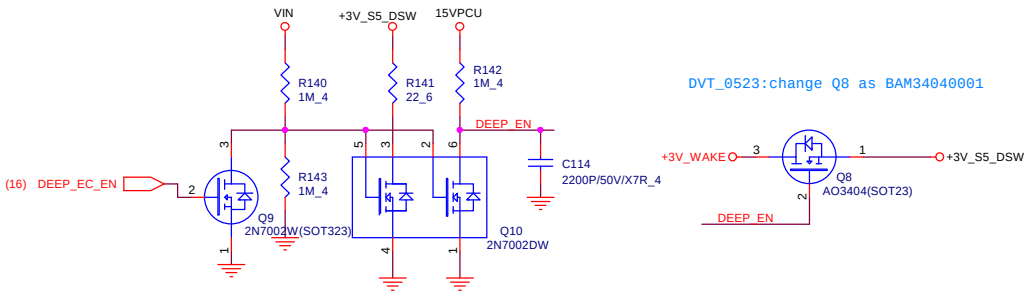


DEEP STANDBY



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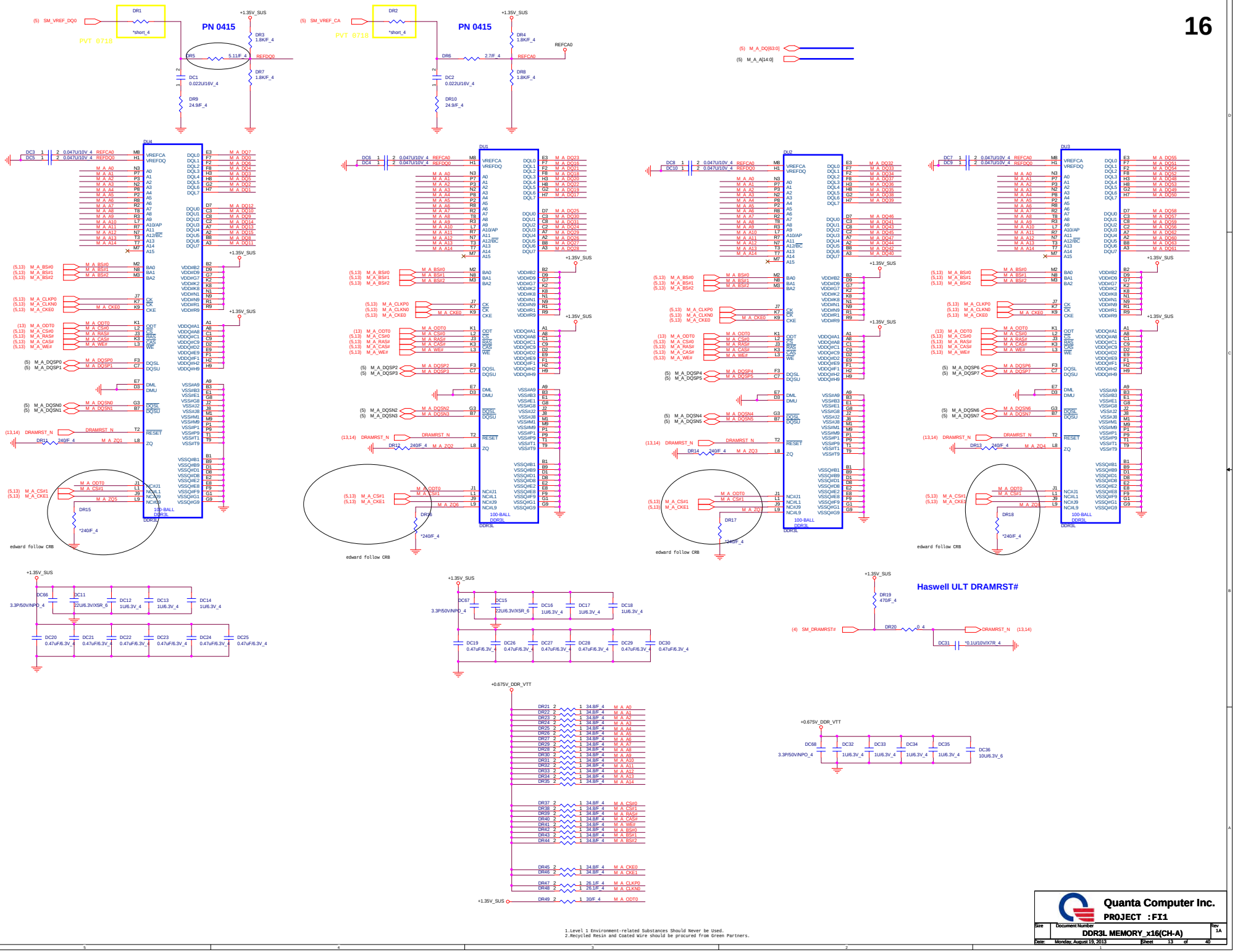
Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HSW PCH(Power)	1A
Date: Monday, August 19, 2013	Sheet 12 of 40	


PN 0415
PVT 0718
*short_4
*240/F_4
edward follow CRB
Haswell ULT DRAMRST#
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.
Quanta Computer Inc.
PROJECT :FI1
DDR3L MEMORY_x16(CH-A)
Size
Document Number
Rev
1A
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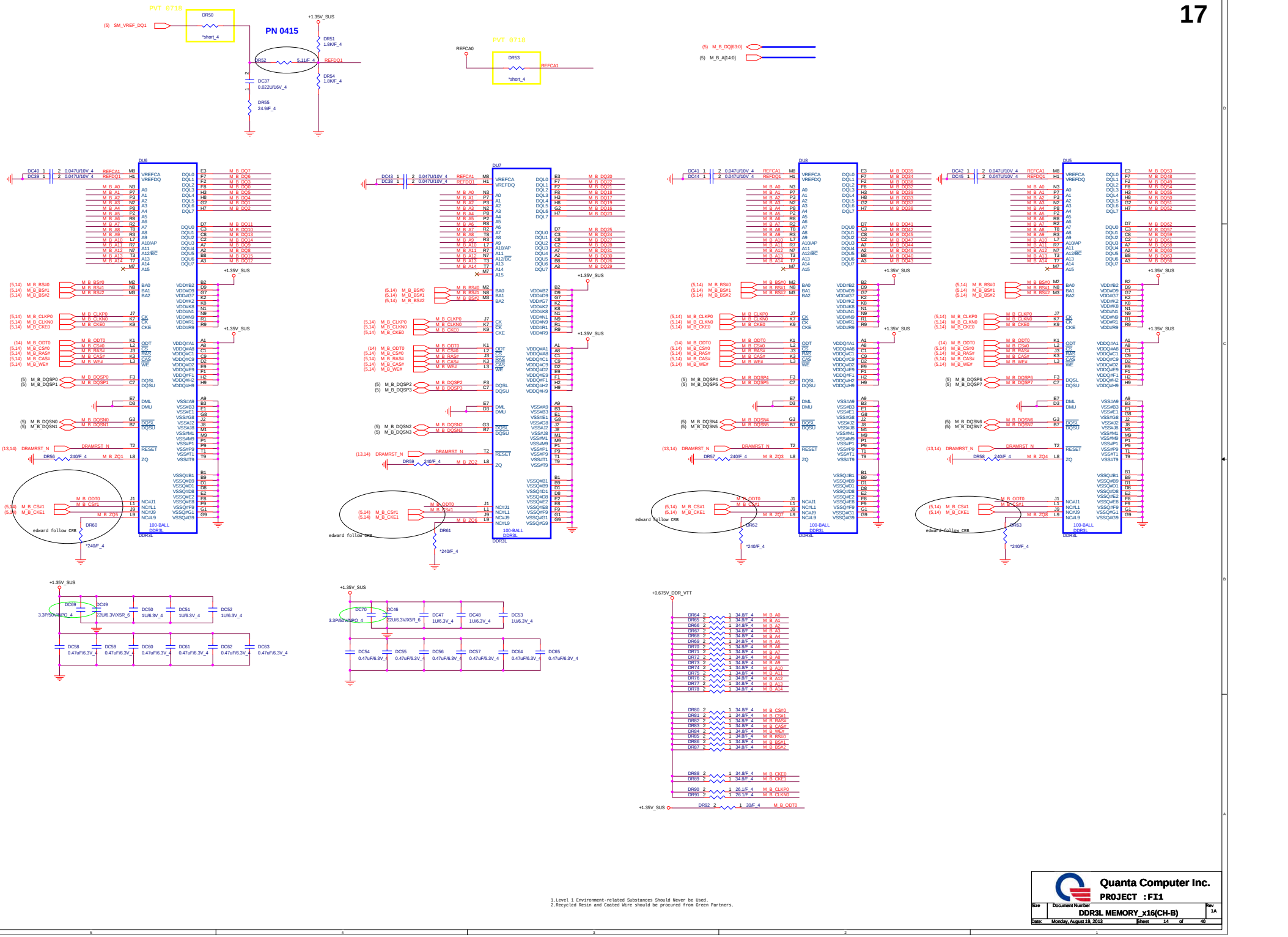

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Quanta Computer Inc.			
PROJECT : FI1			
Size	Document Number		Rev
	DDR3L MEMORY_x16(CH-B)		1A
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H1 *H-C256D91P2
H2 *O-HKD-3
H3 *o-fi1-1
H4 *H-C256D91P2
H5 *O-HKD-3
H6 *H-C256D91P2
H7 *H-C217D91P2
H26 *H-C91D91N
H8 *H-C256D91P2
H9 *H-C256D91P2
H10 *H-TR295X256D91P2
H11 *O-HKD-3
H12 *O-FI1-2
H13 *H-C91D91N
H15 *H-C91D91N
H27 *H-C91D91N
H16 *H-C276D150P2
H17 *H-C276D150P2
H18 *H-C276D150P2
H20 *H-C91D91N
DVT 05-15 remove H19
H21 *O-FI1-4
H24 *O-FI1-3
H22 *H-C91D91N
H23 *H-C91D91N
H25 *H-C91D91N

+3V_S5 +1.05V
C441 1000P/50V/X7R/10%_4
+VCC_CORE
C442 1000P/50V/X7R/10%_4
C443 1000P/50V/X7R/10%_4
C444 1000P/50V/X7R/10%_4

VIN
C450 1000P/50V/X7R/10%_4
C451 1000P/50V/X7R/10%_4
C452 1000P/50V/X7R/10%_4
C458 1000P/50V/X7R/10%_4
C459 1000P/50V/X7R/10%_4
C460 1000P/50V/X7R/10%_4
C461 1000P/50V/X7R/10%_4
C462 1000P/50V/X7R/10%_4
C463 1000P/50V/X7R/10%_4
C464 1000P/50V/X7R/10%_4
C465 1000P/50V/X7R/10%_4
C466 1000P/50V/X7R/10%_4
C453 0.1U/25V/Y5V_4
C454 0.1U/25V/Y5V_4
C455 0.1U/25V/Y5V_4
C456 0.1U/25V/Y5V_4
C457 0.1U/25V/Y5V_4

0327 reverse

KEY BOARD Connector

CON4
KB_ACS(88513-260N)
DVT-2013-05-05

DVT 05-13 SWAP

+3VPCU
MX0 R172 10K/J_4
MX1 R173 10K/J_4
MX2 R174 10K/J_4
MX3 R175 10K/J_4
MX4 R176 10K/J_4
MX5 R177 10K/J_4
MX6 R178 10K/J_4
MX7 R179 10K/J_4

+3V
(16) CAPSLED#
Q32 DTA124EU
R2428 150/F_4
CAPSLED

+3V +1.05V
C431 1000P/50V/X7R/10%_4
+3V_S5 +3V
C433 1000P/50V/X7R/10%_4
+3V
C434 1000P/50V/X7R/10%_4
C435 1000P/50V/X7R/10%_4
+5V_WAKE
C437 1000P/50V/X7R/10%_4
C438 1000P/50V/X7R/10%_4
+3V_S5
C439 1000P/50V/X7R/10%_4
C440 1000P/50V/X7R/10%_4

+3VPCU
C470 1000P/50V/X7R/10%_4
C471 0.1U/25V/Y5V_4
C472 1000P/50V/X7R/10%_4
C473 1000P/50V/X7R/10%_4

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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HOLE/EMI/KB	1A

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New ADD

**** Straping Pin,Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

PVT-2013-07-18

PVT-2013-05-19

Magnetic Lid Switch

KU2
+3VPCU 1 IN OUT 2 LID#
GND 3
E-CMOS

E-CMOS :AL002618001/EC2618NLB1GR
PROLIFIC : AL003661003/PT3661-BB
BCD : AL009249000/AH9249NTR-G1

KU1 PC985L_0

LPC: LAD0/GPIOF1, LAD1/GPIOF2, LAD2/GPIOF3, LAD3/GPIOF4, LRESET#/GPIOF7, LCLK/GPIOF5, LFRAME#/GPIOF6
A/D: AD0/GPIO90, AD1/GPIO91, AD2/GPIO92, AD3/GPIO93, AD4/GPIO05, AD5/GPIO04, AD6/GPIO03, AD7/GPIO07/VD_IN2
D/A: DA0/GPIO94, DA1/GPIO95, DA2/GPIO96, DA3/GPIO97
PWM: A_PWM0/GPIO15, B_PWM/GPIO21, C_PWM/GPIO13, D_PWM/GPIO32, H_PWM/GPIO33/VD1_EN#, G_PWM/GPIO66, E_PWM/GPIO45, F_PWM/GPIO40/1_WIRE
SPI: F_SDI/F_SDIO1, F_SDIO/F_SDIO0, F_SCK, F_CS0#
GPIO: GPIO67/N2TMS, LPCPD#/GPIO10, CLKRUN#/GPIO11, GPIO16, GPIO30/F_WP#, GPIO36, GPIO41/F_WP#, GPIO70, GPIO71, GPIO72, GPIO24, TA1/GPIO56, TMS/GPIO43, SOUT_CR/GPIO83, TDI/GPIO44, GPIO51/N2TCK, GPIO34, TRST#/GPIO46, SIN_CR/GPIO87, PECI, VTT, TCK/GPIO42
K/B: KBSIN0/GPIOA0/N2TCK … KBSIN7/GPIOA7, KBSOUT0/GPOB0/JENK#/SOUT_CR … KBSOUT17/GPIO57
PS/2: RDY#/GPIO52/PSDAT3, TDO/GPIO50/PSCLK3, PSDAT2/GPIO27, PSCLK2/GPIO26, PSDAT1/GPIO35, PSCLK1/GPIO37
PCEI: TA2/GPIO20/IOX_DIN_DIO, TB1/GPIO14, TB2/GPIO01
I/O Expansion: SCL1/GPIO17/N2TCK, SDA1/GPIO22/N2TMS, SCL2/GPIO73/N2TCK, SDA2/GPIO74/N2TMS, SCL3A/GPIO23/N2TCK, SDA3A/GPIO31/N2TMS, SCL4A/GPIO47/N2TCK, SDA4A/GPIO53N2TMS, GPIO00/EXTCLK/F_SDIO3, GPIO06/IOX_DOUT, GPIO82/IOX_LDSH/VD_OUT1, GPIO84/IOX_SCLK/VD_OUT2, CLKOUT/GPIO55/IOX_DIM_DIO, SPI_MISO/GPIO77, **SPI_MOSI/GPO76, SPI_SCK/GPIO75, SPI_CS#/GPIO02, VD_IN1/GPIO80, EXT_RST#, VCORF

VCC POWER ON RESET

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	NPCE885L	1A
Date: Monday, August 19, 2013	Sheet 16 of 40	

Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

Need to confirm total power consumpton

Current limit
Typ:1A(880mA~1120mA)

DMIC

PVT 0718

Current limit
Typ:1A(880mA~1120mA)

PVT 0720

PVT 0722

PVT 0723

USB Camera Power

300mA

PVT 0729

PVT 0731

PVT 0724

PVT 0722

PVT 0801

PVT 0801

Typ: 529mA (397mA~661mA)

30Pin eDP CN

eDP

FAST,UL/CSA

MP 0816

Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

Camera

DVT_05-29

Touch Screen

*WCM2012-90

PVT 0722

NB LVDS enable

AU LCDVCC:
I rush = 2A/0.5ms
IDD = 0.3A

NFC module :
Vender : Samsung SNC-i20
Power consumption : Max. 160mW/48mA
Power Ripple +/- 50mV

NFC

0328 NEO

0328 NEO

DVT 05-31

NFC-ACS(50501-01541-001)

PVT 0721

M/B

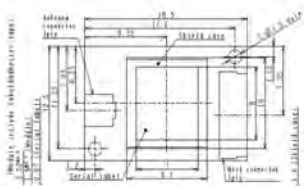
NFC MIDULE

15 GND

1 MOD_VDD

15 GND

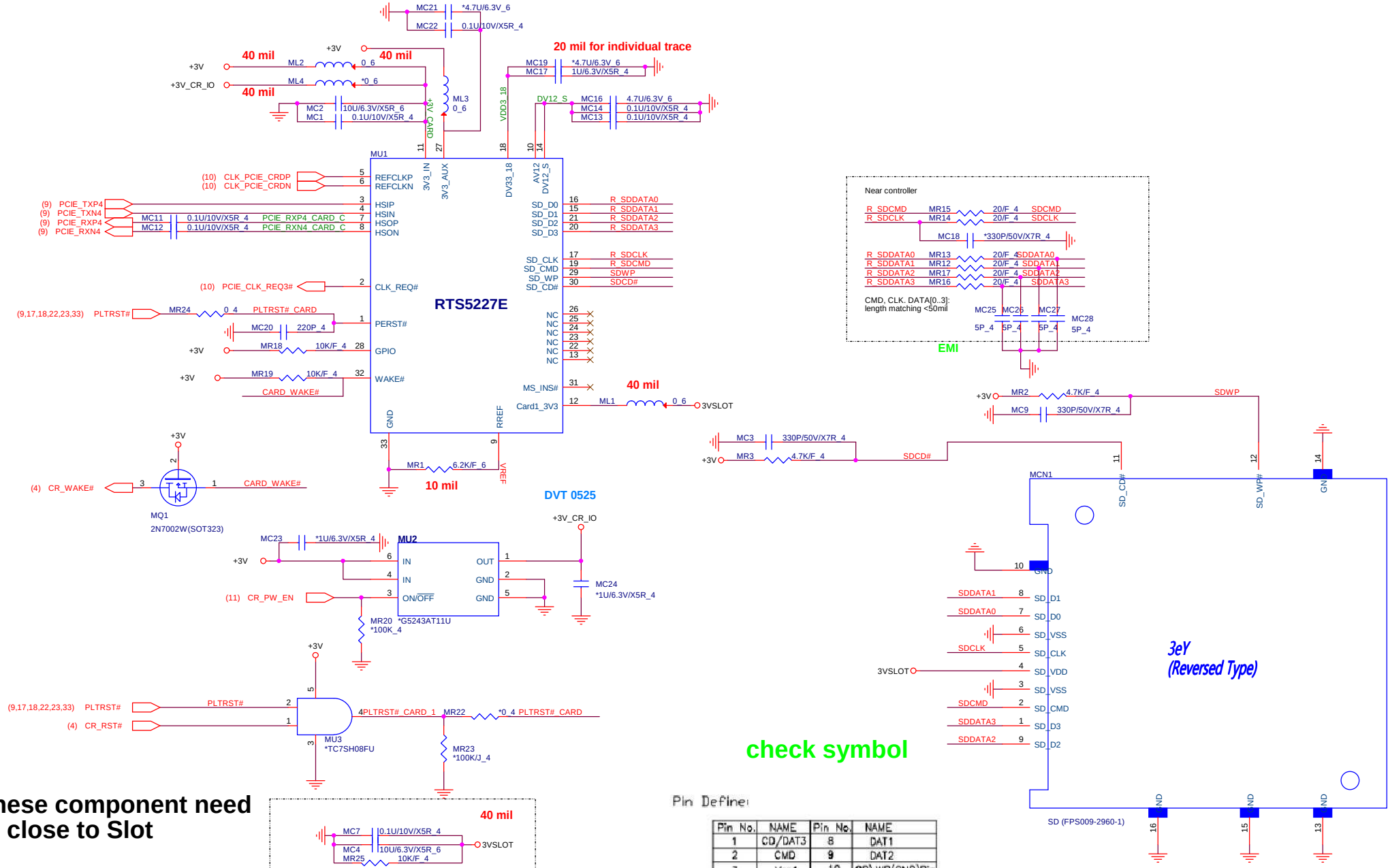
MOD_VDD



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	CRT/LVDS	1A
Date: Tuesday, August 20, 2013	Sheet 17 of 40	



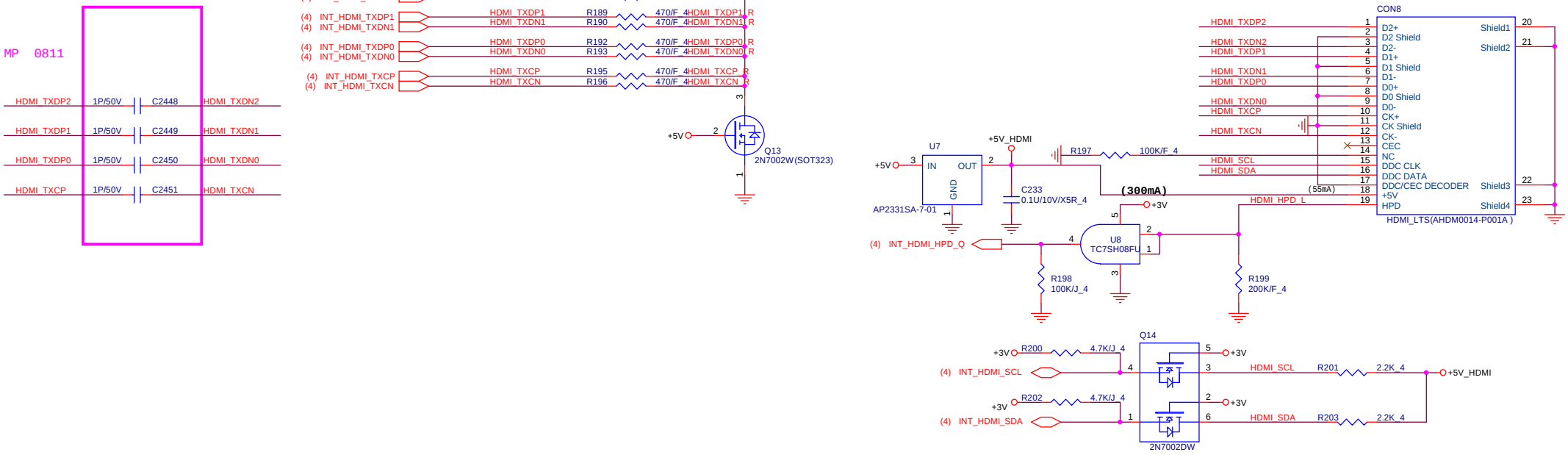
Pin No.	NAME	Pin No.	NAME
1	CD/DAT3	8	DAT1
2	CMD	9	DAT2
3	Vss1	10	CD\WP(GND)Pin
4	VDD	11	CD Pin
5	CLK	12	WP Pin
6	Vss2	13	GND(Shell)
7	DAT0	14	GND(Shell)
		15	GND(Shell)
		16	GND(Shell)

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	CARD	1A

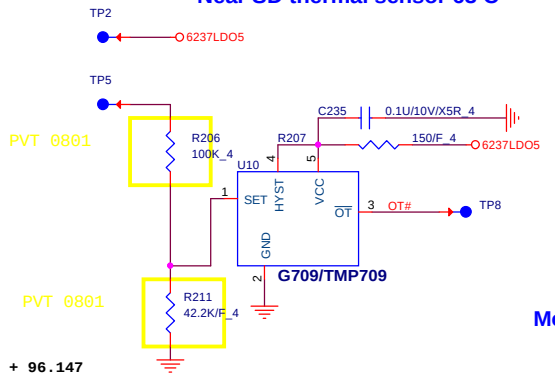
Date: Monday, August 19, 2013 Sheet 18 of 40

HDMI

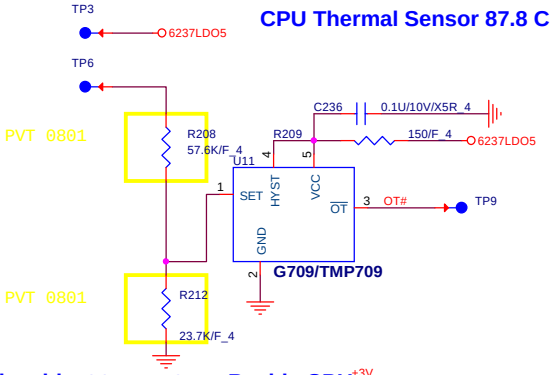


H/W Thermal Protect

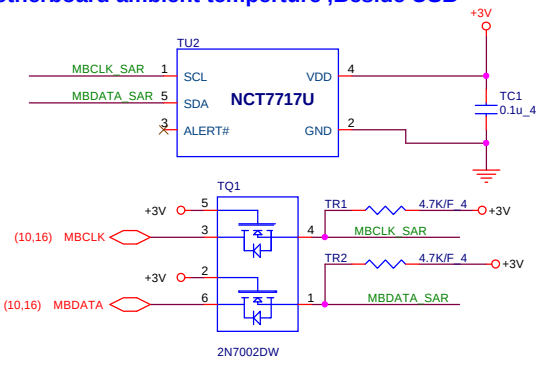
Near SD thermal sensor 63 C



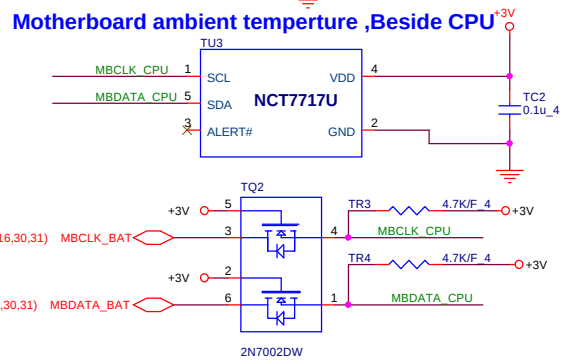
CPU Thermal Sensor 87.8 C

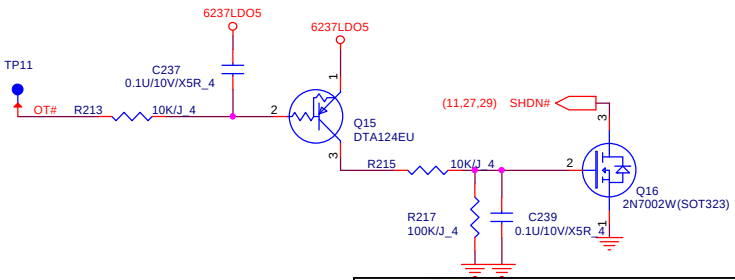


Motherboard ambient temperture ,Beside USB



Motherboard ambient temperture ,Beside CPU





RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

95	18.5K
100	15K
107	10.3K
110	8.2K

DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	70	R208=36.87K	36.5K	71	70
Near GFX sensor temp	65	R146=40.72K	40.2K	66.3	65.1
Near AUDIO sensor temp	60	R345=44.62K	44.2K	61.2	60

UMA SKU

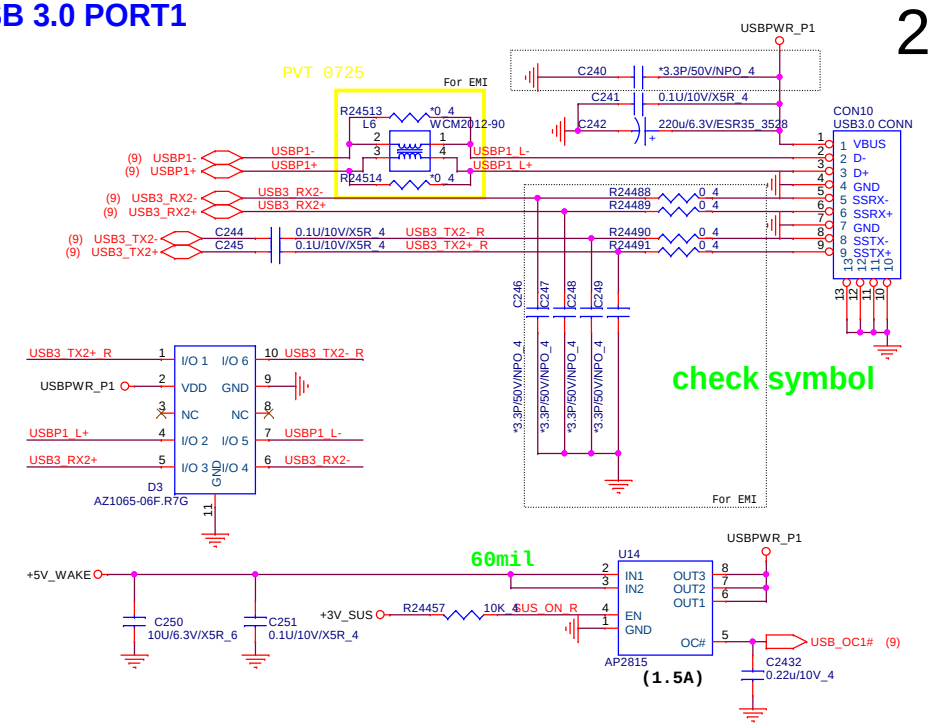
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	81	R208=28.63K	28K	82.3	81.4
Near AUDIO sensor temp	58	R345=46.2K	46.4K	58.4	57.1

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

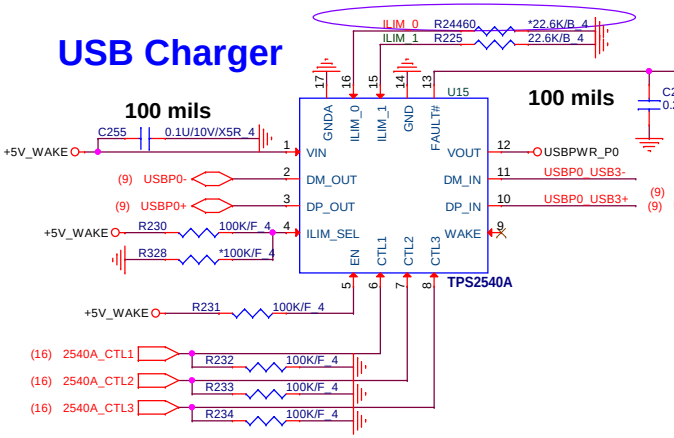
Size	Document Number	Rev
	HDMI/Thermal IC	1A
Date: Monday, August 19, 2013	Sheet 19 of 40	

USB 3.0 PORT1

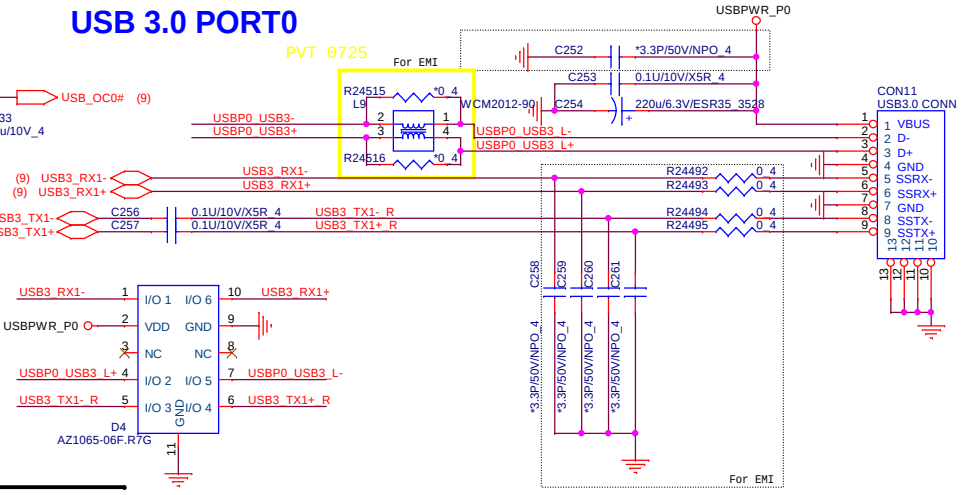


DVT-2013-05-05 : Symbol reserve for TPS2543

USB Charger

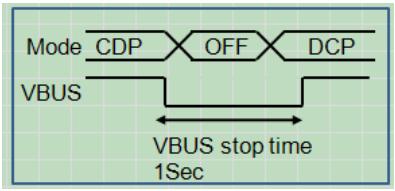


USB 3.0 PORT0



	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

ILIM_SEL	(I LIMIT(A)= 48000/R)	
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

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Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	USB/USB Charger	1A

Date: Monday, August 19, 2013 Sheet 20 of 40

To Rear Camera(8M)

Realtek PC Camera
RTS5825

Check

PVT 0721

CON29

SONY FFC-CN_41pin_HRS

RTS5825 QFN46
(Parallel & MIPI)

Realtek_RTS5825_QFN46

Please Close to IC

Green color(525nm)

EVL_19-21SYGC/S530-E2/TR8(GREEN)
CamLED

Q33
2N7002W(SOT323)

PN 0415

Pull High

PN 0415

SPI Interface

EN25P10-100GIP

Rear Camera LED

USB Rear Camera Power

DVT 05-19

For Rear Camera RTD3

PVT 0722

To Front/Rear Camera(1M/8M)

1.05V LDO for sensor core power

G918T11U(SOT-23-5)

Modify based on LDO part

2.7V LDO for sensor I/O analog power

MP 0809

G916T1UF(ADJ,300MA) (SOT23-5)

Modify based on LDO part

MP 0809

2.8V LDO for sensor ACTVDD

MP 0809

G916T1UF(ADJ,300MA) (SOT23-5)

Modify based on LDO part

3.3V Power Switch:
I limited (min)= 750mA
I limited (Type)= 1000mA
I limited (min)= 1250mA

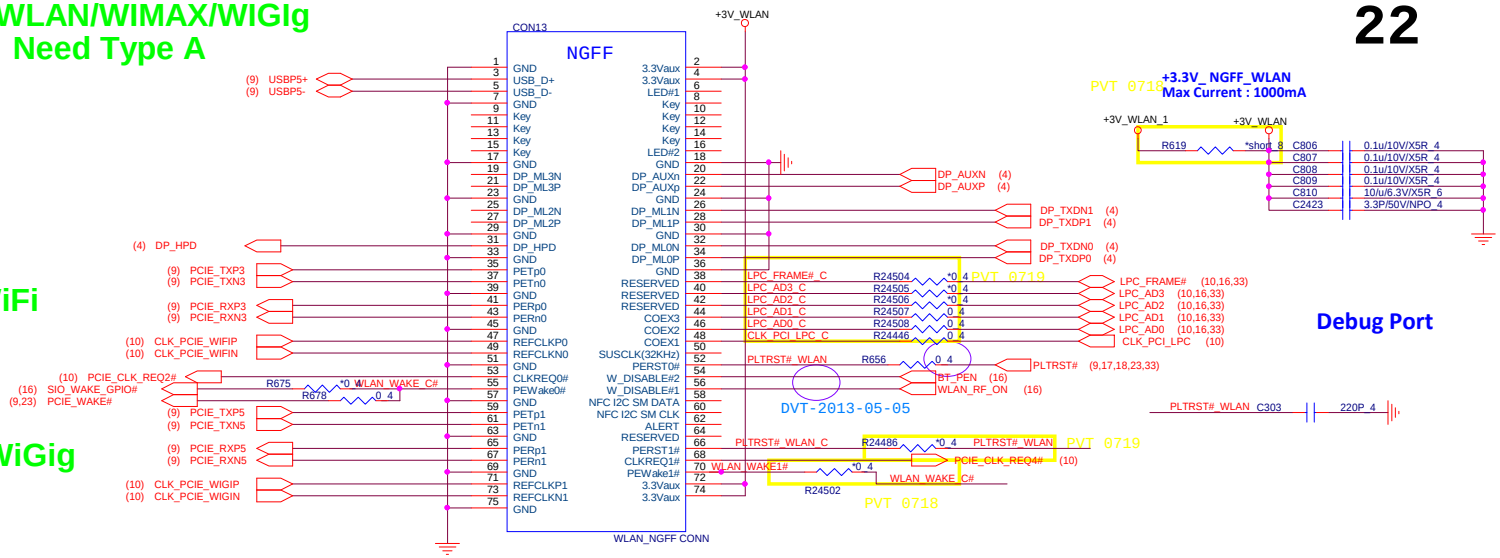
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :FI1

Size	Document Number	Rev
	Camera	1A
Date: Tuesday, August 20, 2013	Sheet 21 of 40	

NGFF Wifi/BT connector

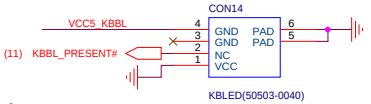
WLAN/WIMAX/WIGIg Need Type A



22

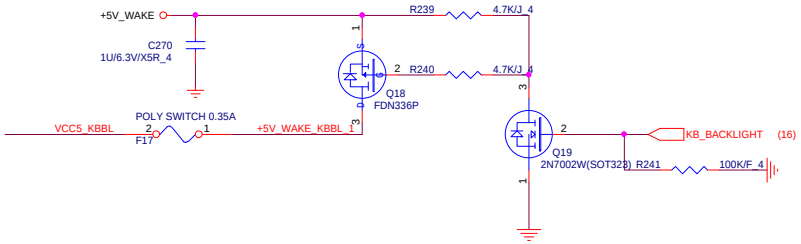
KB BACKLIGHT

Check symbol

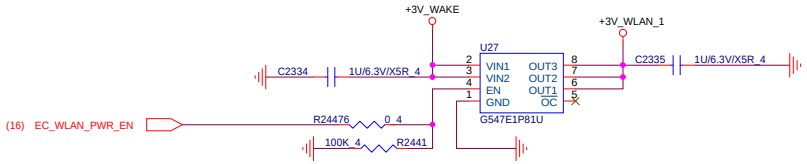


KB Backlight: Max. 360mA

KB Backlight PWM=380Hz



AC Mode : Support Wake on WLAN
DC Mode : Don't support wake on WLAN



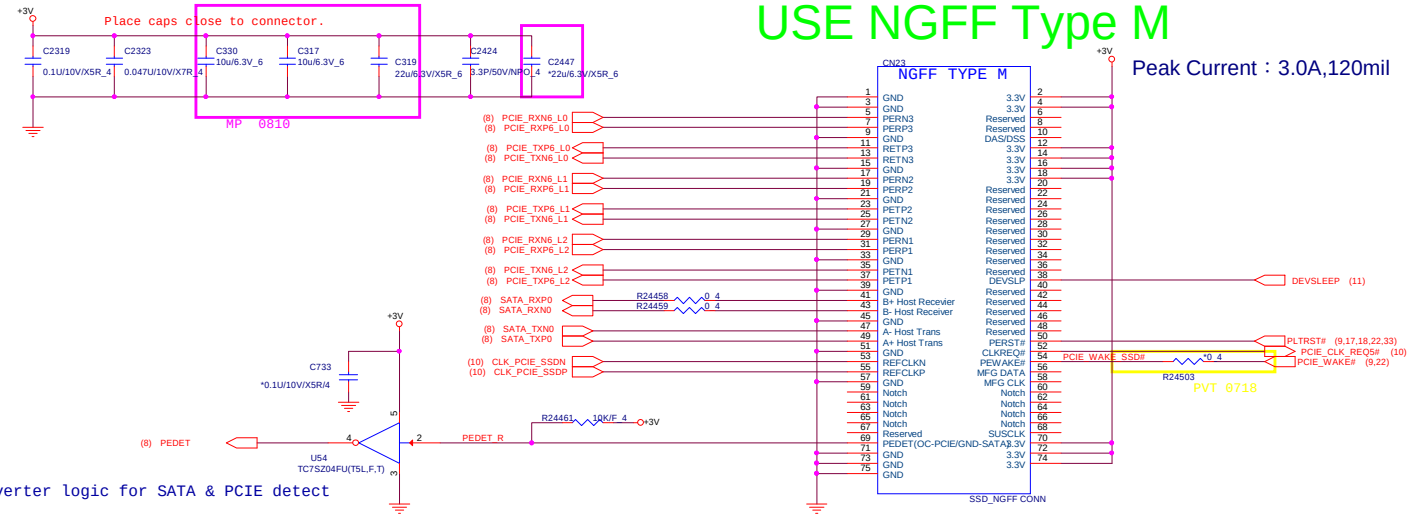
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

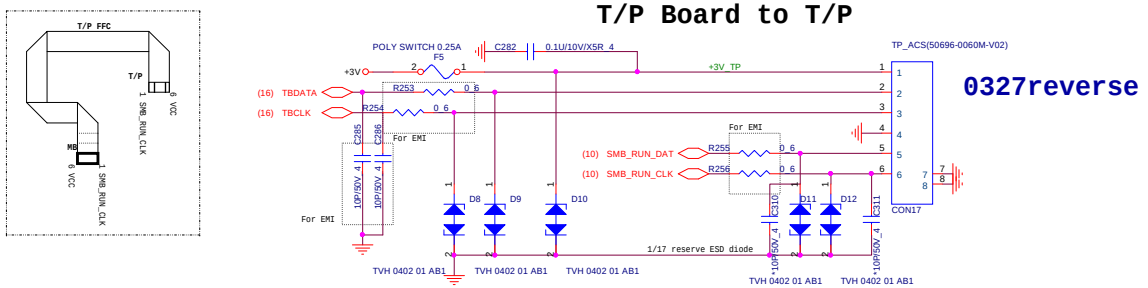
Size	Document Number	Rev
	WLAN/KB BL	1A
Date: Monday, August 19, 2013	Sheet 22 of 40	

USE NGFF Type M

Peak Current：3.0A,120mil

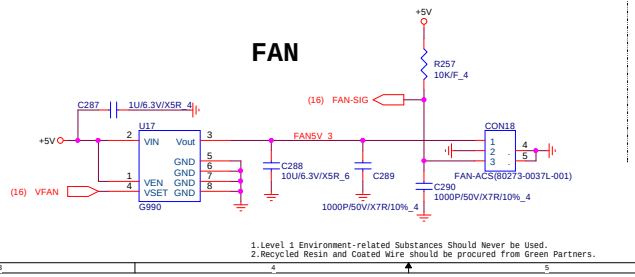


T/P Board to T/P



0327reverse

FAN

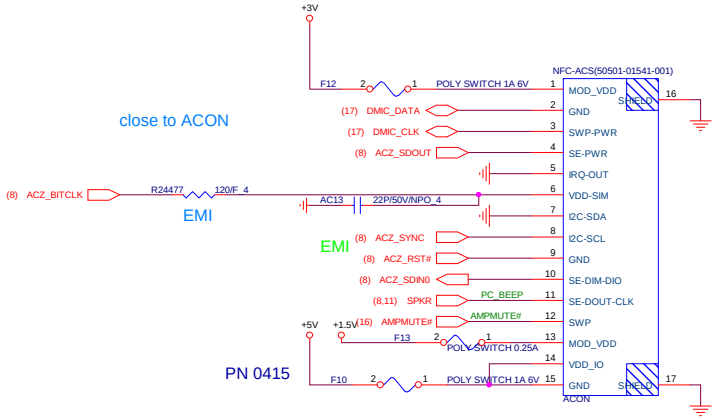


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	HDD/ODD/TP/FAN	1A

Date: Monday, August 19, 2013 Sheet 23 of 40

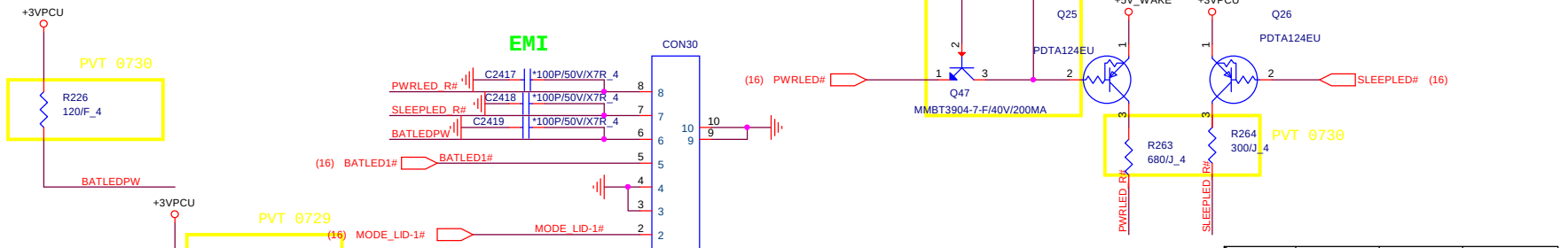


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	Audio Codec ALC233-CG	1A
Date: Monday, August 19, 2013	Sheet 24 of 40	

To Power/Sleep LED & BATTERY LED



	VF MIN	VF MAX	A
Umber LED	1.75V	2.35V	7.27mA / 4.09 mA

(3.3 - 1.75)V /120 Ω = 12.9 mA
(3.3 - 2.35)V / 120Ω =7.92 mA

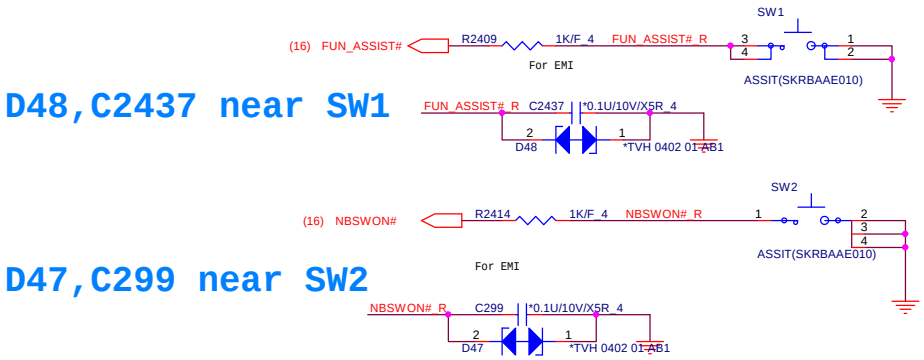
	VF MIN	VF MAX	A
Pure green LED	2.7V	3.7V	4.89mA / 2.76 mA

(5- 2.7)V / 680 Ω =3.38 mA
(5 - 3.7)V / 680Ω = 1.91 mA

	VF MIN	VF MAX	A
Umber LED	1.7V	2.4V	7.27mA / 4.09 mA

(3.3 - 1.7)V /300 Ω = 5.3 mA
(3.3 - 2.4)V / 300Ω =3mA

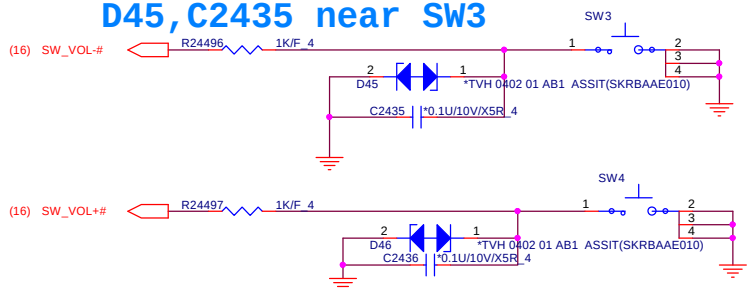
Power & Assist SW Follow FI3



D48,C2437 near SW1

D47,C299 near SW2

D45,C2435 near SW3

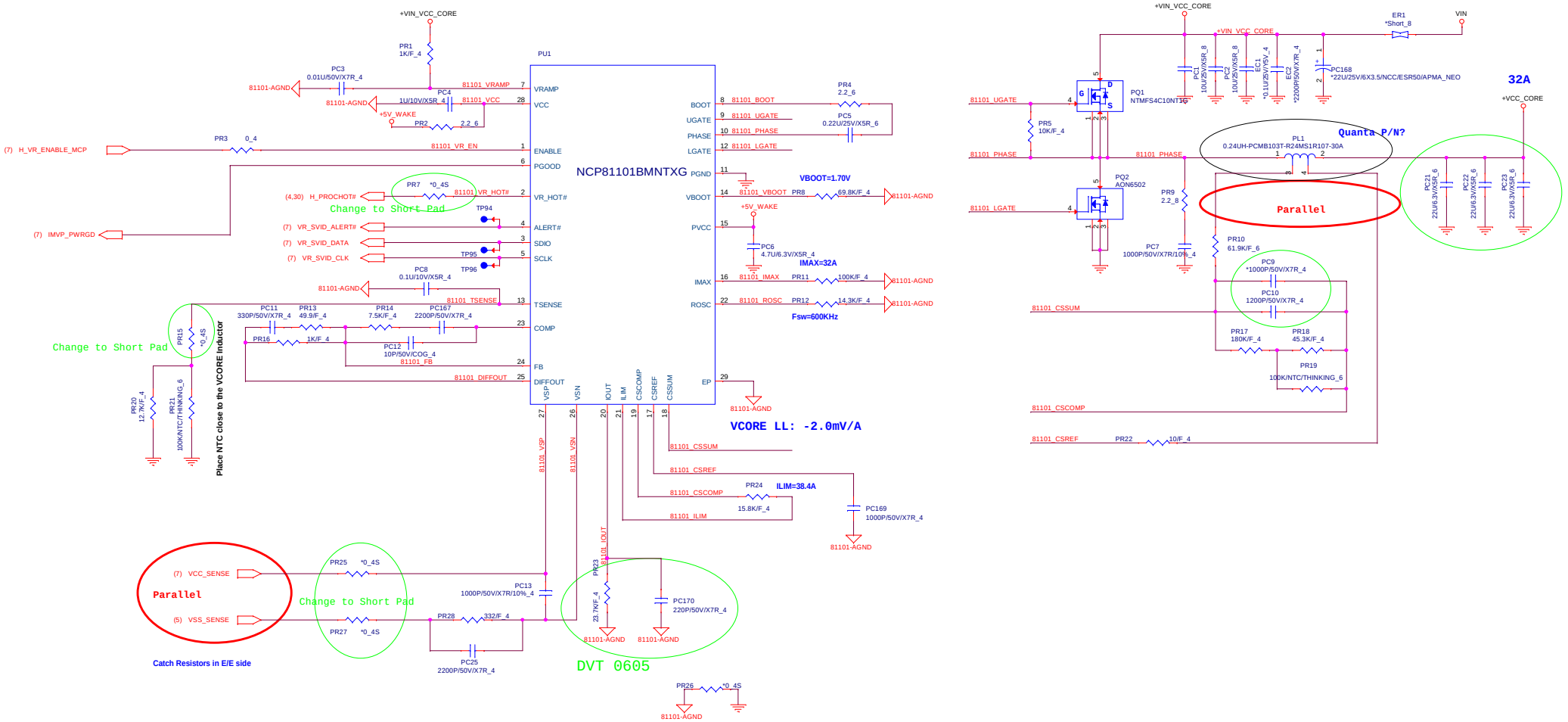


D46,C2436 near SW4

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	LED/RF/KB/PS	1A
Date: Monday, August 19, 2013	Sheet 25 of 40	



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FI1		
Size	Document Number: +VCC_CORE (NCP81101)	Rev: PVT
Date: Tuesday, August 20, 2013	Sheet 26 of 40	

3.3V & 5V

FREQ: 400KHZ

FREQ: 500KHZ

PVT 0715

PVT 0719

Change to Short Pad

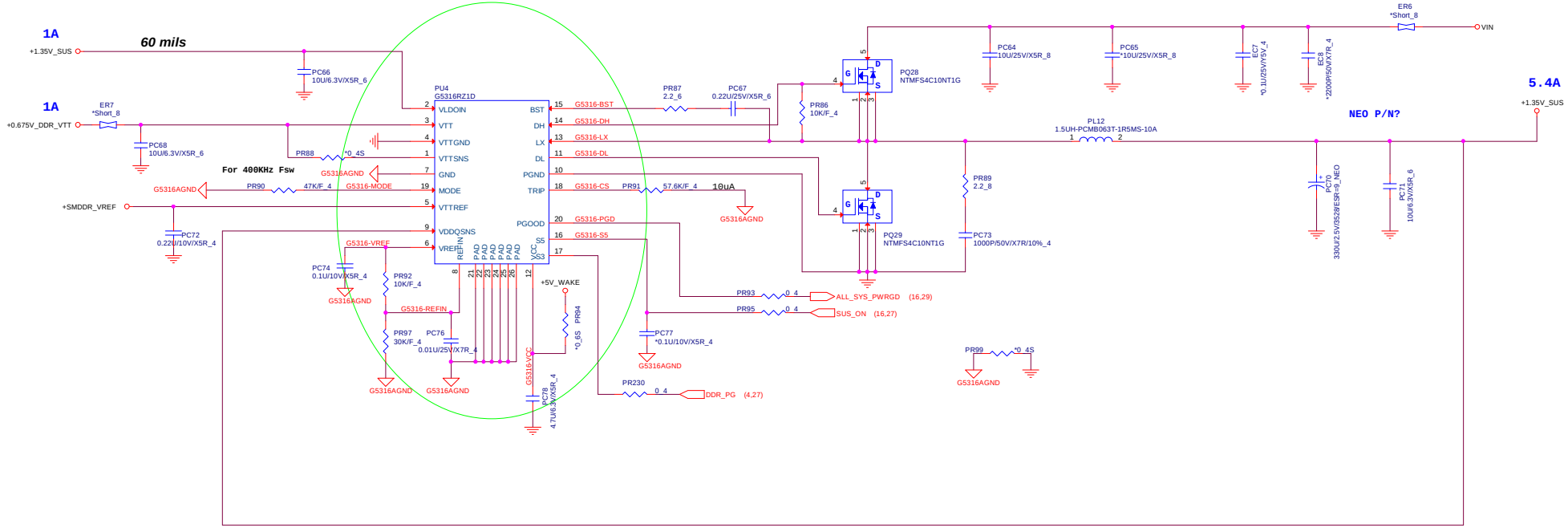
+3V_SUS for DS3

For EuP Lot 6 (2nd stage)

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

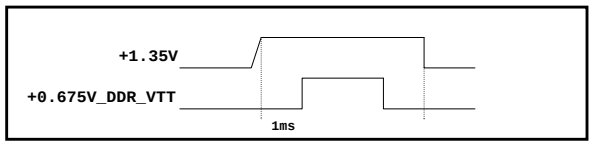
Quanta Computer Inc.
PROJECT : FI1
Size | Document Number: 3VPCU&5VPCU(TPS51427A) | Rev: PVT
Date: Monday, August 19, 2013 | Sheet 27 of 40

1.35VSUS & VTT_MEM



MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	**Non-tracking discharge**
0	**47Kohm**	**400KHz**	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off



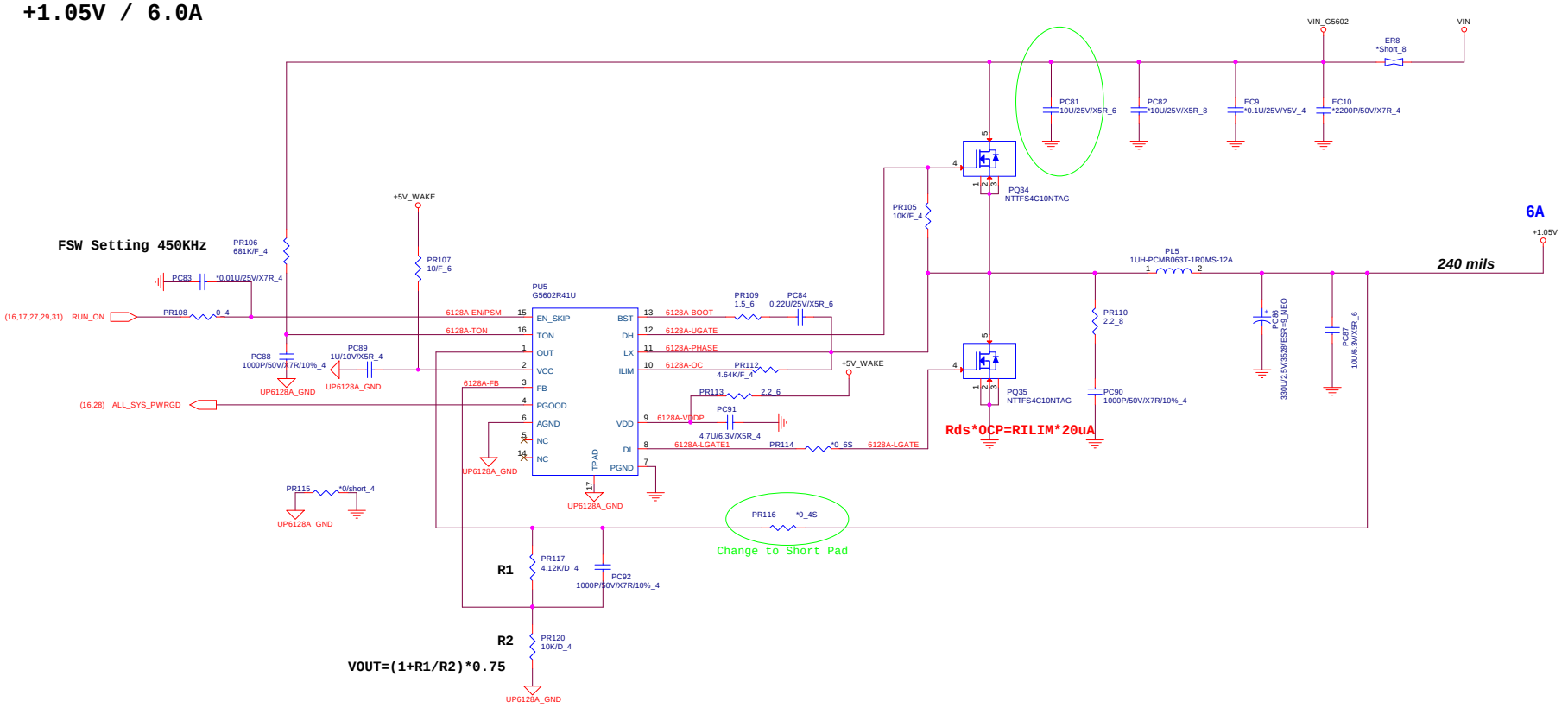
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

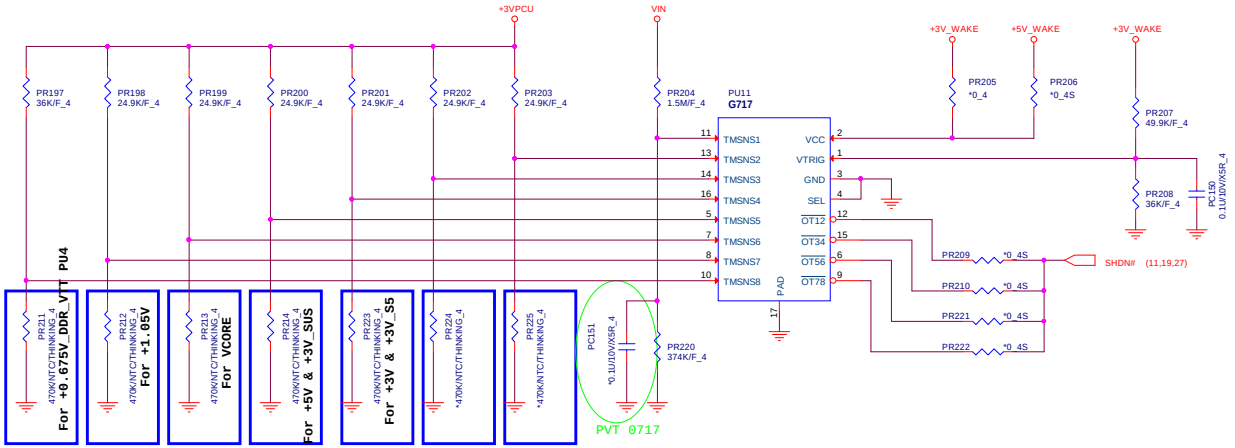
Size	Document Number	Rev
	1.5VSUS/VTT_MEM	PVT

Date: Monday, August 19, 2013 Sheet 28 of 40

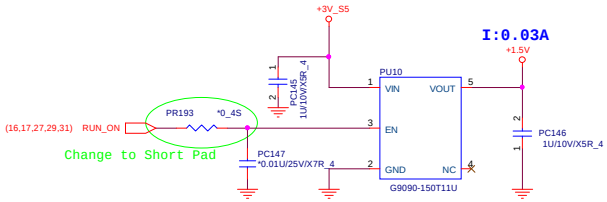
+1.05V / 6.0A



Thermal Protection and Battery UVP for VEDS



VCC1.5

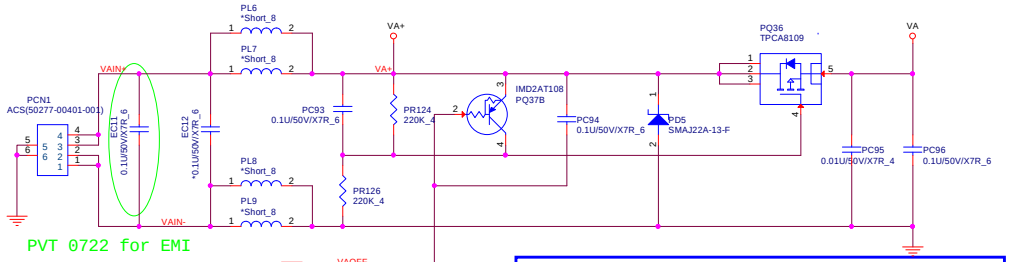


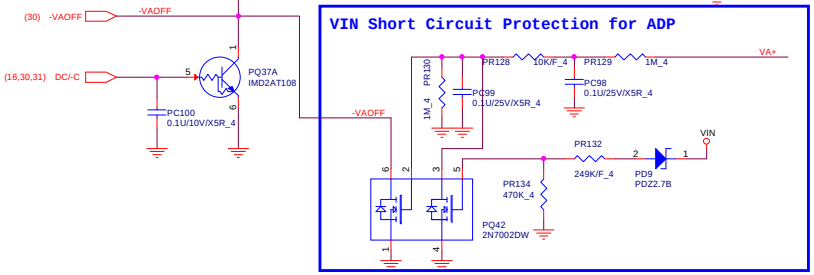
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1

Size	Document Number	Rev
	+1.05V (UP1522RQDD)-6A	PVT

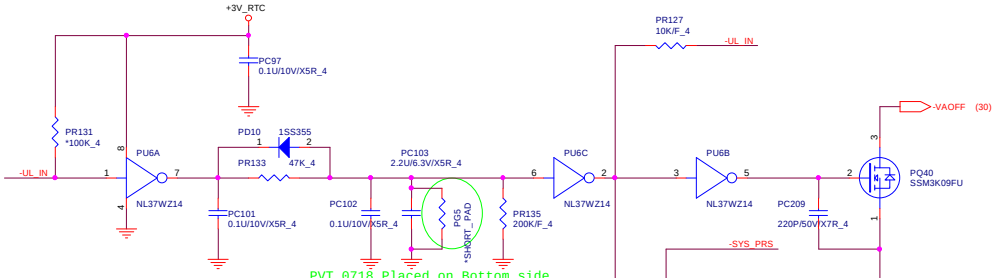
Date: Monday, August 19, 2013 Sheet 29 of 40





VIN Short Circuit Protection for ADP

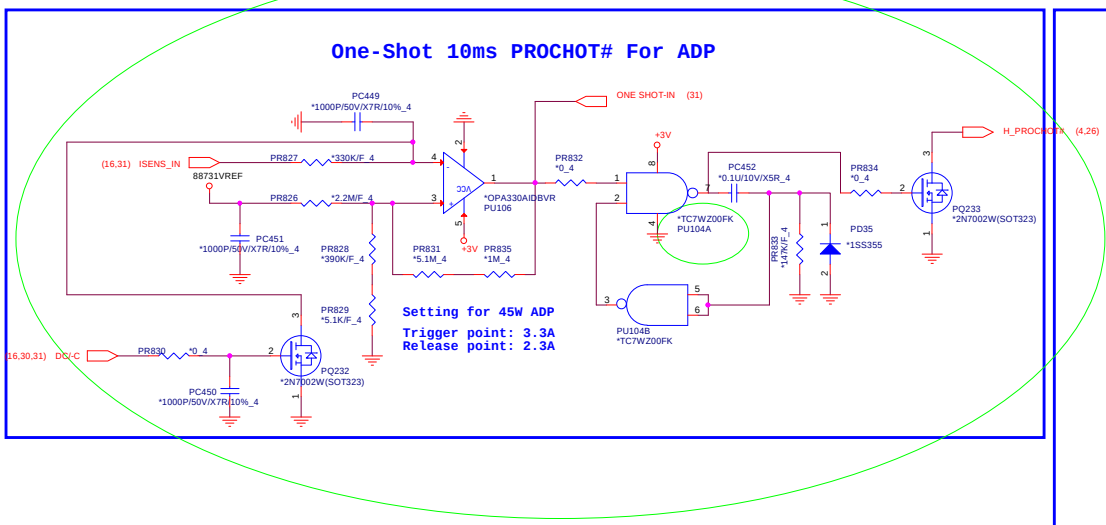
UL Latch Circuit



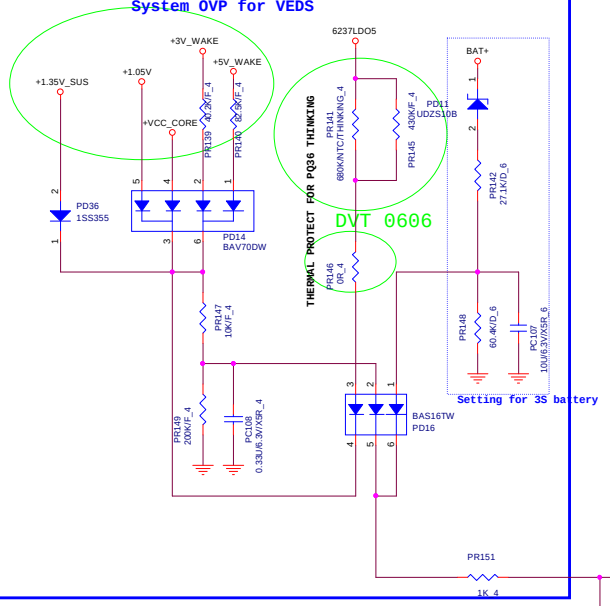
PVT 0718 Placed on Bottom side

Jumper location should be accessable for reset

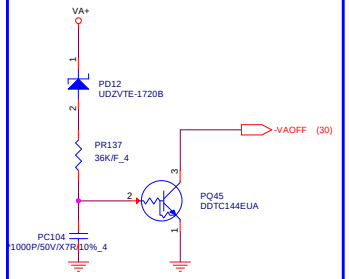
One-Shot 10ms PROCHOT# For ADP

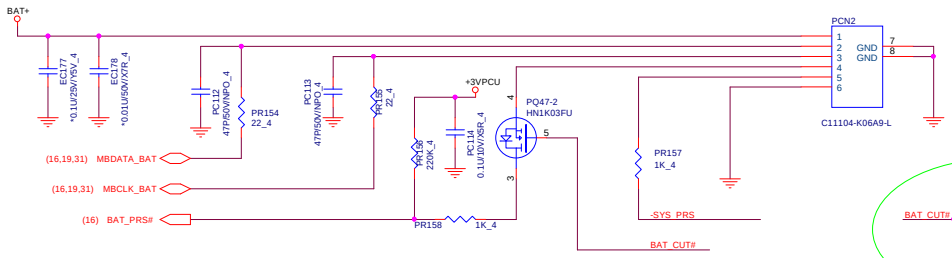


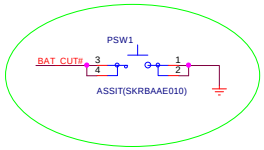
System OVP for VEDS

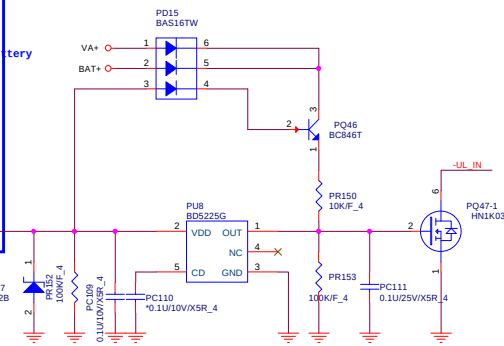


Adapter OVP









1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FI1
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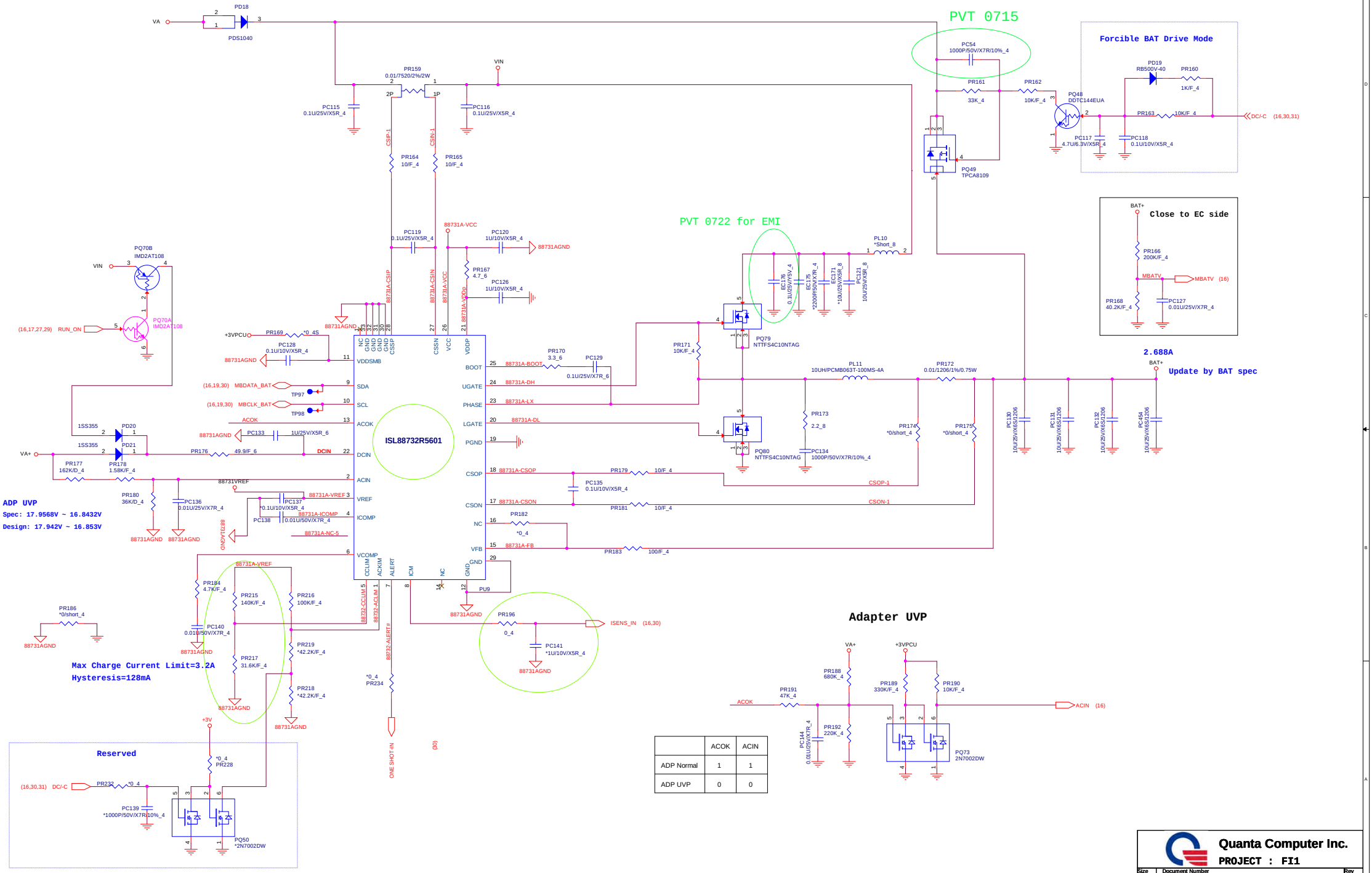

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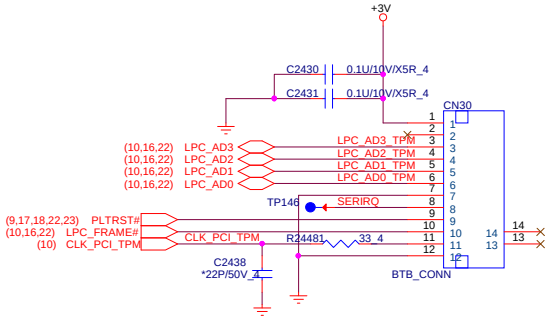
Size	Document Number	Rev
	Debug con	1A
Date: Monday, August 19, 2013	Sheet 32 of 40	



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Size	Document Number	Rev
	Nvidia 2/4	1A

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1.Level 1 Environment-related Substances Should Never be Used.
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Size	Document Number	Rev
	VRAM 3/4	1A
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1.Level 1 Environment-related Substances Should Never be Used.
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Size	Document Number	Rev
	VRAM 4/4	1A
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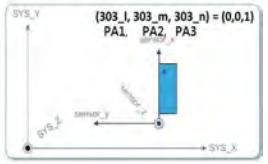
Sensor HUB

LSM303DLHC Orientation Setting (Top)



PVT 0730

PVT 0721

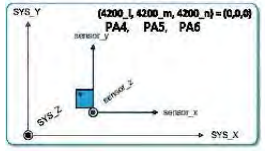
PN 0415

DVT 05-28

DVT 05-14

PN 0415

L3GD20TR Orientation Setting (Top)



Current limit
Typ:1A(880mA~1120mA)

ALS Remove to camera module

DVT 05-14

G-sensor/E-compass/Magnetometer

LSM303DLHC

WR Address : 0x3C
RD Address : 0x3D

all layer delete

Gyroscope

L3GD20TR

WR Address : 0xD2
RD Address : 0xD3

Only surface layer delete

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PROJECT : FI1

Size	Document Number	Rev
	Sensors Hub & Sensors	1A
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1.Level 1 Environment-related Substances Should Never be Used.
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PROJECT : FI1

Size	Document Number	Rev
	Blank	1A

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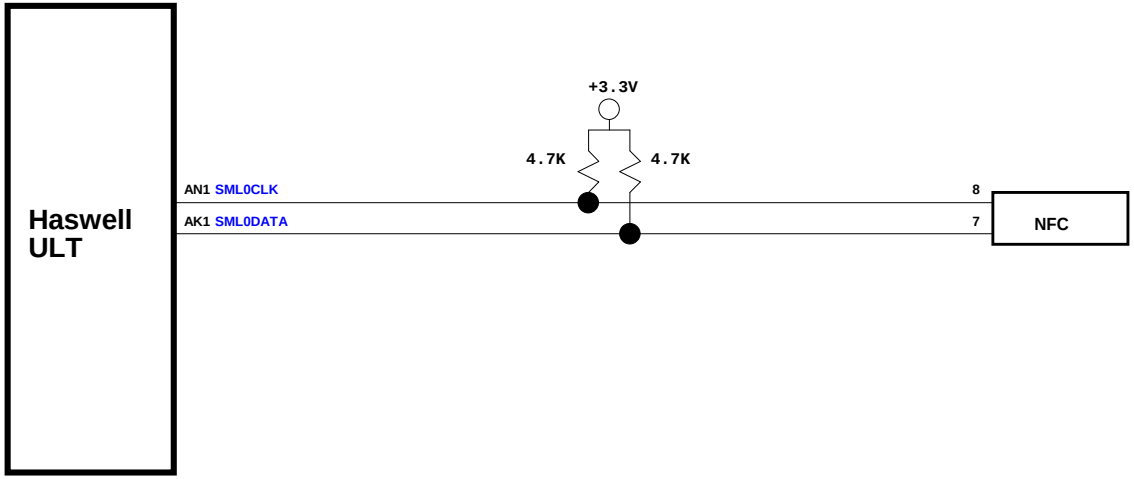
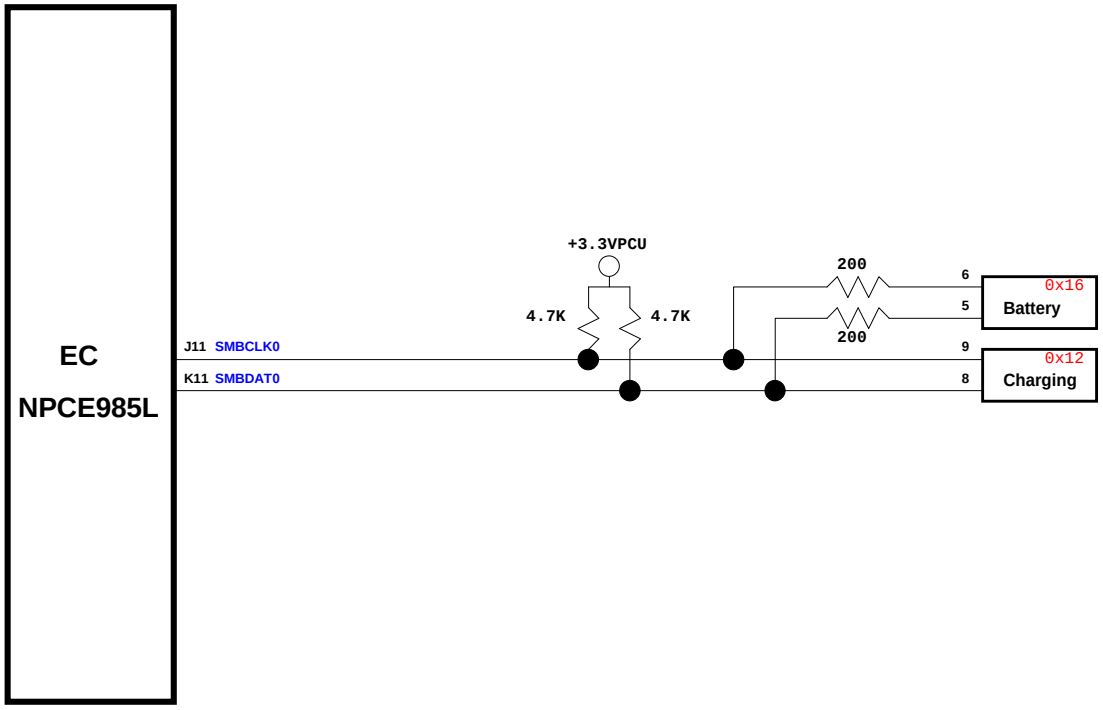


Function	IC	SMBus Address
Charge IC	ISL88731CHRTZ	0X12
Battery	Battery	0X16
NFC		



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Size	Document Number	Rev
	Camera	1A

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Power	Voltage	S0	S3	DS3	S4 (/W RTC Wake up)	S4 (/WO RTC Wake up)	S4 (/WO CHANGE)	S4 (/W CHANGE)	S5 (/WO CHANGE)	S5 (/W CHANGE)	Ctl Signal
+3VPCU	3.3V	V	V	V	V	V	V	V	V	V	Adapter/BAT in
+3.3V_DSW	3.3V	V	V	V	V	V	V	V	V	V	DEEP_EC_EN
+3V_WAKE	3.3V	V	V	V	V			V		V	**EC_WAKE_ON**
+5V_WAKE	5V	V	V	V	V			V		V	**EC_WAKE_ON**
+5V_S5	5V	V	V		V						**S5_ON**
+3V_S5	3.3V	V	V		V						**S5_ON**
+1.35V_SUS	1.35V	V	V	V							**SUS_ON**
+3V	3.3V	V									**RUN_ON**
+5V	5V	V									**RUN_ON**
+0.675V_DDR_VTT	0.675V	V									**RUN_ON**
+1.05V	**1.05V**	V									**RUN_ON**
+1.5V	**1.5V**	V									**RUN_ON**
+VCC_CORE	**By VID**	V									**RUN_ON**

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Size	Document Number	Rev
	Power Table	1A

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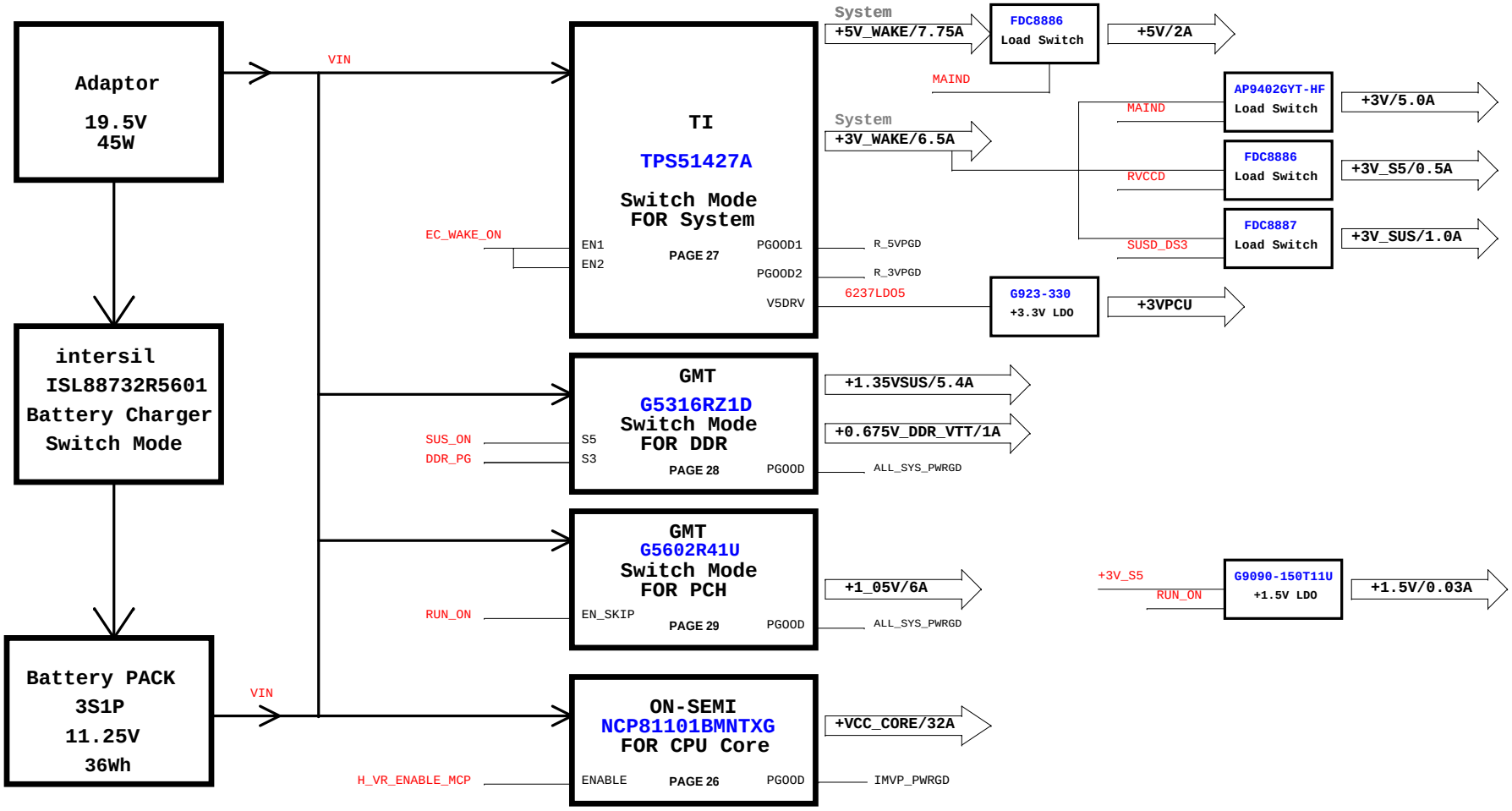

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PROJECT : FI1

Size	Document Number	Rev
	Power TREE	1A

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