

Model : P75/55IMx

Intel Merom CPU + PM965 + ICH8-M Chipset
Santa Rosa plantfrom (No supported AMT)

Revision History		
	08/2006	Initial Rev.RA
	09/2006	Rev.A1
	11/2006	Rev.A2
	01/2007	Rev.B
	03/2007	Rev.C

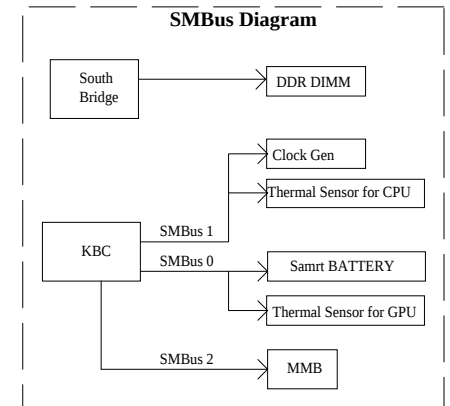
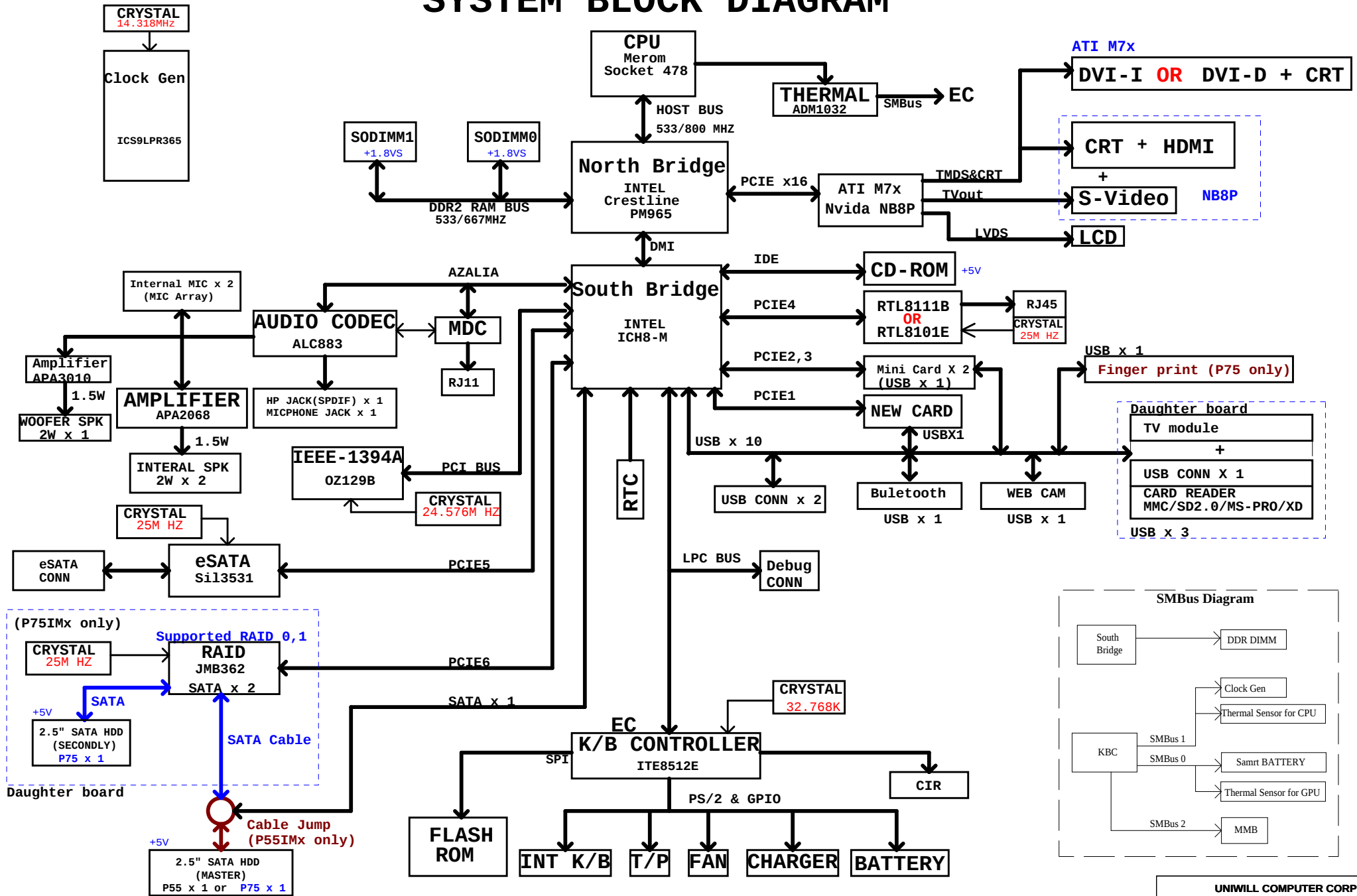
PCB P/N: 37GP55000-C0
PCBA P/N: 82GP55000-C0

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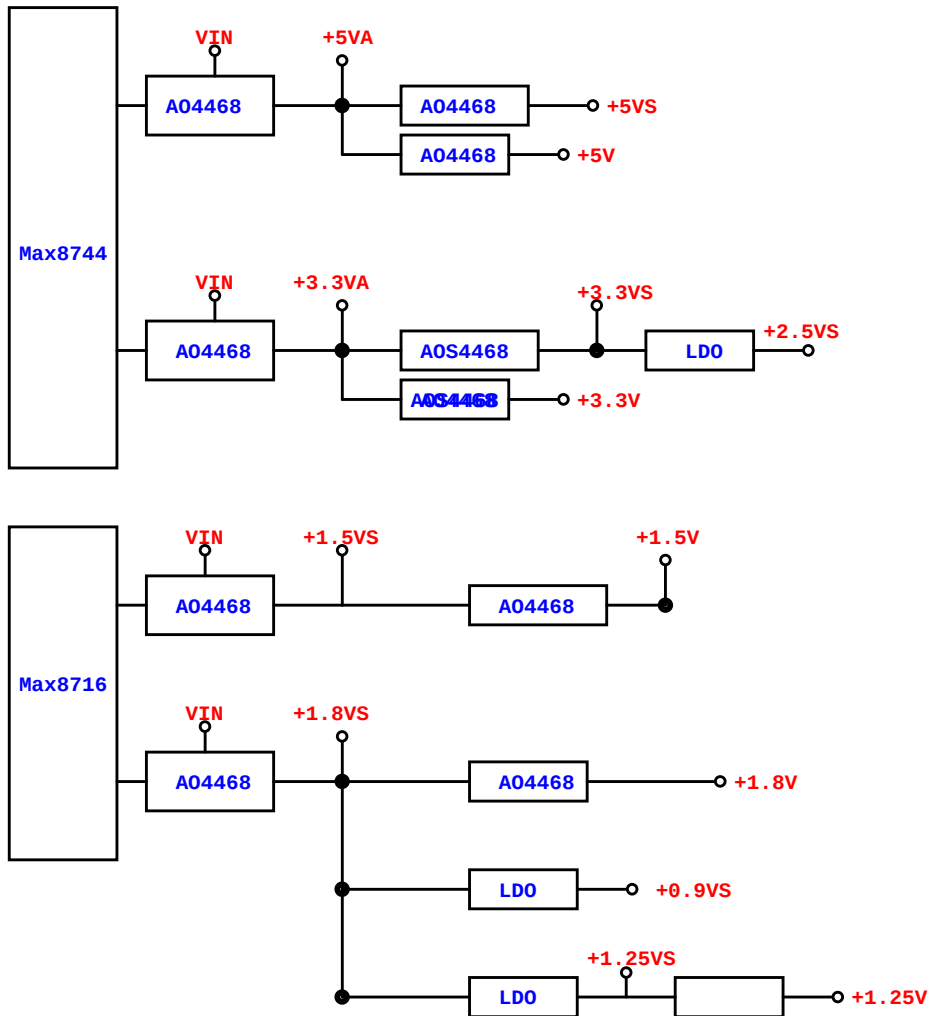
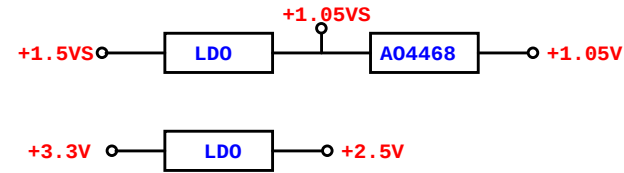
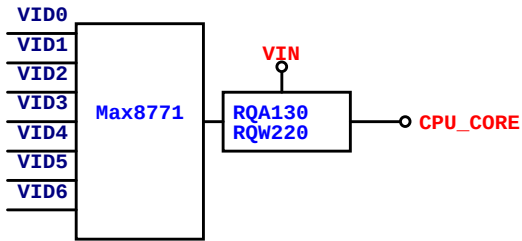
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P75/55IMx SYSTEM BLOCK DIAGRAM

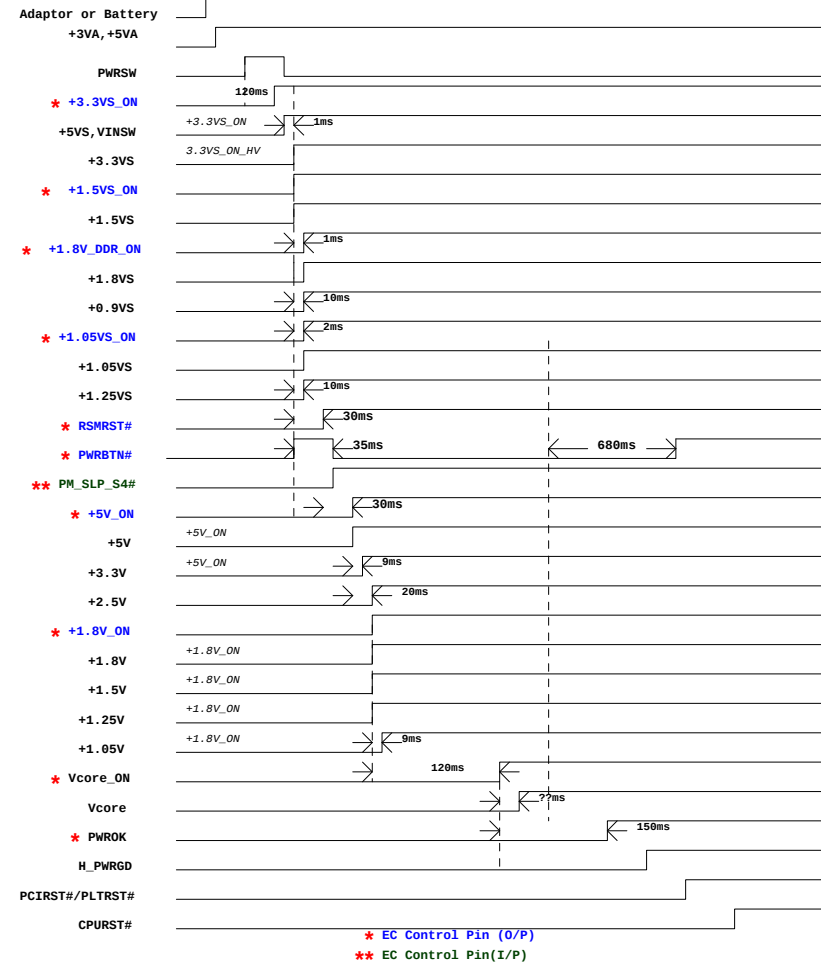


POWER BLOCK DIAGRAM



Poewr On Sequence

EC debouns 100ms



ICH8-M GPIO	
GPI00	PM_BM_BUSY#
GPI01	EC_EXTSMI#
GPI02	INT_PIRQE#
GPI03	INT_PIRQF#
GPI04	INT_PIRQG#
GPI05	INT_PIRQH#
GPI06	BIOS_REC
GPI07	N.C (TACH3)
GPI08	N.C
GPI09	N.C (WOL_EN)
GPI010	N.C (ALERT#)
GPI011	SMB_ALERT#
GPI012	LAN_PHYPC
GPI013	N.C (GLAN_DOCK#)
GPI014	N.C (NETDETECT)
GPI015	PM_STPPCI#
GPI017	N.C (TACH0)
GPI018	N.C
GPI019	SATA1GP
GPI021	SATA0GP
GPI022	N.C (SCLOCK)
GPI023	LDRQ1#
GPI024	CRB_SV_DET
GPI025	PM_STPCPU#
GPI026	PM_SLP_S4_STATE#
GPI027	QRT_STATE0
GPI028	QRT_STATE1
GPI029	USB_OC#5
GPI030	USB_OC#6
GPI031	USB_OC#7
GPI032	PM_CLKRUN#
GPI033	HDA_DOCK_EN
GPI034	N.C (HDA_DOCK_RST)
GPI035	CLK_SATA_OE#
GPI036	SATA2GP
GPI037	SATA3GP
GPI038	ODD_DET
GPI039	ICH_GPIO39
GPI040	USB_OC#1
GPI041	USB_OC#2
GPI042	USB_OC#3
GPI043	USB_OC#4
GPI048	MFG_MODE
GPI049	H_PWRGD
GPI050	PCI_REQ#1
GPI051	PCI_GNT#1
GPI052	PCI_REQ#2
GPI053	PCI_GNT#2
GPI054	PCI_REQ#3
GPI055	PCI_GNT#3

ITE8512E GPIO	
GPA0	PM_RSMRST#
GPA1	SUSPEND_LED
GPA2	SILENT_LED
GPA3	RF_LED
GPA4	CAPS_LED
GPA5	NUM_LED
GPA6	SCROLL/3G_LED
GPA7	EXTTS#0
GPB0	PM_SLP_S4#
GPB1	PM_SLP_S3#
GPB2	CMI_TX
GPB3	SMB_CLK0
GPB4	SMB_DAT0
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	QRT_STATE
GPC0	CMI_RX
GPC1	SMB_CLK1
GPC2	SMB_DAT1
GPC3	KEY_OUT16
GPC4	RF_SW#
GPC5	KEY_OUT17
GPC6	BTL_BEEP
GPC7	SILENT#
GPD0	EC_PREST#
GPD1	PWRBTN#
GPD2	MUTE
GPD3	EC_EXTSMI#
GPD4	N.C
GPD5	SMP1_EN#
GPD6	CHG_ON
GPD7	LCDSW
GPE0	PWRSW
GPE1	SET_V
GPE2	PWROK
GPE3	BT_ON
GPE4	LID#
GPE5	CPPE#
GPE6	FAN_SPD#
GPE7	PCI_RST#
GPF0	EC_CPU_200MHZ
GPF1	N.C
GPF2	CHG_G_LED
GPF3	CHG_R_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	N.C
GPF7	N.C
GPG0	SB_RTCRST
GPG1	EC_WDOG_OK
GPG2	FLFRAME#
GPG6	MPWORK
GPH0	+1.8V_ON
GPH1	+1.8V_DDR_ON
GPH2	VCORE_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	+1.05VS_ON
GPH6	+1.5VS_ON

ITE8512E GPIO	
GPI0	BATT_TEMP
GPI1	ADAPTOR_I
GPI2	ADAP_IN
GPI3	BAT_CHG_I
GPI4	BAT_I
GPI5	CPU_PWR
GPI6	DDR2_TEMP
GPI7	VGA_TEMP
GPJ0	EC_BRGHT
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	BROWSER#
GPJ4	MAIL#
GPJ5	PM_THROTTLING#

Merom CPU				
	CPU CORE (V)	ICC (A)	W	TEMP (°C)
IMVP-6+	1.25	44.0	46.2	

Crestline			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	320	1.056	105
+1.8VS	2860	5.148	
+1.5V	76	0.114	
+1.25V	1100	1.375	
+1.05	4140	4.347	

ICH8-M			
VCC	ICC (mA)	mW	TEMP (°C)
+5V	2	10	70
+5VS	1	5	
+3.3V	556	1834.8	
+3.3VS	159	524.7	
+1.5V	2400	3600	
+1.25V	50	62.5	
+1.05V	1131	1187.55	

ITE8512E			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	270	891	70

AD1986A			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V(DVDD)	52	171.6	70
+5V(AVDD)	73	365	

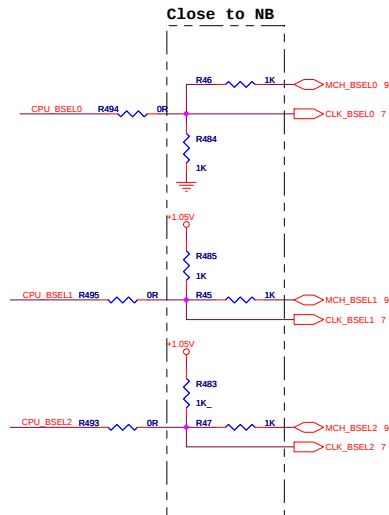
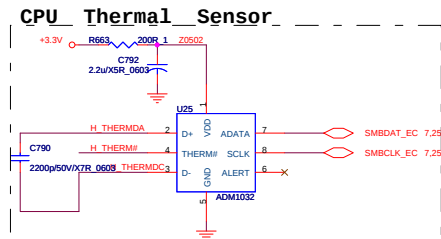
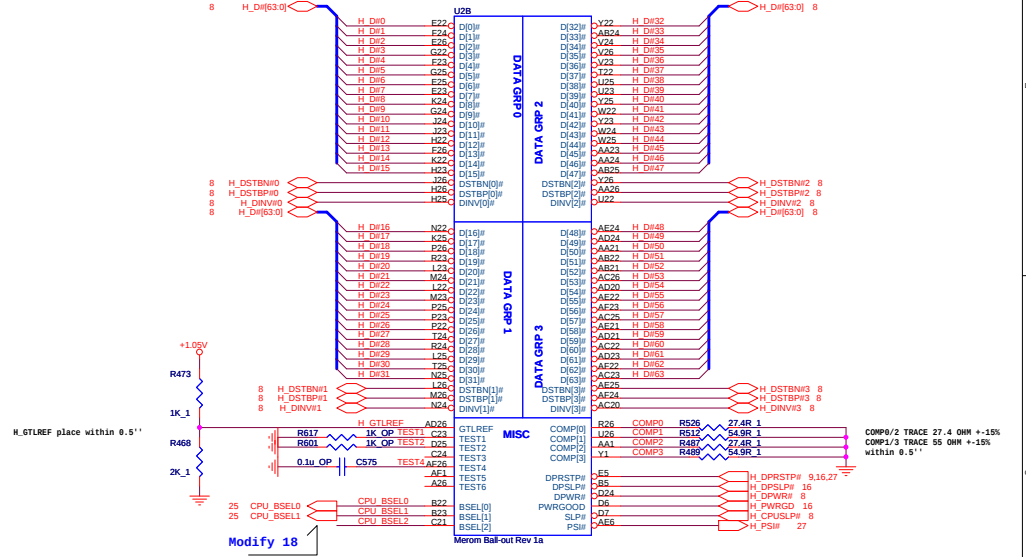
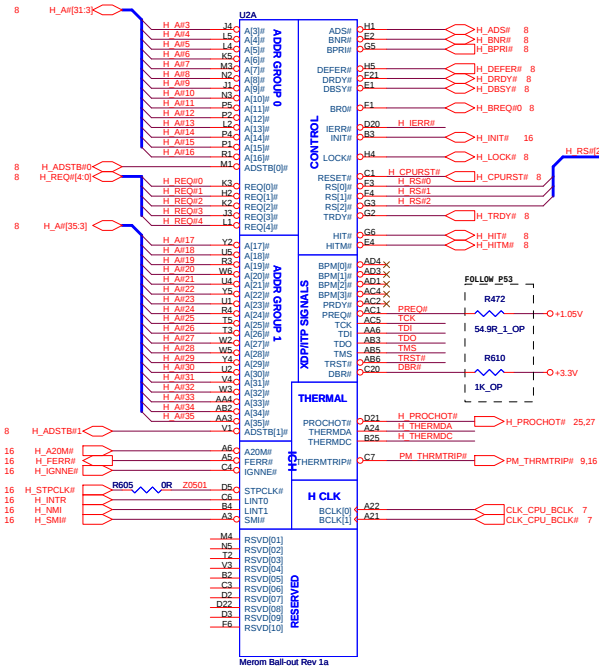
APA2068			
VCC	ICC (mA)	mW	TEMP (°C)
+5V	20	100	85

ADM1032			
VCC	ICC	mW	TEMP (°C)
+3.3V	170uA	0.56	150

OZ129B			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	50	165	70
+1.8V	50	90	

RTL8111B			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3VS	103	339.9	70
+1.8VS	198	356.4	
+1.5VS	367	550.5	

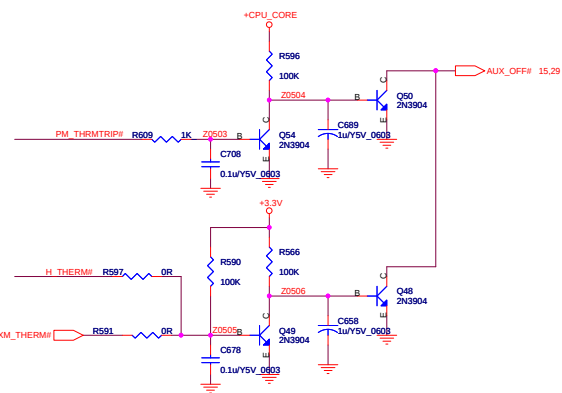
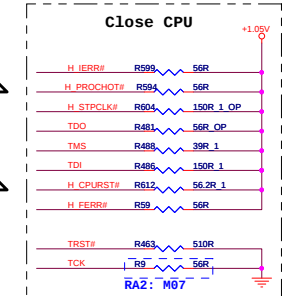
Sil3531			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	TBD		70
+1.8V	TBD		

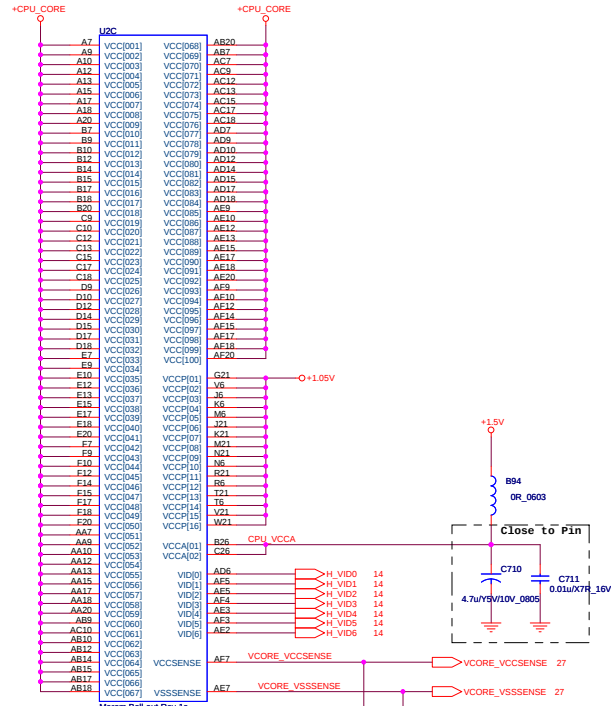


	BSEL2	BSEL1	BSEL0	MHZ
FSB800	0	1	0	200
FSB667	0	1	1	166
FSB533	0	0	1	133

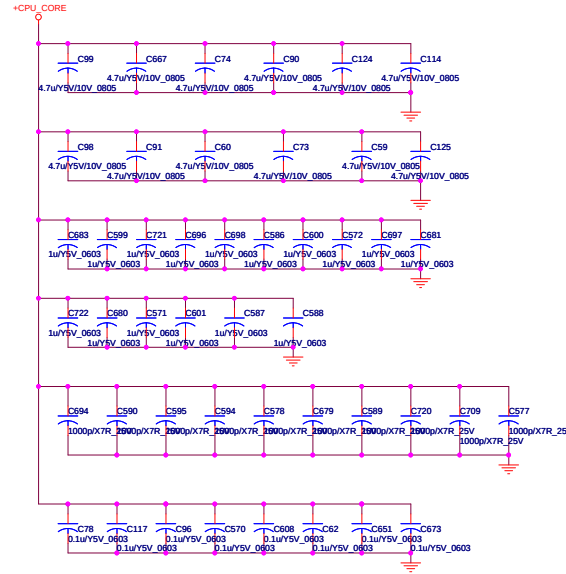
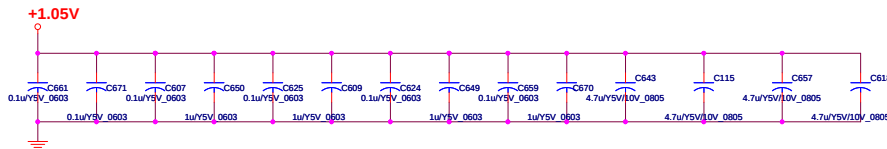
If used, pull-up change from 56R to 68R (Intel recommend)

Intel recommend 51R 1%





QT1608GRL600 = 200mA
 QT1608RL120 = 200mA
 QT1608RL600 = 200 mA
 QT1608RL030 = 500mA
 QT1608RL060 = 500mA

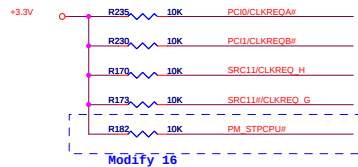


U20			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A27	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T26
B8	VSS[010]	VSS[091]	T24
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U8
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C22	VSS[023]	VSS[104]	W26
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
E5	VSS[043]	VSS[124]	AB22
E8	VSS[044]	VSS[125]	AB25
F11	VSS[045]	VSS[126]	AC6
F13	VSS[046]	VSS[127]	AC8
F16	VSS[047]	VSS[128]	AC11
F19	VSS[048]	VSS[129]	AC14
F2	VSS[049]	VSS[130]	AC16
F22	VSS[050]	VSS[131]	AC19
F25	VSS[051]	VSS[132]	AC21
G4	VSS[052]	VSS[133]	AC24
G11	VSS[053]	VSS[134]	AD2
G13	VSS[054]	VSS[135]	AD5
G16	VSS[055]	VSS[136]	AD8
G19	VSS[056]	VSS[137]	AD11
H4	VSS[057]	VSS[138]	AD13
H6	VSS[058]	VSS[139]	AD16
H21	VSS[059]	VSS[140]	AD19
H24	VSS[060]	VSS[141]	AD22
J2	VSS[061]	VSS[142]	AD25
J5	VSS[062]	VSS[143]	AE1
J25	VSS[063]	VSS[144]	AE4
K1	VSS[064]	VSS[145]	AE8
K4	VSS[065]	VSS[146]	AE11
K23	VSS[066]	VSS[147]	AE14
K26	VSS[067]	VSS[148]	AE16
L3	VSS[068]	VSS[149]	AE19
L6	VSS[069]	VSS[150]	AE22
L11	VSS[070]	VSS[151]	AE25
L13	VSS[071]	VSS[152]	AF6
L24	VSS[072]	VSS[153]	AF8
M2	VSS[073]	VSS[154]	AF11
M5	VSS[074]	VSS[155]	AF13
M22	VSS[075]	VSS[156]	AF16
M25	VSS[076]	VSS[157]	AF19
N1	VSS[077]	VSS[158]	AF21
N4	VSS[078]	VSS[159]	AF24
N23	VSS[079]	VSS[160]	AF25
N26	VSS[080]	VSS[161]	AF25
P3	VSS[081]	VSS[162]	AF25

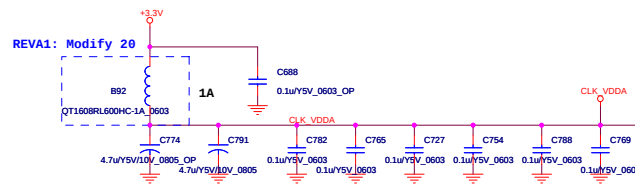
Merom Ball-out Rev 1a

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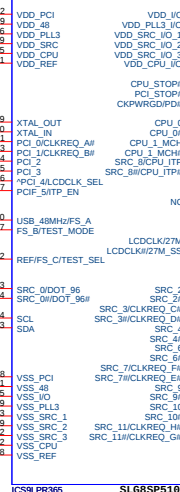
Title	P75/55IMx
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Rev	C



REVA1: Modify 20



U7



Modify 16

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

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PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

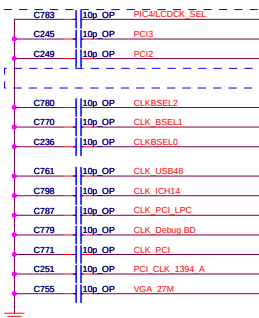
PM_STPCPU#

PM_STPCPU#

PM_STPCPU#

Reserved FOR EMI

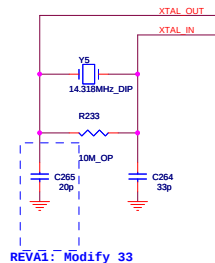
REVA1: Modify 24



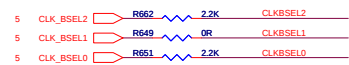
REVA1: Modify 24

	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
PSB800	0	1	0	200		
PSB667	0	1	1	166	33	100
PSB533	0	0	1	133		

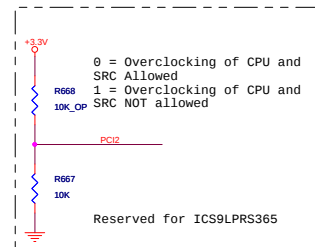
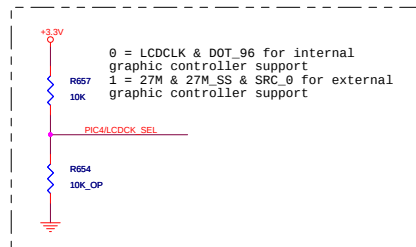
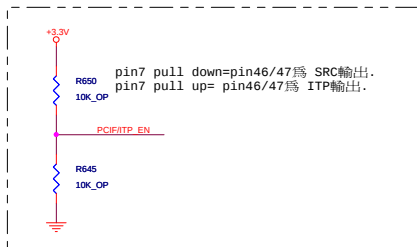
CLK REQ	From	O/P
A	ICH_SATA	SRC2
B	MCH_GCLK	SRC4
H	GLAN	SRC10
G	MINICARD1	SRC9

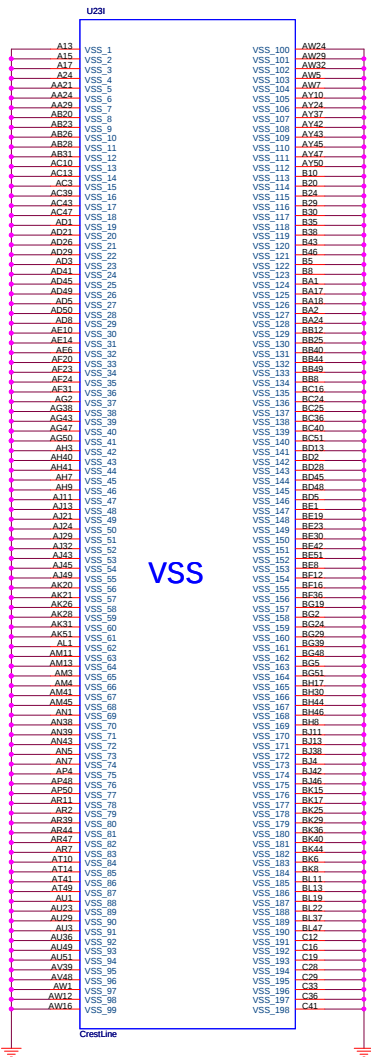


$C_e = 2 \cdot CL - (C_s + C_1)$
 $CL = \text{Crystal Load Cap} = 20P$
 $C_1 = \text{IC internal Cap} = 5P$
 $C_s = 2P$
 $C_e = \text{Crystal external Cap} = 33P$

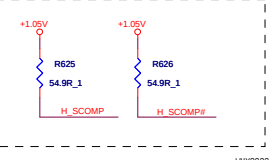


Bsel [0,2] Vil = 0.3 Vih = 0.7

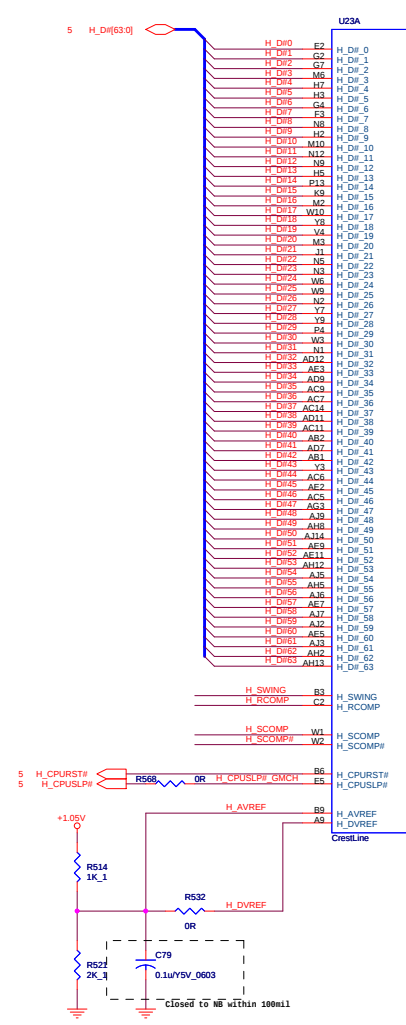
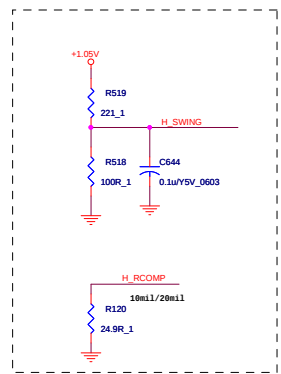




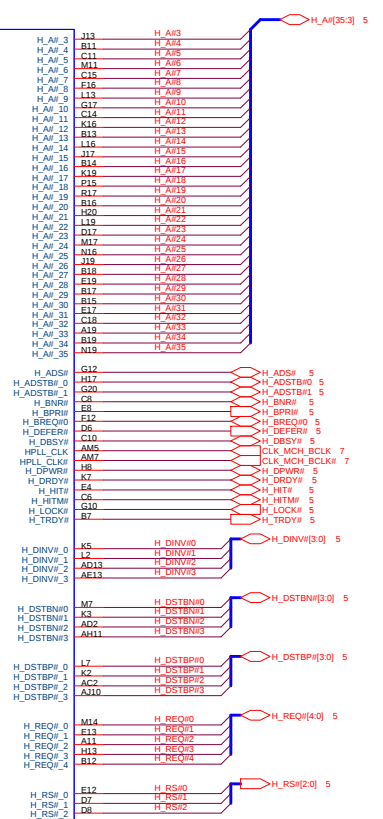
FSB I/O slew rate compensation



Reference Voltage for RCOMP

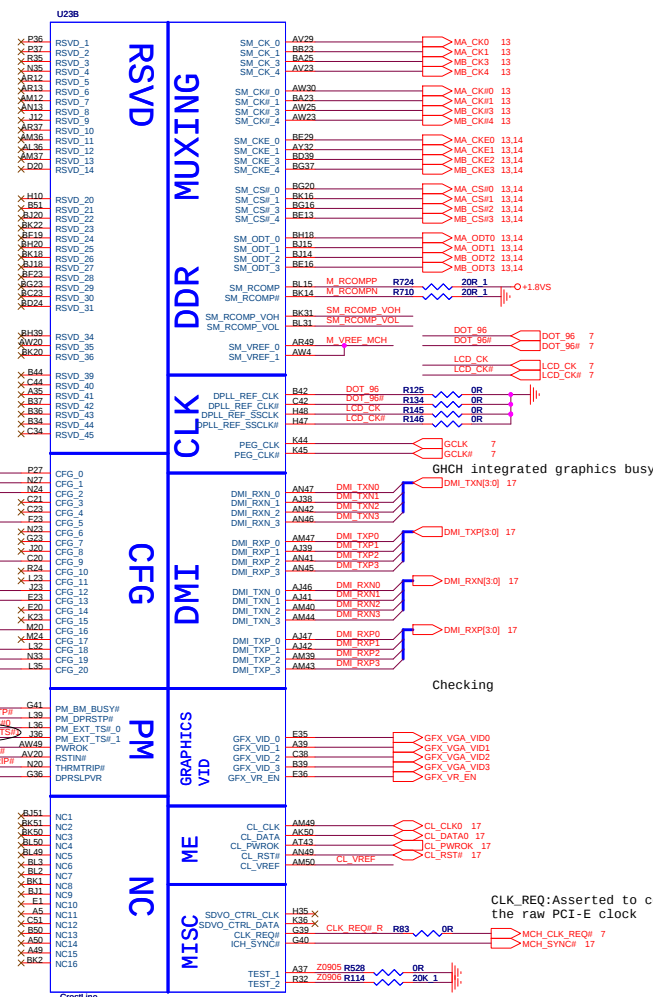
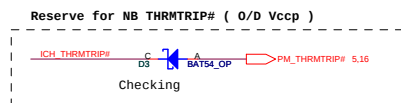
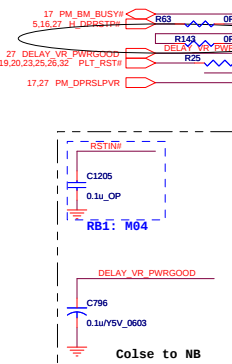


HOST



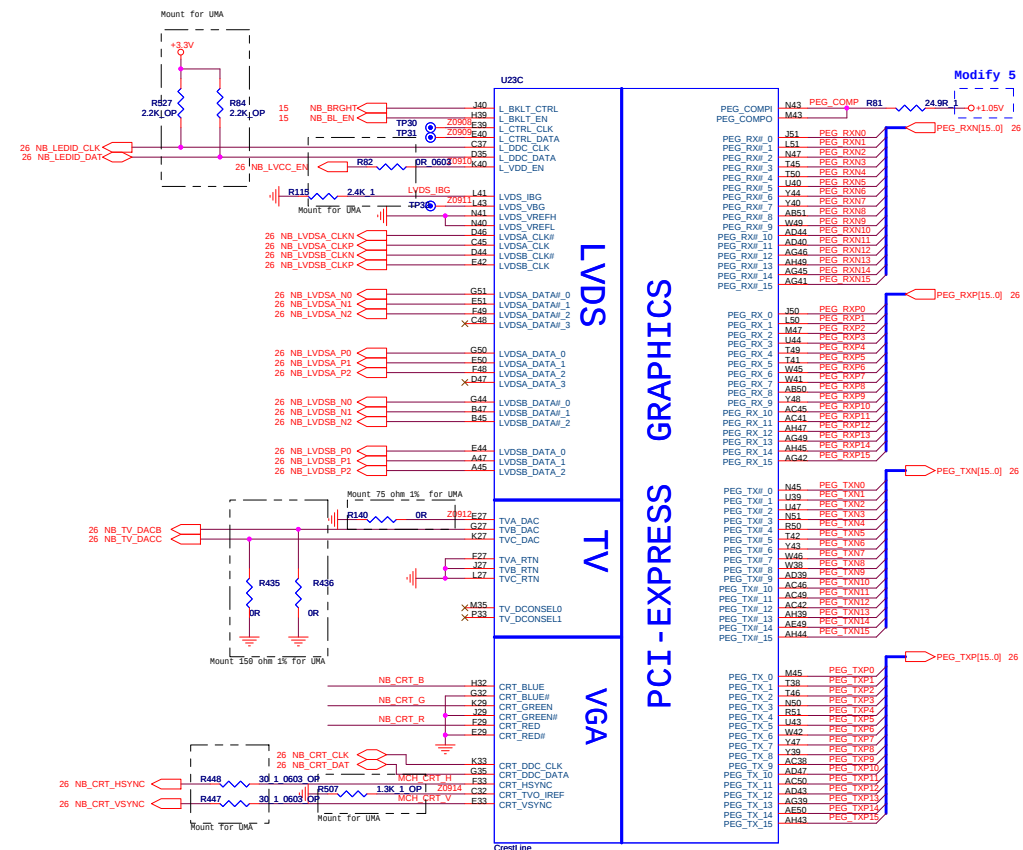
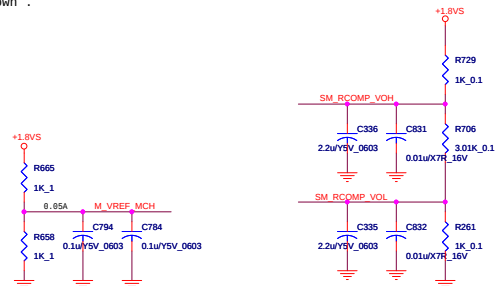
```
GCLK      => PCI-E & DMI      (100MHZ)
DREFCLK   => Dispaly PLLA  ( nun- ss 96MHZ)
DRESSCLK  => Display LVDS PLLB ( ss 100MHZ)
```

CFG0	CFG1	CFG2	Host Clock Frequency
0	1	0	800
1	1	0	667

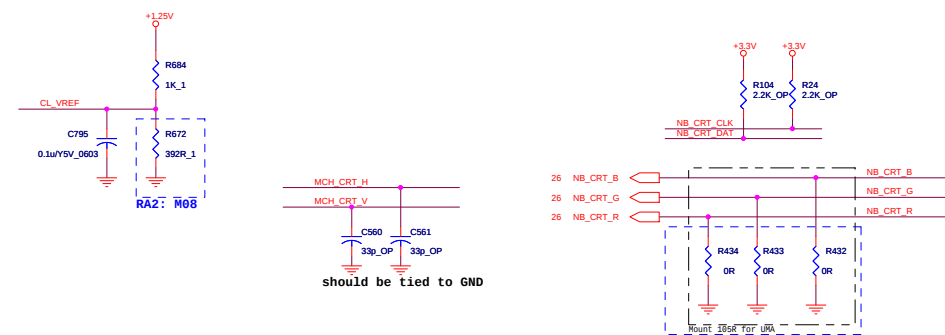


SDVODATA has internal pull down
0= no DVO device
1= DVO device present

SDVOCLK has internal pull down .

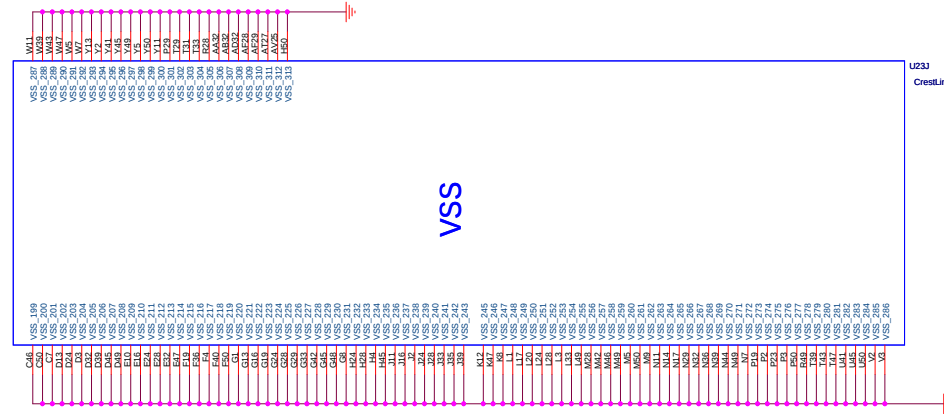
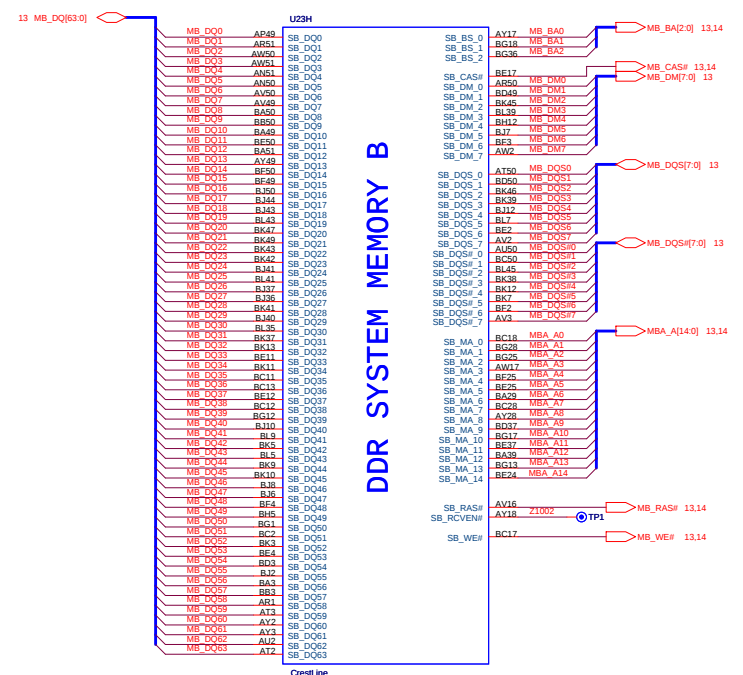
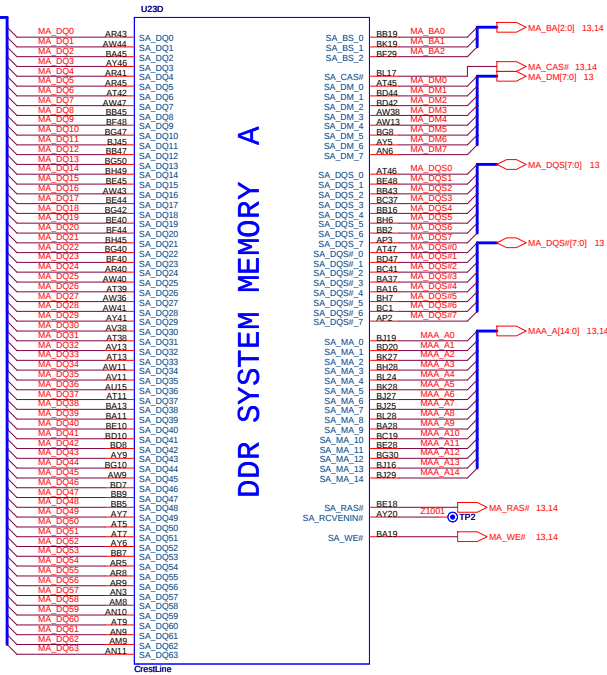


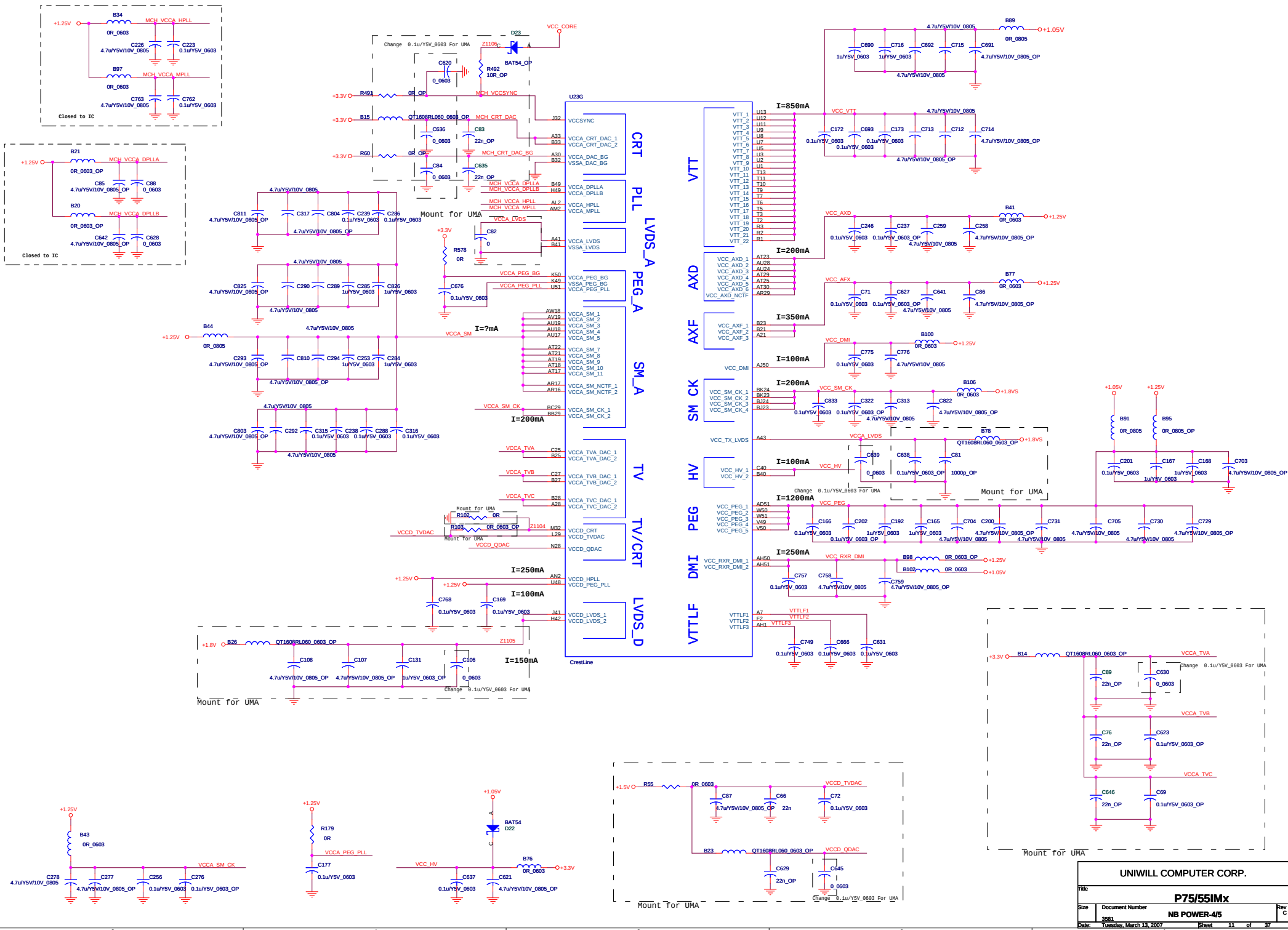
```
CFG20 ( IPD ) => 1= Only SDVO or PCI-E
                  0 = SDVO and PCI-E
CFG7 ( IPU ) => 1= Mobility CPU
                0 = Reverse
```

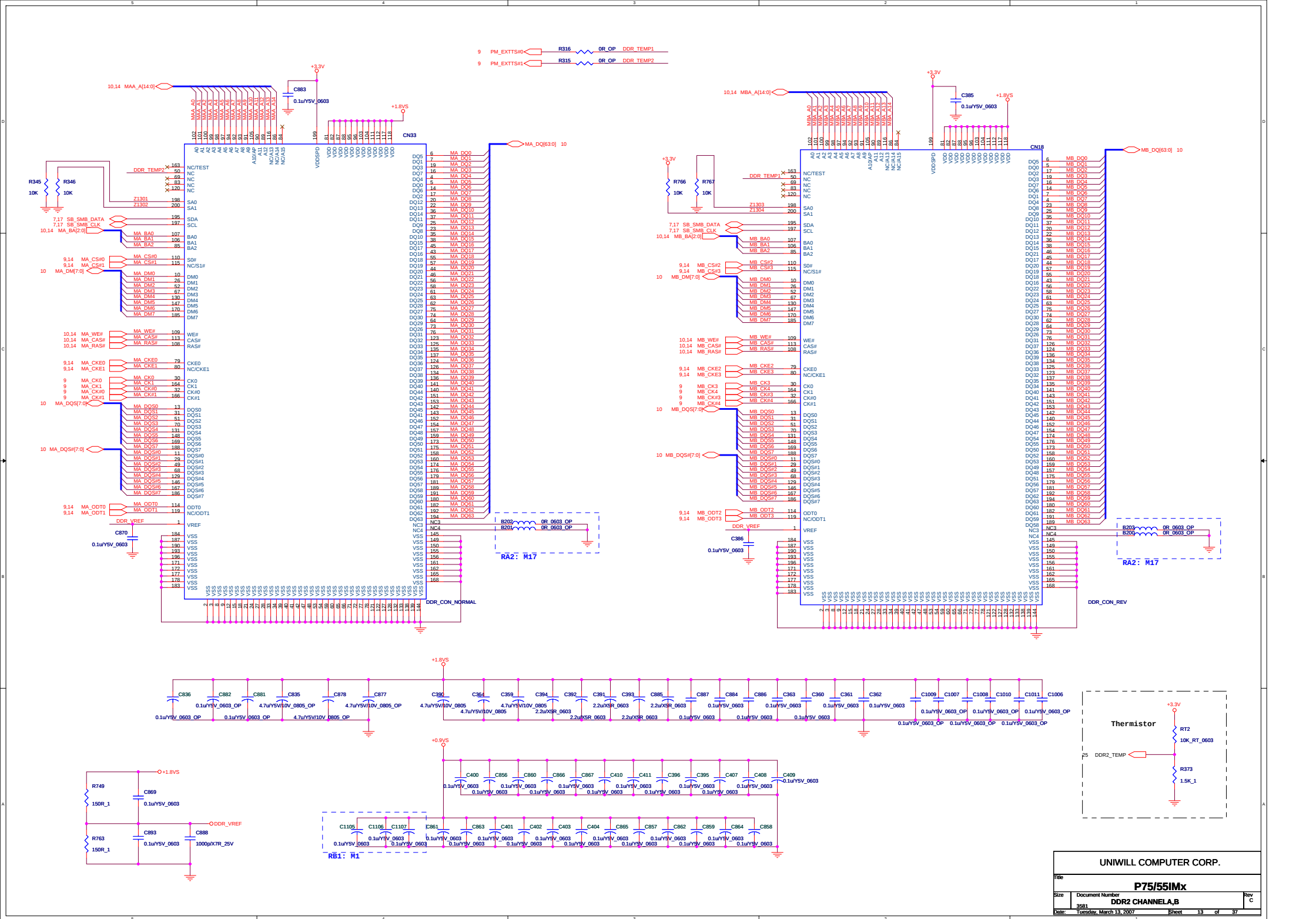


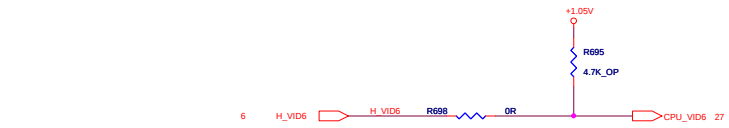
Those should be tied to GND

UNIWILL COMPUTER CORP.			
Title			
P75/55IMx			
Size	Document Number		Rev C
	NB NB DDRCLK_VGA_PCIEXPR-2/5		
	3581		
Date:	Tuesday, March 13, 2007	Sheet	9 of 37

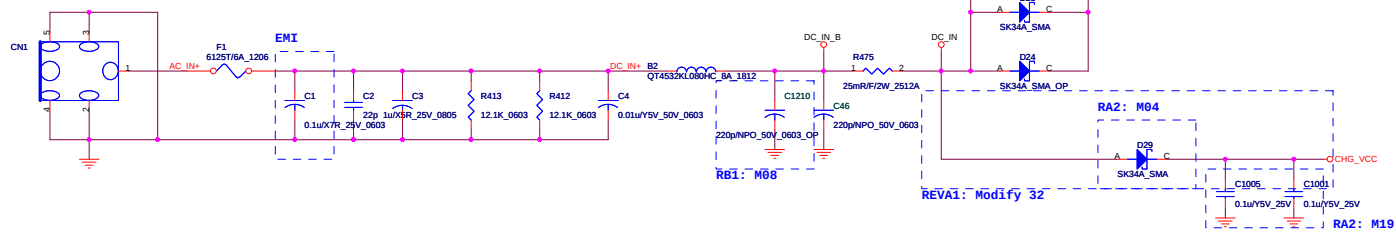
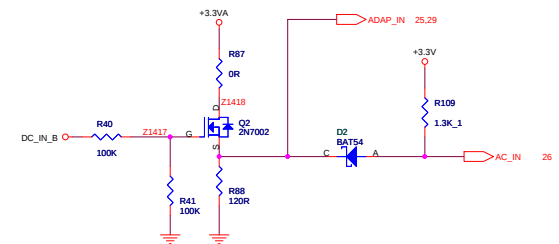
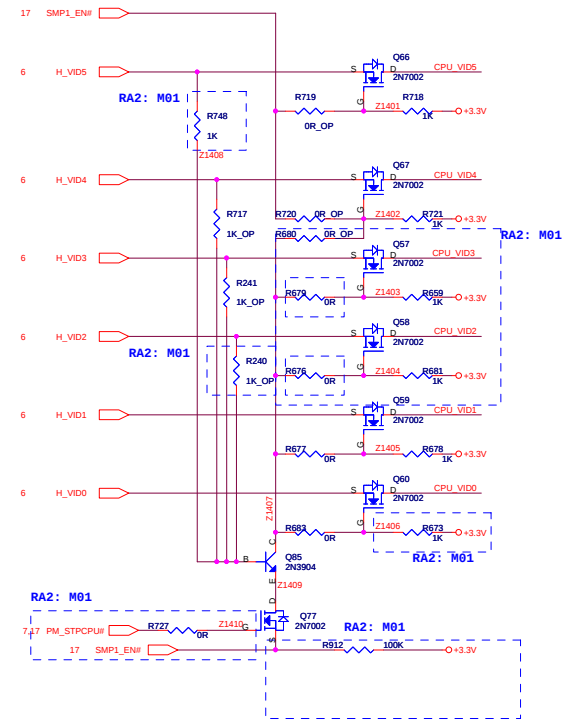




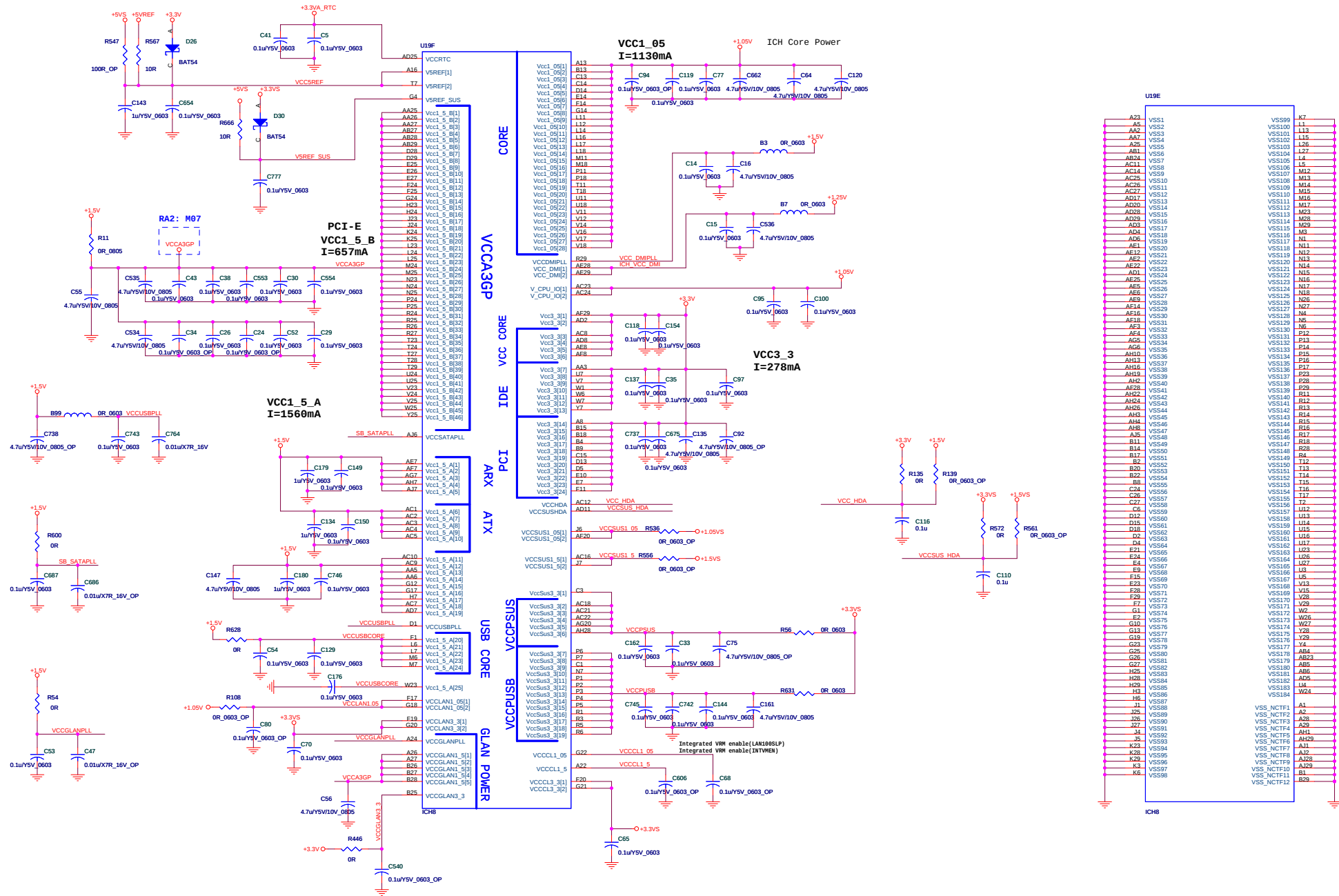




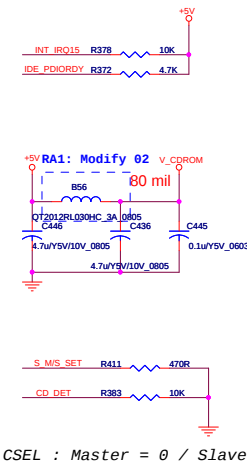
VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+5V
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		



[illegible]



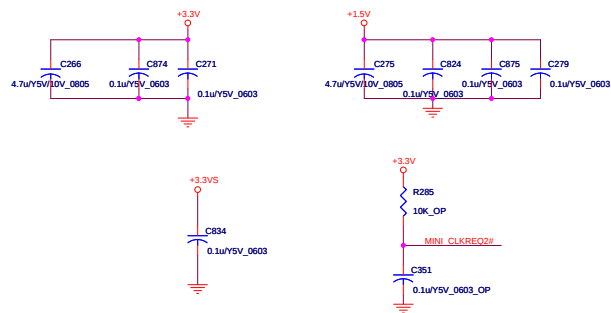
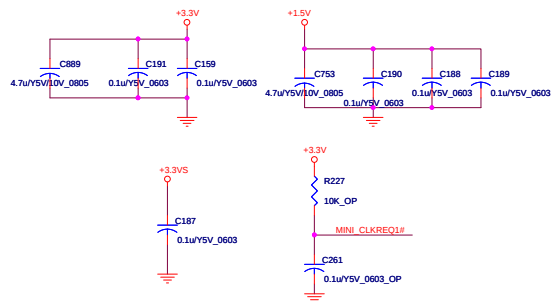
CR-ROM



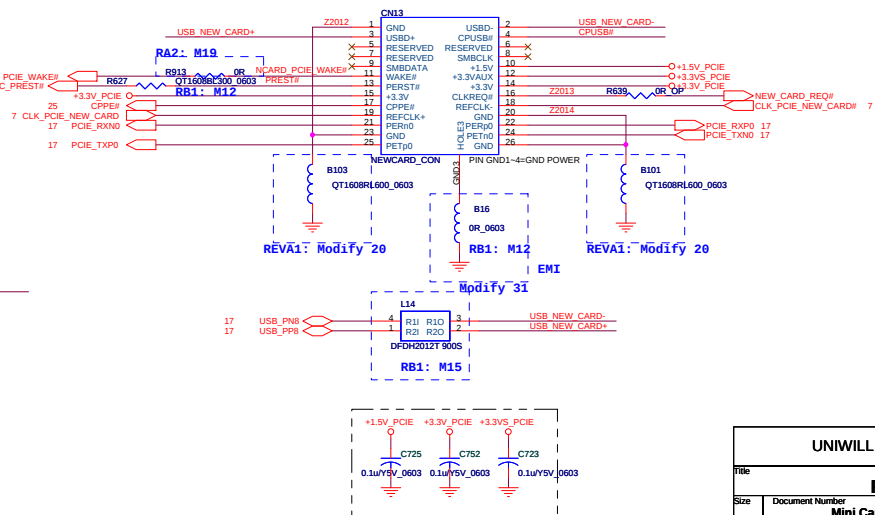
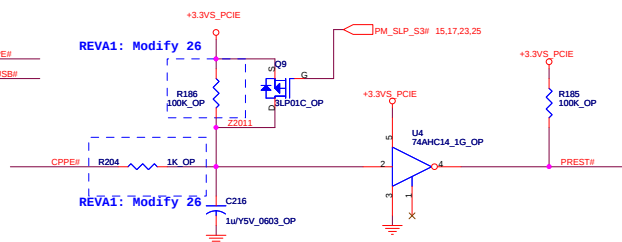
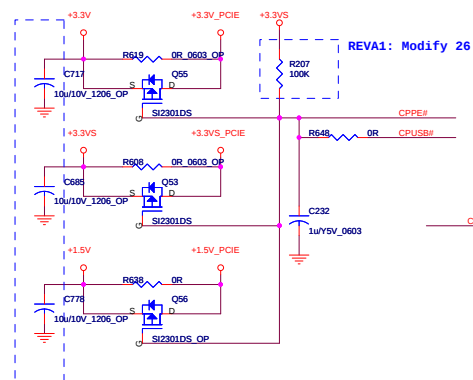
MASTER HDD

Intel PRO/Wireless 2100 LAN

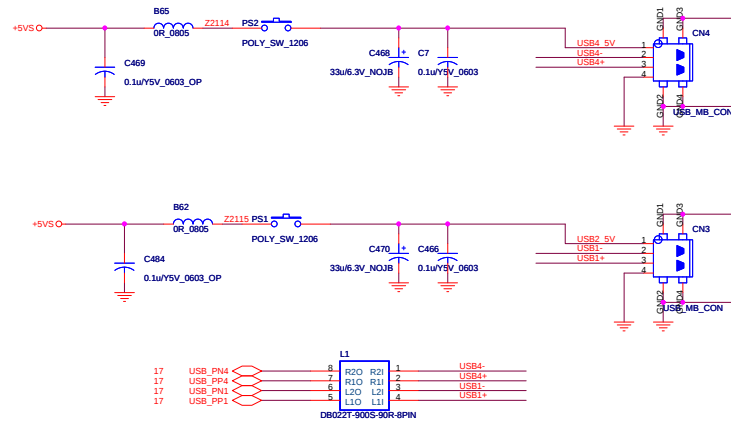
PIN11	LED_WLAN_LINK	Hi(3.3V) 1 flash/3 sec Low(0V)	Solid ON Not Associated with an AP Power OFF or RF_Kill active
PIN12	LED_WLAN_ACT	Hi(3.3V) Rapid Blinking Slow Blinking LED OFF	Passing data traffic to AP Beacon traffic to AP Power OFF or not activity or RF_Kill active
PIN13	Wm_RadioXMIT_OFF#	Hi(3.3V) Low(0V)	Enable Disable Radio transmitter turn off

[illegible][illegible]

REVA1: Modify 26

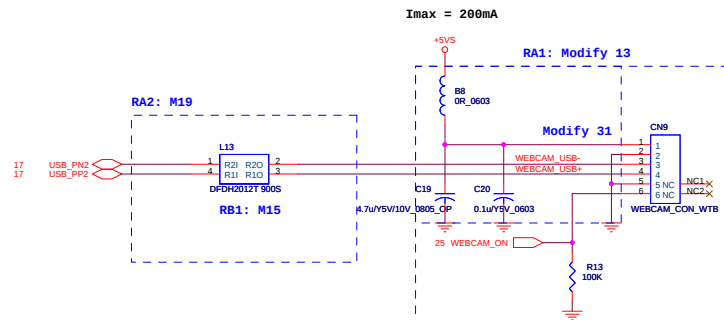


USB PORT CONN

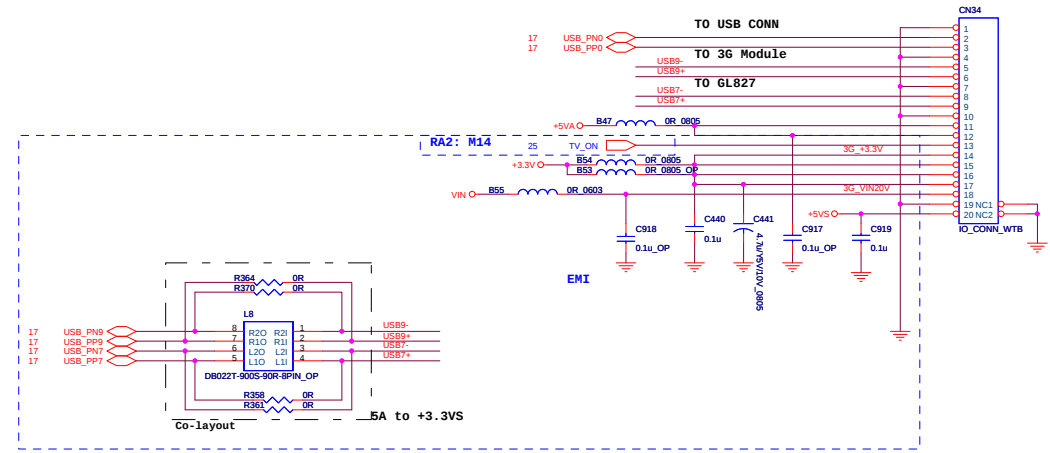


USB CONN change from 3 ports to 2 ports @ REVA2
One USB ports w/I charger remove to daughter board and add eSATA port@ REVA2

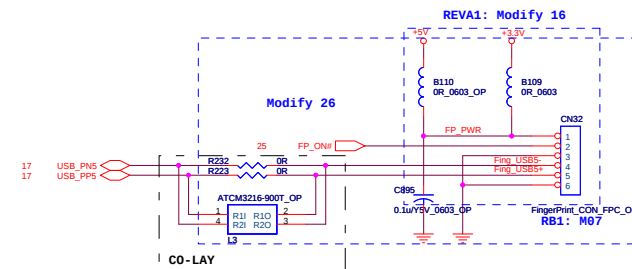
WEBCAM CONN



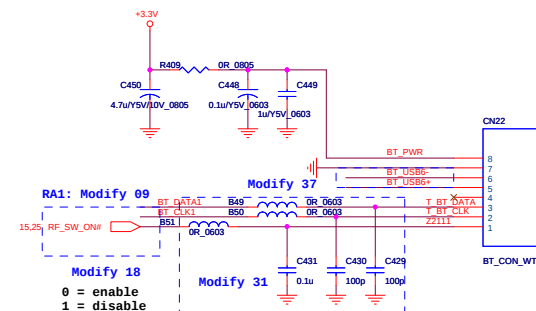
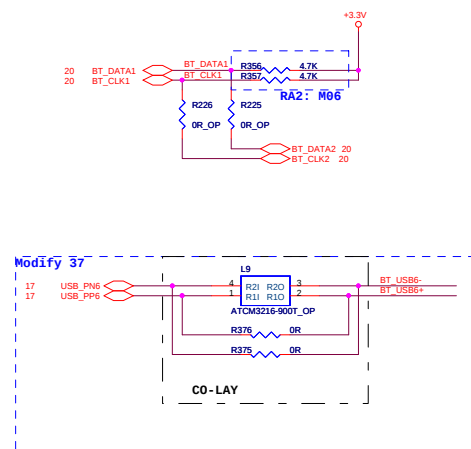
IO PORT CONN



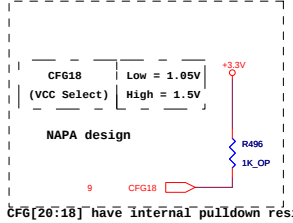
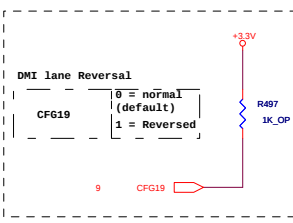
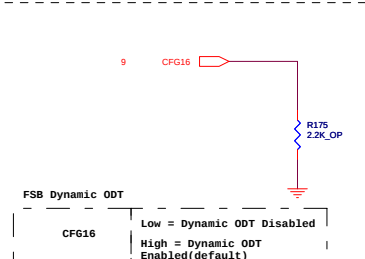
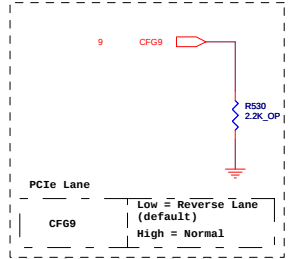
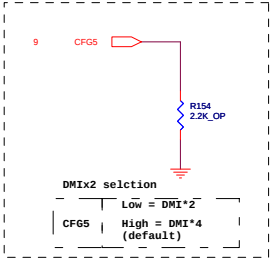
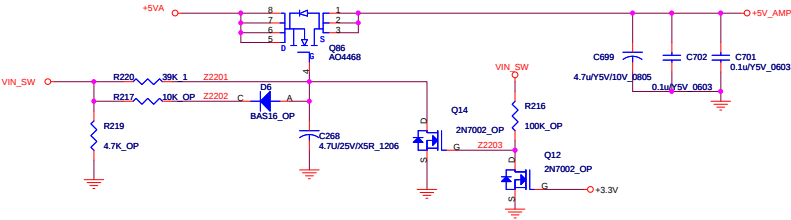
Finger print CONN (P75 only)



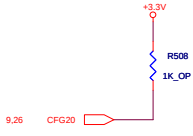
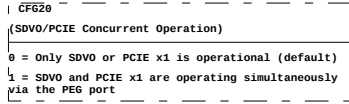
BLUETOOTH CONN



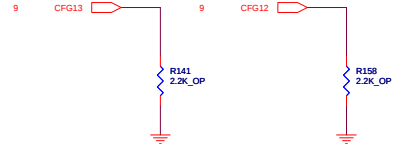
AMP VDD



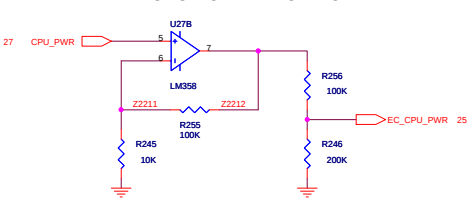
CF6[20:18] have internal pulldown resistors.



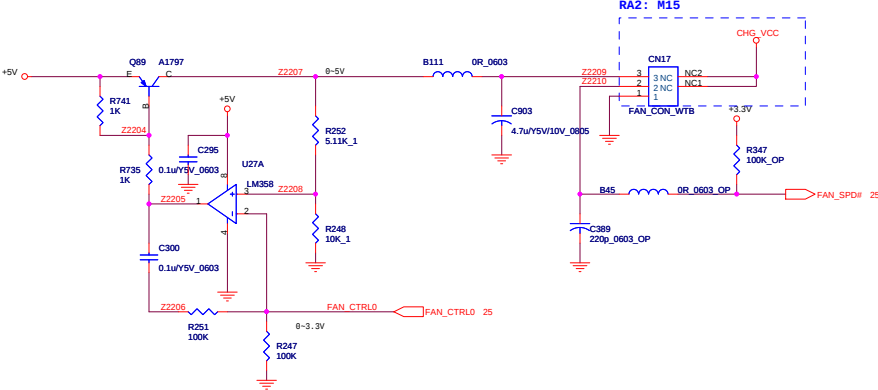
Ror / ALLZ / Clock Un-gating		
CF612	CF613	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation (Default)



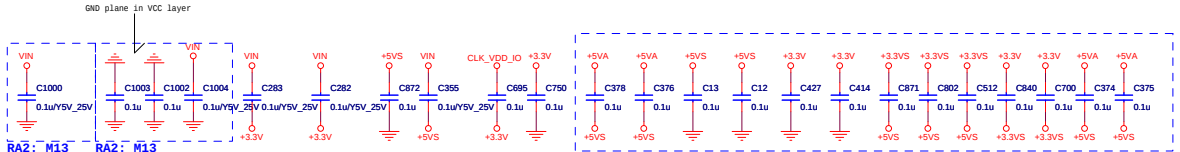
CPU POWER MONITOR



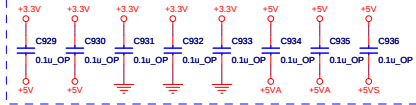
CPU FAN CONTROL

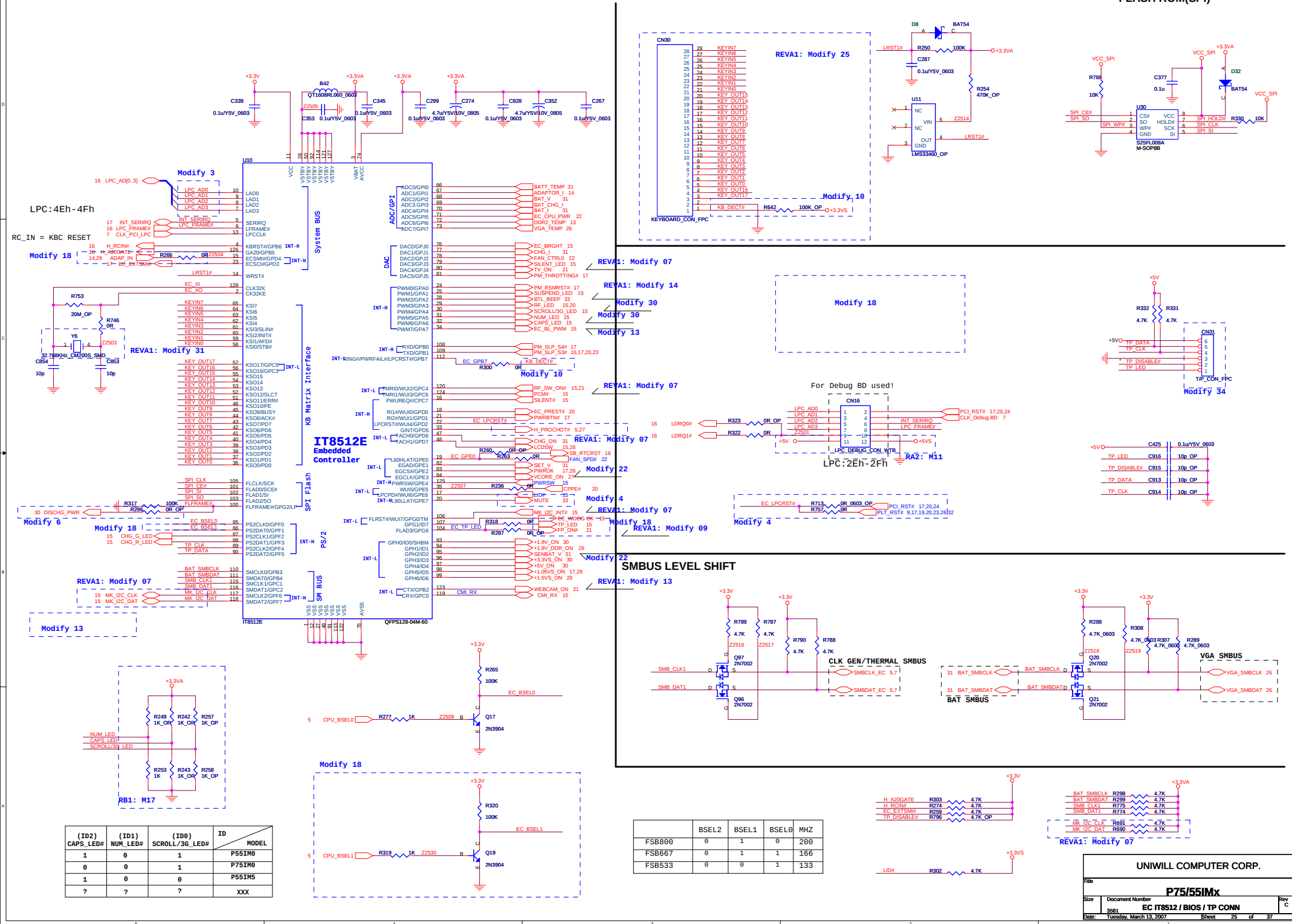


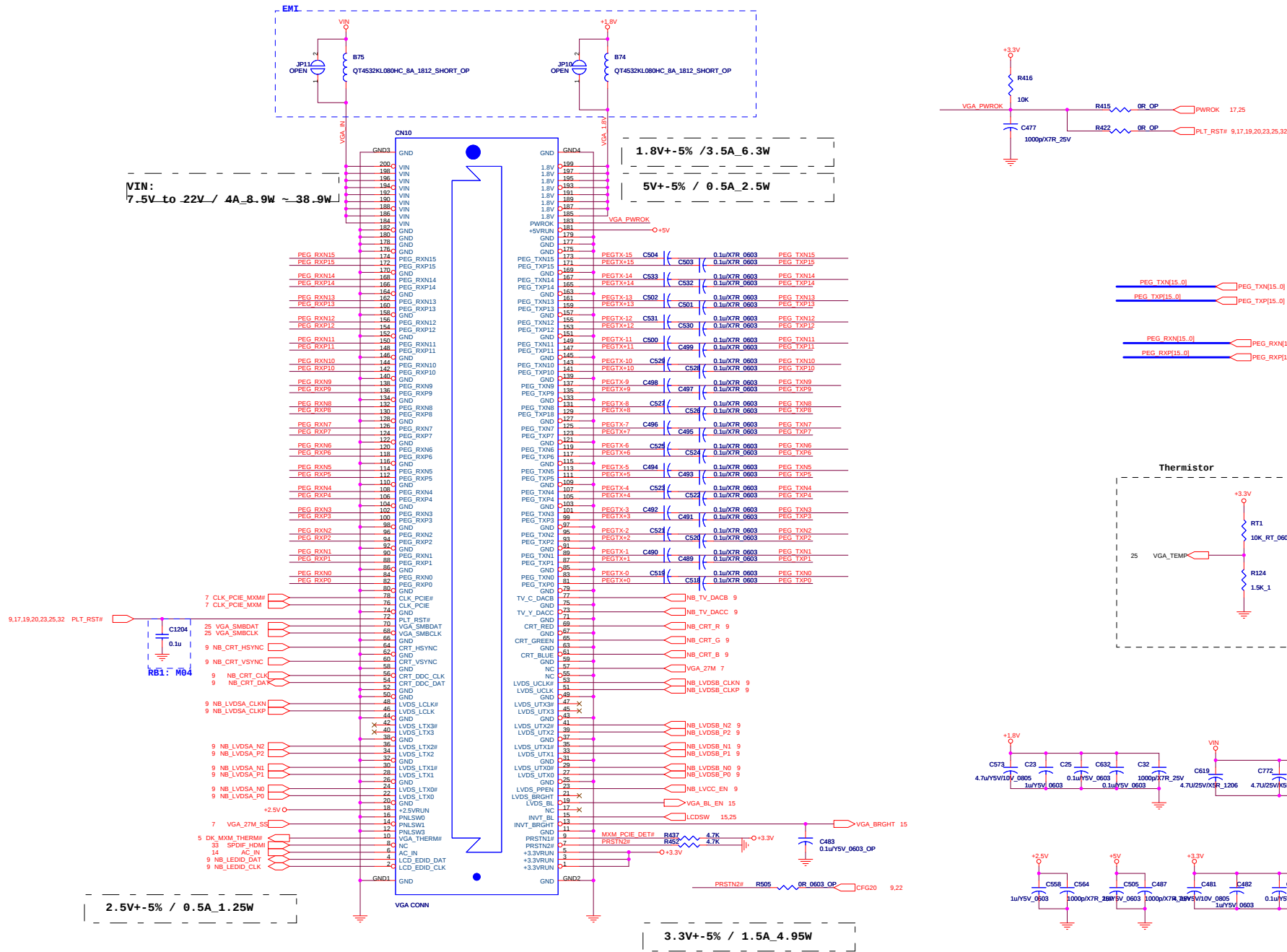
High speed current return path Capacitor

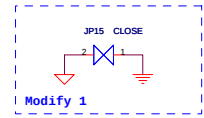


EMI Reserved

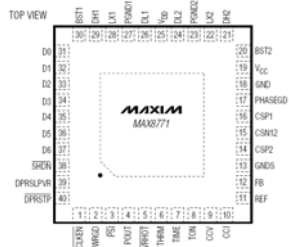


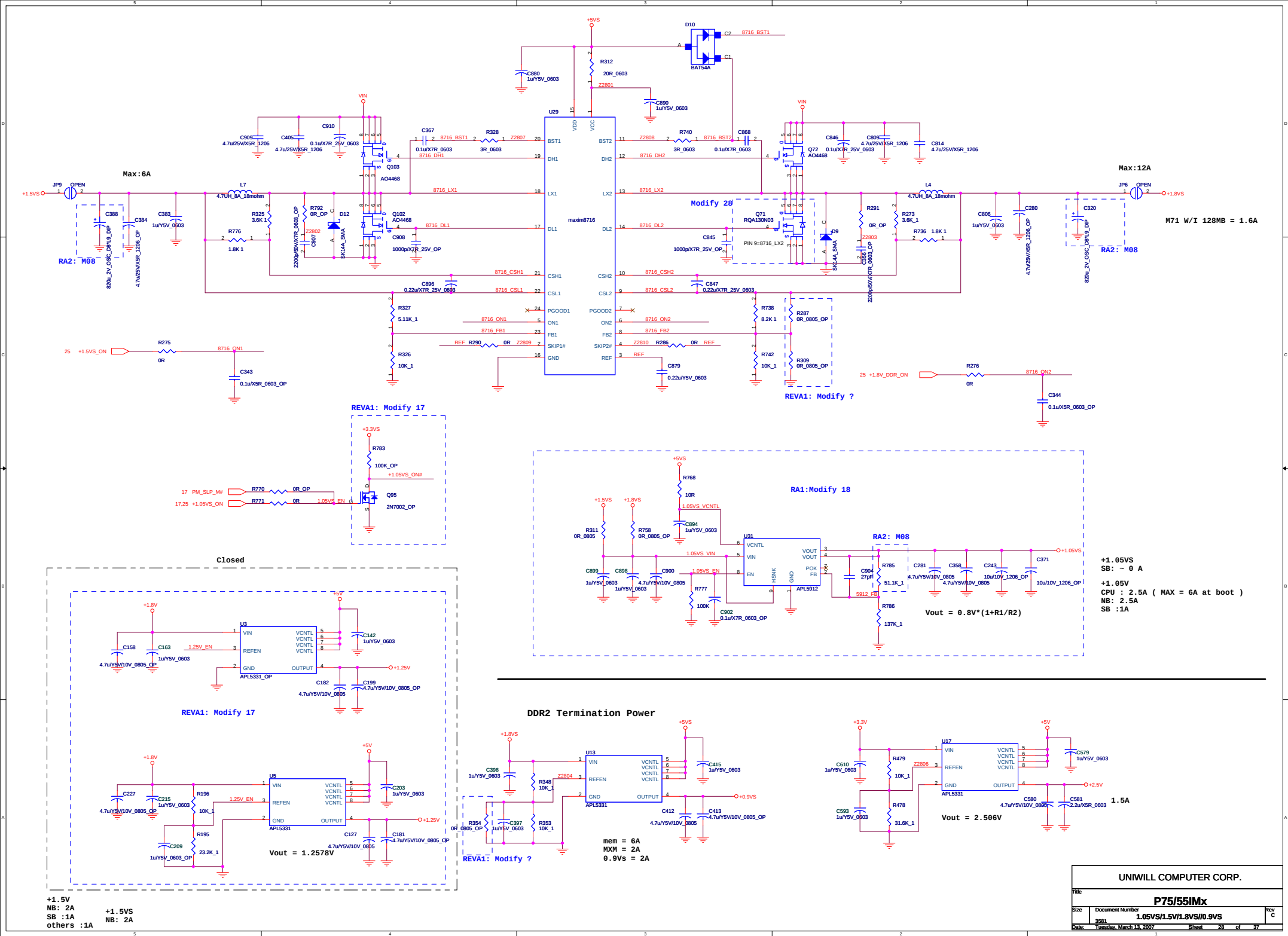


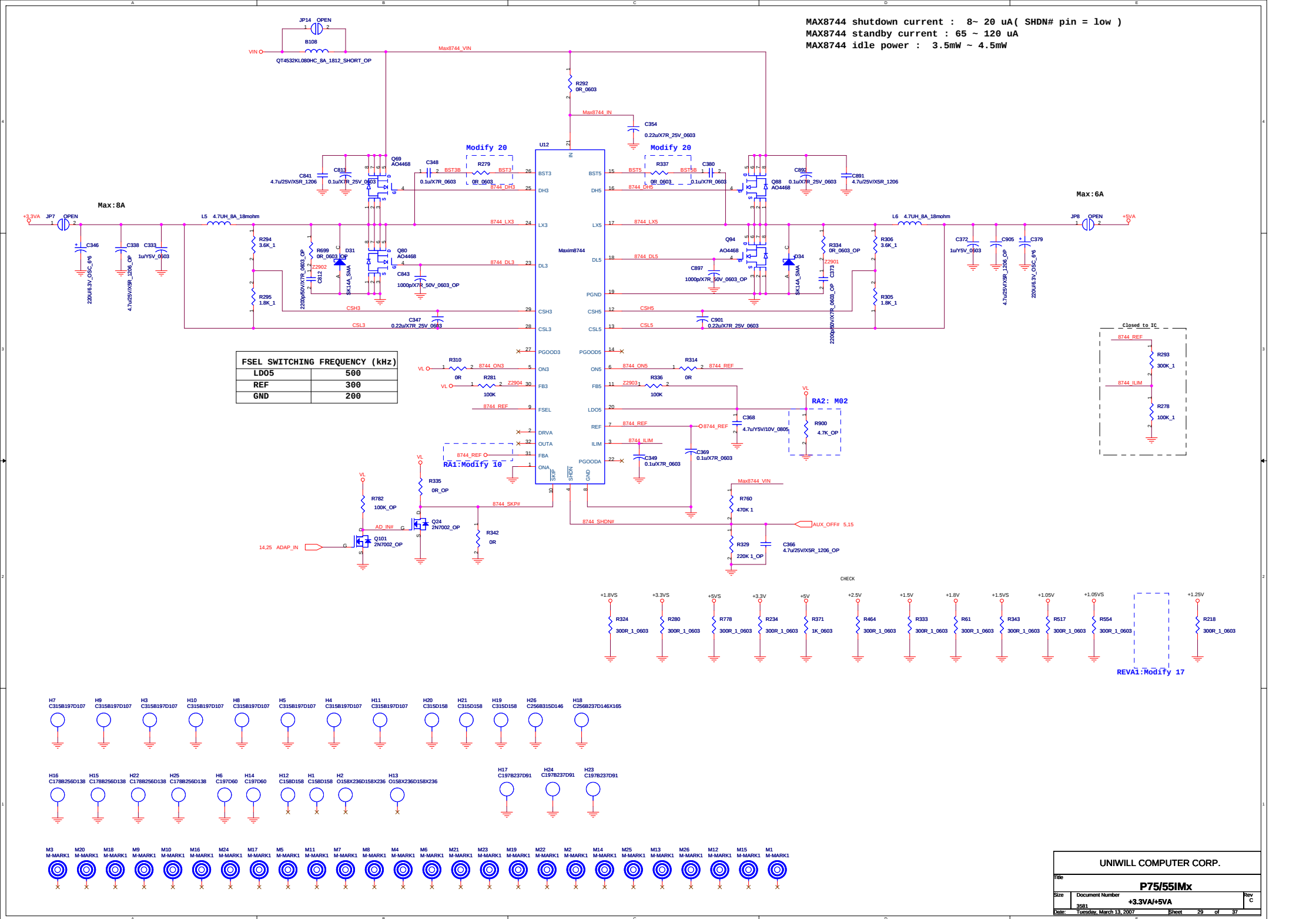


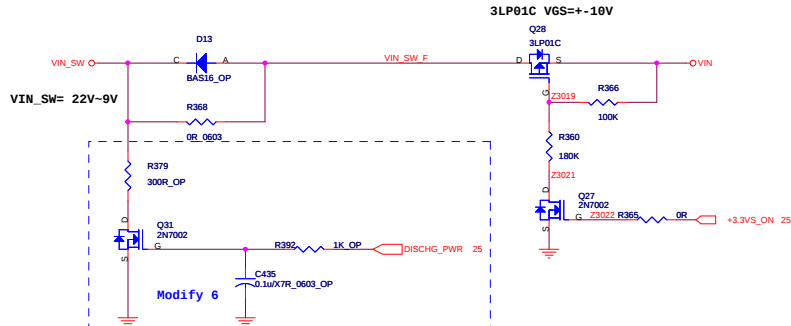
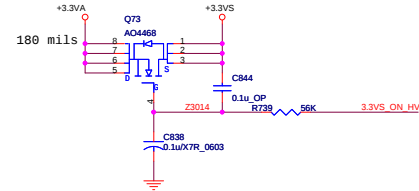
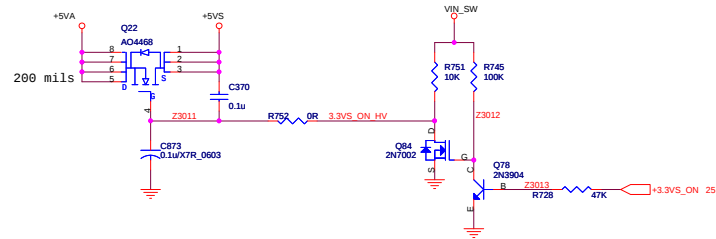
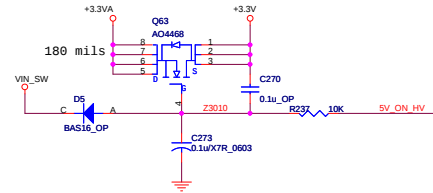
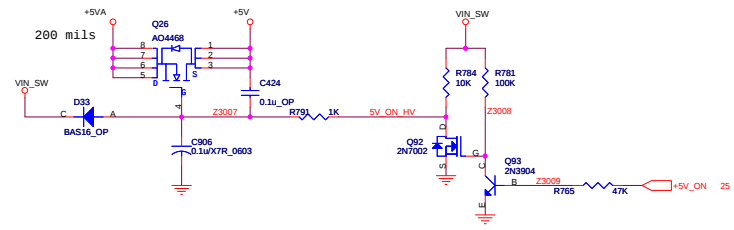
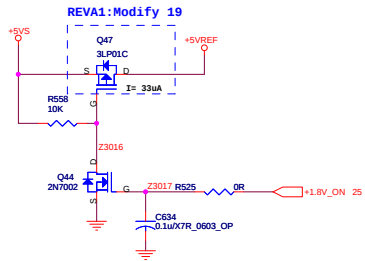
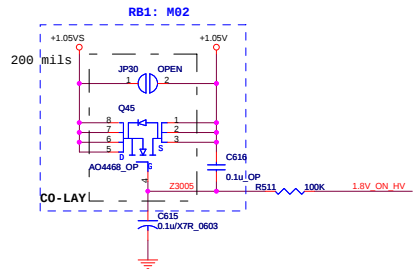
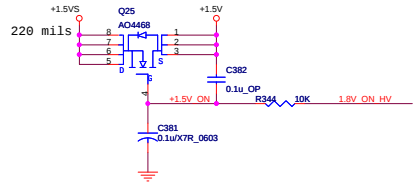
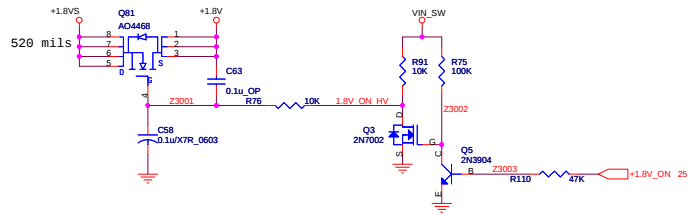


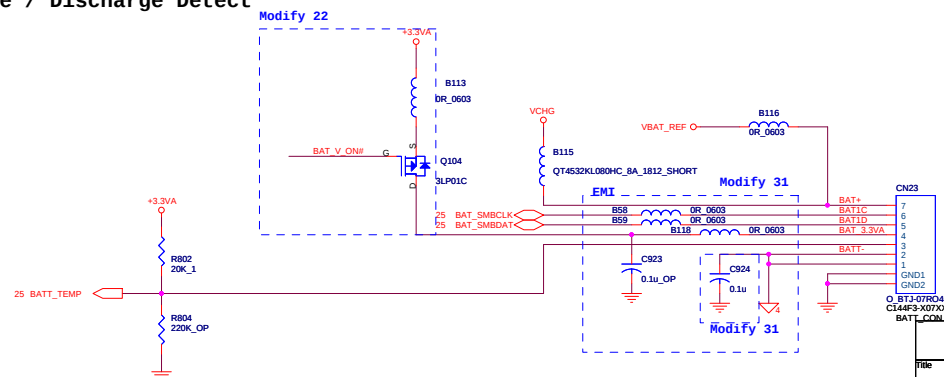
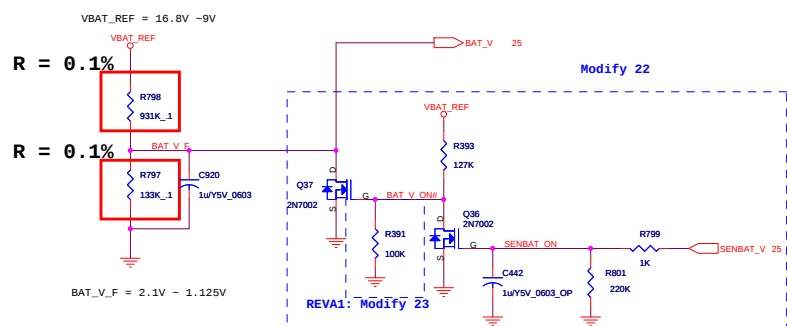
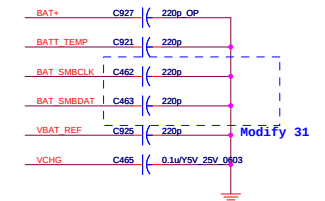
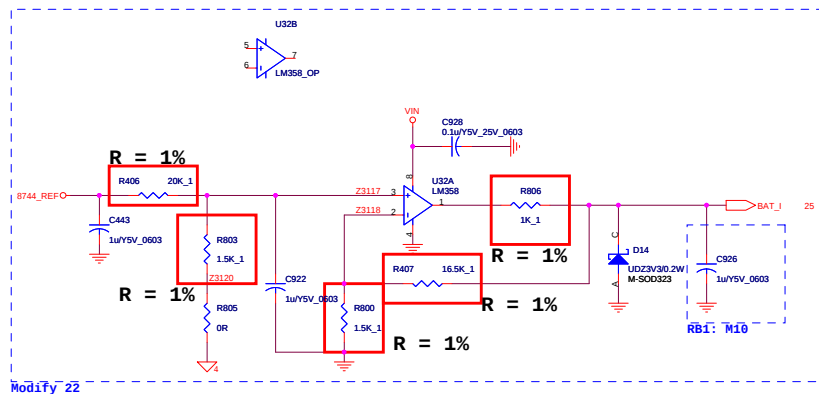
6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	(HFM)
0	0	1	1	0	0	0	1.2600	Boot Vout
0	0	1	1	1	0	0	1.1500	Memor(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down



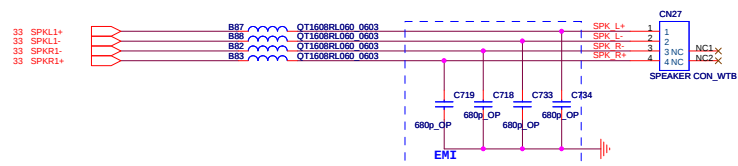




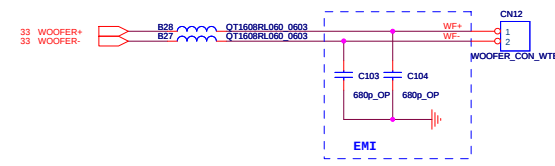




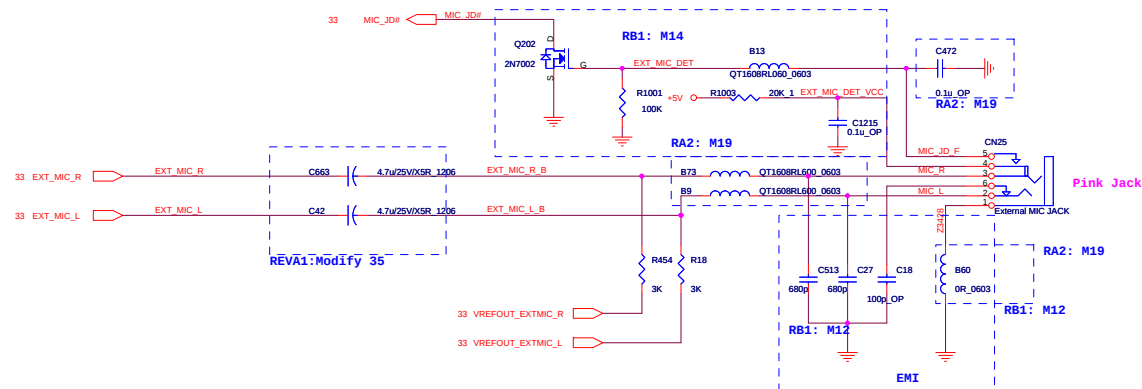
Internal SPK



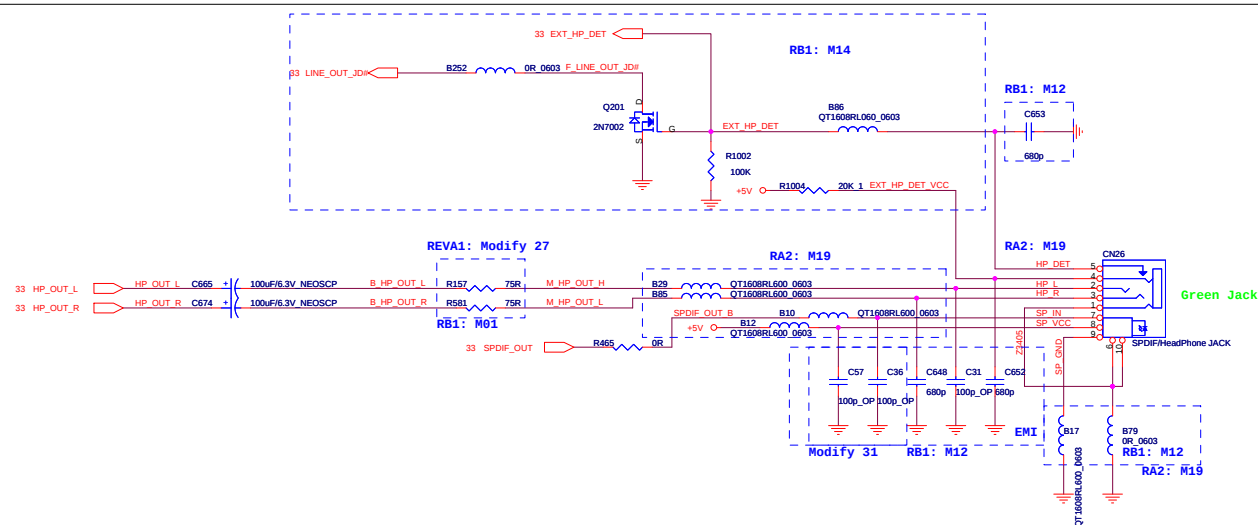
Woofer



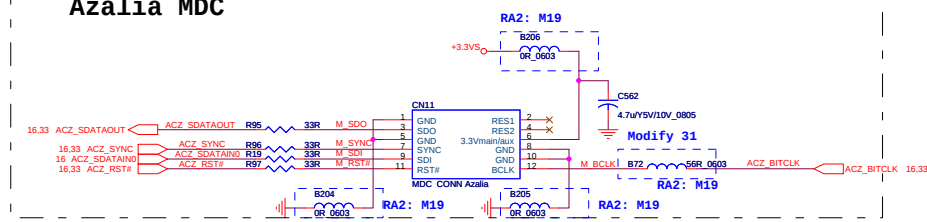
External Mic



SPDIF/HeadPhone



Azalia MDC



RA change list:

Symbol	What change	Page	Why change	Note
Modify 1	Add jump JP19 to conect AGND and GND	27	Presenting from other project mistake	
Modify 2	R8 from +CPU_CORE change to GND	6	Mistake net	
Modify 3	LPC AD0 ~ AD3 mistake	25	Mistake net	
Modify 4	PLT_RST# and MUTE swap	25	Follow older version and pin assingment	
Modify 5	+1.5V changed to +1.05V	9	Mistake net	
Modify 6	Add Q200, R900 and changed EC's MPWORK to DISCHG_PWR	25&30	VIN_SW discharge circuit	
Modify 7	Take out R689, C713 and mount R682 and changed MPWORK to PWR0K	17	Follow Intel recommend	
Modify 8	Add R901,R900 and net: ICH_GPI010, ICH_GPI014	17	Follow Intel recommend (AMT didn't supported AMT)	
Modify 9	U32(1394) change IRQ form INT_PRIQ# to INT_PIRQ#	17&24	For blance IRQ routing	
Modify 10	Add R903 100K_0P, TP50, TP51, and change from QRT_STATE to KB_DECT	17&25	For P75 K/B automatic detect.	
Modify 12	U8 form JMB363 change to JMB362 and other	17&32	cost down solution and form PCIE6 change to PCIE5 by SW required	
Modify 13	Add C1000(0.1u_0603) and C1005(4.7u_0805)	21	Reserved for power bypass and EMI	
Modify 14	Add RP20, RP21 0 ohm and take out L10&L11	23	Reserved for replace com-choke	
Modify 15	Add R910 and change R347,R351(24.9->29K), R137,R151(4.7K->0R), R167(49.9K->0R) and take out R131,R152 ,R568, R142	19&33	Adjust Audio gain	
Modify 16	Change R170 to pull high +3.3V and take off R554(0R)	07&17	Solving for C3 hand up	
Modify 17	Del R487/R492(0R_0P), JP1, R36 and swap net:M358+/- net ; CN11 change type	21	Delete reservedcircuit and swap wrong net ; CN11 by ME required	
Modify 18	Add R904(100K), R905(1K), Q201, net: BSEL1 tired to GPF1 and net:ADAP_IN from GPF1 to GPD4 ;	05&25	For support CPU of FSB 533	
Modify 19	C49&C50 from DIP change to SMD; Mount,Q6,Q52,Q8,Q53,Q12,R165/R176, R640,R189,R194,C709 ; take out R161,R179	05&25	For ME limit and POP nose / Head phone POP nose	
Modify 20	Add R911,R912(0R_0603)	29	Resistor reserved for fine tune	
Modify 21	Take out R618(10K)	17	Pull high wrong power plane	
Modify 22	Delete R837 and JP17; R412,R409,R416,R407,R831,R835,R834,R411, U47 and R832,R836,R840 Change R406(127K->20K 1), R410(127K->1.5K 1), R414(1M->0R_0603), R404(1M->16.5K),R830(1K->1.5K), C898(0.1u->1u_0603) C900(0.1u->0P), and add D50	31	For dumb bettery	
Modify 23	Add R914,R913(0R) , C1007(0.1u), C1008(4.7u), C1006(0.1u), CN37	20&21	Reserved for support P75 TV and 3G together	
Modify 24	Max8776 change to 02811	35	Delete GFX power(965GM) and Add +1.05VS power	
Modify 25	Delete Q91, Q84, Q83, Q90, R774, R725, R726, C817, C324,C308, C294, C776, C826, C214, RT4	27	Delete reserced power circuit	
Modify 26	Add R916, R915(0R), R917,R918(0R_0P) and CN38	20	Reserved for P75 function of Figer print	
Modify 27	L14 from FRC1394 change to ATCM3216 and Add L20	21	CN5 and CN11(USB) split, cause of ME change location	
Modify 28	Change U43 package from MOS-8 to PMOS-8 and U40 mount	28	For support to supply higher current (1.8V:10A ; 1.05V :2.1A max)	
Modify 29	R387 change from 5% to 1%	31	For improve accurate charger currect	
Modify 30	CAPS_LED and SCROLL/3G net swap	25	EC required	
Modify 31	Deleted R95 and add B102 ; Deleted R14 and add B103 ; Deleted R10/R11 and add B101 / B104 ; C1000 Deleted R382,R383,R384 and add C1013,C1014,C1015 ,B105 ,B106, B107 ; Add C895,C896, C899 ; deleted R838,R839, and addB108,B109,B112,B113	15&21 & 34&31 &20	EMI required	
Modify 32	Add Q209, D53	33	For sus-woofer can't mute by codec issue	
Modify 33	Add L21 and delete JP15,B86	27	Co-layout reversed for improve Vocre effect	
Modify 34	CN35 change footprint from 0.5mm to 1.0mm pinch	25	ME required!	
Modify 35	Add B110 to +1.5V and take out B67	7	CLK_GEN power saving	
Modify 36	Add C1010,C1031,C1028,C1022,C1024,C1026,C1029,C1023,C1027,C1030,C1016,C1020,C1019,C1025,C1017,C1021,C1032	15	EMI required	
Modify 37	Add L22_0P and RP22 co-layot and change USB pair ; Add C1033,C1034(OP) and B111	21	EMI required (B111 for +1.5VS cross CLK_GEN)	

RA2 modify list:

Symbol	What change	Page	Why change	Note
RA2: M18	Add C1002/C1003 0.1u Add C1004 0.1u_25V	36	For PCIE6 pair current return path For USB0 pair current return path(remove trace to improve)	
RA2: M19	Add C1005/C1001 0.1u/Y5V 25V Mount L13 0R/0201 9005 B1NTECH ; take out R430/R429 0R Add B204/B205/B206 0R_0603 Take out C472/B60/B79/C471/C488/C653 B25 from AMC16080600NT change to QT1608RL300HC2A R551 from 0R change to 100R B99/B18 from 0R_0805 change to QT2012RL120HC3A-LF_0805 B12/B540 from 33R change to 56R B17 from 0R_0603 change to QT1608RL600_0603 B10/B12 from QT1608RL060 change to QT1608RL600_0603 Add R913 0R Add B207/B208 0R_0603 Add C1006-C1011 0.1uF_0603_0P B29/B85/B73/B9 change to 0R_0603	14 21 33&34 20 15 13 33&34	Reserced for EMI required	EMI memo 2.0
RA2: M20	Add C1012/C1014 0R_0603 ; C1013/C1015 0R_0402	15	Reserced for RAID unstable issue	
RA2: M21	R205 mount 100K	32	eSATA CONN detect pull high	
RB: M01	LT2.3/LT6.6 change to tie to TCD	23		

RA1 change list:

Symbol	What change	Page	Why change	Note
RA1: Modify 01	Add D69 BAT54 between ODD and LED	15	Solving ODD detect fail within HDD issue(BIOS can't detect ODD master or slave)	
RA1: Modify 02	B42 change from QT1608RL060_0603 to QT2012RL030_3A_0805	19	Reserved for more power consumption ODD as HD-DVD	
RA1: Modify 03	Net changed SMBCLK and SMBDAT to ICH_SMBCLK and ICH_SMDATA	17	Net disconnect from SB to CLK GEN	
RA1: Modify 04	R449, R450, R451	9	Intel recommend	
RA1: Modify 05	U24.F20(LAN_TX1-) change to U24.E20	16	update library	
RA1: Modify 06	Net: CRB_SV_DET pull high from +3.3V to 3.3VS	17	Pull high power wrong	
RA1: Modify 07	Change CN26 to 20 pin and add net: MK_I2C_DAT/CLK/INT# to KBC and LED signal Change Net:Mail# to SB_RTCRST to MK_I2C_INT# and SMP1_EN# to H_PROCHOT to MK_I2C_DAT Net: BROWSER# rename to PCM#	15 & 25	For multimedia bottom function used ; Reserved to P75 LED BD	
RA1: Modify 08	Take out R12(1K) and mount R17(1K)	23	Solving +3.3V leakage during power on and S3	
RA1: Modify 09	Net: BT_ON# change to FP_ON# and BT_ONchanged to RF_SW#	15/2125	KBC change GPIO to FP_ON# (Finger print ON)	
RA1: Modify 10	Max8744 pin31 tied to net change from VL to 8744REF	29	FAE recommend(voltage rating of FB pin is VLD0+0.3V only)	
RA1: Modify 11	Add net: RAID_CONF0-3 and CN36/CN41	17 & 19	Reserved for P75 H/W RAID configuration setting and CONN	
RA1: Modify 12	Mount R554	17	Implement STP_CPU(NB CLK set Free run)	
RA1: Modify 13	CN9 4P->6P, add net: WEBCAM_ON to EC, deleted +5V power	21 & 25	Implement WEBCAM ON/OFF function	
RA1: Modify 14	Net: Silent LED and BEEP swap	25	BEEP should be generated by EC's PWM	
RA1: Modify 15	Delete LZ1	27	Delete reserve function	
RA1: Modify 16	USB pair change USB3 to USB5 and CN38 4P->6P and add net:FP_ON#	20 & 21	Implement Finger print ON/OFF function	
RA1: Modify 17	U3/U5 VIN change from +1.8VS to +1.8V and deleted enable; Delete Q46, C598, R543, C596	28 & 30	+1.25VS LDO power change to +1.25V	
RA1: Modify 18	U40 Change from APL5331(2A) to APL5912(5A) and delete U10	28	APL5912 rating(5A) and dropout (200mV) better than APL5331	
RA1: Modify 19	Q47 change from SI2301 to 3LP01	30	Cost saving (VINSW current = 44uA)	
RA1: Modify 20	Add B203 0R_0805, B79/B80 QT1608RL060_0603 ; B66/B110 QT1608RL600HC-1A_0603	7/20/33	EMI requirement	
RA1: Modify 21	Add U50_OP and U4.7 change net to HDMI_SPDIF_ON#	33	U50 reserved for SPDIF buffer ; Could be controlled be codec	
RA1: Modify 22	Add net: MUTE	34	MUTE to controlled HP POP issue	
RA1: Modify 23	F2 0603->1206 ; R413 40mR->25mR ; R387 39K-> ??K ; Add R1003 100K / R925 100K->127K	31	F2 co-layout poly switch; combine with DC1	
RA1: Modify 24	Delete C148/C247 ; SRC11 change to RAID CLK	7	SPEC changed	
RA1: Modify 25	U32 from 24PIN to 28 PIN and deleted CN29	25	New K/B supported	
RA1: Modify 26	Add Cap reserved to power by pass ; change pull high power plane	20	Reserved for imporvement power drop ; the circuit wrong	
RA1: Modify 27	Add R between HP R/L line	34	Reserved for HP amplitude requirement	
RA1: Modify 28	Take out R and C	33	Imporing background noise	
RA1: Modify 29	Add R between HP R/L line	33	Reduce amplitude to meet requirement	
RA1: Modify 30	Take out some component	33	Taking out reserved function	
RA1: Modify 31	Crystal change to SMD	16 & 25	Manufactory required	
RA1: Modify 32	Modify Charger circuit	14 & 31	Reference DC1 circuit and hope to improve yield	
RA1: Modify 33	Modify Cap value	07 & 24	Fine tune crystal precision	
RA1: Modify 34	R change from 100K to 31.6K	15	PWM inverter sink current higher	
RA1: Modify 35	CD tired to GND ; MUTE function ; LINE IN Cap	33 & 34	Vista not support anlog ; ADI can't lost ; AP measure fail	

RA2 modify list:

Symbol	What change	Page	Why change	Note
RA2: M01	Mount R647/R692/R693/R694 4.7K; R673/R748/ 1K; R676/R679/R727 0R; R240 1K_OP	14	For implement smart power function	
RA2: M02	Add R900 4.7K_OP	29	Reserved for AC fast plug in/out fail issue	From DC1 recommend
RA2: M03	Add R904/R906 10K, R902/R903//R905/R907/R908R909 10K_OP Mount R339 10K	15	Solving LED flash when main power insert first For RAID LED pull high	
RA2: M04	Mounting D29 and deleted JP12 ; TL594.9 tried to GND	14 & 31	D29_OP made leakage ; mistake net.	
RA2: M05	C50 remove close to IC ; R106 pull high form 3.3V change to APA_5V U21 package from LQP48/QFN change to QFN48	33 & 34	Solving POP noise Manufactory requisition	
RA2: M06	Mounting R356/R357 4.7K	21	Implement WLAN and Buleetooth coexistence function	
RA2: M07	R9 from 24.9R 1 change to 56R R57 from 0R change to 0R_OP and add R910 0R DMI_ZCOMP pull high power from +1.5V change to VCCA3GP R535/R564/R566/R90/R89/R550/R126/R533/R98/R534 from 0R change to 10K R672 changed form 1K 1 to 392K 1	05 17 09	Intel recommend	
RA2: M08	Mounting C320 820uF/2.5V and delete C319 220uF/6.3V C388 from 220uF/6.3V SMT change 820uF/2.5V_DIP R785 from 43.2K_1 change to 51.1K_1	28	Manufactory requisition (don't co-lay) and cost saving Cost saving Increasing +1.05VS to +1.1VS, prevent voltage drop on the end	
RA2: M09	Add D50-D51 UDZ3V3/0.2W_OP	15	Reserved for FPC cable shift and made EOS issue	
RA2: M10	Add R911 0R_0603_OP	23	Reserved for RTL8101E	
RA2: M11	CN16.11 power from +5VS cahnge to +5V and add pin12 to +5VS	25	LPC is used to normal 5V power plane	
RA2: M12	R731 mount 0R	27	Correcting schematic (VRHOT# is OD INPUT)	
RA2: M13	C153/C145 from 3900pF 0603 change to 0402 R629 from 24.9R 1 change to 18R_1 Add C1000 0.0uF/25v R607 mount 0R	16 22 19	For share the same component on BOM Increasing SATA driving stream to meet eye pattern measure For SATA current return path For SATA spec requirement	
RA2: M14	EC GPJ4 from SMP1_EN#(SB_RTCRST) change to TV_ON EC GP68 change to FAN_SPD#(SB_RTCRST) SMP1_EN# from EC GPJ4 changr to ICH_GPIO2	21 & 25 19 & 25	Add TV ON function	
RA2: M15	CN17 from Vertial change to right angle (88267-0300)	22	Reserved for support VGA type III	
RA2: M16	C61 100uF_DIP change 4.7uF/6.3V_0805	33	Solving POP noise	
RA2: M17	Add B200-B203 0R_0603_OP	13	Reseved for EMI	

*Note: After item of RA2: M18, please seem appendix A

Uniwill International Corp.				
Title	Appendix A. Ver.AtoA1 History			
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*** Rev.B to B1 whcih was changed Codec from ADI1986A to ALC883 ***

RB1 modify list:				
Symbol	What change	Page	Why change	Note
RB1: M01	Add R553 20K 1 ; HP R/L SWAP ; R157/R581 0R->75R Net: SR_OUT_R/L changed channel from sidesurround to surround	33 & 34	The codec's sense resistor miss ; tried wrong net ; AP measure Following up L50II0 pin definition	
RB1: M02	Add JP30 co-lay with Q45 and take out Q45	28 & 30	Power on sequence to simplify and improved MOS Rds(ON) lose and cost saving.	EC change "+1.05VS_ON" sequence to follow "+1.8V_ON"
RB1: M03	Mount U26 APL5331, C208/C297/C233 1uF_0603, R209 100K_1, R213 120K_1, C799 4.7uF_0805 and R222 0R/ R205 100K take out and mount R201 0R Add C1200/C1201 10uF_1206_OP and C1202 0.1uF_OP and B251 0R_0603 and C194 cahnge net form VDDX to VDDA_1.8V	32	Solving PCIe unstable and auto reset issue Resversed for improve power ripple and platform reset nose and Vendor recomend improved for IC's power	
RB1: M04	Add C1203/C1204 0.1uF, C1205/C1206/C1207/C1208 0.1uF_OP			
RB1: M05	Swap net: PWRSW, LID#, FAN_SPD# and update project ID table	25	For support wake up function and sort PCBA REV.B or REV.C	
RB1: M06	R902 mount 10K and add C1209 0.1uF_OP	15	Solving suspend LED flash when first plug-in power and resversed ESD issue	
RB1: M07	Take out CN32	21	FP CONN take out	
RB1: M08	C827 package change form 0805 to 0603 R734 change form 4.5K to 36.1K_1; R744 change form 4.75K to 6.89K_1	27	0.22u/X7R 25V 603 package is public C827 package change form 0805 to 0603	
RB1: M09	Add C1201 0.1uF_0603_OP	14	Resversed for EMI	
RB1: M10	C926 change form 0.1uF_OP to 1uF_0603	31	Improved for BAT_I signal	
RB1: M11	Add C1211-C1214	22	EMI required	
RB1: M12	C325, C301, C324, C302, C331, C305 mount 0.1 u C648, C653, C652, C613, C27 mount 680p, 860, 878 mount 0R R16 QT1008R1000 0603 -> 0R_0603, R627 0R->QT1008R1000_0603 Add C1216/C1217 0.1uF	15 34 20 15	EMI required (EMI memo 2.2) EMI required (EMI memo 3.3)	
RB1: M13	RT2 roatae 180 degree(library modify)	23	Improvement 10/100 LAN signal	
RB1: M14	Add Q200-Q202 2N7002, R1000-R1002 100K, R1003/R1004 20K_1, C1215 0.1uF_OP, B252 0R_0603 and add net: CODEC_GPID0	33 & 34	Realtek recommend circuit	
RB1: M15	L13/L14 change layout footprint and delete R429/R430 0R_OP	20 & 21	Improvement SMT	
RB1: M16	R92/R93 0R-> 10K , Add R1005/R1006 1K	33	Improvement MIC quality	
RB1: M17	R258 1K->0P, R242 1K->0P, R249 1K->0P, R253 mount 1K	25	For support wake up function and sort PCBA REV.B or REV.C	