

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM, MLB, J45

DVT 8/6/2013

Page	Contents	Sync	Date
1	Table of Contents	MASTER	
2	BOM Configuration	J15_MLB	10/25/2012
3	BOM Configuration	J15_MLB	10/31/2012
4	PD Parts	J15_MLB	10/31/2012
5	CPU DMI/PEG/FDI/RSVD	J15_REFERENCE	12/18/2012
6	CPU Clock/Misc/JTAG/CFG	J15_REFERENCE	12/18/2012
7	CPU DDR3 Interfaces	J15_REFERENCE	12/18/2012
8	CPU Power	J15_REFERENCE	12/18/2012
9	CPU Ground	J15_REFERENCE	12/18/2012
10	CPU Decoupling	J15_REFERENCE	12/18/2012
11	PCH RTC/HDA/JTAG/SATA/CLK	J15_REFERENCE	12/18/2012
12	PCH DMI/FDI/PM/GFX/PCI	J15_REFERENCE	12/18/2012
13	PCH PCI-E/USB	J15_REFERENCE	12/18/2012
14	PCH GPIO/MISC/NCTF	J15_REFERENCE	12/18/2012
15	PCH Power	J15_REFERENCE	12/18/2012
16	PCH Grounds	J15_REFERENCE	12/18/2012
17	PCH DECOUPLING	J15_REFERENCE	12/18/2012
18	CPU & PCH XDP	J15_MLB	10/31/2012
19	Chipset Support	J15_REFERENCE	12/18/2012
20	Project Chipset Support	J15_REFERENCE	01/14/2013
21	CPU Memory S3 Support	J15_REFERENCE	12/18/2012
22	DDR3 VREF MARGINING	J15_MLB	10/31/2012
23	DDR3 SDRAM Bank A (1 OF 2)	J15_MLB	10/31/2012
24	DDR3 SDRAM Bank A (2 OF 2)	J15_MLB	10/31/2012
25	DDR3 SDRAM Bank B (1 OF 2)	J15_MLB	10/31/2012
26	DDR3 SDRAM Bank B (2 OF 2)	J15_MLB	10/31/2012
27	DDR3 Termination	J15_MLB	10/31/2012
28	Thunderbolt Host (1 of 2)	T29_RR	01/14/2013
29	Thunderbolt Host (2 of 2)	T29_RR	01/14/2013
30	Thunderbolt Mobile Support	T29_RR	01/14/2013
31	Thunderbolt Connector A	J15_REFERENCE	12/18/2012
32	Thunderbolt Connector B	J15_REFERENCE	12/18/2012
33	DDC Crossbar	J15_REFERENCE	11/16/2012
34	X29C CONNECTOR	J15_MLB	10/31/2012
35	SSD Connector	CLEAN_MLB_KEPLER	06/08/2013
36	Camera 1 of 2	CLEAN_MLB_KEPLER	06/13/2013
37	Camera 2 of 2	CLEAN_MLB_KEPLER	06/13/2013
38	USB 3.0 CONNECTORS	J15_MLB	10/31/2012
39	KEYBOARD/TRACKPAD (1 OF 2)	CHANG_J45	03/15/2013
40	KEYBOARD/TRACKPAD (2 OF 2)	CHANG_J45	03/15/2013
41	SMC	CHANG_J45	03/15/2013

Page	Contents	Sync	Date
42	SMC Shared Support	CHANG_345	11/12/2012
43	SMC Project Support	CHANG_345	03/15/2013
44	SMBus Connections	CHANG_345	11/26/2012
45	High Side Voltage and Current Sensing	CHANG_345	12/21/2012
46	Load Side Voltage and Current Sensing	CHANG_345	03/15/2013
47	Debug Sensors	CHANG_345	12/21/2012
48	Thermal Sensors	CHANG_345	11/26/2012
49	Fan Connectors	J15_MLB	10/31/2012
50	SPI ROM / LPC+SPI Conn.	J15_MLB	10/31/2012
51	AUDIO:CODEC, ANALOG	JOE_345	07/30/2013
52	AUDIO:CODEC, DIGITAL	JOE_345	07/30/2013
53	AUDIO: SPEAKER AMP	JOE_345	07/30/2013
54	AUDIO: JACK	JOE_345	07/30/2013
55	AUDIO: JACK TRANSLATORS	JOE_345	07/30/2013
56	DC-In & Battery Connectors	J15_MLB	10/31/2012
57	PBus Supply & Battery Charger	J15_MLB	10/31/2012
58	CPU VR12.5 VCC Regulator IC	J15_MLB	10/31/2012
59	CPU VR12.5 VCC Power Stage	J15_MLB	10/31/2012
60	1.35V DDR3L SUPPLY	J15_MLB	10/31/2012
61	5V / 3.3V Power Supply	J15_MLB	10/31/2012
62	1V05V POWER SUPPLY	J15_MLB	10/31/2012
63	LCD/KBD Backlight Driver	CLEAN_MLB_KEPLER	06/13/2013
64	Misc Power Supplies	J15_MLB	10/31/2012
65	Power FETS	J15_MLB	10/31/2012
66	Power Control 1/ENABLE	CHANG_345	03/15/2013
67	eDP Display Connector	J15_MLB	10/31/2012
68	RIO Connectors	J15_MLB	10/31/2012
69	Power Aliases	J15_MLB	10/31/2012
70	Signal Aliases	J15_MLB	10/31/2012
71	Functional Test Points	J15_MLB	10/31/2012
72	NC & No Test	J15_MLB	10/31/2012
73	PCB Rule Definitions	SIDLE_345	12/10/2012
74	CPU Constraints	SIDLE_345	12/10/2012
75	PCH Constraints 1	SIDLE_345	12/10/2012
76	PCH Constraints 2	SIDLE_345	12/10/2012
77	Memory Constraints	SIDLE_345	12/10/2012
78	Thunderbolt Constraints	SIDLE_345	12/10/2012
79	Camera Constraints	SIDLE_345	12/10/2012
80	SMC Constraints	SIDLE_345	12/10/2012
81	Project Specific Constraints	SIDLE_345	12/10/2012

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM, MLB, J45	SCH	CRITICAL	
820-3662	1	PCBF, MLB, J45	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED= Tue Aug 6 17:09:28 2013

DRAWING TITLE			
<PART_DESCRIPTION>			
	Apple Inc.		DRAWING NUMBER <SCH_NUM>
			SIZE D
			REVISION <E4LABEL>
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		BRANCH <BRANCH>	PAGE 1 OF 118
		SHEET 1 OF 81	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB, J45	J45_COMMON
985-0045	DEV BOM,MLB, J45	J45_DEVEL :ENG
639-4822	PCBA,MLB,BETTER,8G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BETTER, RAM: MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: BEST, RAM: MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC, J45	BASE_BOM,DEVEL_BOM,CPU_CRW: CTO, RAM: MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE, COMMON, J45_COMMON1, J45_COMMON2, J45_PROGPARTS
J45_COMMON1	CPUMEM:S0, TBTHV:P15V, SKIP_5V3V3:AUDIBLE, CHGR_5V:L00, CPUPEG:X16, S2_PWR:S0
J45_COMMON2	EDP:YES, LPCPLUS_CONN:YES, LPCPLUS_R:YES, XDP_PWR:1V5, SPI:DUAL_IO, SSD_PWR_EN:GPIO, CAM_WAKE:NO
J45_PVB	BKLT:PROD, SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT, BOOTROM_PROG:DVT, TBTRM:PROG, TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE, XDP_DEBUG, S0PGOOD_ISL, DDRVREF_DAC, SENSOR_NONPROD:Y, SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE, XDP_DEBUG, BKLT:PROD, SENSOR_NONPROD:N, SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN, XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW, SR13J, PRQ, C0, 2, 6, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: BETTER
337S4600	1	CRW, SR18B, PRQ, C0, 2, 3, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: BEST
337S4624	1	CRW, SR18S, PRQ, C0, 2, 6, 47W, 4+3E, 6M, BGA	U0500	CRITICAL	CPU_CRW: CTO
337S4542	1	IC, QEWV, LPT-M, HM87, C2, SR199, PRQ, FCBGA	U1100	CRITICAL	
338S1247	1	IC, TBT, FR-4C, AB, PRQ, C10, SR13C, FCBGA288	U2800	CRITICAL	
338S1186	1	IC, BCM15700A2, S2 PCIE CMRA, BXB, 288FCBGA	U3900	CRITICAL	
333S0700	1	IC, SDRAM, 4GBIT, DDR3L-1600, GEMMA, 96B FBGA	U4000	CRITICAL	
333S0667	16	IC, SDRAM, 4GBIT, DDR3L-1600, HUMA, 78P FBGA	_____	CRITICAL	HYNIX_1600_S
333S0624	16	IC, SDRAM, DDR3-1600, 512MX8, 78FBGA, C-DIE, SAMSUNG	_____	CRITICAL	SAMSUNG_1600_S
333S0703	16	IC, SDRAM, 4GBIT, DDR3L-1600, F DIE, RS, 78P	_____	CRITICAL	ELPIDA_1600_S
333S0660	16	IC, SDRAM, 4GBIT, DDR3L-1600, VB8A, 78P, FBGA	_____	CRITICAL	MICRON_1600_S
333S0667	32	IC, SDRAM, 4GBIT, DDR3L-1600, HUMA, 78P FBGA	_____	CRITICAL	HYNIX_1600
333S0624	32	IC, SDRAM, DDR3-1600, 512MX8, 78FBGA, C-DIE, SAMSUNG	_____	CRITICAL	SAMSUNG_1600
333S0703	32	IC, SDRAM, 4GBIT, DDR3L-1600, F DIE, RS, 78P	_____	CRITICAL	ELPIDA_1600
333S0660	32	IC, SDRAM, 4GBIT, DDR3L-1600, VB8A, 78P, FBGA	_____	CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM:MICRON_1600	MICRON_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNCH MASTER=J15 MLB		SYNCH DATE=10/25/2012	
PAGE TITLE			
BOM Configuration			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
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		REVISION <E4LABEL>	
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		PAGE 2 OF 118	
		SHEET 2 OF 81	

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	ODS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TTF
376S1031	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NOX alt to Diodes
376S1089	376S1128		ALL	NOX alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elipide F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohe alt to Vishay
138S0732	138S0715		ALL	Rohe alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4690
311S0649	311S0541		ALL	ON alt to Toshiba (U2036, U7001)

Programmables - All builds

335S0915	1	IC, SERIAL SPI FLASH ROM, 4MBIT, 50MHZ, US0N	U2890	CRITICAL	TBTROM: BLANK
341S3919	1	IC, EPROM, Falcon RIDGE(V13.9) J44/45	U2890	CRITICAL	TBTROM: PROG
337S4587	1	IC, TP PSOC, QFN, BLANK	U4801	CRITICAL	TPAD_PSOC: BLANK
341S3856	1	IC, TRKPD/KYBD, PSOC(V225)	U4801	CRITICAL	TPAD_PSOC: PROG

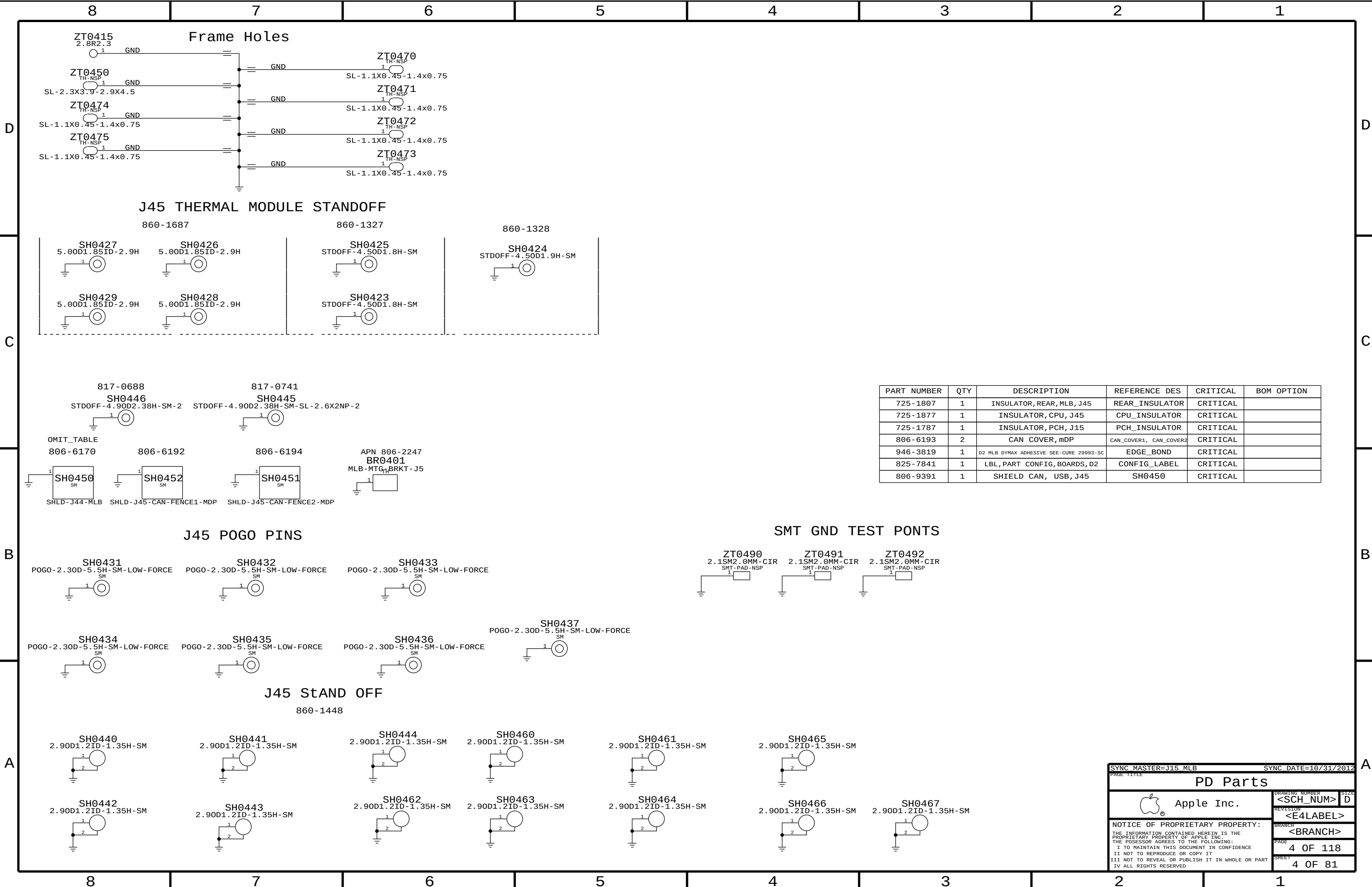
SMC

338S1214	1	IC, SMC-B1, 46MHZ/500MIPS, SCPL FW, 157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC, SMC-B1, EXT, V2.12A54, EVT, 345	U5000	CRITICAL	SMC_PROG: EVT
341S3741	1	IC, SMC-A3, SCPL, EXT, VXXXX, PVT, J15	U5000	CRITICAL	SMC_PROG: PVT

EFI ROM

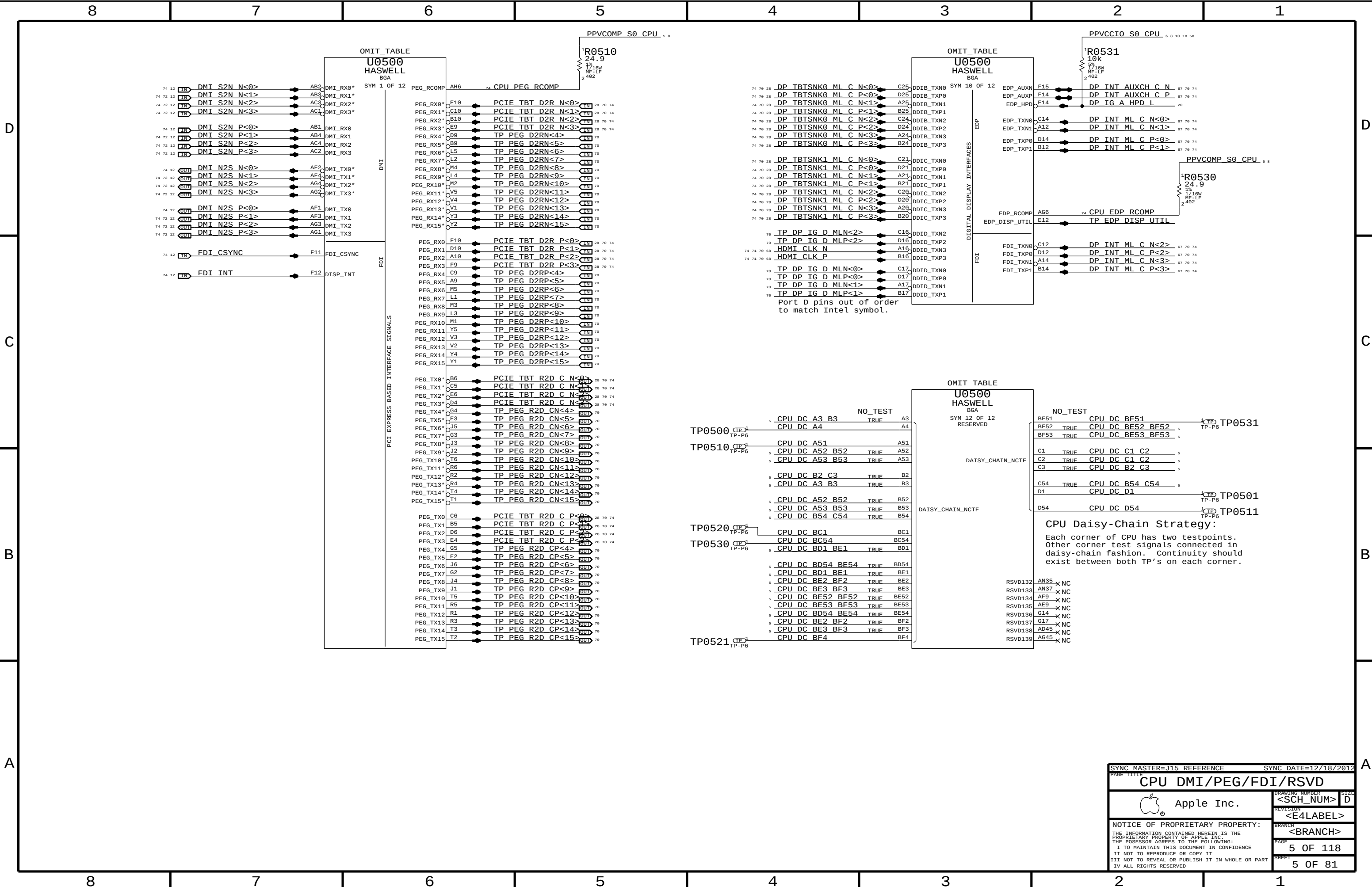
335S0807	1	IC, SPI SRL 50MHZ FLASH, 64MBIT, 850P, FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC, SPI SRL 50MHZ, FLASH, 64MBIT, 501C8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC, EFI ROM(VXXXX)PROTO 0, J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC, EFI ROM(V0035)PRE-PROTO 1, J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC, EFI ROM(V0041)PROTO 1, J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC, EFI ROM(V00xx)PROTO 2, J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC, EFI ROM(V0100)PROTO3- J45 &EVT- J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC, EFI ROM(Vxxxxx)DVT- J45	U6100	CRITICAL	BOOTROM_PROG:DVT

SYNC MASTER=J15 MLB	SYNC DATE=10/31/2012																				
PAGE TITLE																					
BOM Configuration																					
 Apple Inc.	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; padding: 5px;">DRAWING NUMBER</td> <td style="width: 50%; padding: 5px;">SIZE</td> </tr> <tr> <td style="padding: 5px;"><SCH_NUM></td> <td style="padding: 5px;">D</td> </tr> <tr> <td colspan="2" style="padding: 5px;">REVISION</td> </tr> <tr> <td colspan="2" style="padding: 5px;"><E4LABEL></td> </tr> <tr> <td colspan="2" style="padding: 5px;">BRANCH</td> </tr> <tr> <td colspan="2" style="padding: 5px;"><BRANCH></td> </tr> <tr> <td colspan="2" style="padding: 5px;">PAGE</td> </tr> <tr> <td colspan="2" style="padding: 5px;">3 OF 118</td> </tr> <tr> <td colspan="2" style="padding: 5px;">SHEET</td> </tr> <tr> <td colspan="2" style="padding: 5px;">3 OF 81</td> </tr> </table>	DRAWING NUMBER	SIZE	<SCH_NUM>	D	REVISION		<E4LABEL>		BRANCH		<BRANCH>		PAGE		3 OF 118		SHEET		3 OF 81	
DRAWING NUMBER	SIZE																				
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REVISION																					
<E4LABEL>																					
BRANCH																					
<BRANCH>																					
PAGE																					
3 OF 118																					
SHEET																					
3 OF 81																					
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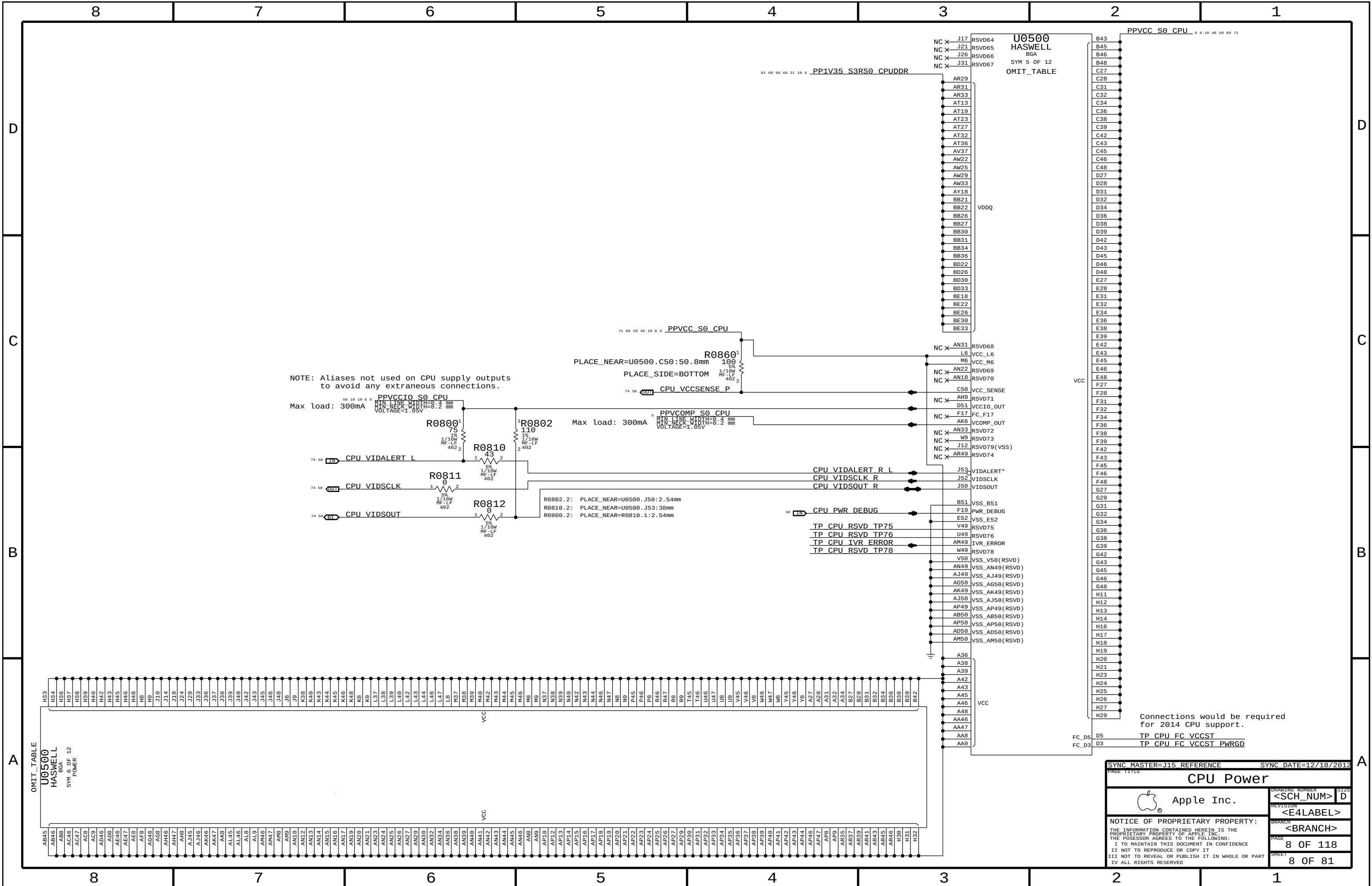


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR, REAR, MLB, J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR, CPU, J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR, PCH, J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER, mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL, PART CONFIG, BOARDS, D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB, J45	SH0450	CRITICAL	

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE		PD Parts	
		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	4 OF 118
		SHEET	4 OF 81







NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

Max load: 300mA
PPVCCIO S0 CPU
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.05V

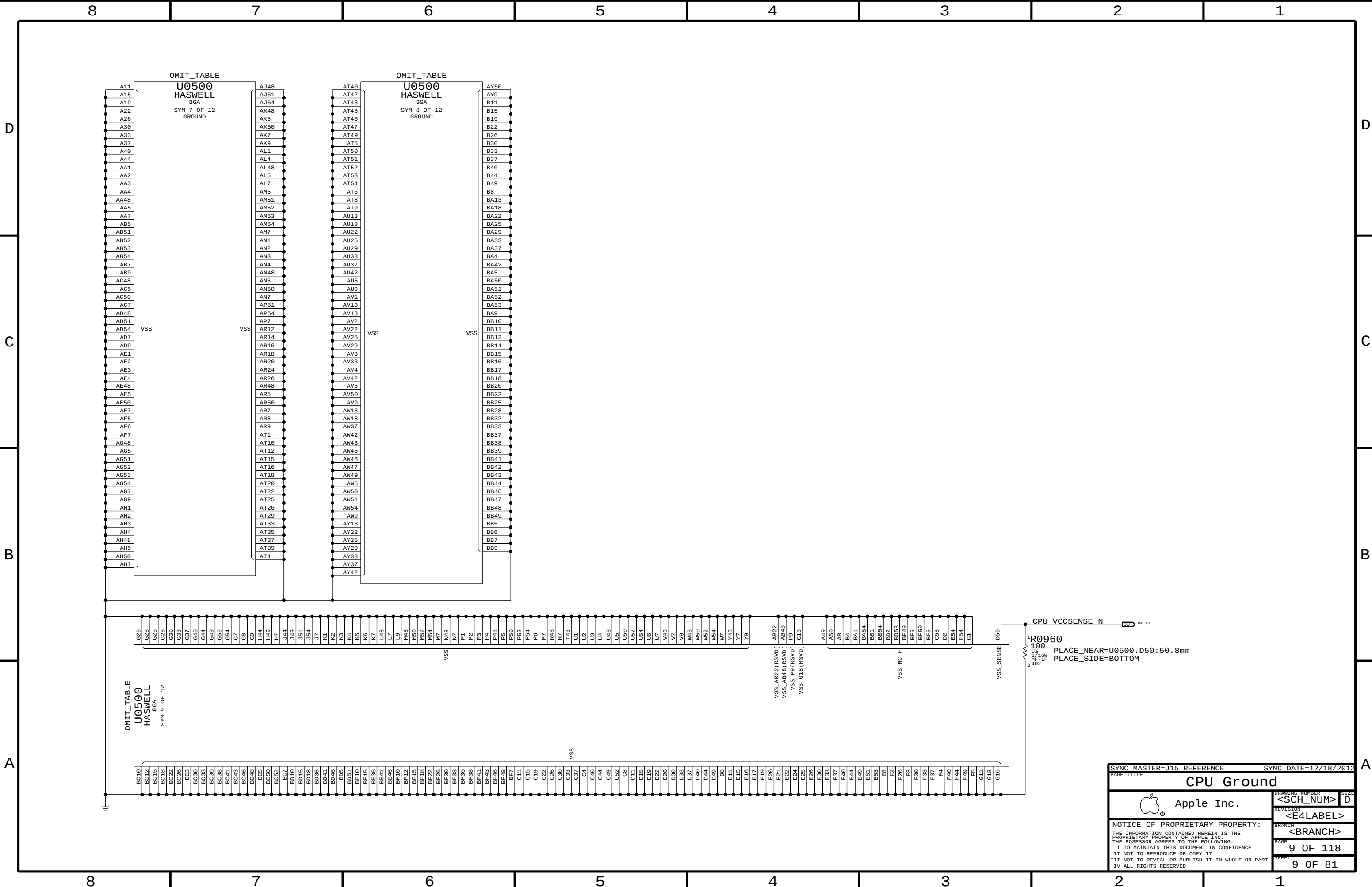
PPVCC S0 CPU
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
CPU VCCSENSE P
PPVCOMP S0 CPU
Max load: 300mA
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.05V

R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

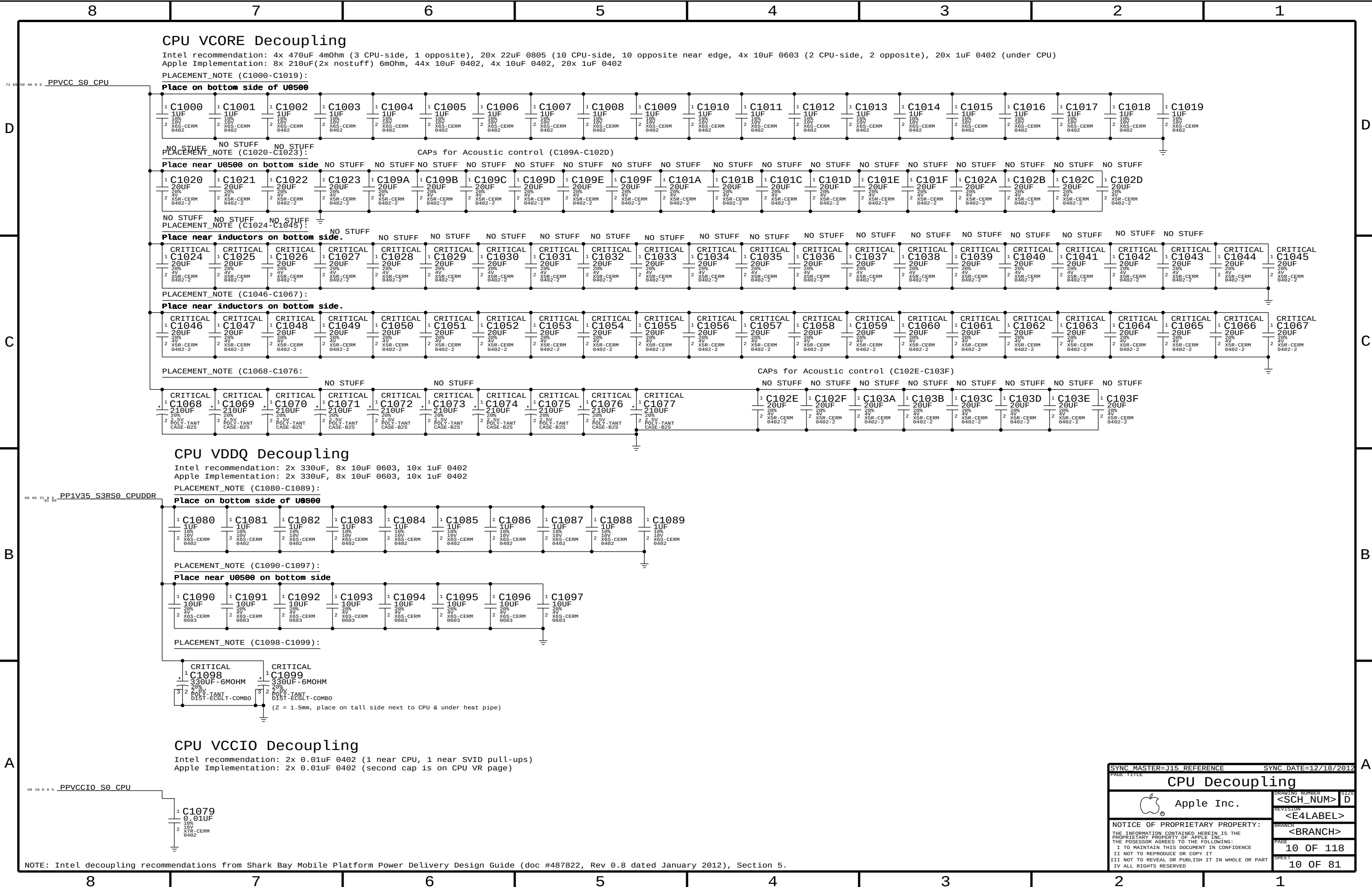
Connections would be required for 2014 CPU support.

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE			
CPU Power			
		Apple Inc.	
DRAWING NUMBER		SIZE	
<SCH_NUM>		D	
REVISION			
<E4LABEL>			
BRANCH			
<BRANCH>			
PAGE		8 OF 118	
SHEET		8 OF 81	

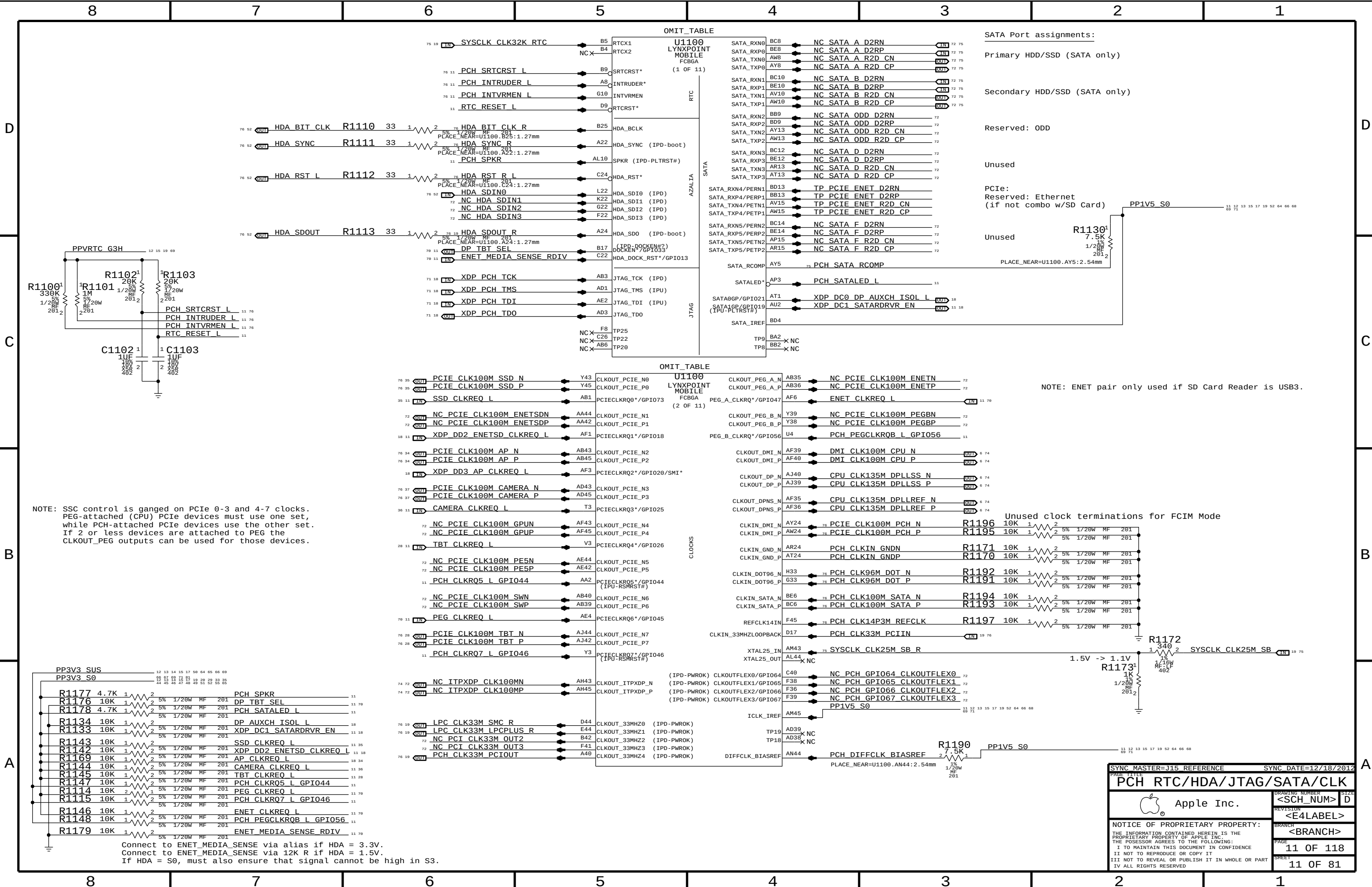
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PAGE TITLE			
CPU Ground			
		DRAWING NUMBER	
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		SIZE	
		D	
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PAGE TITLE			
CPU Decoupling			
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		<BRANCH>	
		PAGE	10 OF 118
		SHEET	10 OF 81



NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks. PEG-attached (CPU) PCIe devices must use one set, while PCH-attached PCIe devices use the other set. If 2 or less devices are attached to PEG the CLKOUT_PEG outputs can be used for those devices.

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCie: Reserved: Ethernet (if not combo w/SD Card)

Unused

PP1V5_S0

R1130¹
7.5K
1/20W MF 201

PLACE_NEAR=U1100.AY5:2.54mm

NOTE: ENET pair only used if SD Card Reader is USB3.

Unused clock terminations for FCIM Mode

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

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SYNC DATE=12/18/2012

PCH RTC/HDA/JTAG/SATA/CLK

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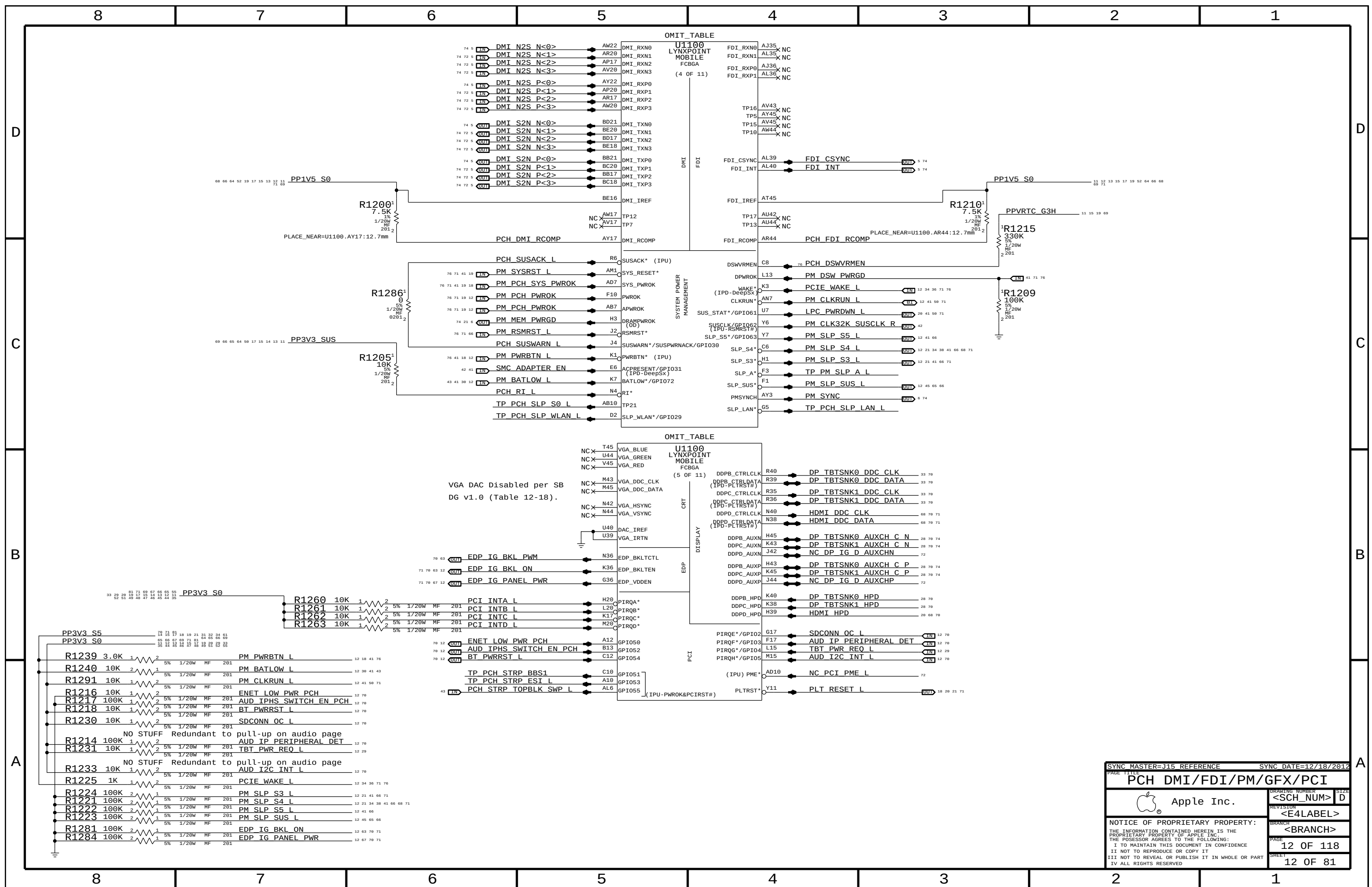
<BRANCH>

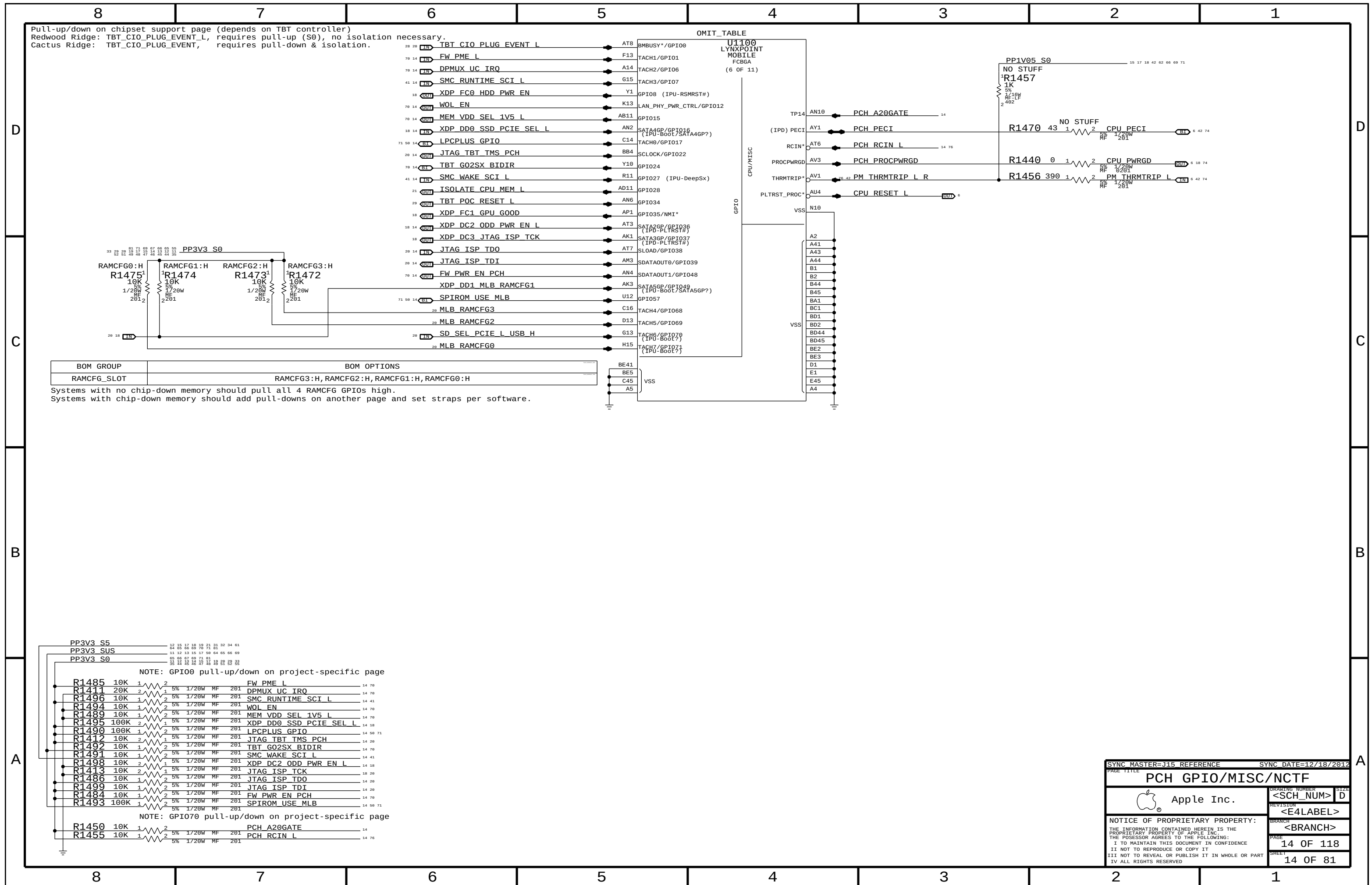
PAGE

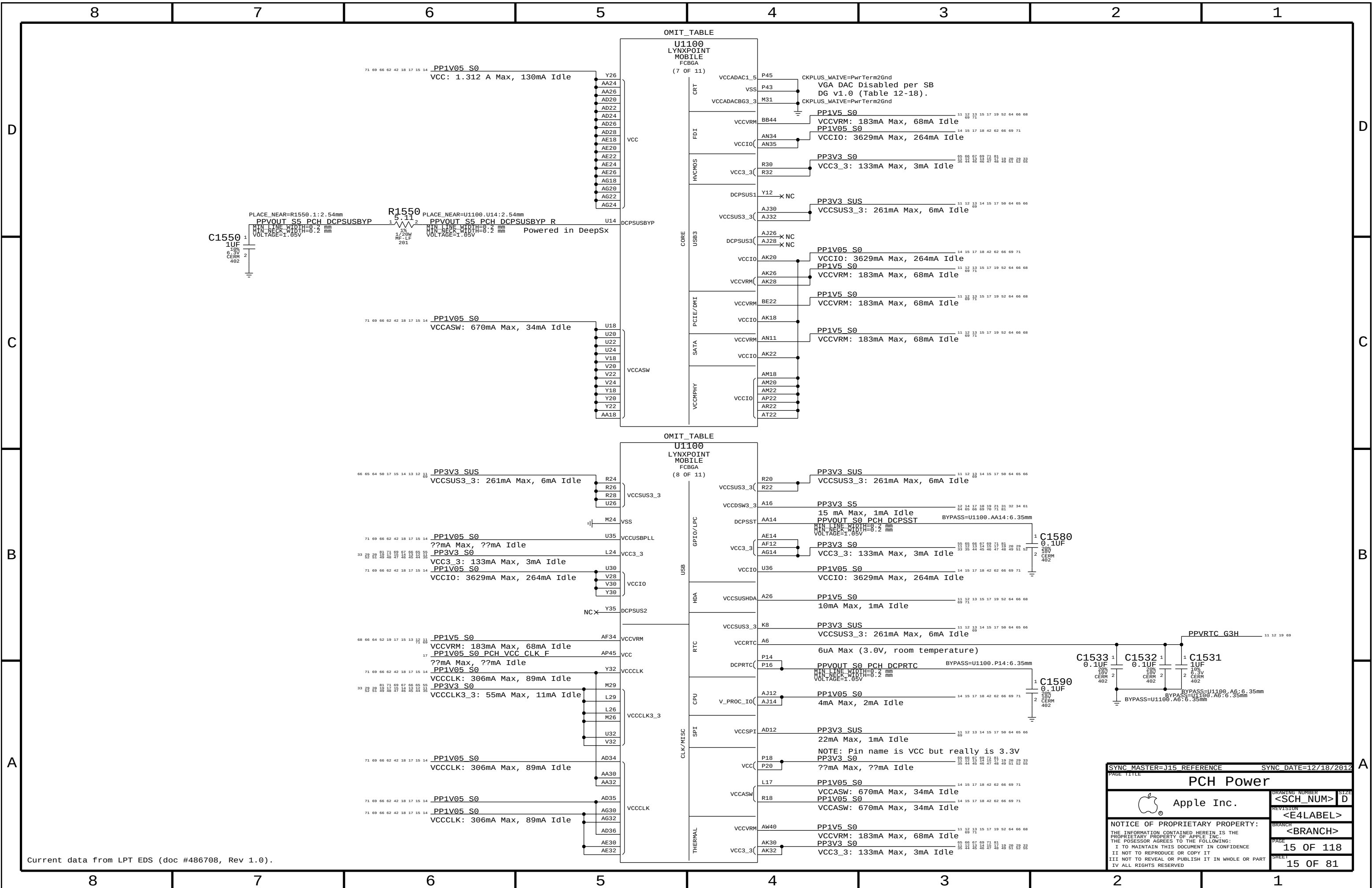
11 OF 118

SHEET

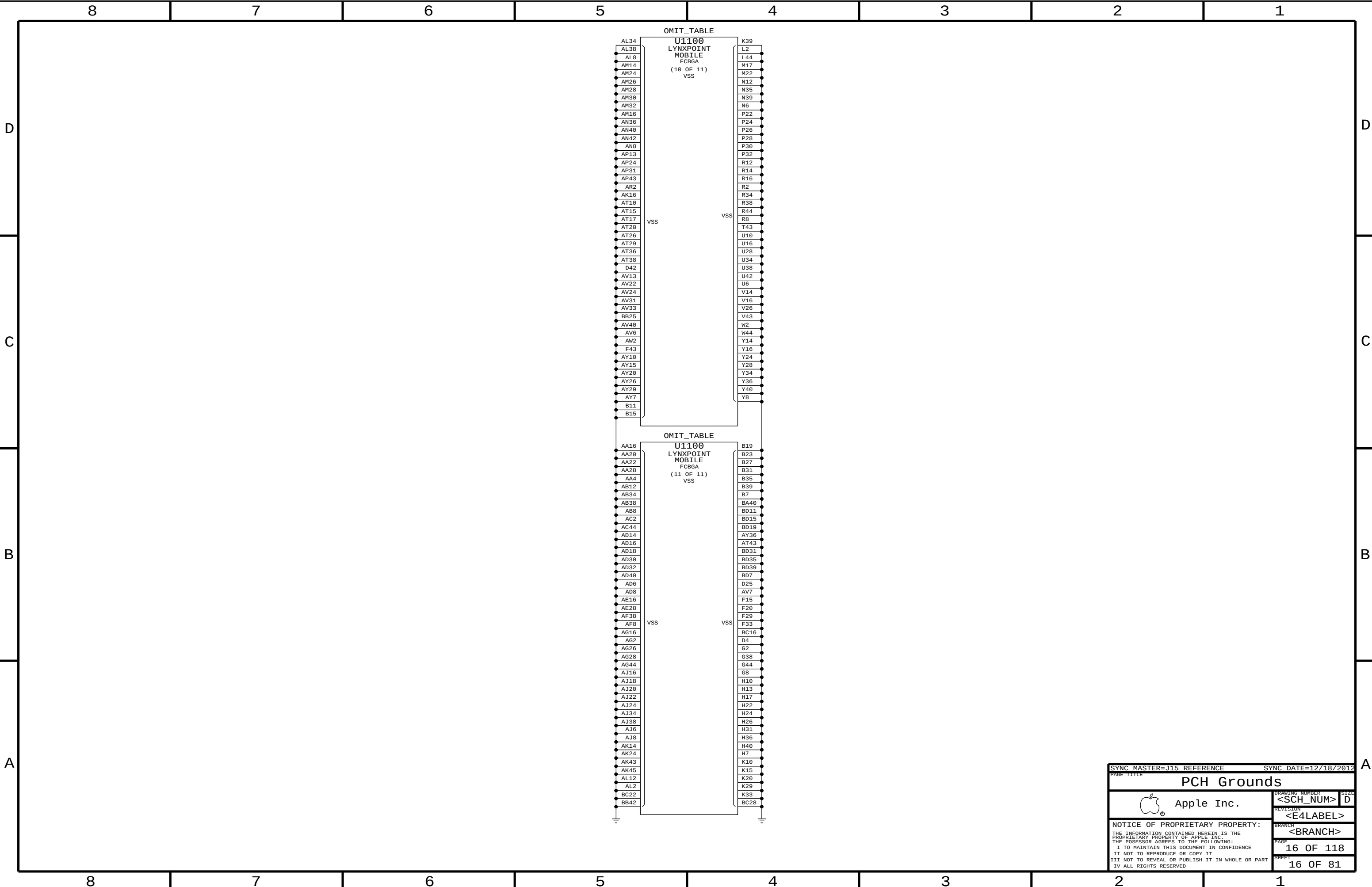
11 OF 81







SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE		PCH Power	
		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		BRANCH	
		<BRANCH>	
		PAGE	15 OF 118
		SHEET	15 OF 81



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PCH Grounds

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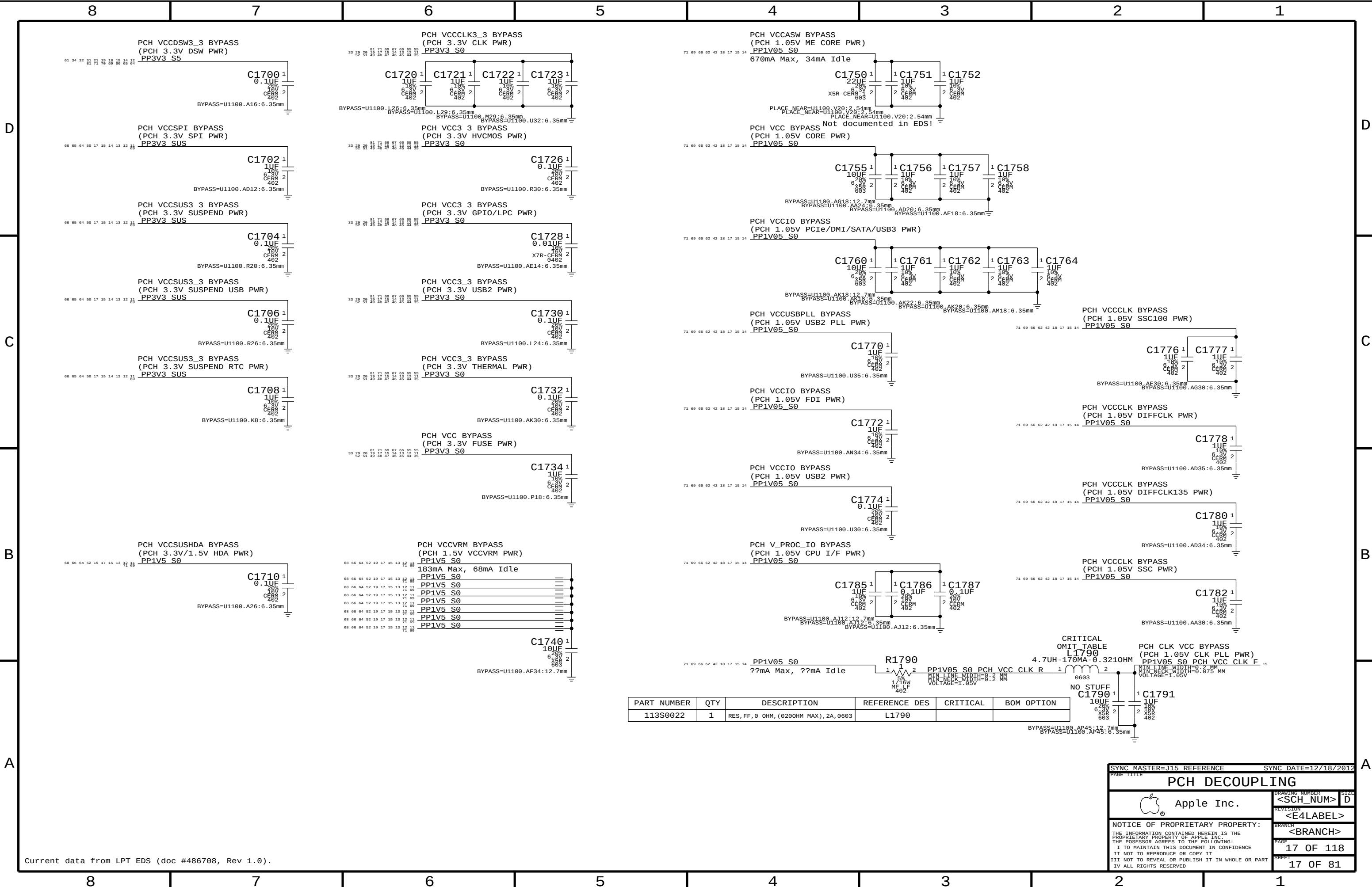
<BRANCH>

PAGE

16 OF 118

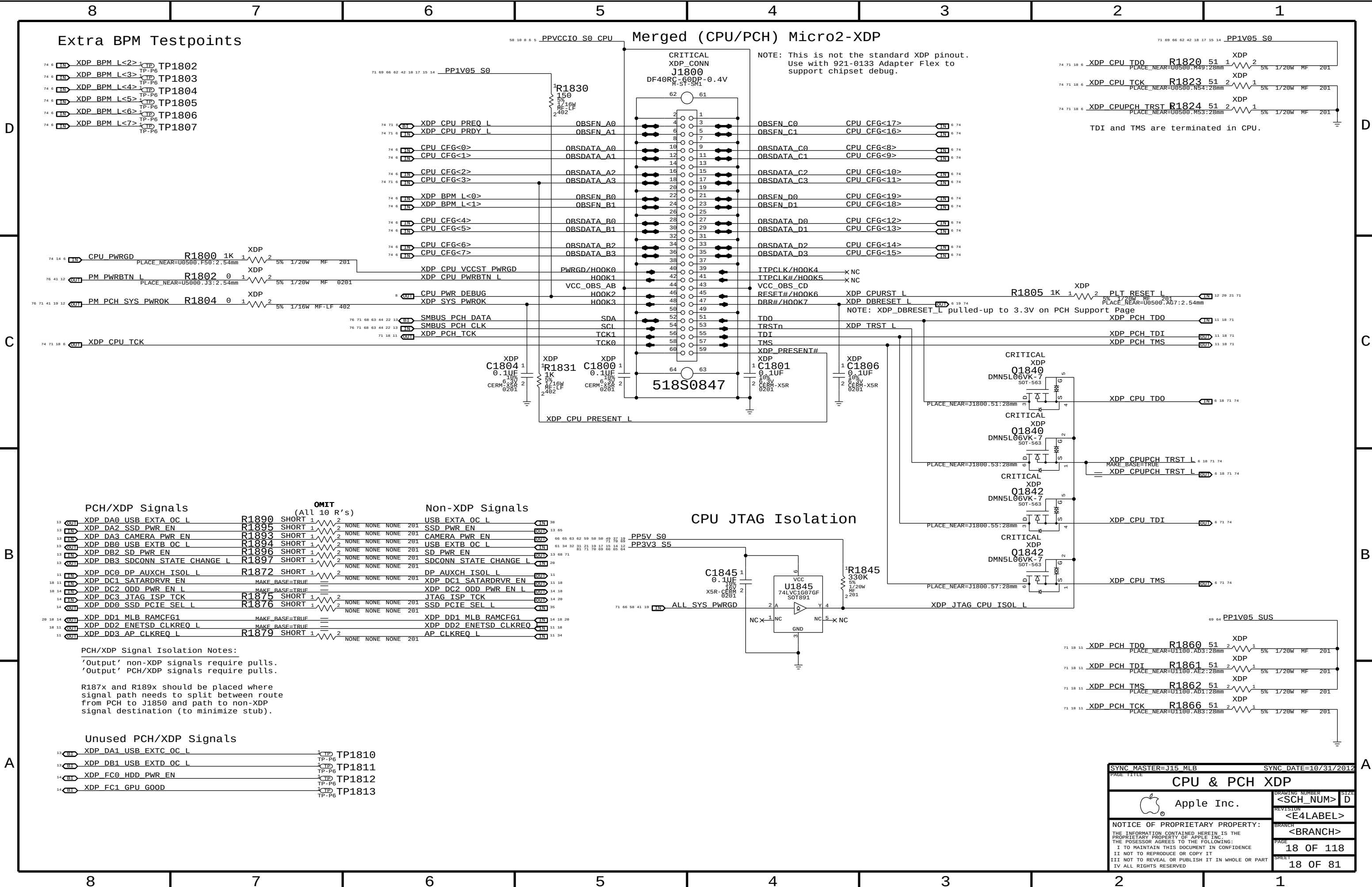
SHEET

16 OF 81



Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
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PCH DECOUPLING			
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PAGE		17 OF 118	
SHEET		17 OF 81	



Extra BPM Testpoints

- XDP BPM L<2> TP1802
- XDP BPM L<3> TP1803
- XDP BPM L<4> TP1804
- XDP BPM L<5> TP1805
- XDP BPM L<6> TP1806
- XDP BPM L<7> TP1807

PCH/XDP Signals

PCH/XDP Signals		Non-XDP Signals	
XDP DA0 USB EXTA OC L	R1890 SHORT 1 2	USB EXTA OC L	TP1808
XDP DA2 SSD PWR EN	R1895 SHORT 1 2	SSD PWR EN	TP1809
XDP DA3 CAMERA PWR EN	R1893 SHORT 1 2	CAMERA PWR EN	TP1810
XDP DB0 USB EXTB OC L	R1894 SHORT 1 2	USB EXTB OC L	TP1811
XDP DB2 SD PWR EN	R1896 SHORT 1 2	SD PWR EN	TP1812
XDP DB3 SDCONN STATE CHANGE L	R1897 SHORT 1 2	SDCONN STATE CHANGE L	TP1813
XDP DC0 DP AUXCH ISOL L	R1872 SHORT 1 2	DP AUXCH ISOL L	TP1814
XDP DC1 SATARDVR EN	MAKE_BASE=TRUE	XDP DC1 SATARDVR EN	TP1815
XDP DC2 ODD PWR EN L	MAKE_BASE=TRUE	XDP DC2 ODD PWR EN L	TP1816
XDP DC3 JTAG ISP TCK	R1875 SHORT 1 2	JTAG ISP TCK	TP1817
XDP DD0 SSD PCIE SEL L	R1876 SHORT 1 2	SSD PCIE SEL L	TP1818
XDP DD1 MLB RAMCFG1	MAKE_BASE=TRUE	XDP DD1 MLB RAMCFG1	TP1819
XDP DD2 ENETSD CLKREQ L	MAKE_BASE=TRUE	XDP DD2 ENETSD CLKREQ L	TP1820
XDP DD3 AP CLKREQ L	R1879 SHORT 1 2	AP CLKREQ L	TP1821

PCH/XDP Signal Isolation Notes:

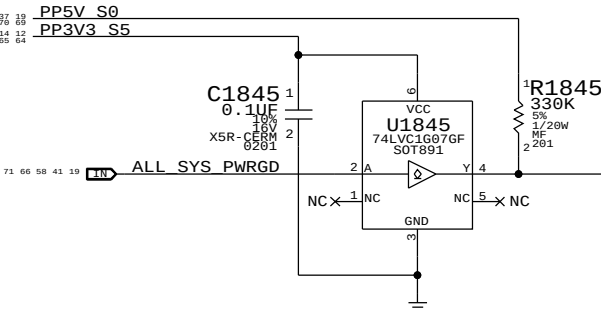
- 'Output' non-XDP signals require pulls.
- 'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1800 and path to non-XDP signal destination (to minimize stub).

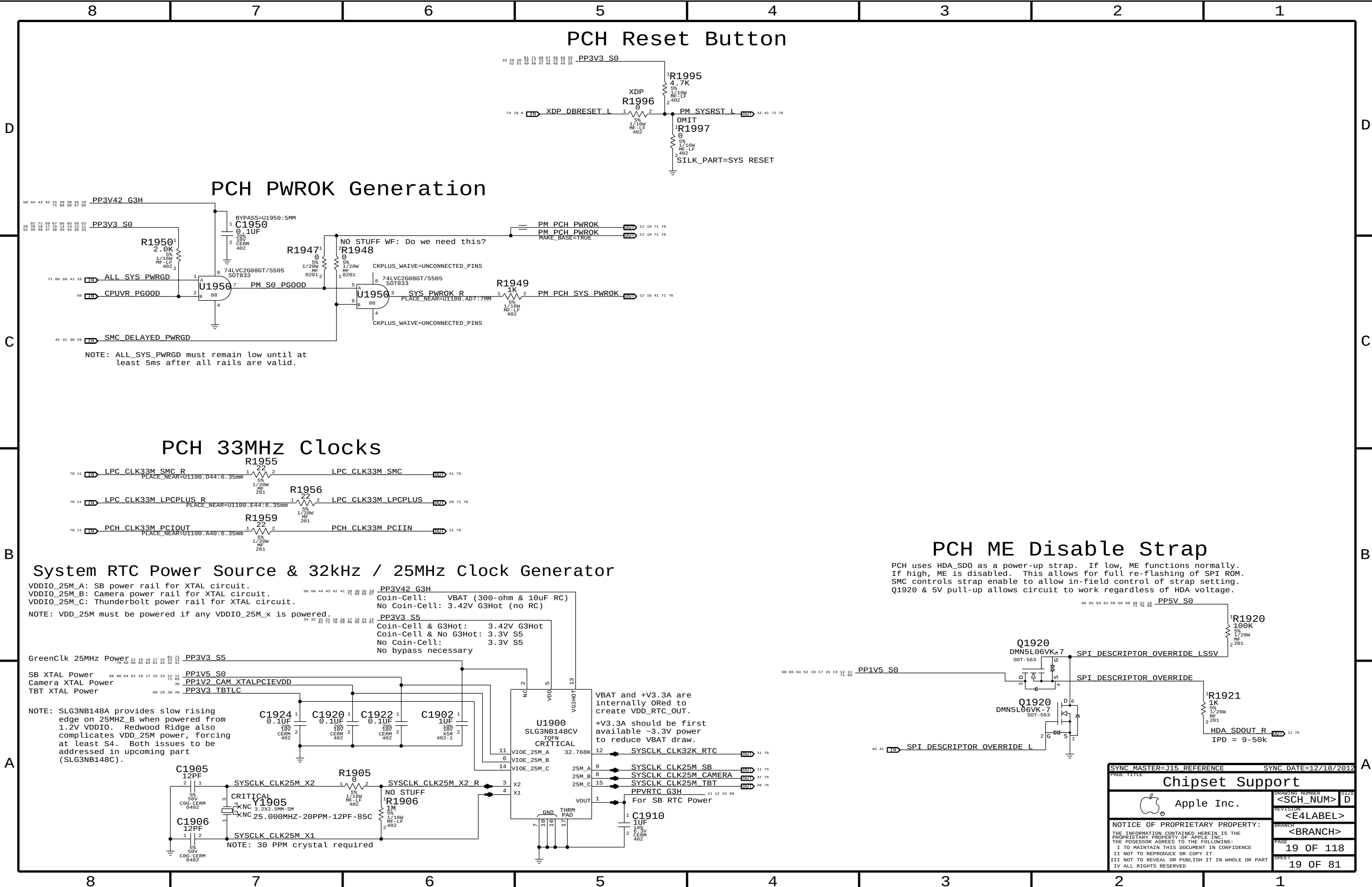
Unused PCH/XDP Signals

- XDP DA1 USB EXTD OC L TP1810
- XDP DB1 USB EXTD OC L TP1811
- XDP FC0 HDD PWR EN TP1812
- XDP FC1 GPU GOOD TP1813

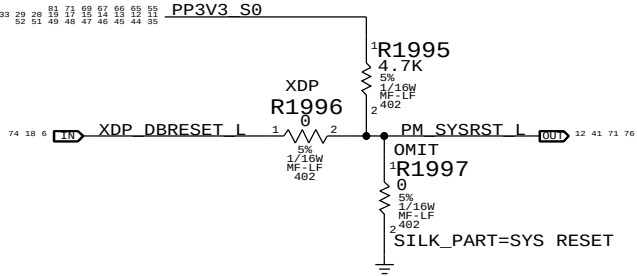
CPU JTAG Isolation



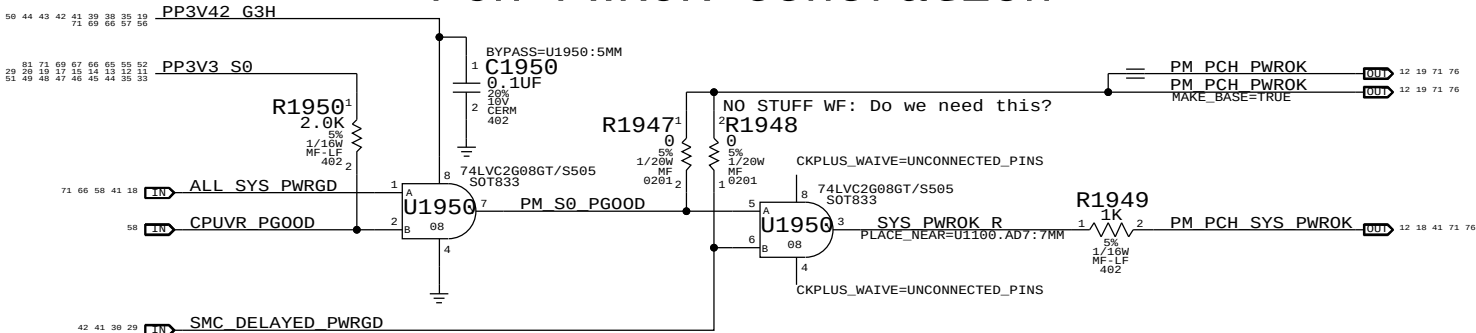
SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
CPU & PCH XDP		DRAWING NUMBER	
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		SHEET	
		18 OF 81	



PCH Reset Button

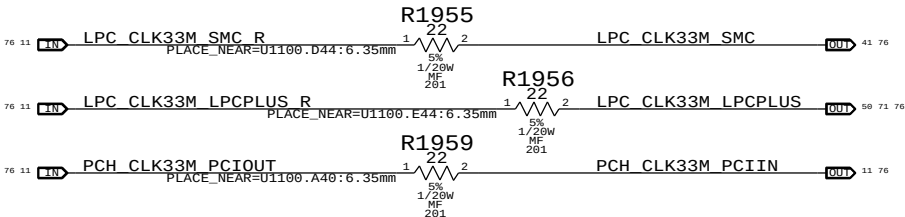


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

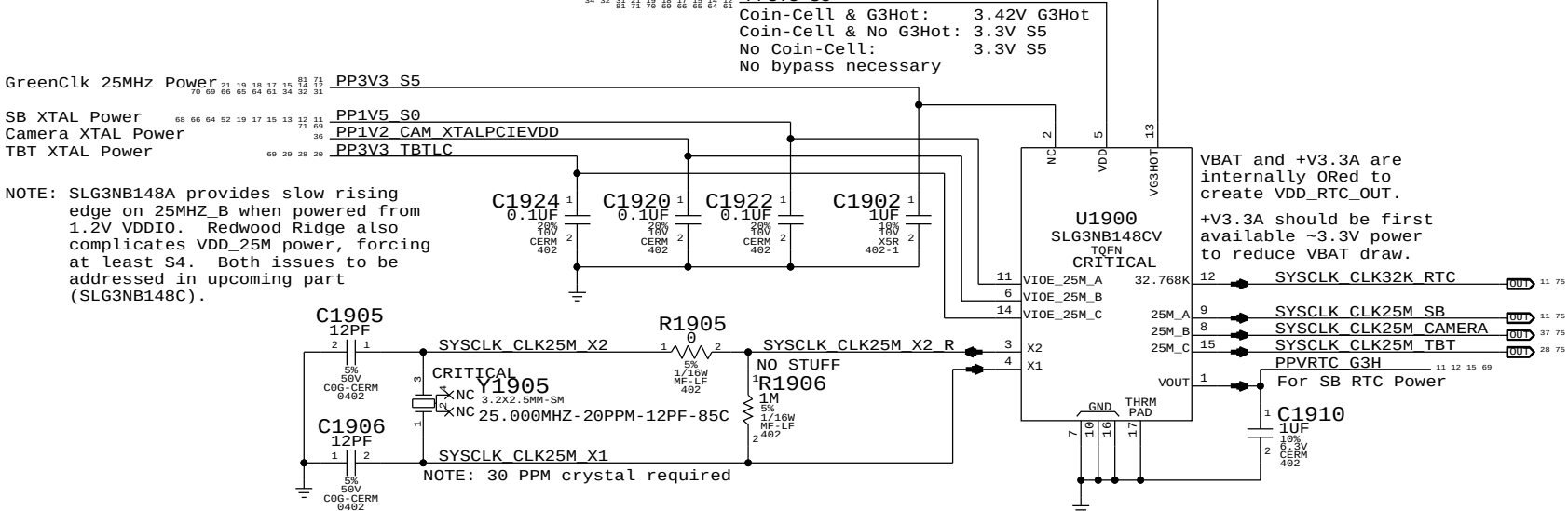
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

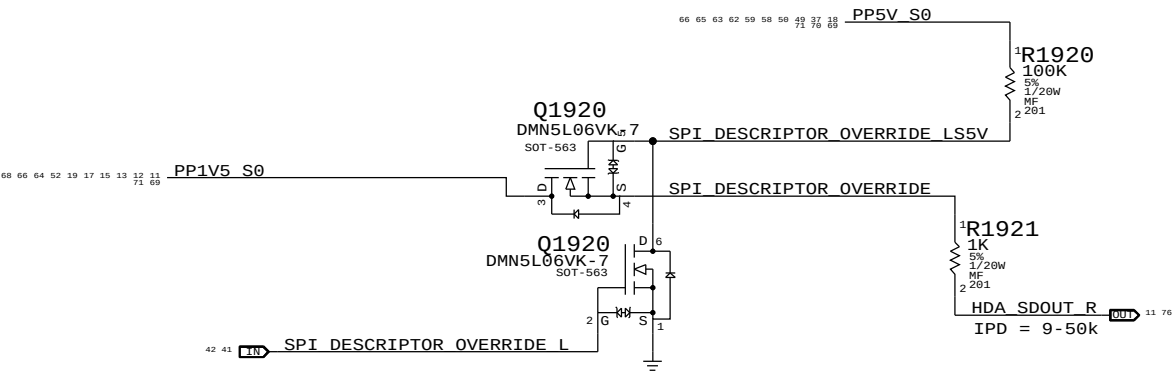
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



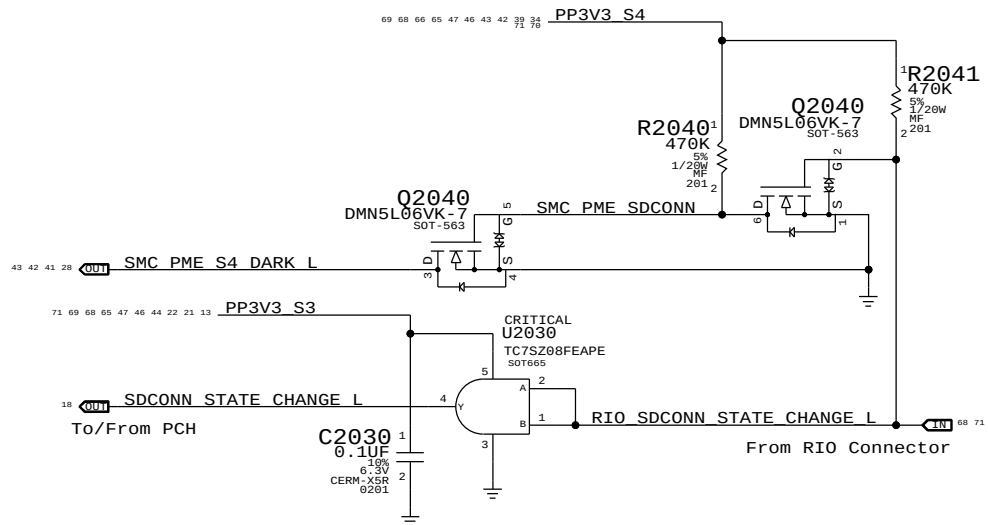
PCH ME Disable Strap

PCH uses HDA_SD0 as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



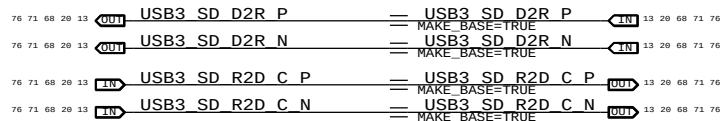
SYNC MASTER=J15 REFERENCE		SYNC DATE=12/18/2012	
PAGE TITLE		Chipset Support	
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		<SCH_NUM>	D
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RIO SD Card Reader Support



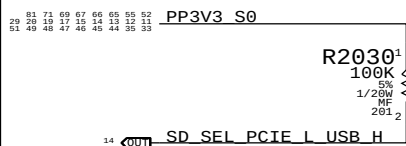
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.

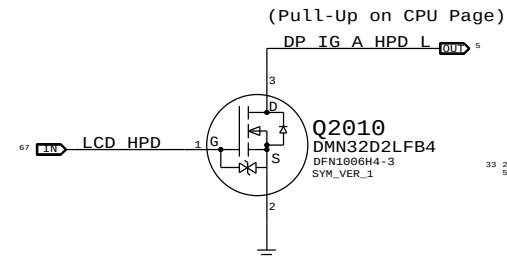


Flexible I/O Configuration Strap

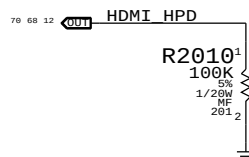
Must pull signal correctly even if always USB or PCIe



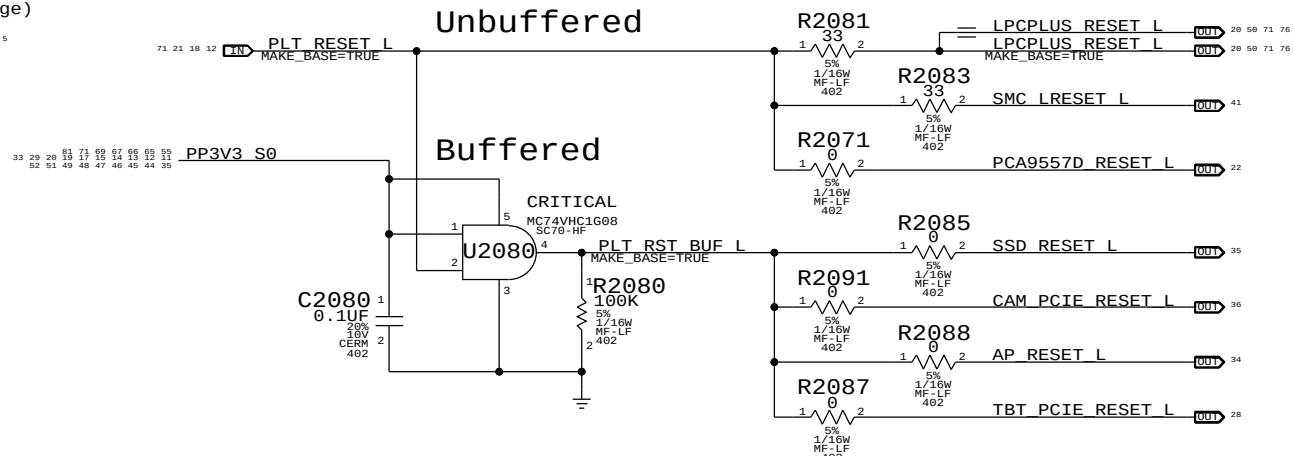
LCD HPD Inverter



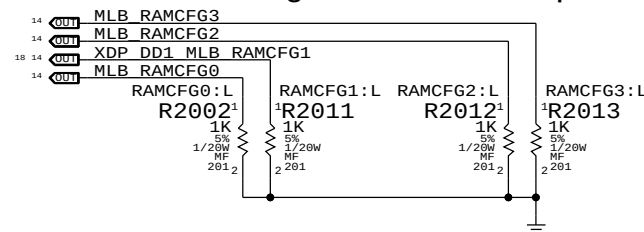
HDMI HPD pull-down



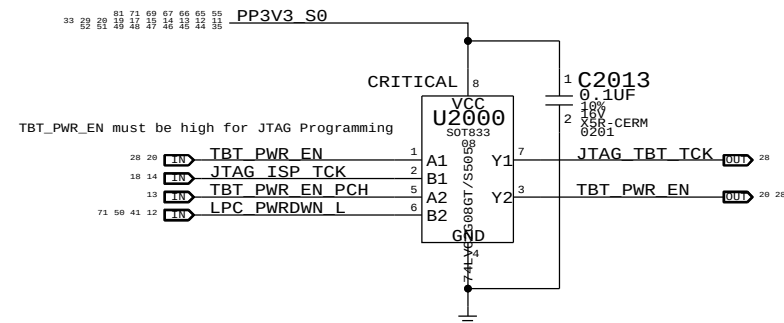
Platform Reset Connections



RAM Configuration Straps

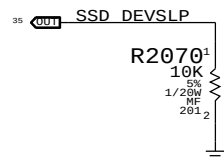


GPIO Glitch Prevention



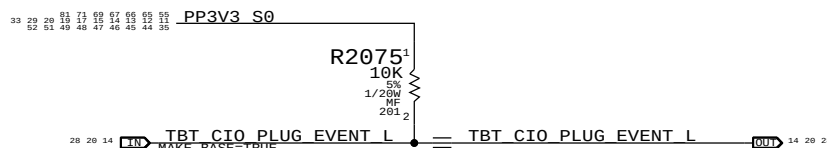
GS3 Connector Support

DEVSLP not supported on LPT-H



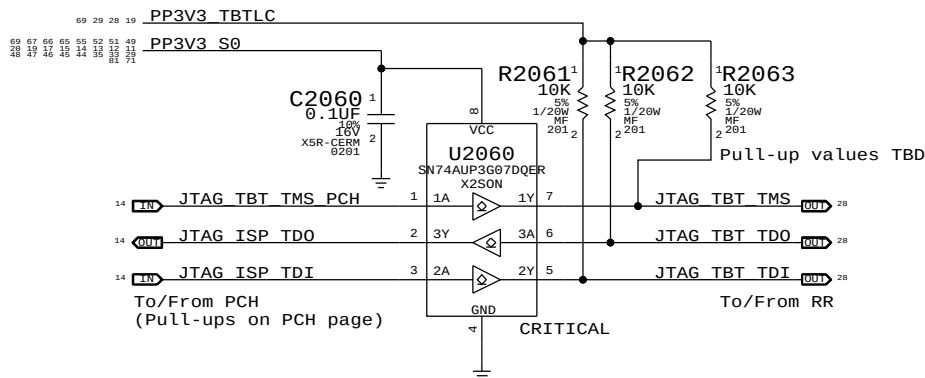
Redwood Ridge Support

RR output is open-drain, no isolation necessary



Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



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		PAGE	20 OF 118
		SHEET	20 OF 81

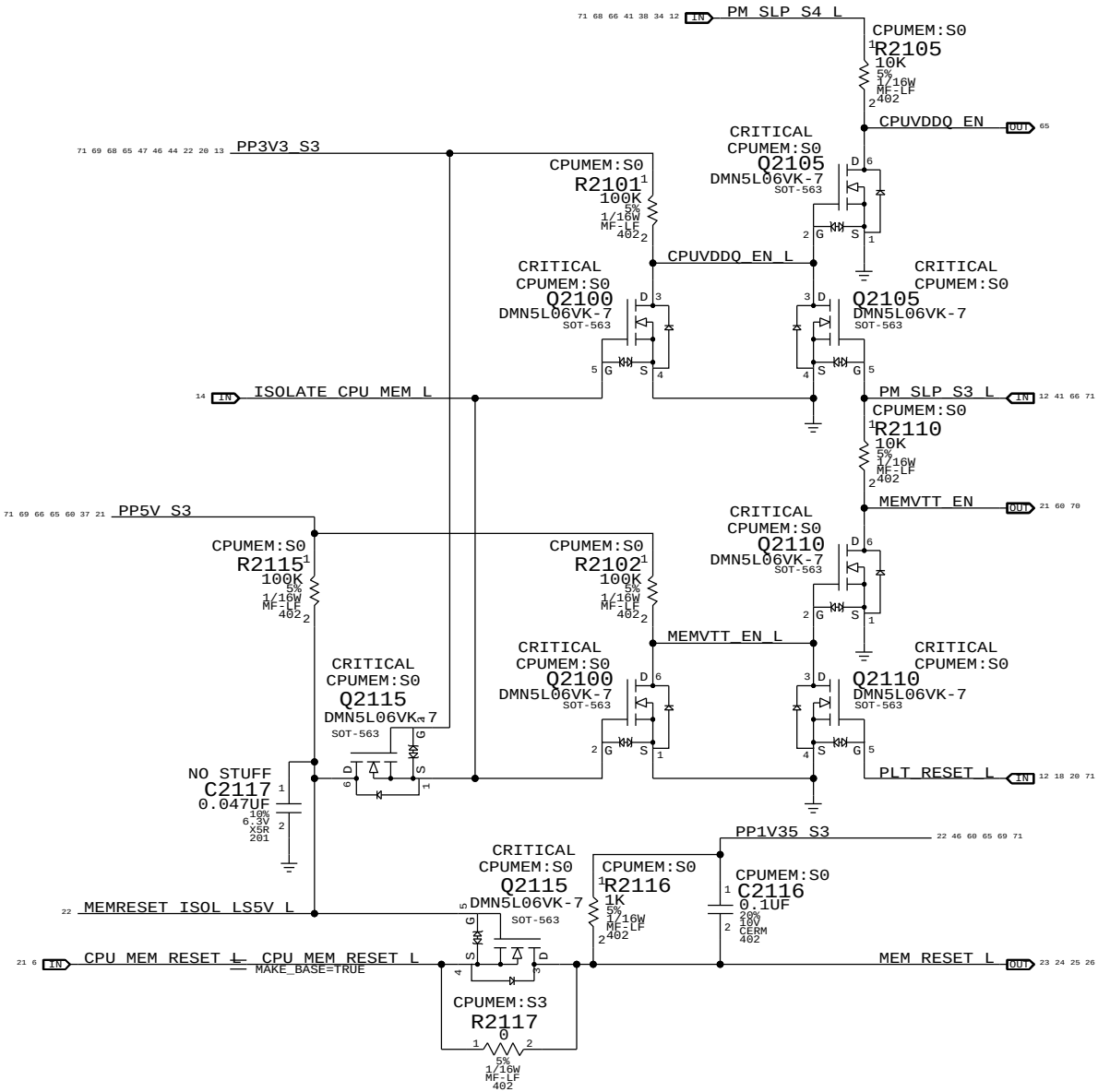
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

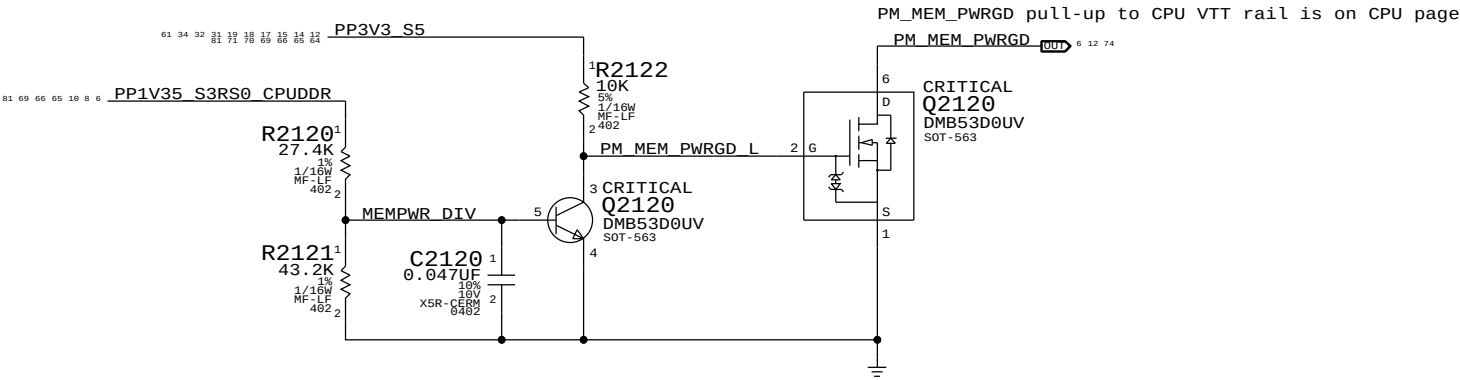
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

$$\text{CPUVDDQ_EN} = (\text{ISOLATE_CPU_MEM_L} + \text{PM_SLP_S3_L}) * \text{PM_SLP_S4_L}$$
$$\text{MEMVTT_EN} = (\text{ISOLATE_CPU_MEM_L} + \text{PLT_RST_L}) * \text{PM_SLP_S3_L}$$
$$\text{MEM_RESET_L} = !\text{ISOLATE_CPU_MEM_L} + \text{CPU_MEM_RESET_L}$$

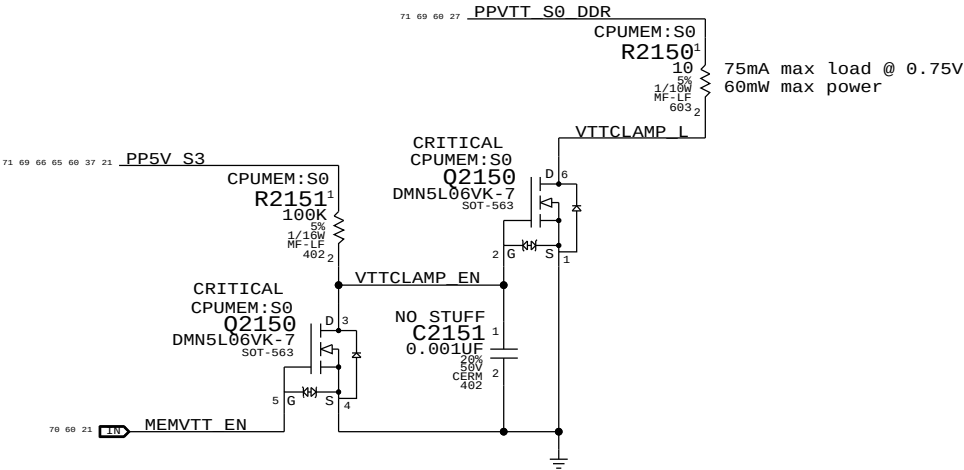


MEM S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
S3	2	0	1	1	1	1	0	1
to	3	0	0	1	X	1	0	0
S0	4	0	1	1	X	1	0	1
	5	0	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

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CPU Memory S3 Support		Drawing Number	
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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

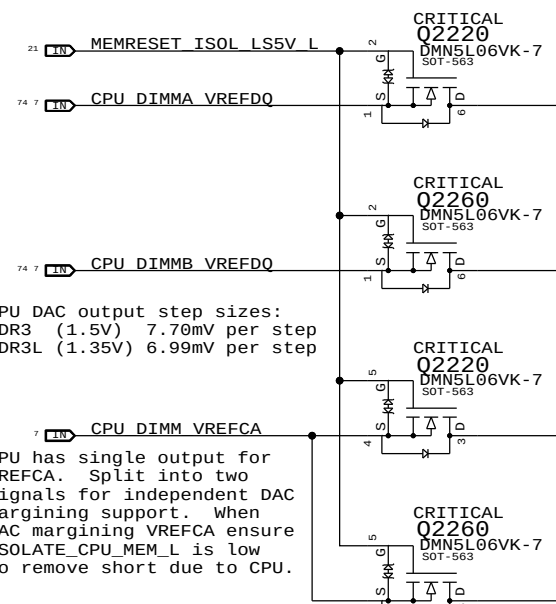
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

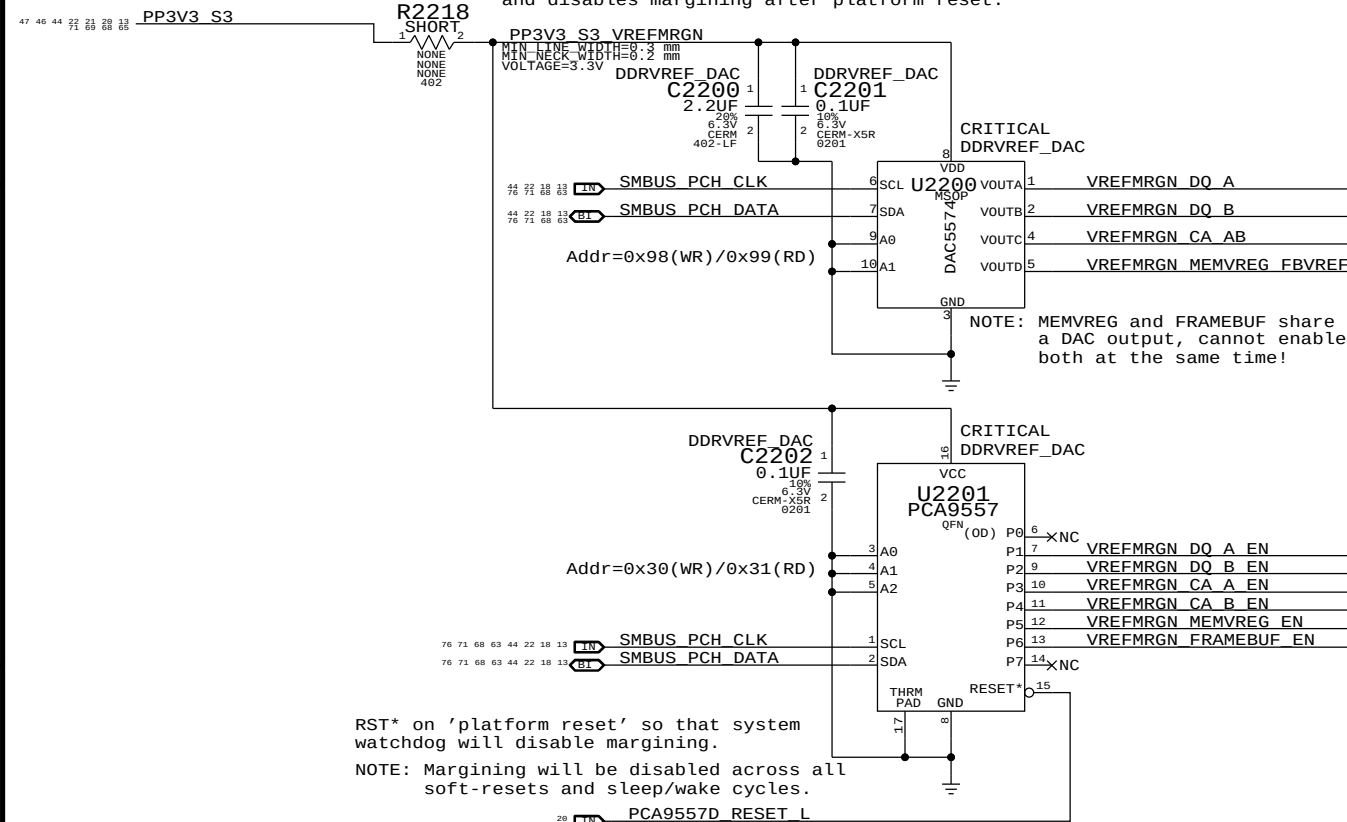


NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFOCA. Split into two signals for independent DAC margining support. When DAC margining VREFOCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



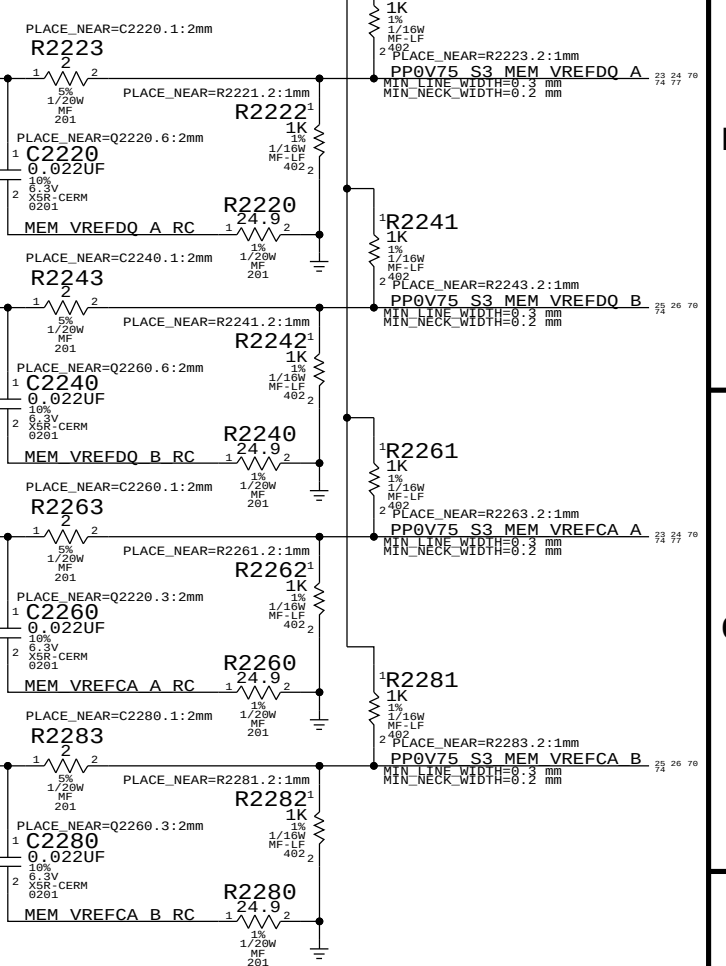
RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

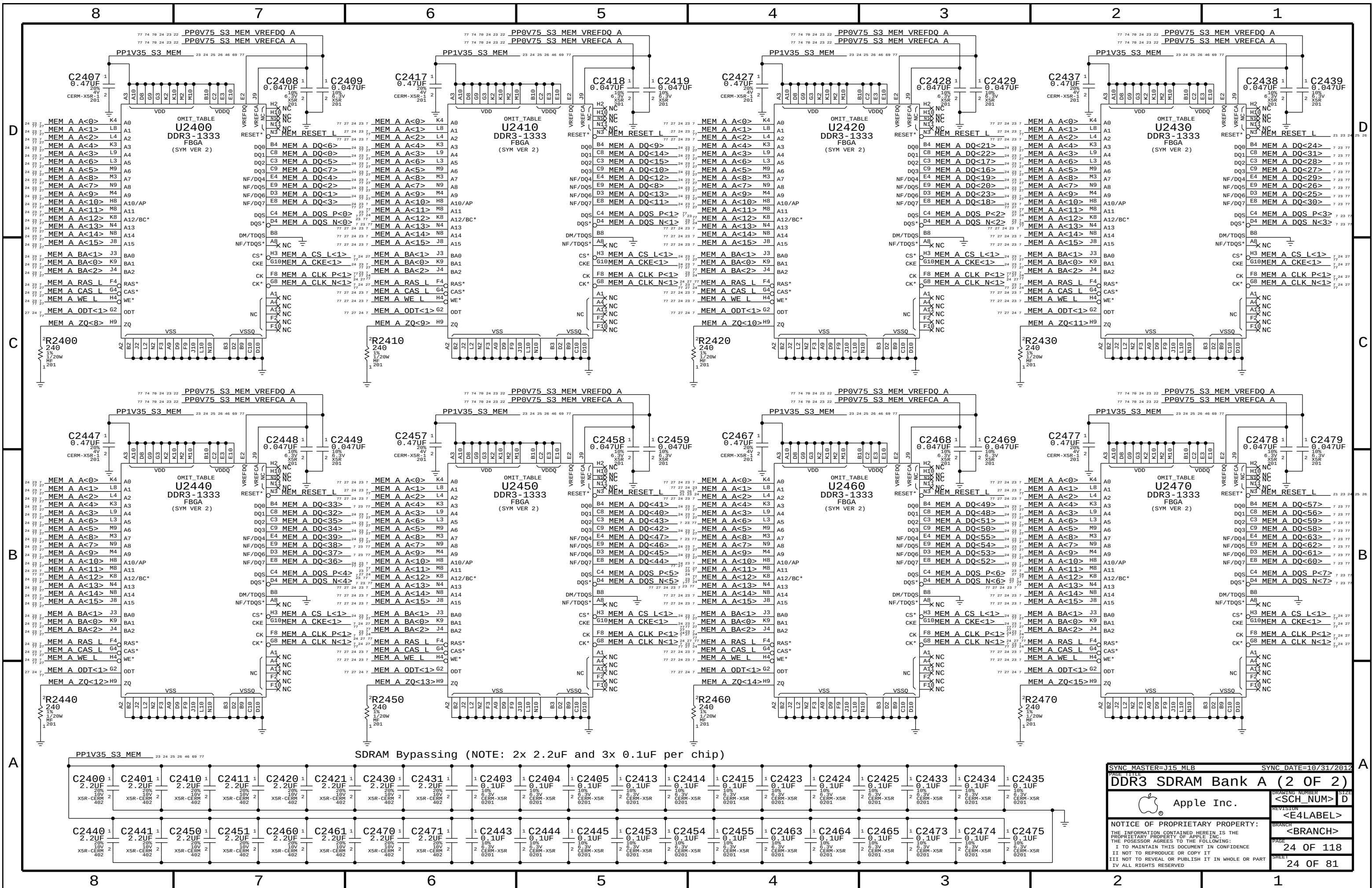
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

VRef Dividers

Always used, regardless of margining option.

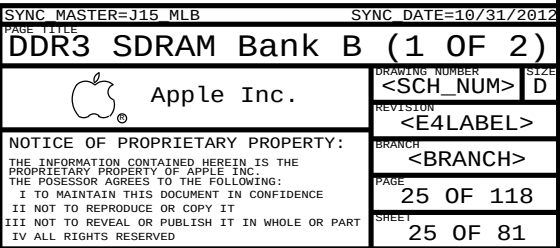


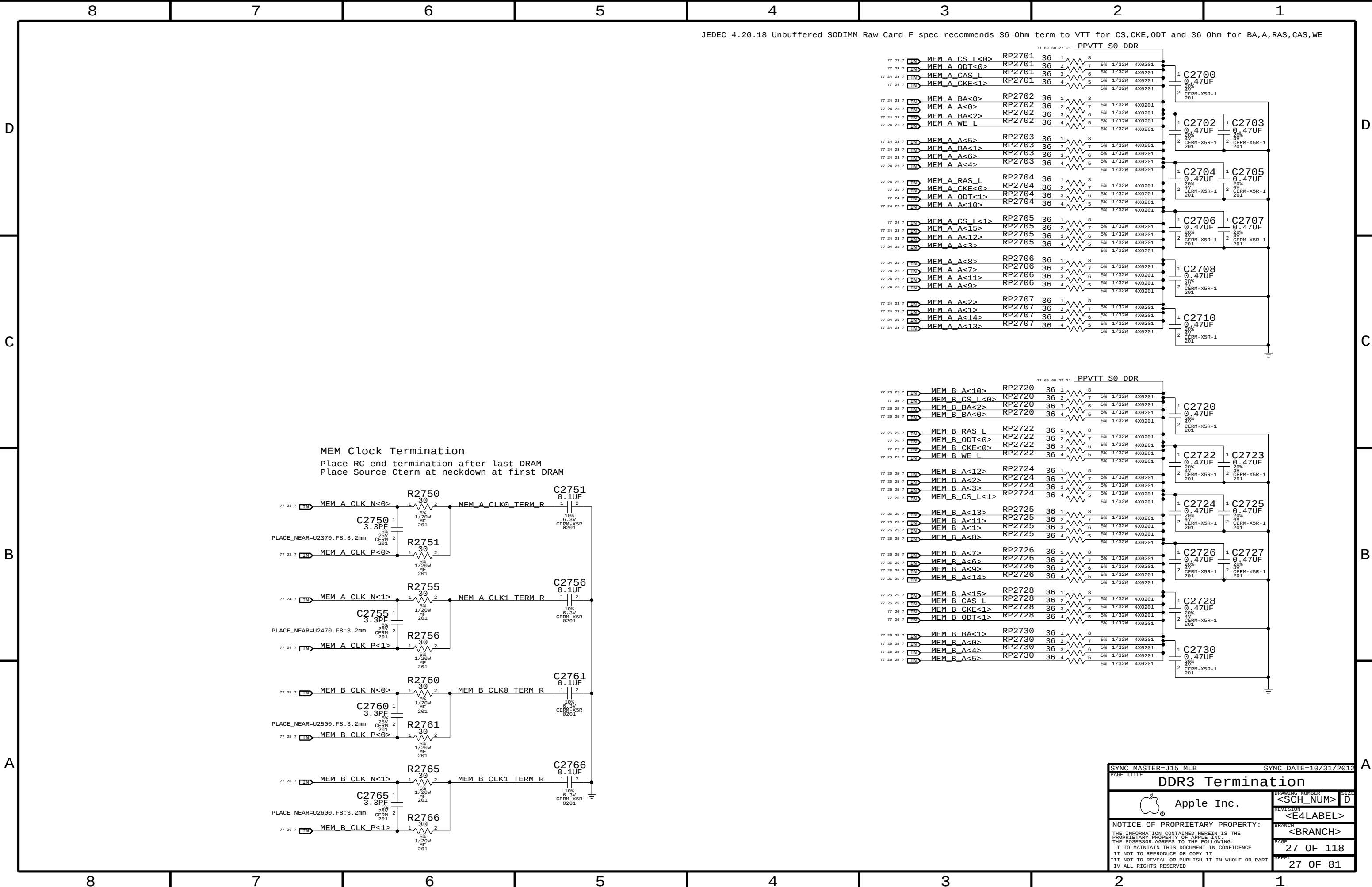
SYNCH MASTER=J15 MLB		SYNCH DATE=10/31/2012	
PAGE TITLE			
DDR3 VREF MARGINING			
		DRAWING NUMBER	
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		<E4LABEL>	
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DDR3 SDRAM Bank A (2 OF 2)
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PAGE
24 OF 118
SHEET
24 OF 81





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PAGE TITLE

DDR3 Termination

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<E4LABEL>

BRANCH

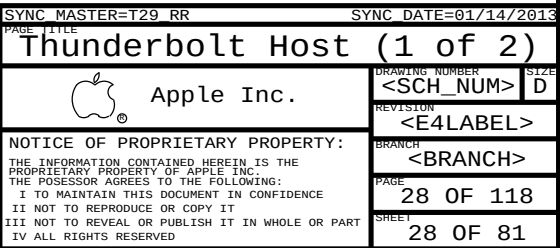
<BRANCH>

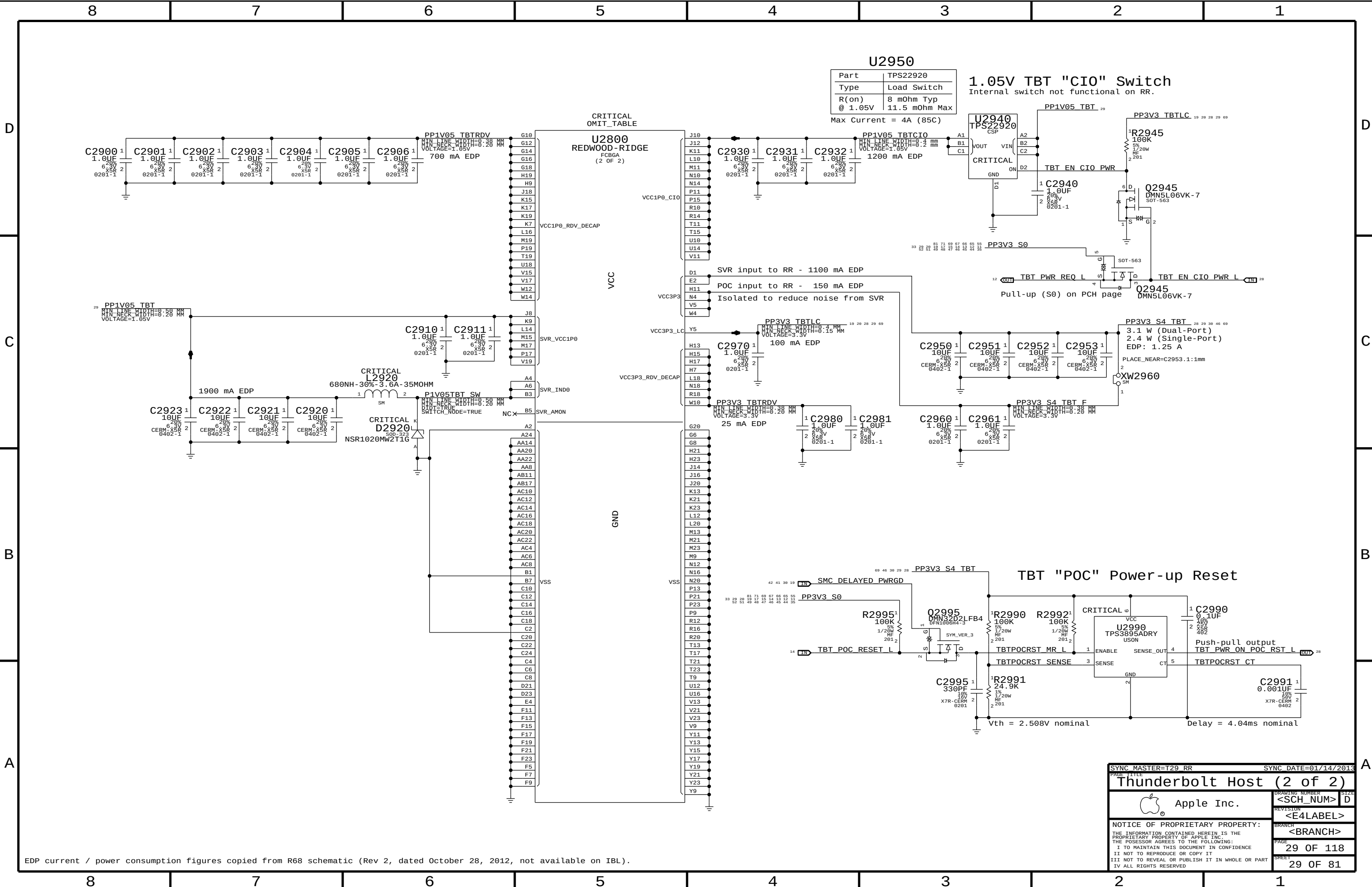
PAGE

27 OF 118

SHEET

27 OF 81





U2950	
Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max
Max Current = 4A (85C)	

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

SYNC MASTER=T29 RR		SYNC DATE=01/14/2013	
PAGE TITLE		Thunderbolt Host (2 of 2)	
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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		<BRANCH>	
		PAGE	29 OF 118
		SHEET	29 OF 81

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

Power aliases required by this page:	
- PPVIN_SW_TBTBST	(8-13V Boost Input)
- PP15V_TBT_REG	(15V Boost Output)
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

[illegible]

03000
DMN3202LFB4
DFN1608HA-3
SW_V6.3

PM BATLOW L

3V3

5V

Pull-up on RR page

TBT BATLOW L

MAKE BASE=TRUE

SYNC MASTER=T29 RR		SYNC DATE=01/14/2013	
PAGE TITLE		SIZE	
Thunderbolt Mobile Support		D	
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		REVISION <E4LABEL>	
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8	7	6	5	4	3	2	1
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D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210, R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211, R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

B

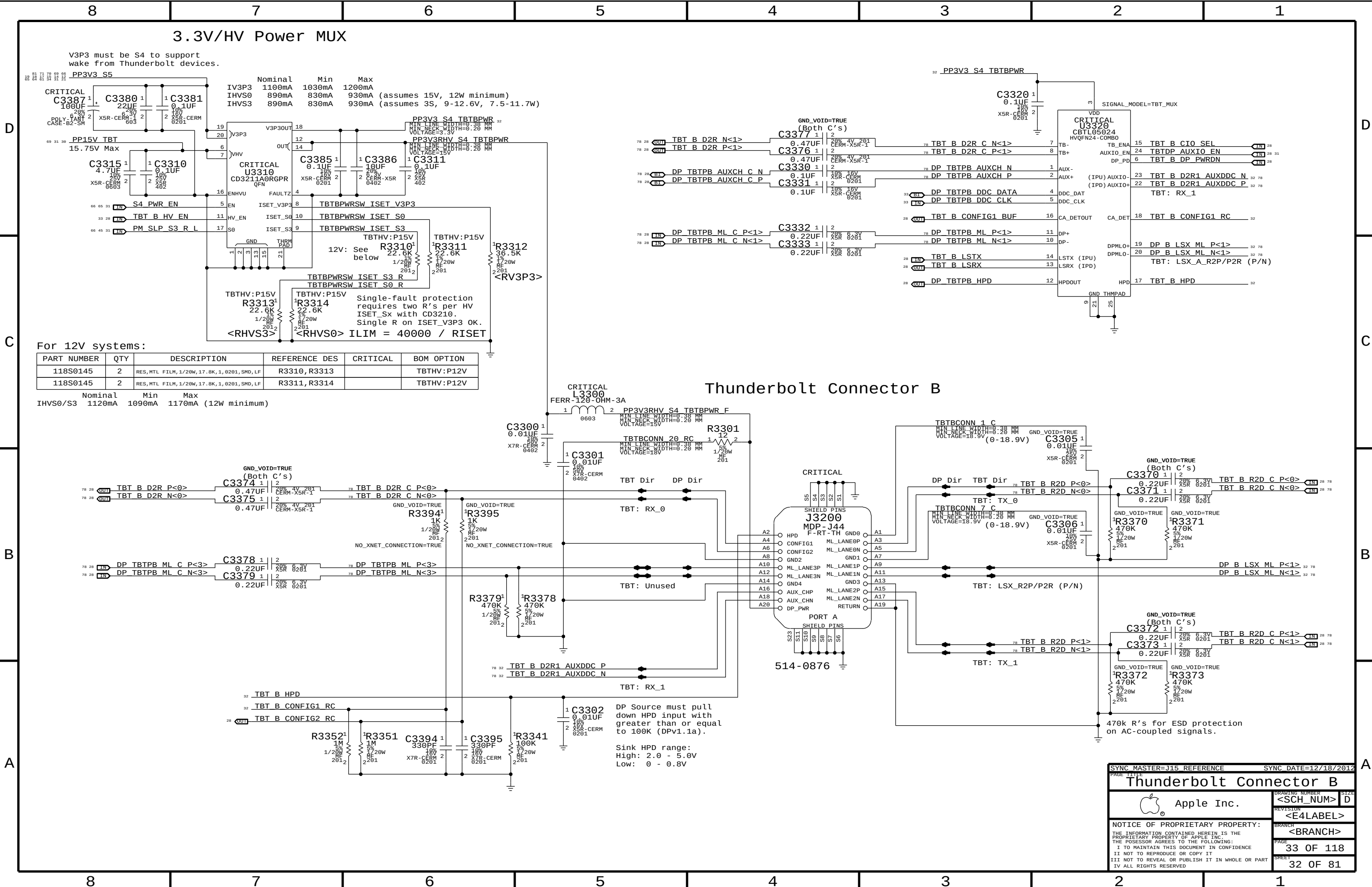


Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

D



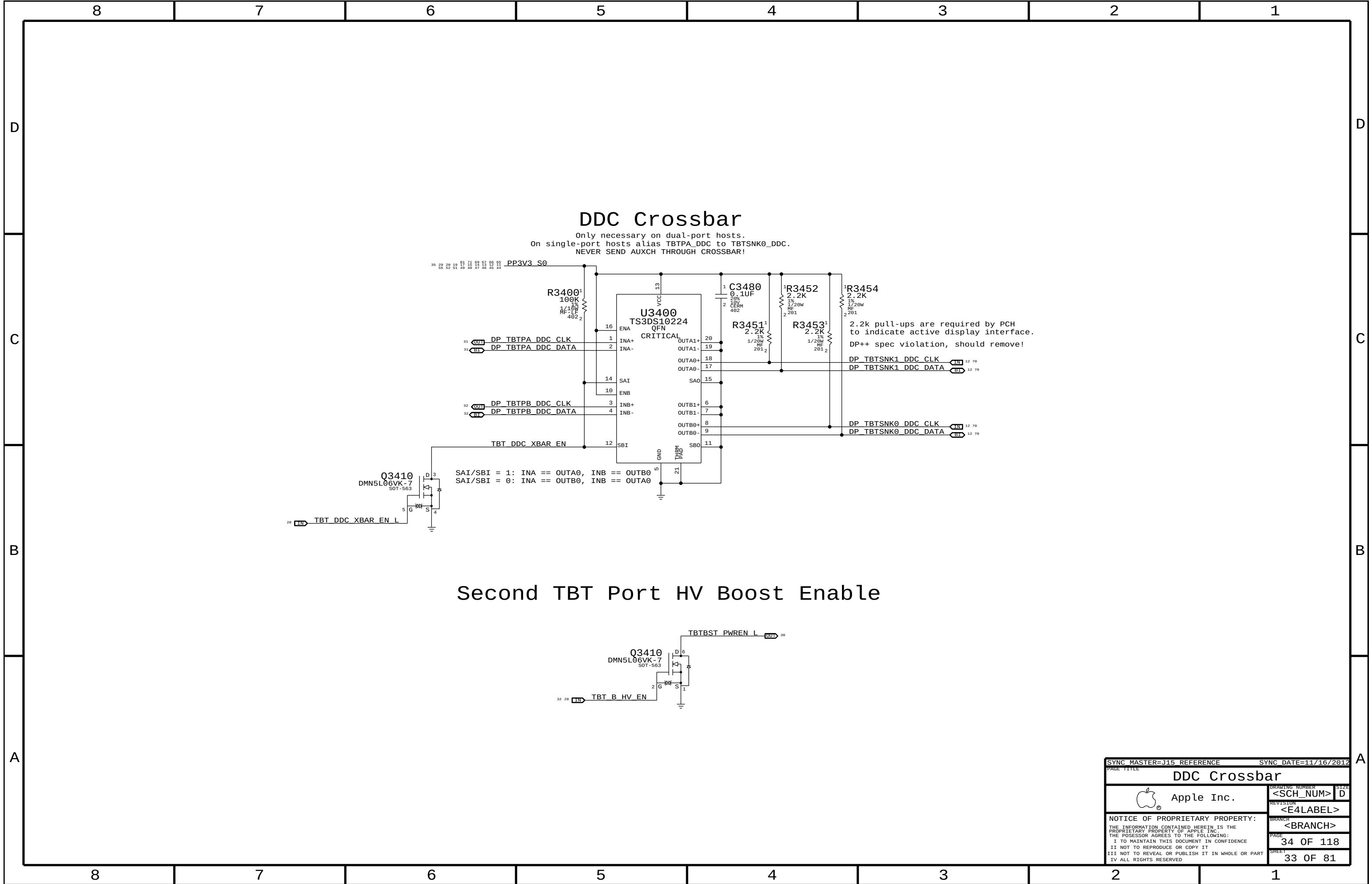
A

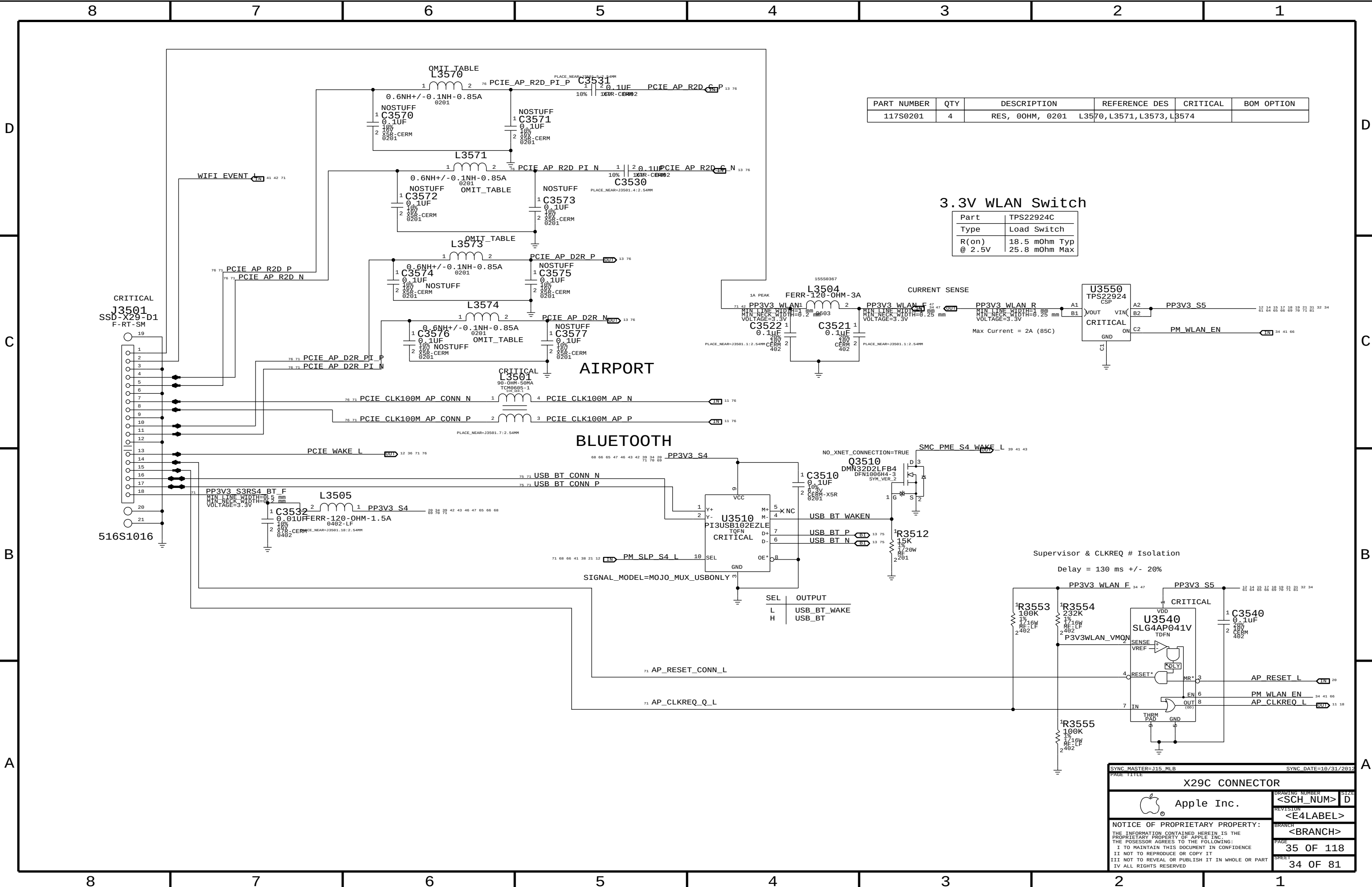


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES, MTL FILM, 1/20W, 17.8K, 1, 0201, SMD, LF	R3310, R3313		TBTHV:P12V
118S0145	2	RES, MTL FILM, 1/20W, 17.8K, 1, 0201, SMD, LF	R3311, R3314		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 00HM, 0201	L3570, L3571, L3573, L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

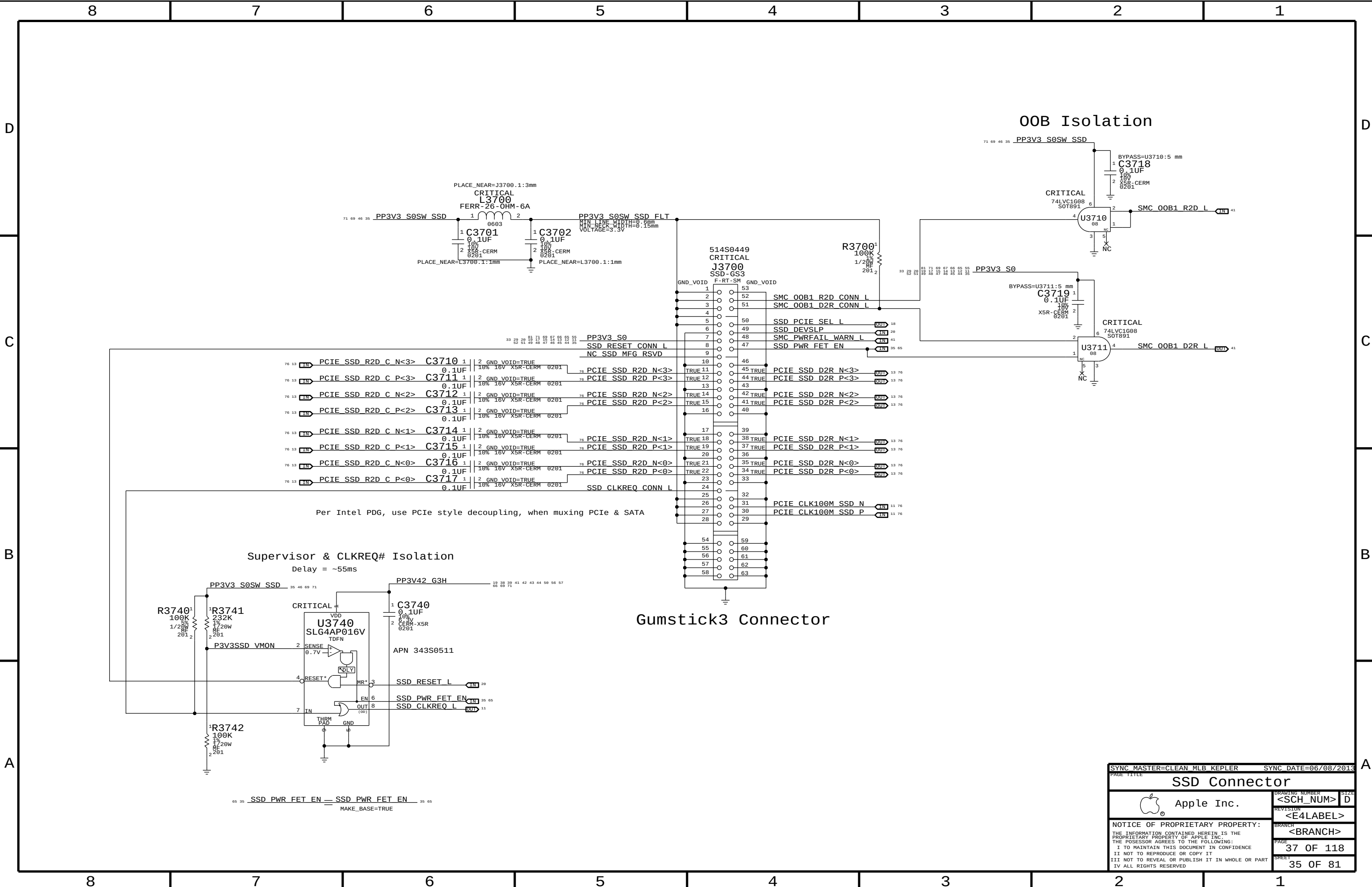
AIRPORT

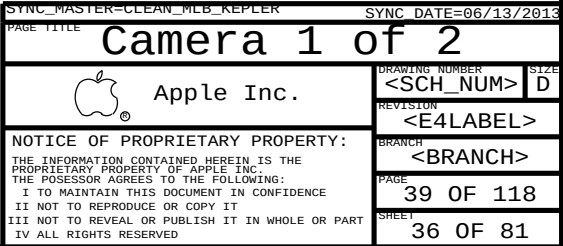
BLUETOOTH

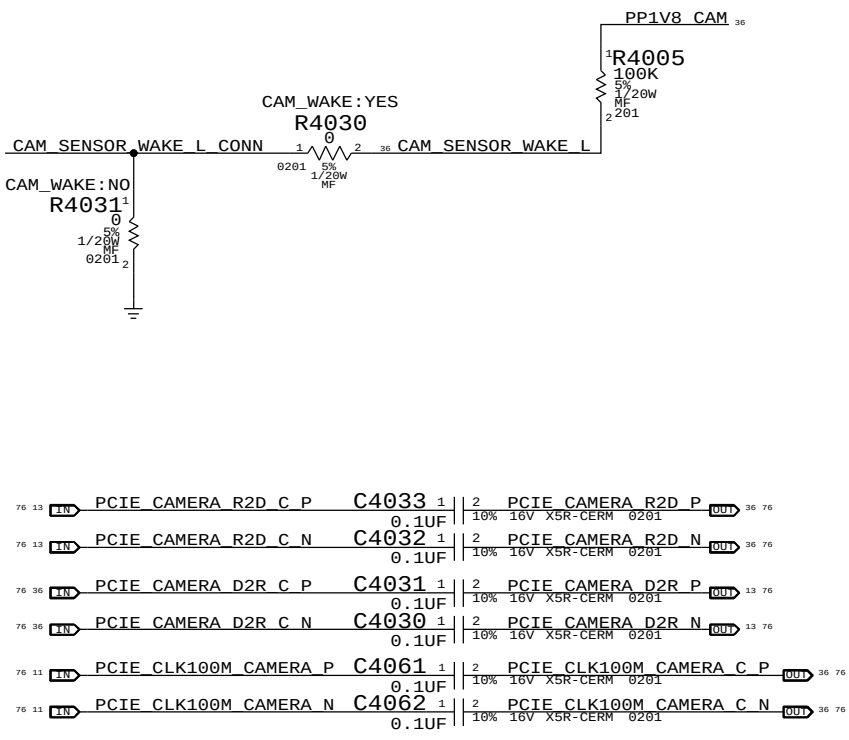
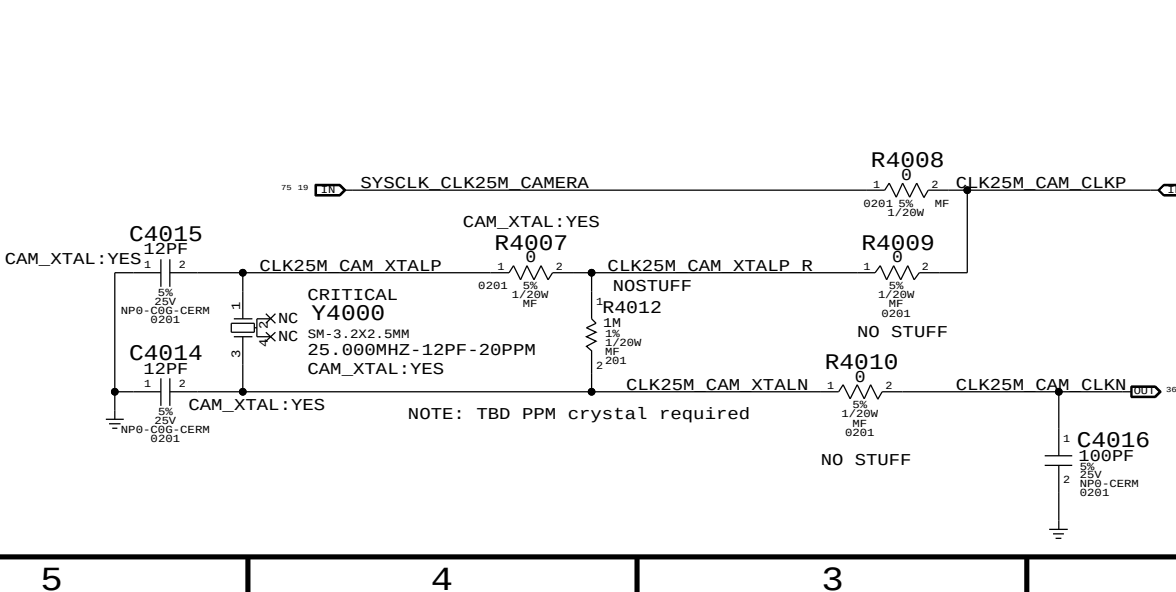
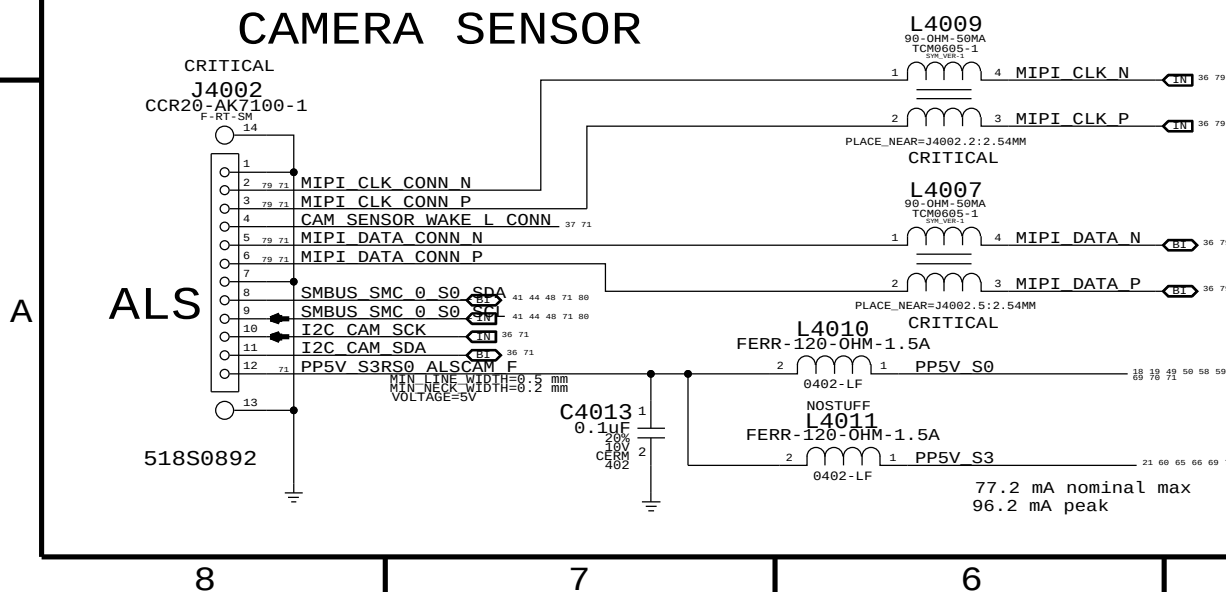
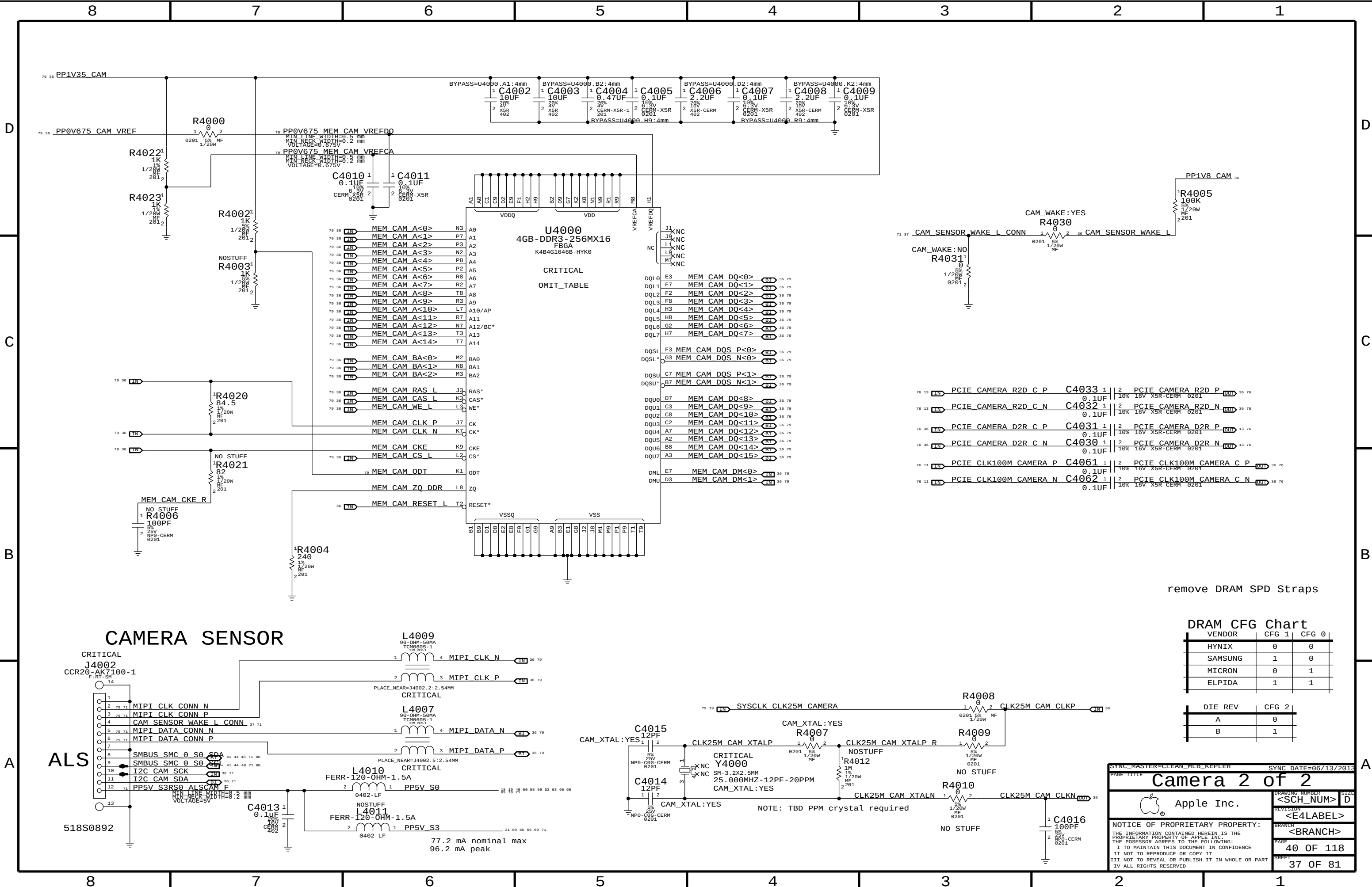
Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

SYNC MASTER=J15_MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
X29C CONNECTOR			
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		PAGE	35 OF 118
		SHEET	34 OF 81







remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

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<E4LABEL>

<BRANCH>

40 OF 118

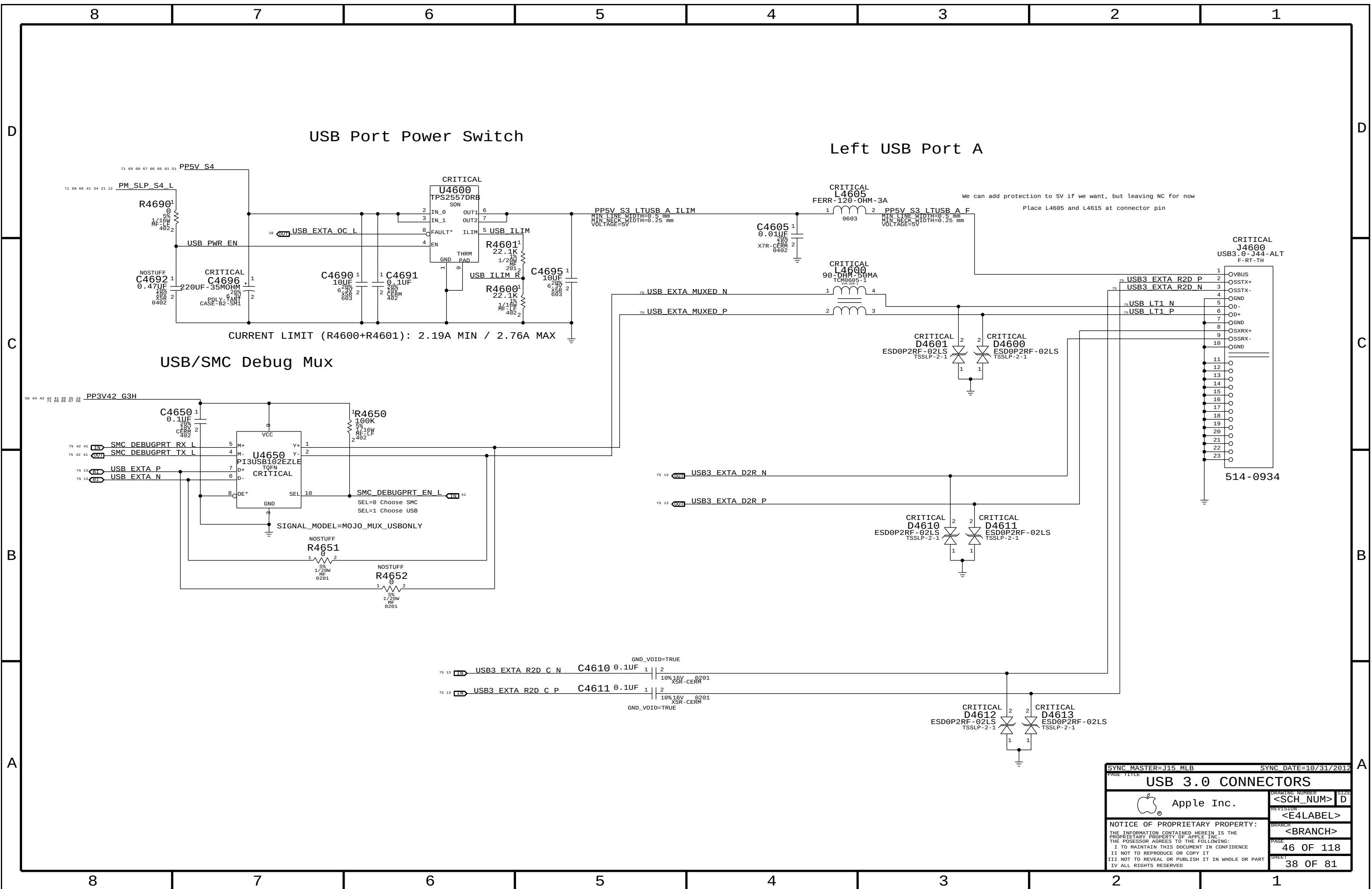
37 OF 81

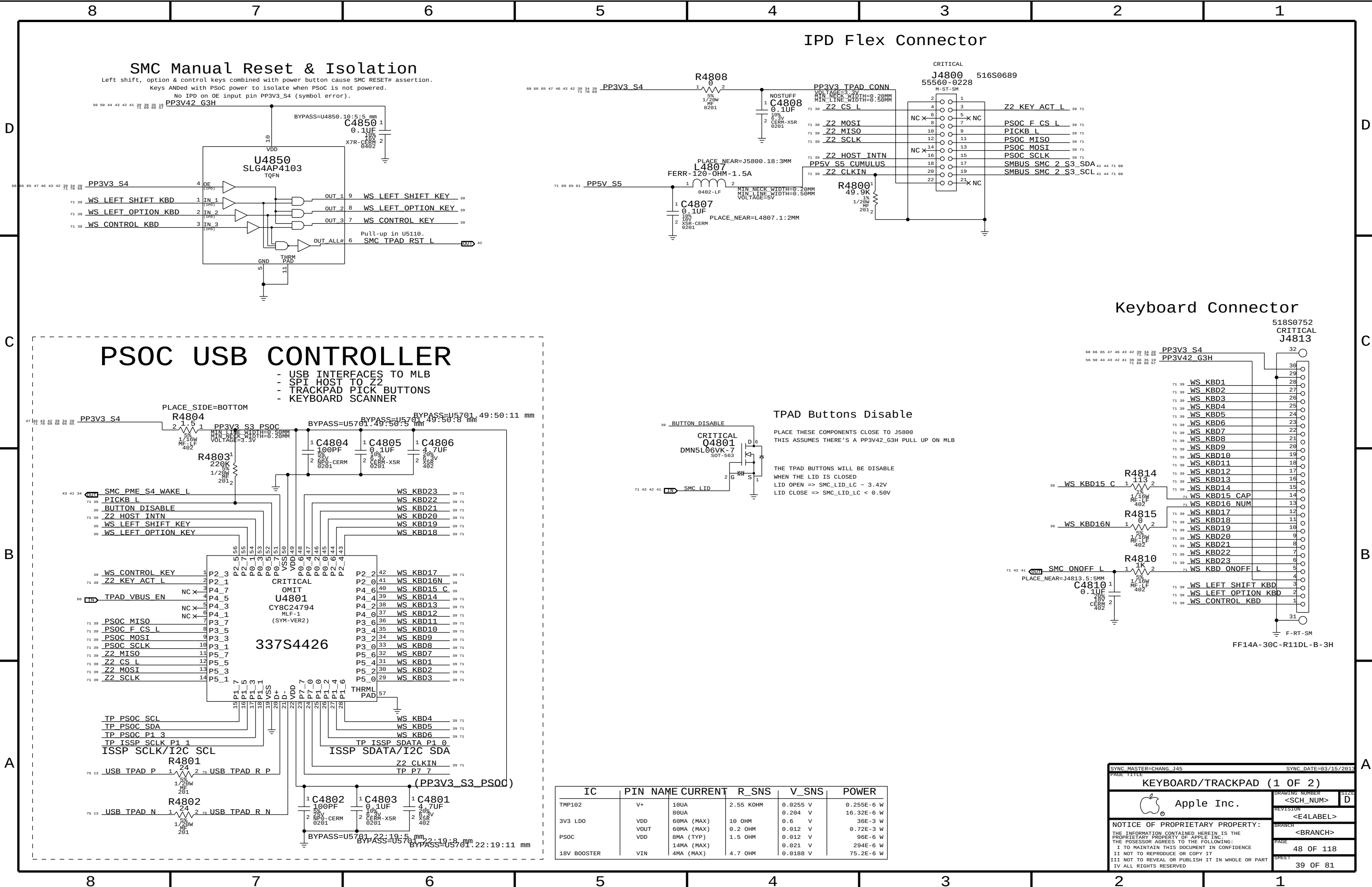
SYNC_MASTER=CLEAN_MLB_REPLER

SYNC_DATE=06/13/2013

A

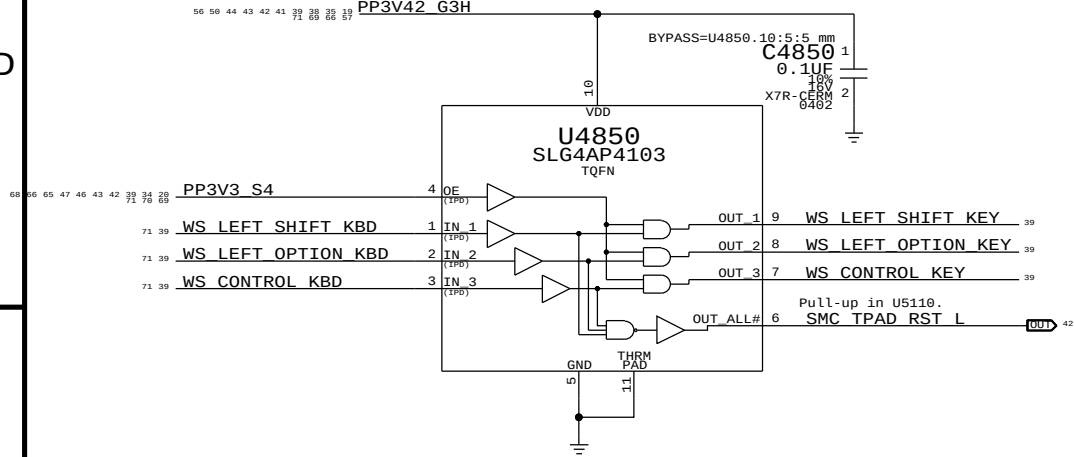
A



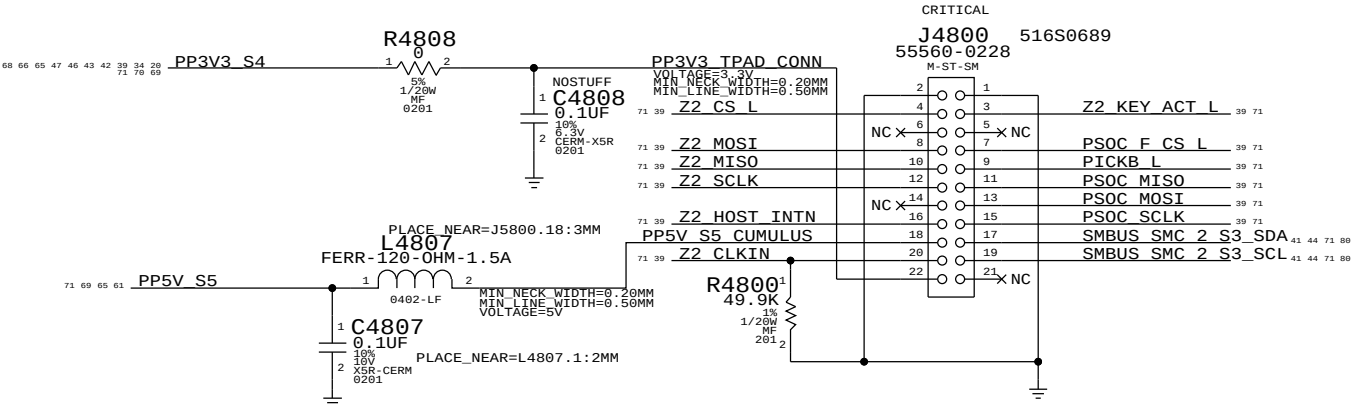


SMC Manual Reset & Isolation

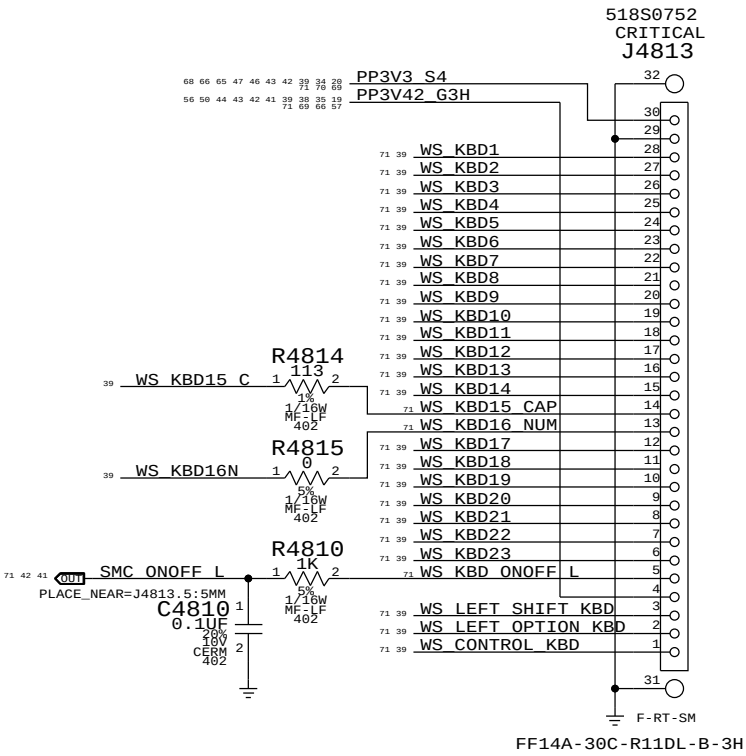
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector

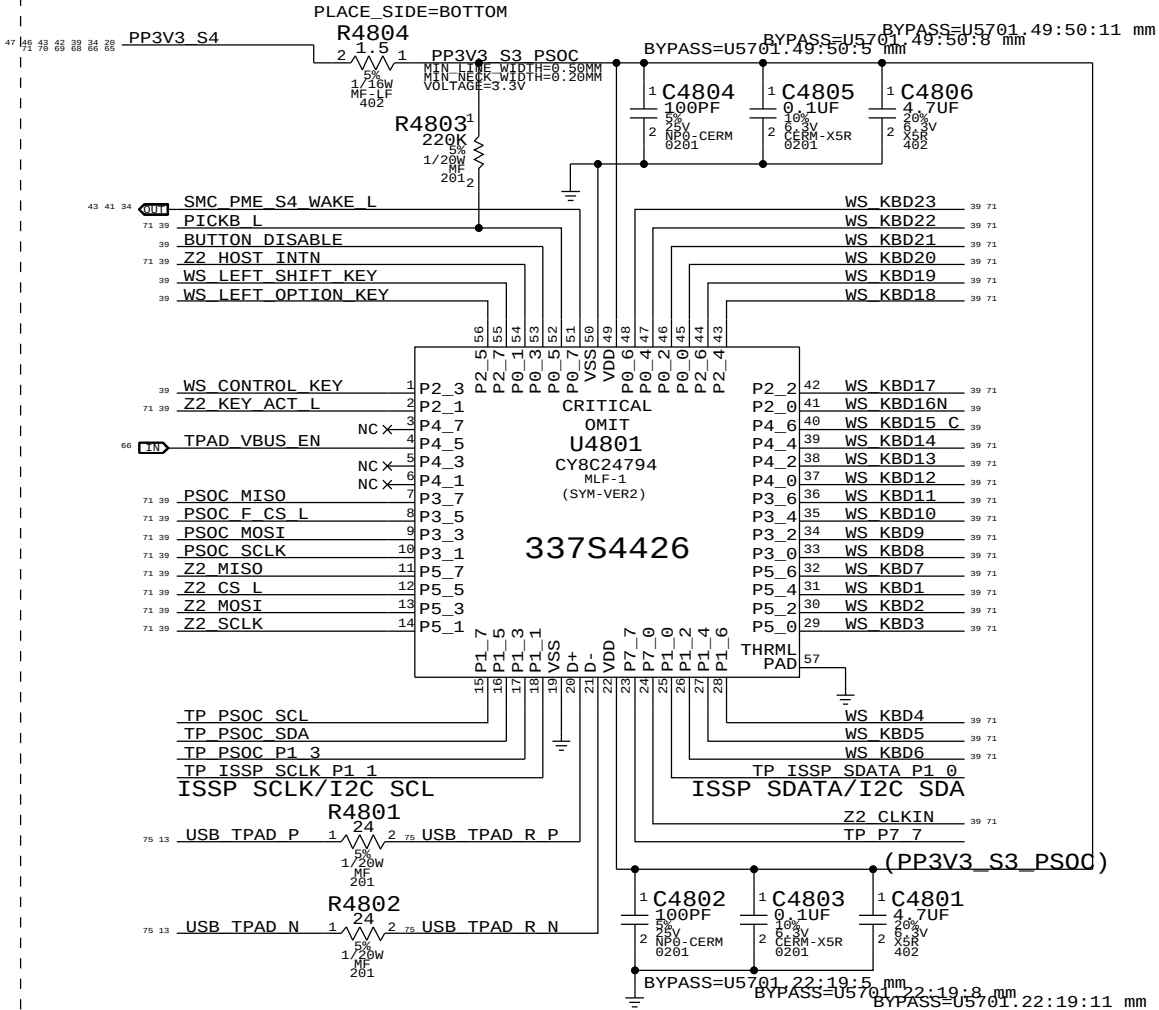


Keyboard Connector



PSOC USB CONTROLLER

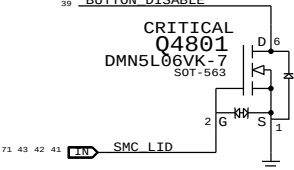
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



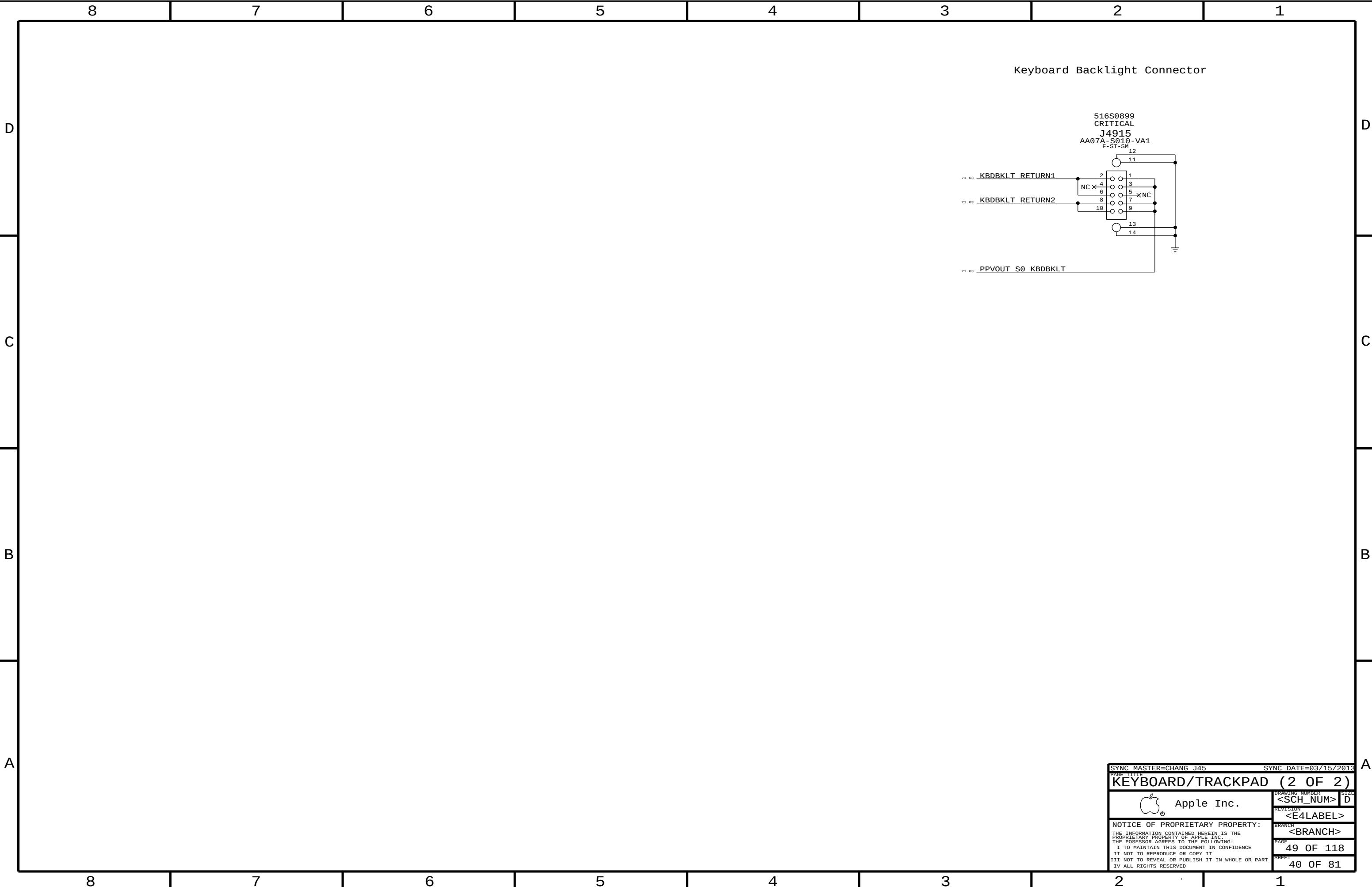
TPAD Buttons Disable

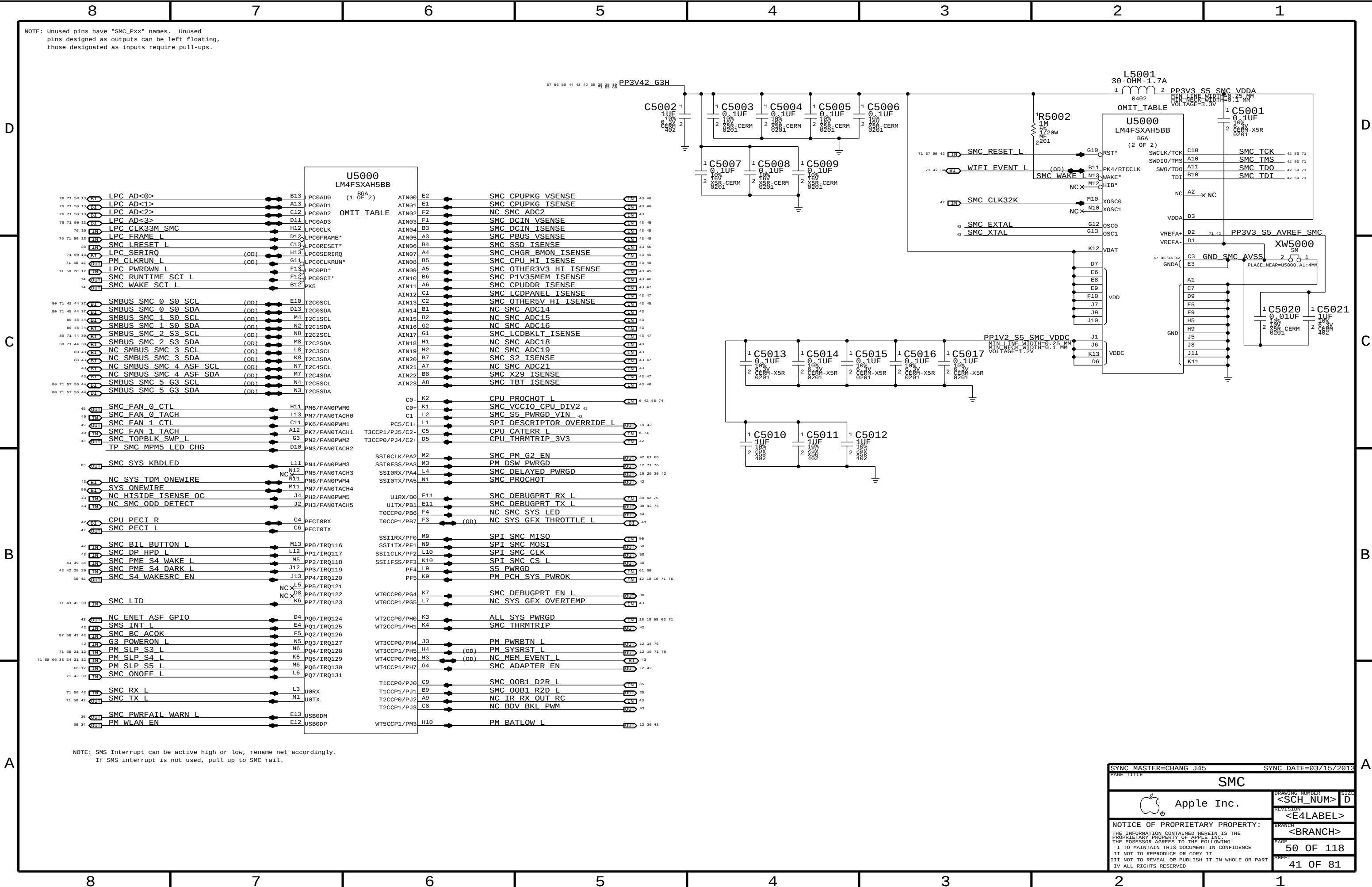
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

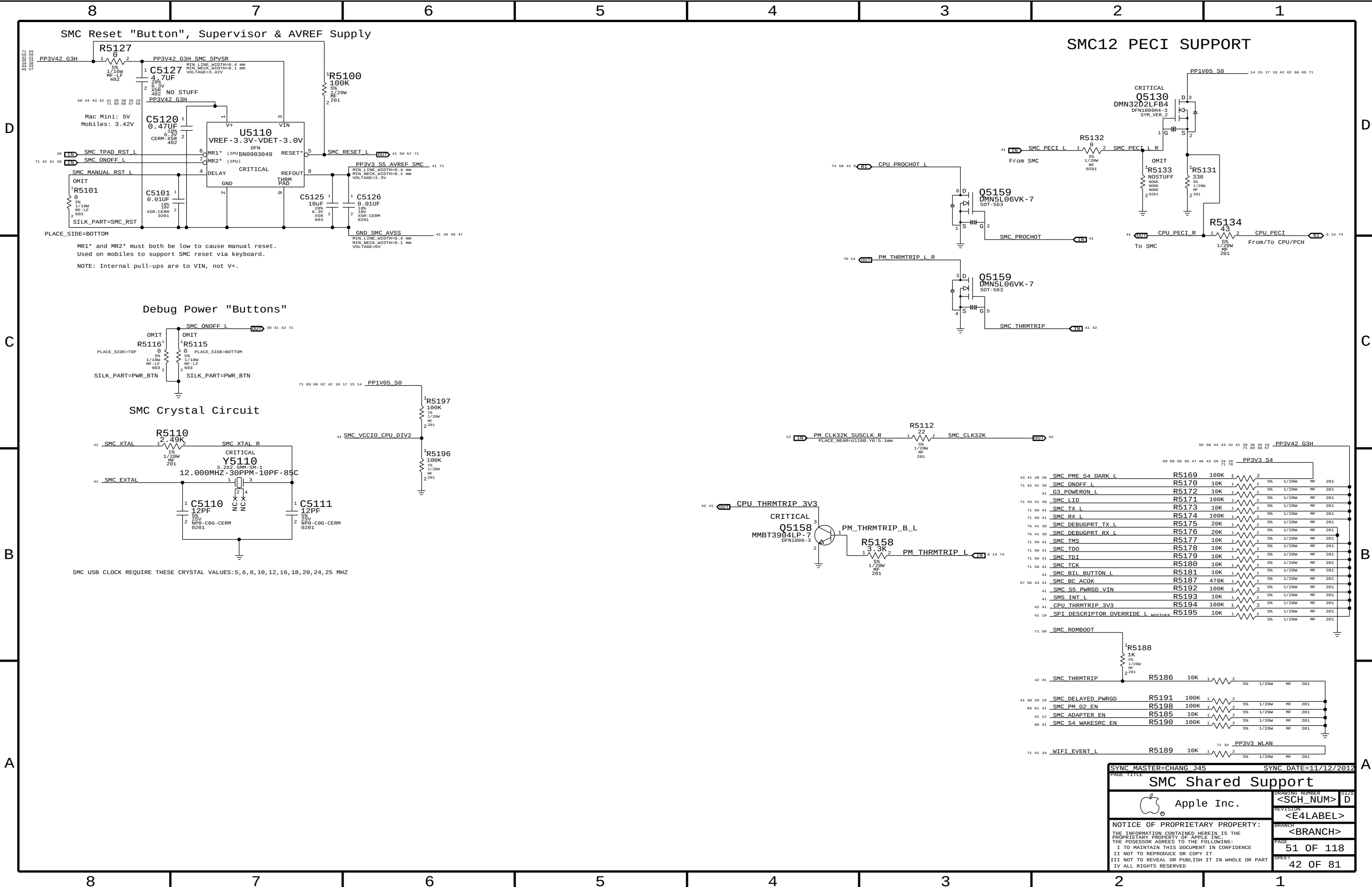
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM		0.0255 V	0.255E-6 W
		80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM		0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM		0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM		0.012 V	96E-6 W
		14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM		0.0188 V	75.2E-6 W







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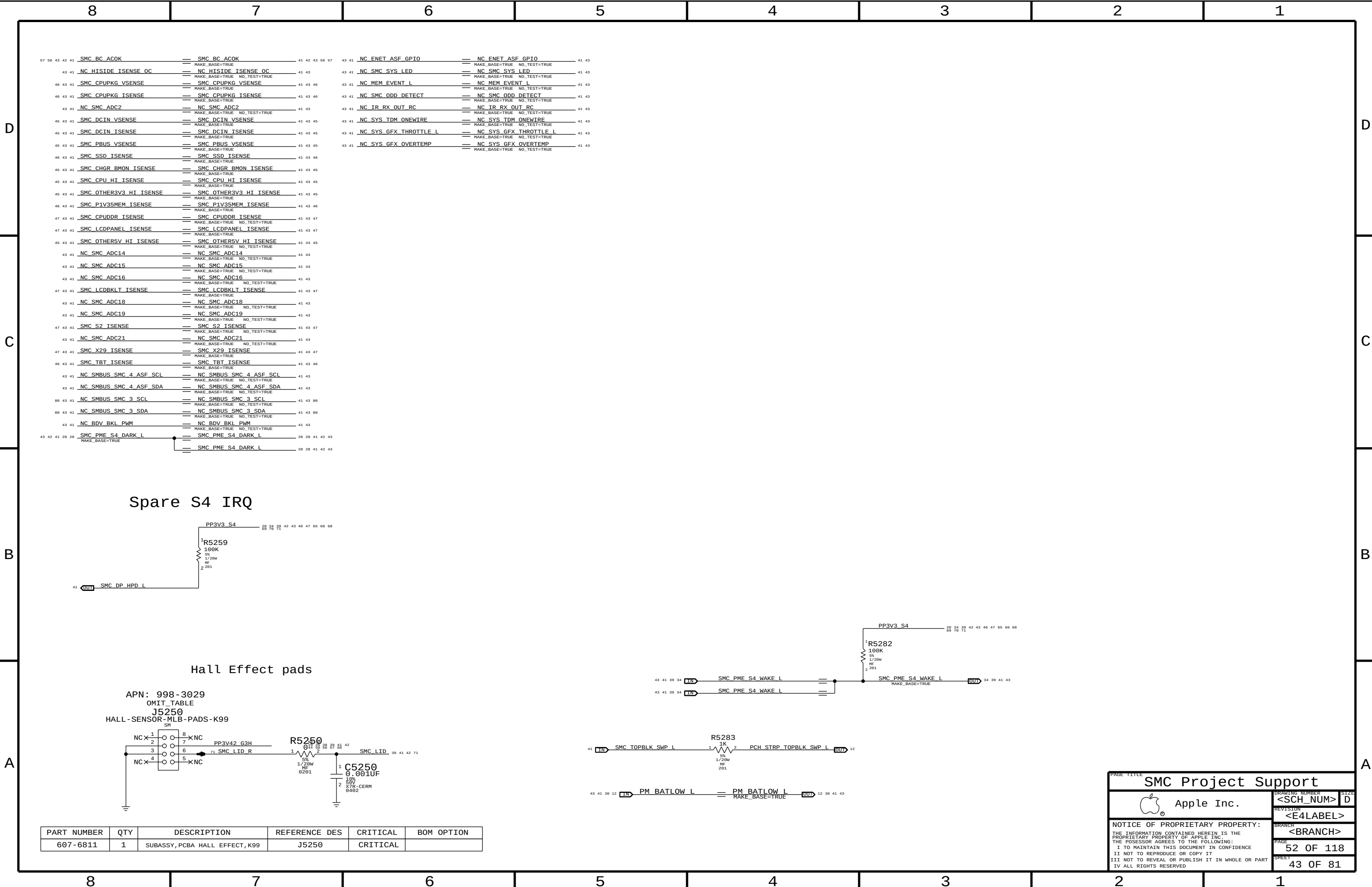
DRAWING NUMBER
<SCH_NUM> D

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<E4LABEL>

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PAGE
51 OF 118

SHEET
42 OF 81



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<E4LABEL>

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PAGE

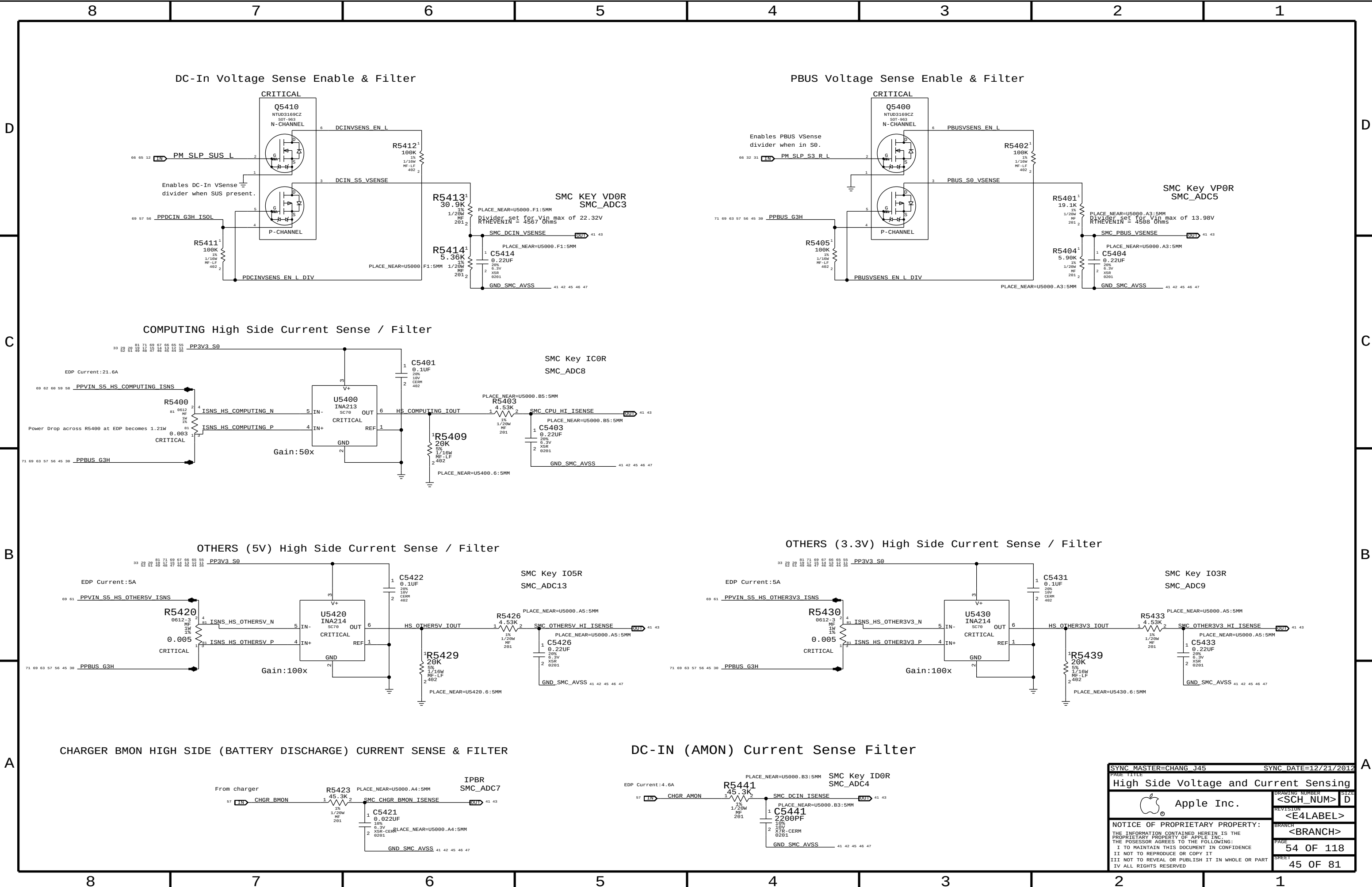
52 OF 118

SHEET

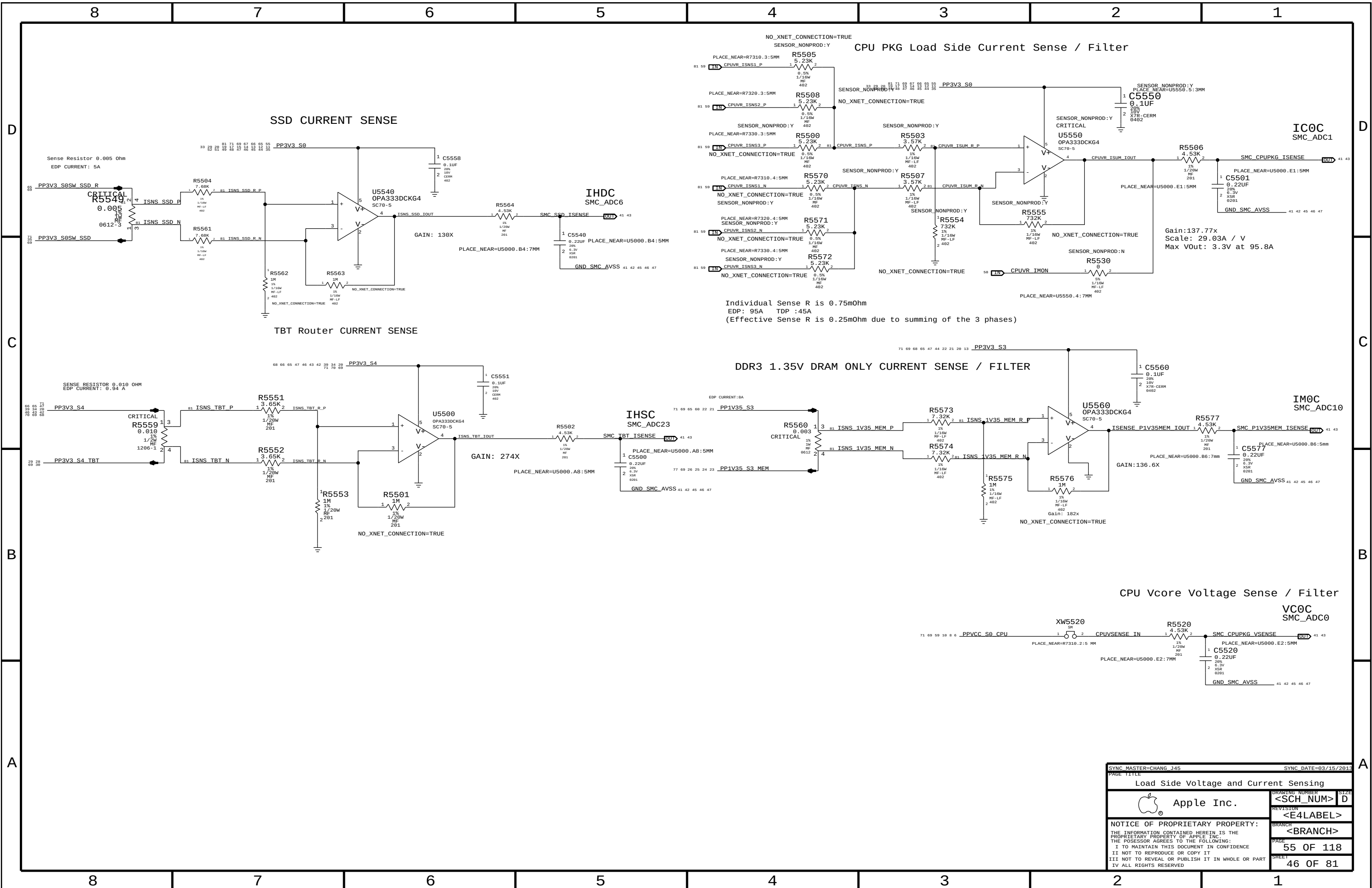
43 OF 81

SIZE

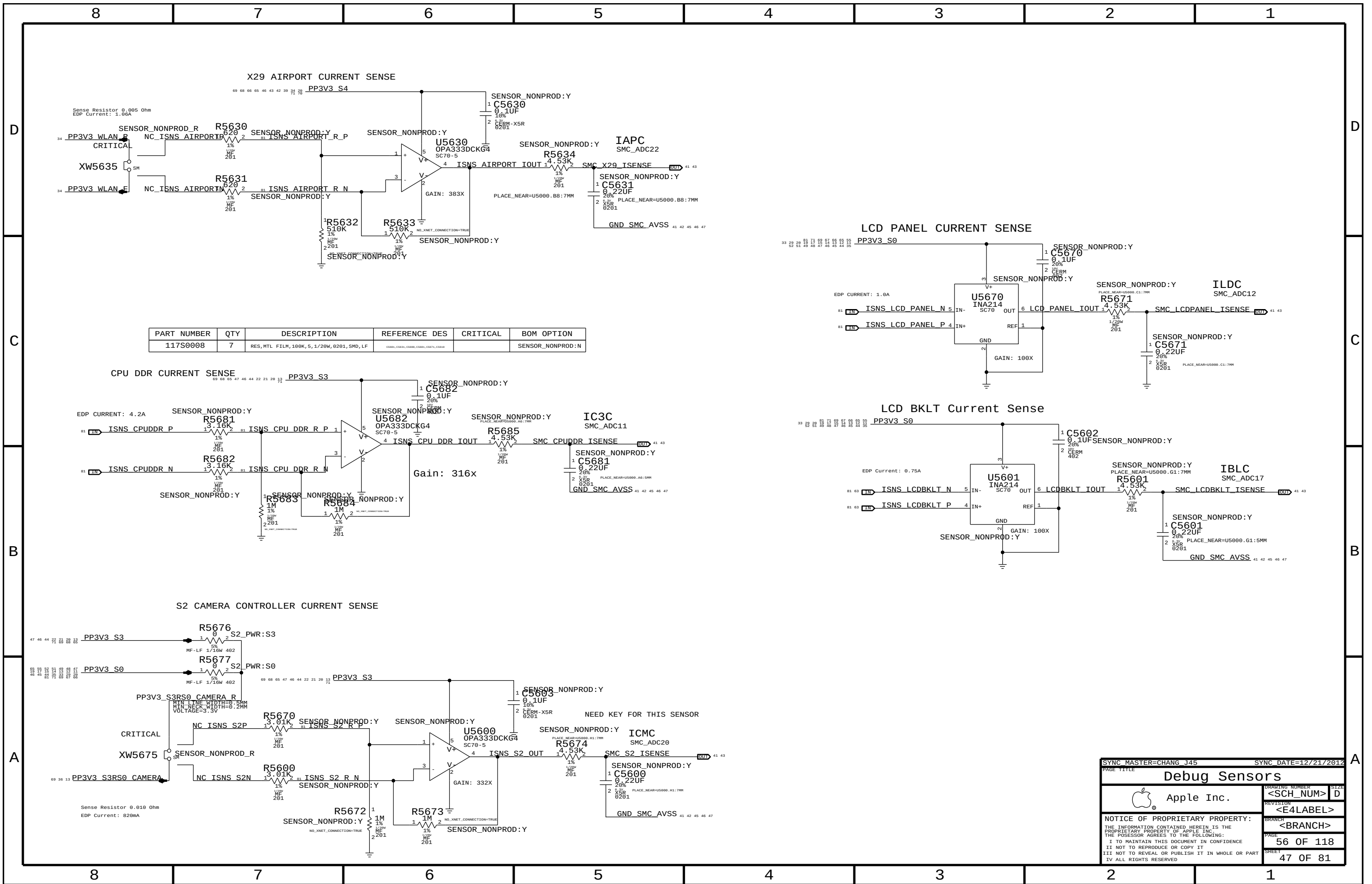
D

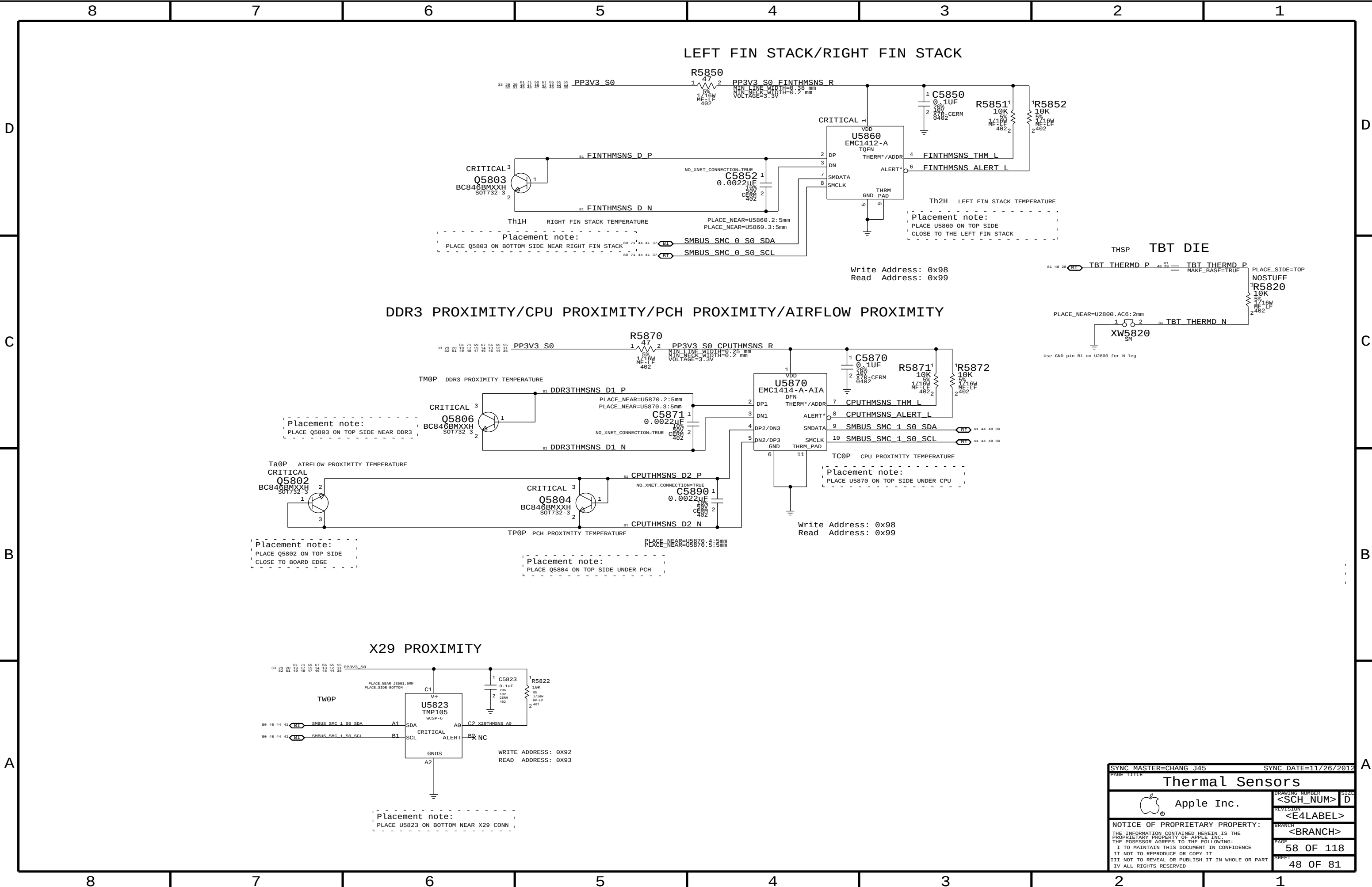


SYNC MASTER=CHANG J45		SYNC DATE=12/21/2012	
PAGE TITLE			
High Side Voltage and Current Sensing			
	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
	REVISION		<E4LABEL>
	BRANCH		<BRANCH>
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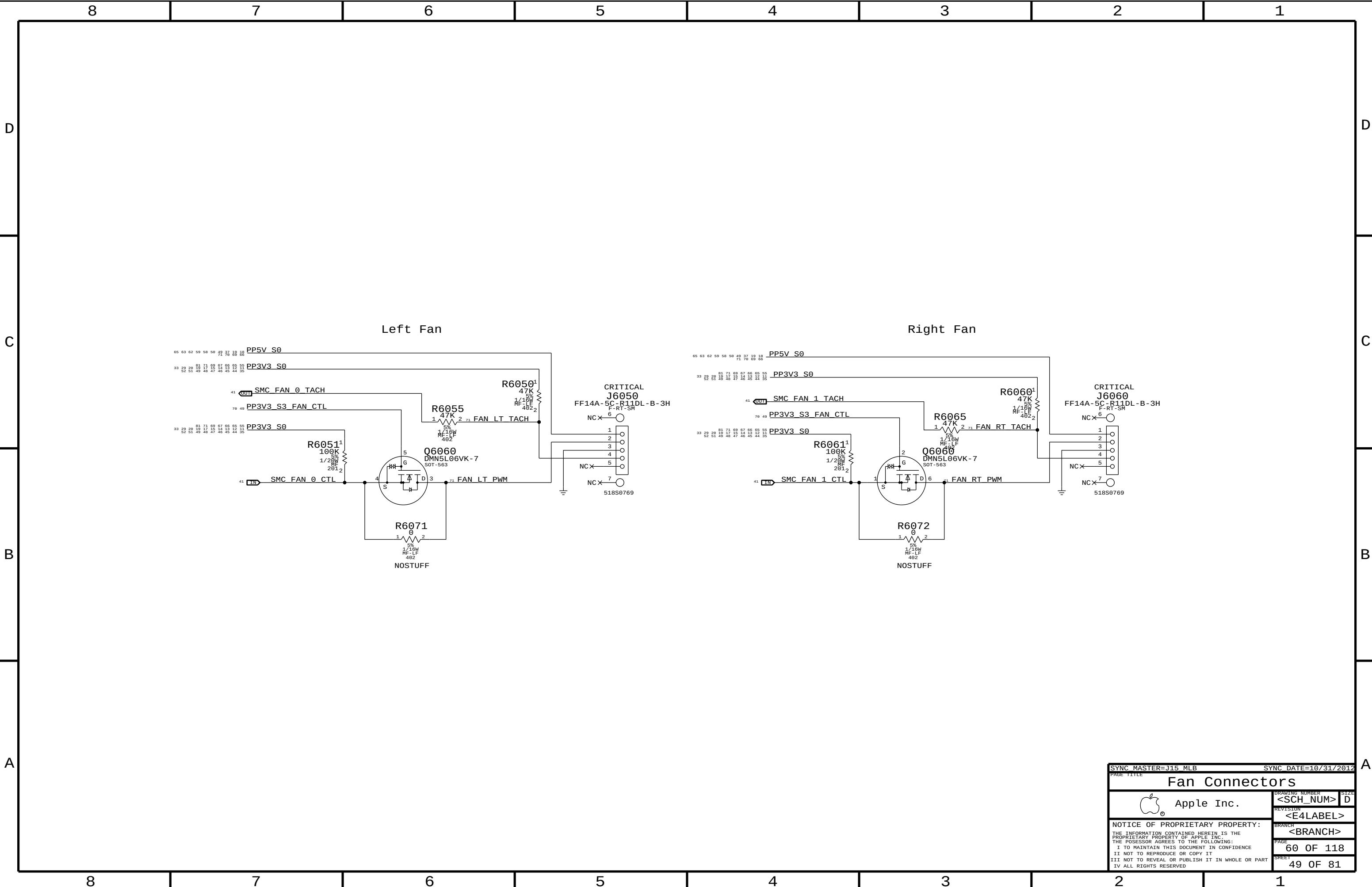


SYNC MASTER=CHANG J45		SYNC DATE=03/15/2013	
PAGE TITLE			
Load Side Voltage and Current Sensing			
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	<SCH_NUM>		D
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	<E4LABEL>		
	BRANCH		
	<BRANCH>		
	PAGE		
	55 OF 118		
	SHEET		
	46 OF 81		





SYNC MASTER=CHANG J45		SYNC DATE=11/26/2012	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
	REVISION		
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		<BRANCH>	
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		SHEET	48 OF 81



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A

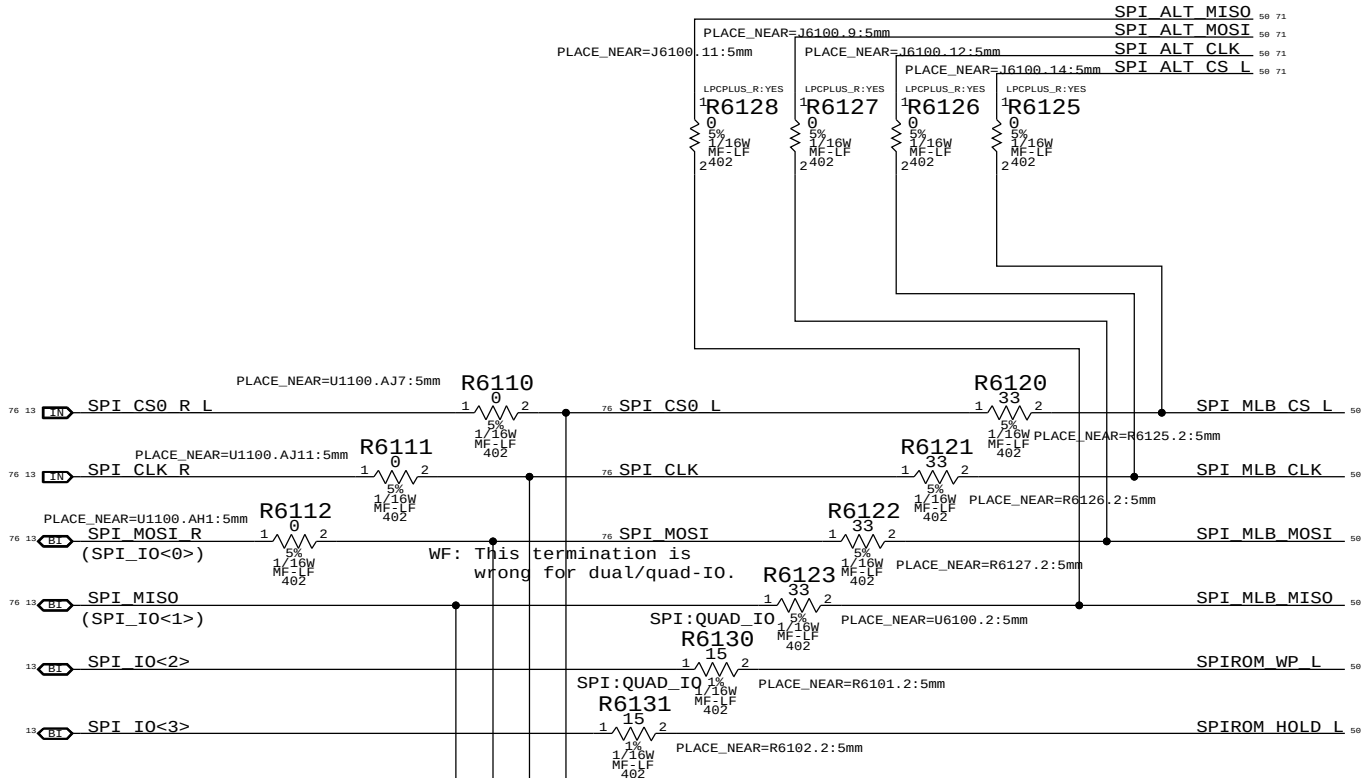
D

C

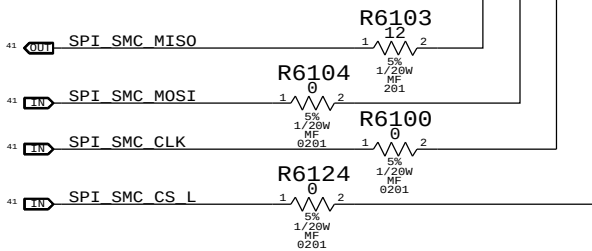
B

A

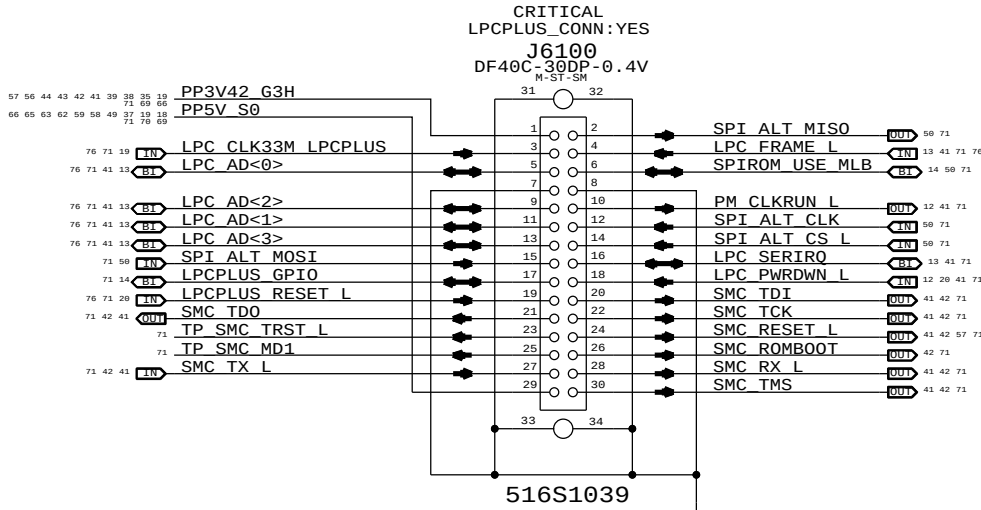
SPI Bus Series Termination



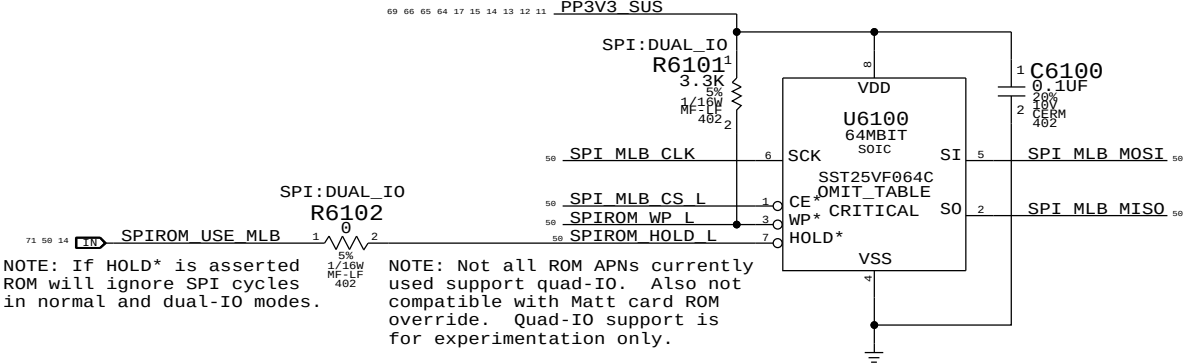
SMC12 SPI SUPPORT



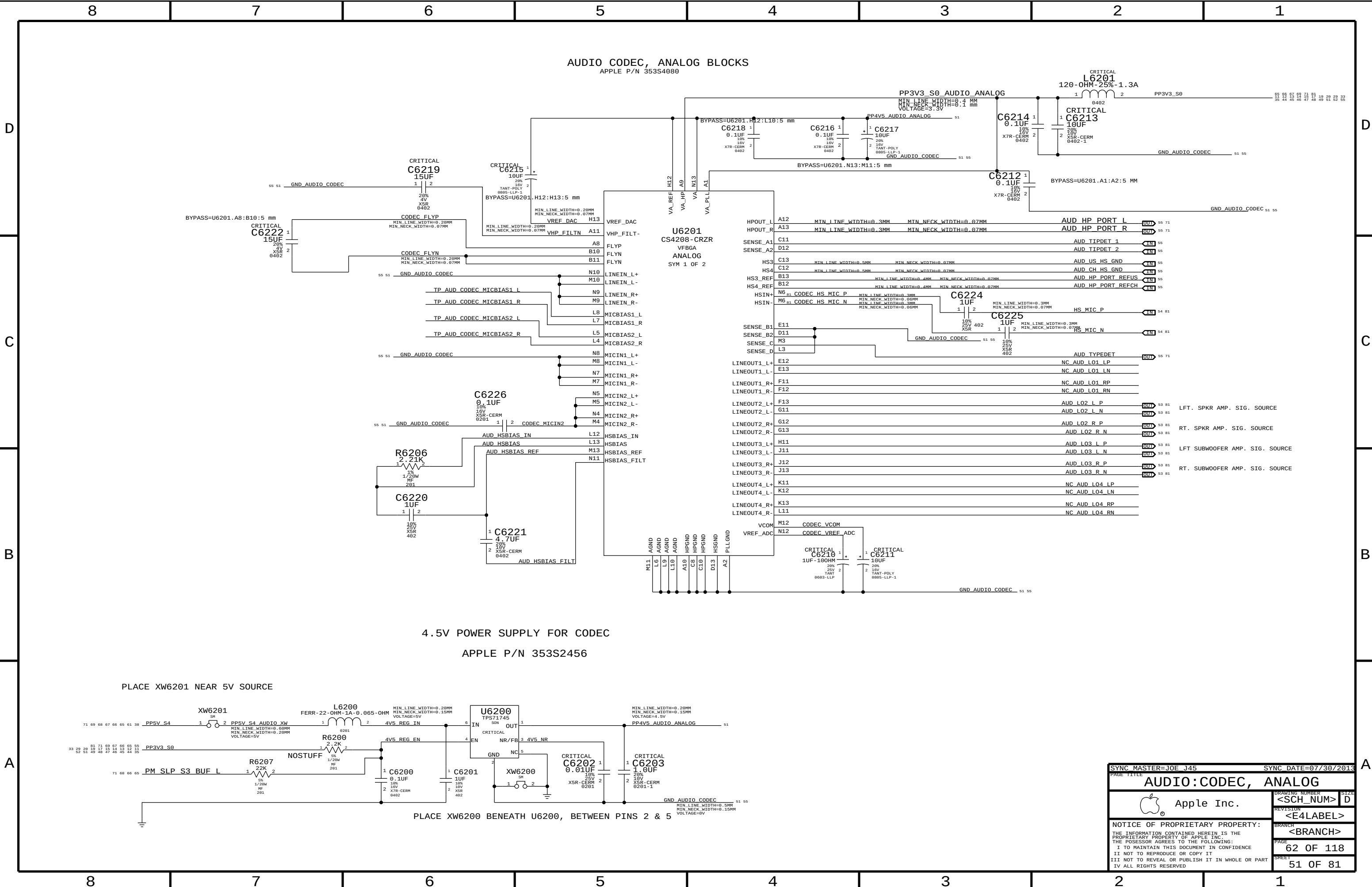
LPC+SPI Connector



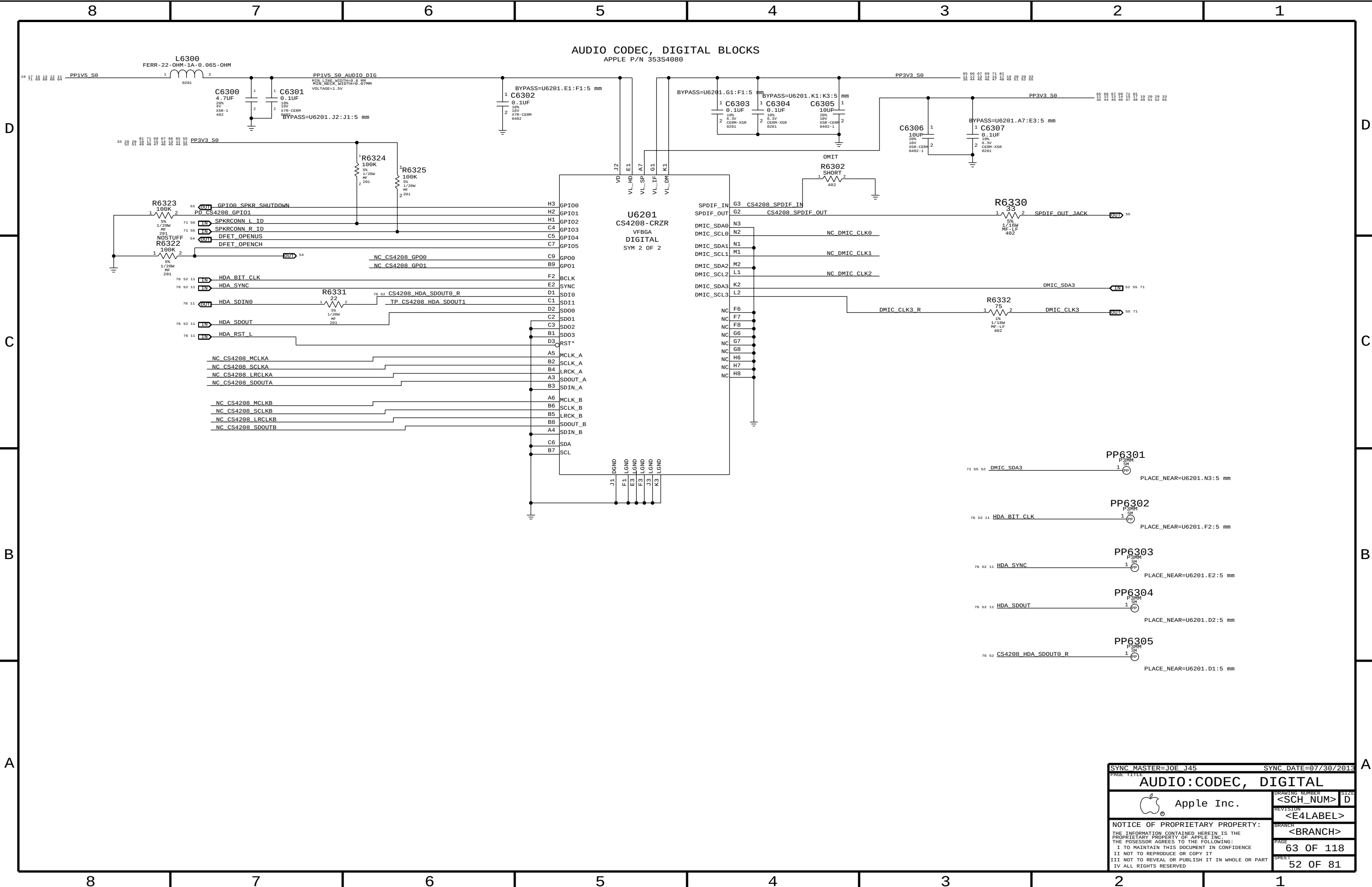
SPI ROM



SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
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SPI ROM / LPC+SPI Conn.		DRAWING NUMBER	
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		SHEET	
		50 OF 81	

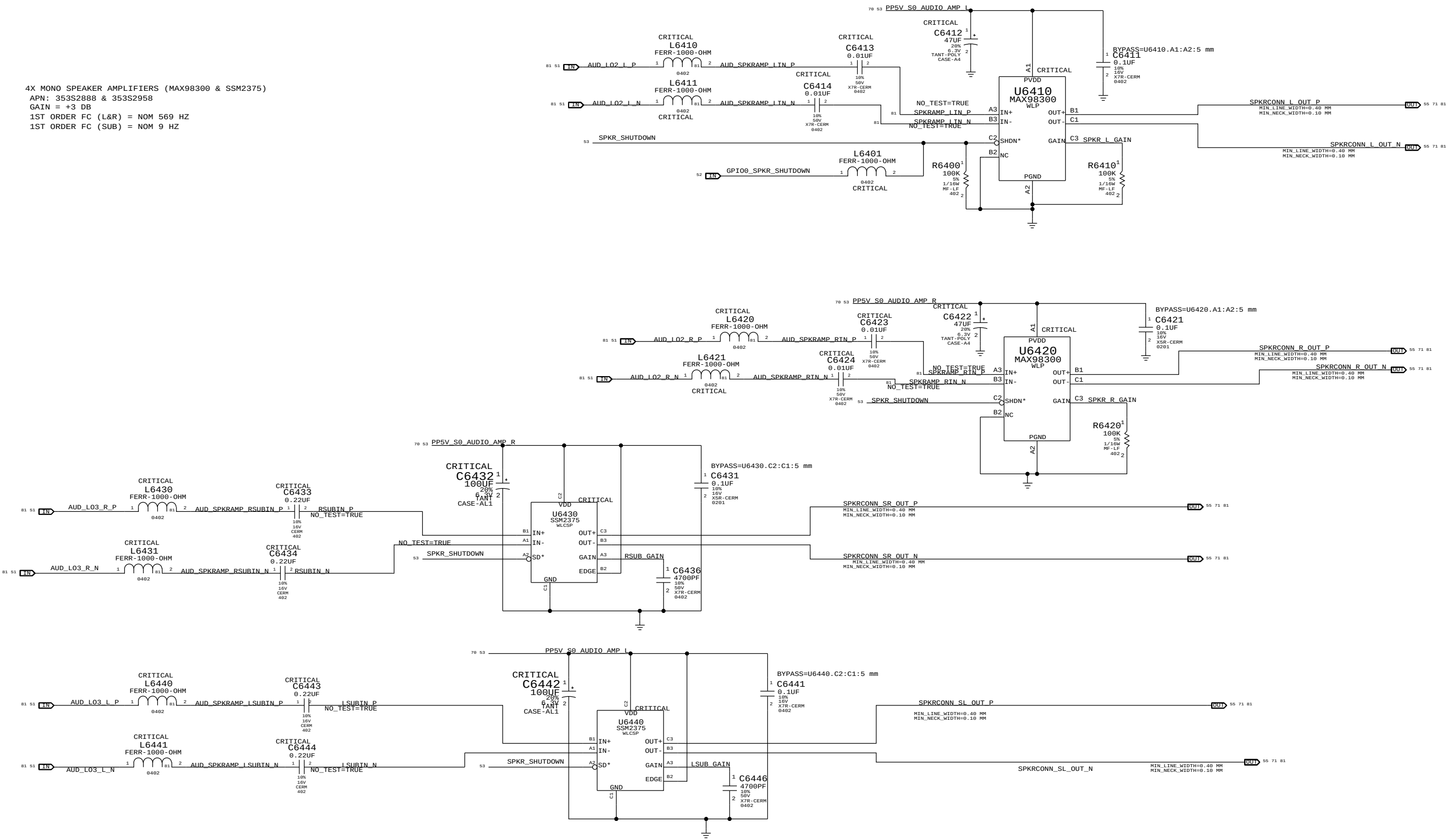


SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE		DRAWING NUMBER	
AUDIO:CODEC, ANALOG		<SCH_NUM> D	
Apple Inc.		REVISION	
		<E4LABEL>	
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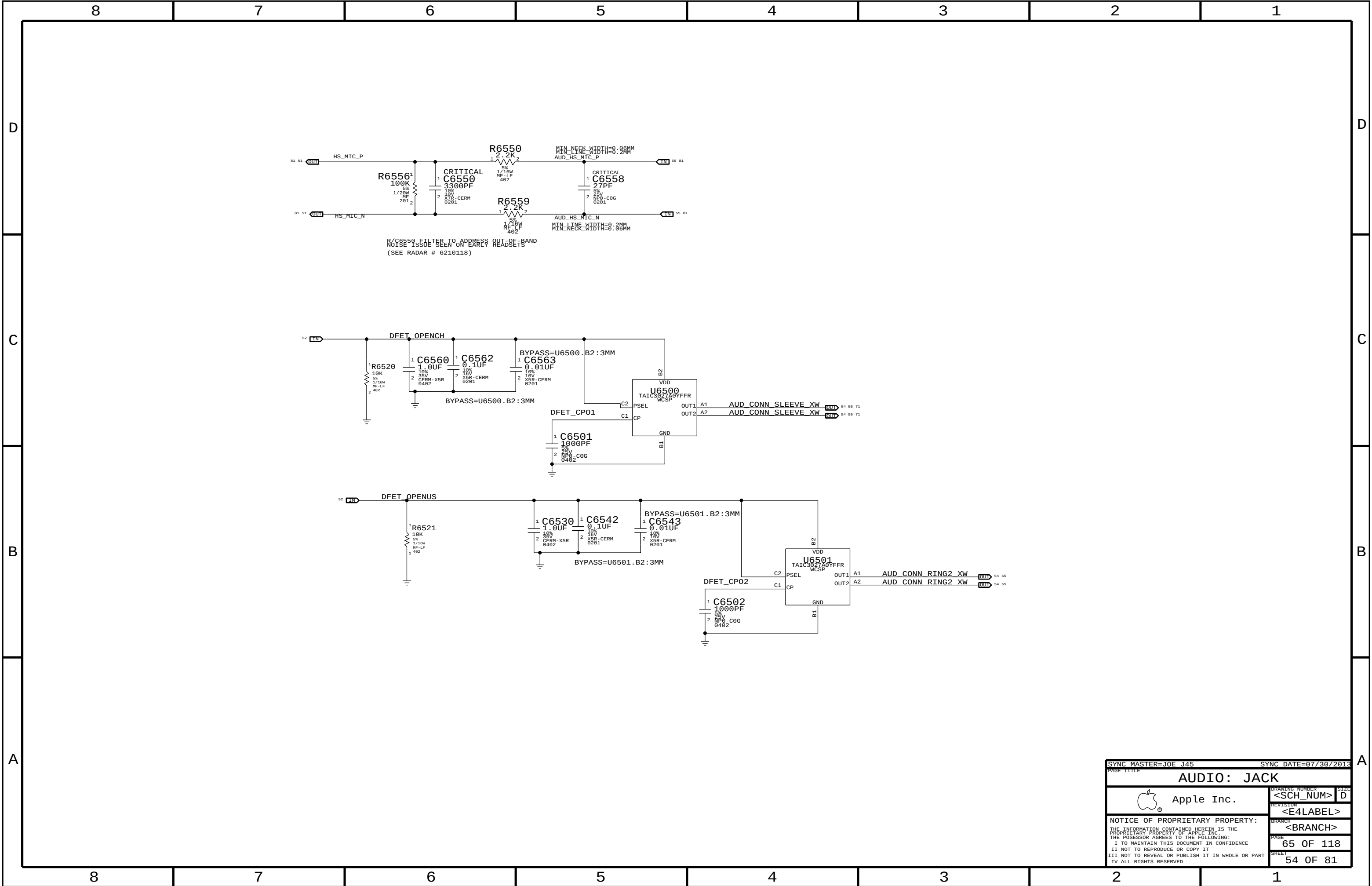


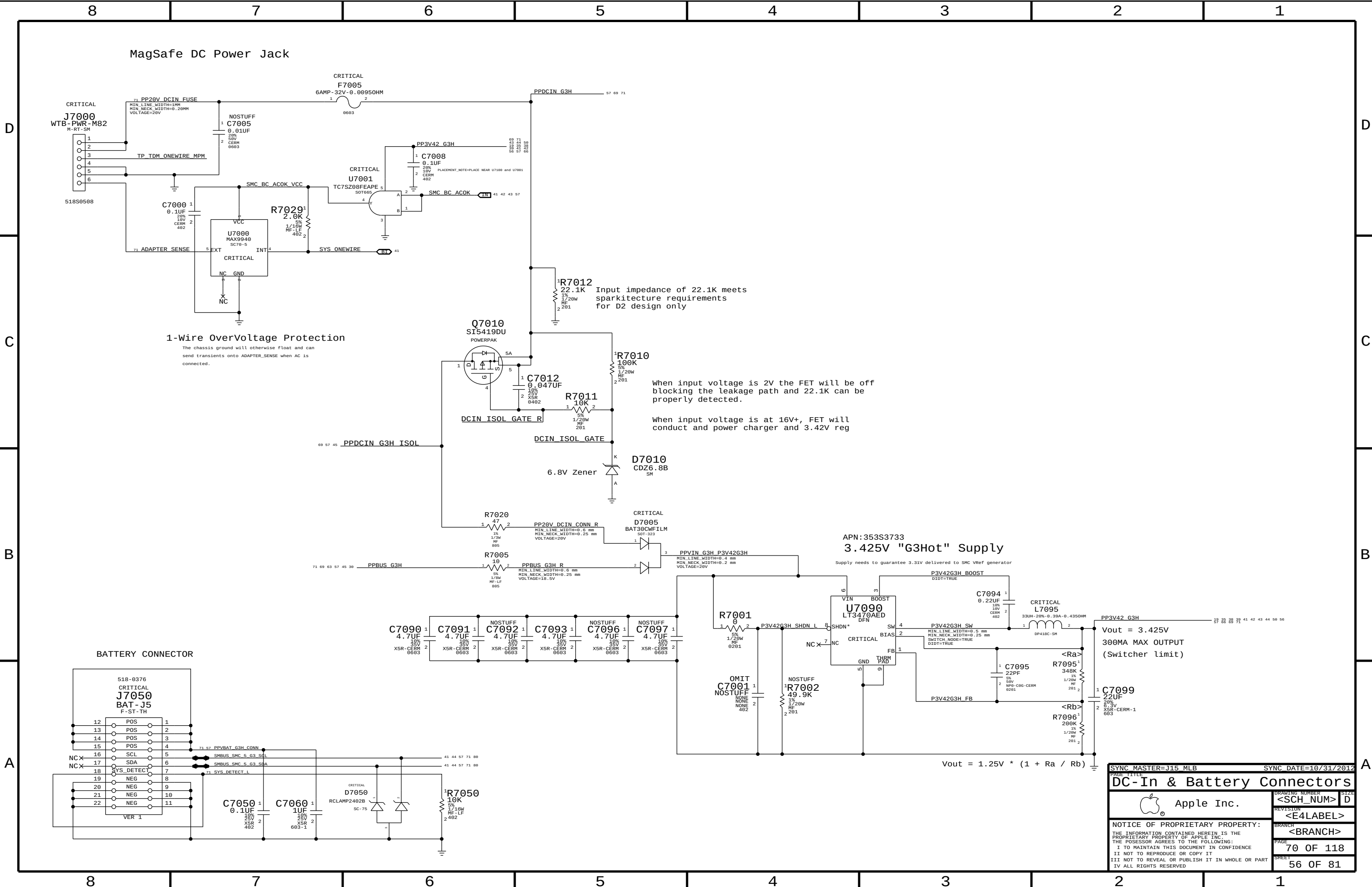
SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO:CODEC, DIGITAL			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	63 OF 118
SHEET	52 OF 81		

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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		BRANCH	
		<BRANCH>	
		PAGE	64 OF 118
		SHEET	53 OF 81





MagSafe DC Power Jack

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

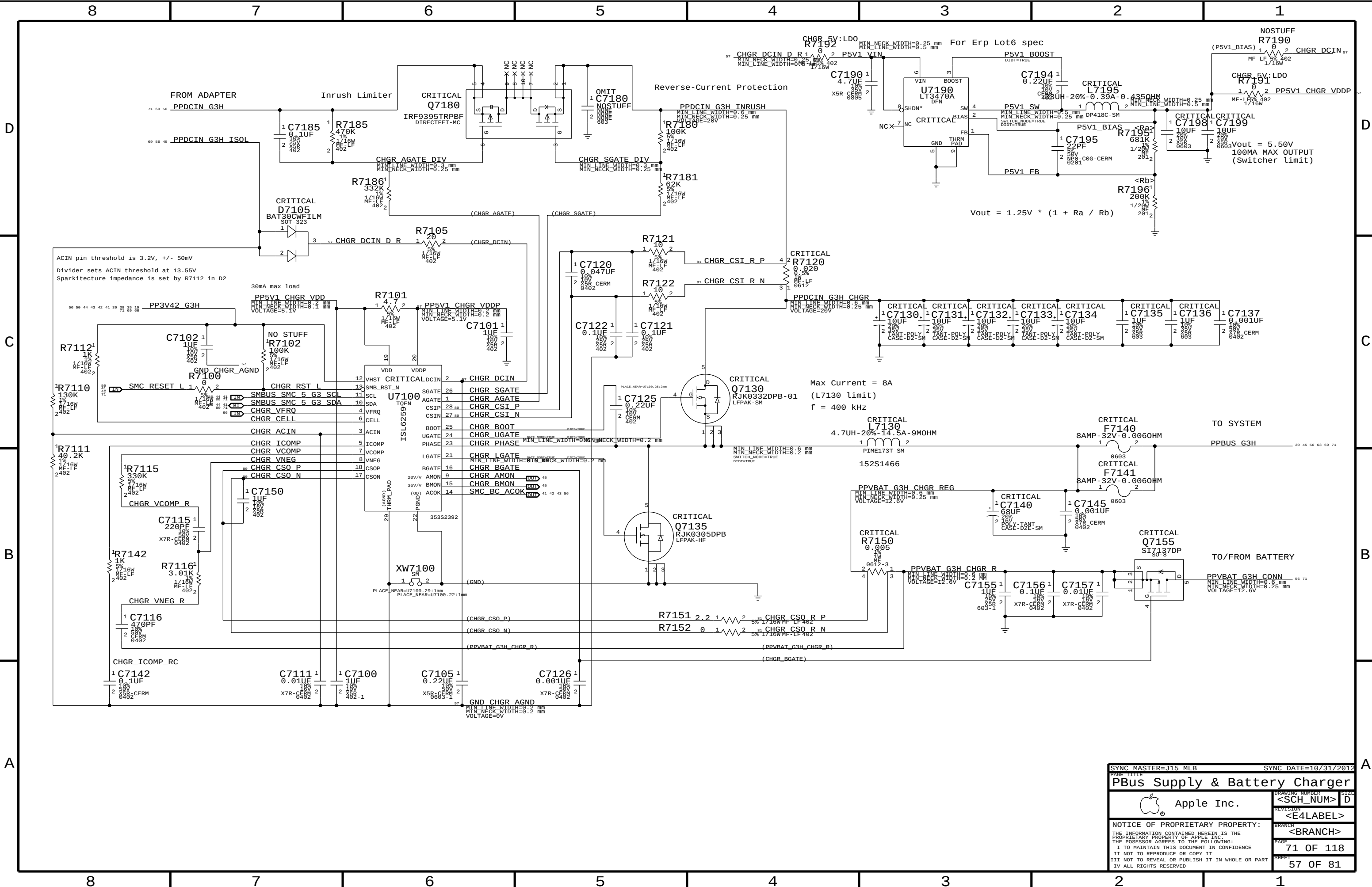
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

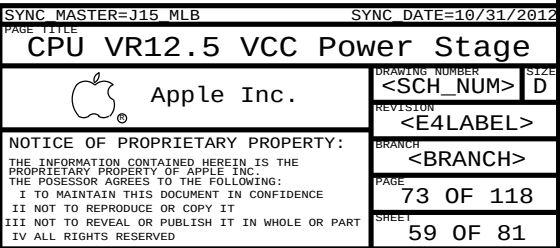
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

PAGE TITLE		SYNC DATE=10/31/2012	
DC-In & Battery Connectors		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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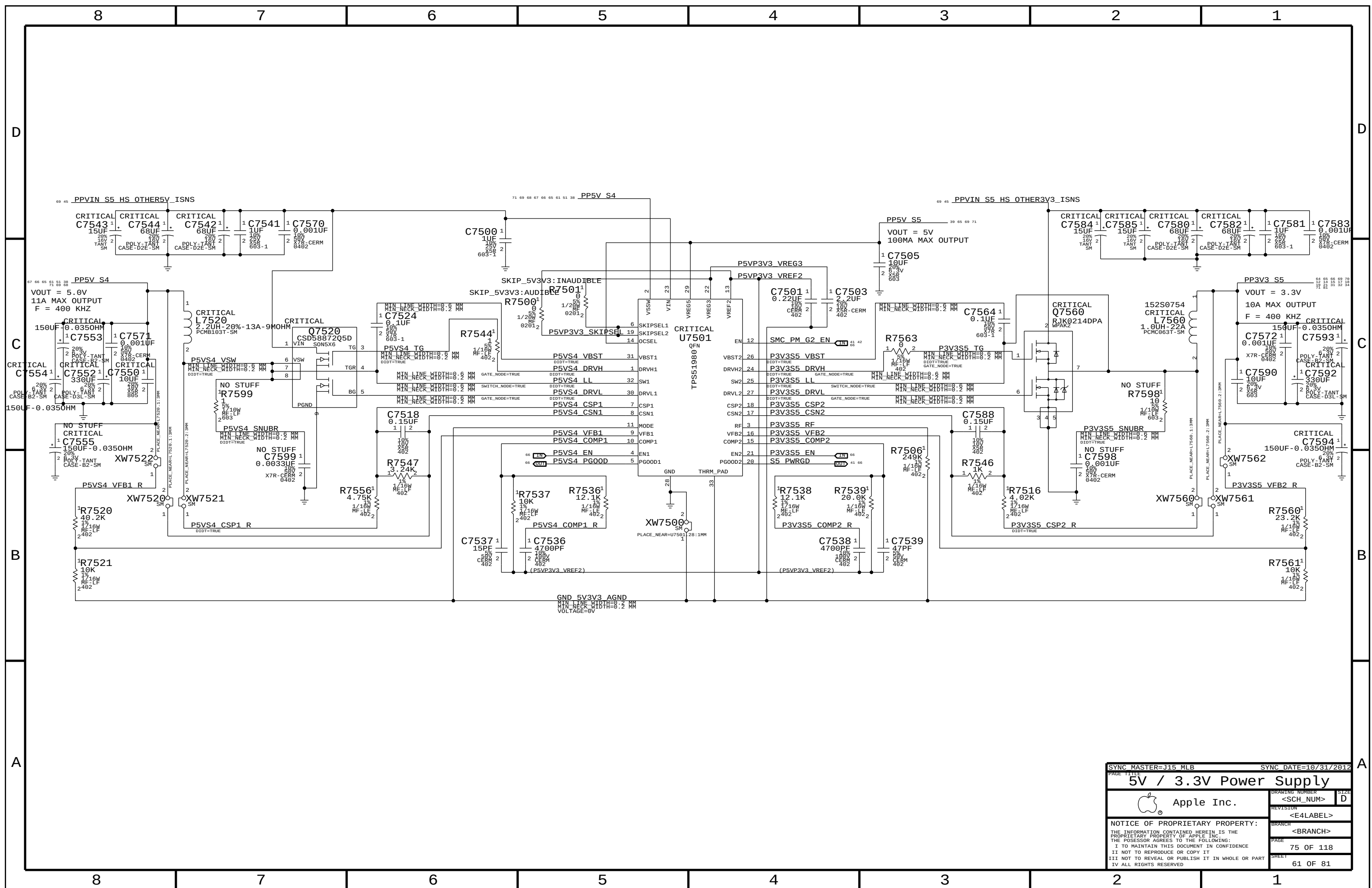


SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012		
PAGE TITLE				
PBus Supply & Battery Charger				
 Apple Inc.	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
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BRANCH		<BRANCH>		
PAGE		71 OF 118		
SHEET		57 OF 81		

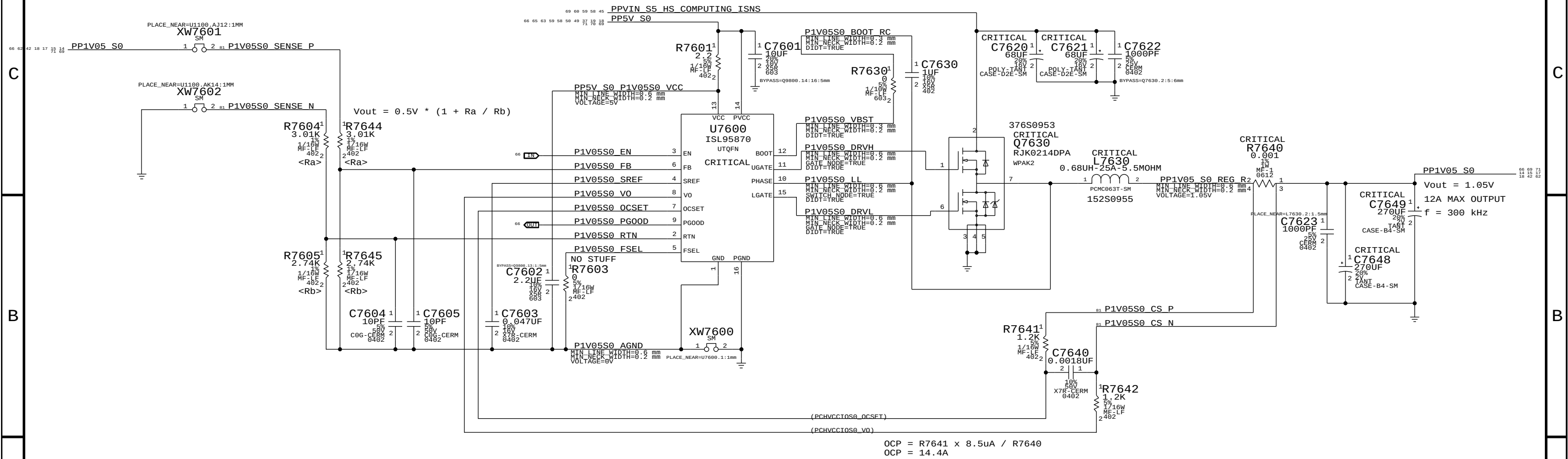


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1V05 S0 REGULATOR



SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012		
PAGE TITLE				
1V05V POWER SUPPLY				
 Apple Inc.		DRAWING NUMBER		SIZE
		<SCH_NUM>		D
		REVISION		<E4LABEL>
		BRANCH		<BRANCH>
PAGE				76 OF 118
SHEET				62 OF 81
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Power aliases required by this page:

- PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT:PROD - Stuffs 0 ohm series R for production

PLACE_NEAR=L7710.2:3MM

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

CRITICAL
D7701
POWER1-123

C7715, C7716 SHOULD BE PLACED MIRRORED

C7718, C7719 SHOULD BE PLACED MIRRORED

S0_LCDBKLT_PWR_SW

WIDTH=0.25 MM

MIN_NBR WIDTH=0.25 MM

MIN_NBR WIDTH=0.25 MM

VOLTAGE=55V

7717

DFLS2100

CRITICAL
1 C7715 2.2UF
100V
X7R
1210-1

CRITICAL
1 C7716 2.2UF
100V
X7R
1210-1

CRITICAL
1 C7718 2.2UF
100V
X7R
1210-1

CRITICAL
1 C7719 2.2UF
100V
X7R
1210-1

1 C7717 1000PF
100V
X7R-CERM
0603

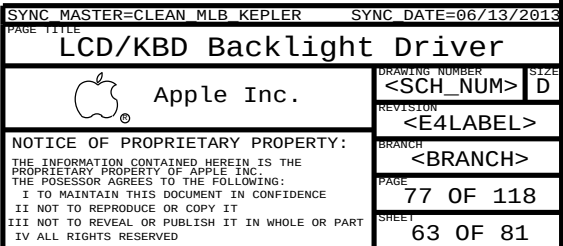
PLACE_NEAR=D7701.K:3MM

PLACE_NEAR=D7701.K:5MM

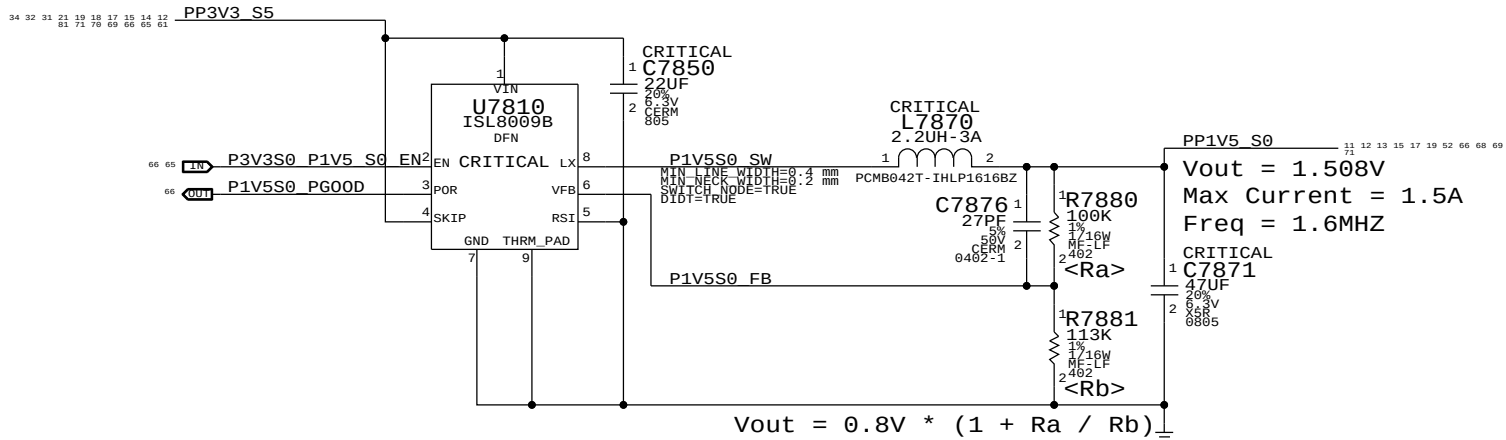
PLACE_NEAR=D7701.K:3MM

PLACE_NEAR=D7701.K:5MM

PLACE_NEAR=R7708.1:5MM

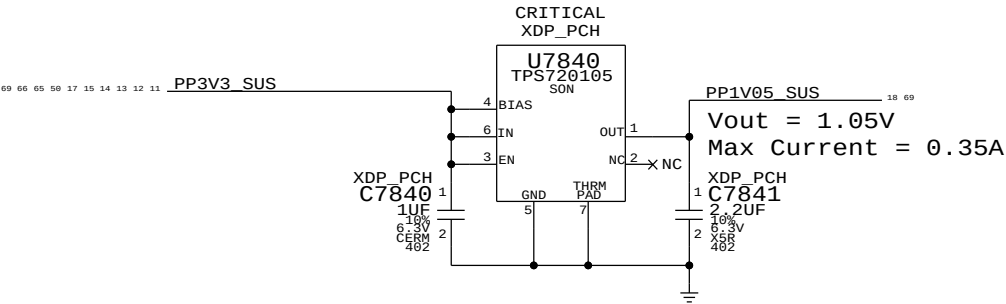


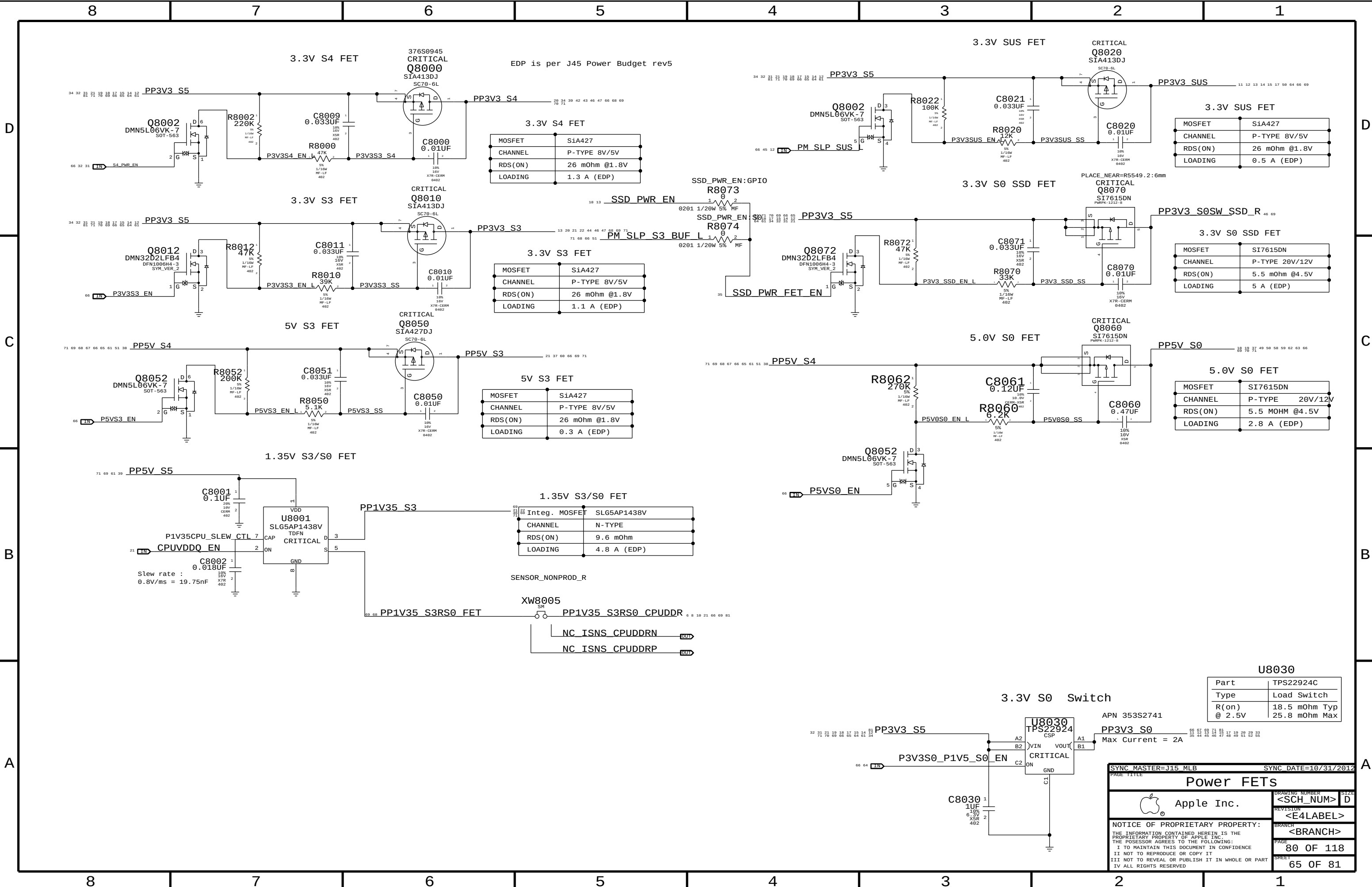
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.





EDP is per J45 Power Budget rev5

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R

PP1V35 S3RS0 FET	NC ISNS_CPUDDR
PP1V35 S3RS0 FET	NC ISNS_CPUDDR

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

SYNC MASTER=J15 MLB

SYNC DATE=10/31/2012

Power FETs

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PAGE

80 OF 118

SHEET

65 OF 81

D

C

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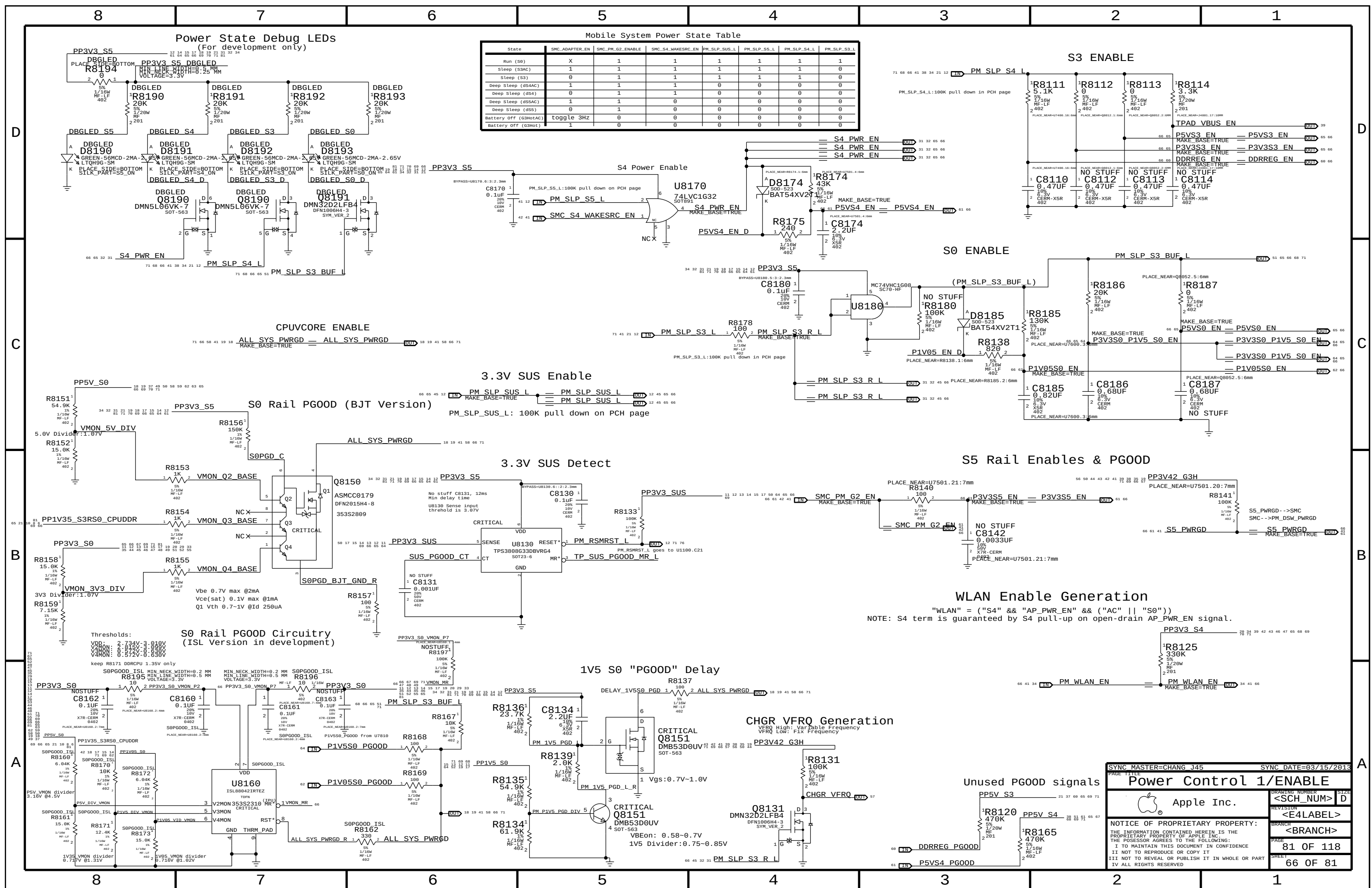
A

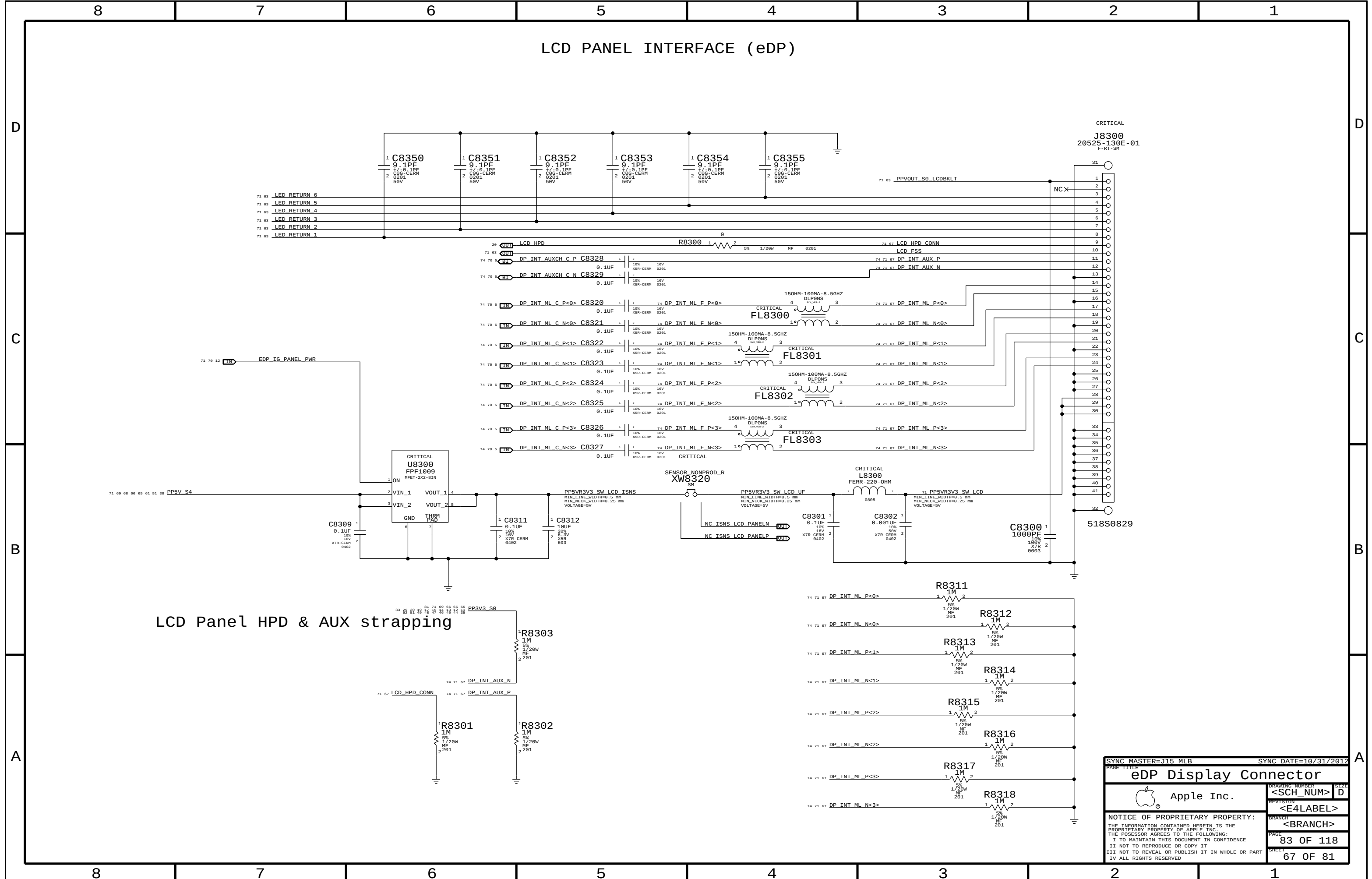
D

C

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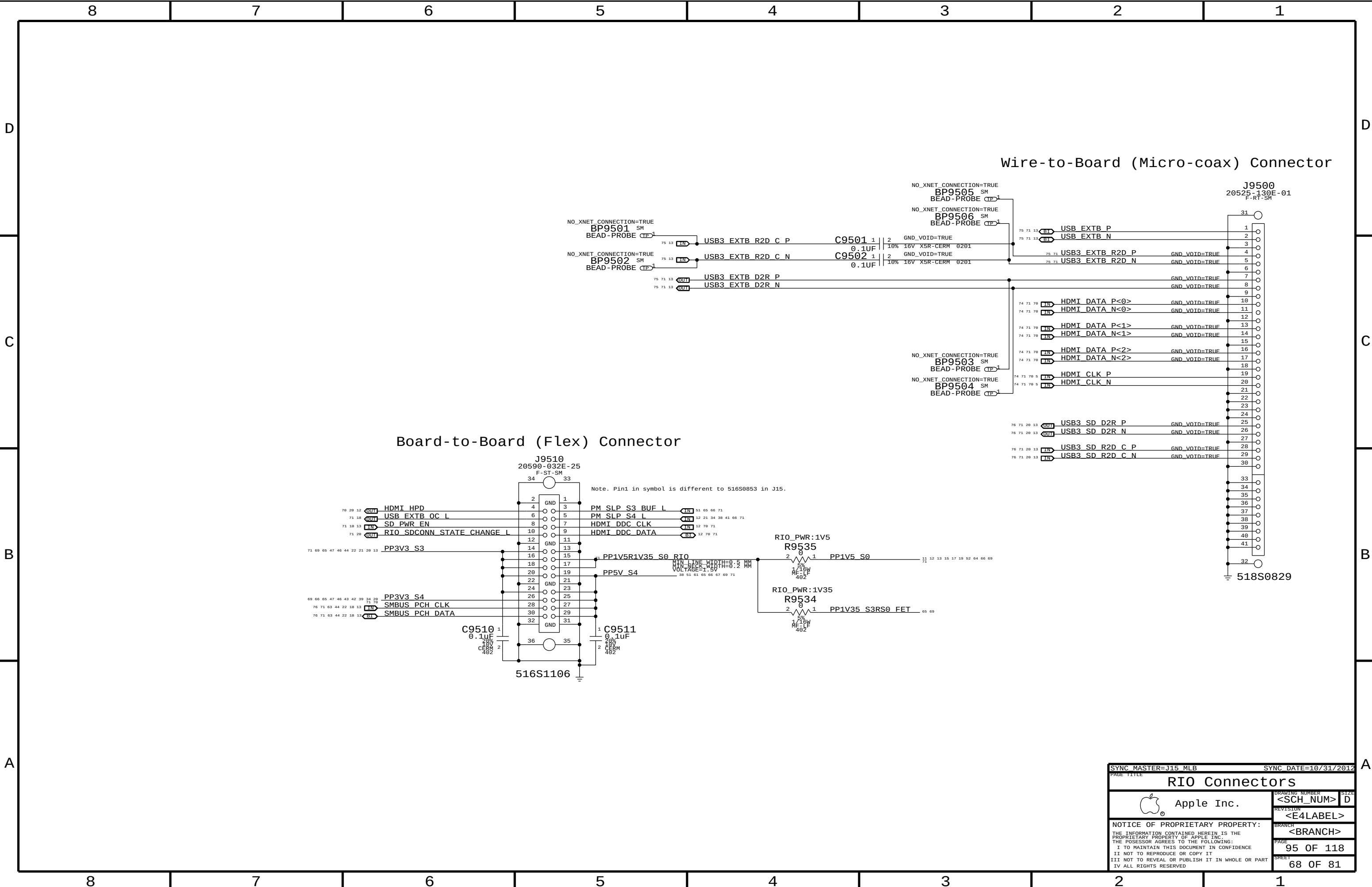
[illegible][illegible]

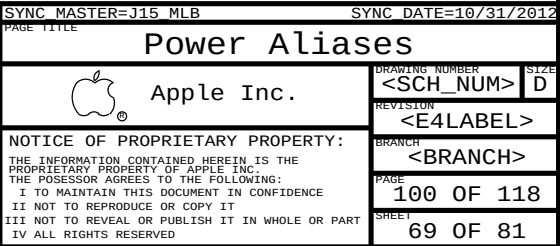
The diagram illustrates the electrical interface between a system and an LCD panel. Key components include:

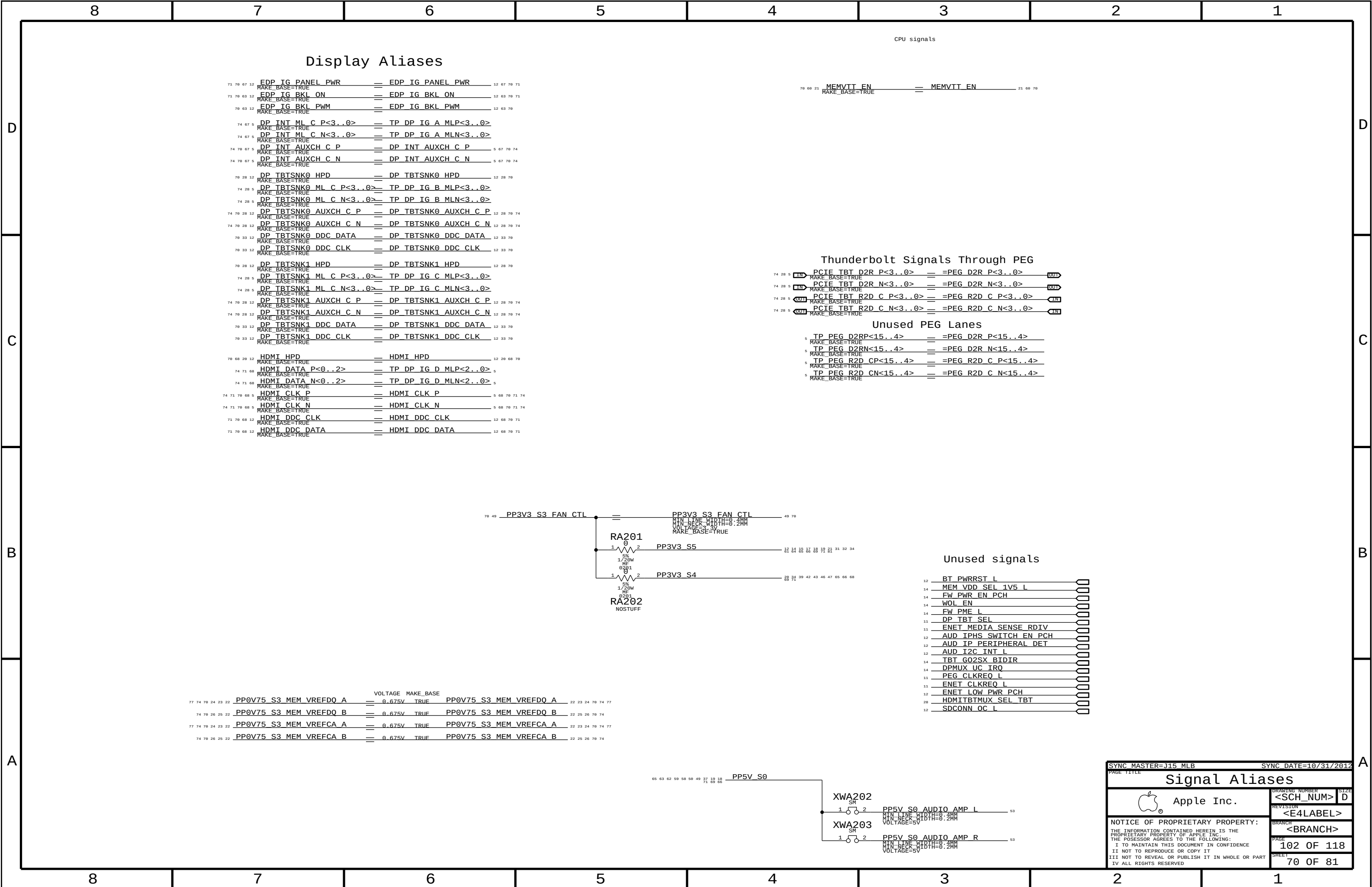
- Capacitors:** C8350-C8355 (0.1µF, 50V), C8309 (0.1µF, 10V), C8311 (0.1µF, 10V), C8312 (0.1µF, 10V), C8301 (0.1µF, 10V), C8302 (0.001µF, 10V), C8300 (1000PF, 10V), C8320-C8327 (0.1µF, 10V).
- Resistors:** R8300 (1M, 1/20W), R8301 (1M, 1/20W), R8302 (1M, 1/20W), R8303 (1M, 1/20W), R8311 (1M, 1/20W), R8312 (1M, 1/20W), R8313 (1M, 1/20W), R8314 (1M, 1/20W), R8315 (1M, 1/20W), R8316 (1M, 1/20W), R8317 (1M, 1/20W), R8318 (1M, 1/20W).
- Inductors:** FL8300, FL8301, FL8302, FL8303 (150OHM-100MA-8.5GHZ DLPBNS).
- Connectors:** J8300 (20525-130E-01 F-RT-SM), J8301 (20525-130E-01 F-RT-SM).
- Other Components:** U8300 (FPF1009), XW8320 (SENSOR_NONPROD_R), L8300 (FERR-220-OHM).

The diagram also shows connections to various power and ground planes, including PP5V_S4, PP3V3_S0, and various ground points. A section labeled "LCD Panel HPD & AUX strapping" shows connections for HPD and AUX signals. A table at the bottom right contains metadata:

SYNC MASTER=J15 MLB	SYNC DATE=10/31/2012
eDP Display Connector	
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83 OF 118	67 OF 81







Functional Test Points

J3501 - airport	
TRUE AP CLKREQ0 Q L	34
TRUE AP RESET CONN L	34
TRUE PCIE AP D2R PI N	34 76
TRUE PCIE AP D2R PI P	34 76
TRUE PCIE AP R2D N	34 76
TRUE PCIE AP R2D P	34 76
TRUE PCIE CLK100M AP CONN N	34 76
TRUE PCIE CLK100M AP CONN P	34 76
TRUE PCIE WAKE L	12 34 36 76
TRUE PP3V3 S3RS4 BT F	34
TRUE PP3V3 WLAN	34 42
TRUE USB BT CONN N	34 75
TRUE USB BT CONN P	34 75
TRUE WIFI EVENT L	34 41 42
TRUE GND	4X

J4002 - Camera	
TRUE MIPI CLK CONN N	37 79
TRUE MIPI CLK CONN P	37 79
TRUE CAM SENSOR WAKE L CONN	37
TRUE MIPI DATA CONN N	37 79
TRUE MIPI DATA CONN P	37 79
TRUE SMBUS SMC 0 S0 SDA	37 41 44 48 88
TRUE SMBUS SMC 0 S0 SCL	37 41 44 48 88
TRUE I2C CAM SCK	36 37
TRUE I2C CAM SDA	36 37
TRUE PP5V S3RS0 ALSCAM F	37
TRUE GND	

J9500 - rio coax	
TRUE HDMI CLK N	5 68 70 74
TRUE HDMI CLK P	5 68 70 74
TRUE HDMI DATA N<0>	68 70 74
TRUE HDMI DATA N<1>	68 70 74
TRUE HDMI DATA N<2>	68 70 74
TRUE HDMI DATA P<0>	68 70 74
TRUE HDMI DATA P<1>	68 70 74
TRUE HDMI DATA P<2>	68 70 74

TRUE USB3 SD D2R N	13 20 68 76
TRUE USB3 SD D2R P	13 20 68 76
TRUE USB3 SD R2D C N	13 20 68 76
TRUE USB3 SD R2D C P	13 20 68 76
TRUE USB3 EXTB D2R N	13 68 75
TRUE USB3 EXTB D2R P	13 68 75
TRUE USB3 EXTB R2D N	68 75
TRUE USB3 EXTB R2D P	68 75
TRUE USB EXTB N	13 68 75
TRUE USB EXTB P	13 68 75
TRUE GND	19X

J9510 - rio flex	
TRUE SD PWR EN	13 18 68
TRUE PP1V5R1V35 S0 RIO	68
TRUE HDMI DDC CLK	12 68 70
TRUE HDMI DDC DATA	12 68 70
TRUE HDMI HPD L	
TRUE SMBUS PCH CLK	13 18 22 44 63 68 76
TRUE SMBUS PCH DATA	13 18 22 44 63 68 76
TRUE PM SLP S3 BUF L	51 65 66 68
TRUE PM SLP S4 L	12 21 34 38 41 66 68
TRUE PP3V3 S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE PP3V3 S4	20 21 22 44 46 47 65 66 68
TRUE PP5V S4	5X 38 51 61 65 66 67 68 69
TRUE RIO SDCONN STATE CHANGE L	26 68
TRUE USB EXTB OC L	18 68
TRUE GND	10X

J5150 - hall effect	
TRUE PP3V42 G3H	19 35 38 39 41 42 43 44 50 56
TRUE SMC LID R	43
TRUE GND	

J6050 - left fan	
TRUE FAN LT PWM	49
TRUE FAN LT TACH	49
TRUE PP5V S0	3X 18 19 37 49 50 58 59 62 63
TRUE GND	5X

J6060 - right fan	
TRUE FAN RT PWM	49
TRUE FAN RT TACH	49
TRUE PP5V S0	3X 18 19 37 49 50 58 59 62 63
TRUE GND	5X

J6100 - lpc + spi	
TRUE LPCPLUS GPIO	14 50
TRUE LPCPLUS RESET L	20 50 76
TRUE LPC AD<0>	13 41 50 76
TRUE LPC AD<1>	13 41 50 76
TRUE LPC AD<2>	13 41 50 76
TRUE LPC AD<3>	13 41 50 76
TRUE LPC CLK33M LPCPLUS	19 50 76
TRUE LPC FRAME L	13 41 50 76
TRUE LPC PWRDWN L	12 20 41 50
TRUE LPC SERIRQ	13 41 50
TRUE PM CLKRUN L	12 41 50
TRUE PP5V S0	18 19 37 49 50 58 59 62 63 65
TRUE SMC RESET L	41 42 50 57
TRUE SMC ROMBOOT	42 50
TRUE SMC RX L	41 42 50
TRUE SMC TCK	41 42 50
TRUE SMC TDI	41 42 50
TRUE SMC TDO	41 42 50
TRUE SMC TMS	41 42 50
TRUE SMC TX L	41 42 50
TRUE SPIROM USE MLB	14 50
TRUE SPI ALT CLK	50
TRUE SPI ALT CS L	50
TRUE SPI ALT MISO	50
TRUE SPI ALT MOSI	50
TRUE TP SMC MD1	50
TRUE TP SMC TRST L	50
TRUE GND	2X

J4800 - ipd flex	
TRUE Z2 CS L	39
TRUE Z2 MOSI	39
TRUE Z2 MISO	39
TRUE Z2 SCLK	39
TRUE Z2 HOST INTN	39
TRUE Z2 CLKIN	39
TRUE Z2 KEY ACT L	39
TRUE PS0C F CS L	39
TRUE PICKB L	39
TRUE PS0C MOSI	39
TRUE PS0C MISO	39
TRUE PS0C SCLK	39
TRUE SMBUS SMC 2 S3 SCL	39 41 44 88
TRUE SMBUS SMC 2 S3 SDA	39 41 44 88
TRUE SMC LID	39 41 42 43
TRUE SMC T101 COM 1	
TRUE PP3V3 S4	20 34 39 42 43 46 47 65 66 68
TRUE PP5V S5	39 61 65 69 71
TRUE GND	2X

J4813 - keyboard	
TRUE PP3V3 S4	20 34 39 42 43 46 47 65 66 68
TRUE PP3V42 G3H	19 35 38 39 41 42 43 44 50 56
TRUE WS CONTROL KBD	39
TRUE WS KBD1	39
TRUE WS KBD10	39
TRUE WS KBD11	39
TRUE WS KBD12	39
TRUE WS KBD13	39
TRUE WS KBD14	39
TRUE WS KBD15 CAP	39
TRUE WS KBD16 NUM	39
TRUE WS KBD17	39
TRUE WS KBD18	39
TRUE WS KBD19	39
TRUE WS KBD2	39
TRUE WS KBD20	39
TRUE WS KBD21	39
TRUE WS KBD22	39
TRUE WS KBD23	39
TRUE WS KBD3	39
TRUE WS KBD4	39
TRUE WS KBD5	39
TRUE WS KBD6	39
TRUE WS KBD7	39
TRUE WS KBD8	39
TRUE WS KBD9	39
TRUE WS KBD ONOFF L	39
TRUE WS LEFT OPTION KBD	39
TRUE WS LEFT SHIFT KBD	39
TRUE GND	2X

J4915 - kbd bklt	
TRUE KBDBKLT RETURN1	2X 40 63
TRUE KBDBKLT RETURN2	2X 40 63
TRUE PPVOUT S0 KBDBKLT	40 63
TRUE GND	4X

J6701 - audio flex	
TRUE AUD_HP_PORT L	51 55
TRUE AUD_HP_PORT R	51 55
TRUE AUD SPDIF OUT JACK	
TRUE AUD TIPDET INV	
TRUE AUD TYPEDET	51 55
TRUE AUD CONN MIC XW	4X
TRUE CH HS MIC	
TRUE PP3V3 S0	18 19 37 49 50 58 59 62 63 65
TRUE AUD CONN SLEEVE XW	4X 54 55
TRUE US HS MIC	
TRUE GND	2X GND

J6601 - mic	
TRUE DMIC CLK3	52 55
TRUE PP3V3 S0	18 19 37 49 50 58 59 62 63 65
TRUE DMIC SDA2	55
TRUE DMIC SDA3	52 55
TRUE GND	

J6602 - L speaker	
TRUE SPKRCONN L ID	52 55
TRUE SPKRCONN L OUT N	53 55 81
TRUE SPKRCONN L OUT P	53 55 81
TRUE SPKRCONN SL OUT N	53 55 81
TRUE SPKRCONN SL OUT P	53 55 81
TRUE GND	

J6603 - R speaker	
TRUE SPKRCONN R ID	52 55
TRUE SPKRCONN R OUT N	53 55 81
TRUE SPKRCONN R OUT P	53 55 81
TRUE SPKRCONN SR OUT N	53 55 81
TRUE SPKRCONN SR OUT P	53 55 81
TRUE GND	

J7000 - DC PWR	
TRUE ADAPTER SENSE	56
TRUE PP20V DCIN FUSE	2X 56
TRUE GND	2X

J7050 - battery	
TRUE PPVBAT G3H CONN	8X 56 57
TRUE SMBUS SMC 5 G3 SCL	41 44 56 57 80
TRUE SMBUS SMC 5 G3 SDA	41 44 56 57 80
TRUE SYS DETECT L	56
TRUE GND	8X

J8300 - eDP	
TRUE DP INT AUX N	67 74
TRUE DP INT AUX P	67 74
TRUE DP INT ML N<0>	67 74
TRUE DP INT ML N<1>	67 74
TRUE DP INT ML N<2>	67 74
TRUE DP INT ML N<3>	67 74
TRUE DP INT ML P<0>	67 74
TRUE DP INT ML P<1>	67 74
TRUE DP INT ML P<2>	67 74
TRUE DP INT ML P<3>	67 74
TRUE LCD FSS	63 67
TRUE LCD HPD CONN	67
TRUE LED RETURN 1	63 67
TRUE LED RETURN 2	63 67
TRUE LED RETURN 3	63 67
TRUE LED RETURN 4	63 67
TRUE LED RETURN 5	63 67
TRUE LED RETURN 6	63 67
TRUE PP5VR3V3 SW LCD	3X 67
TRUE PPVOUT S0 LCDBKLT	63 67
TRUE GND	16X

Power Rails	
TRUE PM SLP S3 L	12 21 41 66
TRUE PPVTT S0 DDR	21 27 60 69
TRUE PP3V3 S0	60 66 67 69 71 81
TRUE PP3V3 S3	35 44 45 46 47 48 49 51 52 55
TRUE PP3V3 S5	72 20 21 22 44 46 47 65 68 69
TRUE PP3V3 S5 AVREF SMC	31 32 34
TRUE PP3V42 G3H	41 42
TRUE PP5V S0	19 35 38 39 41 42 43 44 50 56
TRUE PP5V S3	21 37 60 65 66 69
TRUE PP5V S5	39 61 65 69 71
TRUE PPBUS G3H	39 45 56 57 63 69
TRUE PPDCIN G3H	56 57 69
TRUE PPVCC S0 CPU	6 8 10 46 50 69
TRUE PPVTIDDR S3	60 69
TRUE PP3V3 S0SW SSD	35 46 69
TRUE PP1V5 S0	12 13 15 17 19 52 64 66 68
TRUE PP1V35 S3	21 22 46 60 65 69

XDP	
TRUE XDP CPU TCK	6 18 74
TRUE XDP PCH TCK	11 18
TRUE XDP CPU TDI	6 18 74
TRUE XDP CPU TDO	6 18 74
TRUE XDP CPUPCH TRST L	6 18 74
TRUE XDP CPU TMS	6 18 74
TRUE XDP PCH TMS	11 18
TRUE XDP PCH TDI	11 18
TRUE XDP PCH TDO	11 18
TRUE XDP CPU PREQ L	6 18 74
TRUE XDP CPU PRDY L	6 18 74
TRUE PM RSMRST L	12 66 76
TRUE PM PCH PWROK	12 19 76
TRUE PM SYSRST L	12 19 41 76
TRUE CPU CFG<3>	6 18 74
TRUE PP1V05 S0	14 15 17 18 42 62 66 69
TRUE GND	2X GND

Power Sequence	
TRUE SMC ONOFF L	39 41 42
TRUE PM DSW PWRGD	12 41 76
TRUE ALL SYS PWRGD	18 19 41 58 66
TRUE PM PCH SYS PWROK	12 18 19 41 76
TRUE PLT RESET L	12 18 20 21
TRUE EDP IG PANEL PWR	12 67 70
TRUE EDP IG BKL ON	12 63 70

SYNC MASTER=J15 MLB

SYNC DATE=10/31/2012

Functional Test Points

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PAGE
104 OF 118

SHEET
71 OF 81

8	7	6	5	4	3	2	1					
NC NO_TESTS												
D	PCH		Thunderbolt		PLACEABLE BEAD-PROBES FOR TBT							
	NO_TEST MAKE_BASE		NO_TEST MAKE_BASE									
	72 13	NC USB3 SPARE D2RN	== TRUE TRUE	NC USB3 SPARE D2RN	13 72	72 28	NC TBT XTAL250UT	== TRUE TRUE	NC TBT XTAL250UT	28 72		
	72 13	NC USB3 SPARE D2RP	== TRUE TRUE	NC USB3 SPARE D2RP	13 72							
	72 13	NC USB3 SPARE R2D CN	== TRUE TRUE	NC USB3 SPARE R2D CN	13 72							
	72 13	NC USB3 SPARE R2D CP	== TRUE TRUE	NC USB3 SPARE R2D CP	13 72							
	75 72 13	NC USB3 EXTC D2RN	== TRUE TRUE	NC USB3 EXTC D2RN	13 72 75							
	75 72 13	NC USB3 EXTC D2RP	== TRUE TRUE	NC USB3 EXTC D2RP	13 72 75							
	75 72 13	NC USB3 EXTC R2D CN	== TRUE TRUE	NC USB3 EXTC R2D CN	13 72 75							
	75 72 13	NC USB3 EXTC R2D CP	== TRUE TRUE	NC USB3 EXTC R2D CP	13 72 75							
	75 72 13	NC USB3 EXT D2RN	== TRUE TRUE	NC USB3 EXT D2RN	13 72 75							
	75 72 13	NC USB3 EXT D2RP	== TRUE TRUE	NC USB3 EXT D2RP	13 72 75							
	75 72 13	NC USB3 EXT R2D CN	== TRUE TRUE	NC USB3 EXT R2D CN	13 72 75							
	75 72 13	NC USB3 EXT R2D CP	== TRUE TRUE	NC USB3 EXT R2D CP	13 72 75							
	72	NC PCIE ENET D2RN	== TRUE TRUE	NC PCIE ENET D2RN	72							
	72	NC PCIE ENET D2RP	== TRUE TRUE	NC PCIE ENET D2RP	72							
	72	NC PCIE ENET R2D CN	== TRUE TRUE	NC PCIE ENET R2D CN	72							
	72	NC PCIE ENET R2D CP	== TRUE TRUE	NC PCIE ENET R2D CP	72							
	75 72 11	NC SATA A D2RN	== TRUE TRUE	NC SATA A D2RN	11 72 75							
	75 72 11	NC SATA A D2RP	== TRUE TRUE	NC SATA A D2RP	11 72 75							
	75 72 11	NC SATA A R2D CN	== TRUE TRUE	NC SATA A R2D CN	11 72 75							
	75 72 11	NC SATA A R2D CP	== TRUE TRUE	NC SATA A R2D CP	11 72 75							
	75 72 11	NC SATA B D2RN	== TRUE TRUE	NC SATA B D2RN	11 72 75							
	75 72 11	NC SATA B D2RP	== TRUE TRUE	NC SATA B D2RP	11 72 75							
	75 72 11	NC SATA B R2D CN	== TRUE TRUE	NC SATA B R2D CN	11 72 75							
	75 72 11	NC SATA B R2D CP	== TRUE TRUE	NC SATA B R2D CP	11 72 75							
	75 72 11	NC SATA ODD D2RN	== TRUE TRUE	NC SATA ODD D2RN	11 72 75							
	75 72 11	NC SATA ODD D2RP	== TRUE TRUE	NC SATA ODD D2RP	11 72 75							
	75 72 11	NC SATA ODD R2D CN	== TRUE TRUE	NC SATA ODD R2D CN	11 72 75							

78	31	28	TBT A R2D C P<1>	1	TP	SM	BEAD-PROBE	BPA535	NO_XNET_CONNECTION=TRUE
78	31	28	TBT A D2R P<1>	1	TP	SM	BEAD-PROBE	BPA531	NO_XNET_CONNECTION=TRUE
78	31	28	TBT A D2R N<1>	1	TP	SM	BEAD-PROBE	BPA532	NO_XNET_CONNECTION=TRUE

72	11	NC_PCIE_CLK100M_GPUN	==	TRUE	TRUE	NC_PCIE_CLK100M_GPUN	11	72
72	11	NC_PCIE_CLK100M_GPUP	==	TRUE	TRUE	NC_PCIE_CLK100M_GPUP	11	72
72	11	NC_PCIE_CLK100M_PESN	==	TRUE	TRUE	NC_PCIE_CLK100M_PESN	11	72
72	11	NC_PCIE_CLK100M_PESP	==	TRUE	TRUE	NC_PCIE_CLK100M_PESP	11	72
72	11	NC_PCIE_CLK100M_ENETSDN	==	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN	11	72
72	11	NC_PCIE_CLK100M_ENETSDP	==	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP	11	72
72	11	NC_PCIE_CLK100M_ENETN	==	TRUE	TRUE	NC_PCIE_CLK100M_ENETN	11	72
72	11	NC_PCIE_CLK100M_ENETP	==	TRUE	TRUE	NC_PCIE_CLK100M_ENETP	11	72
72	11	NC_PCIE_CLK100M_PEGBN	==	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN	11	72
72	11	NC_PCIE_CLK100M_PEGBP	==	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP	11	72
72	11	NC_PCIE_CLK100M_SWN	==	TRUE	TRUE	NC_PCIE_CLK100M_SWN	11	72
72	11	NC_PCIE_CLK100M_SWP	==	TRUE	TRUE	NC_PCIE_CLK100M_SWP	11	72

75	NC USB 4N	—	TRUE	TRUE	NC USB 4N	13	72
76	NC USB 4P	—	TRUE	TRUE	NC USB 4P	13	72

109	TRUE	DMI S2N P<3..1>	5	12	74
109	TRUE	DMI S2N N<3..1>	5	12	74
109	TRUE	DMI N2S P<3..1>	5	12	74
109	TRUE	DMI N2S N<3..1>	5	12	74

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE		NC & No Test	
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		SHEET 72 OF 81	

87654321

J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (ALL OF MM)	ALLEGRO OVERSIGHT
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA			MM	16.2
PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1X_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

87654321

PCB Rule Definitions

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<SCH_NUM> D

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110 OF 118

73 OF 81

87654321

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	28 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKL2N2S	*	=6X_DIELECTRIC	?	DMICKL2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKL2S2N	*	=3X_DIELECTRIC	?	DMICKL2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKL20THER	*	=4X_DIELECTRIC	?	DMICKL20THER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKL2N2S
CLK_DMI	DMI_S2N	*	DMICKL2S2N
CLK_DMI	*	*	DMICKL20THER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_20THER	*	=4X_DIELECTRIC	?	PEG_20THER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_20THER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3X_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DP_20THER	*	=4X_DIELECTRIC	?	DP_20THER	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKL_2CLK	*	=7X_DIELECTRIC	?	HDMICKL_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
HDMICKL_2DP	*	=4X_DIELECTRIC	?	HDMICKL_2DP	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKL_20THER	*	=7X_DIELECTRIC	?	HDMICKL_20THER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_20THER
HDMI_CLK	CLK_*	*	HDMICKL_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICKL_2DP
HDMI_CLK	*	*	HDMICKL_20THER

DisplayPort/TMDs intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDs TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTI	FDI_INT	5 12
FDI_CSYSN	CPU_50S	CPU_AGTI	FDI_CSYSN	5 12
DMI_CLK	CPU_85D	CLK_DMT	DMI_CLK100M CPU P	6 11
DMI_CLK	CPU_85D	CLK_DMT	DMI_CLK100M CPU N	6 11
CPU_CLK135_PLI	CPU_85D	CLK_PCTF	CPU_CLK135M DPLLREF N	6 11
CPU_CLK135_PLI	CPU_85D	CLK_PCTF	CPU_CLK135M DPLLREF P	6 11
CPU_CLK135_PLI	CPU_85D	CLK_PCTF	CPU_CLK135M DPLLSS N	6 11
CPU_CLK135_PLI	CPU_85D	CLK_PCTF	CPU_CLK135M DPLLSS P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCTF_85D	CLK_PCTF	NC ITPXDP CLK100MP	11 72
XDP_CLK_PCH	CLK_PCTF_85D	CLK_PCTF	NC ITPXDP CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTI	CPU_CATERR_L	6 41
CPU_PECT	CPU_45S	CPU_VTD	CPU_PECT	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTI	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTI	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_AGTI	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTI	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTI	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VTD	CPU_VIDSOUT	8 58
CPU_VTD	CPU_45S	CPU_VTD	CPU_VIDSClk	8 58
CPU_VTD	CPU_45S	CPU_VTD	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R P<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R N<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R C P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT D2R C N<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C P<3..0>	5 28 70
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML C P<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML C N<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML P<3..0>	67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML N<3..0>	67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML F P<3..0>	67
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML F N<3..0>	67
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML P<3..0>	67 71 74
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML N<3..0>	67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH C P	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH C N	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX P	67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA P<2..0>	68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA N<2..0>	68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK P	5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK N	5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C P<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C N<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C P<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C N<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE		CPU Constraints	
Apple Inc.		DRAWING NUMBER	SIZE
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP, BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP, BOTTOM	=10X_DIELECTRIC	?
SATA_20THOR	*	=4X_DIELECTRIC	?	SATA_20THOR	TOP, BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?	SATA_RCOMP	TOP, BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_25AME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_20THER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_BIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_850	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_850	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_20THER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_20THER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
	SATA_85D	SATA_R2D	NC SATA A R2D CP	11 72
	SATA_85D	SATA_R2D	NC SATA A R2D CN	11 72
	SATA_85D	SATA_D2R	NC SATA A D2RP	11 72
	SATA_85D	SATA_D2R	NC SATA A D2RN	11 72
	SATA_85D	SATA_R2D	NC SATA B R2D CP	11 72
	SATA_85D	SATA_R2D	NC SATA B R2D CN	11 72
	SATA_85D	SATA_D2R	NC SATA B D2RP	11 72
	SATA_85D	SATA_D2R	NC SATA B D2RN	11 72

1213	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP
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	USB_EXT_A	USB_85D	USB	USB_EXT_A_P	13	38
	USB_EXT_A	USB_85D	USB	USB_EXT_A_N	13	38
	USB_EXT_A	USB_85D	USB	USB_EXT_A_MUXED_P	38	38
	USB_EXT_A	USB_85D	USB	USB_EXT_A_MUXED_N	38	38
	USB_EXT_A	USB_85D	USB	USB_LT1_P	38	38
	USB_EXT_A	USB_85D	USB	USB_LT1_N	38	38

	USB_NC	USB_85D	USB	NC USB_EXTCP	13 72
	USB_NC	USB_85D	USB	NC USB_EXTCN	13 72
	USB_NC	USB_85D	USB	NC USB_SDP	13 72
	USB_NC	USB_85D	USB	NC USB_SDN	13 72
		CPU1_45S	CPU1_TTP	SMC_DEBUGPRPT_RX_L	38 41 42
		CPU1_45S	CPU1_TTP	SMC_DEBUGPRPT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC USB_SMP	72
	USB_SMC	USB_85D	USB	NC USB_SMCN	72

19A00	USB_NC	USB_R5D	USB	NC_USB_6P	13 72
19A00	USB_NC	USB_R5D	USB	NC_USB_6N	13 72
19A00	USB_NC	USB_R5D	USB	NC_USB_7P	13 72
19A00	USB_NC	USB_R5D	USB	NC_USB_7N	13 72
19A00	USR_EXTR	USR_R5D	USR	USB_EXTB_P	13 68 71
19A00	USR_EXTR	USR_R5D	USR	USB_EXTB_N	13 68 71
19A00	USB_NC	USB_R5D	USB	NC_USB_EXTDP	13 72
19A00	USB_NC	USB_R5D	USB	NC_USB_EXTDN	13 72
19A00	USR_BT	USR_R5D	USR	USB_BT_P	13 34
19A00	USR_BT	USR_R5D	USR	USB_BT_N	13 34
19A00		USR_R5D	USR	USB_BT_CONN_P	34 71
19A00		USR_R5D	USR	USB_BT_CONN_N	34 71
19A00	USB_NC	USB_R5D	USB	NC_USB_IRP	13 72
19A00	USB_NC	USB_R5D	USB	NC_USB_IRN	13 72
19A00	USR_TP4D	USR_R5D	USR	USB_TP4D_P	13 39
19A00	USR_TP4D	USR_R5D	USR	USB_TP4D_N	13 39
19A00		USR_R5D	USR	USB_TP4D_R_P	39
19A00		USR_R5D	USR	USB_TP4D_R_N	39
19A00	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13

U3P0	USB3_EXT_A_RX	USB_85D	USB3_D2R	USB3_EXT_A_D2R_P	13 38
U3P1	USB3_EXT_A_RX	USB_85D	USB3_D2R	USB3_EXT_A_D2R_N	13 38
U3P2		USB_85D	USB3_D2R	USB3_EXT_A_D2R_C_P	
U3P3		USB_85D	USB3_D2R	USB3_EXT_A_D2R_C_N	
U3P4	USB3_EXT_A_TX	USB_85D	USB3_R2D	USB3_EXT_A_R2D_P	38
U3P5	USB3_EXT_A_TX	USB_85D	USB3_R2D	USB3_EXT_A_R2D_N	38
U3P6		USB_85D	USB3_R2D	USB3_EXT_A_R2D_C_P	13 38
U3P7		USB_85D	USB3_R2D	USB3_EXT_A_R2D_C_N	13 38
U3P8	USB3_EXT_B_RX	USB_85D	USB3_D2R	USB3_EXT_B_D2R_P	13 68 71
U3P9	USB3_EXT_B_RX	USB_85D	USB3_D2R	USB3_EXT_B_D2R_N	13 68 71
U3P10		USB_85D	USB3_D2R	USB3_EXT_B_D2R_C_P	
U3P11		USB_85D	USB3_D2R	USB3_EXT_B_D2R_C_N	
U3P12	USB3_EXT_B_TX	USB_85D	USB3_R2D	USB3_EXT_B_R2D_P	68 71
U3P13	USB3_EXT_B_TX	USB_85D	USB3_R2D	USB3_EXT_B_R2D_N	68 71
U3P14		USB_85D	USB3_R2D	USB3_EXT_B_R2D_C_P	13 68
U3P15		USB_85D	USB3_R2D	USB3_EXT_B_R2D_C_N	13 68
U3P16	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
U3P17	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
U3P18		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
U3P19		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
U3P20	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
U3P21	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
U3P22		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
U3P23		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
FE500	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC 11 19
FE500	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB 11 19
FE500		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB R 11
FE500	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA 19 37
FE500		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT 19 28
FE500		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT R 28

SYNCH MASTER=SIDLE J45		SYNCH DATE=12/10/2012	
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PAGE		112 OF 118	
SHEET		75 OF 81	

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?	PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-T0-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_20THER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_20THER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_20THER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_20THER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC_45S	LPC	LPC AD<3..0> 13 41 50 71
	LPC_FRAME_I	LPC_45S	LPC	LPC FRAME L 13 41 50 71
	LPC_RESET_I	LPC_45S	LPC	LPCPLUS RESET L 20 50 71
	SMBUS_PCH_CLK	SMR_45S	SMR	SMBUS PCH CLK 13 18 22 44 63 68 71
	SMBUS_PCH_DATA	SMR_45S	SMR	SMBUS PCH DATA 13 18 22 44 63 68 71
	SMBUS_PCH_0_CLK	SMR_45S	SMR	SML PCH 0 CLK 13 44
	SMBUS_PCH_0_DATA	SMR_45S	SMR	SML PCH 0 DATA 13 44
	SMBUS_PCH_1_CLK	SMR_45S	SMR	SML PCH 1 CLK 13 44
	SMBUS_PCH_1_DATA	SMR_45S	SMR	SML PCH 1 DATA 13 44
	HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK 11 52
		HDA_45S	HDA	HDA BIT CLK R 11
	HDA_SYNC	HDA_45S	HDA	HDA SYNC 11 52
		HDA_45S	HDA	HDA SYNC R 11
		HDA_45S	HDA	HDA RST R L 11
	HDA_RST_I	HDA_45S	HDA	HDA RST L 11 52
	HDA_SDIN0	HDA_45S	HDA	HDA SDIN0 11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208 HDA SDOUT0 R 52
	HDA_SDOUIT	HDA_45S	HDA	HDA SDOUIT 11 52
		HDA_45S	HDA	HDA SDOUIT R 11 19
		SPT_45S	SPT	SPI CLK R 13 50
	SPT_CLK	SPT_45S	SPT	SPI CLK 50
		SPT_45S	SPT	SPI MOSI R 13 50
	SPT_MOST	SPT_45S	SPT	SPI MOSI 50
	SPT_MISO	SPT_45S	SPT	SPI MISO 13 50
		SPT_45S	SPT	SPI CS0 R L 13 50
	SPT_CS0	SPT_45S	SPT	SPI CS0 L 50
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3 SD R2D C P 13 29 68 71
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3 SD R2D C N 13 29 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3 SD D2R P 13 29 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3 SD D2R N 13 29 68 71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE AP R2D P 34 71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE AP R2D N 34 71
		PCIE_85D	PCIE_R2D	PCIE AP R2D C P 13 34
		PCIE_85D	PCIE_R2D	PCIE AP R2D C N 13 34
		PCIE_85D	PCIE_R2D	PCIE AP R2D PT P 34
		PCIE_85D	PCIE_R2D	PCIE AP R2D PT N 34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE AP D2R P 13 34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE AP D2R N 13 34
		PCIE_85D	PCIE_D2R	PCIE AP D2R PI P 34 71
		PCIE_85D	PCIE_D2R	PCIE AP D2R PI N 34 71
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE CAMERA R2D P 36 37
	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE CAMERA R2D N 36 37
		PCIE_85D	PCIE_R2D	PCIE CAMERA R2D C P 13 37
		PCIE_85D	PCIE_R2D	PCIE CAMERA R2D C N 13 37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE CAMERA D2R P 13 37
	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE CAMERA D2R N 13 37
		PCIE_85D	PCIE_D2R	PCIE CAMERA D2R C P 36 37
		PCIE_85D	PCIE_D2R	PCIE CAMERA D2R C N 36 37
		CLK LPC_45S	CLK LPC	LPC CLK33M SMC R 11 19
	PCH_LPC_CLK0	CLK LPC_45S	CLK LPC	LPC CLK33M SMC 19 41
	PCH_LPC_CLK0	CLK LPC_45S	CLK LPC	LPC CLK33M LPCPLUS 19 41 50 71
		CLK LPC_45S	CLK LPC	LPC CLK33M LPCPLUS R 11 19
	PCIE_CLK100M	CPU_45S	CLK PCIE	PCH CLK33M PCIIN 11 19
	PCIE_CLK100M	CPU_45S	CLK PCIE	PCH CLK14P3M REFCLK 11
	PCIE_CLK100M	CPU_45S	CLK PCIE	PCH CLK33M PCIOUT 11 19
	PCIE_CLK100M_PCH	CLK PCIE_85D	CLK PCIE	PCIE CLK100M PCH P 11
	PCIE_CLK100M_PCH	CLK PCIE_85D	CLK PCIE	PCIE CLK100M PCH N 11
	PCIE_CLK100M_TBT	CLK PCIE_85D	CLK PCIE	PCIE CLK100M TBT P 11 28
	PCIE_CLK100M_TBT	CLK PCIE_85D	CLK PCIE	PCIE CLK100M TBT N 11 28
	PCIE_CLK100M_DOT	CLK PCIE_85D	CLK PCIE	PCH CLK96M DOT P 11
	PCIE_CLK100M_DOT	CLK PCIE_85D	CLK PCIE	PCH CLK96M DOT N 11
	PCIE_CLK100M_SATA	PCIE_85D	CLK PCIE	PCH CLK100M SATA P 11
	PCIE_CLK100M_SATA	PCIE_85D	CLK PCIE	PCH CLK100M

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL		SPACING		NET_TYPE	
1E100	PCH_PM_NET	PCH_45S	PCH_SF	PCH_INTRUDER_L		11	
1E101	PCH_PM_NET	PCH_45S	PCH_SF	PCH_INTVRMEN_L		11	
1E102	PCH_PM_NET	PCH_45S	PCH_SF	PCH_DSWMRMEN		12	
1E103	PCH_PM_NET	PCH_45S	PCH_SF	PCH_SRTCRST_L		11	
1E104	PCH_PM_NET	PCH_45S	PCH_SF	PM_RSMRST_L		12	66 71
1E105	PCH_PM_NET	PCH_45S	PCH_SF	PM_SYSRST_L		12	19 41 71
1E106	PCH_PM_NET	PCH_45S	PCH_SF	PM_PCH_PWROK		12	19 71 76
1E107	PCH_PM_NET	PCH_45S	PCH_SF	PM_PCH_PWROK		12	19 71 76
1E108	PCH_PM_NET	PCH_45S	PCH_SF	PM_DSW_PWRGD		12	41 71
1E109	PCH_PM_NET	PCH_45S	PCH_SF	PM_PCH_SYS_PWROK		12	18 19 41 72
1E110	PCH_PM_NET	PCH_45S	PCH_SF	PM_PWRBTN_L		12	18 41
1E111	PCH_PM_NET	PCH_45S	PCH_SF	PM_THRMTRIP_L_R		14	42
1E112	PCH_PCTF_WAKE	PCH_45S	PCH_SF	PCIE_WAKE_L		12	34 36 71
1E113	PCH_PM_NET	PCH_45S	PCH_SF	PCH_RCIN_L		14	
1E114	PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>		13	36
1E115	PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>		13	36
1E116	PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>		13	36
1E117	PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>		13	36
1E118		PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>		35	
1E119		PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>		35	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_20THER
MEM_*_DQS_*	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CLK	*	*	MEM_20THER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_20THERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to cClock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A RAS L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A CAS L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A WE L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A DQS P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A DQS N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A DQS P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A DQS N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A DQS P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A DQS N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A DQS P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A DQS N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A DQS P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A DQS N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A DQS P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A DQS N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A DQS P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A DQS N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A DQS P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A DQS N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B RAS L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B CAS L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B WE L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B DQS P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B DQS N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B DQS P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B DQS N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B DQS P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B DQS N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B DQS P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B DQS N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B DQS P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B DQS N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B DQS P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B DQS N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B DQS P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B DQS N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B DQS P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B DQS N<7> 7 25 26
		MEM_PWR	PP0V75_S3 MEM VREFD0 A 22 23 24 78 74
		MEM_PWR	PP0V75_S3 MEM VREFCA A 22 23 24 78 74
		MEM_PWR	PP1V35_S3 MEM 23 24 25 26 46 69

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Memory Constraints			
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	REVISION		
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		PAGE	114 OF 118
		SHEET	77 OF 81

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTD_P_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTD_P_850	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTD_P_2SAME	*	=3X_DIELECTRIC	?
TBTD_P_TXR	*	=6X_DIELECTRIC	?
TBTD_P_2OTHER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBDP_*	=SAME	*	TBDP_2SAME
TBDP_R2D	TBDP_D2R	*	TBDP_TXRX
TBDP_*	*	*	TBDP_20THER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	TBT A R2D	TRTDP_85D	TRTDP_R2D	TBT A R2D C P<1..0>	28 31 72
	TBT A R2D	TRTDP_85D	TRTDP_R2D	TBT A R2D C N<1..0>	28 31
	TBT A R2D	TRTDP_85D	TRTDP_R2D	TBT A R2D P<1..0>	28 31
	TBT A R2D	TRTDP_85D	TRTDP_R2D	TBT A R2D N<1..0>	31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>	28 31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>	28 31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>	31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>	31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>	31
	DP A LSX ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>	31
	DP TBTPA ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>	28 31
	DP TBTPA ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>	28 31
	DP TBTPA ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>	31
	DP TBTPA ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>	31
	TBT A D2R0	TRTDP_85D	TRTDP_D2R	TBT A D2R C P<0>	31
	TBT A D2R0	TRTDP_85D	TRTDP_D2R	TBT A D2R C N<0>	31
	TBT A D2R0	TRTDP_85D	TRTDP_D2R	TBT A D2R P<0>	28 31
	TBT A D2R0	TRTDP_85D	TRTDP_D2R	TBT A D2R N<0>	28 31
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R C P<1>	31
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R C N<1>	31
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R P<1>	31 72
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R N<1>	31 72
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R1 AUXDDC P	31
	TBT A D2R1	TRTDP_85D	TRTDP_D2R	TBT A D2R1 AUXDDC N	31
	TBT A AUXCH	DP_85D		DP TBTPA AUXCH C P	28 31
	TBT A AUXCH	DP_85D		DP TBTPA AUXCH C N	31
	TBT A AUXCH	DP_85D		DP TBTPA AUXCH P	31
	TBT A AUXCH	DP_85D		DP TBTPA AUXCH N	31

FE01	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28	32
FE02	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28	32
FE03	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32	32
FE04	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32	32
FE05	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28	32
FE06	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28	32
FE07	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	32	32
FE08	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32	32
FE09	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32	32
FE0A	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32	32
FE0B	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28	32
FE0C	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28	32
FE0D	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32	32
FE0E	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32	32
FE0F	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32	32
FE10	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32	32
FE11	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28	32
FE12	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28	32
FE13	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	28	32
FE14	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32	32
FE15	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28	32
FE16	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28	32
FE17	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	28	32
FE18	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32	32
FE19	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28	32
FE1A	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28	32
FE1B	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32	32
FE1C	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DP_85D	DISPLAYPORT	DP_TBTSRC ML C P<3..0>
		DP_85D	DISPLAYPORT	DP_TBTSRC ML C N<3..0>
		DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C P
		DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C N
	TRT_SPT_CLK	TRT_SPT_45S	TRT_SPT	TBT SPI CLK
	TBT_SPT_MOSI	TRT_SPT_45S	TBT_SPT	TBT SPI MOSI
	TBT_SPT_MISO	TRT_SPT_45S	TBT_SPT	TBT SPI MISO
	TRT_SPT_CS_L	TRT_SPT_45S	TRT_SPT	TBT SPI CS_L

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE 11111			
Thunderbolt Constraints			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		SIZE D	
		REVISION <E4LABEL>	
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		PAGE 115 OF 118	
		SHEET 78 OF 81	

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_850	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_20THER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICKL_20THER	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_20THER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICKL_20THER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?
S2_DQS20WNDATA	*	=2X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?
S2_20THERMEM	*	=4X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?
S2MEM_20THER	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS20WNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_20THERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_20THER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_20THER
S2_MEM_DQS*	*	*	S2MEM_20THER
S2_MEM_CMD	*	*	S2MEM_20THER
S2_MEM_CTRL	*	*	S2MEM_20THER
S2_MEM_CLK	*	*	S2MEM_20THER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_20THERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS20WNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS20WNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

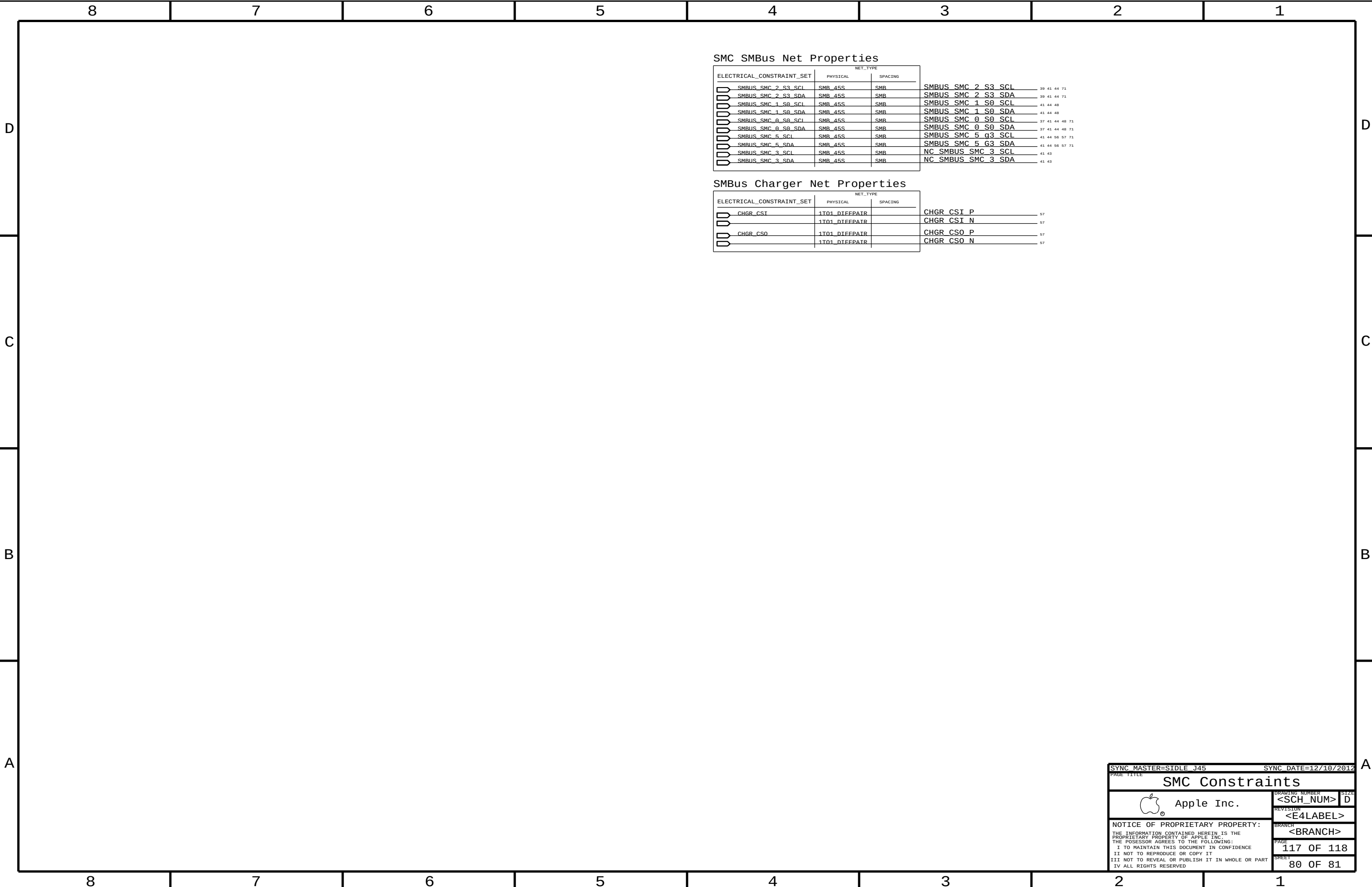
Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
		S2_MEM_PWR	PP1V35_CAM
		S2_MEM_PWR	PP0V675_CAM_VREF
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

SYNC_MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Camera Constraints			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	SIZE D
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		BRANCH <BRANCH>	
		PAGE 116 OF 118	
		SHEET 79 OF 81	



SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 SMBUS_SMC_2_S3_SCL	SMB_45S	SMR	SMBUS_SMC_2_S3_SCL	39 41 44 71
 SMBUS_SMC_2_S3_SDA	SMB_45S	SMR	SMBUS_SMC_2_S3_SDA	39 41 44 71
 SMBUS_SMC_1_S0_SCL	SMB_45S	SMR	SMBUS_SMC_1_S0_SCL	41 44 48
 SMBUS_SMC_1_S0_SDA	SMB_45S	SMR	SMBUS_SMC_1_S0_SDA	41 44 48
 SMBUS_SMC_0_S0_SCL	SMB_45S	SMR	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
 SMBUS_SMC_0_S0_SDA	SMB_45S	SMR	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
 SMBUS_SMC_5_SCL	SMB_45S	SMR	SMBUS_SMC_5_g3_SCL	41 44 56 57 71
 SMBUS_SMC_5_SDA	SMB_45S	SMR	SMBUS_SMC_5_g3_SDA	41 44 56 57 71
 SMBUS_SMC_3_SCL	SMB_45S	SMR	NC SMBUS_SMC_3_SCL	41 43
 SMBUS_SMC_3_SDA	SMB_45S	SMR	NC SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
 CHGR_CSI	1T01_DIEFPATR		CHGR_CSI_P	57
	1T01_DIEFPATR		CHGR_CSI_N	57
 CHGR_CS0	1T01_DIEFPATR		CHGR_CS0_P	57
	1T01_DIEFPATR		CHGR_CS0_N	57

SYNC_MASTER=SIDLE_J45

SYNC_DATE=12/10/2012

PAGE TITLE

SMC Constraints

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<SCH_NUM>

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PAGE

117 OF 118

SHEET

80 OF 81

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_50S	"	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_50S	"	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	"	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	"	=1:1_DIFFPAIR	0.1 MM	0.1 MM	16 MM	0.1 MM	0.1 MM
THERM_45S_CPUVIDNSG1	"	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1T01_45S	"	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1T01_45S	"	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_F20M
GND	PCIE_*	*	GND_F20M
GND	SATA_*	*	GND_F20M
USB	GND	*	GND_F20M
CLK_PCIE	SB_POWER	*	PWR_F20M
SB_POWER	SATA_*	*	PWR_F20M
USB	SB_POWER	*	PWR_F20M

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1T01_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS CPUDDR P 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS CPUDDR N 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS CPU DDR R P 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS CPU DDR R N 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	CPUTHMSNS D2 P 48
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	CPUTHMSNS D2 N 48
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS LCD PANEL P 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS LCD PANEL N 47
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	DDR3THMSNS D1 P 48
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	DDR3THMSNS D1 N 48
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	FINTHMSNS D P 48
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	FINTHMSNS D N 48
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS 1V35 MEM P 46
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS 1V35 MEM N 46
		SENSE 1T01_45S	SENSE	ISNS 1V35 MEM R P 46
		SENSE 1T01_45S	SENSE	ISNS 1V35 MEM R N 46
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS AIRPORT P 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS AIRPORT N 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS AIRPORT R P 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS AIRPORT R N 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS LCDCLKLT N 47 63
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS LCDCLKLT P 47 63
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS OTHER5V P 45
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS OTHER5V N 45
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS OTHER3V3 P 45
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS OTHER3V3 N 45
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS COMPUTING P 45
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS HS COMPUTING N 45
		SENSE 1T01_45S	SENSE	CPUVR ISNS P 46
		SENSE 1T01_45S	SENSE	CPUVR ISNS N 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	P1V05 GPU PEX IOVDD SNS P 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	P1V05 GPU PEX IOVDD SNS N 46
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS1 P 46 59
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS1 N 46 59
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS2 P 46 59
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS2 N 46 59
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS3 P 46 59
	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS3 N 46 59
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	CPUVR ISUM R P 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	CPUVR ISUM R N 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	GFXIMVP ISNS1 P 81
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	GFXIMVP ISNS1 N 81
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	GFXIMVP ISNS1 P 81
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	GFXIMVP ISNS1 N 81
	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT N 46
	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT P 46
		AUDIODIFF	AUDIO	ISNS TBT R N 46
		AUDIODIFF	AUDIO	ISNS TBT R P 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS SSD P 46
		THERM 1T01_45S	THERM	ISNS SSD N 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	ISNS SSD R P 46
		THERM 1T01_45S	THERM	ISNS SSD R N 46
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	P1V05S0 CS P 62
		THERM 1T01_45S	THERM	P1V05S0 CS N 62
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	P1V05S0 SENSE P 62
		THERM 1T01_45S	THERM	P1V05S0 SENSE N 62
	SENSE_DIEFFPAIR	THERM 1T01_45S	THERM	TBT THERMD P 28
		THERM 1T01_45S	THERM	TBT THERMD N 28
	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	CHGR CSI R P 57
		AUDIODIFF	AUDIO	CHGR CSI R N 57
	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	CHGR CS0 R P 57
		AUDIODIFF	AUDIO	CHGR CS0 R N 57
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS S2 P 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS S2 N 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS S2 R P 47
	SENSE_DIEFFPAIR	SENSE 1T01_45S	SENSE	ISNS S2 R N 47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	MET_TYPE	SPACING
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N
	AUDIODIFF	AUDIO	RSUBIN_P
	AUDIODIFF	AUDIO	RSUBIN_N
	AUDIODIFF	AUDIO	LSUBIN_P
	AUDIODIFF	AUDIO	LSUBIN_N
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP LIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP LIN N
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N
	AUDIODIFF	AUDIO	SPKRAMP LIN_P
	AUDIODIFF	AUDIO	SPKRAMP LIN N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SL_OUT_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SL_OUT_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SR_OUT_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SR_OUT_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_L_OUT_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_L_OUT_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_R_OUT_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_R_OUT_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	AUD_MIC_IN1_R_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	AUD_MIC_IN1_R_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	CODEC_HS_MIC_P
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	CODEC_HS_MIC_N
AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	AUD_MIC_IN1_L_P
	DIFFEPAIR	AUDIO	AUD_MIC_IN1_L_N
	DIFFEPAIR	AUDIO	AUD_HS_MIC_P
	DIFFEPAIR	AUDIO	AUD_HS_MIC_N
	DIFFEPAIR	AUDIO	HS_MIC_P
	DIFFEPAIR	AUDIO	HS_MIC_N
	DIFFEPAIR	AUDIO	AUD_CONN_HS_MIC_P
	DIFFEPAIR	AUDIO	AUD_CONN_HS_MIC_N
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P
AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		SB_POWER	PP1V35_S3RS0_CPUDDR
		GND	GND

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		PAGE 118 OF 118	
		SHEET 81 OF 81	