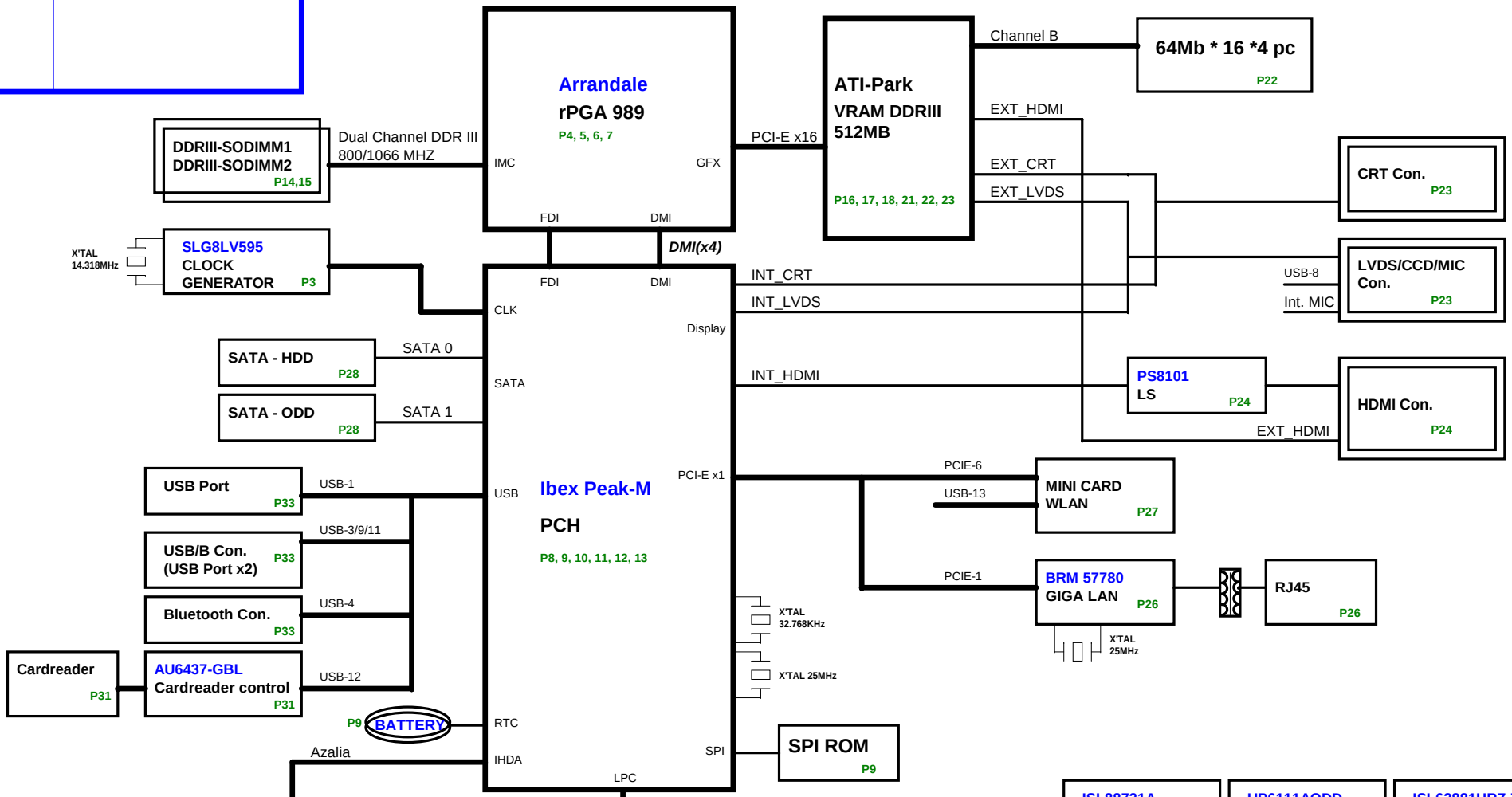
VER : 1A

BOM P/N	Description

ZQH SYSTEM BLOCK DIAGRAM



ISL88731A Batery Charger P36	UP6111AQDD +1.05V P39	ISL62881HRZ-T +VGFX_AXG P41
RT8206B 3V/5V P37	RT8207A +1.5V_SUS P40	HPA00835RTER +1.8V P43
ADP3212 CPU core P38	MAX8792ETD+T +VGPU_CORE P42	Discharger P43
RT9018A +1V P44		Thermal Protection P44

BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	Block Diagram	1A

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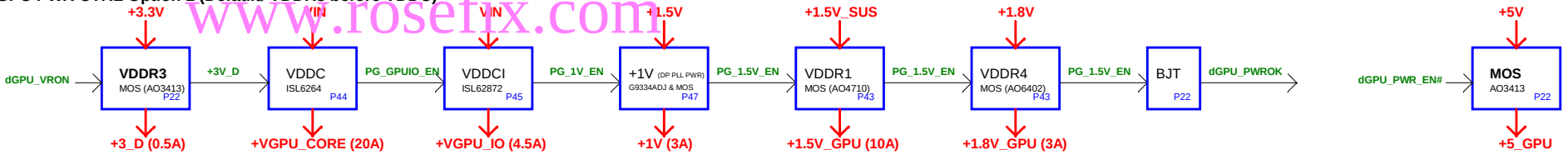
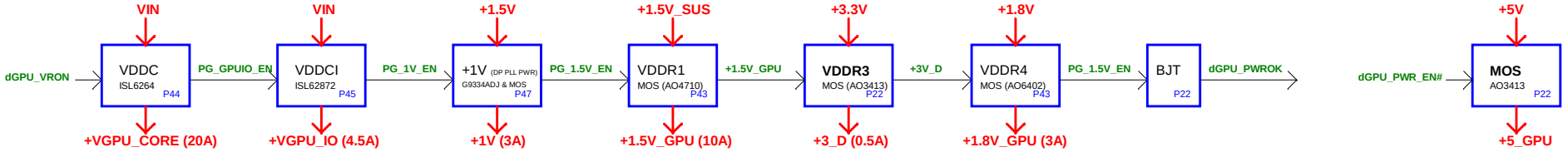
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



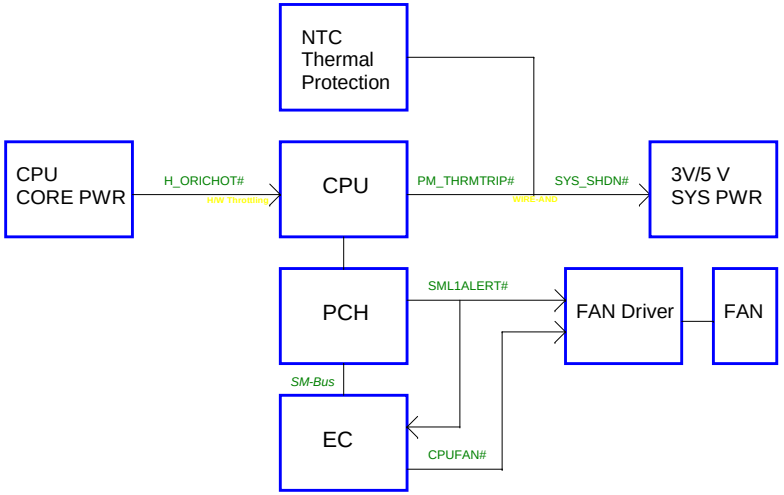
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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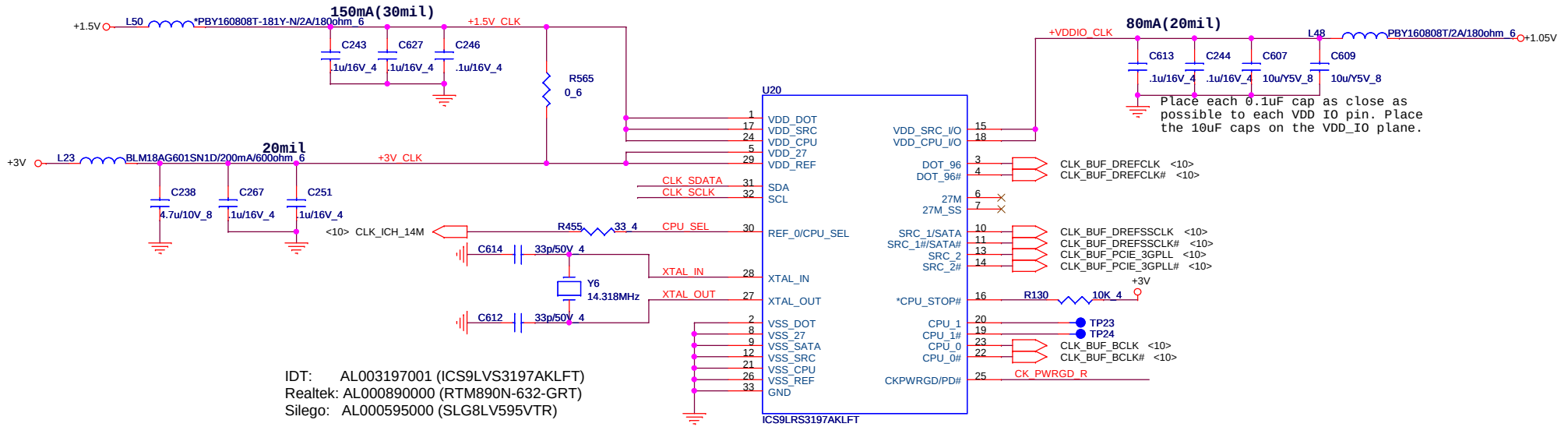
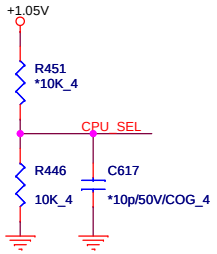


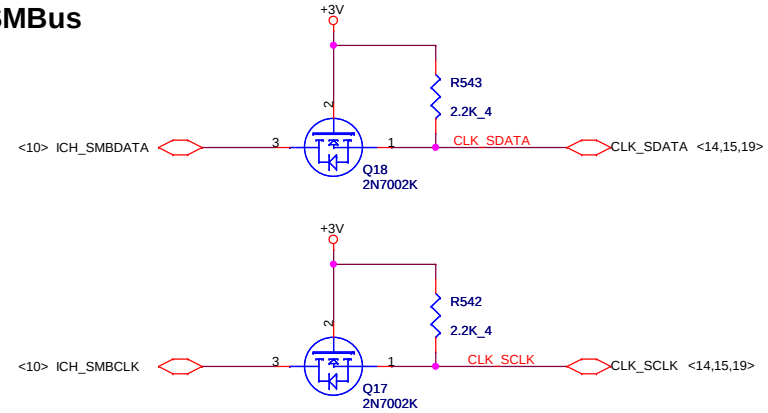
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

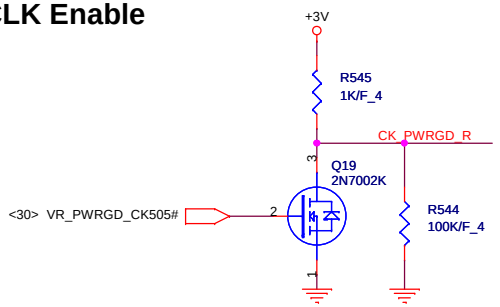


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



Quanta Computer Inc.
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Size	Document Number	Rev
	Clock Generator	1A
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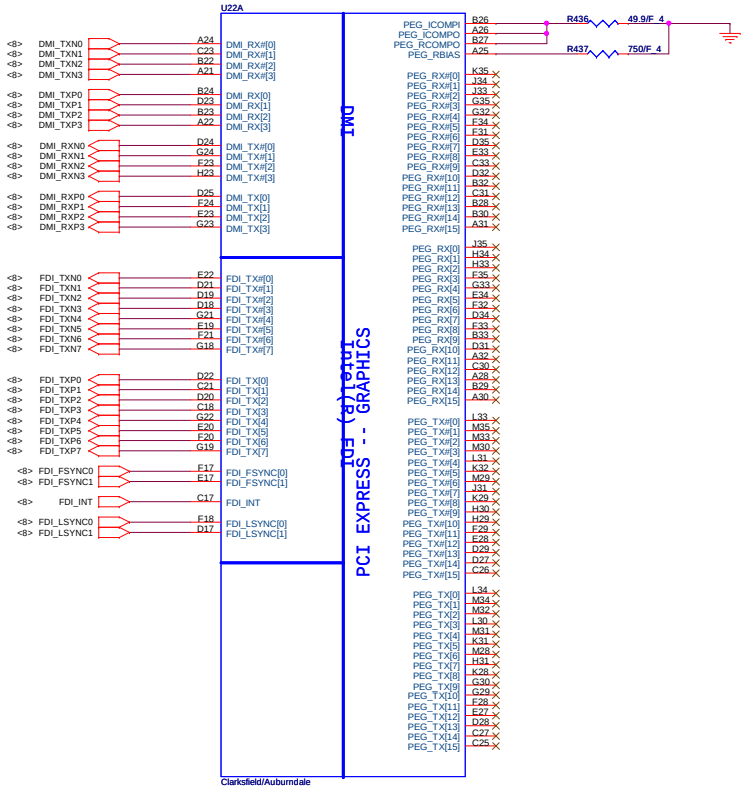
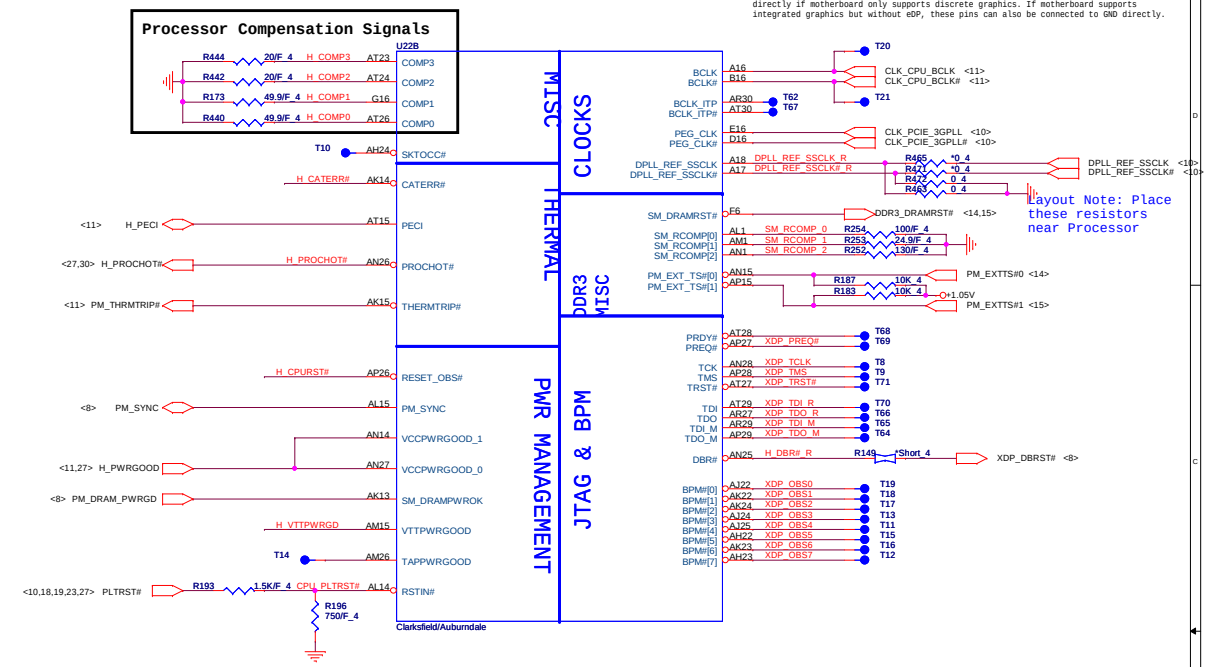
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

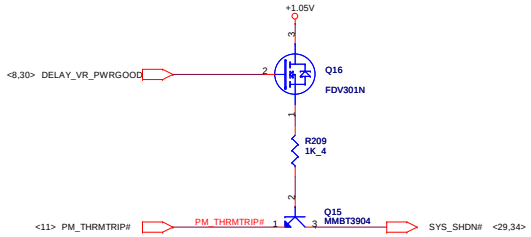


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

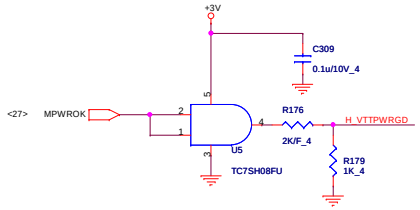
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.



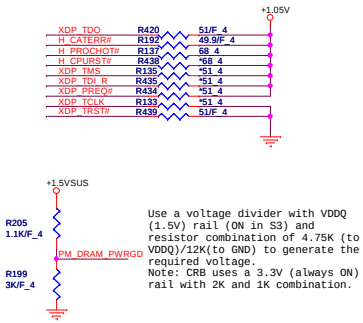
Thermaltrip protect



VTT PWR_Good

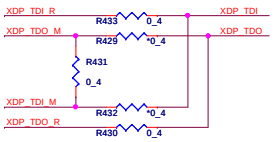


Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

Quanta Computer Inc.
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	AUBURNDA 1/4	1A

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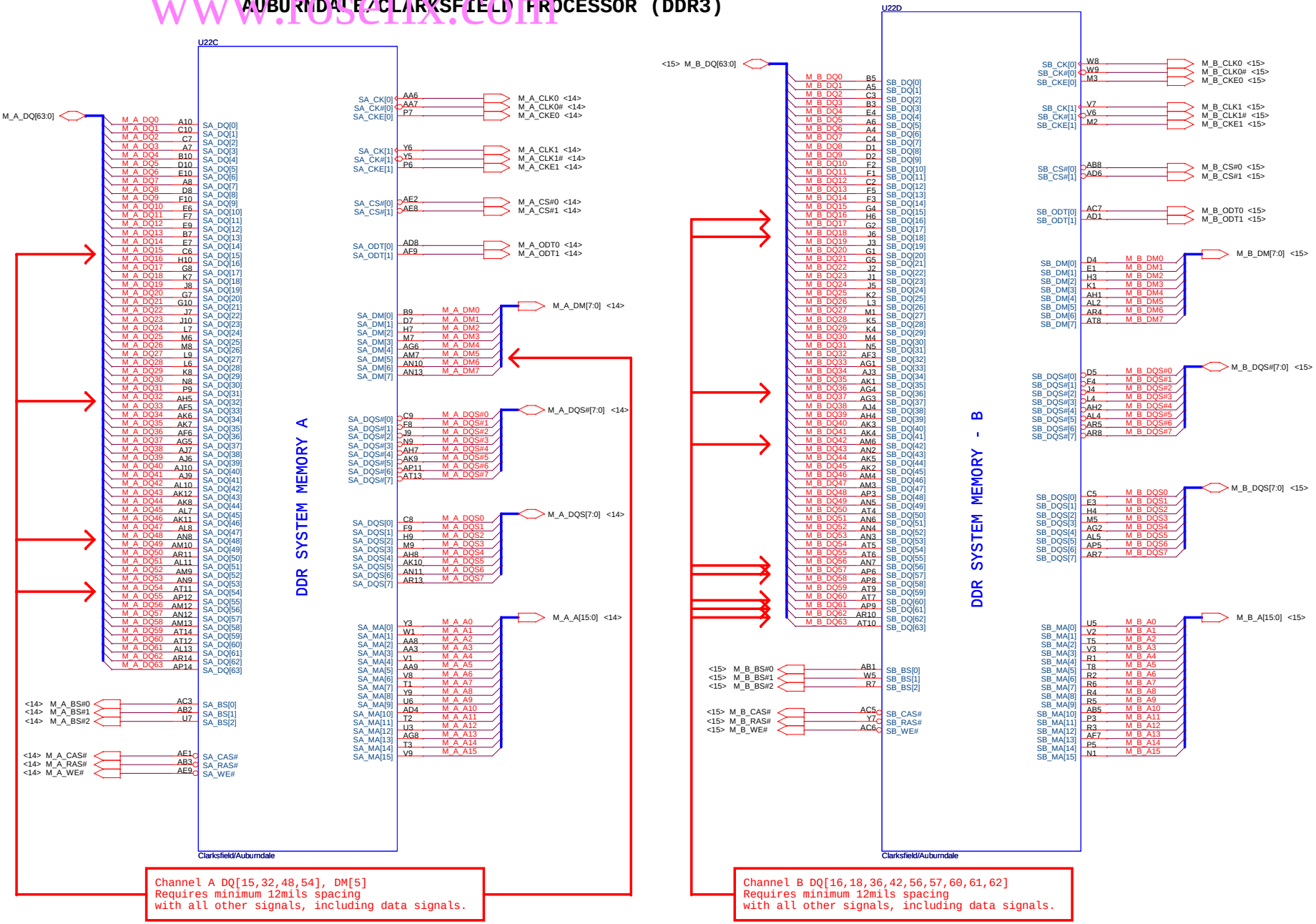
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
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AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

CPU Core Power

ARD:48A
CFD:52A

+VCC_CORE

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

C568 10U/6.3V_8
C626 22U/6.3V_8
C234 10U/6.3V_8
C589 22U/6.3V_8
C623 22U/6.3V_8
C643 10U/6.3V_8
C642 10U/6.3V_8
C590 22U/6.3V_8
C567 22U/6.3V_8
C640 10U/6.3V_8
C230 10U/6.3V_8
C588 22U/6.3V_8
C235 10U/6.3V_8
C569 10U/6.3V_8
C297 10U/6.3V_8
C624 10U/6.3V_8
C621 10U/6.3V_8
C638 10U/6.3V_8
C625 10U/6.3V_8
C566 10U/6.3V_8
C622 10U/6.3V_8
C266 10U/6.3V_8
C265 10U/6.3V_8
C236 10U/6.3V_8
C641 10U/6.3V_8
C287 10U/6.3V_8
C232 10U/6.3V_8
C633 10U/6.3V_8
C275 0.1u/10V_4 X7R
C271 0.1u/10V_4 X7R
C284 330u/2V_7343
C285 330u/2V_7343

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

18A

+1.05V

C658 10U/6.3V_8
C657 10U/6.3V_8
C634 10U/6.3V_8
C327 10U/6.3V_8
C648 10U/6.3V_8
C649 10U/6.3V_8
C644 10U/6.3V_8
C659 10U/6.3V_8
C652 10U/6.3V_8
C331 10U/6.3V_8
C316 330u/2V_7343

C313 22U/6.3V_8
C326 22U/6.3V_8

1.1V RAIL POWER
CPU CORE SUPPLY

POWER
CPU VIDS

PSI# AN33 H_PSI# → H_PSI# <30>

VID[0] AK35 H_VID0 → H_VID0 <30>
VID[1] AK33 H_VID1 → H_VID1 <30>
VID[2] AK34 H_VID2 → H_VID2 <30>
VID[3] AL35 H_VID3 → H_VID3 <30>
VID[4] AL33 H_VID4 → H_VID4 <30>
VID[5] AM33 H_VID5 → H_VID5 <30>
VID[6] AM35 H_VID6 → H_VID6 <30>
PROC_DPRSLPVR AM34 H_DPRSLPVR → H_DPRSLPVR <30>

VTT_SELECT G15

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE AN35 → I_MON <30>

R104 100/F_4 +VCC_CORE
R103 100/F_4

VCC_SENSE AJ34 → VCCSENSE <30>
VSS_SENSE AJ35 → VSSSENSE <30>

VTT_SENSE B15 VTT_SENSE → T75
VSS_SENSE_VTT A15 VSS_SENSE_VTT → T74

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

U22G

22A

+VGFX_AXG

C635 330U/2V_7343
C281 22u/6.3V_8
C280 22u/6.3V_8
C651 330U/2V_7343
C298 10u/6.3V_8
C299 10u/6.3V_8

GRAPHICS

SENSE LINES
VAXG_SENSE AR22 → VCC_AXG_SENSE <33>
VSSAXG_SENSE AT22 → VSS_AXG_SENSE <33>
T72
T73

GRAPHICS VIDS
GFX_VID[0] AM22 → GFX_VID0 <33>
GFX_VID[1] AP22 → GFX_VID1 <33>
GFX_VID[2] AN22 → GFX_VID2 <33>
GFX_VID[3] AP23 → GFX_VID3 <33>
GFX_VID[4] AM23 → GFX_VID4 <33>
GFX_VID[5] AP24 → GFX_VID5 <33>
GFX_VID[6] AN24 → GFX_VID6 <33>

GFX_VR_EN AR25 → GFX_ON <33>
GFX_DPRSLPVR AT25 → GFX_DPRSLPVR <33>
GFX_IMON AM24 → GFX_IMON <33>

POWER

PDL

PEG & DMI

+1.05V

C311 10U/6.3V_8
C655 22u/6.3V_8
C332 10U/6.3V_8
C656 10U/6.3V_8
C312 22u/6.3V_8
C330 22u/6.3V_8

J24 VTT1_45
J23 VTT1_46
H25 VTT1_47

K26 VTT1_48
J27 VTT1_49
J26 VTT1_50
J25 VTT1_51
H27 VTT1_52
G28 VTT1_53
G27 VTT1_54
G26 VTT1_55
F26 VTT1_56
E26 VTT1_57
E25 VTT1_58

DDR3 - 1.5V RAILS

ARD:3A
CFD:6A

VDDQ1 AJ1 → +1.5VSUS
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

C358 1U/6.3V_4
C356 1U/6.3V_4
C355 1U/6.3V_4
C352 1U/6.3V_4
C417 1U/6.3V_4
C360 22U/6.3V_8
C357 22U/6.3V_8
C363 330U/2V_7343

1.1V

VTT0_59 P10 → +1.05V
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

C660 10U/6.3V_8
C654 10U/6.3V_8

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

C618 10U/6.3V_8
C630 10U/6.3V_8

0.6A

1.8V

VCCPLL1 L26 → +1.8V
VCCPLL2 L27
VCCPLL3 M26

C258 22U/6.3V_8
C274 4.7U/6.3V_6
C231 2.2U/6.3V_6
C233 1U/6.3V_4
C239 1U/6.3V_4

Clarksfield/Auburndale

H_VID0 R388 1K_4
H_VID1 R395 *1K/F_4
H_VID2 R387 1K_4
H_VID3 R394 *1K/F_4
H_VID4 R389 1K_4
H_VID5 R396 *1K/F_4
H_VID6 R400 1K_4
H_DPRSLPVR R409 *1K/F_4
H_PSI# R401 1K_4
R410 *1K/F_4
R404 1K_4
R413 *1K/F_4
R402 1K_4
R411 *1K/F_4
R403 1K_4
R412 *1K/F_4
R419 1K_4
R418 *1K/F_4
→ +1.05V

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A

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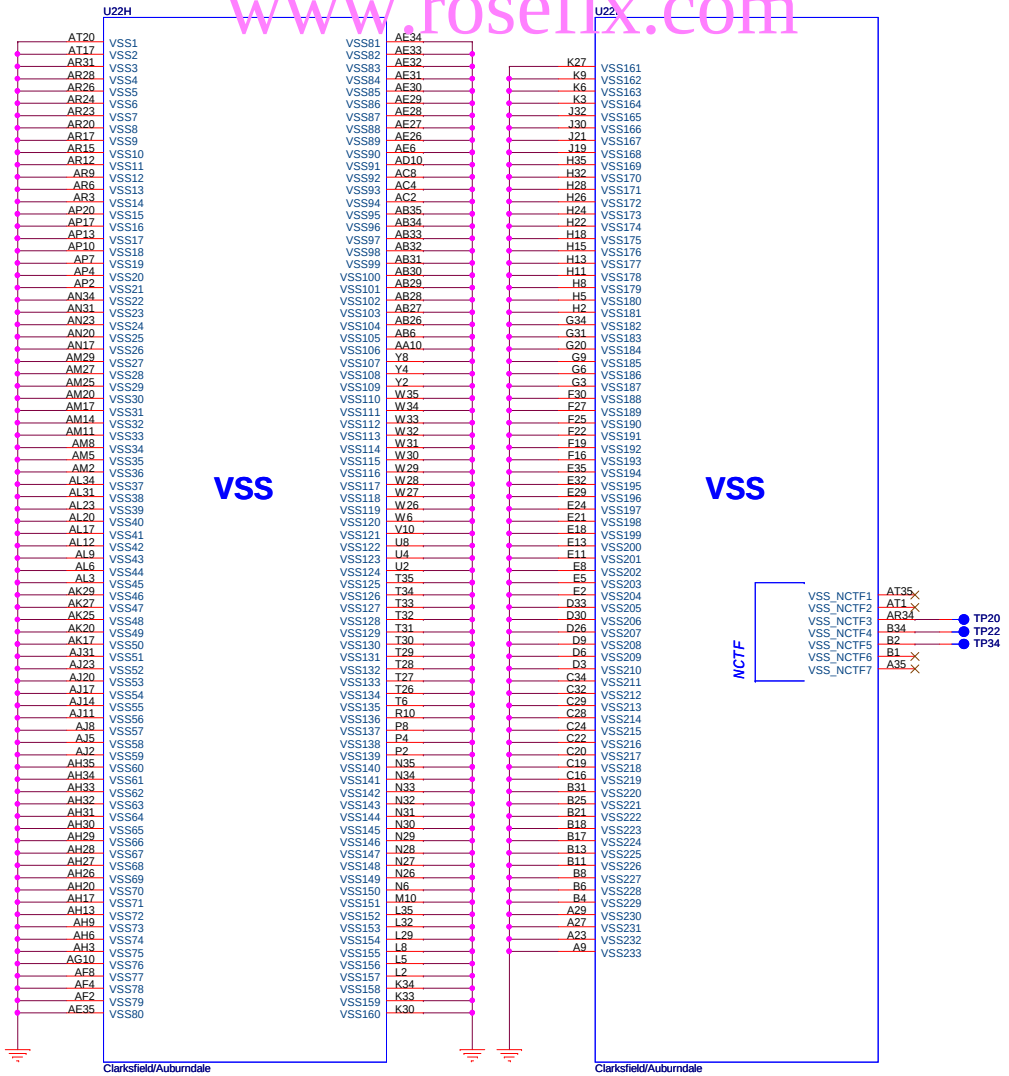
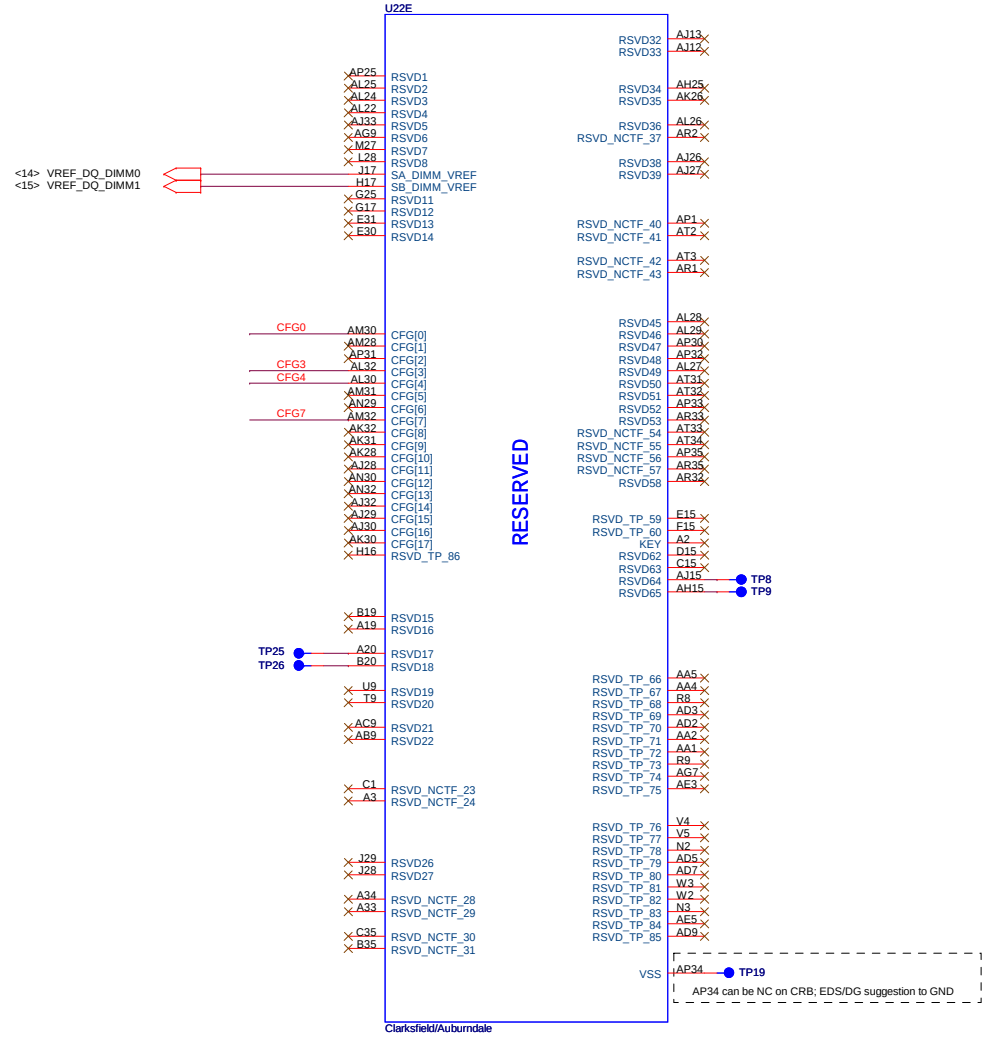
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 *3.01K
T h b e c p B B *				CFG7 R126 *3.01K/F_4

Quanta Computer Inc.
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	AUBURNDA 4/4	1A

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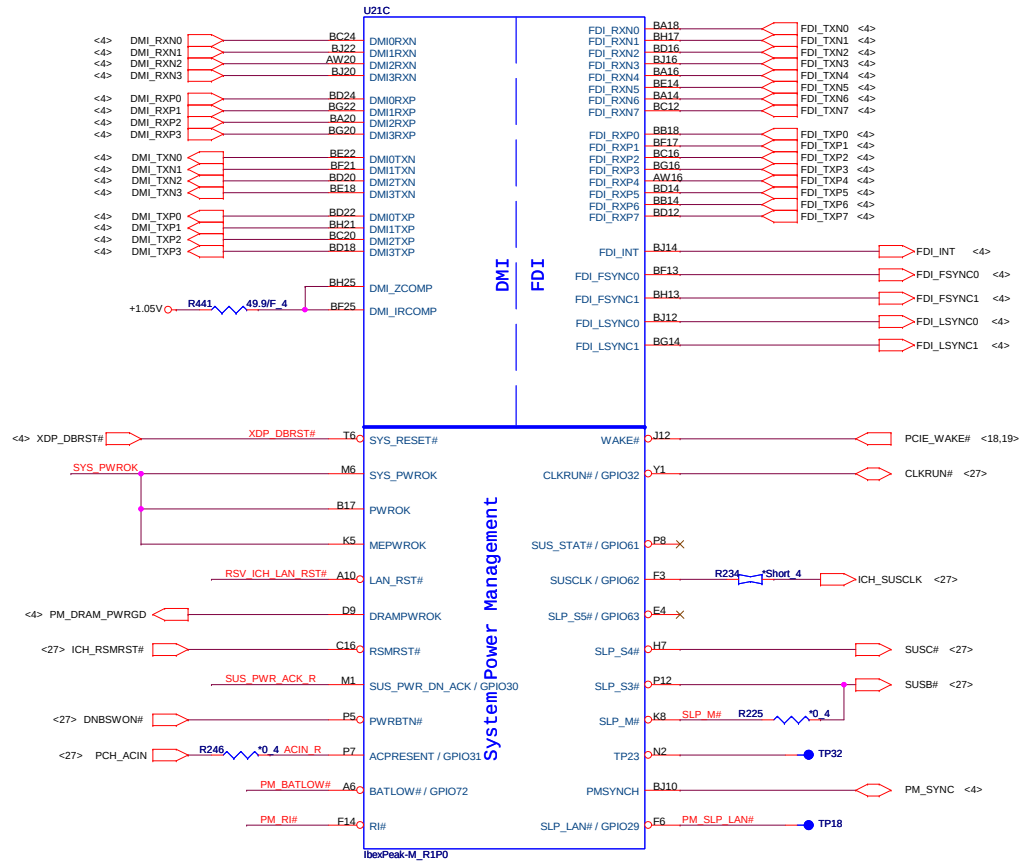
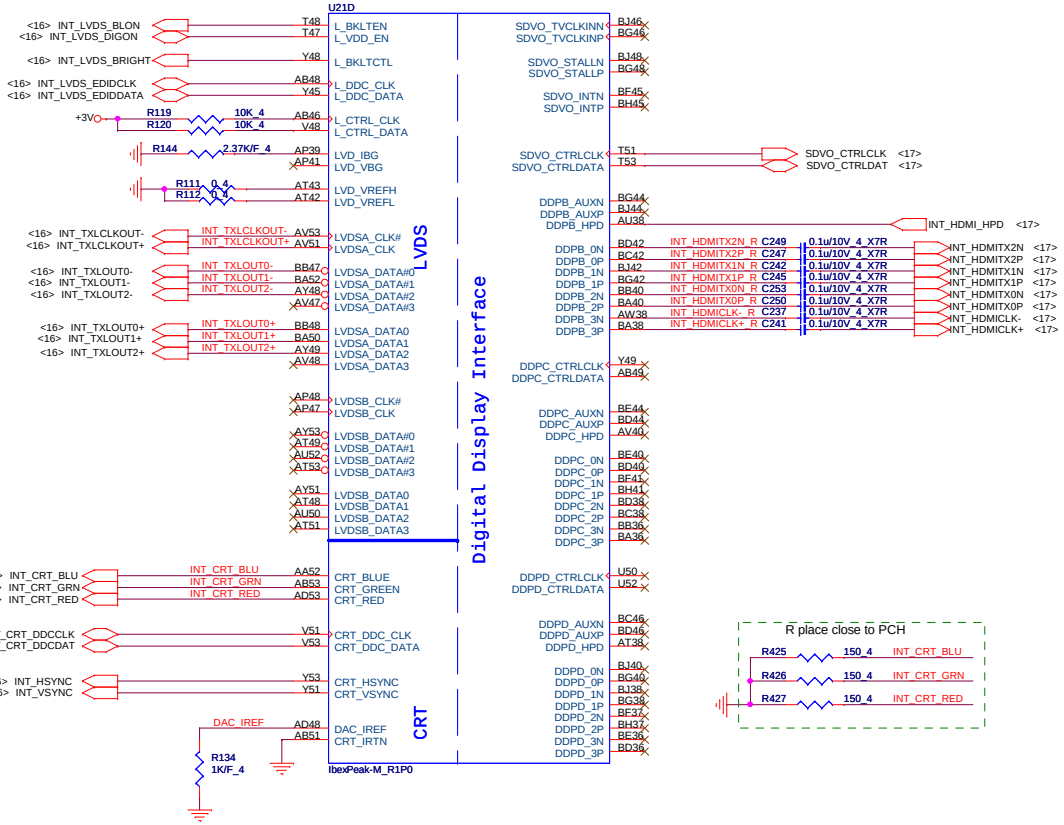
IBEX PEAK-M (DMI, FDI, GPIO)

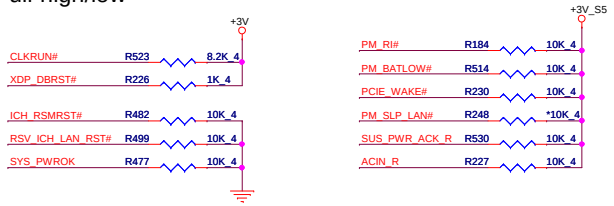
AC-coupling CAP place close to PCH

IBEX PEAK-M (LVDS,DDI)

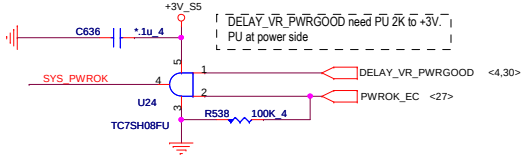




PCH Pull-high/low



System PWR_OK



Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: IBEX PEAK-M 1/6	Rev 1A
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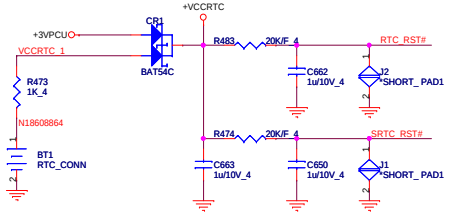
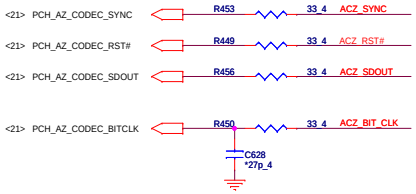
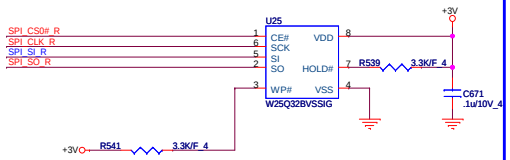
RTC Circuitry

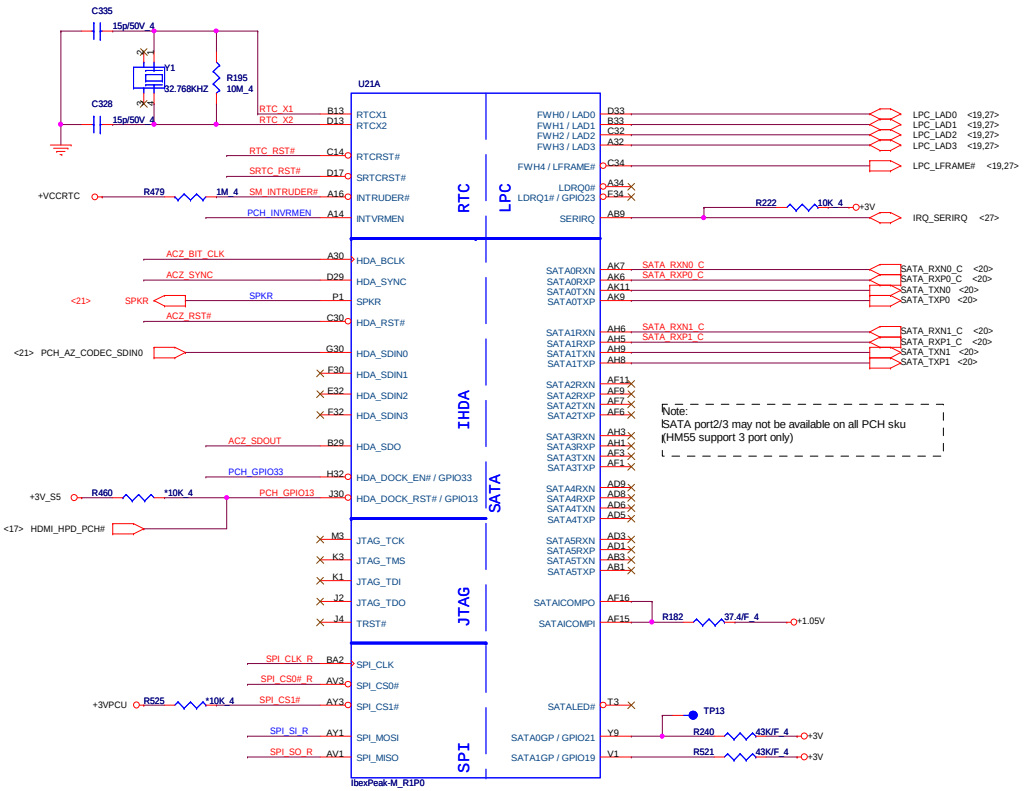


HDA Bus



PCH SPI





HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 *1K/F_4 R145 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K_4 R122 1K_4 R123 *1K_4 R131 *1K_4 +3V <10> PCI_GNT0# <10> PCI_GNT1#
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R204 10K_4 +3V_S5 R203 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R244 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 *10K_4

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	IBEX PEAK-M 2/6	1A
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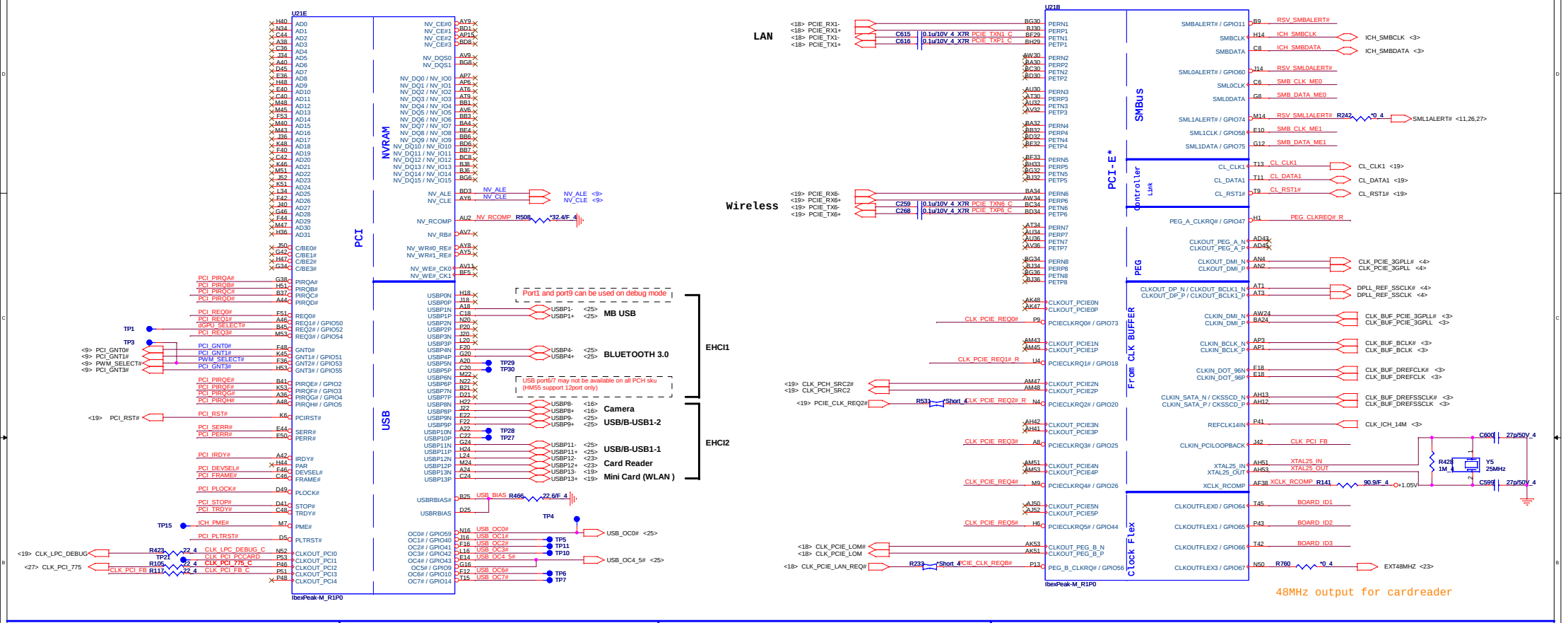
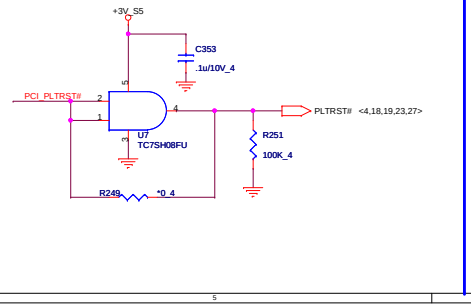
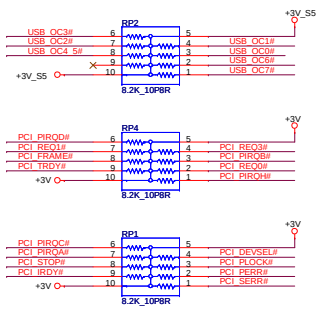
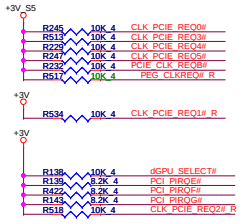
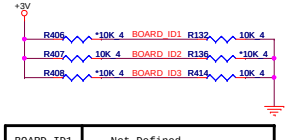


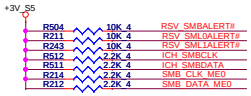


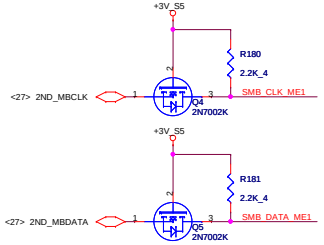






BOARD_ID1	Not Defined
BOARD_ID2	High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3	High = Reserved Low = Reserved (Default)





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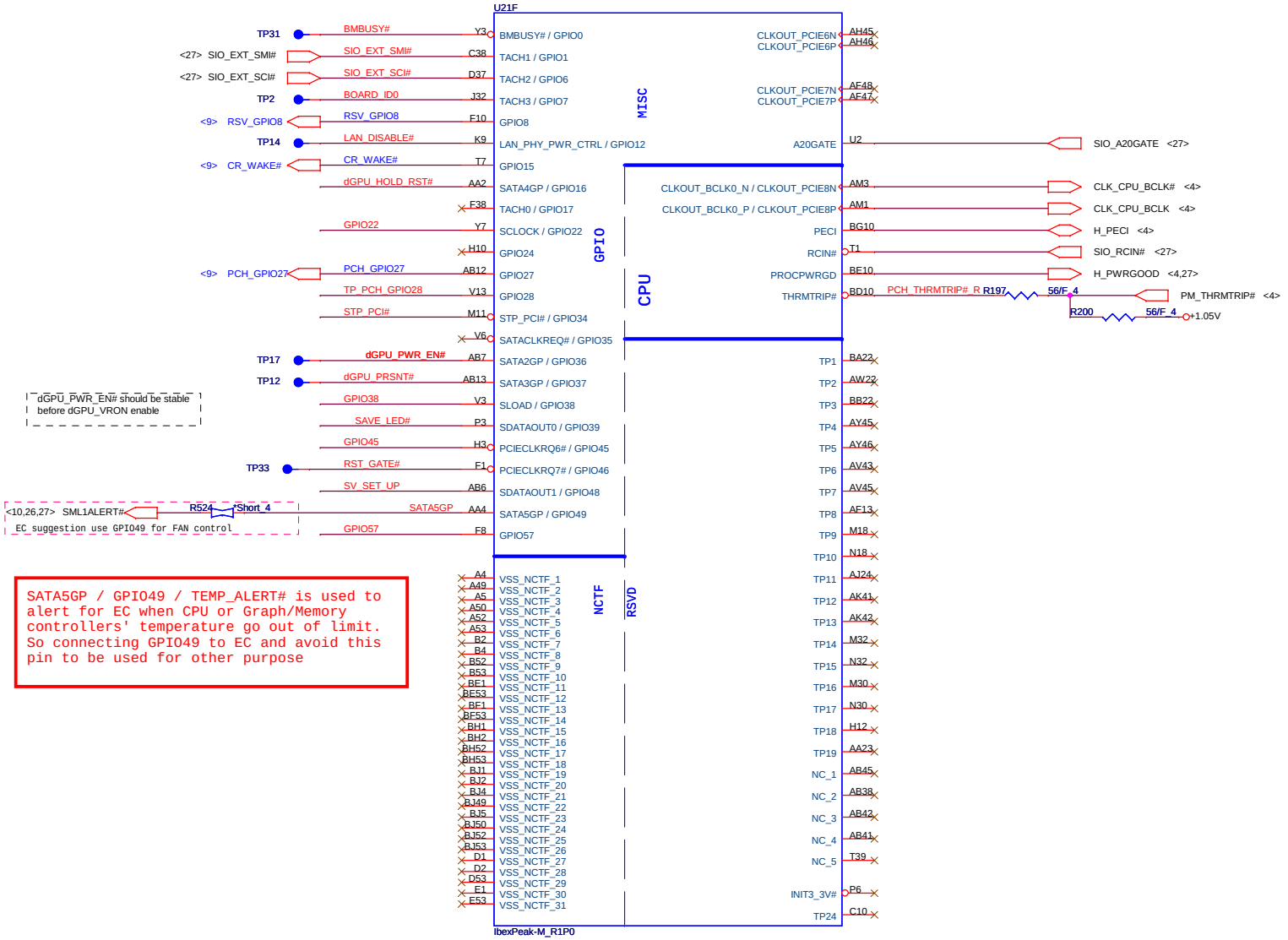
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

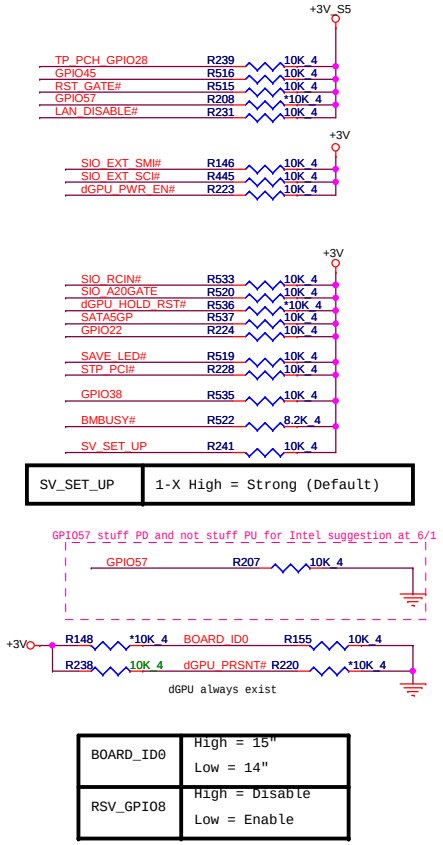


dGPU_PWR_EN# should be stable before dGPU_VRON enable

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#

GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = 15" Low = 14"
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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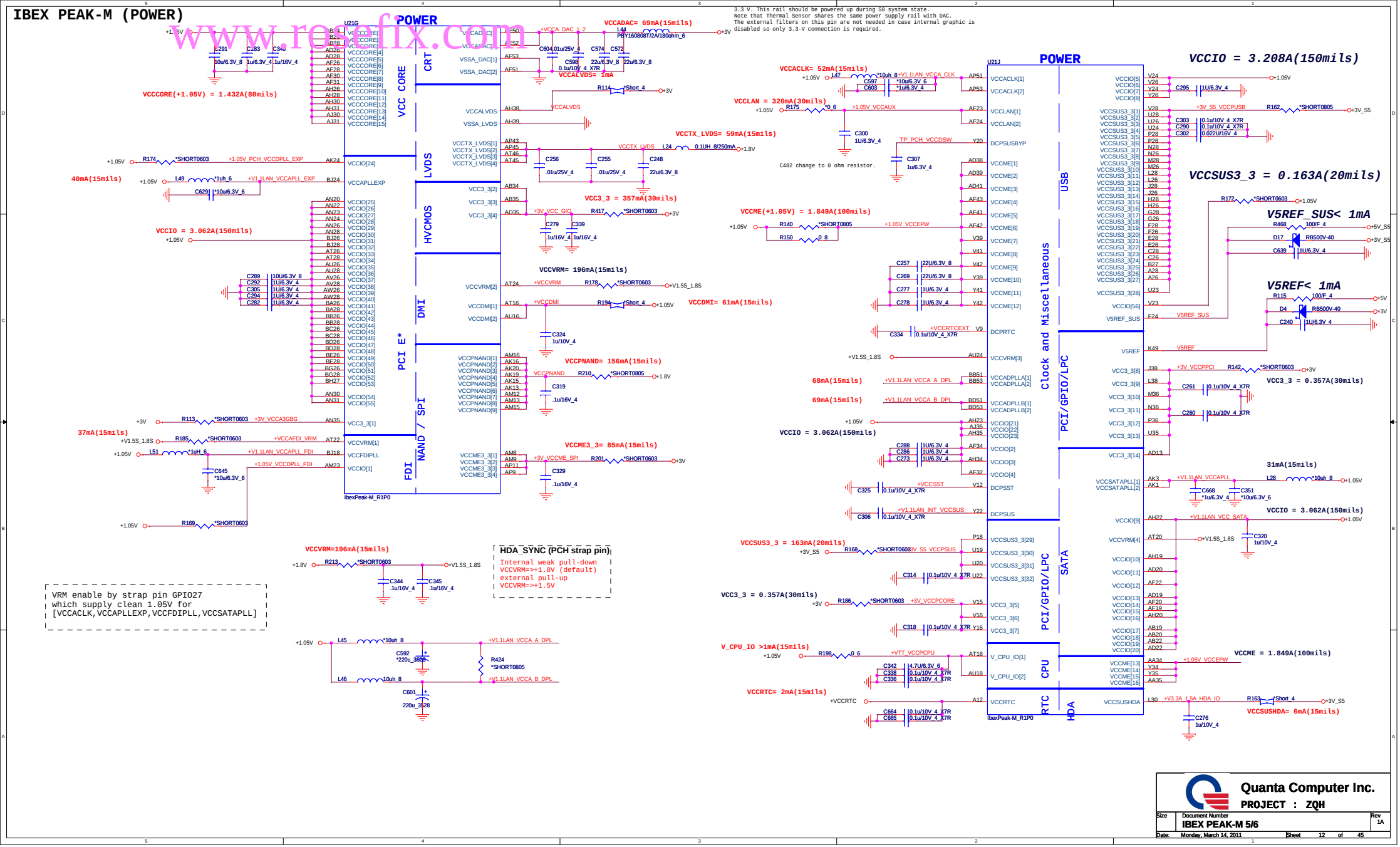
IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



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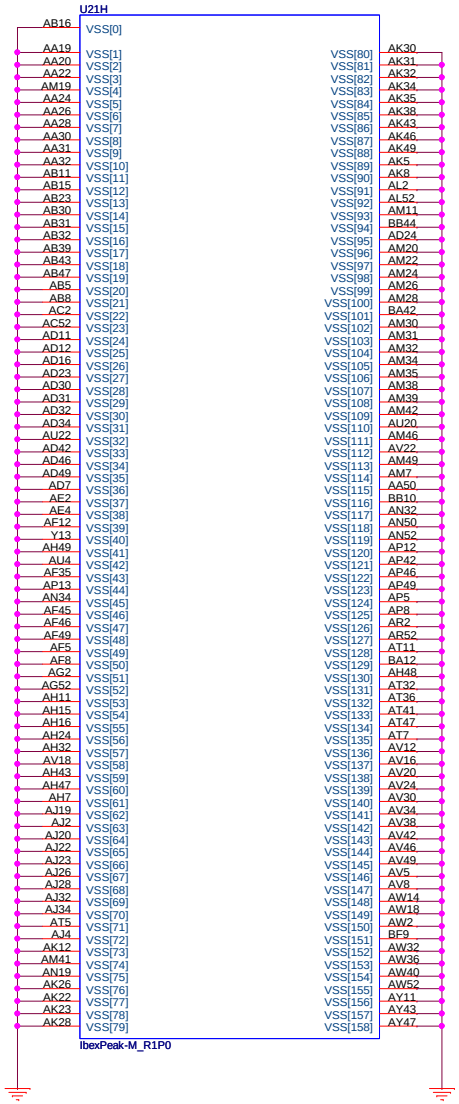
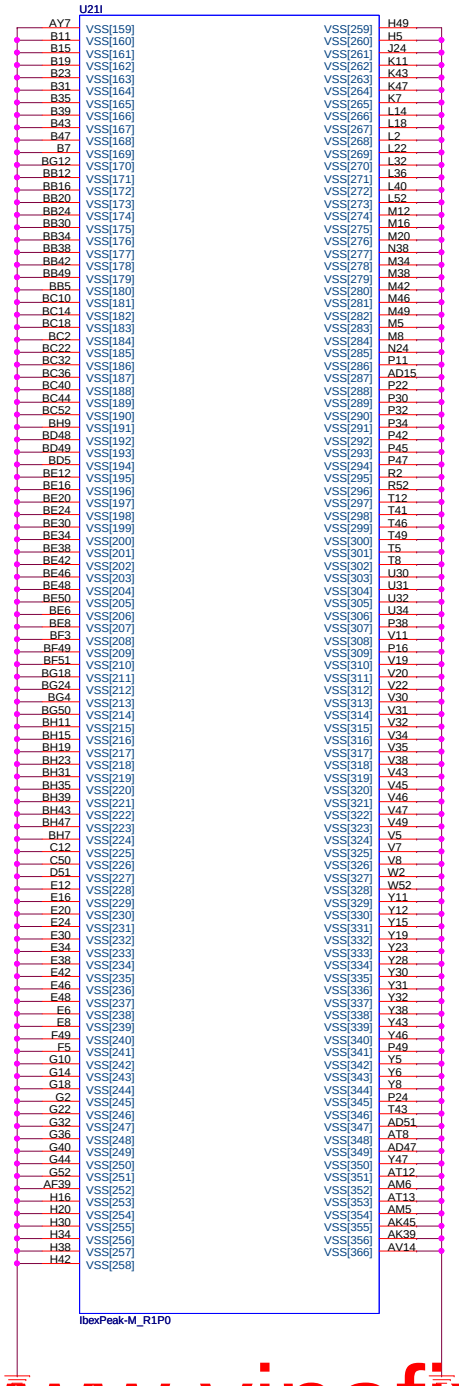
IBEX PEAK-M (GND)





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	IBEX PEAK-M 6/6	1A
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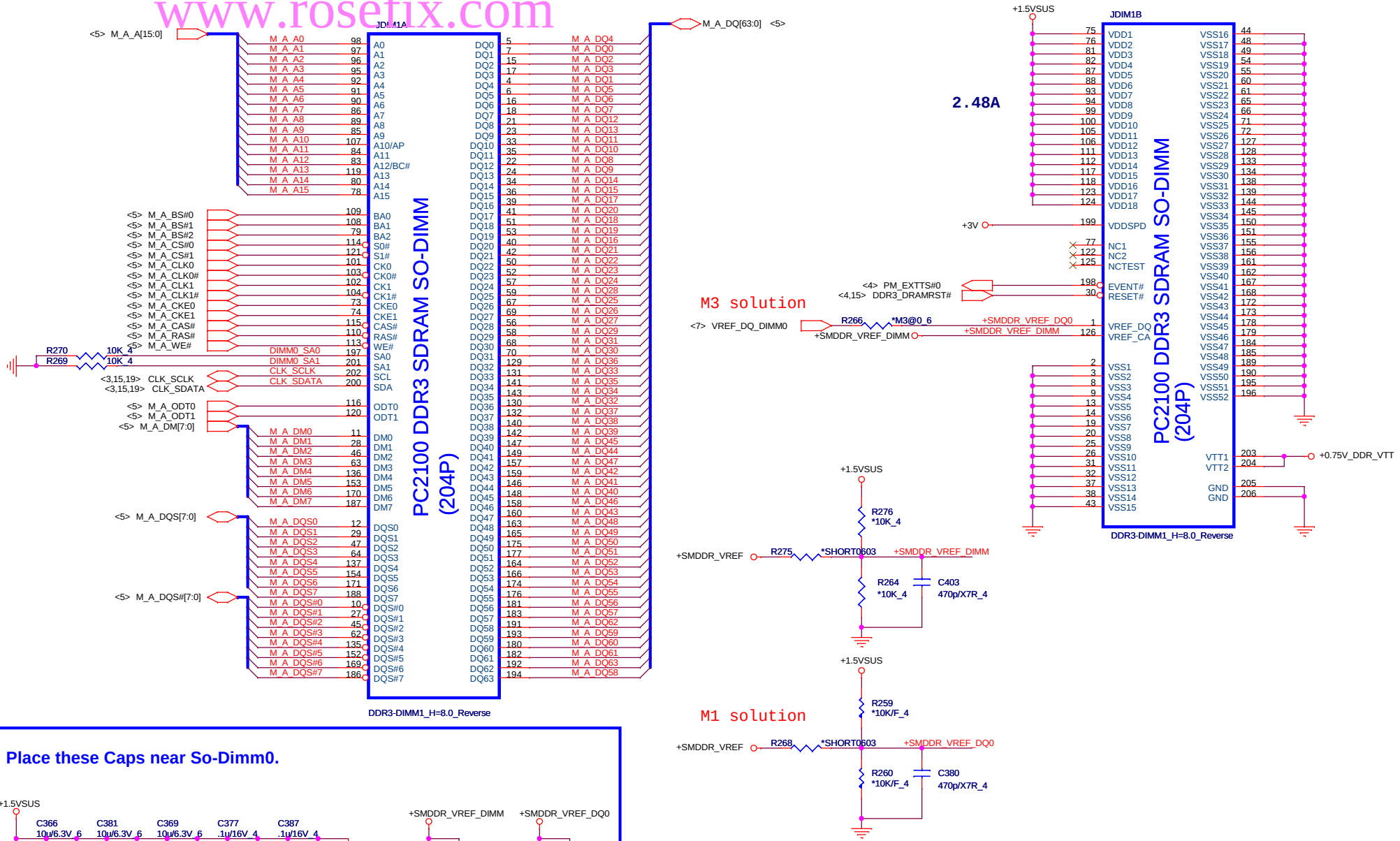
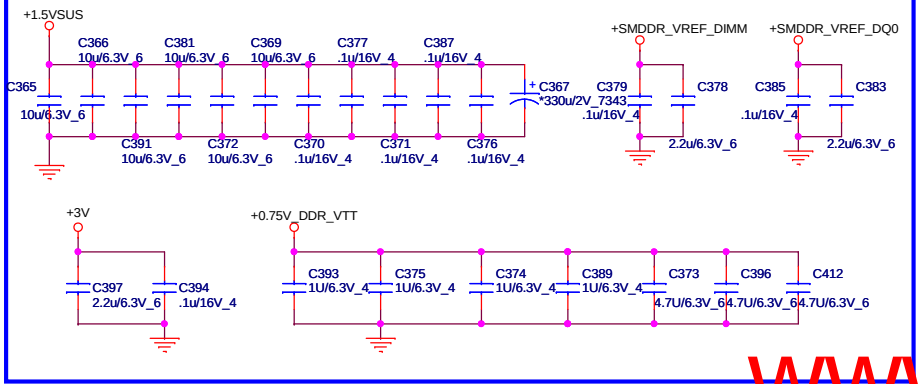


Place these Caps near So-Dimm0.



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	DDRIII SO-DIMM-0	1A
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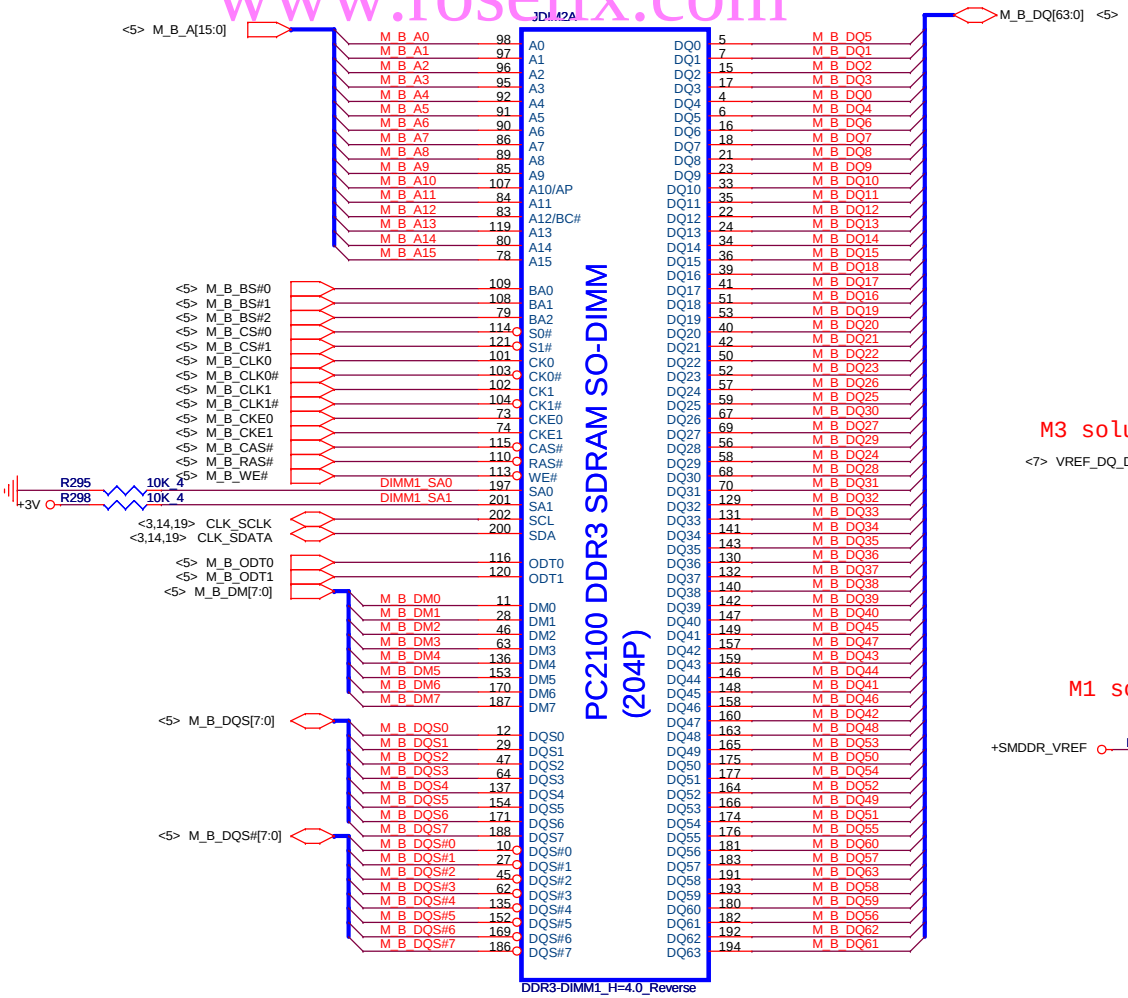

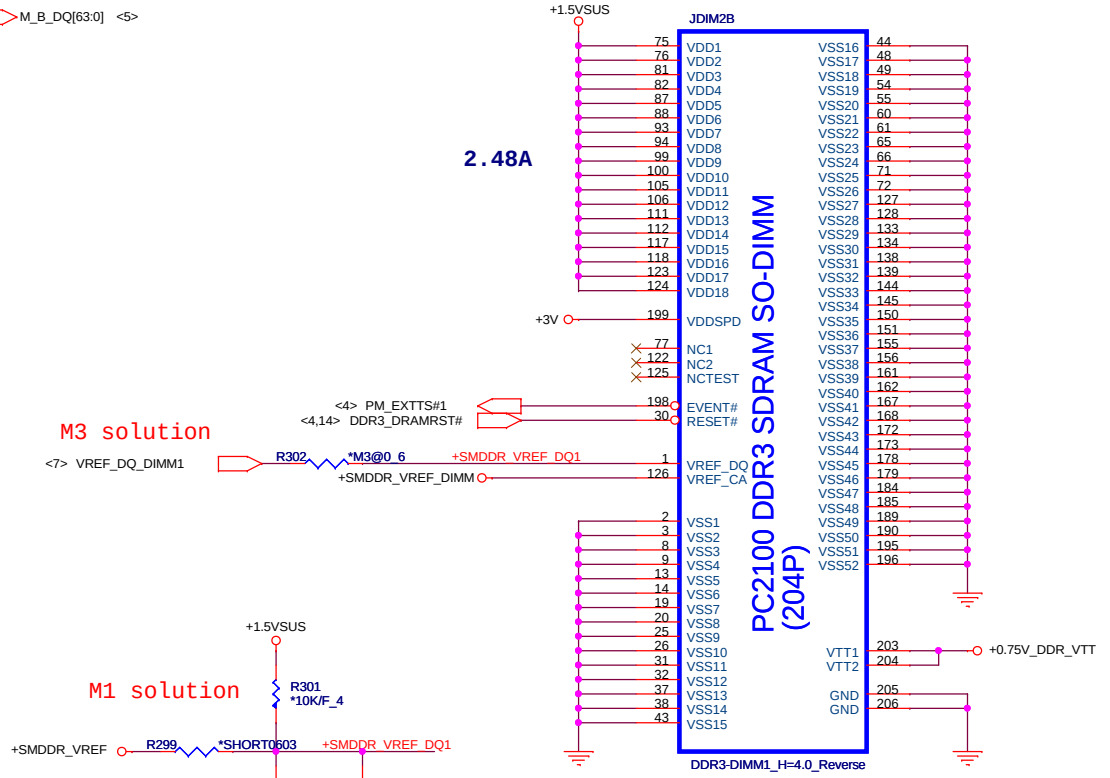

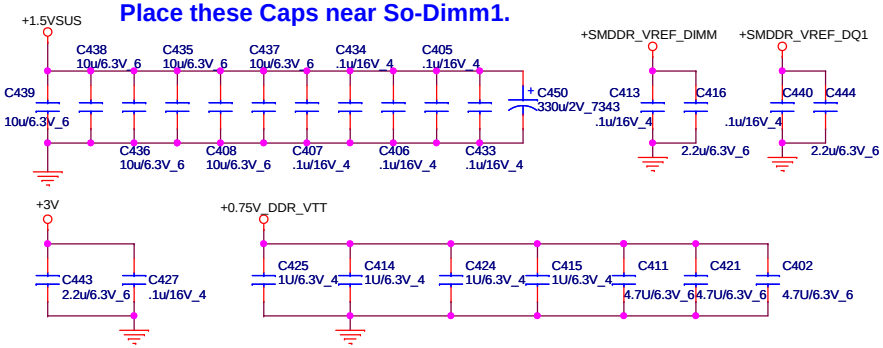

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	DDRIII SO-DIMM-1	1A
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CRT Switch

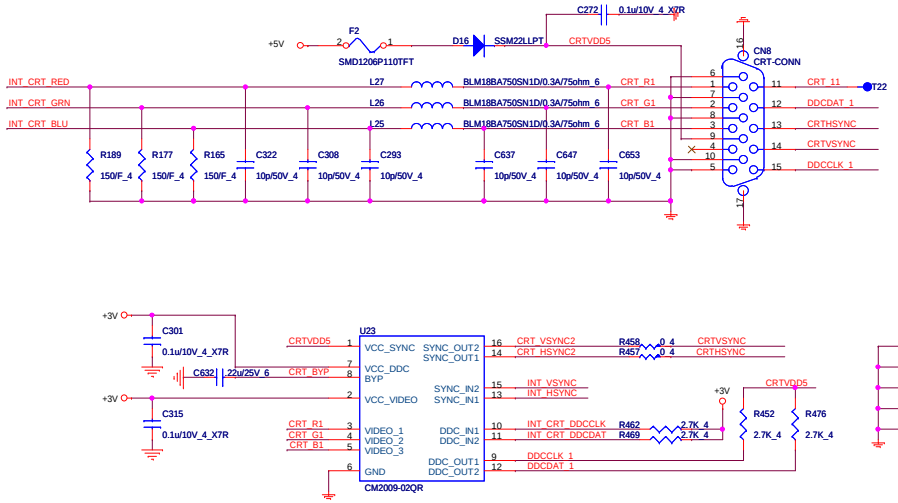
0_ohm Resistor place close to Joint-Point

<8> INT_CRT_RED — INT_CRT_RED
<8> INT_CRT_GRN — INT_CRT_GRN
<8> INT_CRT_BLU — INT_CRT_BLU

<8> INT_VSYNC — INT_VSYNC
<8> INT_HSYNC — INT_HSYNC

<8> INT_CRT_DDCDAT — INT_CRT_DDCDAT
<8> INT_CRT_DDCCLK — INT_CRT_DDCCLK

CRT



LVDS

0_ohm Resistor place close to Joint-Point

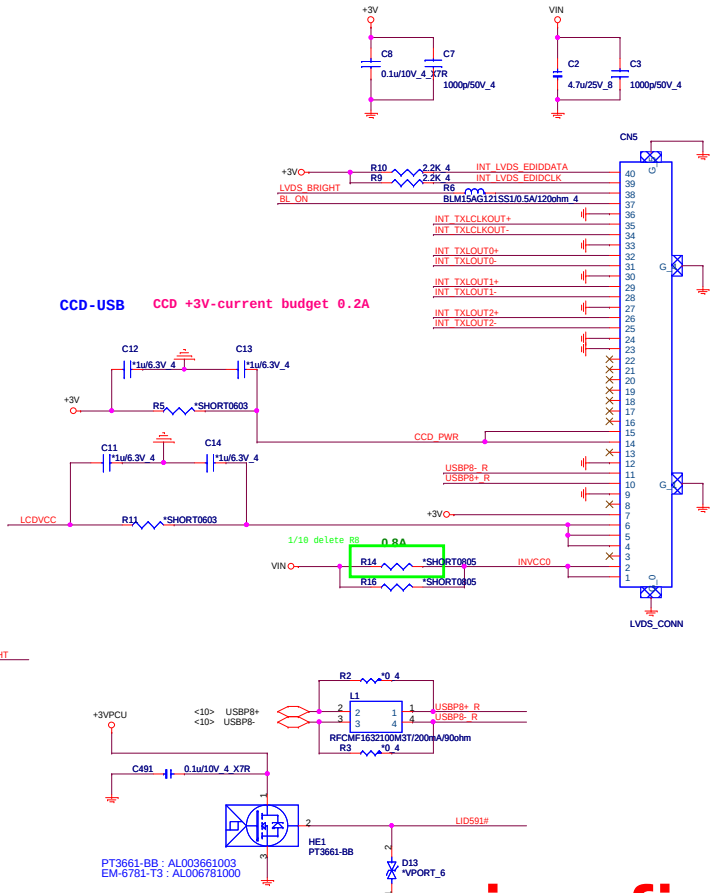
<8> INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
<8> INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA

<8> INT_LVDS_DIGON — INT_LVDS_DIGON
<8> INT_LVDS_BLON — INT_LVDS_BLON

<8> INT_TXLCLKOUT+ — INT_TXLCLKOUT+
<8> INT_TXLCLKOUT- — INT_TXLCLKOUT-
<8> INT_TXLOUT0+ — INT_TXLOUT0+
<8> INT_TXLOUT0- — INT_TXLOUT0-
<8> INT_TXLOUT1+ — INT_TXLOUT1+
<8> INT_TXLOUT1- — INT_TXLOUT1-
<8> INT_TXLOUT2+ — INT_TXLOUT2+
<8> INT_TXLOUT2- — INT_TXLOUT2-

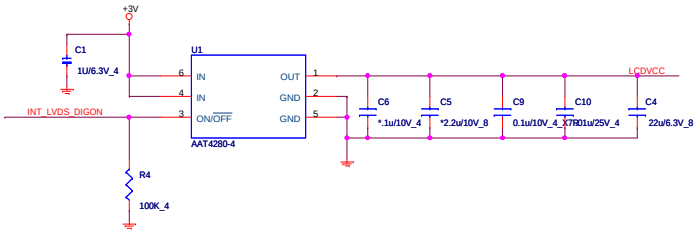
<27> CONTRAST — R7 *0_4 — LVDS_BRIGHT
<8> INT_LVDS_BRIGHT — R13 0_4

CCD-USB CCD +3V-current budget 0.2A

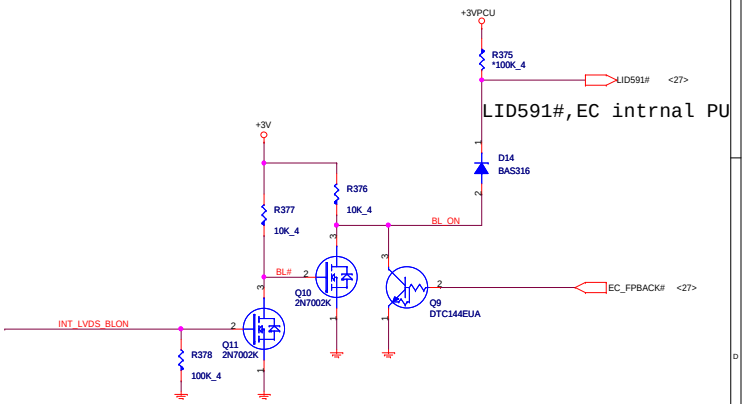


Lid Switch (Hall Sensor)

LCD Power



Backlight Control



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	CRT/LVDS/CAMERA/LID	1A
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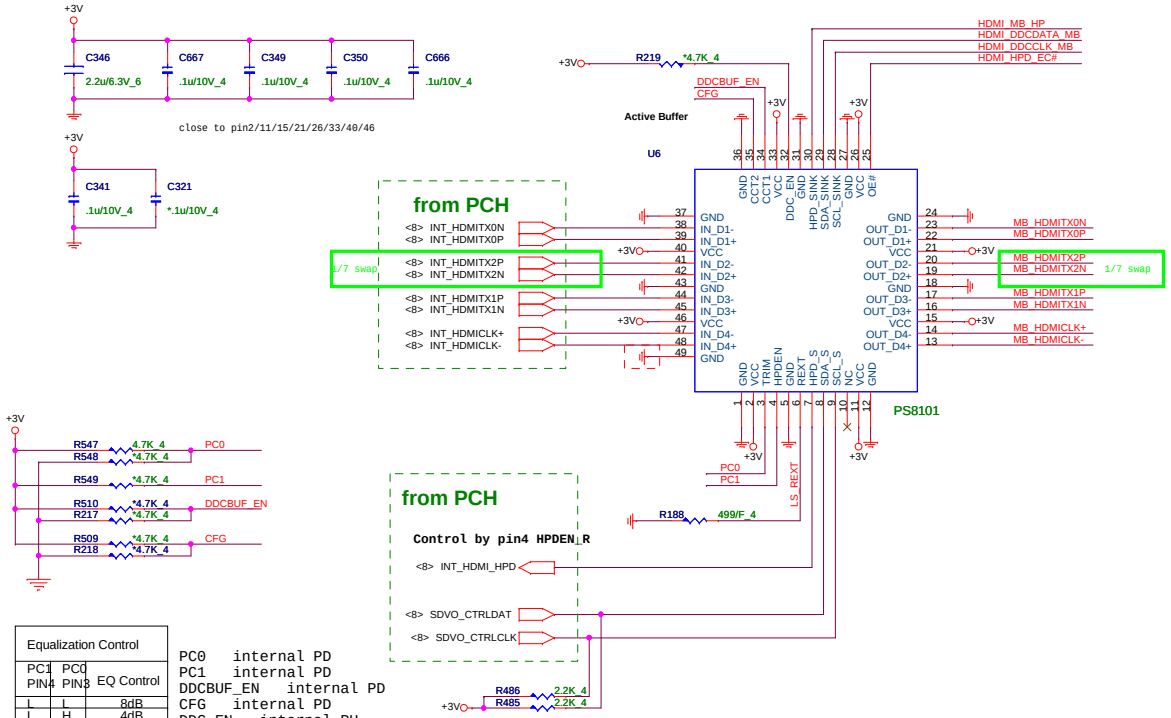
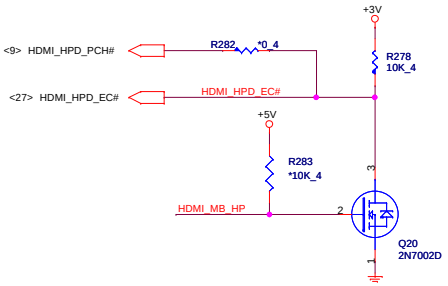
HDMI LEVEL SHIFTER



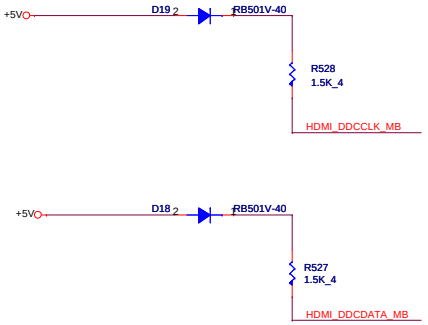
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

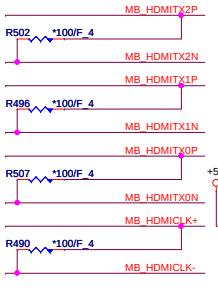
HDMI-detect



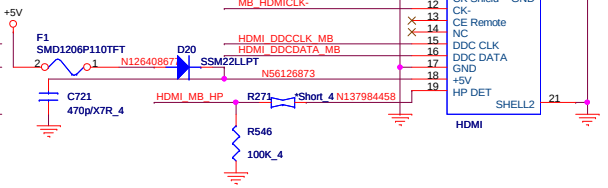
I2C



EMI



HDMI connector



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Size	Document Number	Rev
	HDMI (PS8101)	1A
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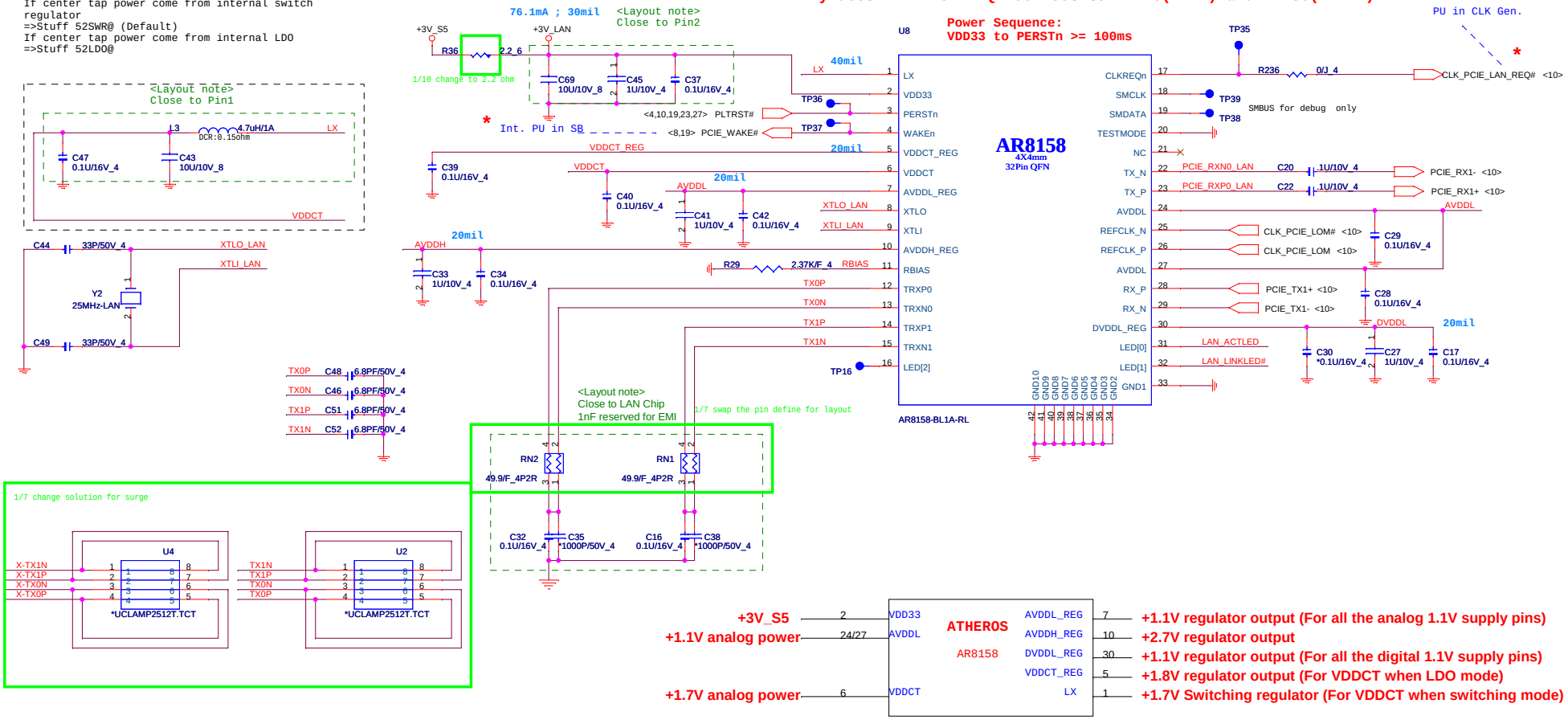
LAN (LAN)

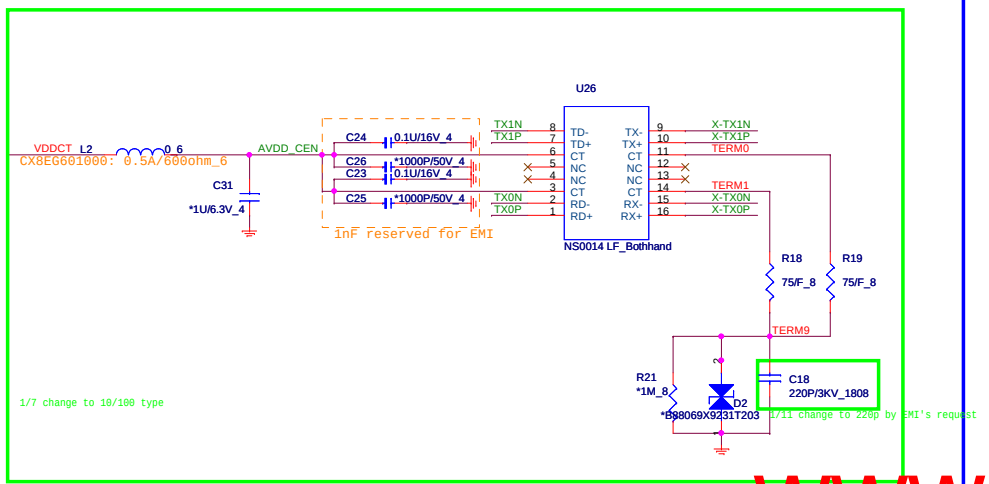
<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

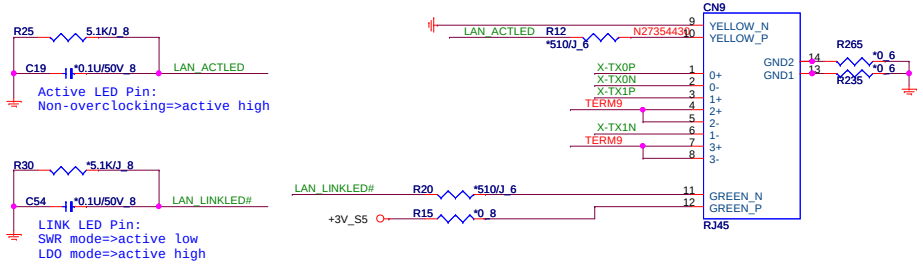
Power Sequence:
VDD33 to PERSTn >= 100ms



TRANSFORMER (LAN)



RJ45 Connector (LAN)



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	LAN AR8158L		1A
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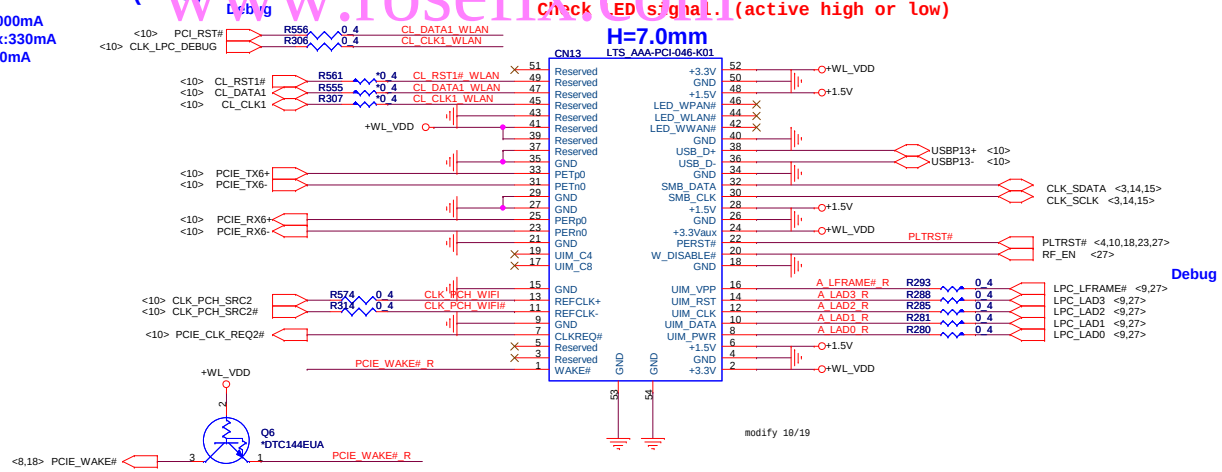
MINI-CARD WLAN(MPC)

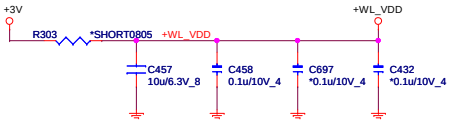
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

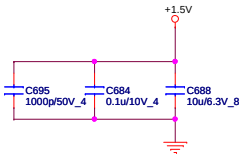
Debug

Check ED signal.(active high or low)

H=7.0mm







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	MINI PCI-E card/TV	1A
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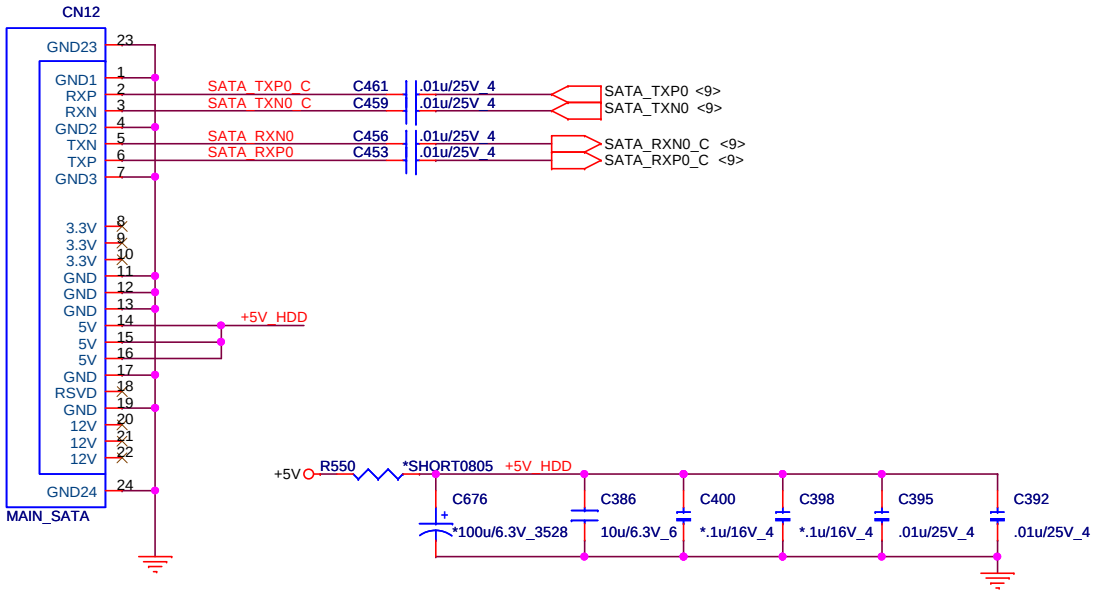
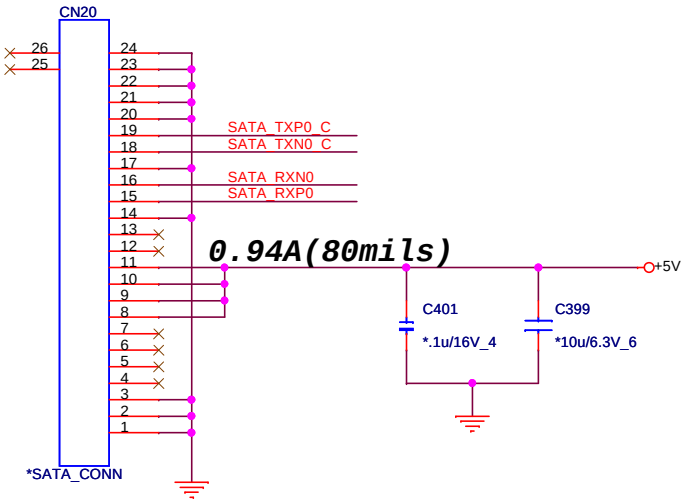
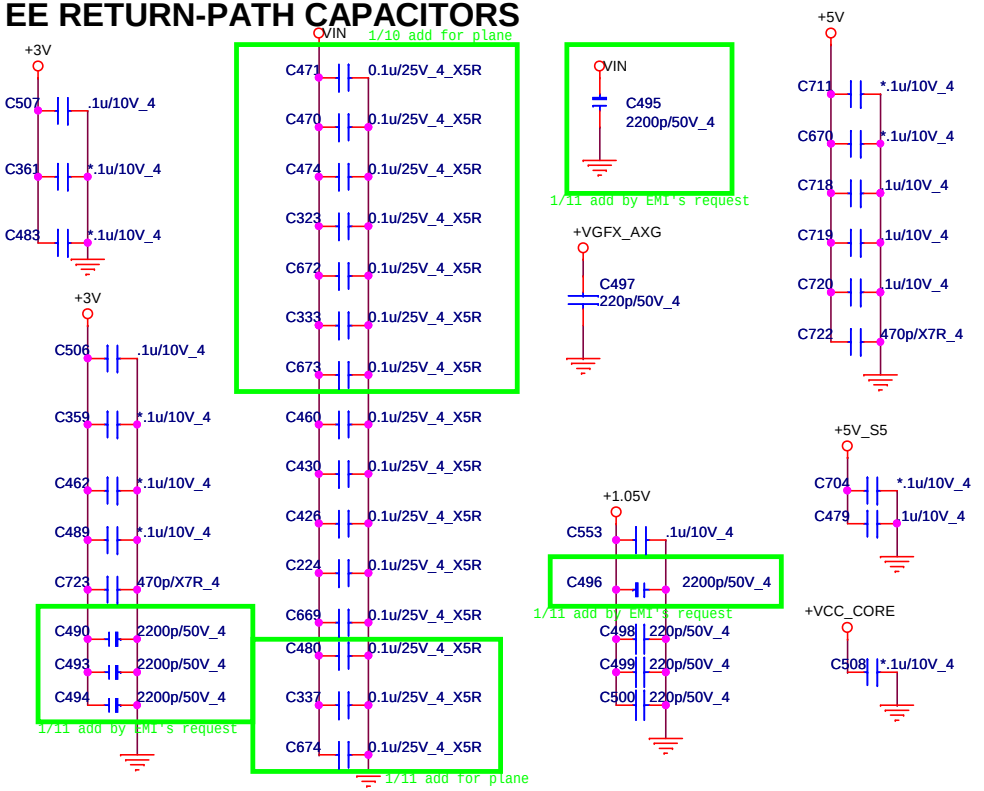
MAIN SATA HDD



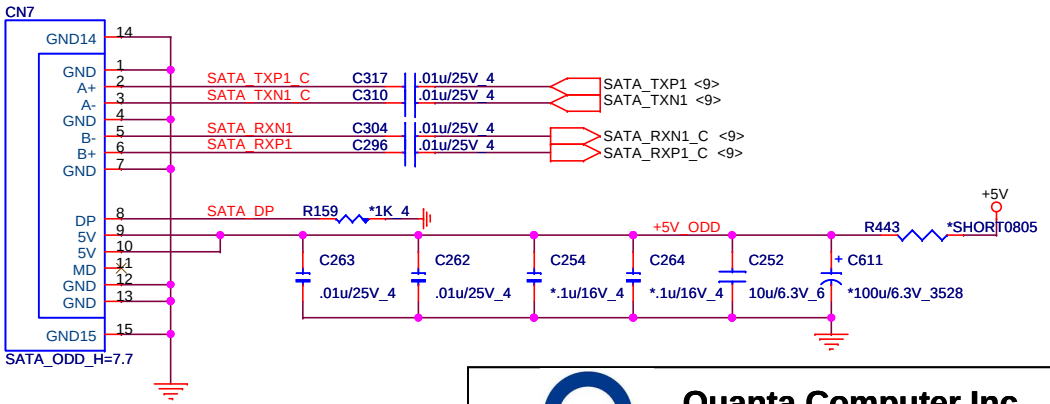
2.5" SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



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	SATA-HDD/ODD/USB-ESATA	1A
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Codec(ADO)

HP

Mute(ADO)

MIC

(Vista Premium Version)

ANALOG

DIGITAL

Spilt by AGND

Spilt by DGND

reverse R441

Place next to pin 38

Place next to pin 46

Place next to pin 1

Place next to pin 27

Place next to pin 25

Place next to pin 9

PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion

1.6Vrms

0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer

ALC271X-VB3-GR

Power (ADO)

C730, C787 close U37 pin3 and L65

Tied at one point only under the codec or near the codec

INT MIC array

cap place close to MIC-connector

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Size	Document Number: REALTEK ALC663&888/MDC
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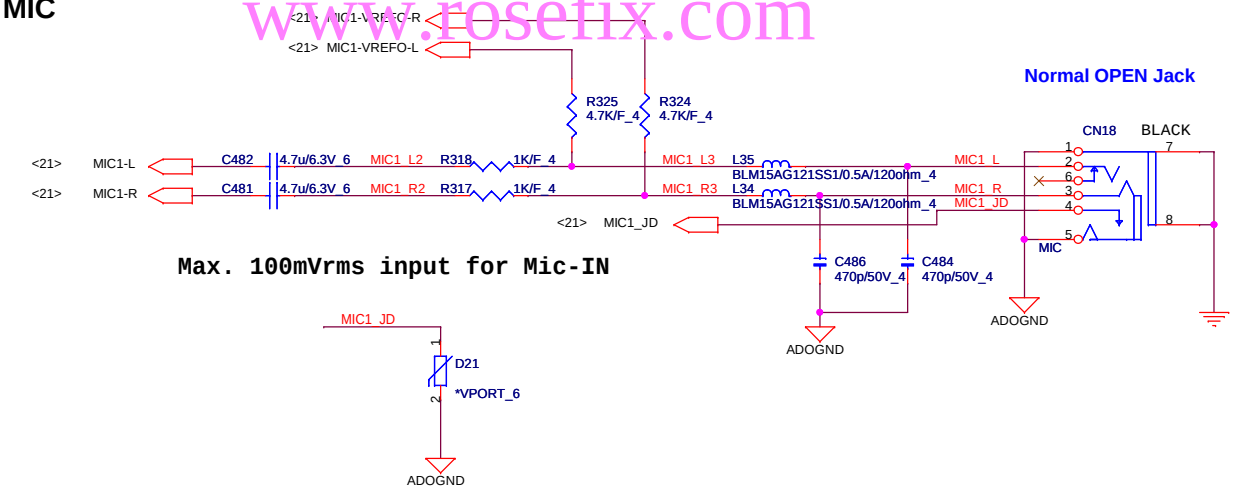
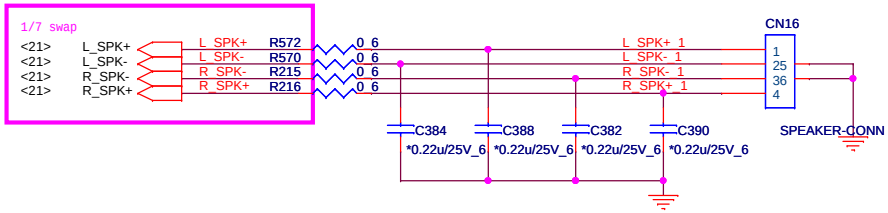
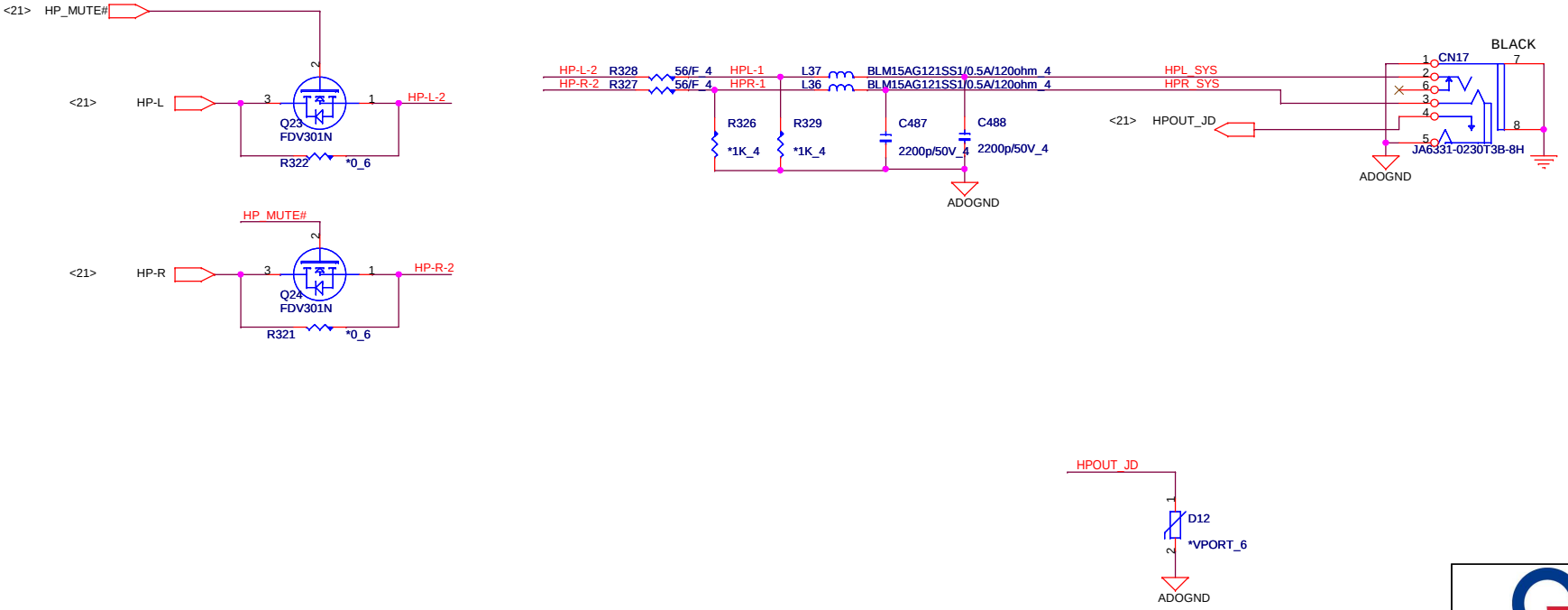
MIC



Internal Speaker



HP/SPDIF



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	AMP /AUDIO JACK CONN	1A
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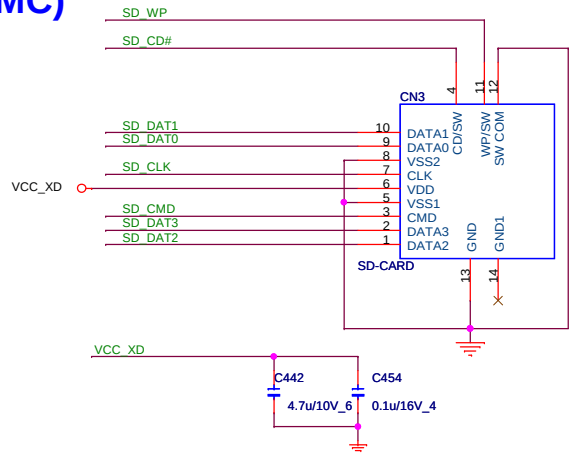
CARD READER Controller
AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033



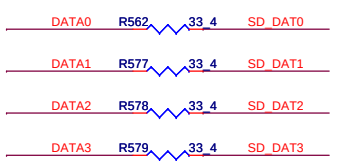
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

PIN43=Power saving mode enable.
'1' for enable [Default]
'0' for disable

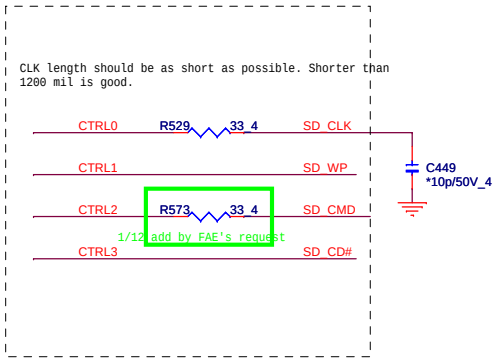
CTRL0, CRTL 1 trace length shorter , and surround with GND.

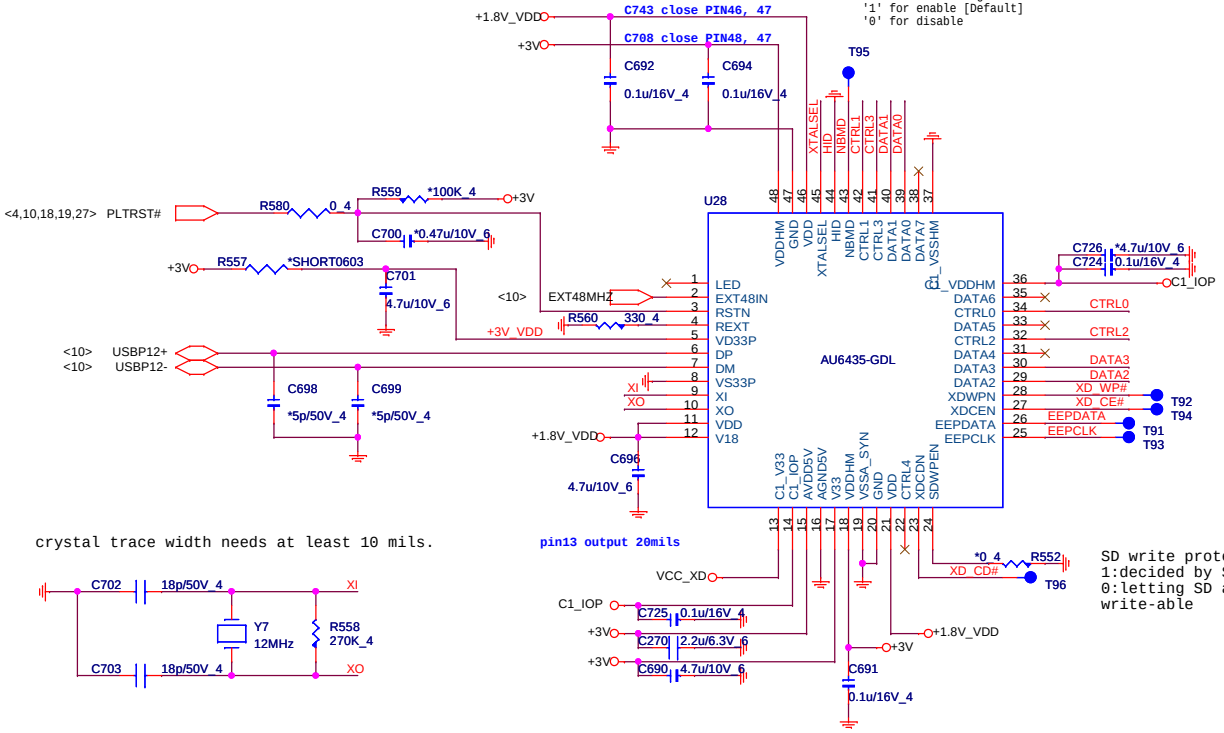
The trace length difference for each card interfaces should be smaller than 500 mil



Close to connector

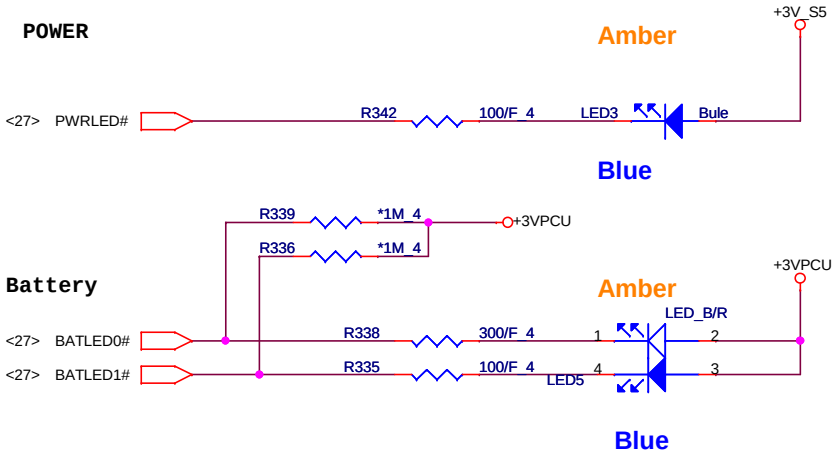
CLK length should be as short as possible. Shorter than 1200 mil is good.





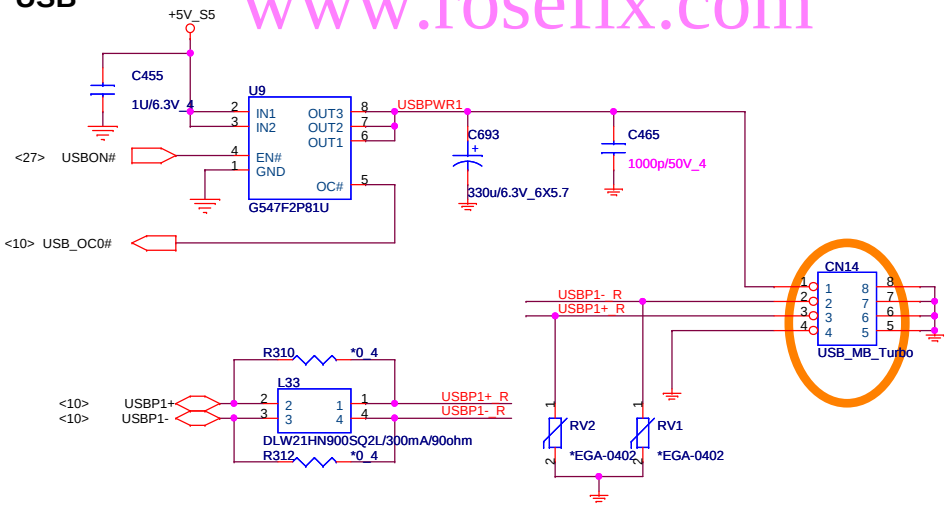
PROJECT : ZQ5 Quanta Computer Inc.			
Size	Document Number		Rev
	AU6433 CardReader		1A
Date:	Monday, March 14, 2011	Sheet 23 of	43

LED

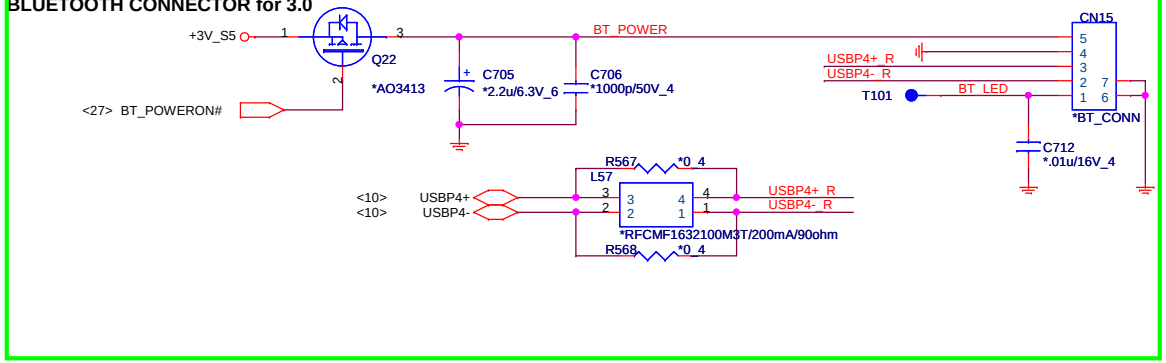


Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1A
Date: Monday, March 14, 2011	Sheet 24 of 35	

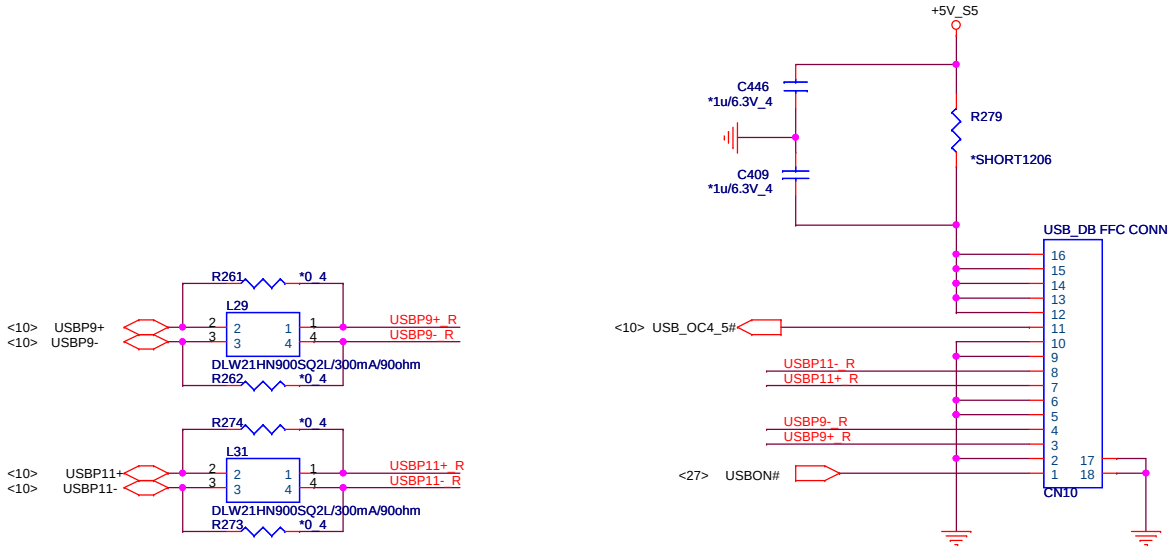
USB



BLUETOOTH CONNECTOR for 3.0



USB/B



Quanta Computer Inc.

PROJECT : ZQH

Size	Document Number	Rev
	USB/ BT	1A

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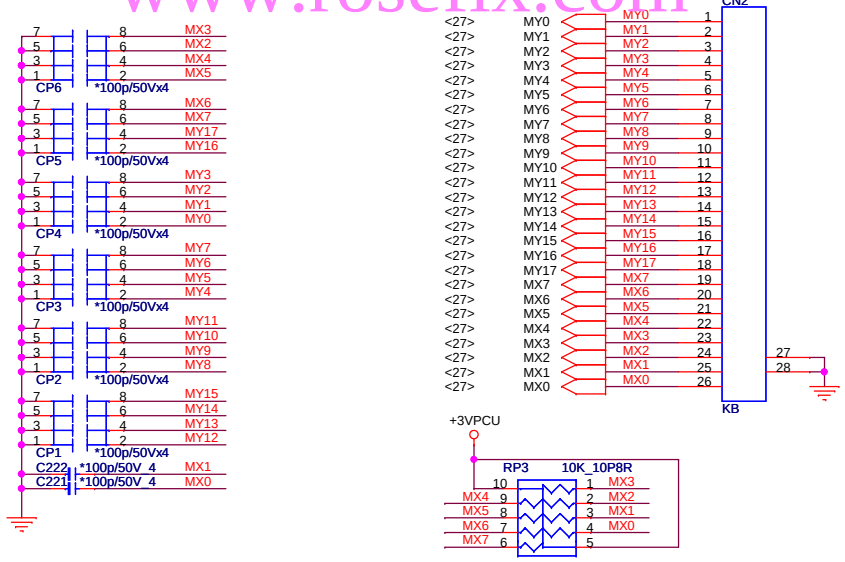
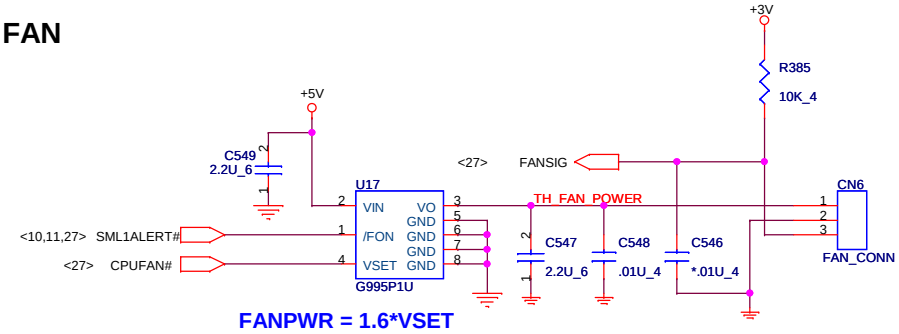
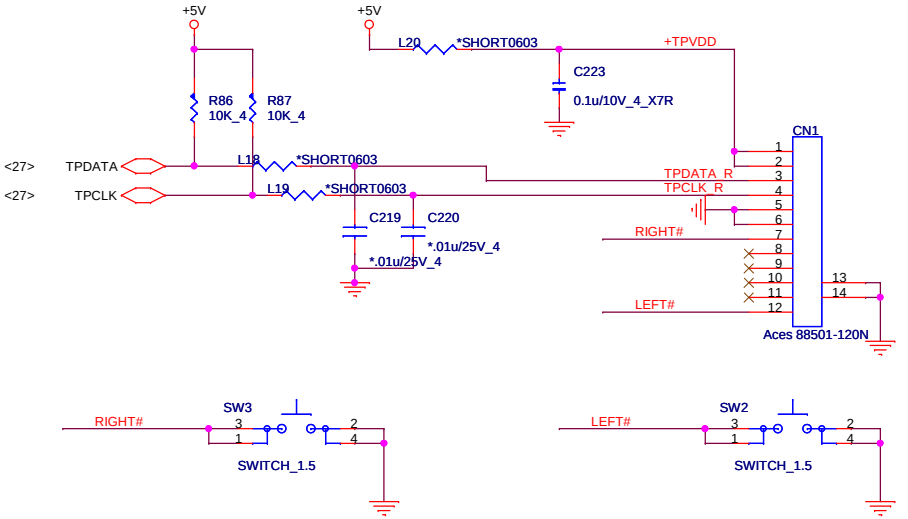
K/B



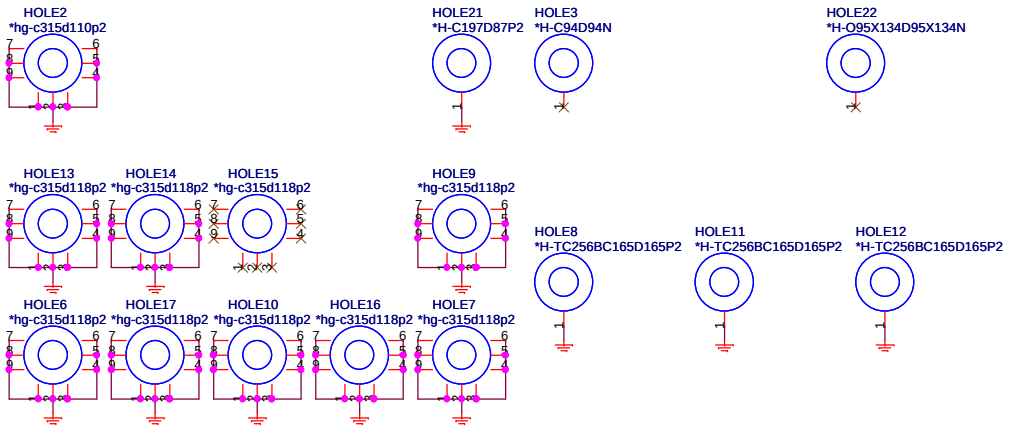
CPU FAN



TOUCHPAD & Switch CONN.

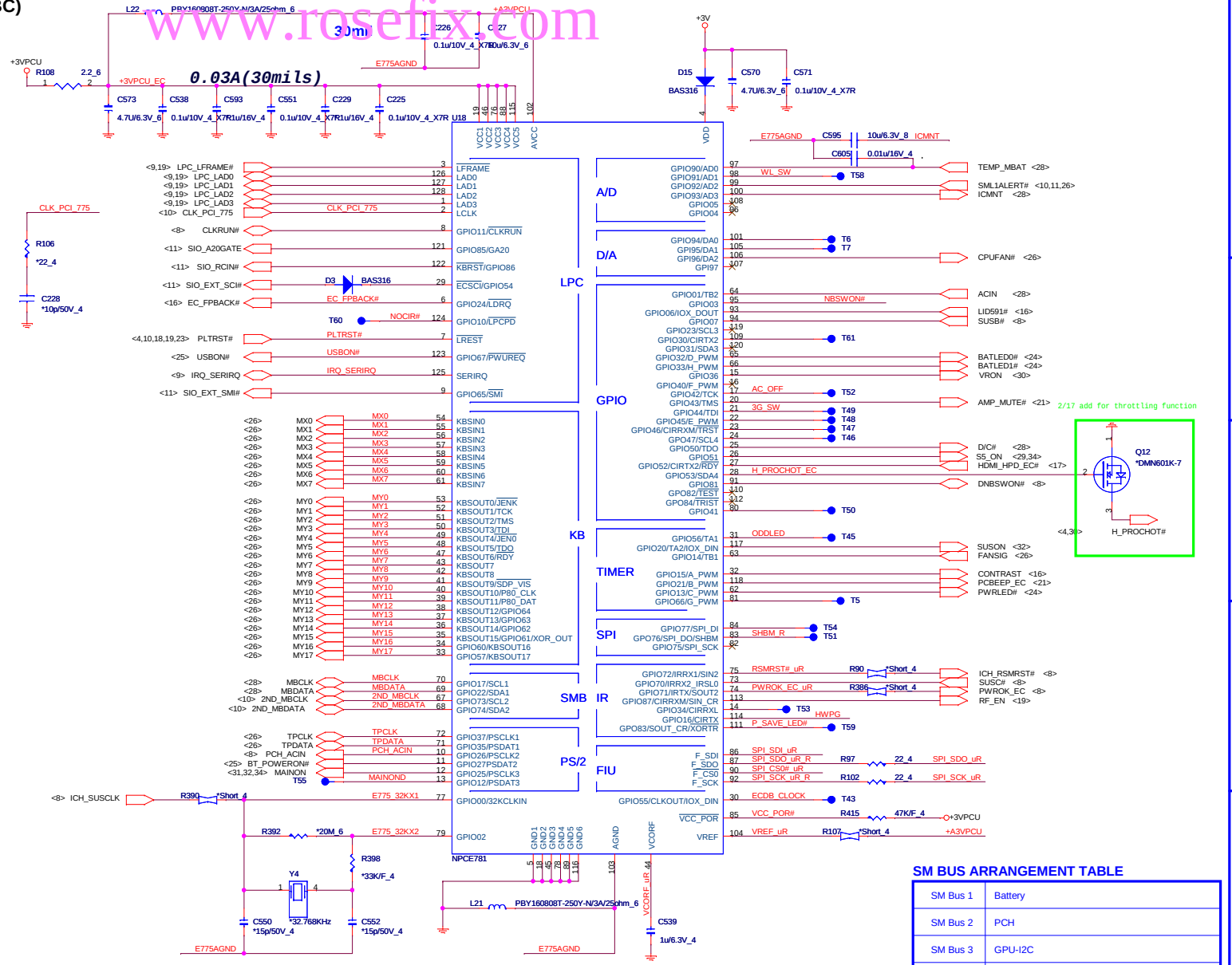


HOLE



Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date: Monday, March 14, 2011	Sheet 26 of 35	

EC(KBC)



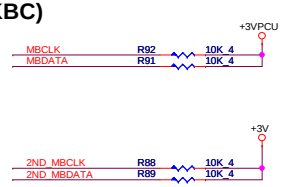
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

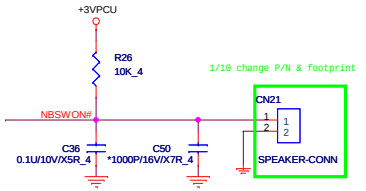
SHBM R405 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

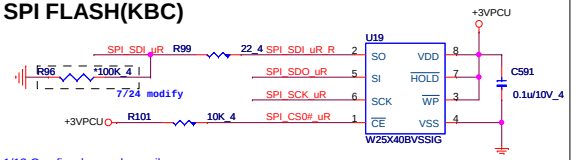
SM BUS PU(KBC)



PWR/B

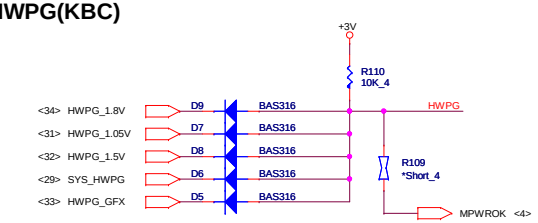


SPI FLASH(KBC)



1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

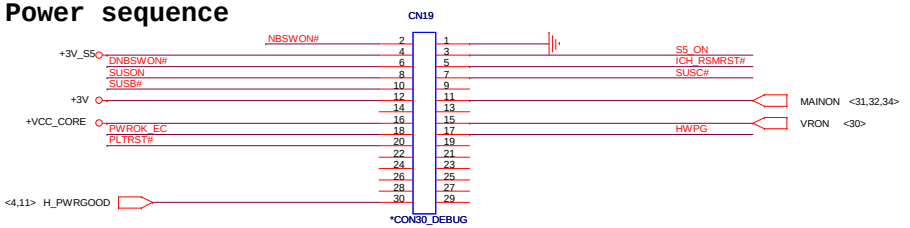
HWPG(KBC)



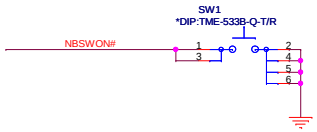
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

Power sequence



POWER-ON Switch(KBC)

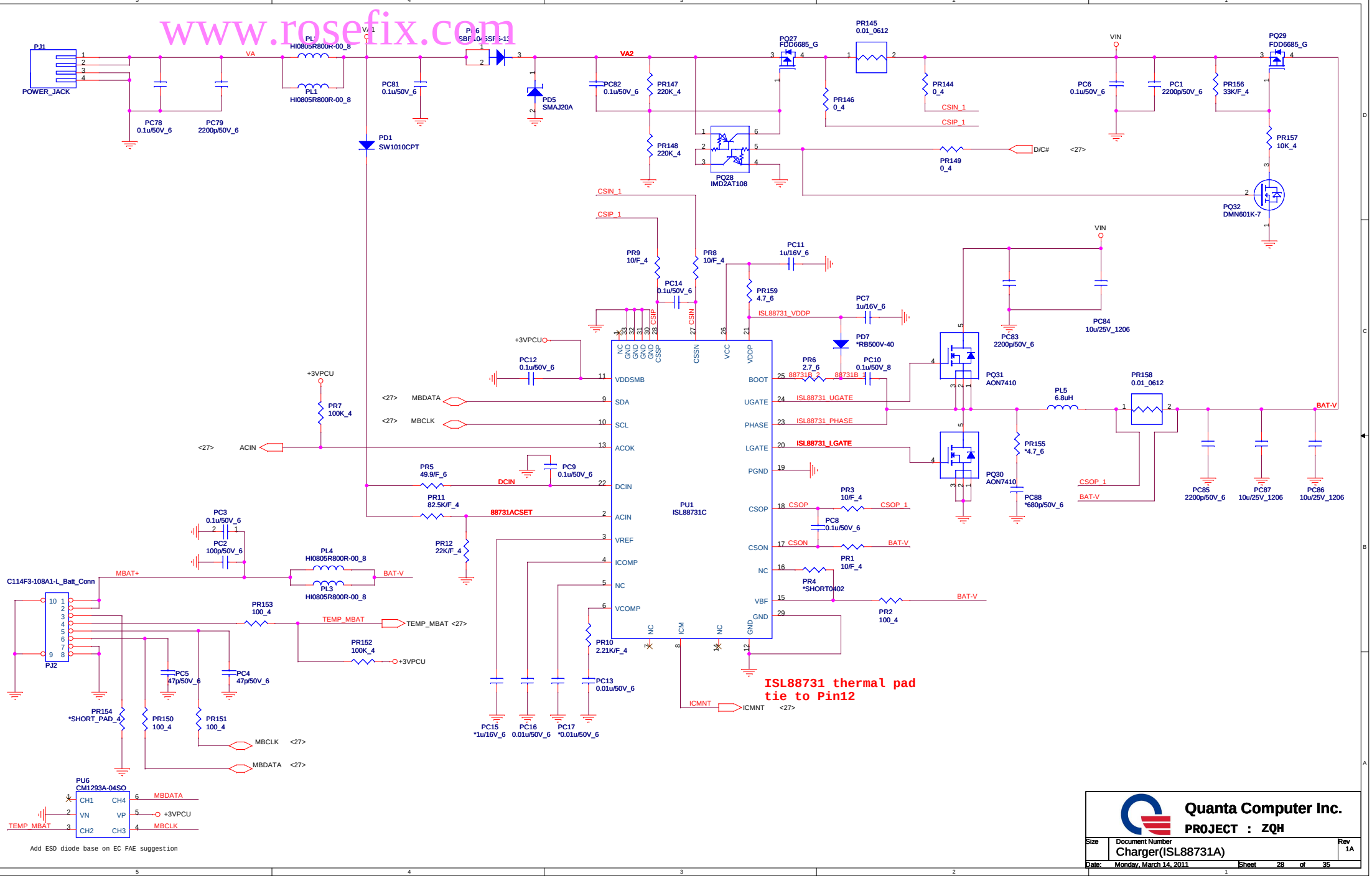


INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	WPCE781 & FLASH	1A

Date: Monday, March 14, 2011 Sheet 27 of 35

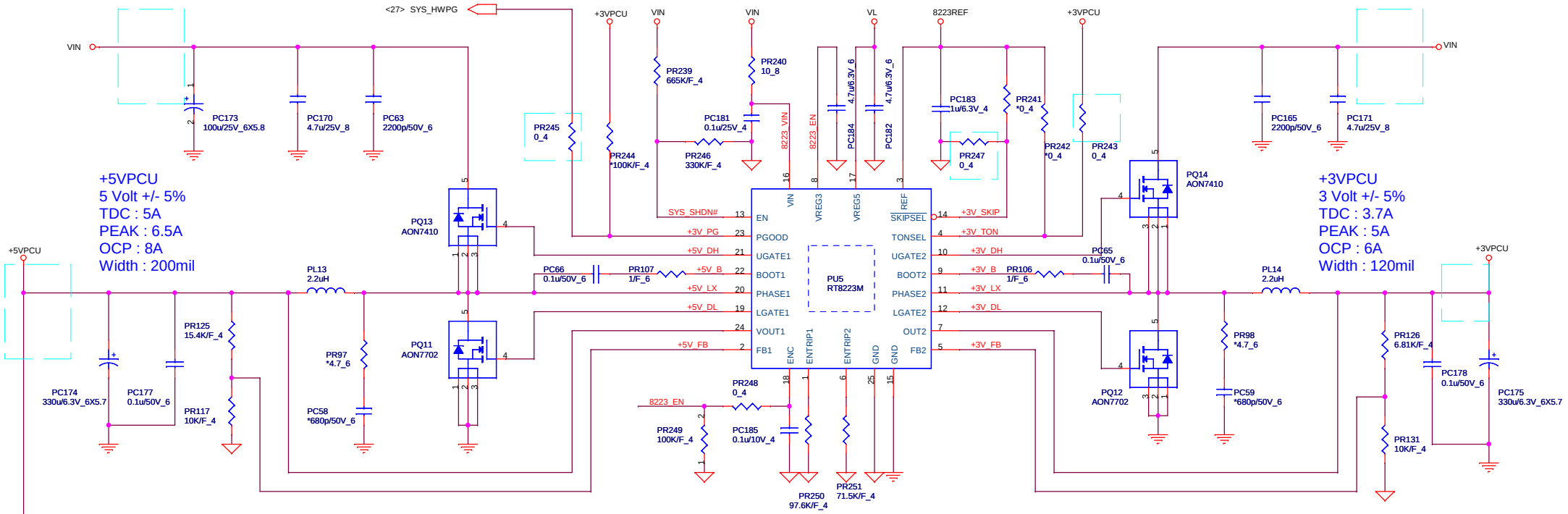


Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Monday, March 14, 2011	Sheet 28 of 35	

MAIND — MAIND <32,34> — SYS_SHD_# — SYS_SHDN <4,34>

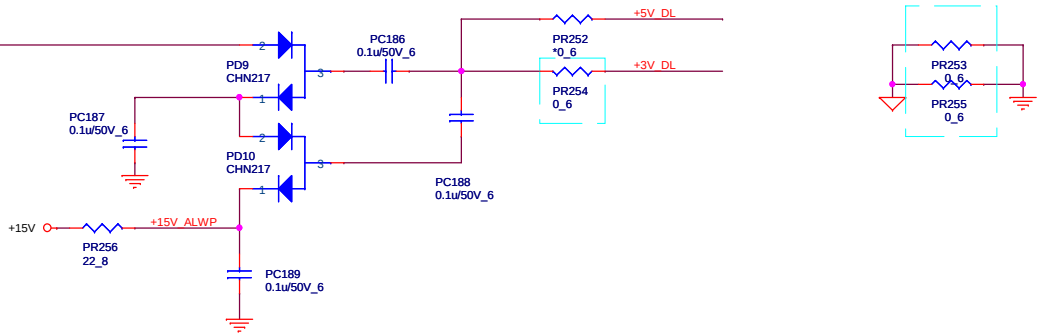
Ven=7.23V



OCP:8A

L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A

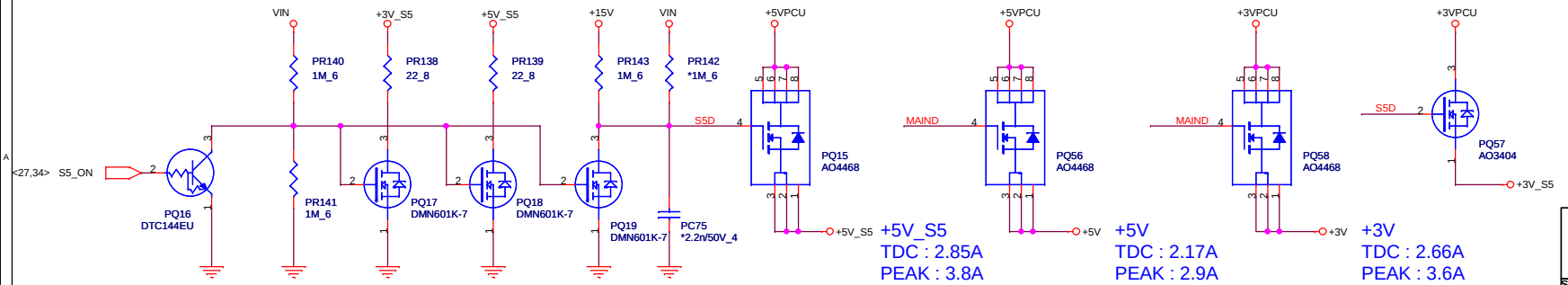
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K



OCP:6A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A

Iocp=6-(1.9/2)=5.05A
Vth=5.05A*14mOhm=70.7mV
R(Ilim)=(70.7mV*10)/10uA
=70.7K



+5V_S5
TDC : 2.85A
PEAK : 3.8A
Width : 120mil

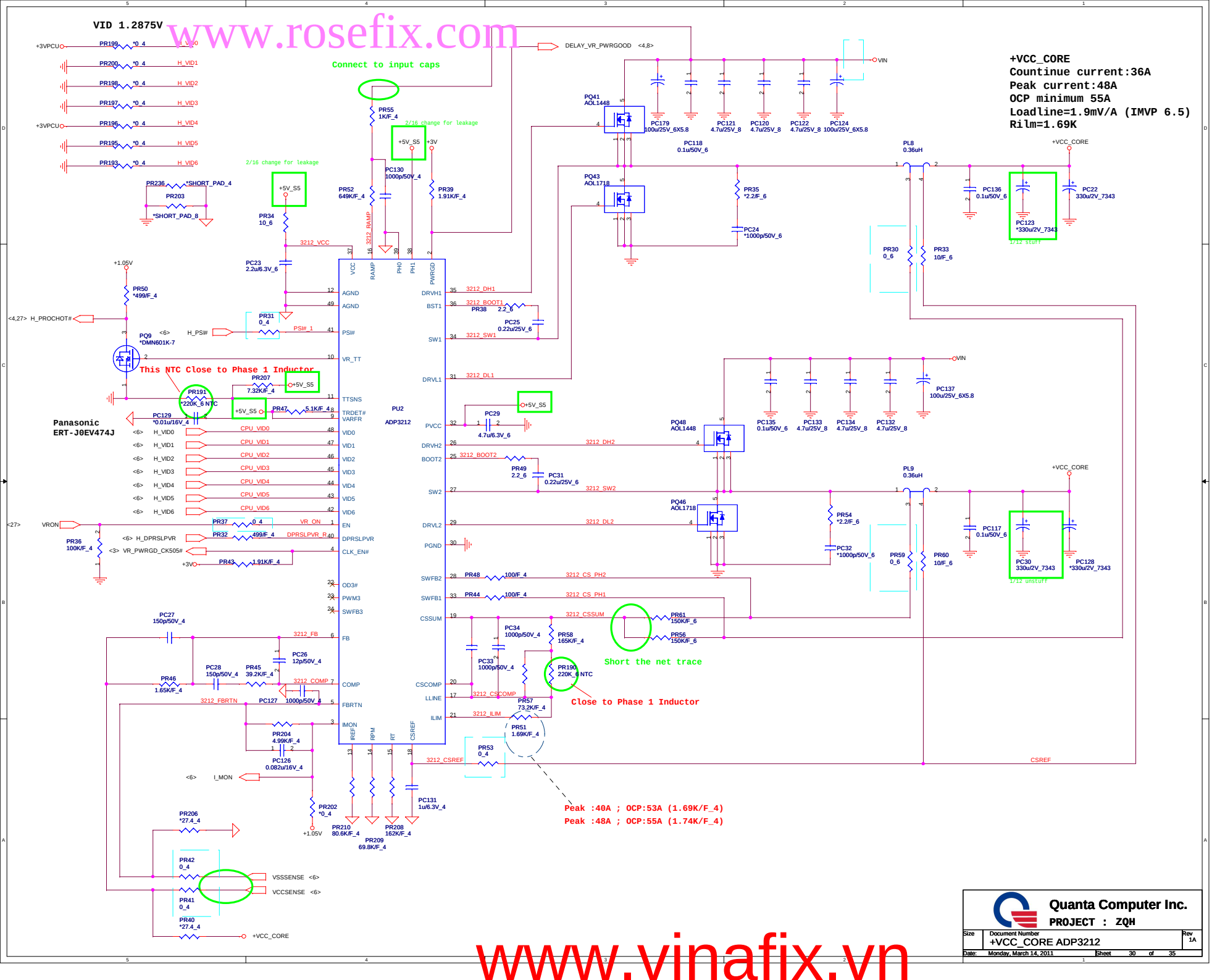
+5V
TDC : 2.17A
PEAK : 2.9A
Width : 90mil

+3V
TDC : 2.66A
PEAK : 3.6A
Width : 120mil

+3V_S5
TDC : 0.23
PEAK : 0.3A
Width : 20mil

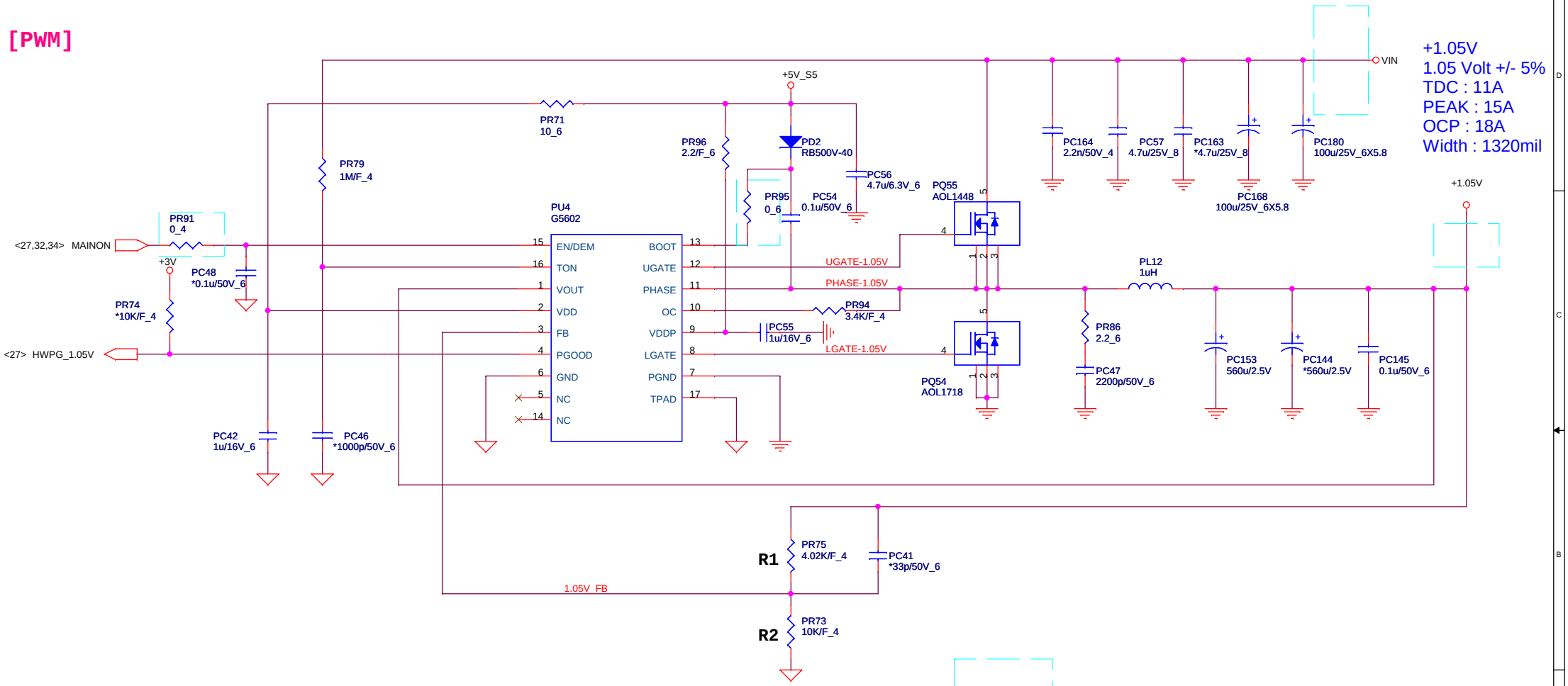
Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date: Monday, March 14, 2011	Sheet 29 of 35	



Quanta Computer Inc.	
PROJECT : ZQH	
Size	Document Number: +VCC_CORE ADP3212 — Rev: 1A
Date: Monday, March 14, 2011	Sheet 30 of 35

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

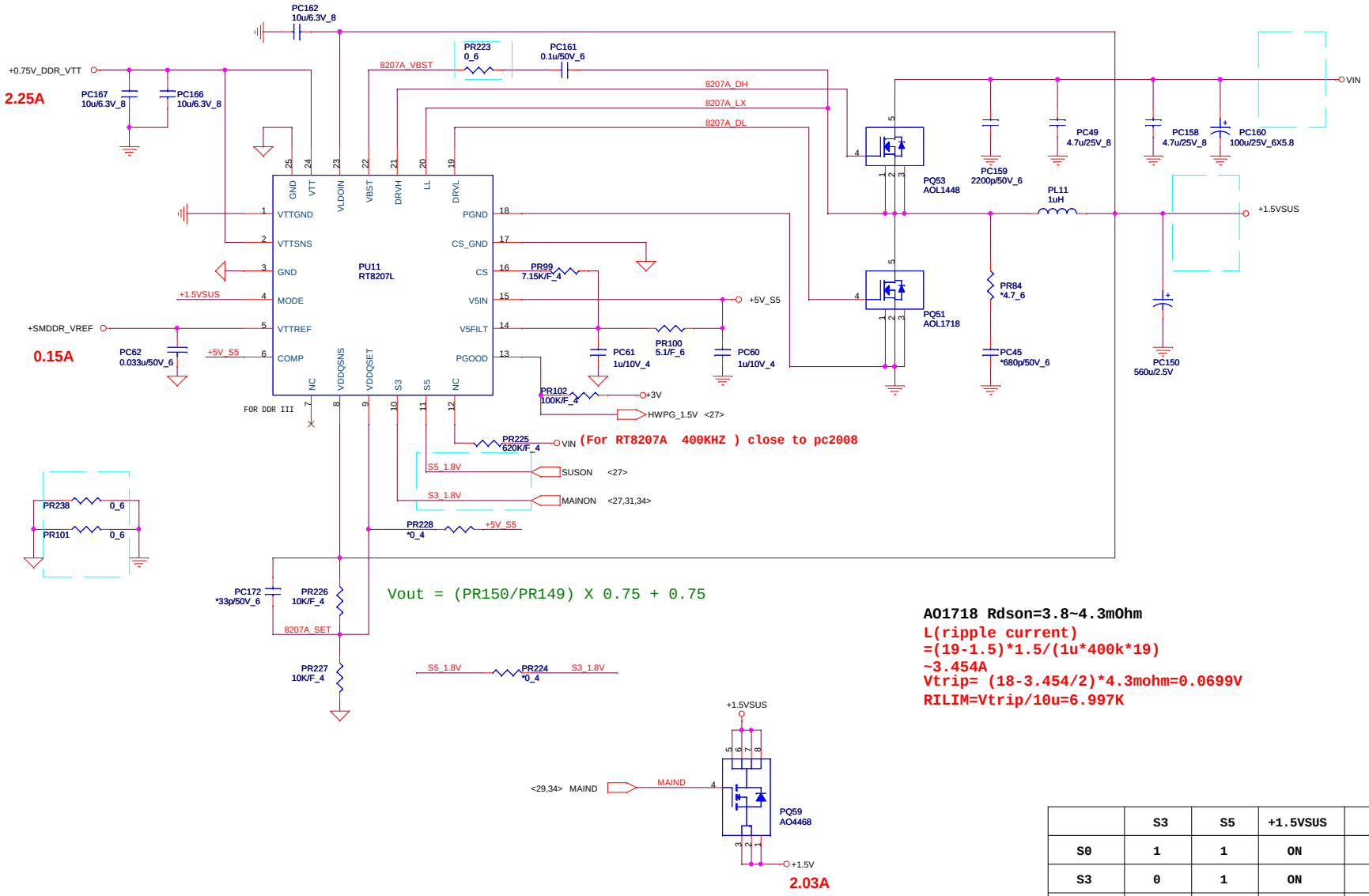
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.647A

RILIM=4.3mohm*18-1.823/20uA=3.477Kohm

I(choke)peak=21.647A

Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: +VTT (G5602R41U)	Rev: 1A
Date: Monday, March 14, 2011	Sheet 31 of 35	

[PWM]



+1.5V_SUS
1 Volt +/- 5%
TDC : 12A
PEAK : 16A
OCP : 18A
Width : 480mil

AO1718 Rdson=3.8~4.3mOhm

L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (18-3.454/2)*4.3mohm=0.0699V
RILIM=Vtrip/10u=6.997K

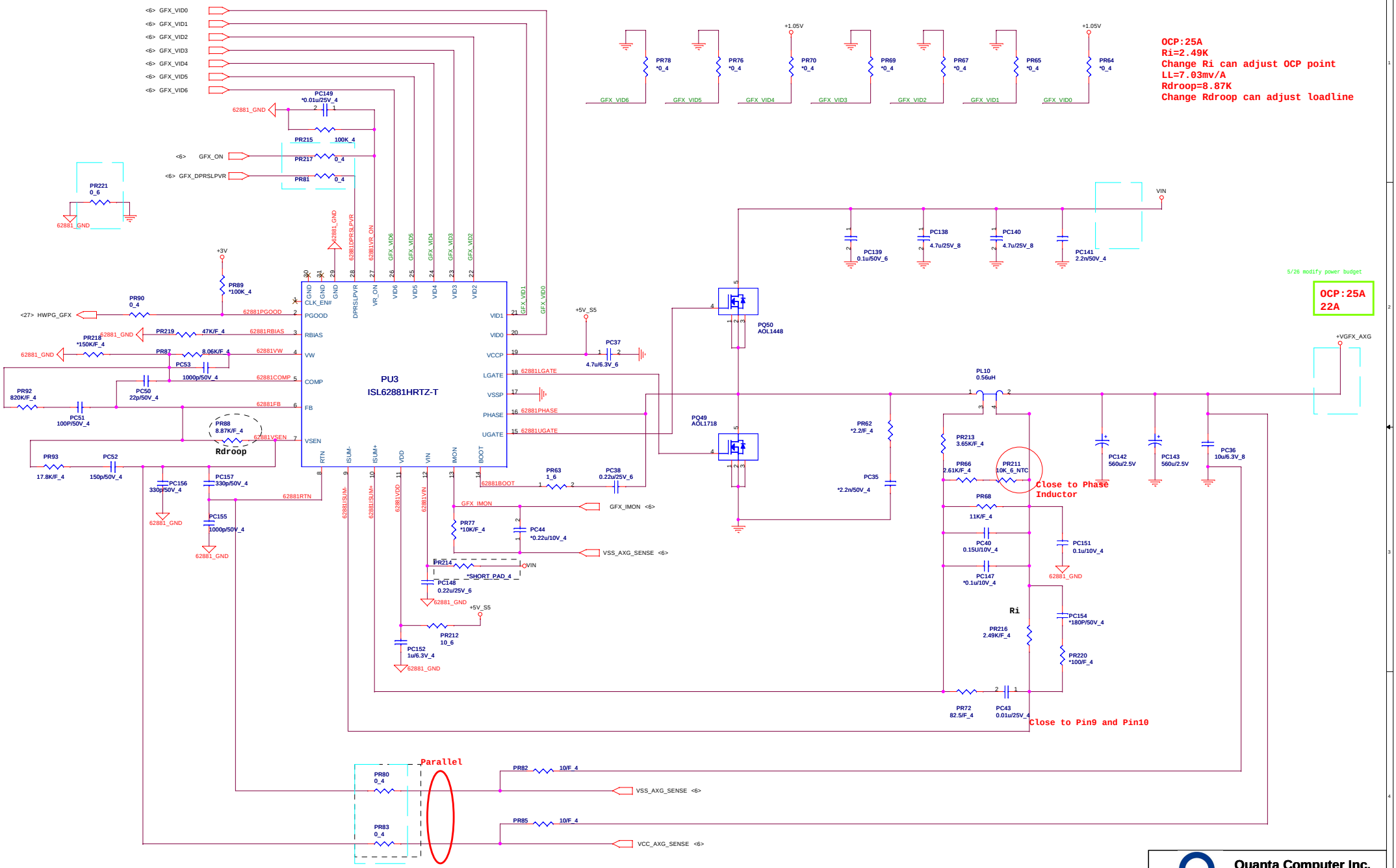
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

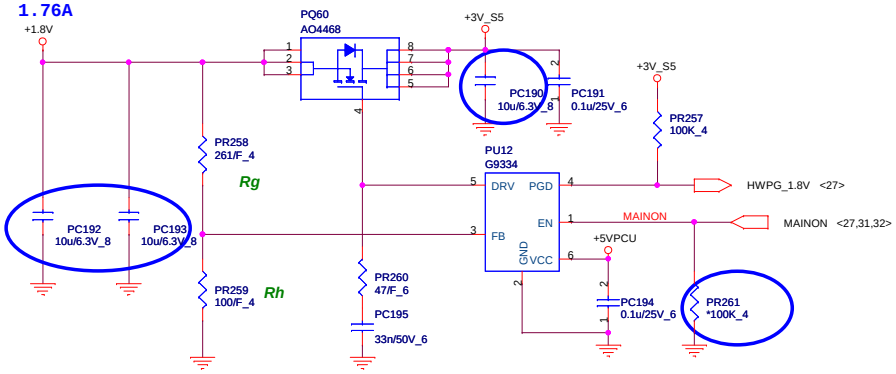
Date: Monday, March 14, 2011 Sheet 32 of 35

Int_VGA [PWM]



+1.8V
1.8 Volt +/- 5%
TDC : 0.76A
PEAK : 1.01A
Width : 40mil

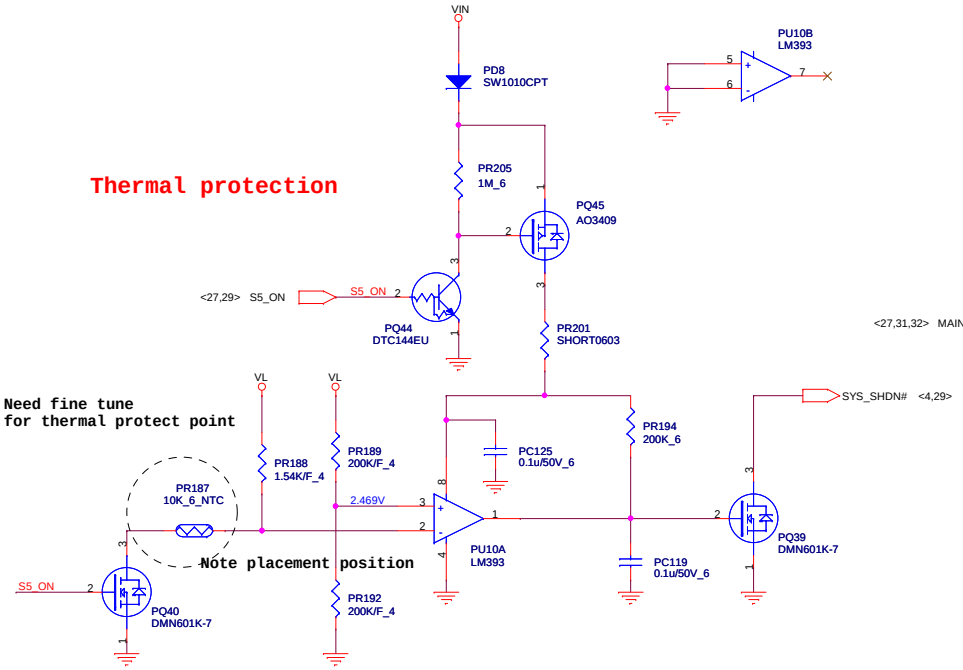
1.76A

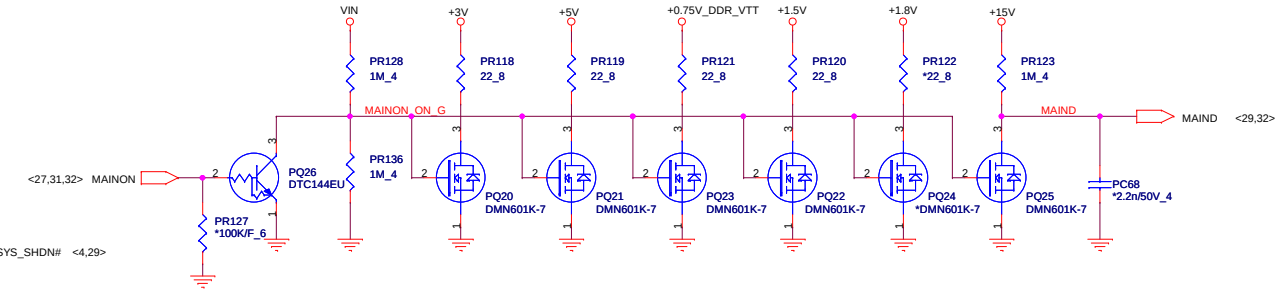


*Vout1 = (1+Rg/Rh)*0.5*

For EC control thermal protection (output 3.3V)

Thermal protection





Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	Discharge/1.8V)	1A
Date: Monday, March 14, 2011	Sheet 34 of 35	

7/7 modify

CHANGE LIST

Model	REV	CHANGE LIST
ZQH	1A	1/7 page.24 U6 HDMI pin 19,20 & pin 41,42 swap for layout page.30 CN16 speaker conn. pin1,2,3,4 swap for layout page.25 U26 transformer change to 10/100 type page.25 U2, U4 change type, add D2, R21 for surge solution. page.25 RN1, RN2 swap the pin define for layout page.29 R337 change to 2.2K, R476 change to 10u by FAE's recommend 1/10 page.16 delete R8 page.20 add C323, C333, C470, C471, C474, C672, C673 for Vin plane page.27 change CN21 PWR/B connector P/N & footprint page.18 change R36 to 2.2 ohm 1/11 page.20 add C480, C337, C674 for Vin plane page.34 delete +1V LDO power circuit page.20 add C490, C493, C494, C495, C496 by EMI's request page.18 change C18 to 220P by EMI's request 1/10 page.30 stuff PC123, unstuff PC30 page.23 add R573 for FAE's request
	2A	2/14 Test-Point change footprint. TP3075 change to TP2675 TP3050 change to TP2650 2/14 page.21 Add R574 & R575 page.21 R599 chane to 10K ohm resistor. 2/14 page.30 PC123 unstuff , PC30 stuff. page.27 unstuff SW1 & CN19 page.25 unstuff Bluetooth group. page.26 EMI CP1, CP2, CP3, CP4, CP5, CP6 stuff 100pF cap array page.20 EMI stuff C553 , ADD C361/C483/C507,C497,C498,C499,C500. page.16 EMI stuff C619/C620 2/14 page20 Reserve C508 2/14 page19 LED5 , PIN1 connect to<BATLED0#>& PIN4 connect to<BATLED1#> 2/14 page16 add R16 C671 & C40 change to TOP side. 2/14 FDI :: delete R152/R161/R157/R171/R167 , R454/R470/R481/R487/R464/R480/R500/R495/R459/R475/R478/R491/R461/R484/R498/R493 Change to 0402short :: R149/R234/R233/R531/R524/R114/R163/R194/R271/R554/R107/R109/R386/R390/R90 2/14 Change to 0603short :: R113/R142/R168/R186/R169/R172/R174/R178/R185/R201/R213/R417/R268/R275/R299/R5/R11/R581/R587/R588/R557/L18/L19/L20 2/14 page.18 Add C46/C48/C51/C52 2/15 POWER cahnge to shortpad 2/15 page12 delete R116 & R124. Add C574. C598 & C604 change to TOP Add C339 , C340 page16 stuff C661 2/16 page.30 change +5V_PCU power to +5V_S5 for leakage 2/17 page.21 remove R574, R575 & add D10, D11 2/17 page.27 add Q12 and use GPIO53 for throttling function for 40W adaptor 2/17 page.21 change U10 P/N 2/17 page.16 change R14, R16 to 0805 shortpad page.18 change R15 to 0805 shortpad page.12 change R140, R162, R210,R424 to 0805 shortpad page.19 change R303 to 0805 shortpad page.20 change R443, R550 to 0805 shortpad 2/17 page.25 change R279 to 1206 shortpad 2/17 page.18 unstuff C30
	3C	3/10 page.27 Unstuff Q12 3/14 page25. L33 exchange order for USB signal routing. 3/14 page.18 R12 & R20 unstuff , R15 change to 0805 resistor and unstuff. 3/10 page.19 Add R314 & R574 , 0 ohm or CAP depend on result. 3/10 page.32 delete shortpad , PR229 & PR230
	4A	

MODEL ZQ9 — FROM / To

Quanta Computer Inc.
PROJECT : ZQH
Change list2

DOC NO.	PROJECT MODEL :	ZQH	APPROVED BY:		DATE:
	PART NUMBER:		DRAWING BY:		REVISON: