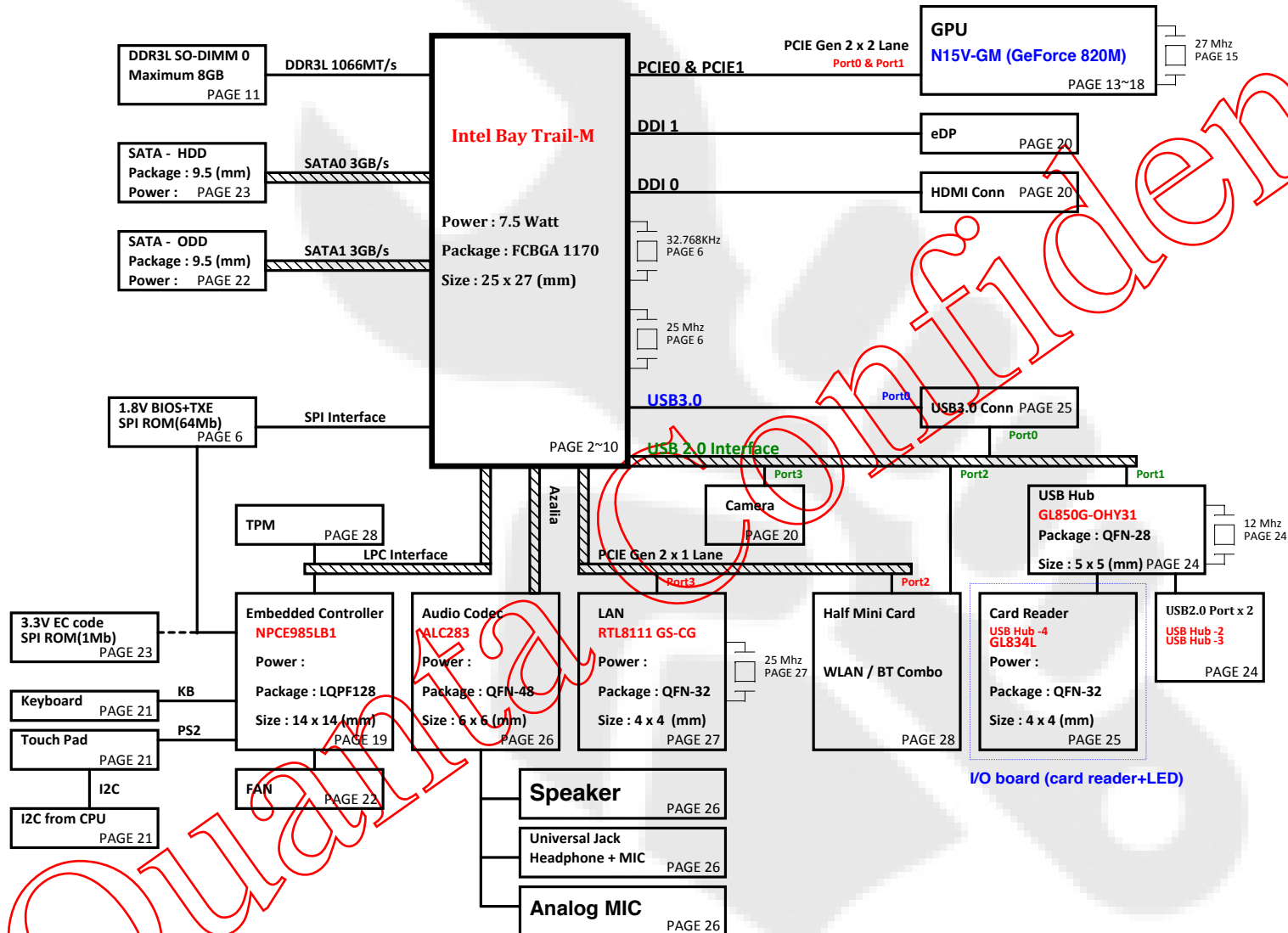


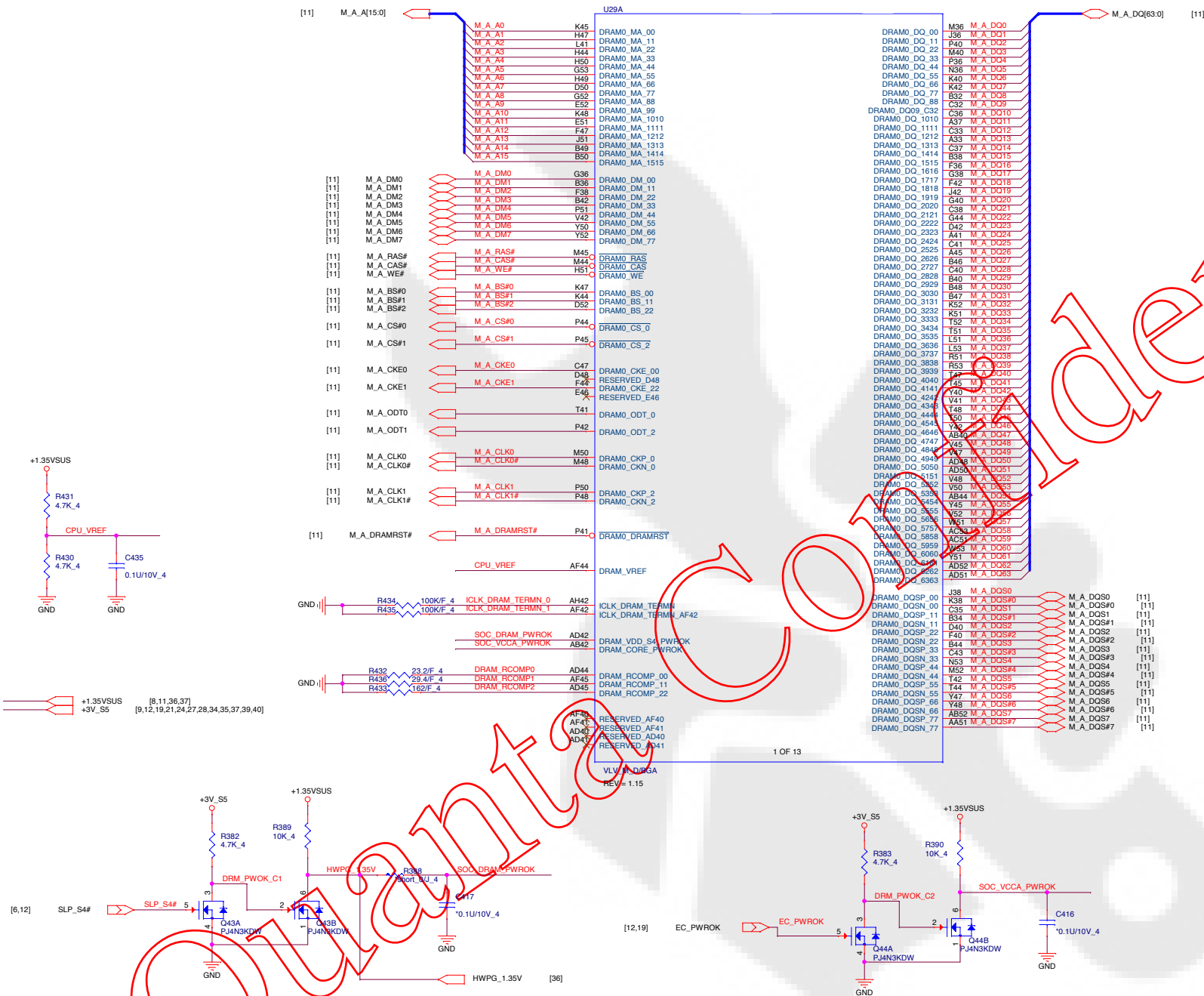
ZYL (17")

Intel Bay Trail-M Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SVCC
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SGND
 LAYER 6 : BOT





U29B

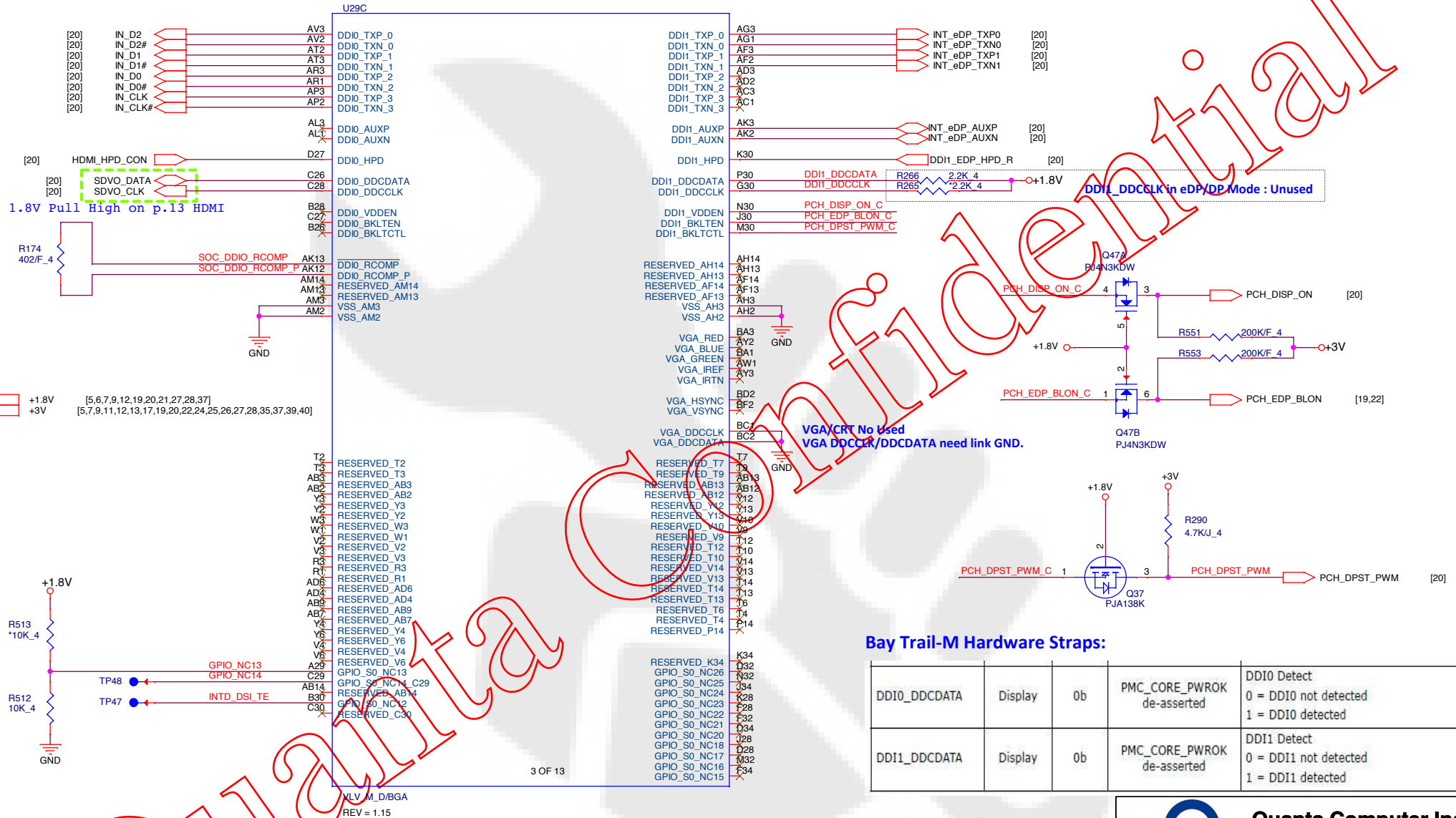
AY45	DRAM1_MA_00	DRAM1_DQ_00	BG38
BB40	DRAM1_MA_11	DRAM1_DQ_11	BD40
AW40	DRAM1_MA_22	DRAM1_DQ_22	BA42
BB40	DRAM1_MA_33	DRAM1_DQ_33	BD42
BC35	DRAM1_MA_44	DRAM1_DQ_44	BC38
BB40	DRAM1_MA_55	DRAM1_DQ_55	BF42
BF30	DRAM1_MA_66	DRAM1_DQ_66	BC44
BC35	DRAM1_MA_77	DRAM1_DQ_77	BH32
BE35	DRAM1_MA_88	DRAM1_DQ_88	BC32
AY48	DRAM1_MA_99	DRAM1_DQ_99	BG36
BD40	DRAM1_MA_1010	DRAM1_DQ_1010	BH37
BA30	DRAM1_MA_1111	DRAM1_DQ_1111	BG33
BH40	DRAM1_MA_1212	DRAM1_DQ_1212	BH33
BH40	DRAM1_MA_1313	DRAM1_DQ_1313	BG37
BH50	DRAM1_MA_1414	DRAM1_DQ_1414	BH38
	DRAM1_MA_1515	DRAM1_DQ_1515	BH36
		DRAM1_DQ_1616	AT36
BD38	DRAM1_DM_00	DRAM1_DQ_1717	AV40
BH38	DRAM1_DM_11	DRAM1_DQ_1818	AT40
BC36	DRAM1_DM_22	DRAM1_DQ_1919	BH36
BH42	DRAM1_DM_33	DRAM1_DQ_2020	AV36
AT30	DRAM1_DM_44	DRAM1_DQ_2121	AV42
AM42	DRAM1_DM_55	DRAM1_DQ_2222	AV40
AK30	DRAM1_DM_66	DRAM1_DQ_2323	BH41
AK35	DRAM1_DM_77	DRAM1_DQ_2424	BG41
AV45	DRAM1_RAS	DRAM1_DQ_2525	BH45
AV45	DRAM1_CAS	DRAM1_DQ_2626	BH46
BB30	DRAM1_WE	DRAM1_DQ_2727	BG40
AY42		DRAM1_DQ_2828	BH40
AY45	DRAM1_BS_00	DRAM1_DQ_2929	BH48
BF32	DRAM1_BS_11	DRAM1_DQ_3030	BH47
BF32	DRAM1_BS_22	DRAM1_DQ_3131	AV52
AT44	DRAM1_CS_0	DRAM1_DQ_3232	AV51
AT45	DRAM1_CS_2	DRAM1_DQ_3333	BH51
		DRAM1_DQ_3434	BH51
		DRAM1_DQ_3535	BH53
		DRAM1_DQ_3636	BH53
BG47	DRAM1_CKE_00	DRAM1_DQ_3737	SP47
BE40	RESERVED_BE46	DRAM1_DQ_3838	SP47
BD40	DRAM1_CKE_22	DRAM1_DQ_3939	SP45
BF40	RESERVED_BF48	DRAM1_DQ_4040	SP45
		DRAM1_DQ_4141	SP45
AP41	DRAM1_ODT_0	DRAM1_DQ_4242	BM41
AT42	DRAM1_ODT_2	DRAM1_DQ_4343	SP48
		DRAM1_DQ_4444	SP40
		DRAM1_DQ_4545	SK42
		DRAM1_DQ_4646	SK40
		DRAM1_DQ_4747	BH40
AV50	DRAM1_CKP_0	DRAM1_DQ_4848	AV45
AV48	DRAM1_CKN_0	DRAM1_DQ_4949	AV47
		DRAM1_DQ_5050	BF48
		DRAM1_DQ_5151	BF50
		DRAM1_DQ_5252	BM45
AT50	DRAM1_CKP_2	DRAM1_DQ_5353	BM44
AT48	DRAM1_CKN_2	DRAM1_DQ_5454	SK45
		DRAM1_DQ_5555	AV52
		DRAM1_DQ_5656	AL51
		DRAM1_DQ_5757	BG53
		DRAM1_DQ_5858	BG51
AT41	DRAM1_DRAMPSP	DRAM1_DQ_5959	AL53
		DRAM1_DQ_6060	SK51
		DRAM1_DQ_6161	BF52
		DRAM1_DQ_6262	BF51
		DRAM1_DQ_6363	BF40
		DRAM1_DQSP_00	BD40
		DRAM1_DQSN_00	BG35
		DRAM1_DQSP_11	BH34
		DRAM1_DQSN_11	BA38
		DRAM1_DQSP_22	AT38
		DRAM1_DQSN_22	BH44
		DRAM1_DQSP_33	BG43
		DRAM1_DQSN_33	BH53
		DRAM1_DQSP_44	AV52
		DRAM1_DQSN_44	AP42
		DRAM1_DQSP_55	AP44
		DRAM1_DQSN_55	SK47
		DRAM1_DQSP_66	BH48
		DRAM1_DQSN_66	BH52
		DRAM1_DQSP_77	BH51
		DRAM1_DQSN_77	

2 OF 13

VLV_M_D/BGA
REV = 1.15

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 2/9 (DDR8)	1A
Date:	Thursday, July 10, 2014	Sheet 3 of 44

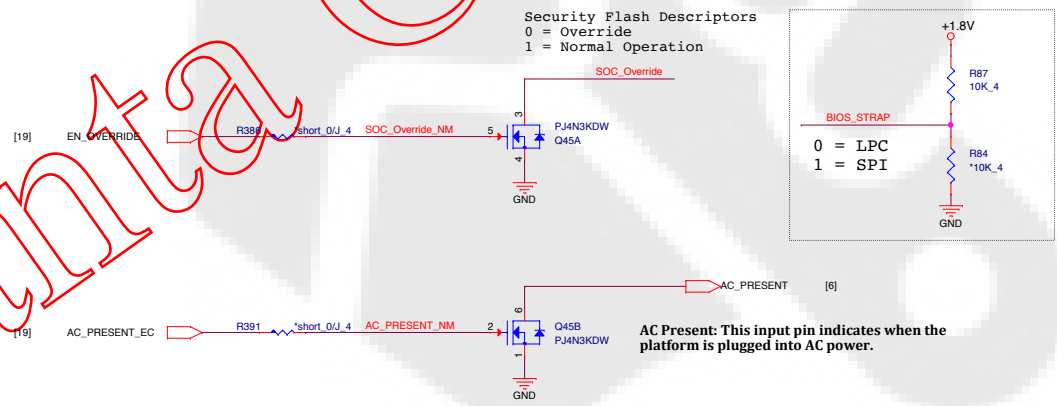
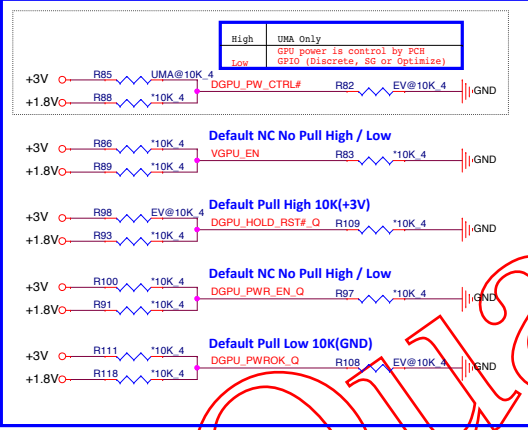


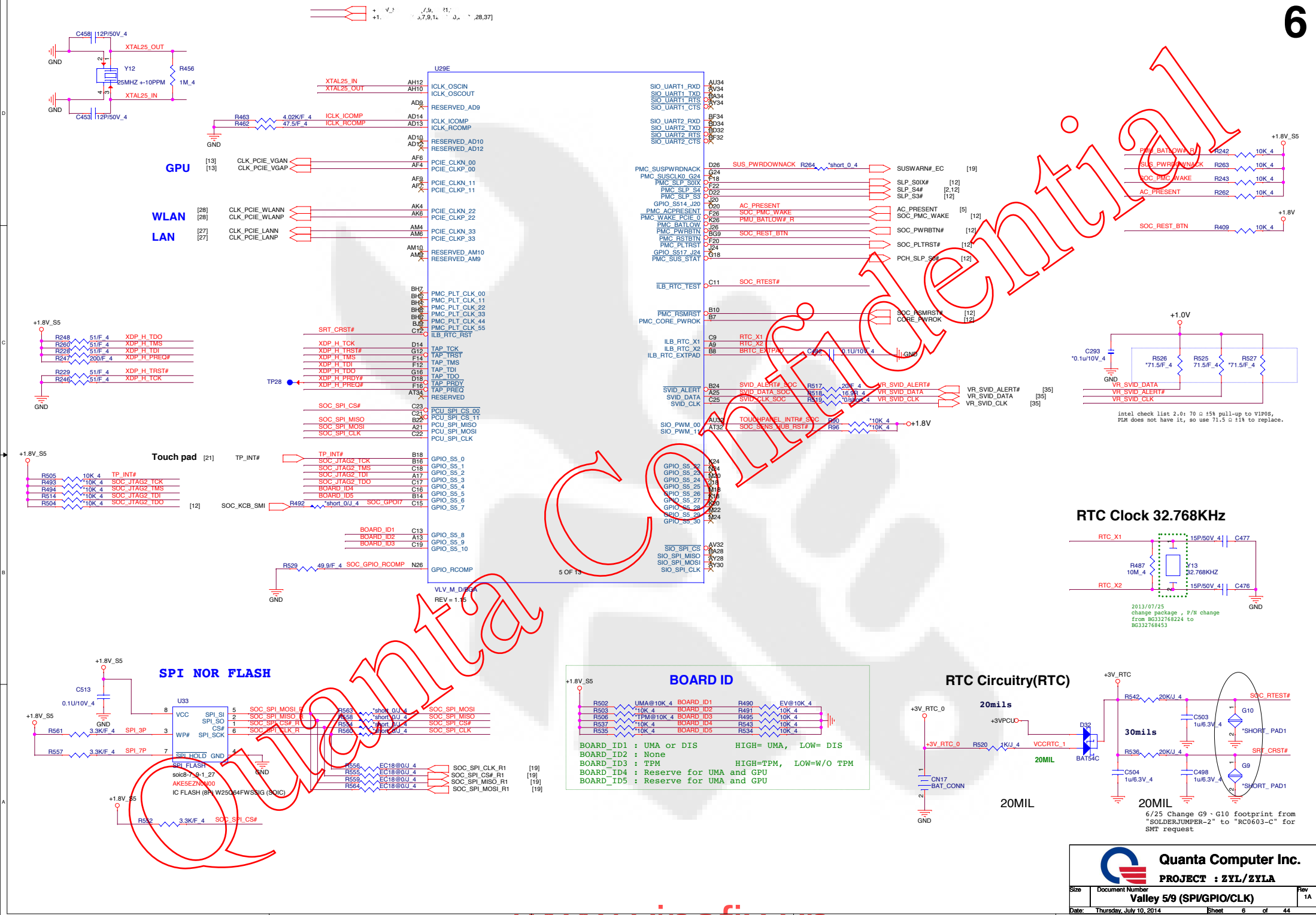
Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 3/9 (Display)	1A

Date: Thursday, July 10, 2014 Sheet 4 of 44





+1.8V_S5 [6,9,12,21,37]
+1.8V [4,5,6,9,12,19,20,21,27,28,37]
+3V [4,5,9,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]

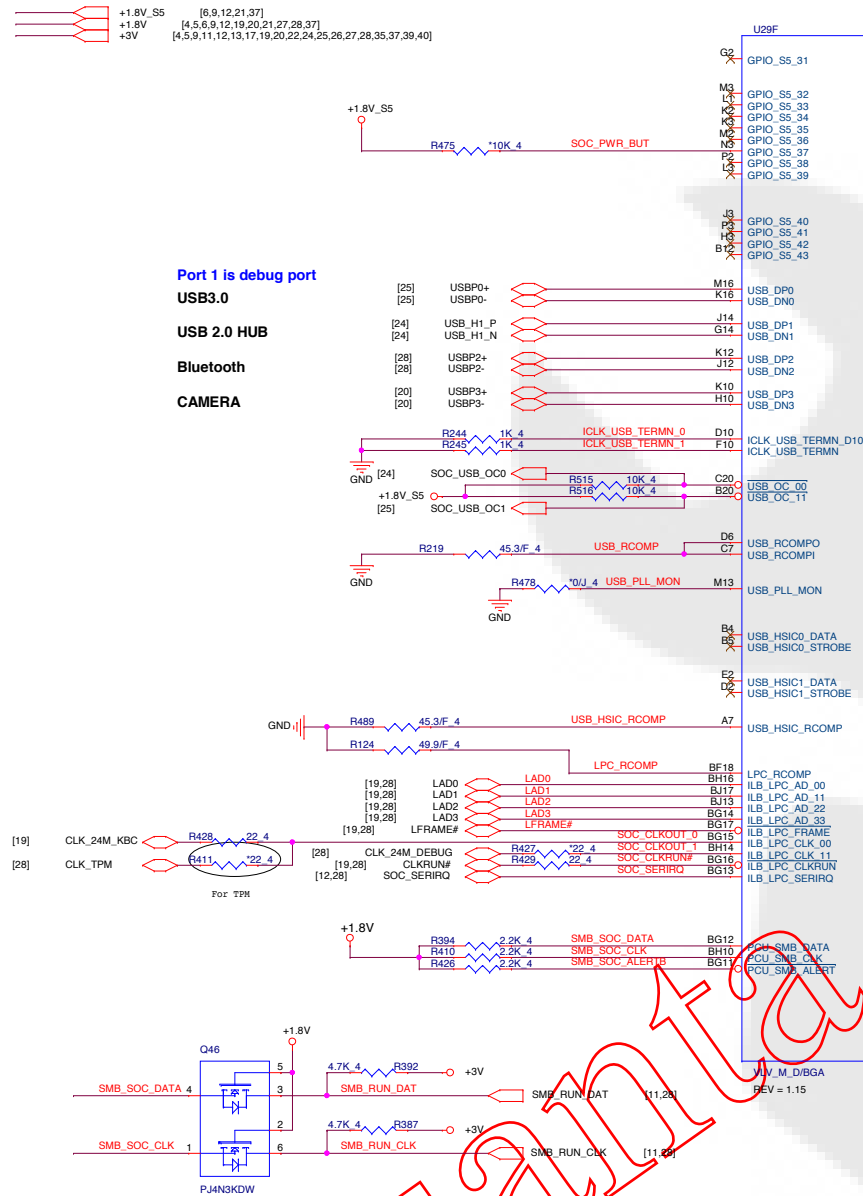
Port 1 is debug port

USB3.0

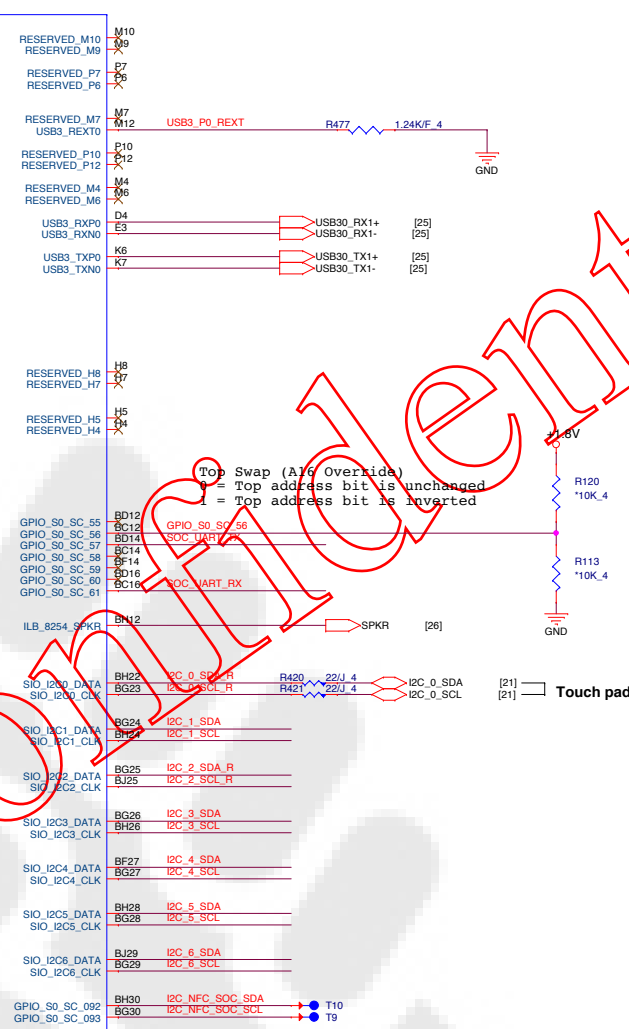
USB 2.0 HUB

Bluetooth

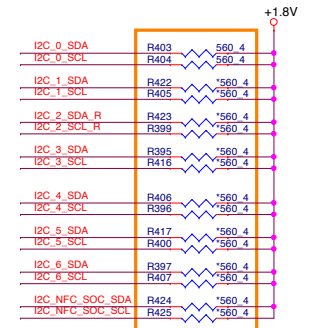
CAMERA



6 OF 13



Un-Stuff for Test Only

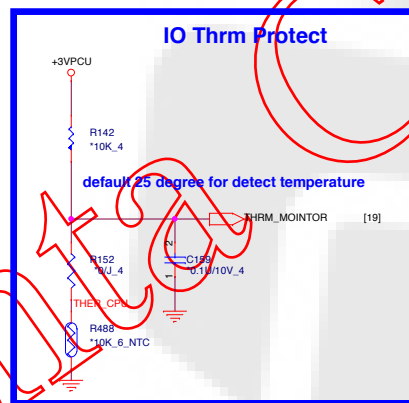
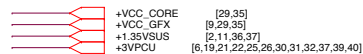


I2C pull up:
Standard/ Fast Mode --> 560 ohm
High speed mode --> CLK- 560 ohm;
DATA- 910 ohm

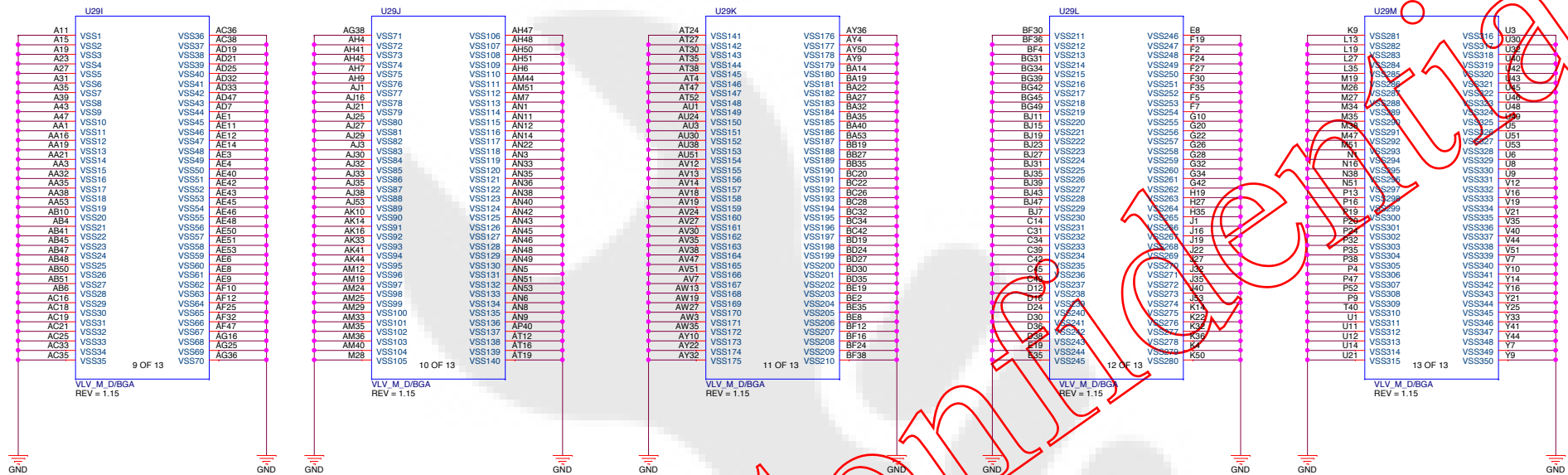


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PROJECT : ZYL/ZYLA

Size Document Number Valley 6/9 (USB/LPC/I2C) Rev 1A
Date: Thursday, July 10, 2014 Sheet 7 of 44



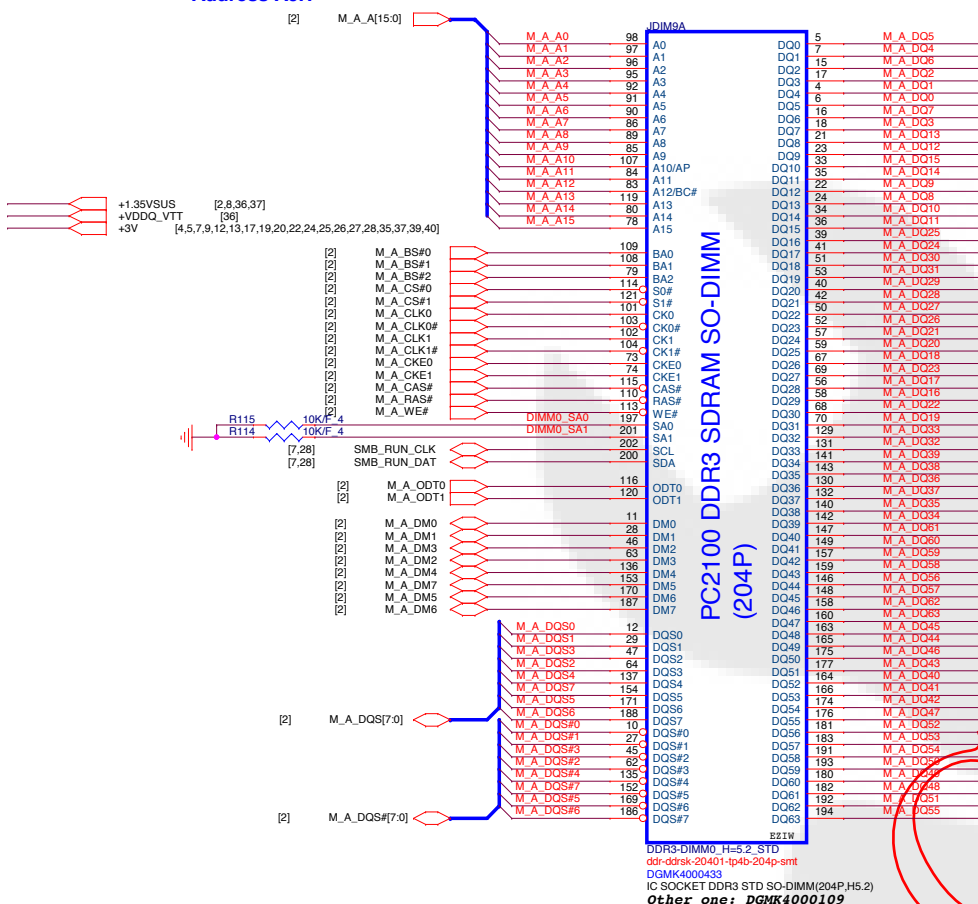




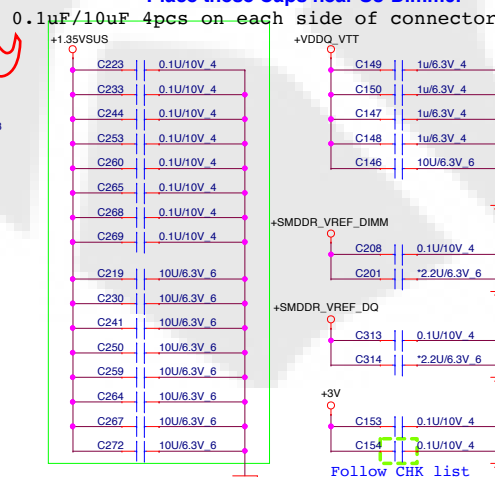
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
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Date: Thursday, July 10, 2014		
Sheet 10 of 44		

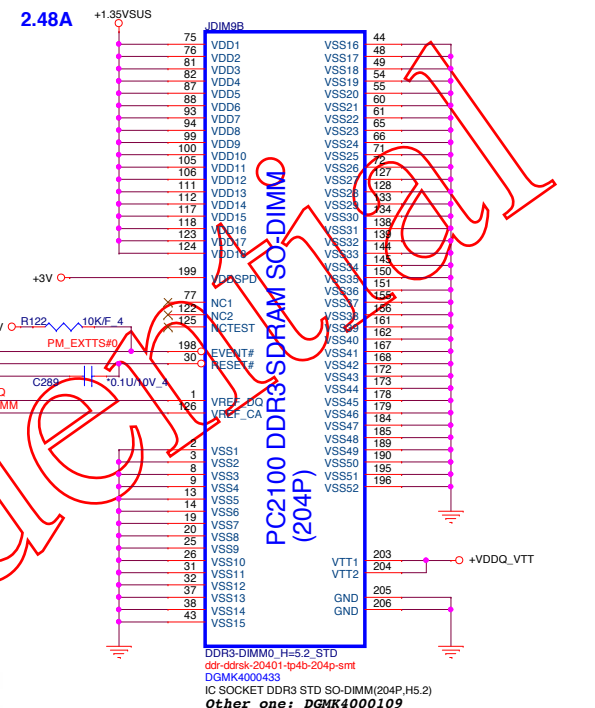
Address A0H

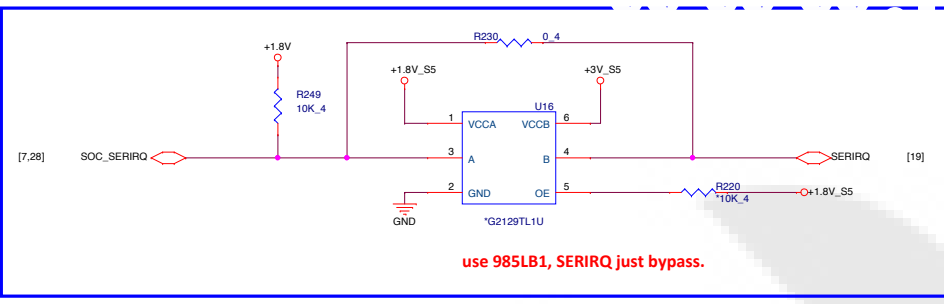


Place these Caps near So-Dimm0.

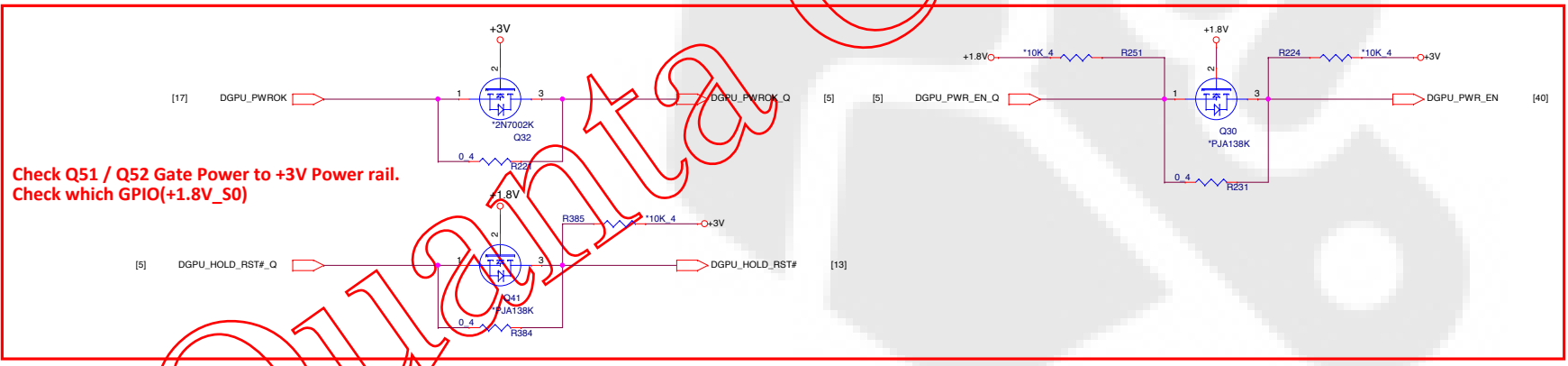
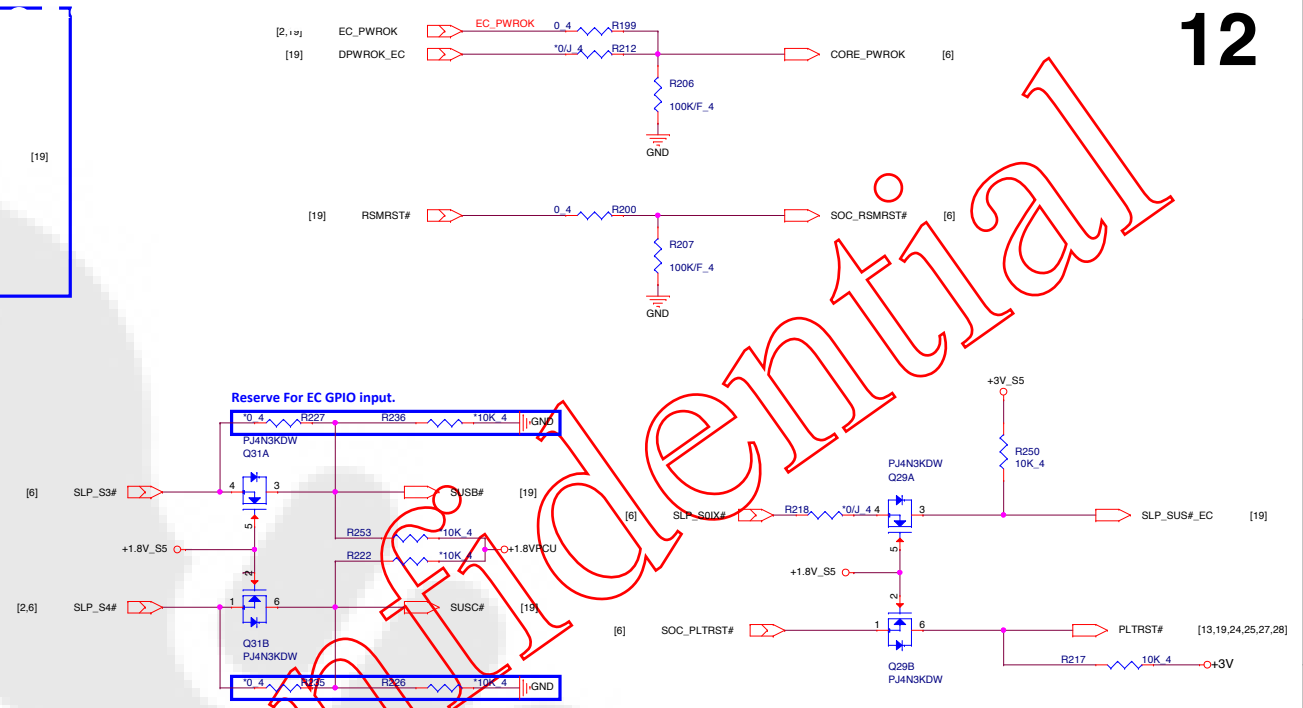
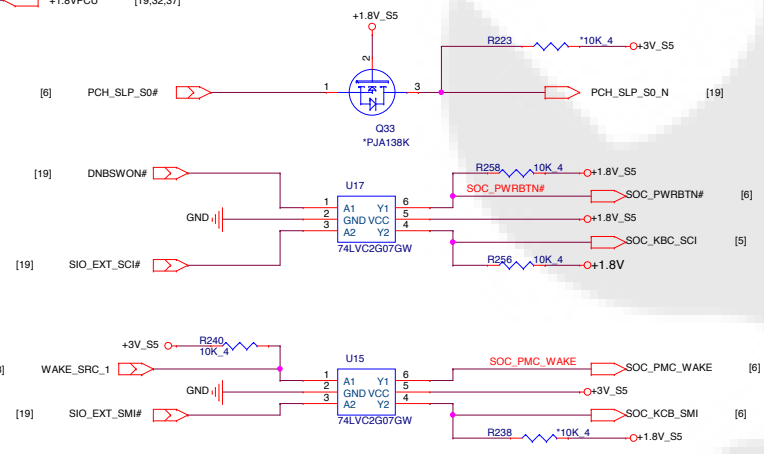


2.48A





- +1.8V [4,5,6,7,9,19,20,21,27,28,37]
- +3V_S5 [2,9,19,21,24,27,28,34,35,37,39,40]
- +3V [4,5,7,9,11,13,17,19,20,22,24,25,26,27,28,35,37,39,40]
- +1.8V_S5 [6,7,9,21,37]
- +1.8VPCU [19,32,37]



Check Q51 / Q52 Gate Power to +3V Power rail.
Check which GPIO(+1.8V_S0)

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Level Shifter	1A
Date: Thursday, July 10, 2014	Sheet 12 of 44	

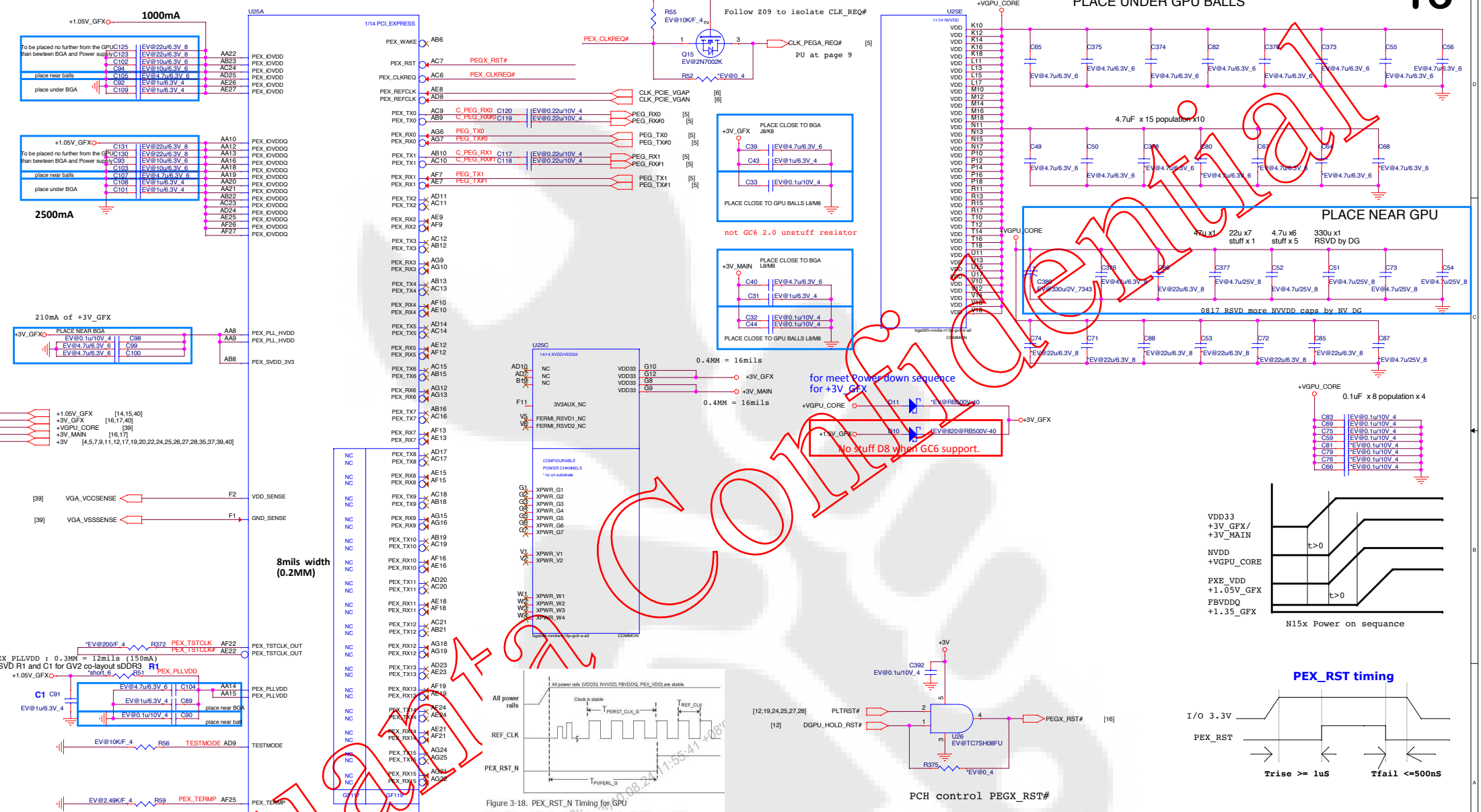


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PWRUP_G}	$T_{PWRUP_G} \geq 100$	
$T_{PWRUP_CLK_G}$	$T_{PWRUP_CLK_G} \geq 1T_{REF_CLK}$	

PEX_RST_N timing diagram showing Trise >= 1uS and Tfall <= 500ns.

PEX_RST_N timing diagram showing Trise >= 1uS and Tfall <= 500ns.

N15V-GM no support GC6 function.

For Fermi

FBA_CMD2 R36 EV@10K/F 4
FBA_CMD3 R32 EV@10K/F 4
FBA_CMD5 R41 EV@10K/F 4
FBA_CMD18 R368 EV@10K/F 4
FBA_CMD19 R53 EV@10K/F 4

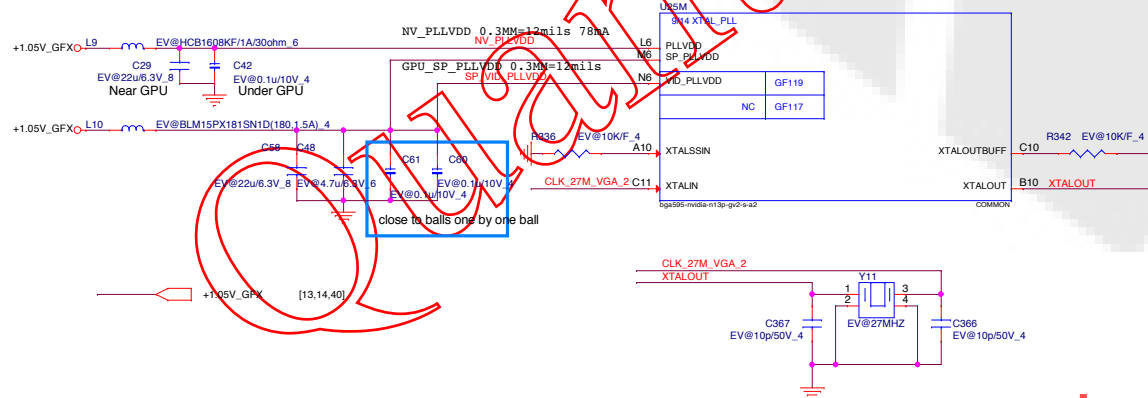
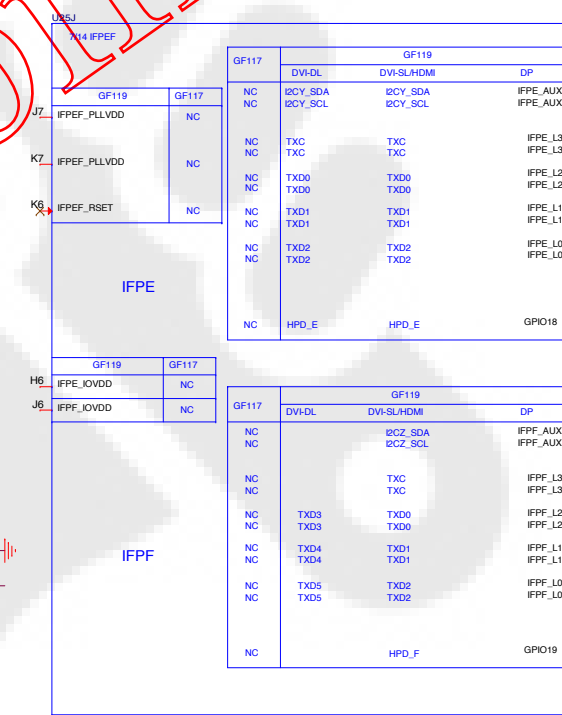
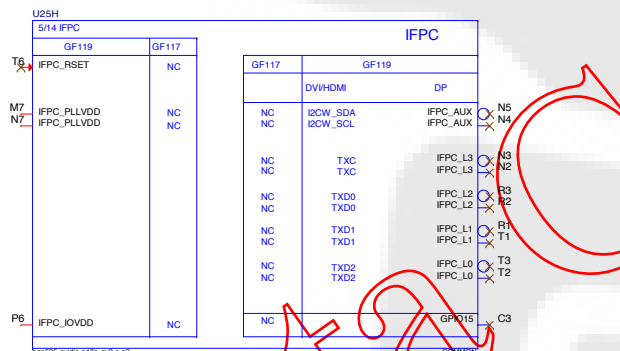
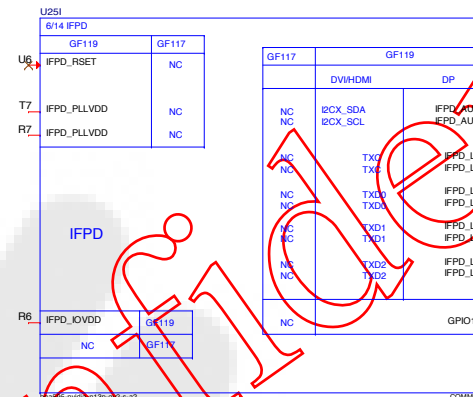
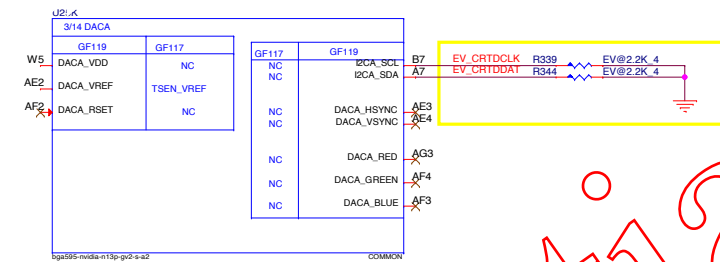
PLACE CLOSE TO GPU BALLS
C38 EV@0.1u/10V 4
C35 EV@0.1u/10V 4
C57 EV@0.1u/10V 4
C36 EV@0.1u/10V 4

C30 EV@1u/6.3V 4
C27 EV@1u/6.3V 4
C28 EV@1u/6.3V 4
C77 EV@1u/6.3V 4

C45 EV@4.7u/6.3V 6
C133 EV@4.7u/6.3V 6
C97 EV@4.7u/6.3V 6
C14 EV@4.7u/6.3V 6

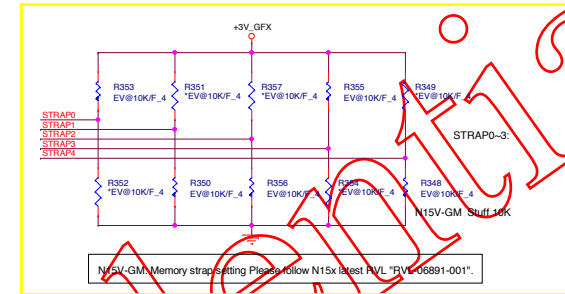
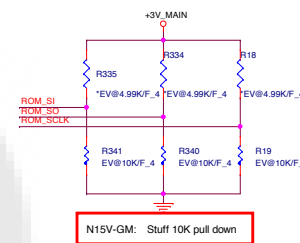
C46 EV@10u/6.3V 3V 6
C84 EV@10u/6.3V 3V 6
C21 EV@10u/6.3V 3V 6
C11 EV@10u/6.3V 3V 6

PLACE CLOSE TO BGA
EV@330u/2V 7343 C10
EV@330u/2V 7343 C350



Binary mode setting.
For N15V-GM-B-A2:
Device ID=0x1140
R3= N.C.
1.ROM_SCLK=10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory
5.Strap4 =10k pull down

Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3	Strap4
HYNIX	HT5C4G63A0R-11C	0	0	1	0	
MICRON	MT41J256M16HA-093G:E	1	0	1	1	
SAMSUNG	K4W4G164D-BC1A	1	0	0	1	Default

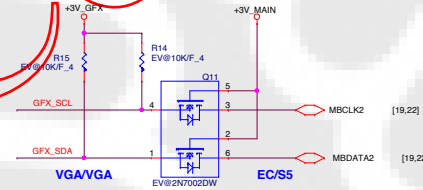


N15V-GM VRAM Configuration Table:

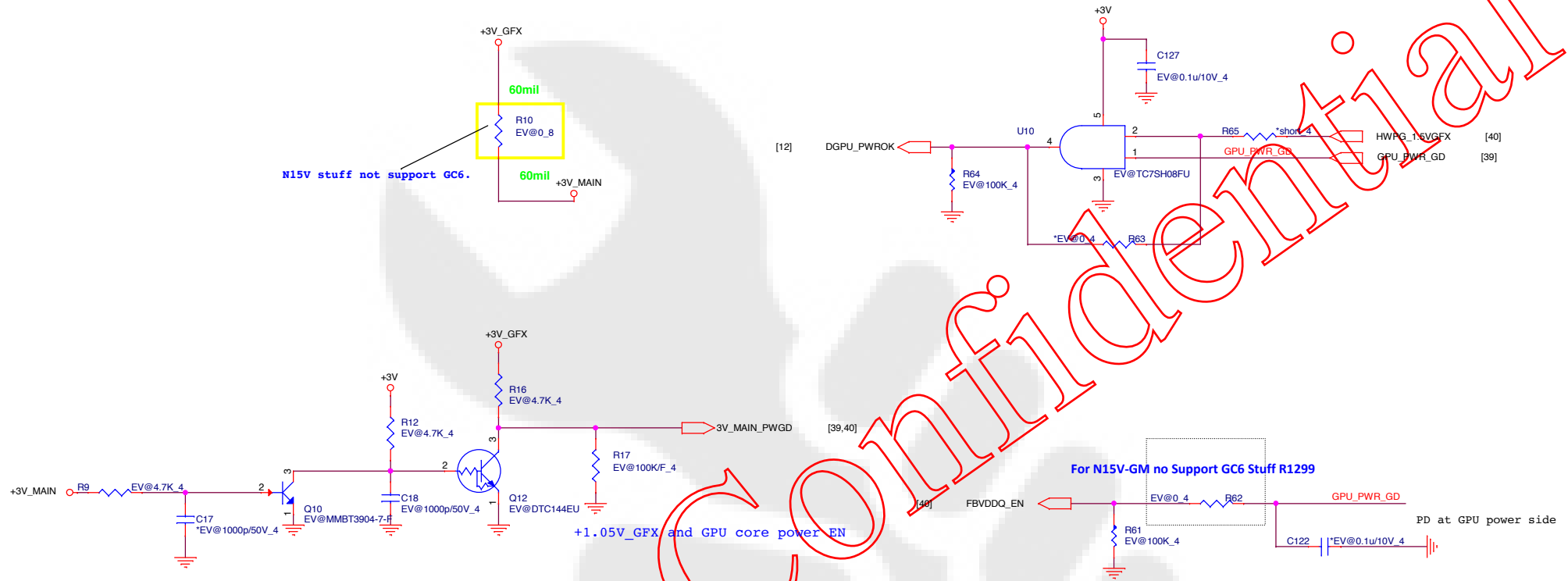
4Gb	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
	0100 (0x0)	DDR3 256MBx16, 1000MHz	HYNIX	H5TC4G63A0R-11C	
	1101 (0x0)	DDR3 256MBx16, 1000MHz	MICRON	MT41J256M16HA-093G:E	
	1001 (0x0)	DDR3 256MBx16, 1000MHz	SAMSUNG	K4W4G164D-BC1A	

STRAP3 Optimus -> 4.99k PD
Resistor P/N 10K -> CS31002FB26

SMBus(VGA)

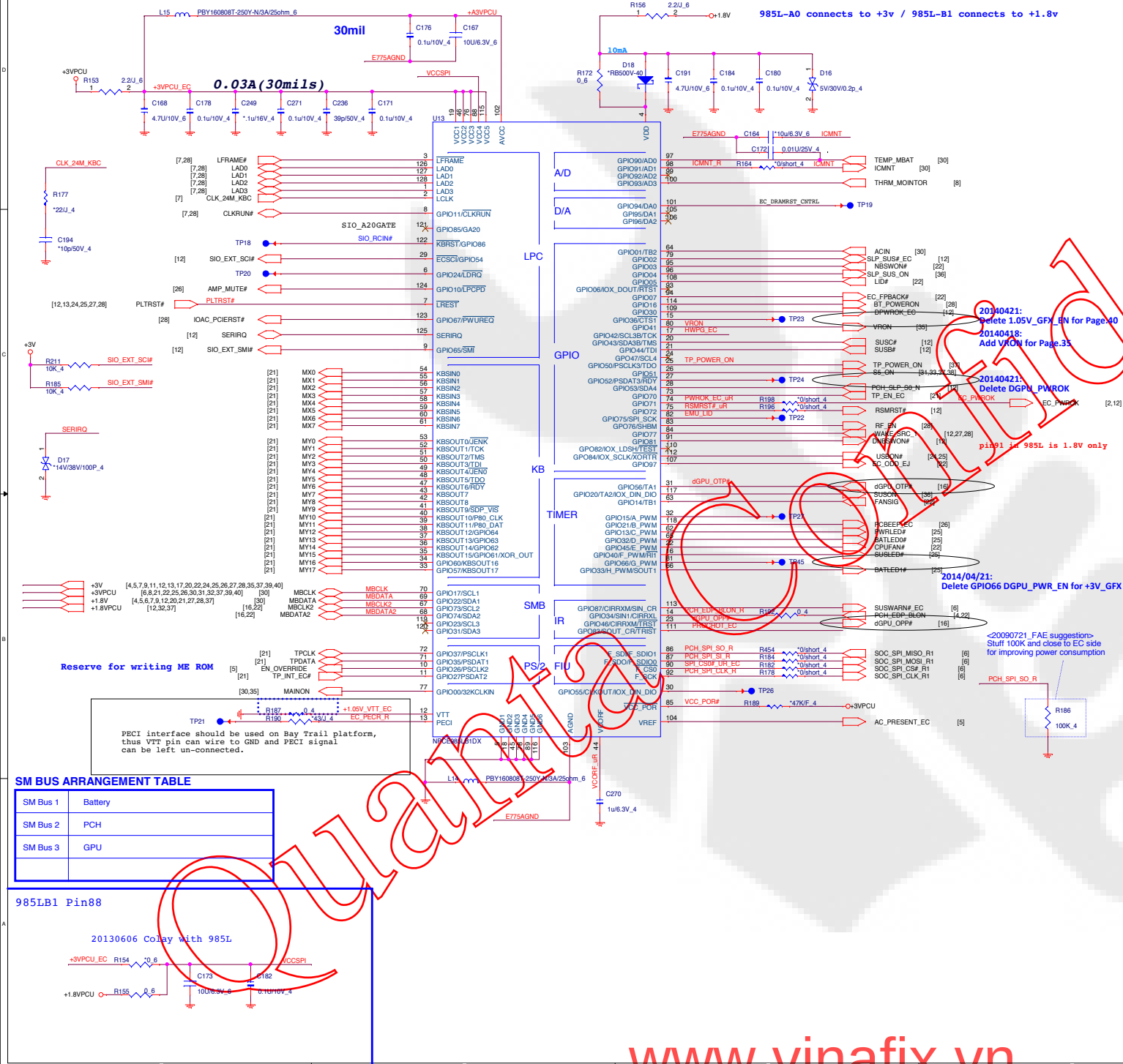


Vendor P/N	820M	QCI P/N
N15V-GM-B-A2	GeForce 820M	0x1140
		AJON15V0703



CHANNEL A: 2048MiB DDR3X16

1.8V p/n: AJ009050F02
Discription: IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

[illegible]

20140421:
Change to HWPG_1.5V

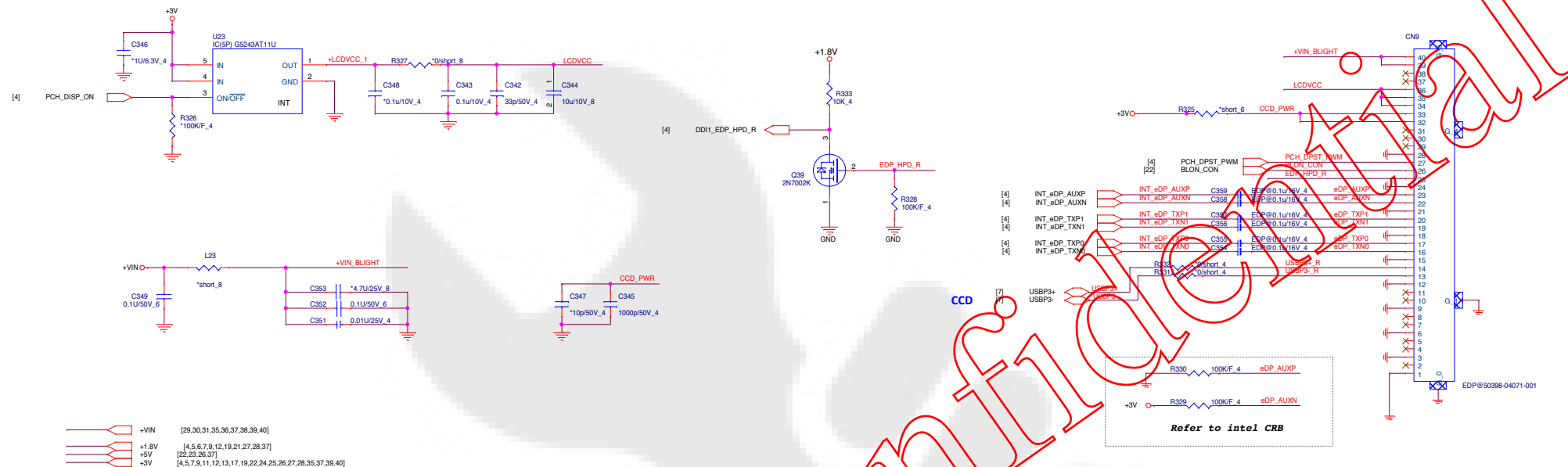
<20130722>-Change power from +3V to +3V_SS for power sequence issue

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

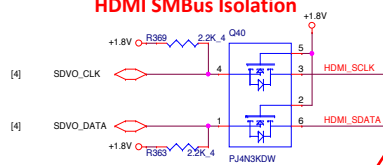
985LB1 Pin88

20130606 Colay with 985L

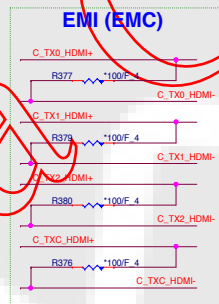


HDMI Conn.

HDMI SMBus Isolation

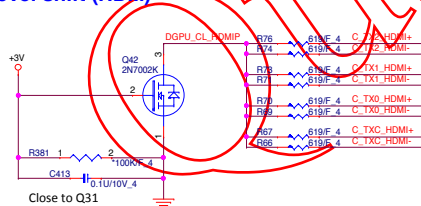


EMI (EMC)

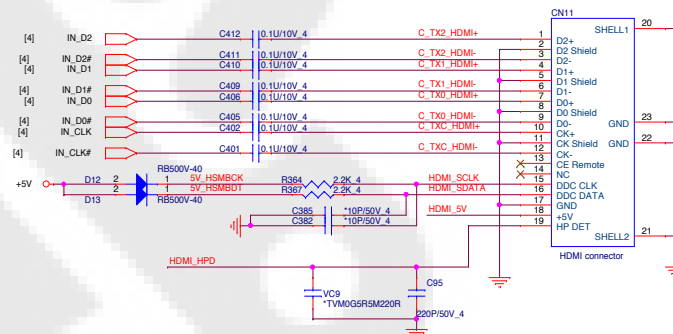
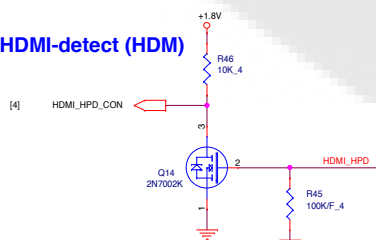


HDMI-Level shift (HDM)

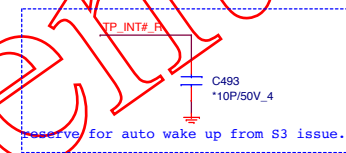
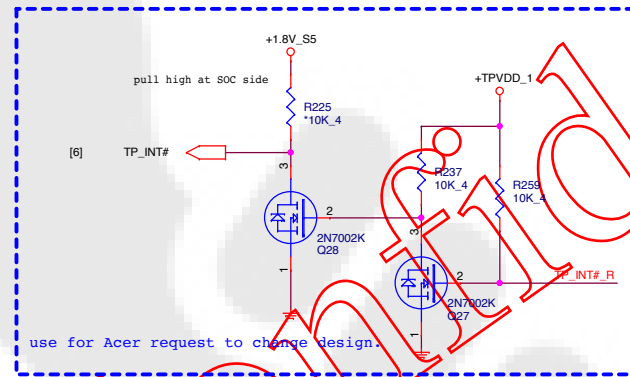
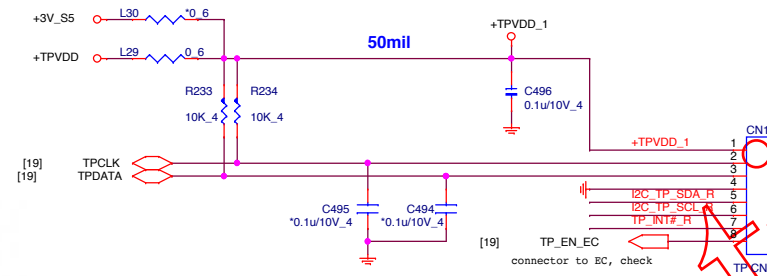
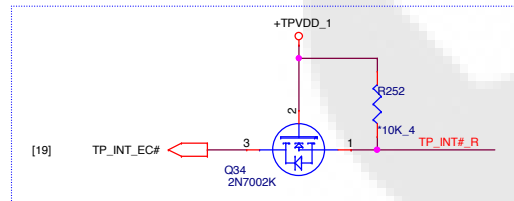
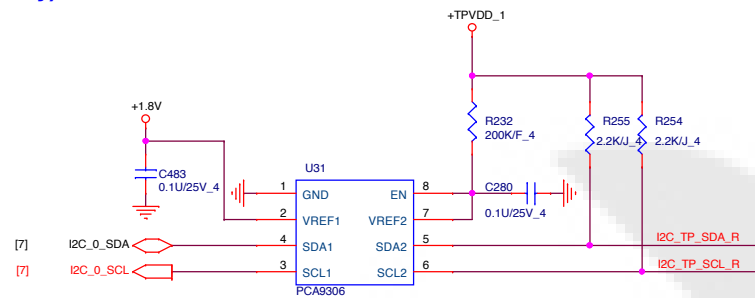
Close to HDMI connector



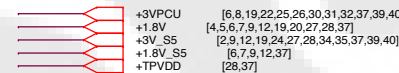
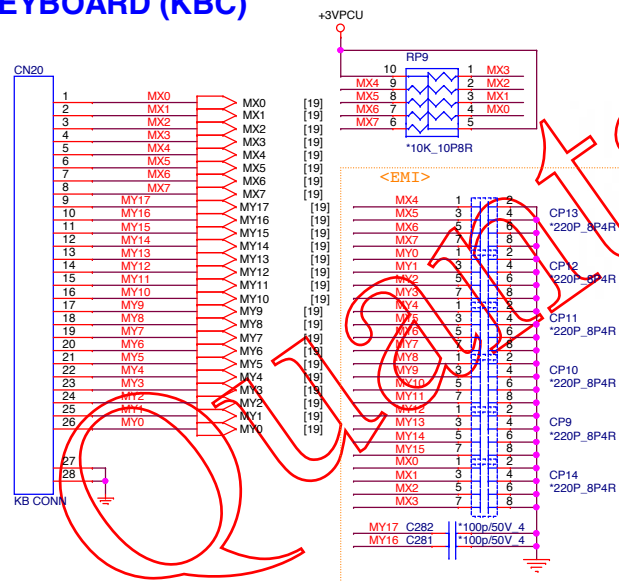
HDMI-detect (HDM)



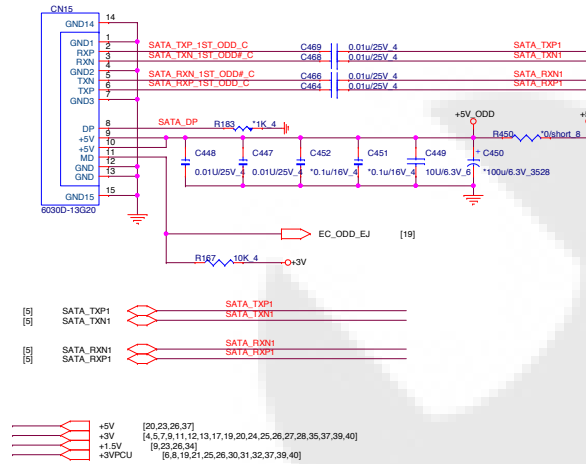
TOUCHPAD BOARD CONN (TPD) I2C/PS2 co-lay



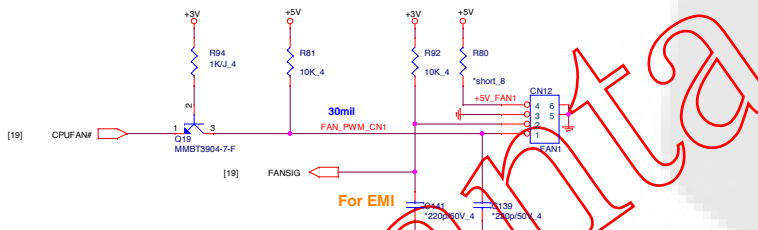
KEYBOARD (KBC)



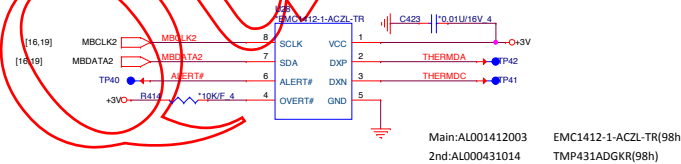
SATA ODD Connector



CPU FAN CTRL(THM)

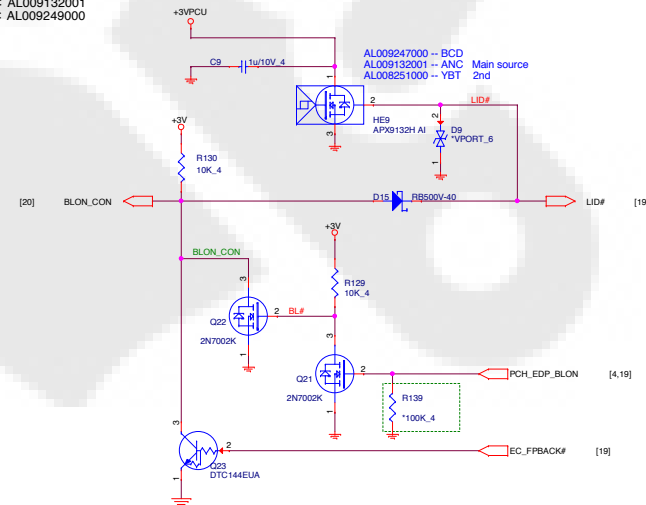


CPU Thermal sensor(THS) / MB Local TEMP

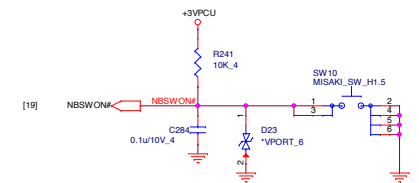


HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



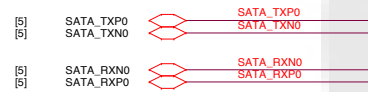
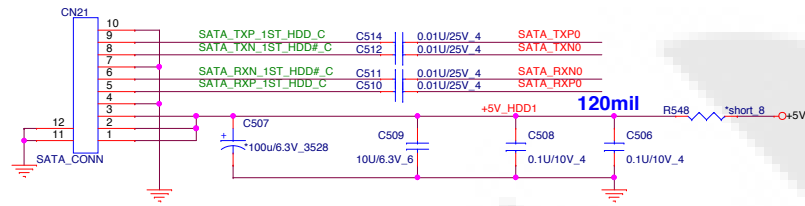
Power Switch. (FSW)



SATA HDD1

23

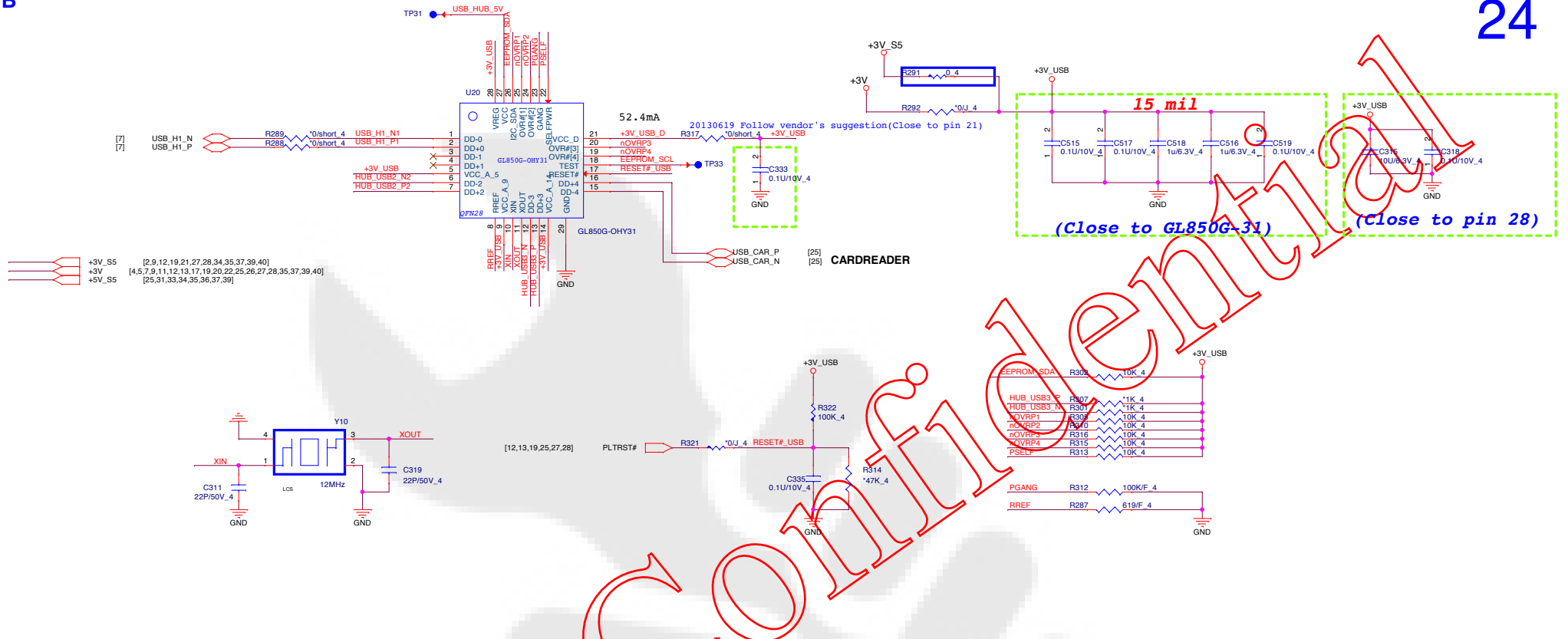
HDD1



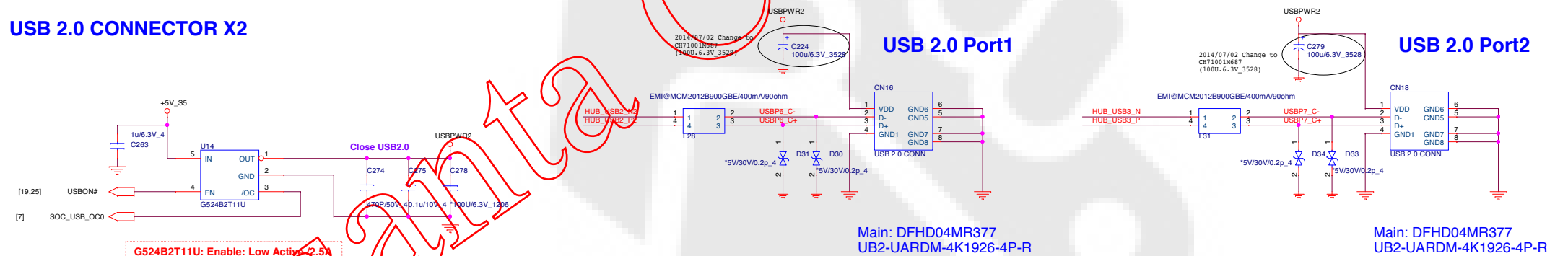
 Quanta Computer Inc.		PROJECT : ZYL/ZYLA	
Size	Document Number	SATA HDD/SATA REDRIVER	
Date: Thursday, July 10, 2014	Sheet 23 of 44	Rev 1A	

USB HUB

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USB 2.0 CONNECTOR X2



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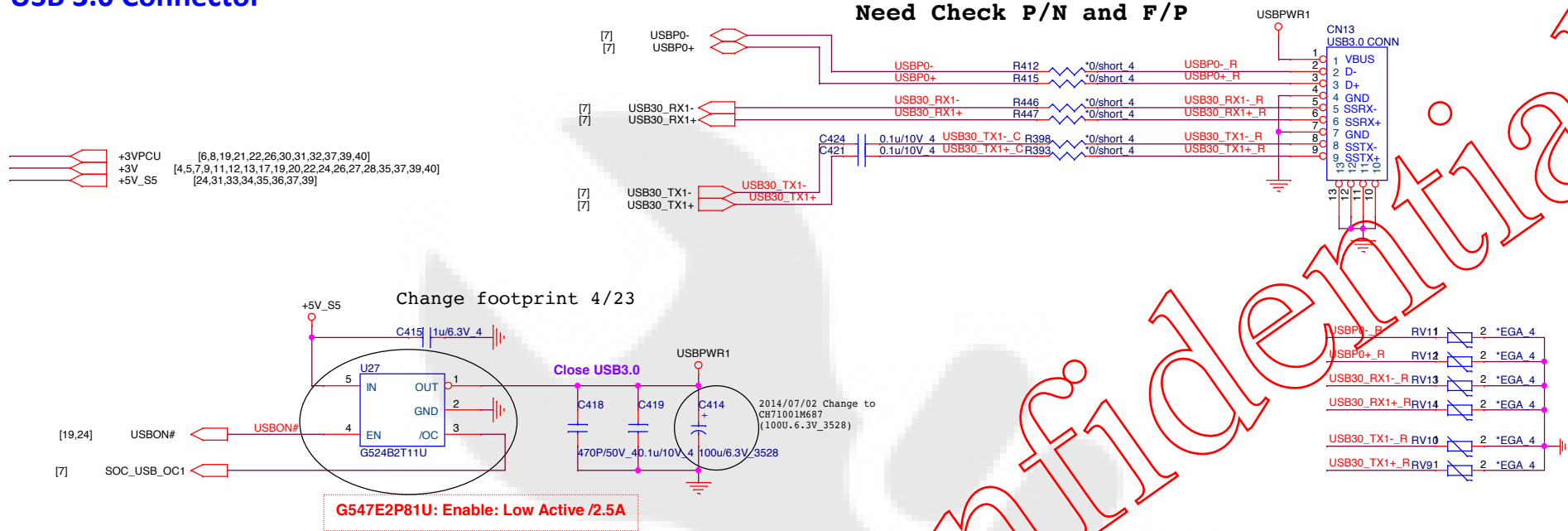
PROJECT : ZYL/ZYLA

USB BOARD CONN

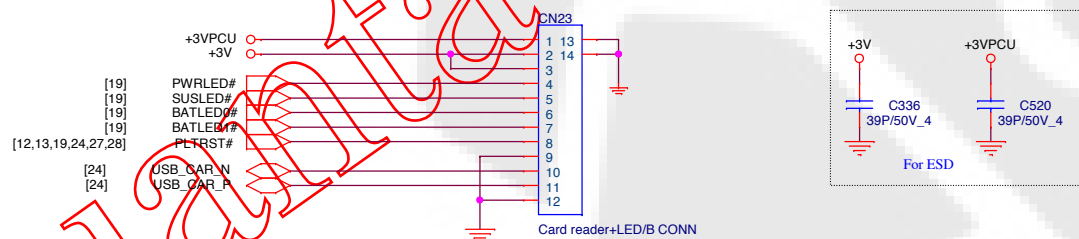
Size: Document Number: Rev 1A

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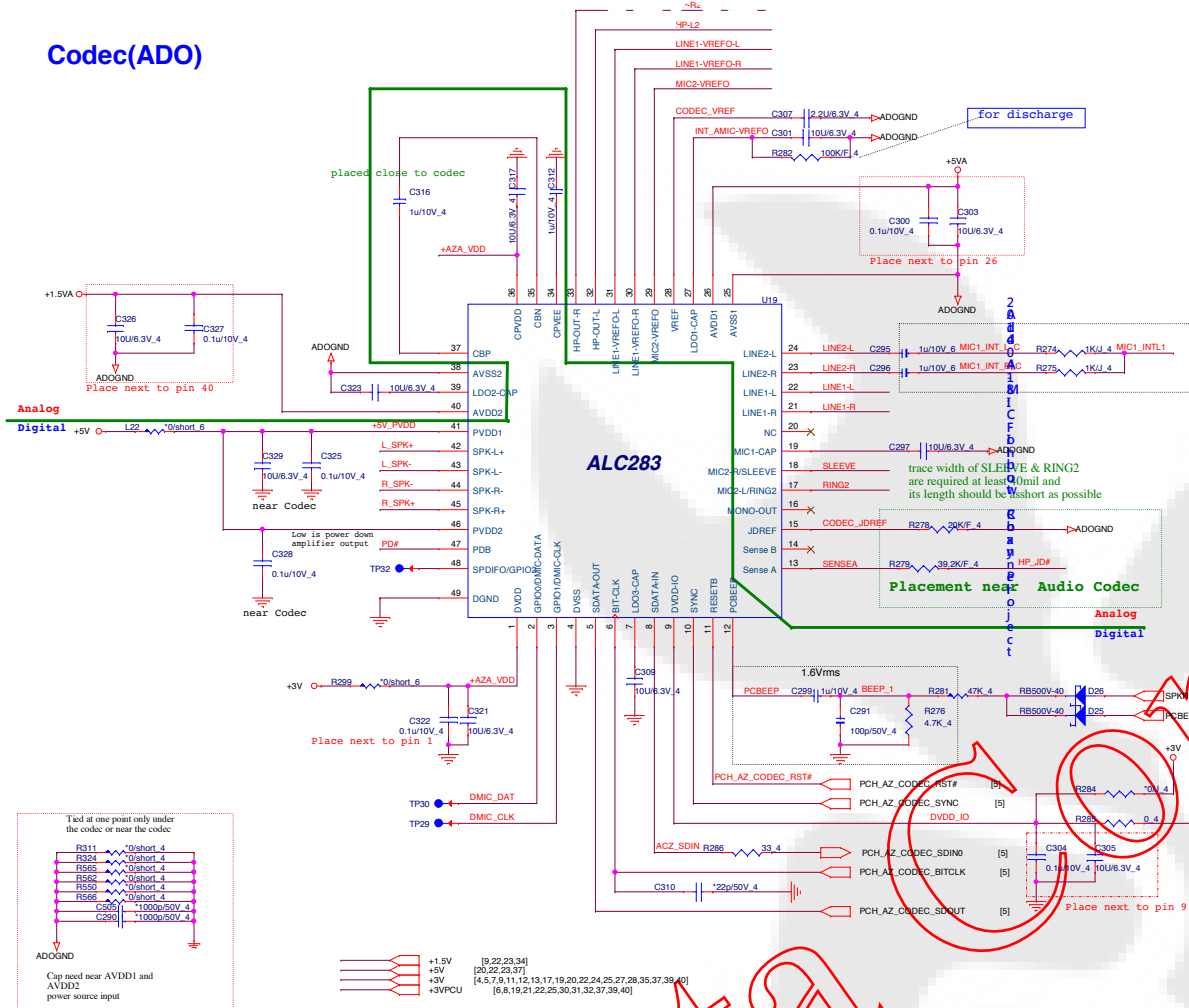
USB 3.0 Connector



Card Reader+ LED/B Connector

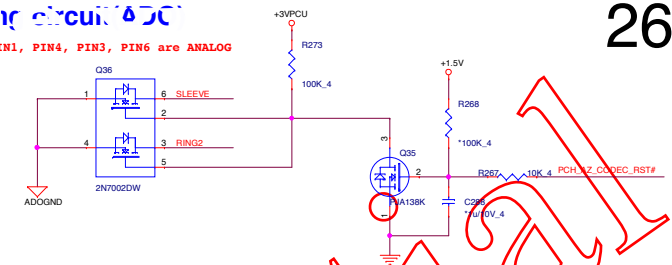


Codec(ADO)

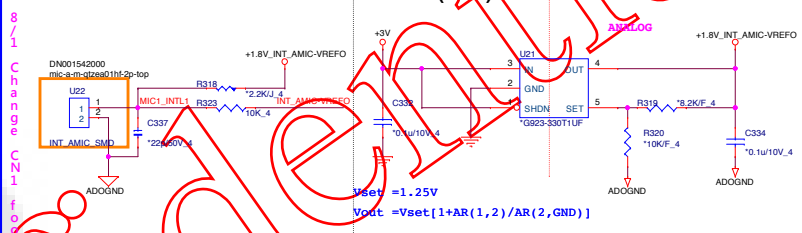


Giải bài tập circuit ĐĐC

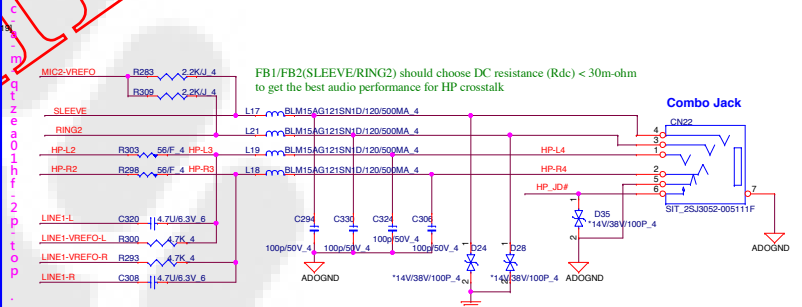
PIN1, PIN4, PIN3, PIN6 are ANALOG



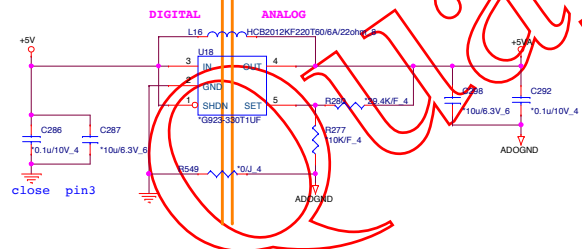
Analog-MIC



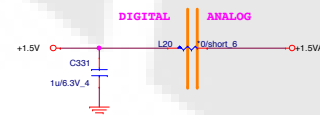
HEADPHONE/MIC/LINE combo (AMP)



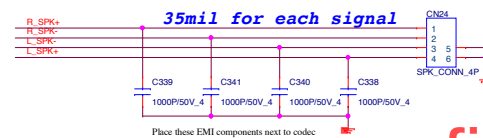
Codec PWR 5V(ADO)



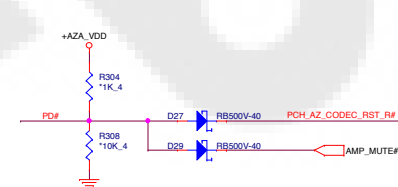
Codec PWR 1.5V(ADO)



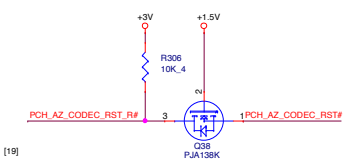
Internal Speaker



Mute(ADO)

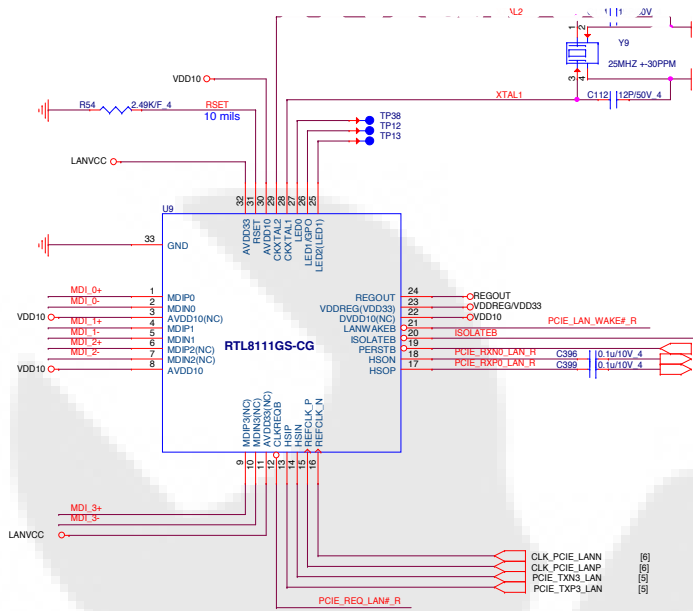
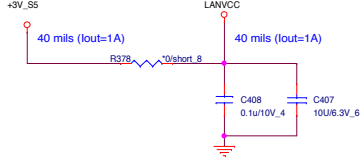


Level shift

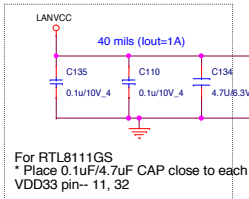
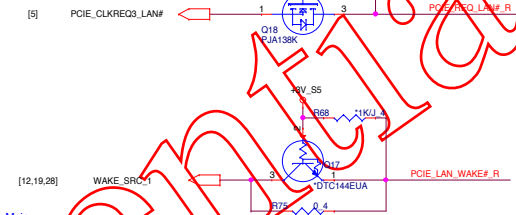


+3V [4,5,7,9,11,12,13,17,19,20,22,24,25,26,28,35,37,39,40]
 +1.8V [4,5,6,7,9,12,19,20,21,28,37]
 +3V_S5 [2,9,12,19,21,24,28,34,35,37,39,40]

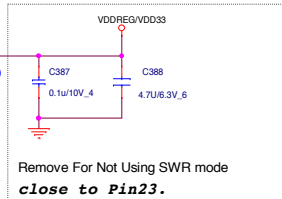
LANVCC



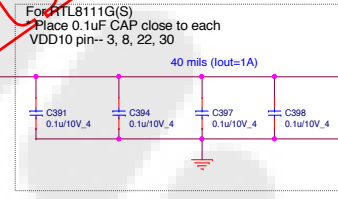
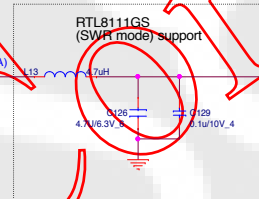
Consider VCC33 may be connected to Main Power or chipset/bios's GPO. In either case, resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1-S5.
 If the ISOLATEB pin can not be well-controlled to voltage level < 0.8V at S1-S5, the pulldown resistor R14 is needed to make sure the LAN chip is well isolated.



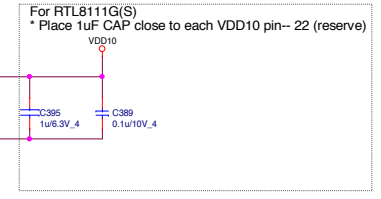
For RTL8111GS
 * Place 0.1uF/4.7uF CAP close to each VDD33 pin-- 11, 32



Remove For Not Using SWR mode
 close to Pin23.

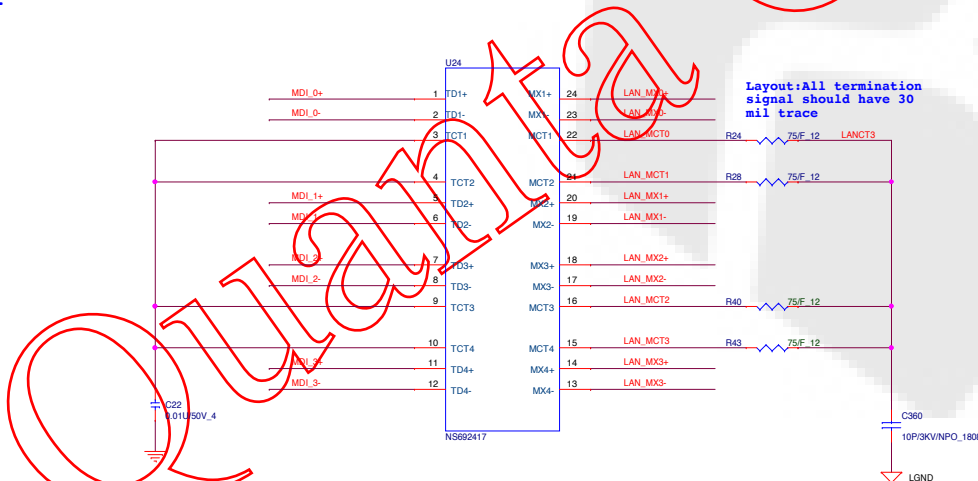


For RTL8111G(S)
 Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30



For RTL8111G(S)
 * Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

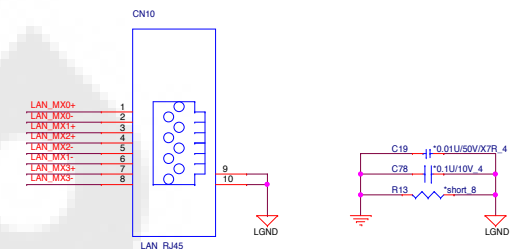
Transformer



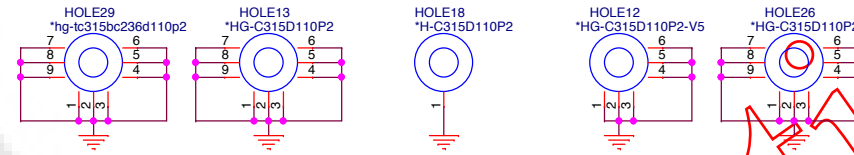
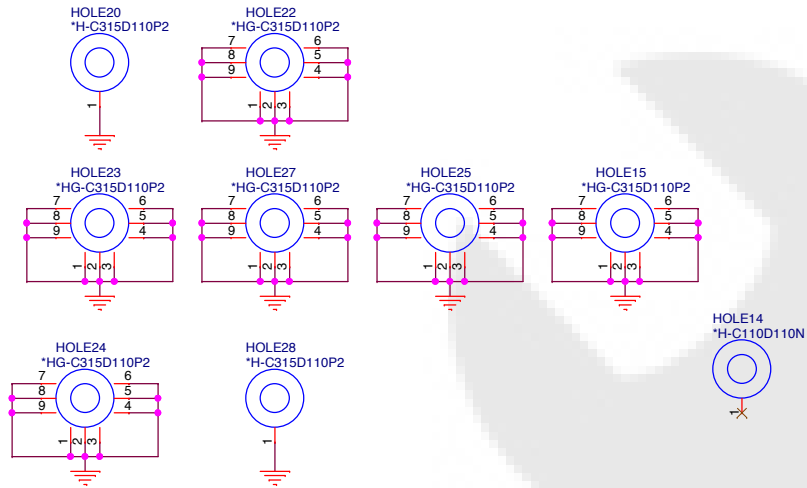
Layout: All termination signal should have 30 mil trace

RJ45 Connector

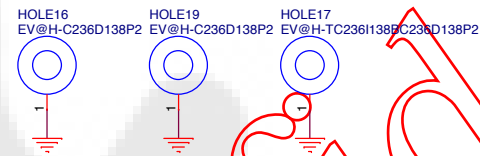
Need Check P/N and F/P







GPU nuts

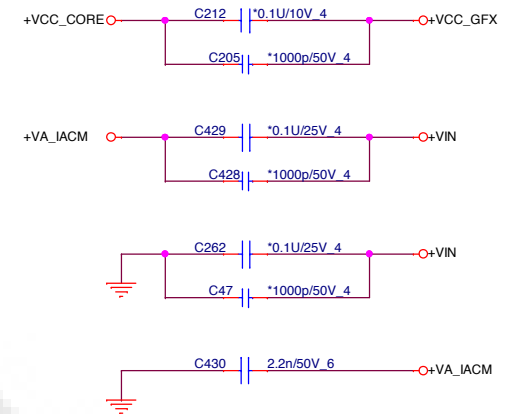
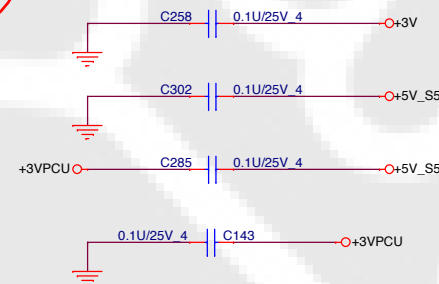
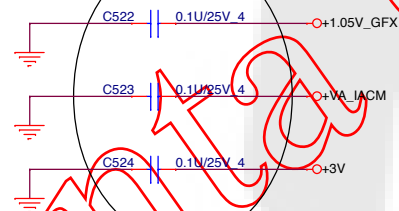


Mini card nuts

CPU nuts



reserve for ESD



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PROJECT : ZYL/ZYLA

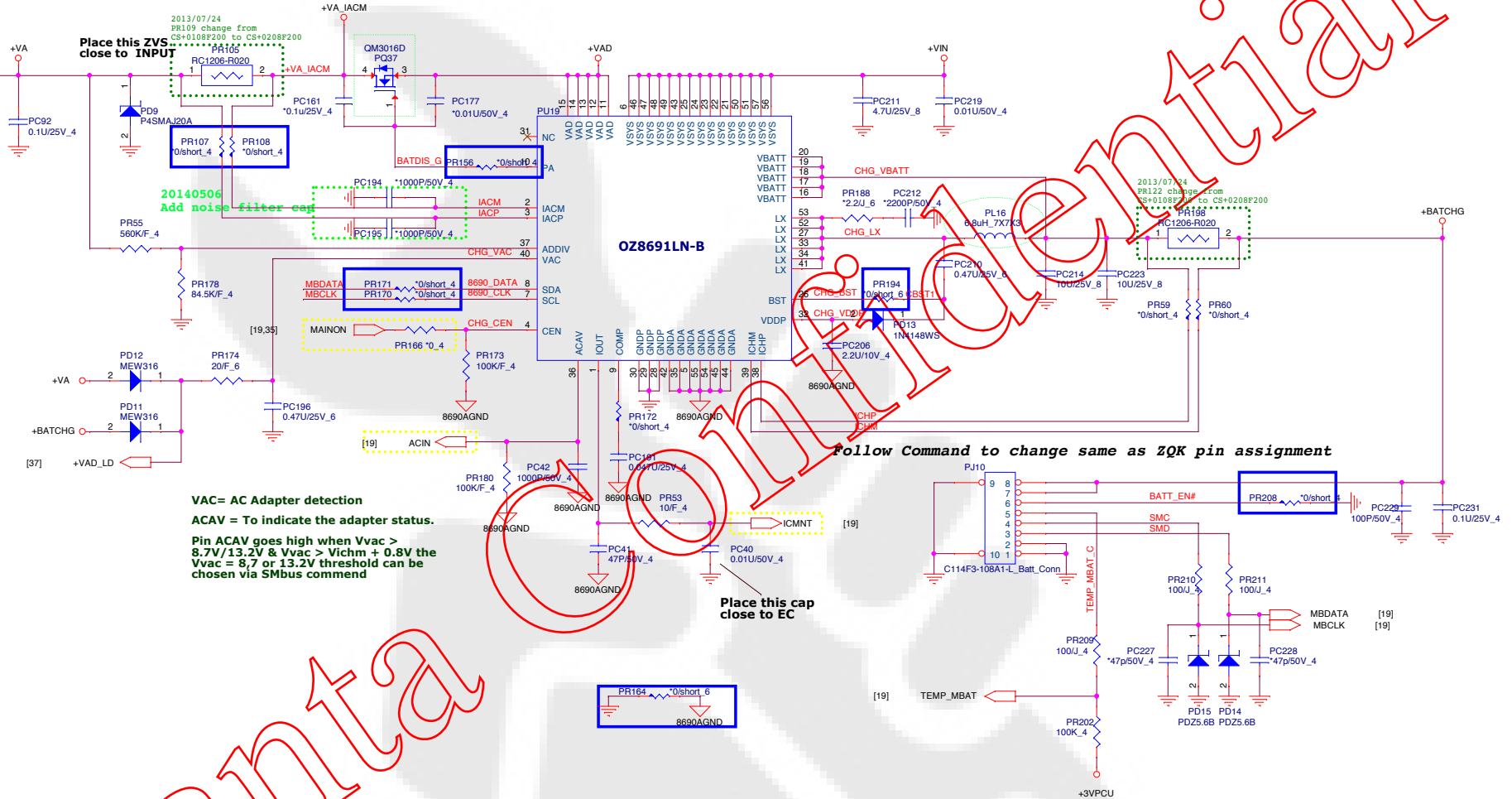
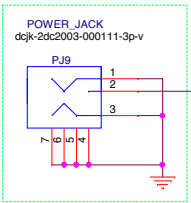
Size	Document Number	Rev
	USB BOARD CONN	1A

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DFPJ06MR013-- 95W
DFPJ06MR007--- 45W

ZE7



Quanta Computer Inc.

PROJECT : ZEJ

Size Document Number
Charger (OZ8690ALN)

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LDO (MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A

Remove JP13

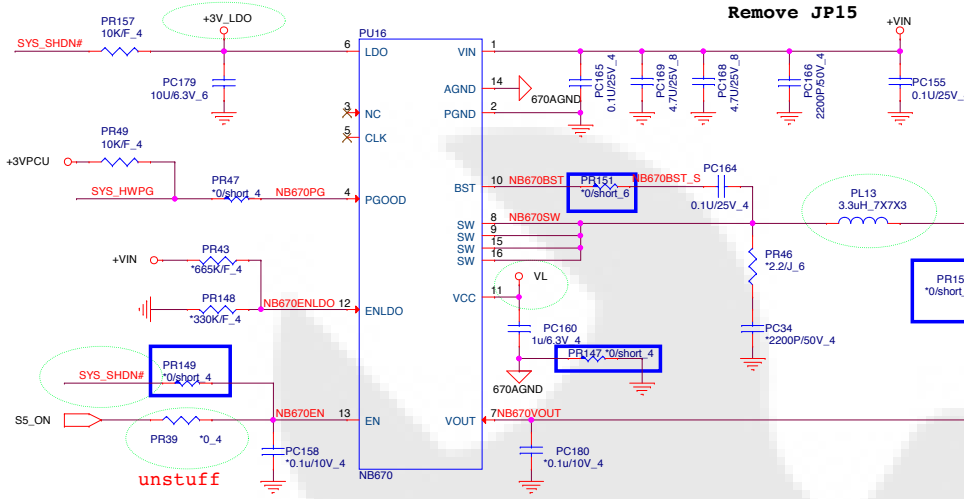
Remove JP15

Remove JP18

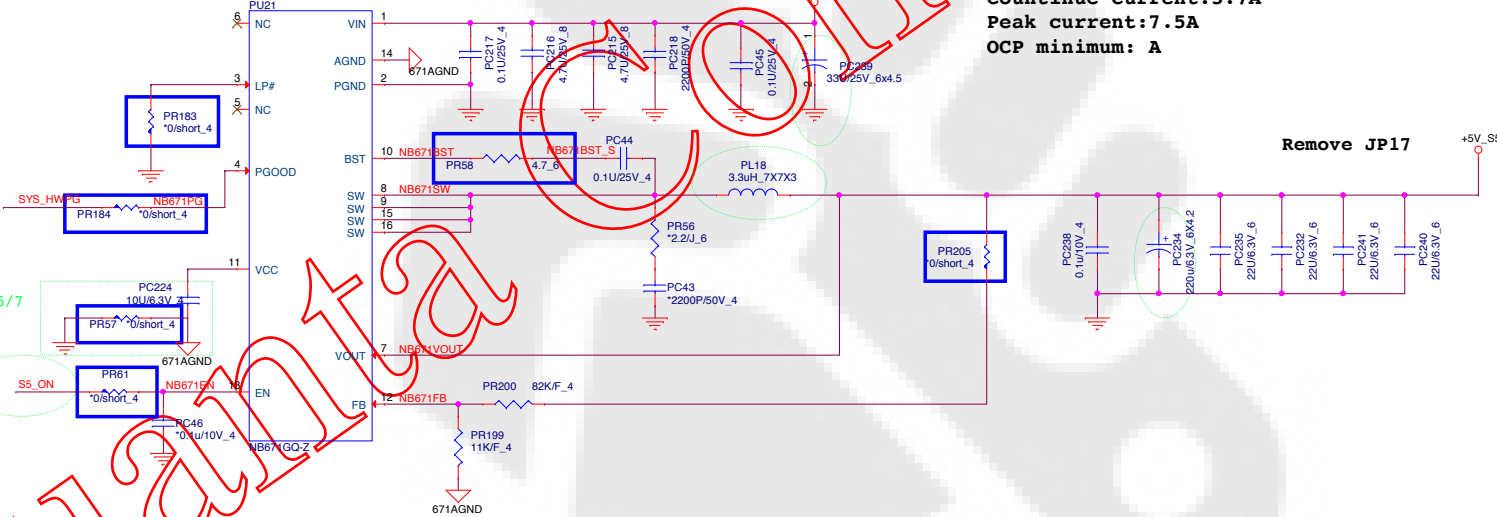
+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A

Remove JP17

Exchange AGND and PGND 5/7



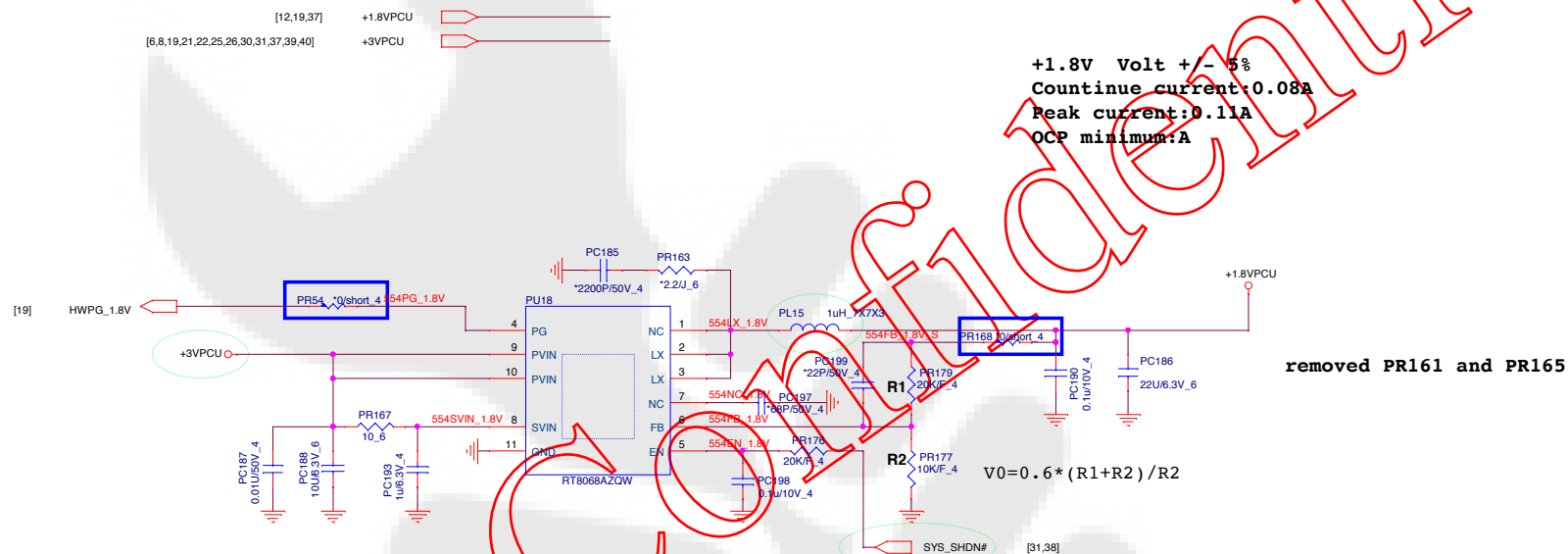
unstuff



Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	3/5VS5 (NB670/NB669)	1A

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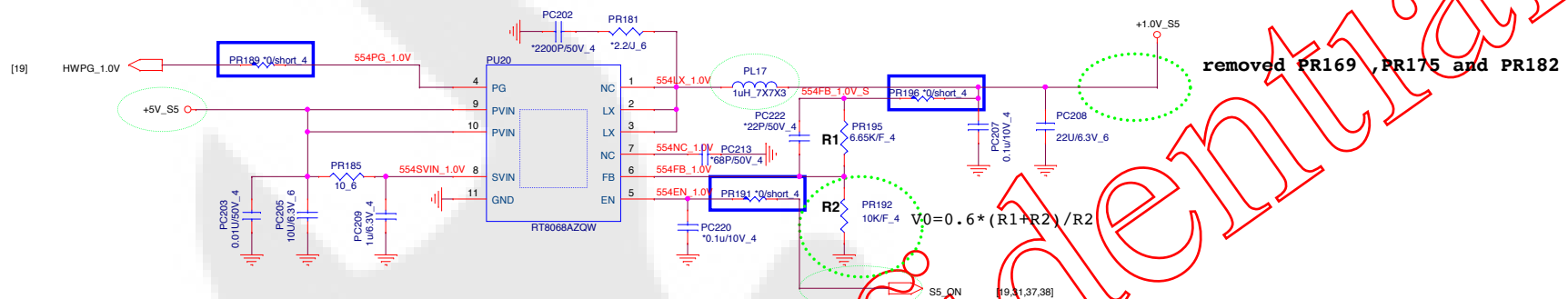


Quanta Computer Inc.

PROJECT : ZHJ

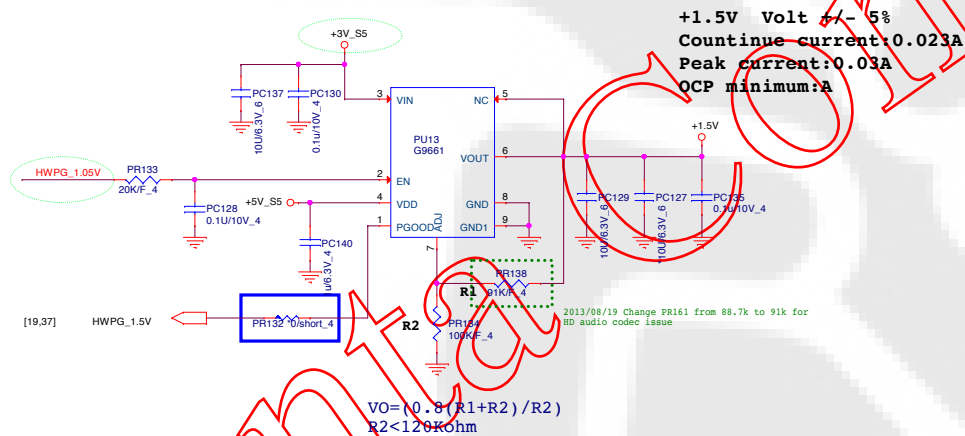
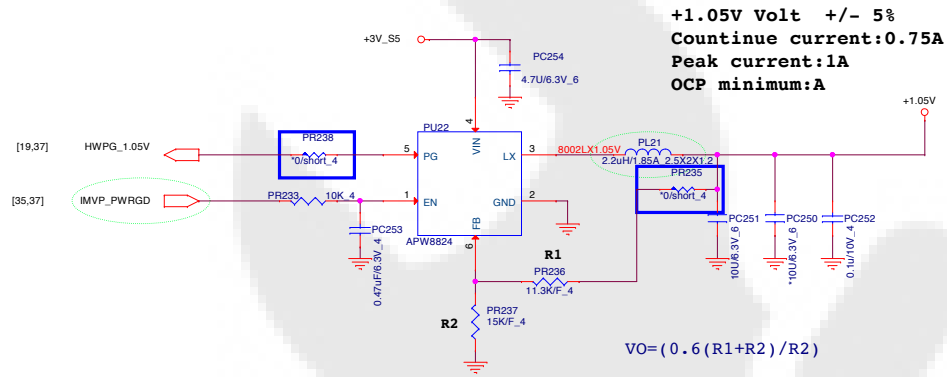
Size	Document Number	Rev
	+1.8VPCU	1A

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20140609:
Change PR192 from 10K to 9.31K Ohm

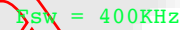
[2,9,12,19,21,24,27,28,35,37,39,40]	+3V_S5	
[5,9]	+1.05V	
[9,22,23,26]	+1.5V	

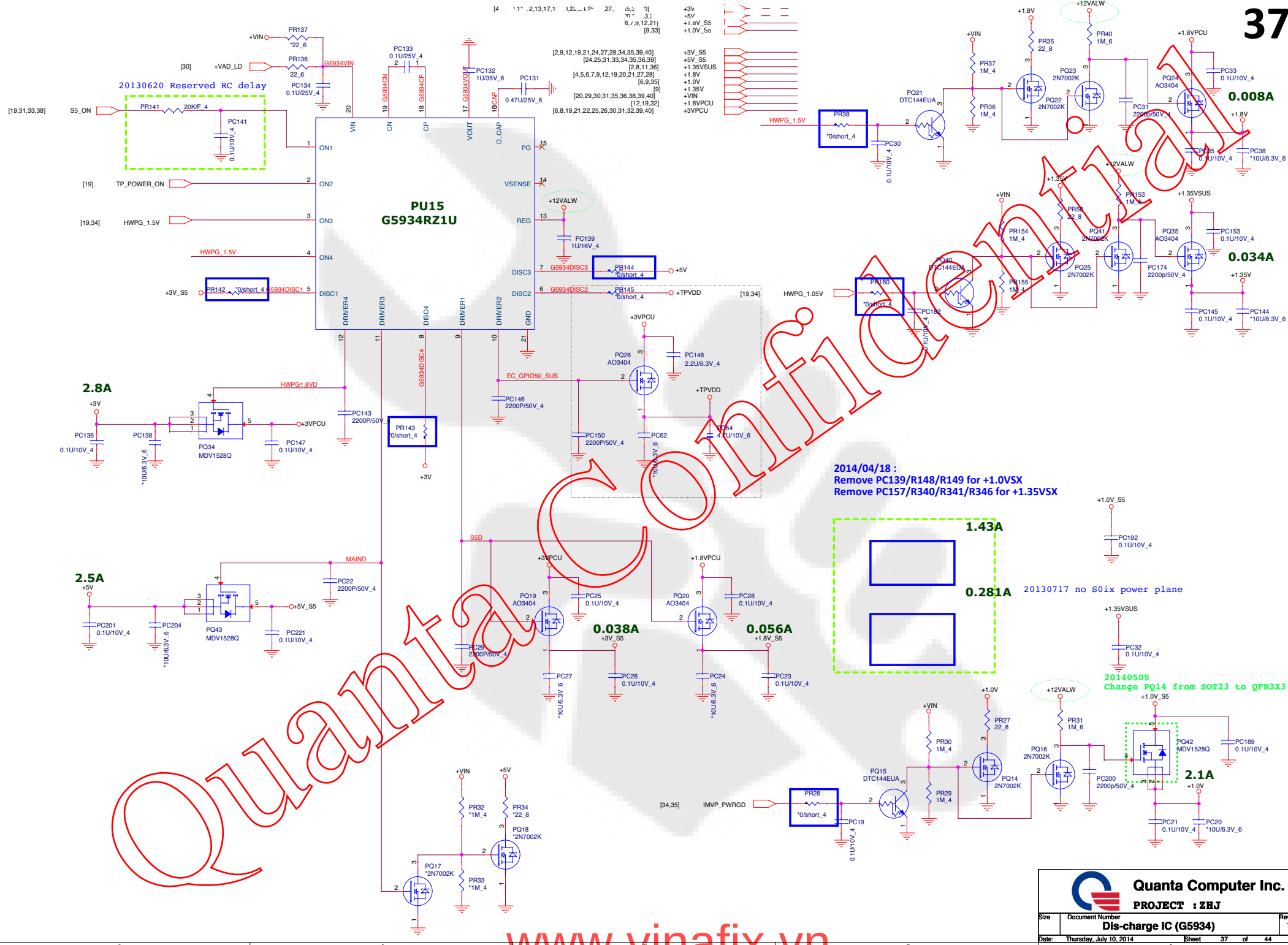


Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.05V/1.5V	1A
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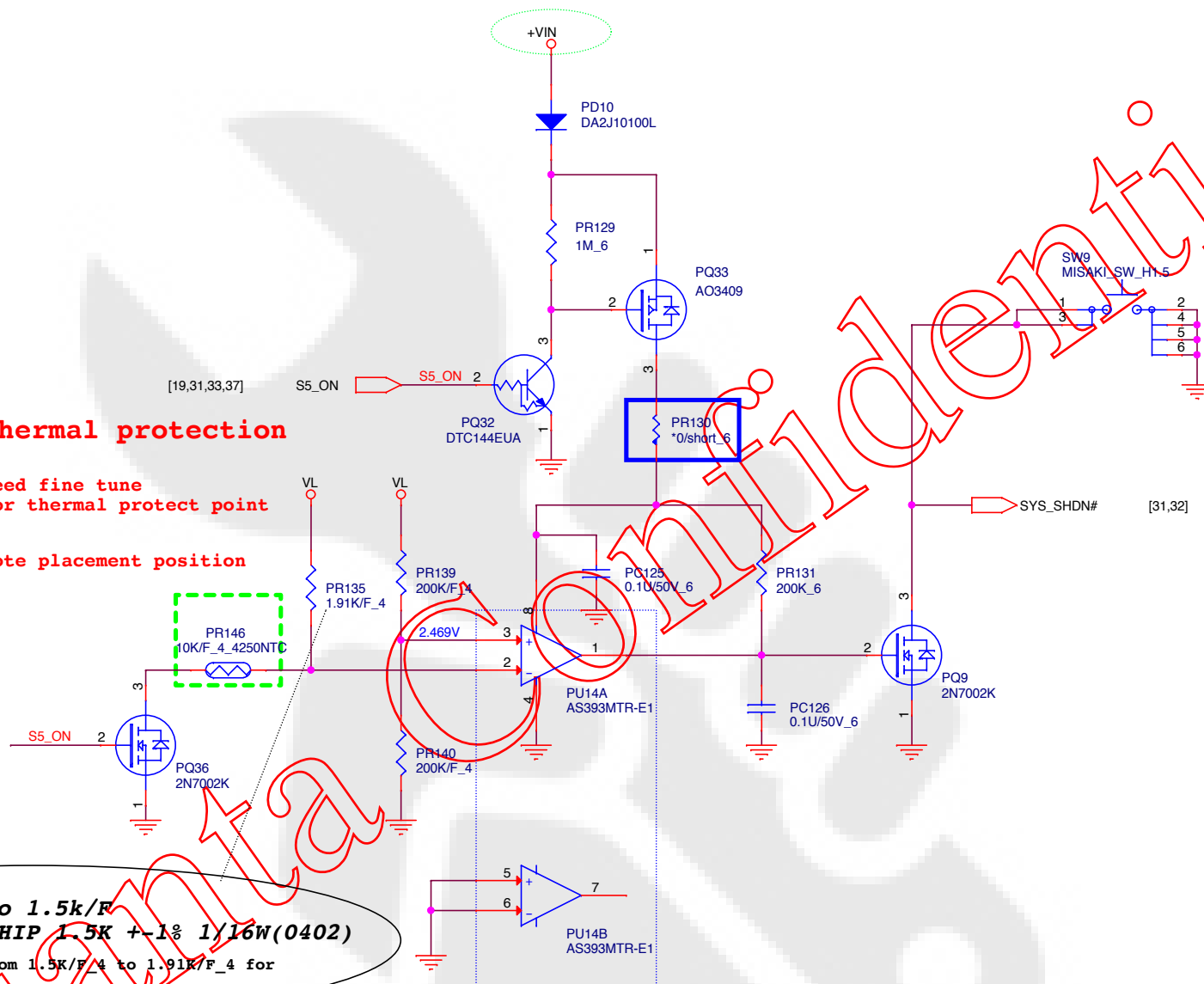




Thermal protection

Need fine tune
for thermal protect point

Note placement position



note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K $\pm 1\%$ 1/16W(0402)

20140702 Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request

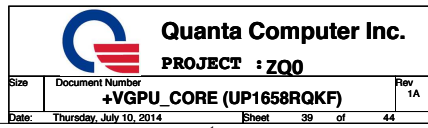
For EC control thermal protection (output 3.3V)



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PROJECT : ZHJ

Size	Document Number	Rev
	Thermal / Hole	1A
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[13,14,15] +1.05V_GFX
[13,14,16] +1.5V_GFX
[13,16,17] +3V_GFX

Remove JP12

20140421:
Change 554PG_1.05V to Test PAD.

TP37

554PG_1.05V

+1.05V_GFX
TDC : 1.553A
PEAK : 2.29A
Width : 90mil

Remove JP14

20140529:
Change PR125 from 10K to 26.7K Ohm
 $V0 = 0.6 * (R1 + R2) / R2$

20140421:
Change Enable from 3V_MAIN_PWRGD

+3V_GFX
TDC : 0.17A
PEAK : 0.342A
Width : 20mil

Remove JP9

20140609:
Change PL9 from 3.3uH to 2.2uH

Remove JP10

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.24A
PEAK : 4.25A
Width : 170mil

Change to 1.35V_GFX

20140606:
modify +1.5V_GFX PG sequence

20140709 Change PR9 from 54.9K to 66.5K for EMI request and +1.5V_GFX will Change to 1.35V_GFX



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PROJECT : ZQ0

Size Document Number
+1.5V_GFX/+1.05V_GFX/+3V_GFX
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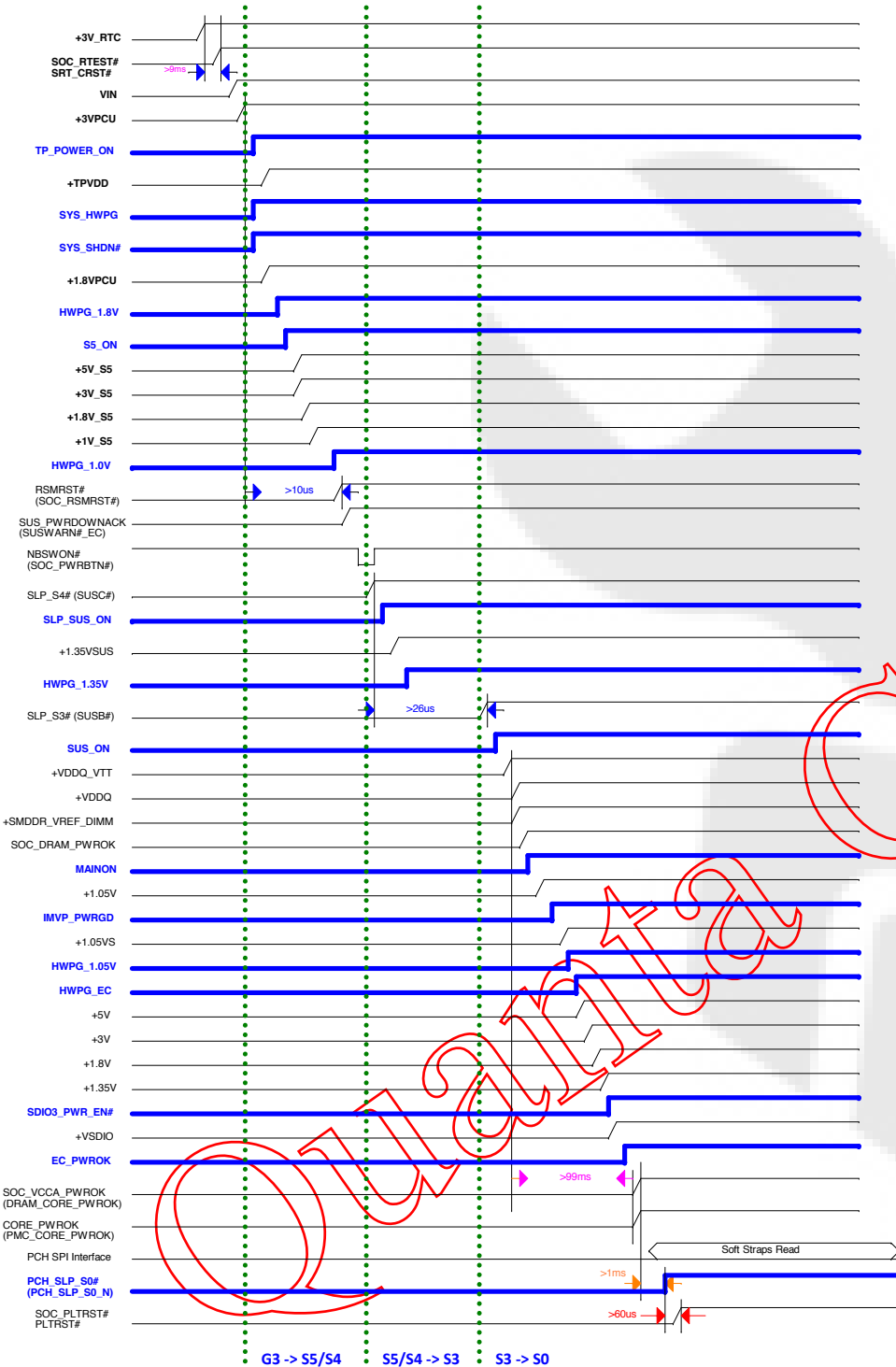
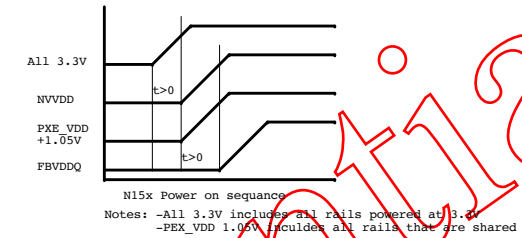
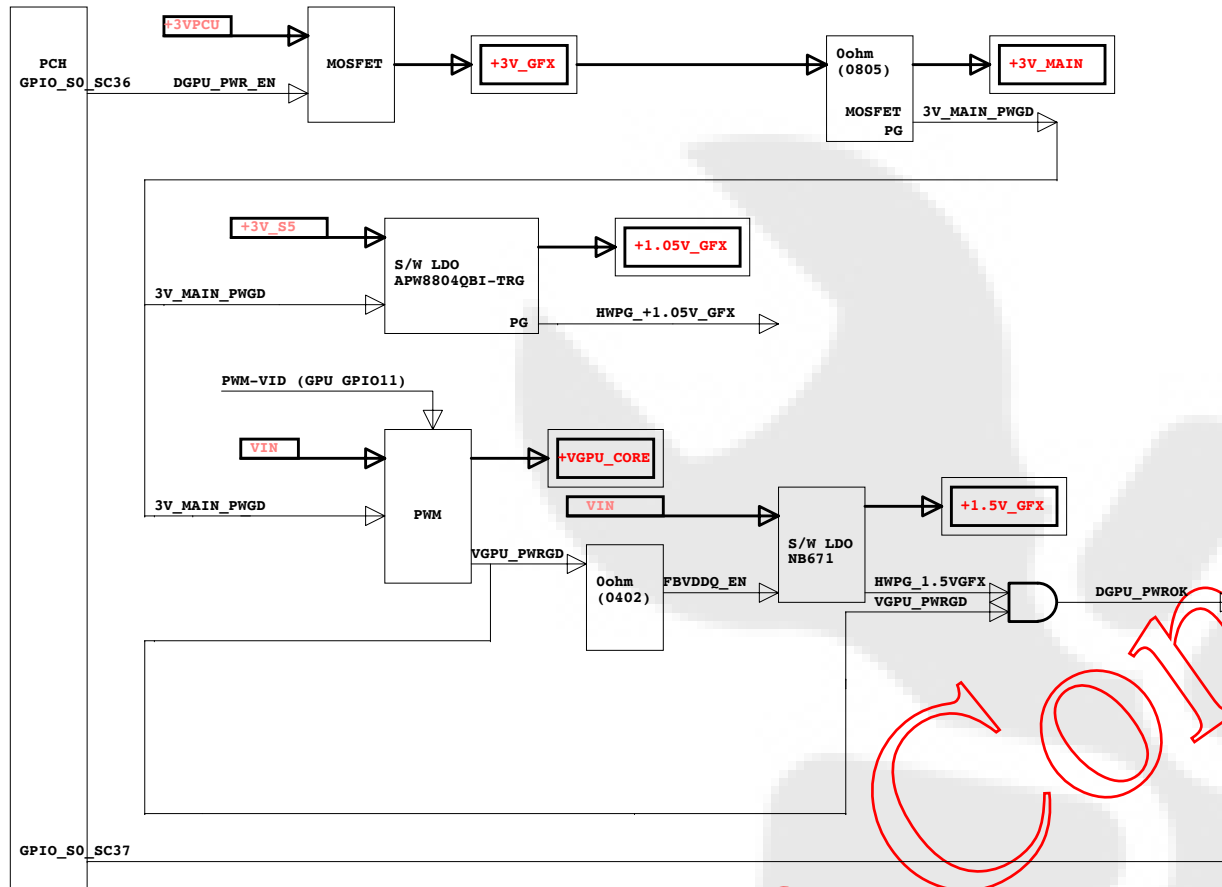


Table 37. SoC Sx-States to SLP_S*#

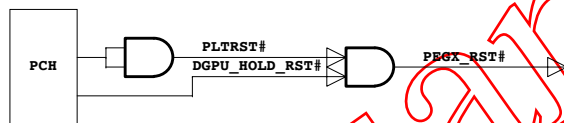
State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

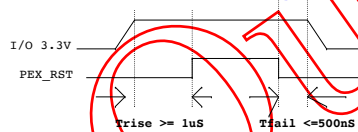
VGA power up sequence

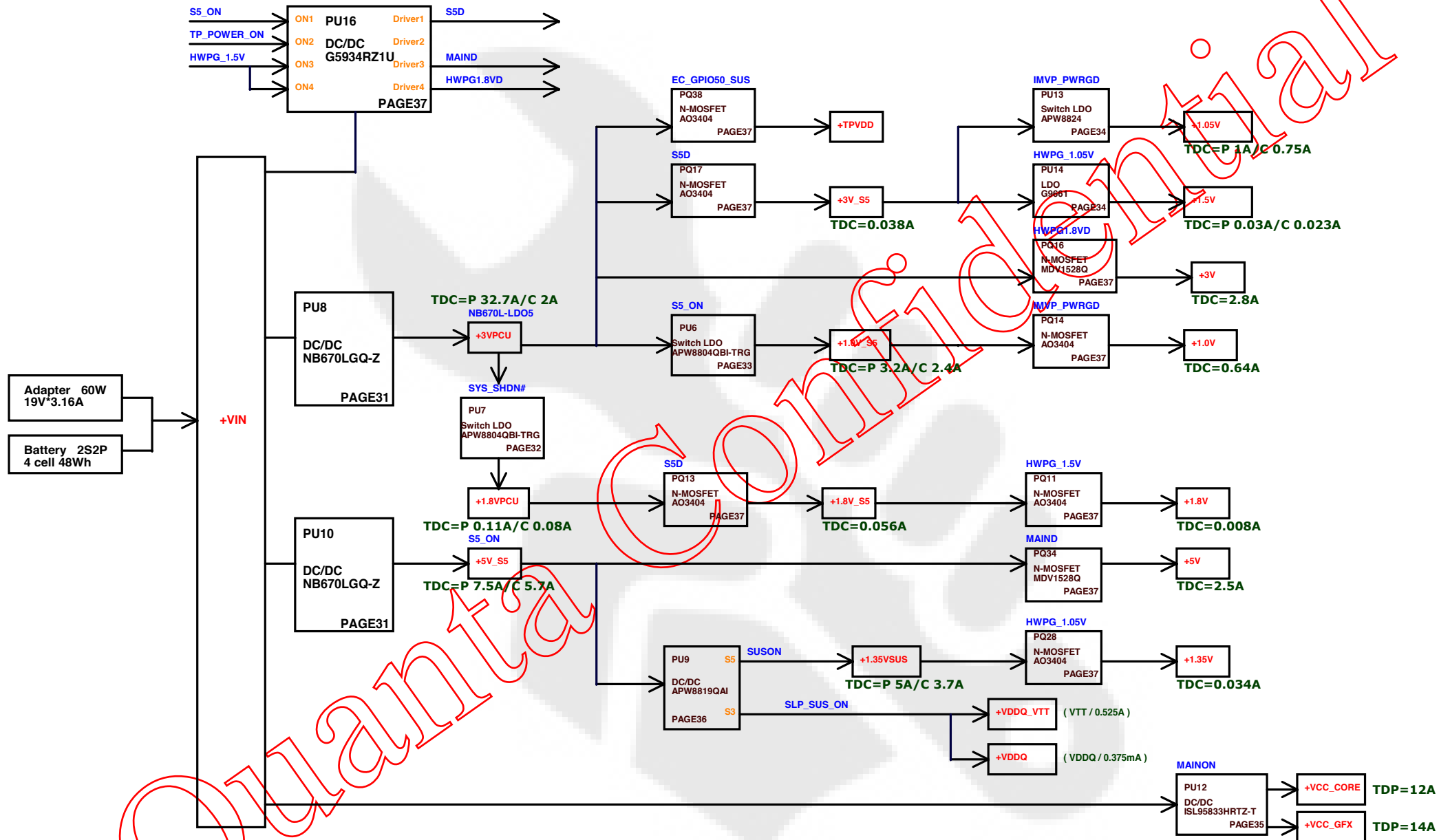


VGA Reset



PEX_RST timing





Model	Date	CHANGE LIST
ZYL REV:A		1. FIRST RELEASED
		Check CPU of P/N. Change VRAM of P/N. Check PJ6 for UMA or Dis- GVA.
		VGA Chip (Buy and Sell) AJON15VOT07 VR4GbIII9: HYNIX Graphic DDRIII 900 4Gb H5TC4G63APR-11C AKD5PGWTW13 (B/S) MICRON Graphic DDRIII 900 4Gb MT41J256M16HA-093G:E AKD5F2S1L05 (B/S) SAMSUNG Graphic DDRIII 900 4Gb K4W4G1646D-BC1A AKD5PGWT504 (B/S) CPU (Buy and Sell) Intel BayTrail M cpu n3530 VGA Chip (Buy and Sell) AJON15VOT07 VRAM (Buy and Sell) VR2GbIII9 HYNIX Graphic DDRIII 900 2Gb H5VTC2G63PFR-11C AKD5M2DTW04 ; AKD5M2DTW05 (B/S) MICRON Graphic DDRIII 900 2Gb MT41J128M16JT-093G:K AKD5MGSTL15 ; AKD5MGSTL25 (B/S) SAMSUNG Graphic DDRIII 900 2Gb K4W2G1646Q-BC1A AKD5MGST117 ; AKD5MGST113 (B/S)
ZYL REV:B	5/27	1.PAGE.22 , modify SW10 pin3 connect to pin1 ,pin2 connect to pin4&pin5&pin6 2.PAGE.24 , modify CN16 & CN18 footprint from "USB-TARA4-9B1323-9P-SMT" to "UB2-UARDM-4K1926-4P-R"
	5/28	1.PAGE.25 , SWAP CN23 USB_CAR_N & USB_CAR_P
	5/29	1.PAGE.40 , Change PR125 from 10K to 26.7K due to 1.05V_GFX output is incorrect
	6/6	1.PAGE.6 , Change C458 - C453 from 10P/50V to 12P/50V 2.PAGE.40 , Add PR239 to modify +1.5V_GFX PG sequence
	6/9	1.PAGE.29 , change hole 18 - hole20 - hole28 footprint from "HG-C315D110P2" to "H-C315D110P2" 2.PAGE.19 , Add D37 D38 C521 3.PAGE.20 , change R66 R67 R69 R70 R71 R73 R74 R76 from 620ohm to 619 ohm 4.PAGE.29 , Change C430 from "CH22206K917" to "CH22206J911" 5.PAGE.22 , Change C464 C466 C468 C469 from "0.01u/16V_4" to "0.01u/25V_4"
	6/10	1.PAGE.29 , reserve & mount C522 C523 C524 for ESD 2.PAGE.40 , Change PL9 from 3.3uH to 2.2uH for modified 1.5V_GFX efficiency.
	6/11	1.PAGE.24 , delete R465 R468 R522 R530 & mount L28,L31 for EMI
	6/13	1.PAGE.7 , PAGE.26,PAGE.28 , unmount R427,C310,R452,R453 2.PAGE.19 , mount D16 and change value form 14V/38V to 5V/30V 3.PAGE.26 , mount C338,C339,C340,C341 for EMI
ZYL REV:C	6/25	1.PAGE.6 , Change G9 - G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" 2.PAGE.26 , Change R311 - R324 - R565 - R562 - R550 - R566 - L23 - R13 from "0ohm" to "shortpad"
	6/27	1.PAGE.7 & 28 , Unmount R411 & Delete R147,R148,R149 2.PAGE.9 , Delete R180 for CPU +1.0V voltage
	7/1	1.PAGE.24 & 25 , Change C279,C224,C414 from 100u/6.3V_3216 to 100u/6.3V_3528
	7/2	1.PAGE.38 , Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request
	7/9	1.PAGE.40 , Change PR9 from 54.9K to 64.9K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

 Quanta Computer Inc.		DOC NO.	PROJECT MODEL :	ZYL/ZYLA	APPROVED BY:		DATE:
File	Document Number		PART NUMBER:		DRAWING BY:		REVISION:
PROJECT : ZYL/ZYLA							
Change list							
Rev 1A							