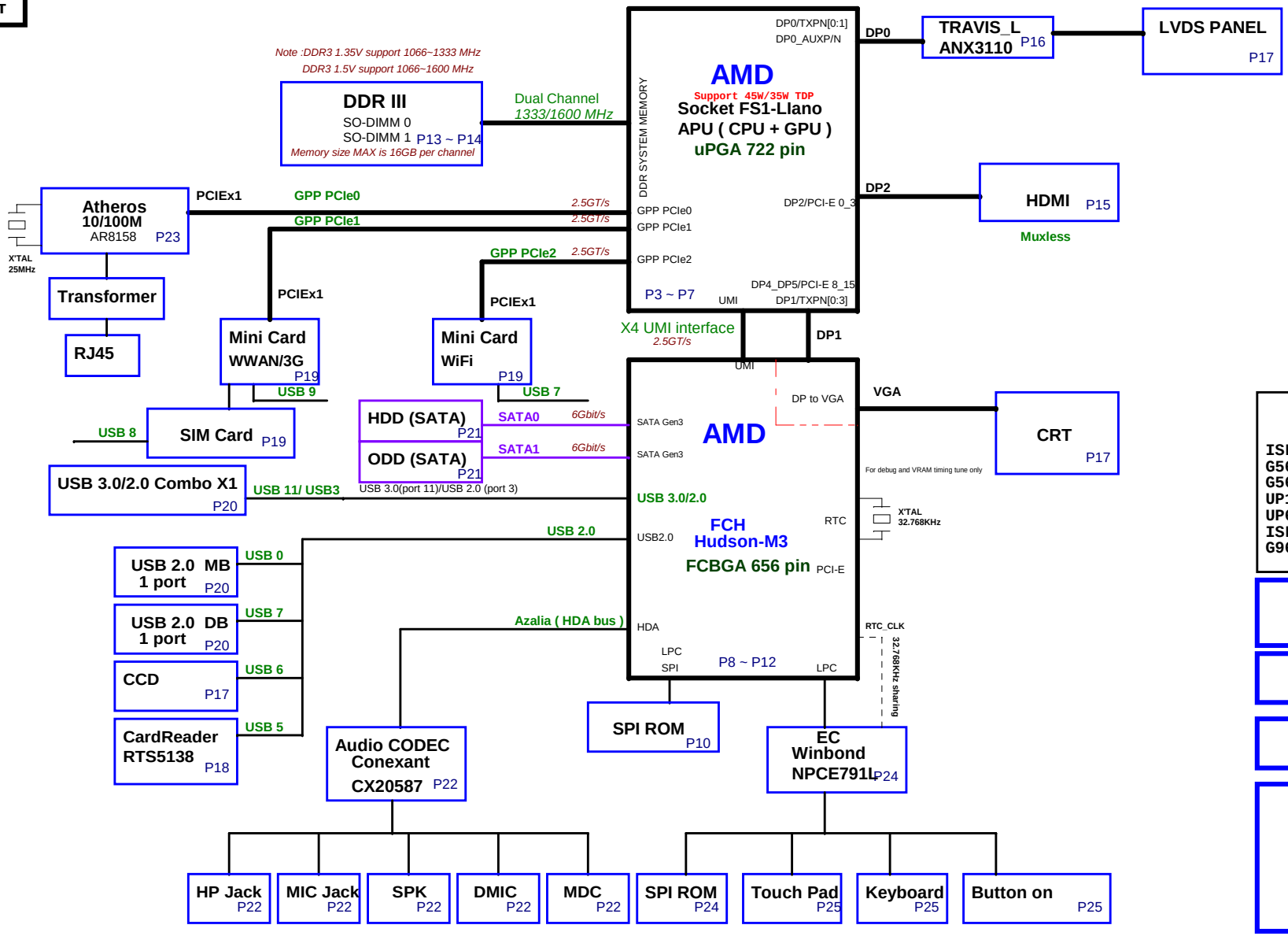
Rostock 20AS

TE8 BLOCK DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



POWER SYSTEM

ISL6267HRZ-T	P.28
G5602R41U	P.29
G5602R41U	P.30
UP1561PQAG	P.31
UP6188AQAI	P.32
ISL88731CHRTZ-T	P.33
G9661-25ADJF12U	P.34

+VDD_CORE
+VDDNB_CORE

+1.5V
+1.5VSUS

+1.1V_DUAL
+1.1V

+3VPCU
+3V_S5
+3V
+5VPCU
+5V
+0.75V_DDR_VTT
+1.2V_VDDPR
+2.5V_VDDA

Quanta Computer Inc.
PROJECT : TE8
Size | Document Number | Rev
System Block Diagram | D3A
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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIN_ON	S0
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUS_ON	S0~S5
+VDD_CORE		VDDA_PWRGD	S0
+VDDNB_CORE		VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+3V_S5	S0
+1.1V	+1.1V	VRM_PWRGD	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+2.5V_VDDA	+2.5V	RUN_ON	S0

GND PLANE	PAGE
	ALL
AGND_DC/DC	
GND	20

Quanta Computer Inc.
PROJECT : TE8

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	FRONTPAGE	D3A

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Processor FS1-Llano (PCIE,UMI,GPP) <CPU>

03

U18F

PCI EXPRESS

GRAPHICS

GPP

UMI-LINK

HDMI

LAN

WLAN

3G

D3A: 0328

D3A: 0328

ok E3A BOM remove

CPU Thermal sensor / MB Local TEMP <THC>

near CPU

U28 G708T1U

Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 86dgree

Hysteresis is 30C

CPU Thermal trip

D3A: 0328

Q52 *2N7002_200MA

Q49 *MMBT3904-7-F_200MA

Q10 *MMBT3904-7-F_200MA

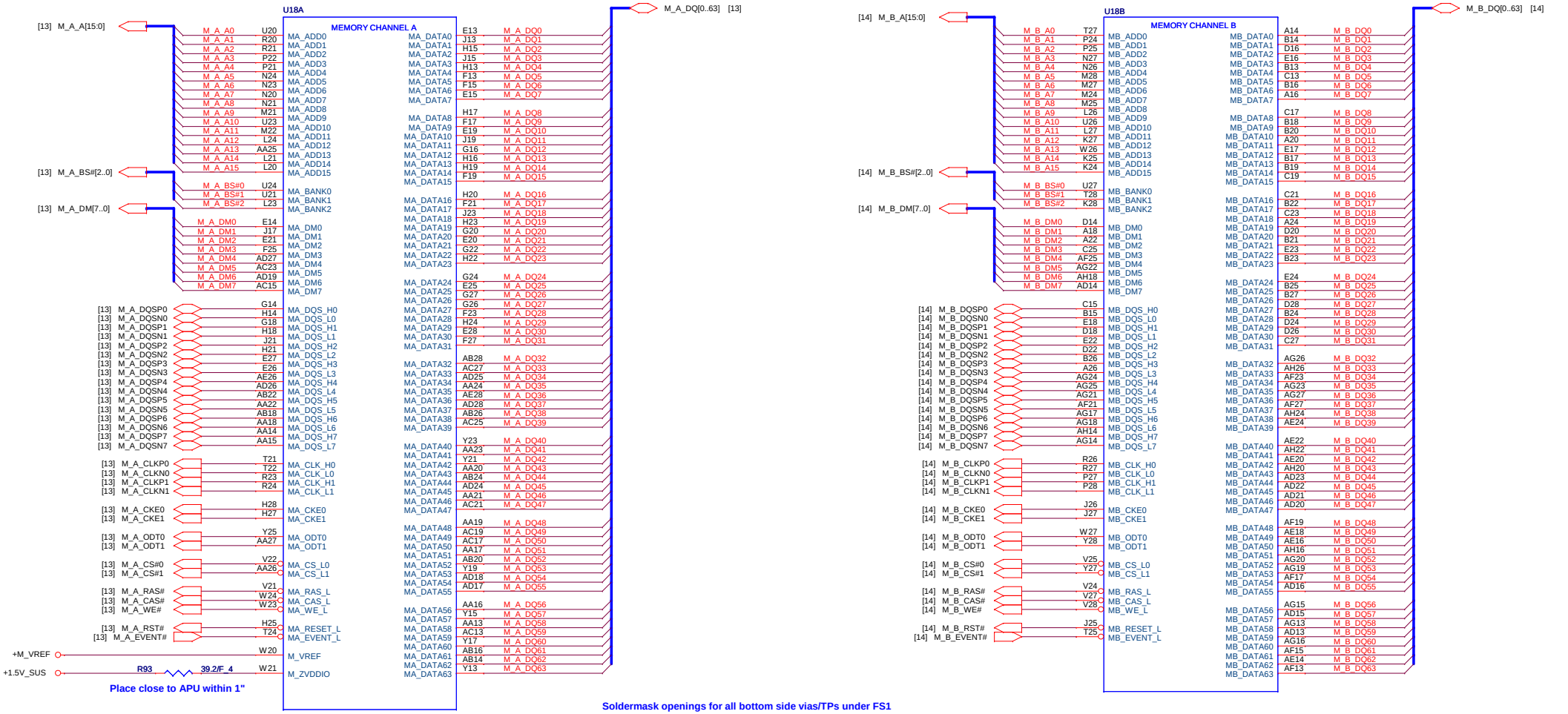
Quanta Computer Inc.

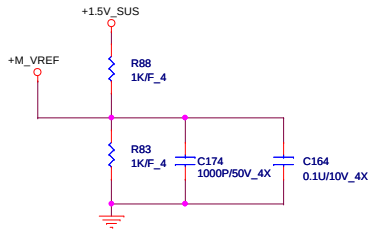
PROJECT : TE8

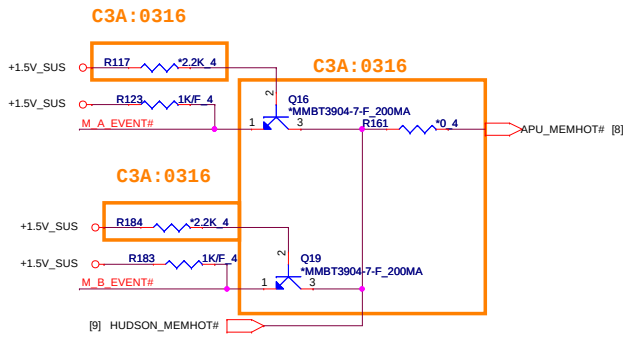
Size	Document Number	Rev
	Llano PCIE/UMI/GPP	D3A

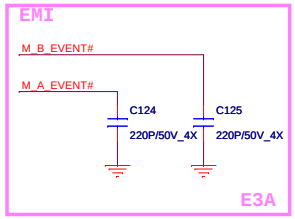
Date: Tuesday, April 26, 2011 Sheet 3 of 37

Processor FS1-Llano (DDR3 MEM I/F) <CPU>









Quanta Computer Inc.
PROJECT : TE8

Size	Document Number	Rev
	Llano DDR3 MEM I/F	D3A

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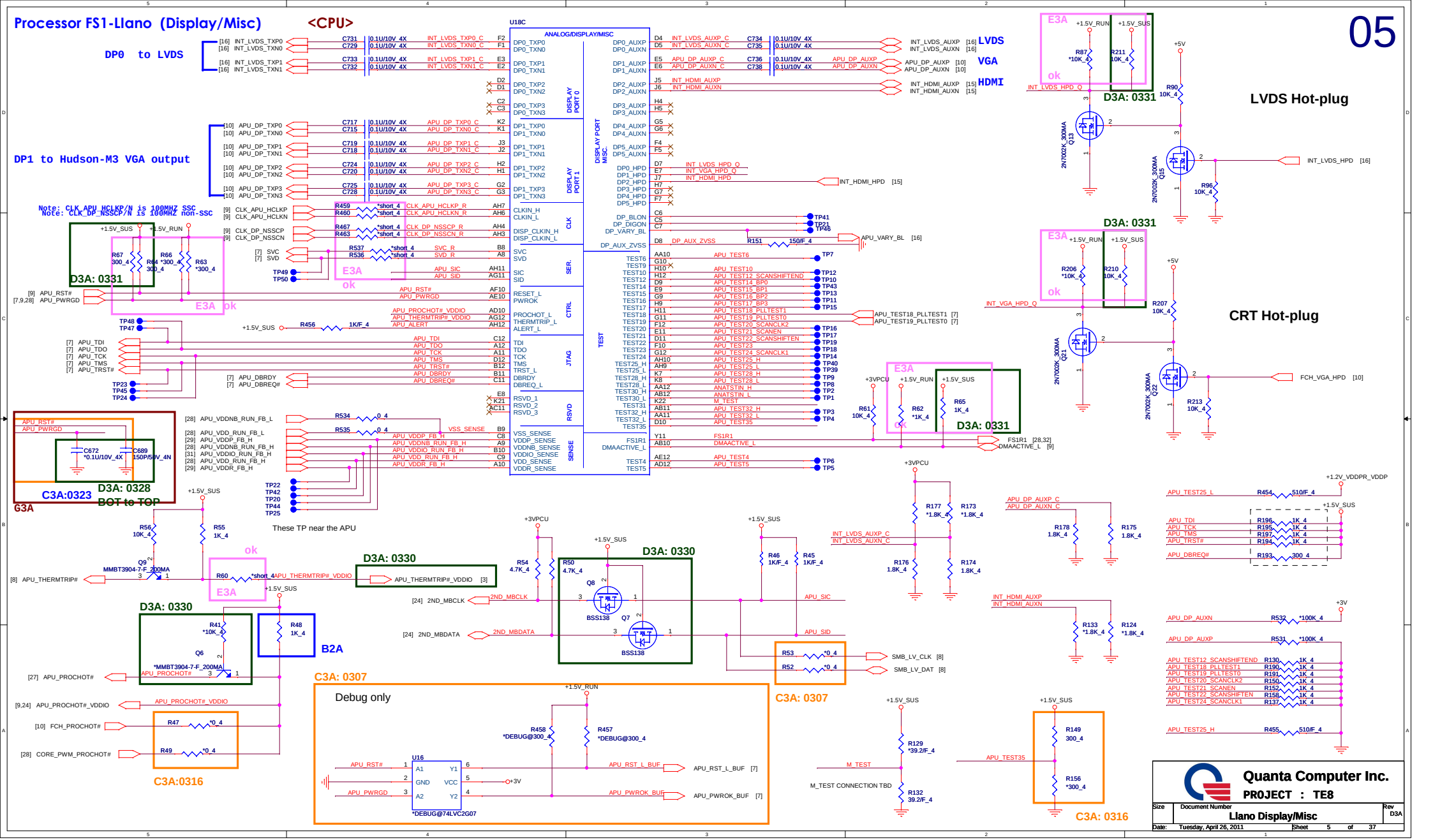
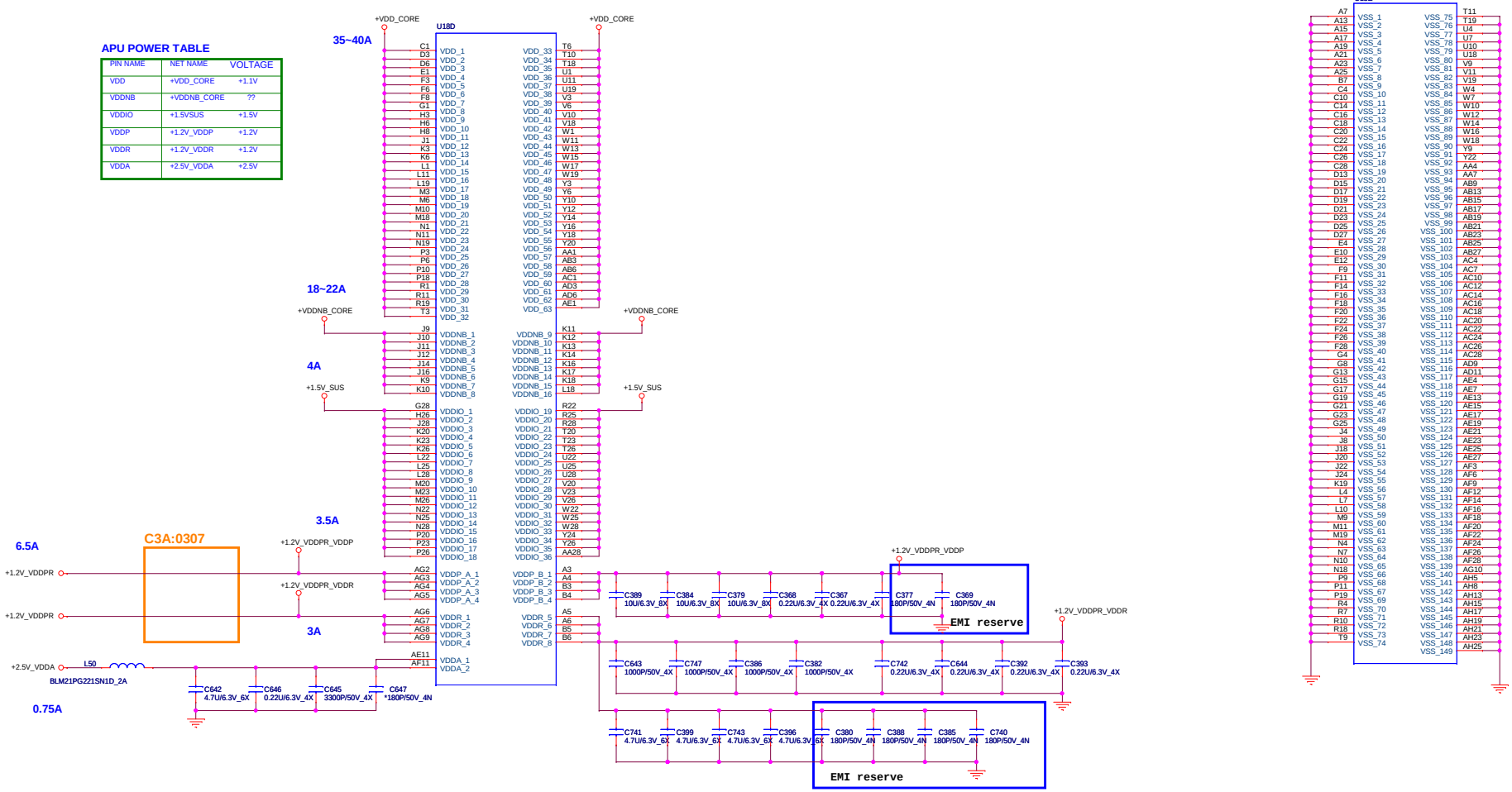


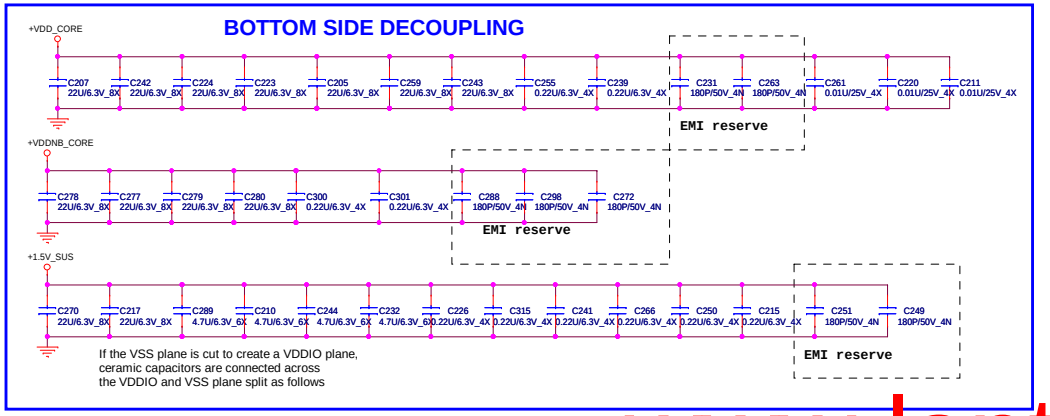
Processor FS1-Llano (POWER/GND) <CPU>

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



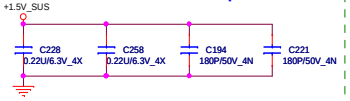
BOTTOM SIDE DECOUPLING



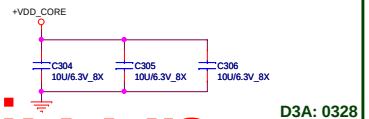
If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

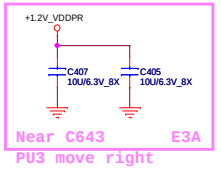
DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



DECOUPLING near power source





Quanta Computer Inc.		
PROJECT : TE8		
Size	Document Number: Llano POWER/GND	Rev: D3A
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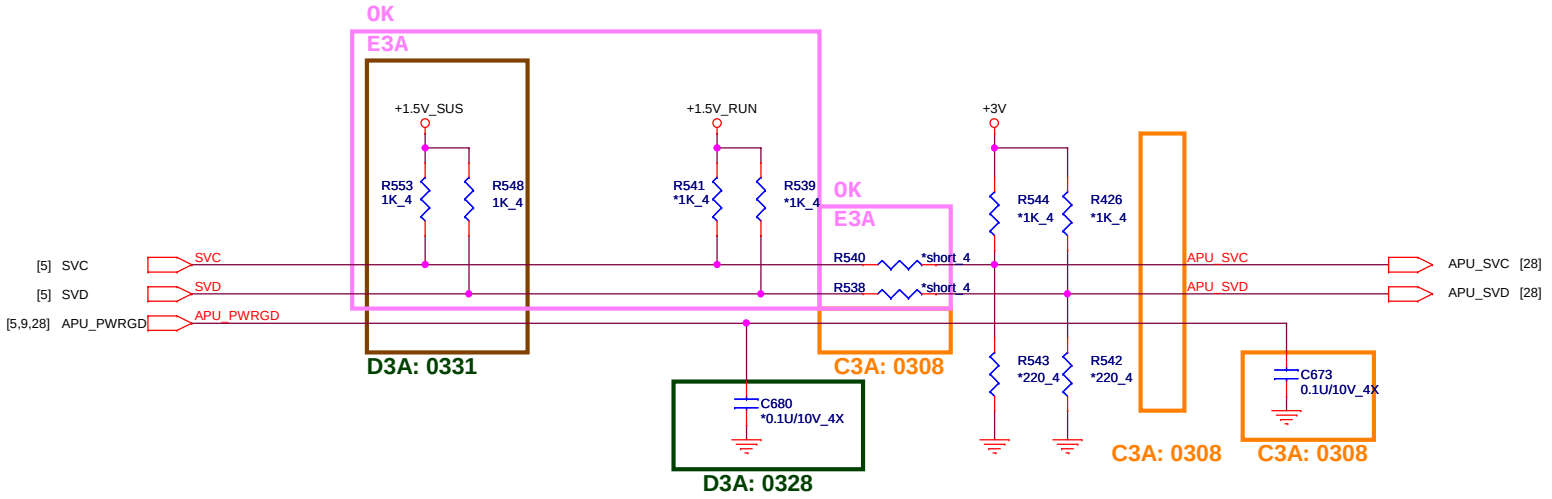
Processor FS1-Llano (DEBUG / OTHER) <CPU>

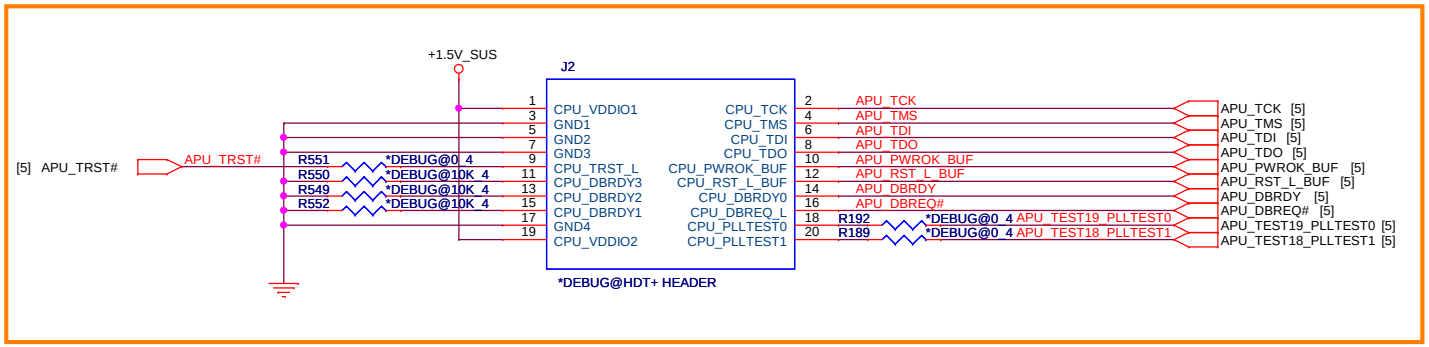
07

VID Override Circuit



HDT+ Connector

Debug only

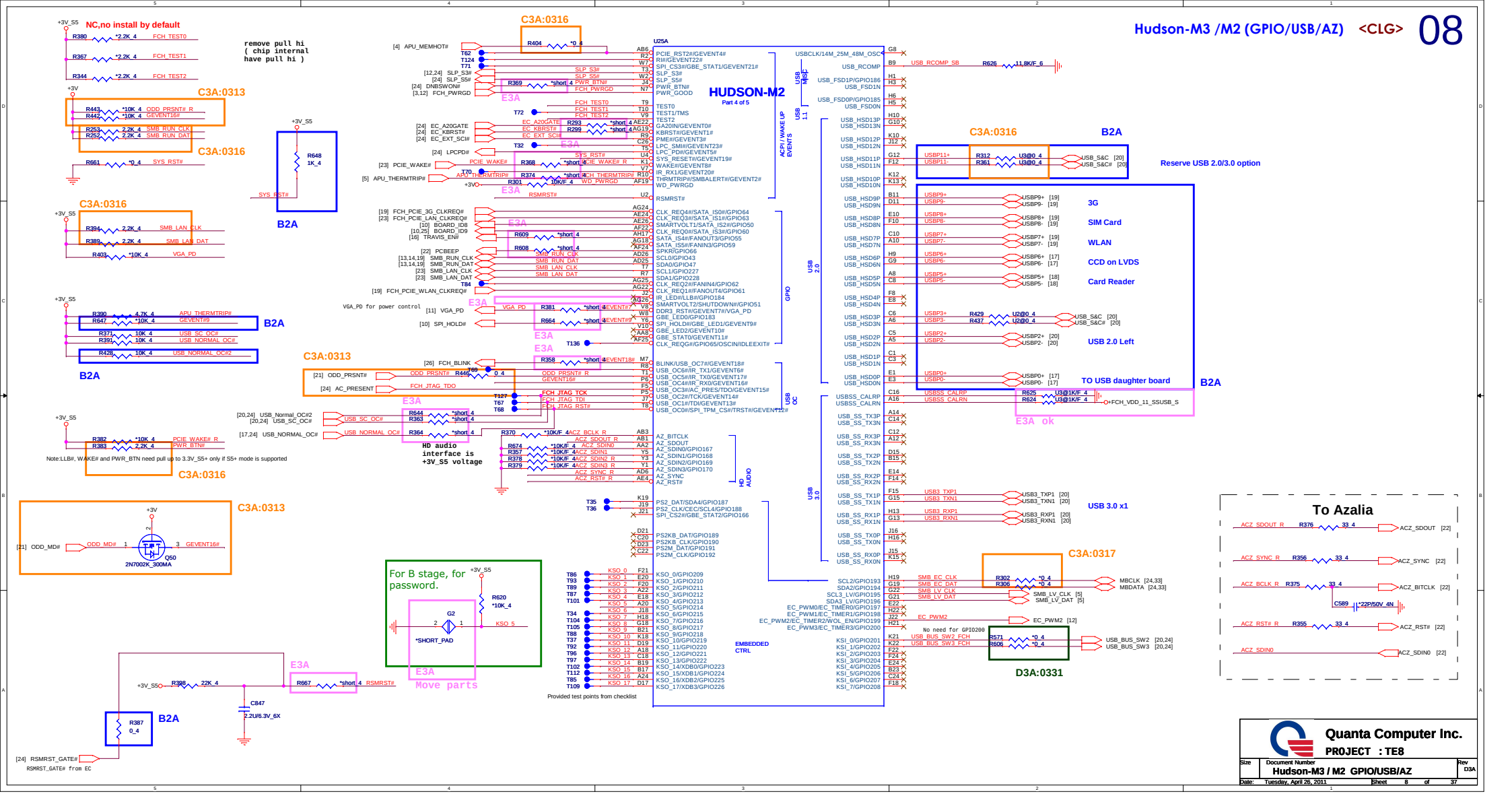


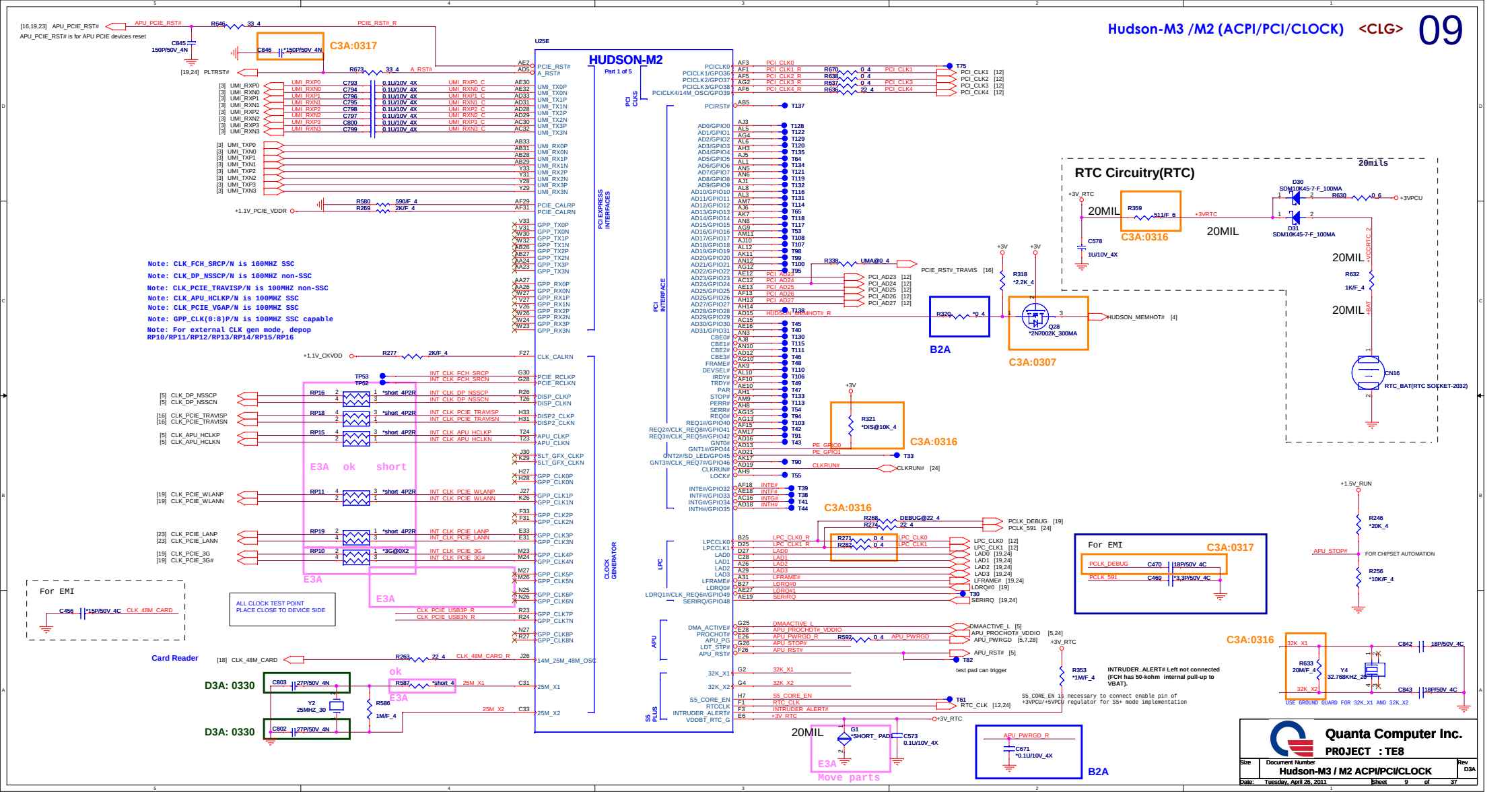
C3A: 0316

Quanta Computer Inc.

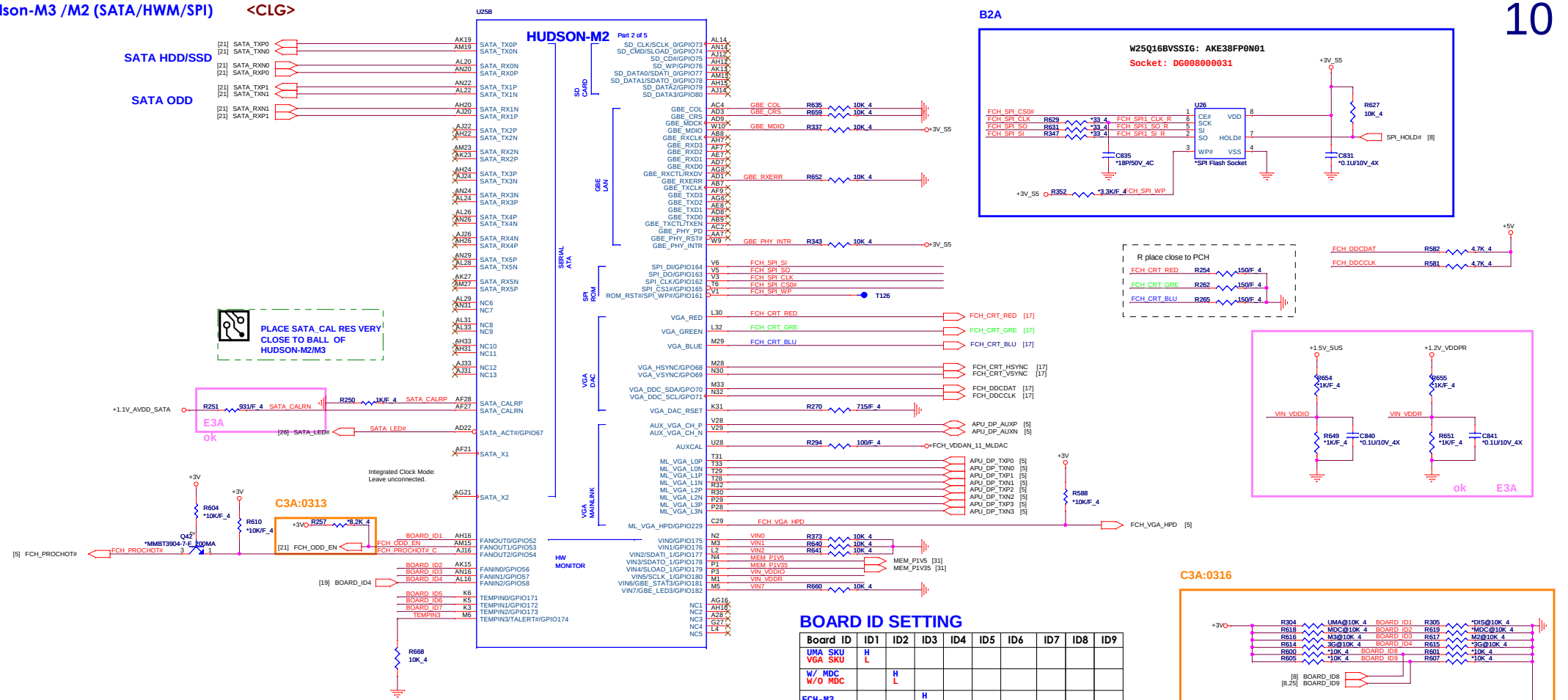
PROJECT : TE8

Size	Document Number	Rev
	Llano DEBUG&OTHER	D3A
Date: Tuesday, April 26, 2011	Sheet 7 of 37	





Hudson-M3 /M2 (SATA/HWM/SPI) <CLG>



B2A

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/ MDC W/O MDC		H L							
FCH-M3 FCH-M2			H L						
W/O 3G W/ 3G				H L					
15" 14"					H L				
W/O BT W/ BT						H L			
Reserve							H L		
Reserve								H L	
Reserve									H L

C3A:0316

Quanta Computer Inc.			
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	Hudson-M3 / M2 SATA/HWM/SPI		D3A
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Hudson-M3 /M2 (POWER/GND) <CLG>

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

11

VDDQ--3.3V I/O power 102mA

VDD-- S/B CORE power

CKVDD_1.1V-- Internal clock Generator I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

S5_3.3--3.3v standby power

S5_1.1V--1.1V standby power

C3A:0322

D3A: 0331

D3A: BOM do not change in C2

D3A: 0331

E3A ok

B2A

B2A

B2A

B2A

32 mA Max

233 mA Max

C3A : 0308

VGA_PD is generated from FCH

Quanta Computer Inc.
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Hudson-M3 / M2 POWER/GND
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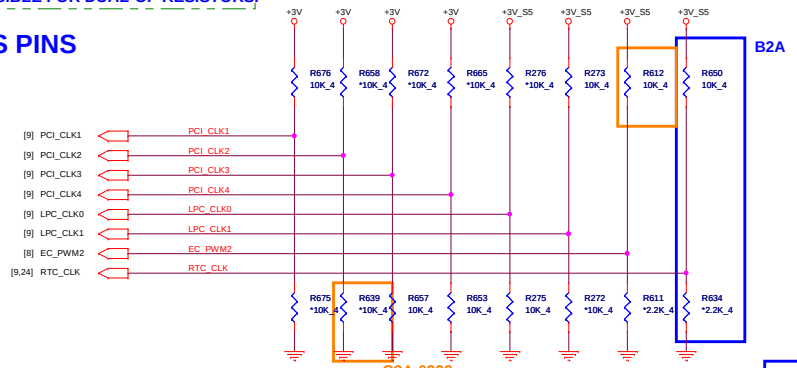
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

C3A:0317



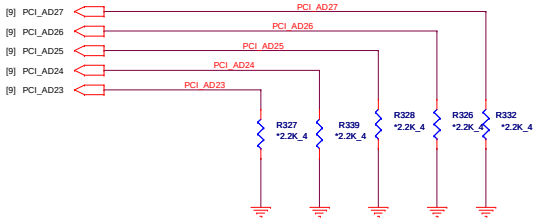
REQUIRED STRAPS

	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer enable	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	Watchdog Timer disable DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

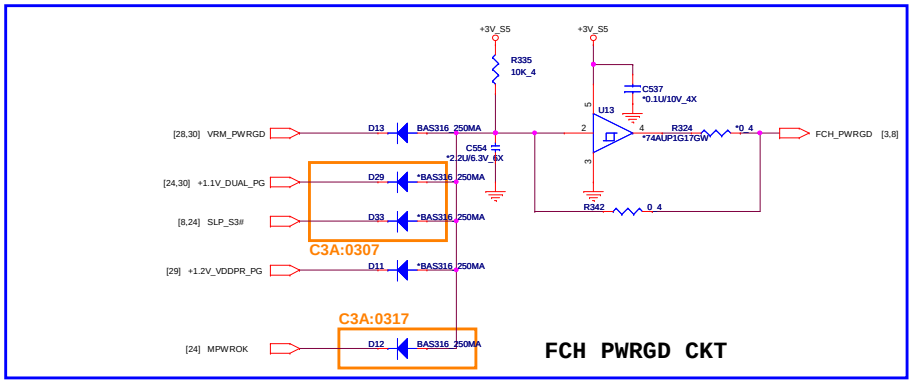
B2A

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



Quanta Computer Inc.
PROJECT : TE8

Size	Document Number	Rev
	Hudson-M3 / M2 STRAP/PWRGD	D3A

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DDRIII SO-DIMM-0 <DDR>

H=4

13

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4

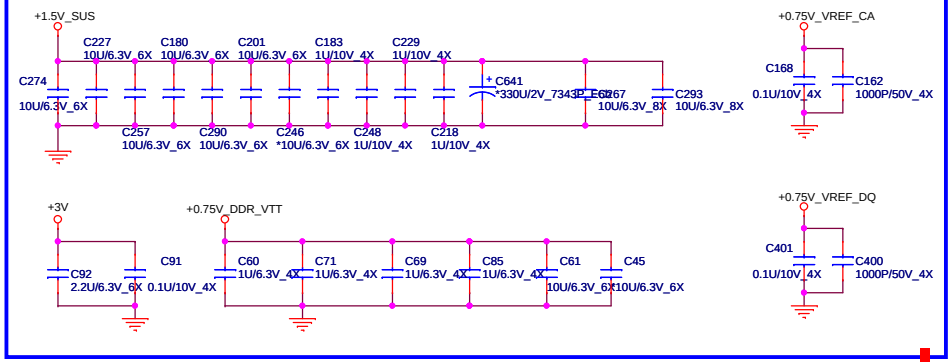
JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4

2.48A

Place these Caps near So-Dimm0.



Quanta Computer Inc.		
PROJECT : TE8		
Size	Document Number: DDRIII SO-DIMM-0	Rev: D3A
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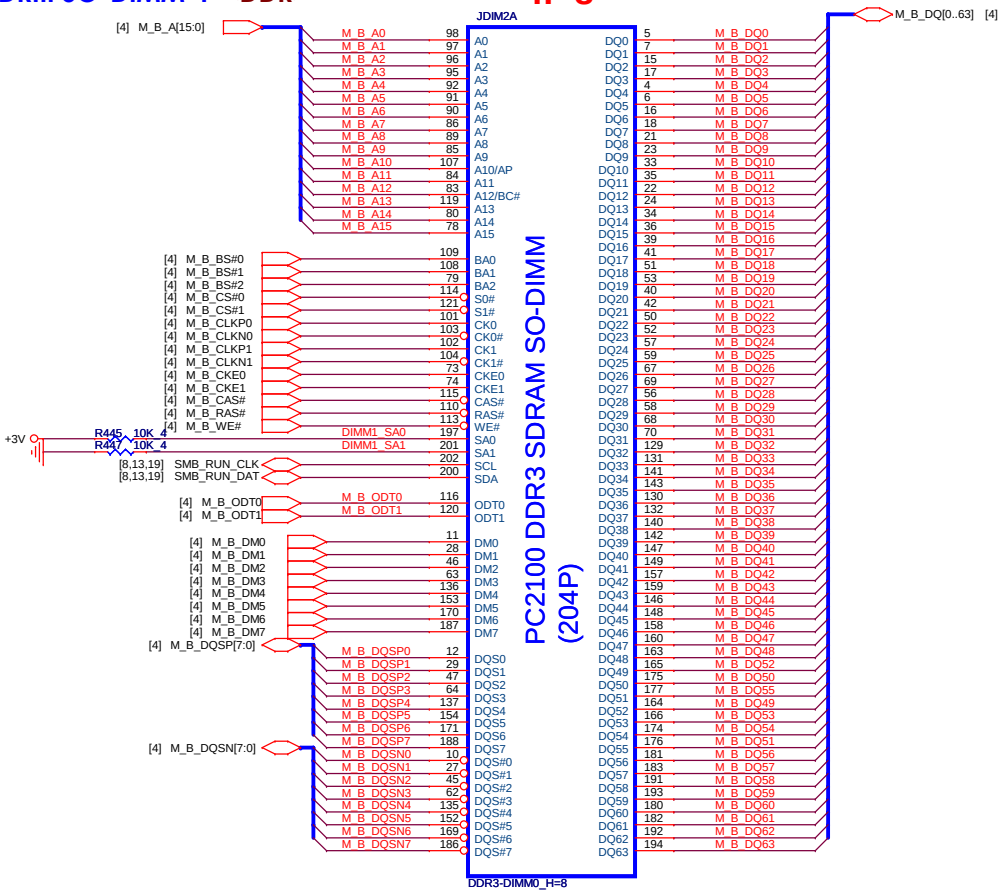
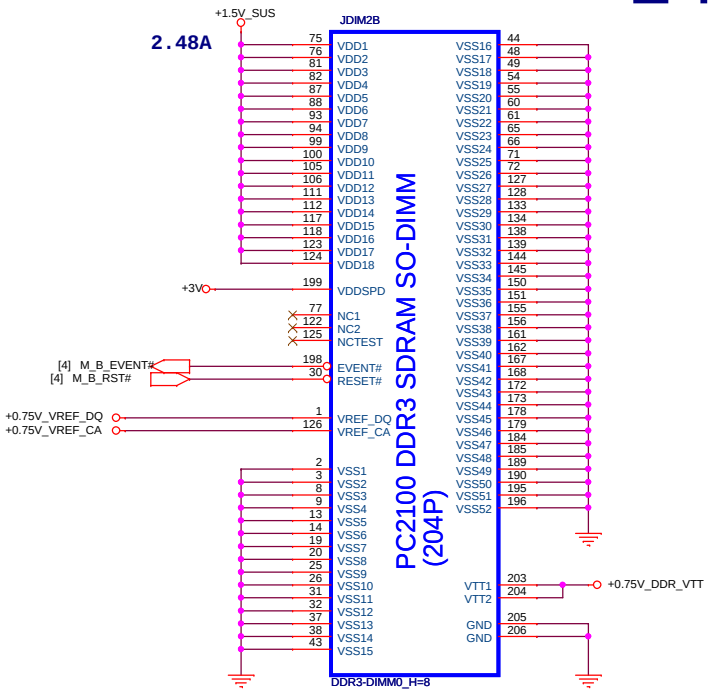
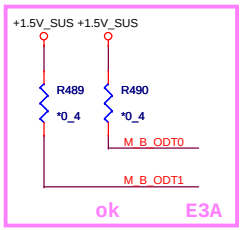
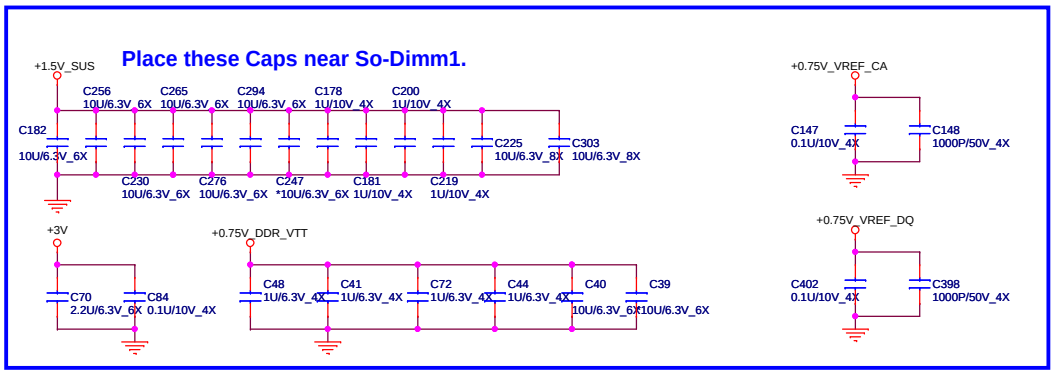
DDRIII SO-DIMM-1 <DDR>

H=8









Quanta Computer Inc.

PROJECT : TE8

Size	Document Number	Rev
	DDRIII SO-DIMM-1	D3A

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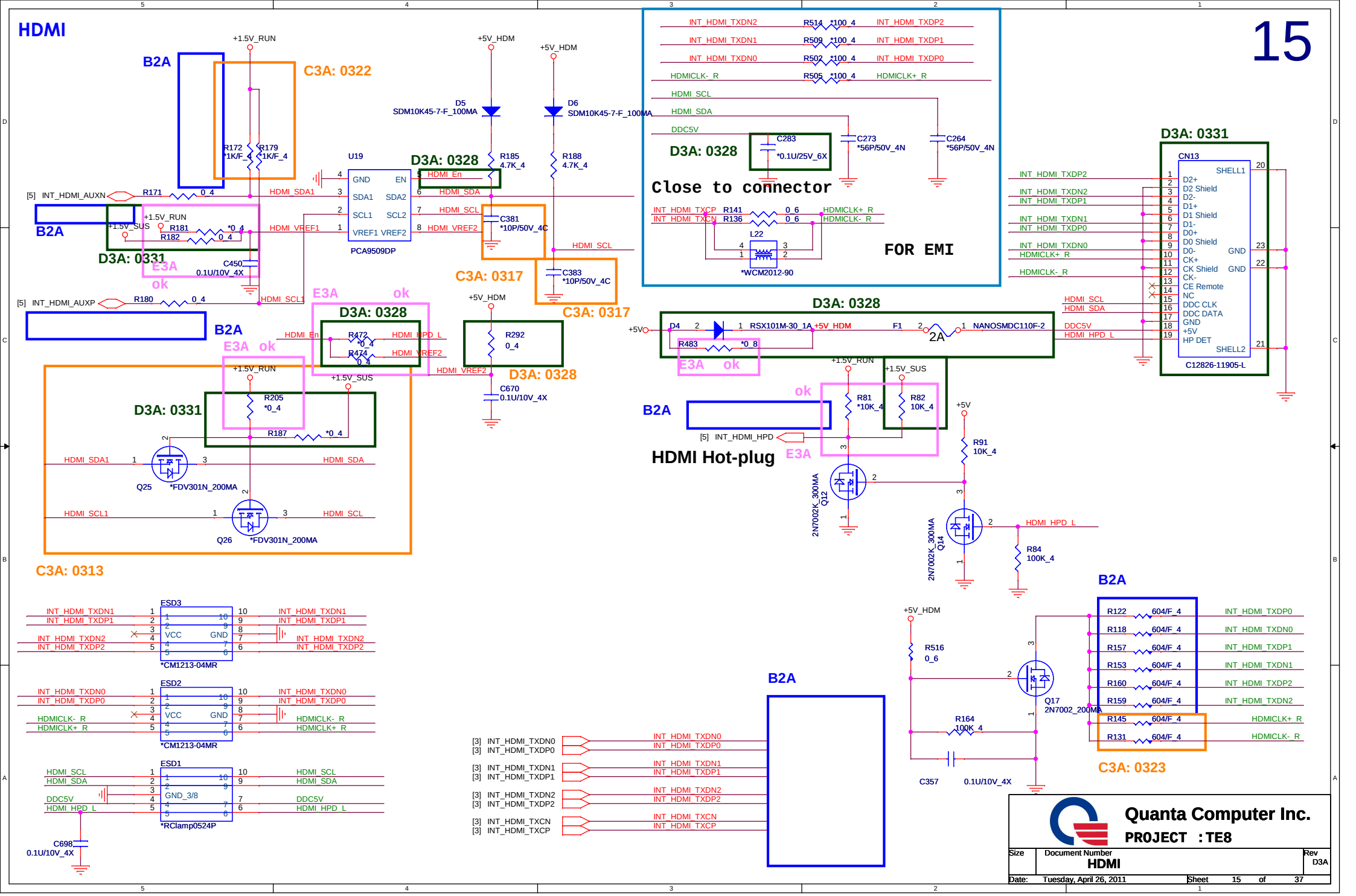
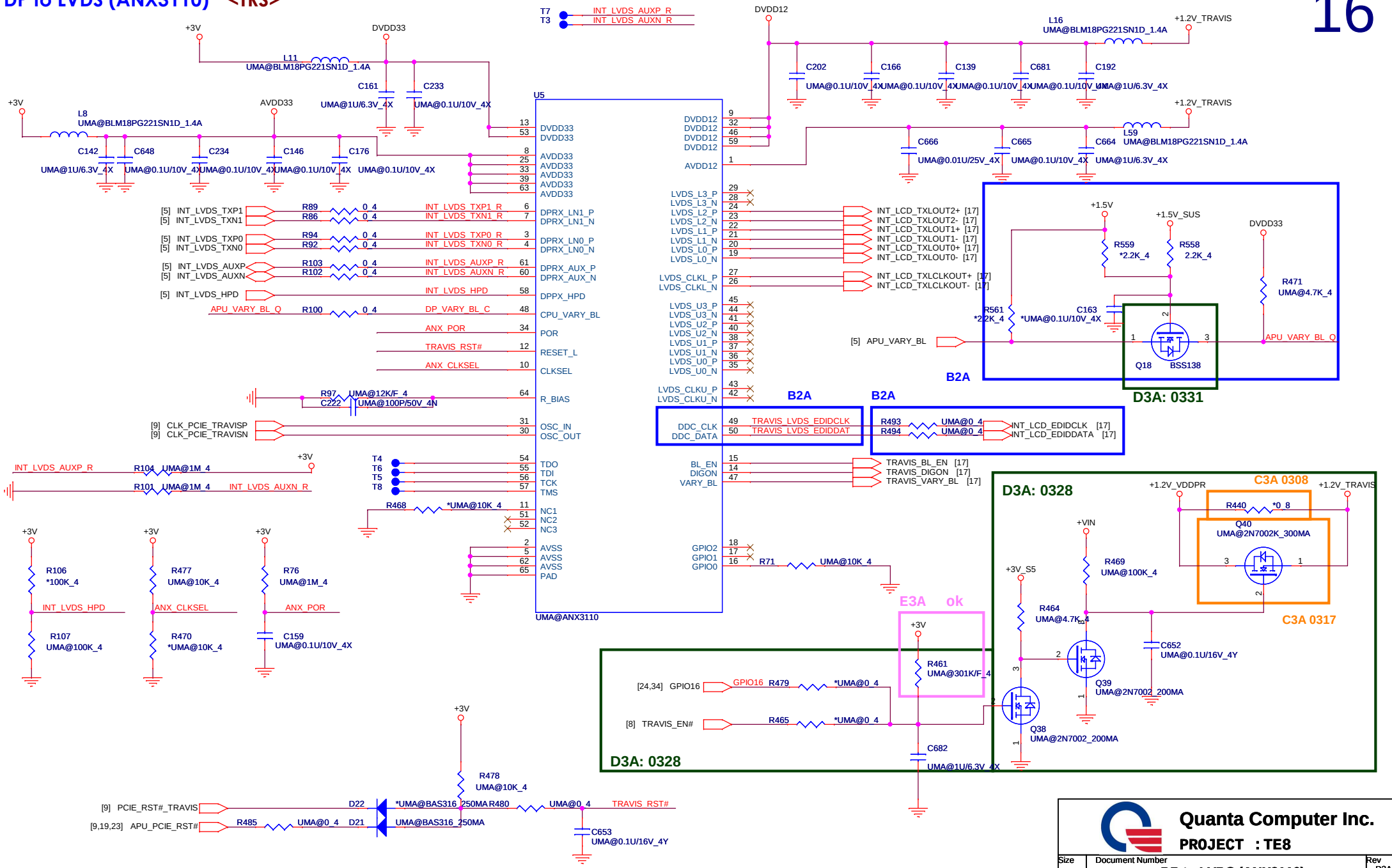
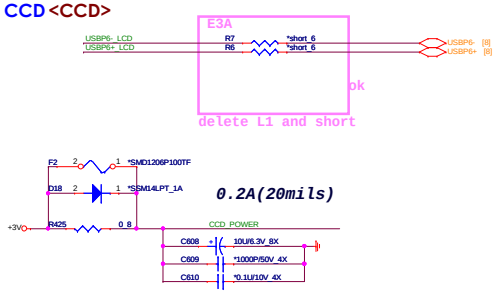


DP to LVDS (ANX3110) <TRS>

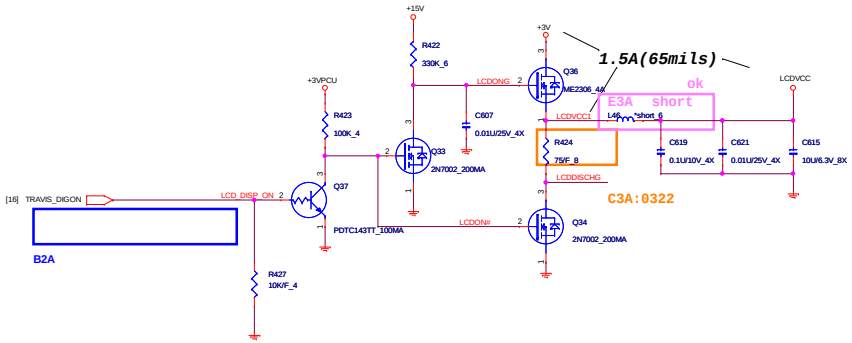
16



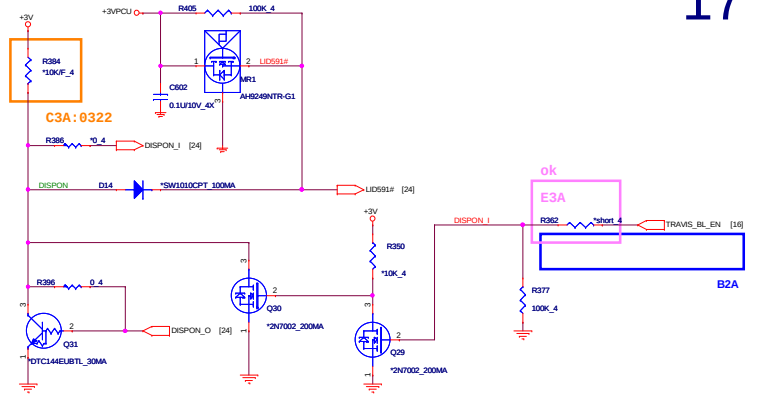
CCD <CCD>



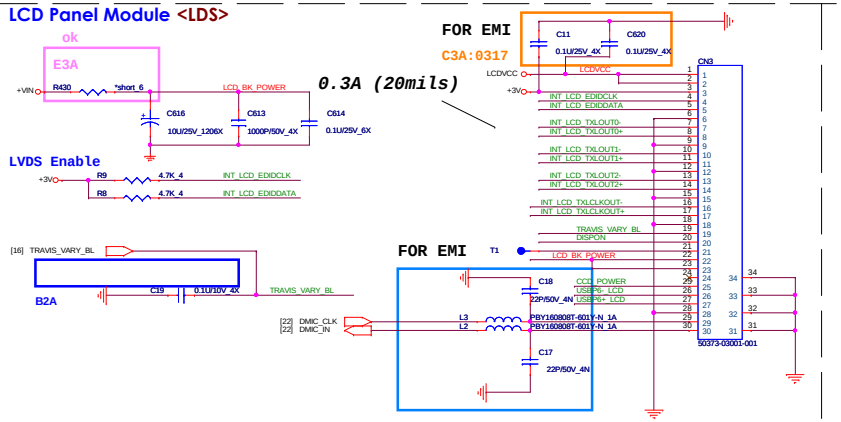
LCD POWER SWITCH <LDS>

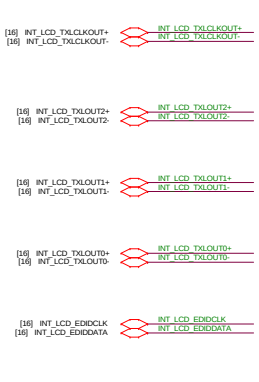


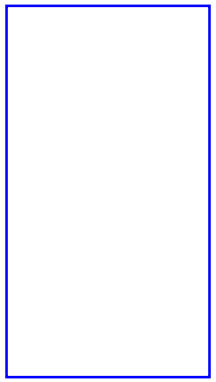
HALL SENSOR&BACK LIGHT SWITCH <HSR>

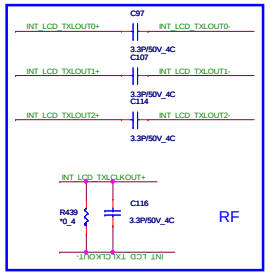


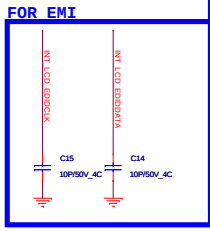
LCD Panel Module <LDS>

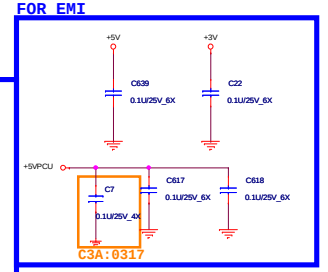




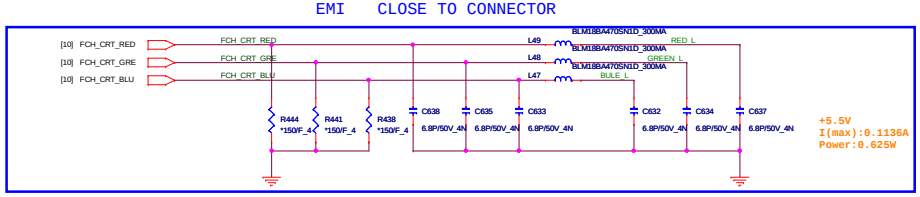


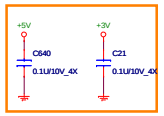


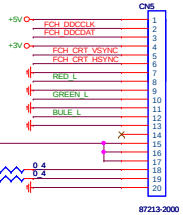


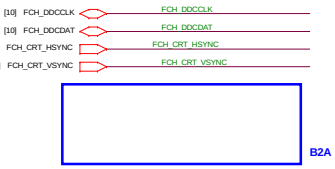


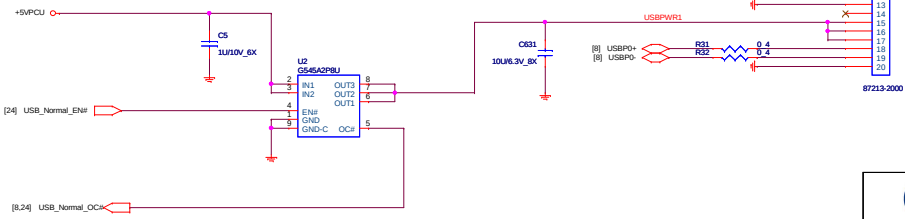
CRT <CRT>











Quanta Computer Inc.
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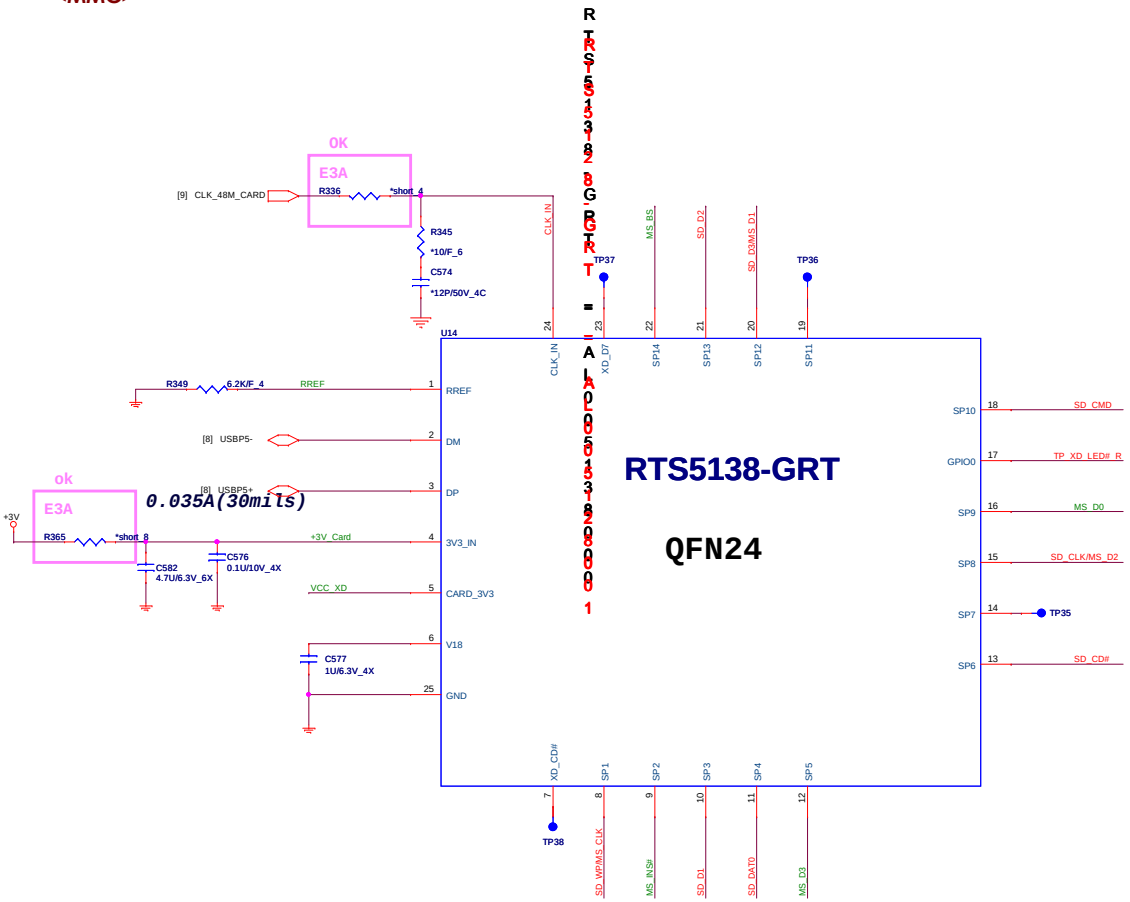
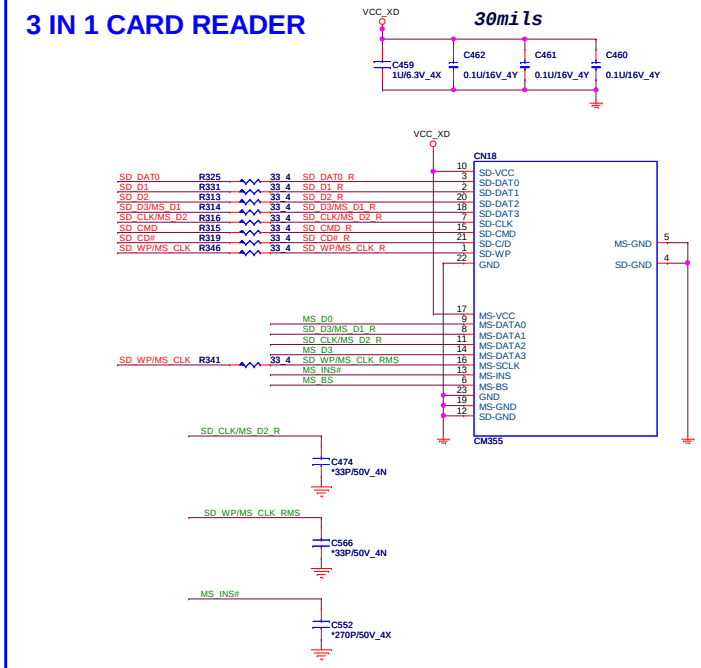
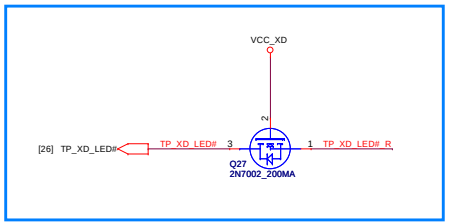
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER





Quanta Computer Inc.

PROJECT : TE8

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	CARD READ	D3A

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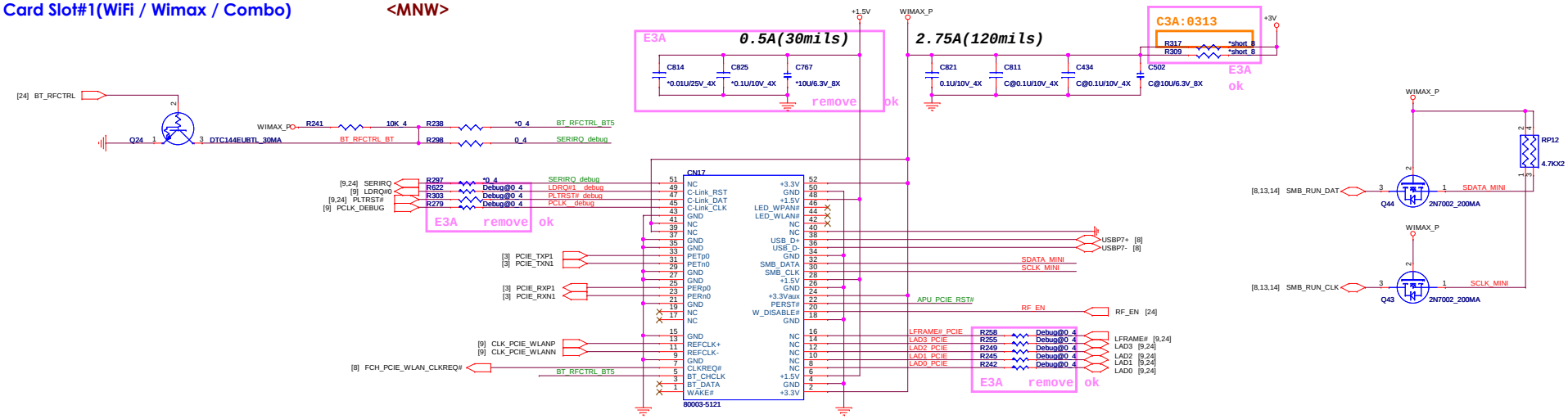
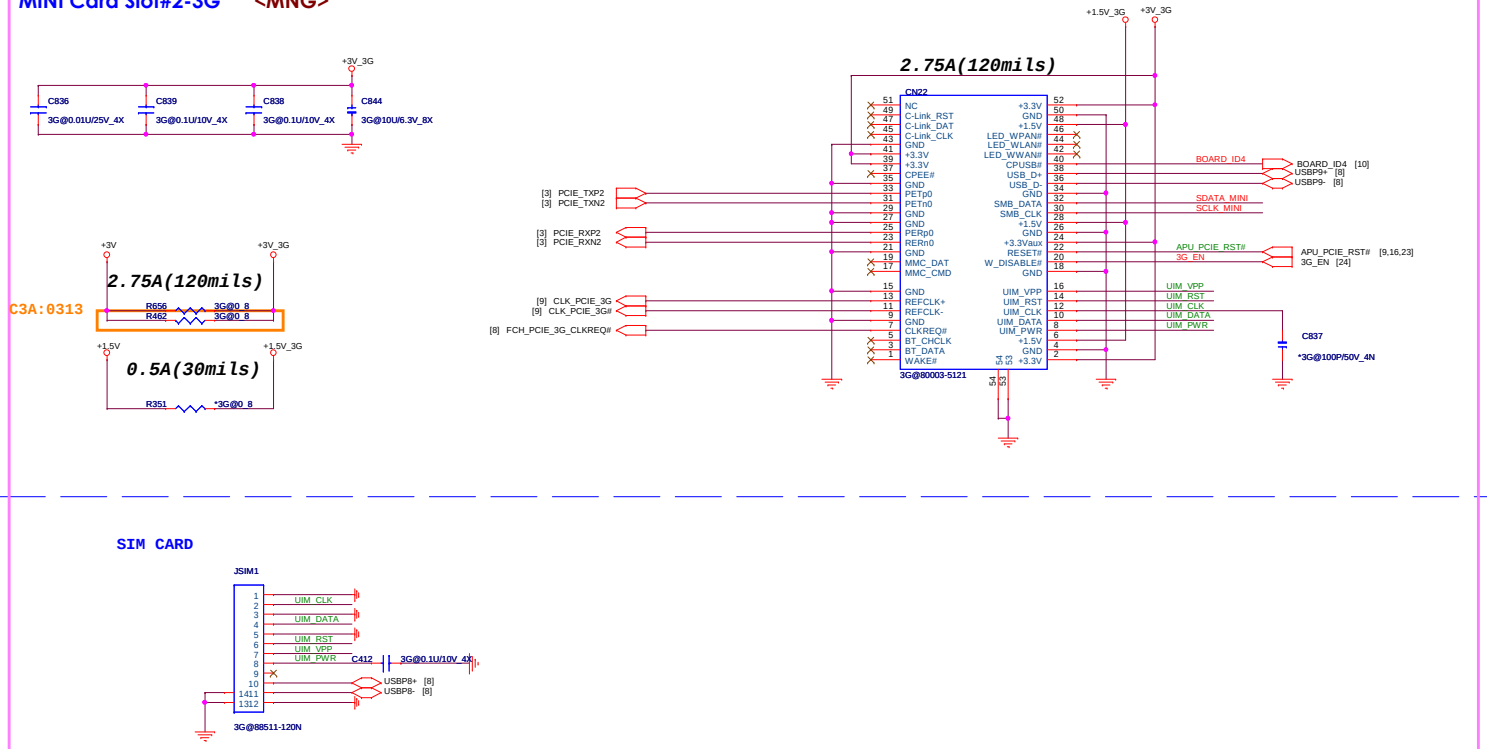
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNG>



SIM CARD

BOM remove E3A ok

Quanta Computer Inc.
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	WLAN/3G/SIM	D3A
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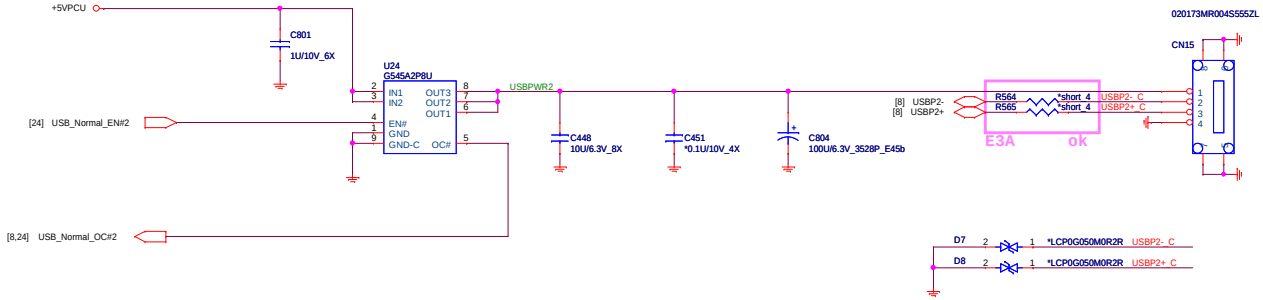
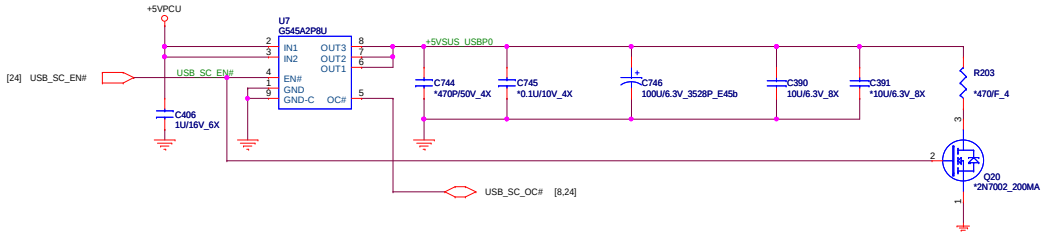
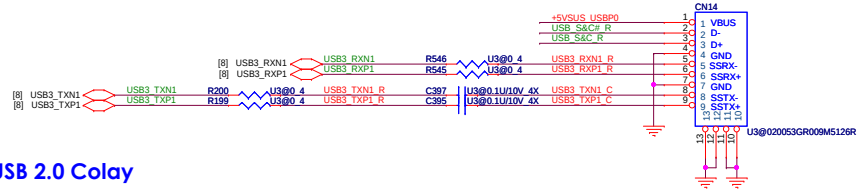
USB2.0 MB SIDE (Left)



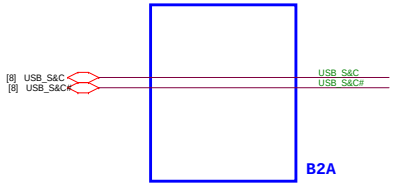
USB 3.0 Power switch <SLC>



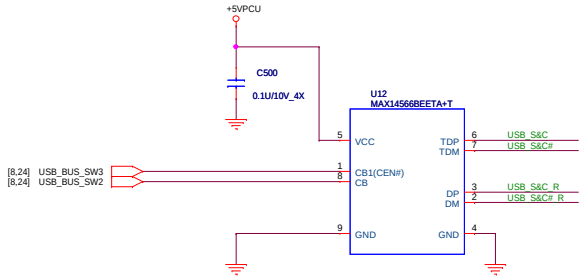
USB 3.0 CONN <U3B>



USB 2.0 Colay



USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

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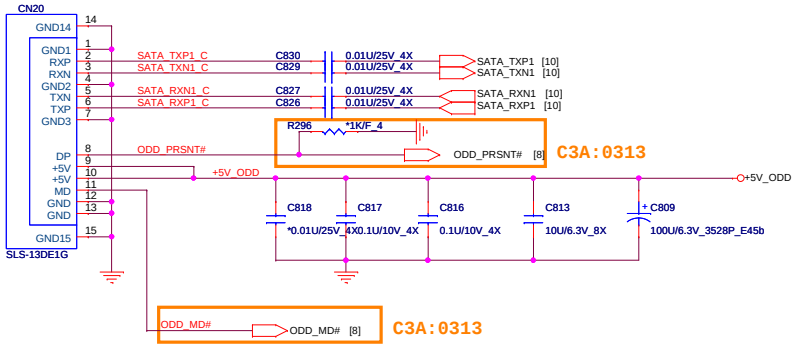
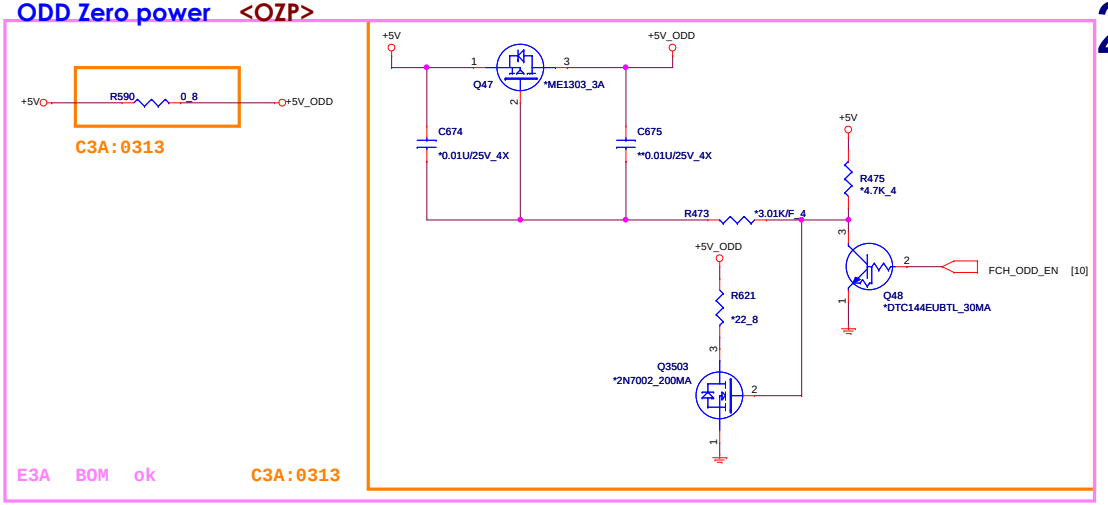
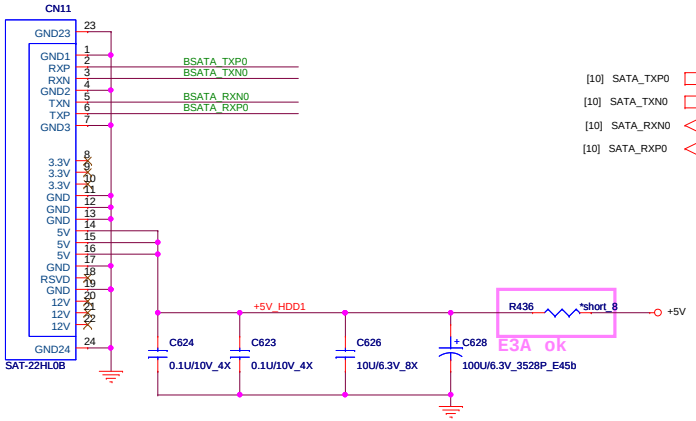
SATA ODD <ODD>



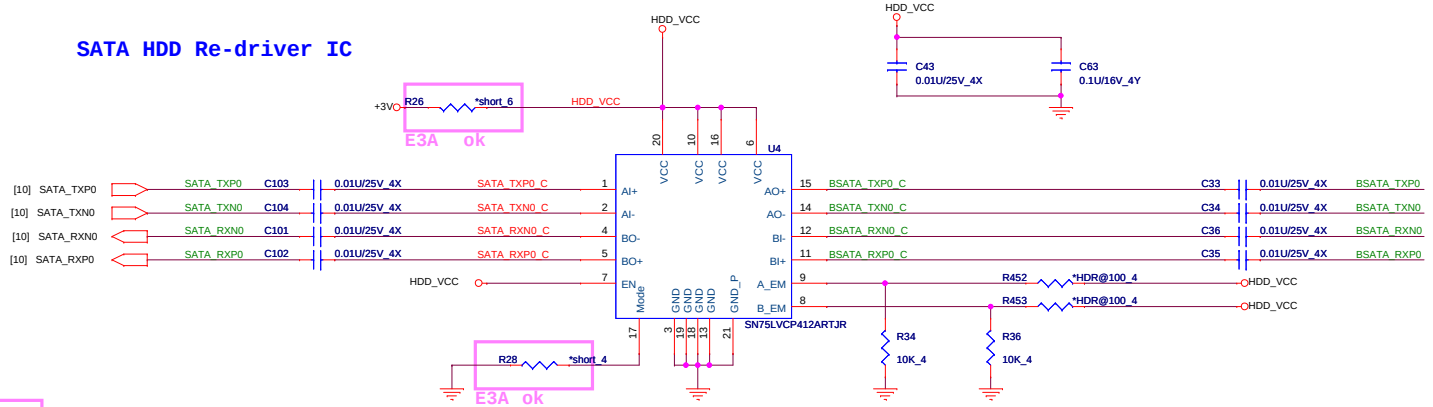
ODD Zero power <OZP>



SATA HDD <HDD>

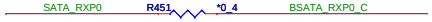


SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC



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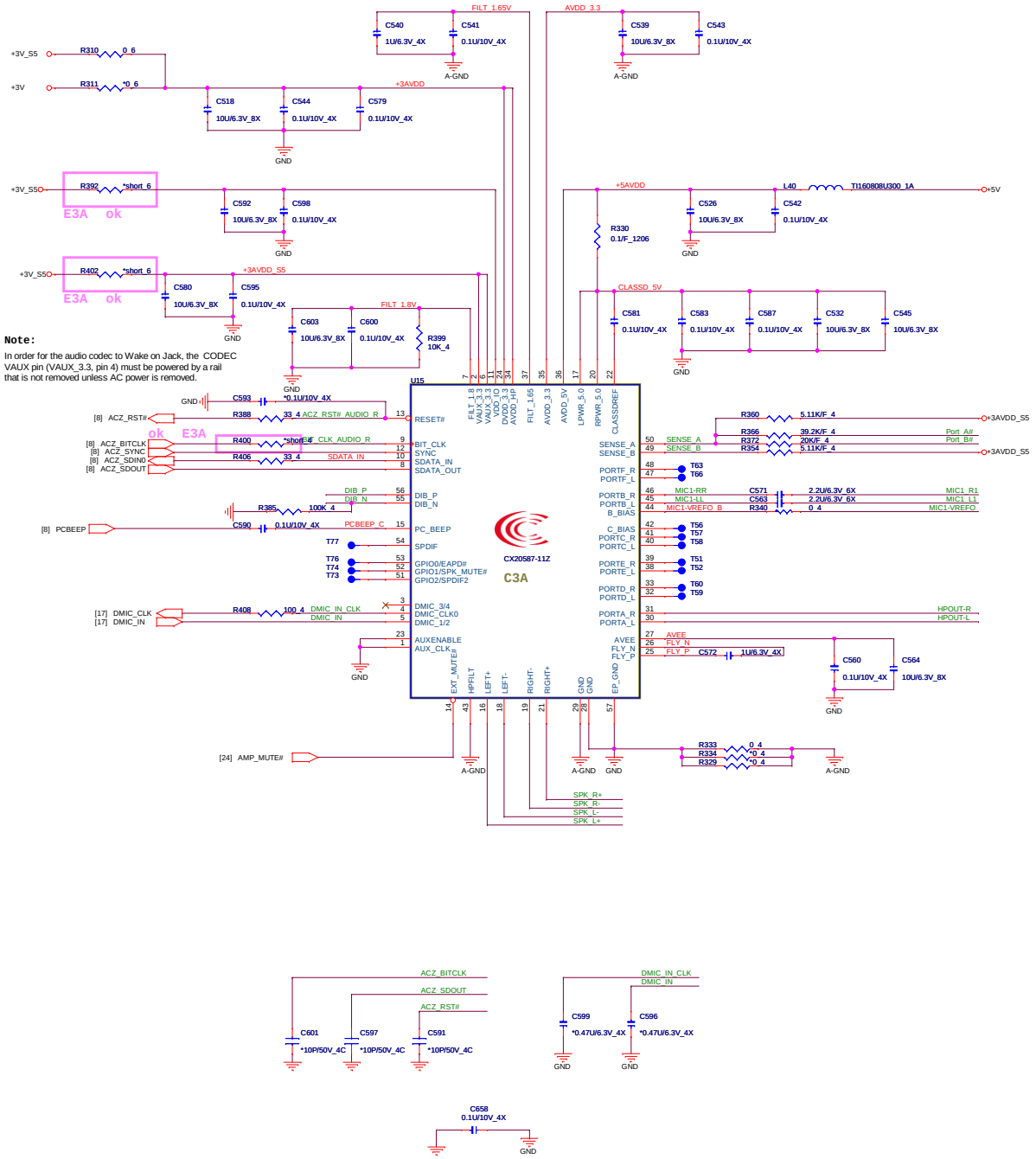
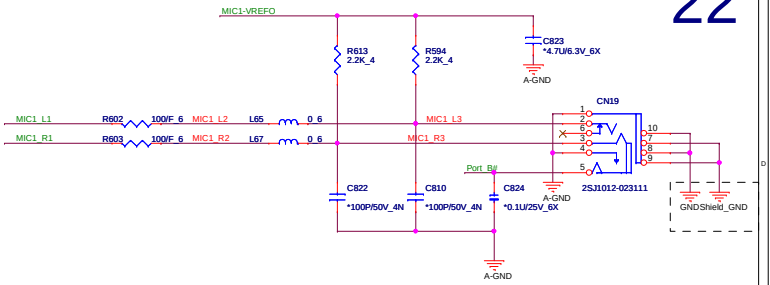
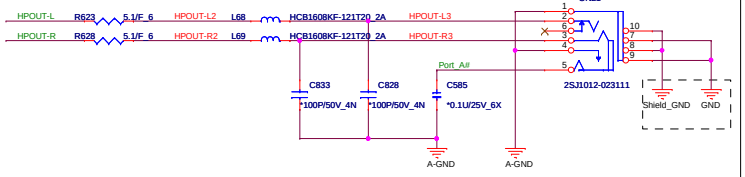
Codec(CX20587-11Z) <ADO/MDC/SLM>



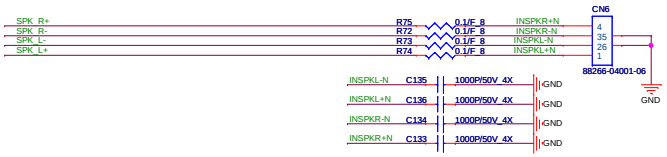
EXT MIC <ADO/SLM>



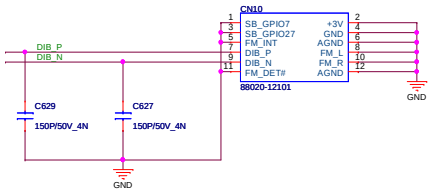
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO>



MDC <MDC>



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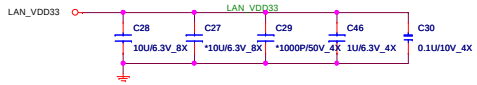
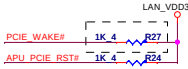
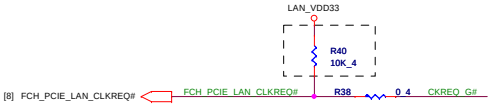
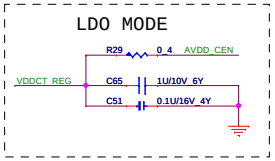
Atheros Lan AR5158 <LAN/LN1>

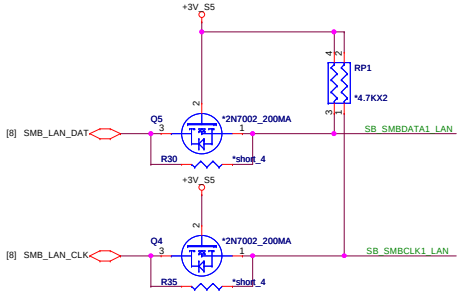
10/100 = 0 ohm CS00002JB38

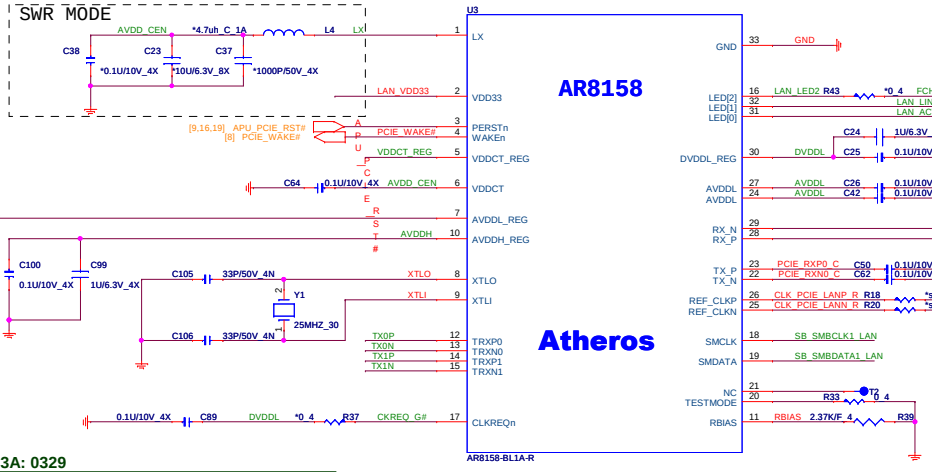




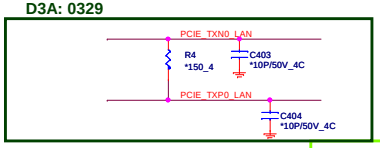






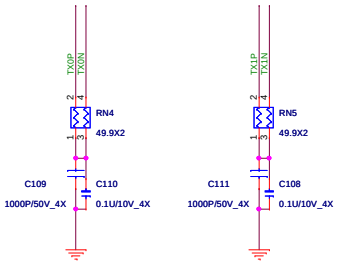


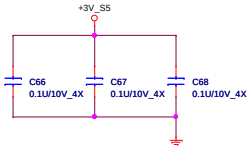
D3A: 0329

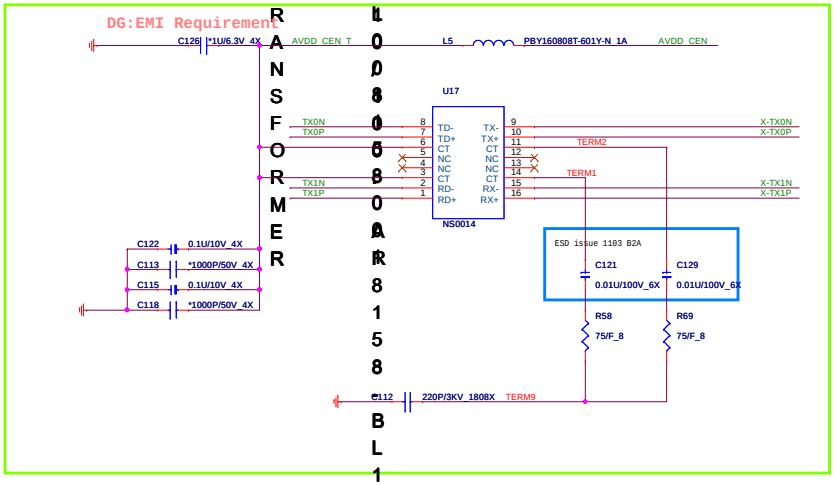


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

PLACE NEAR LAN IC SIDE



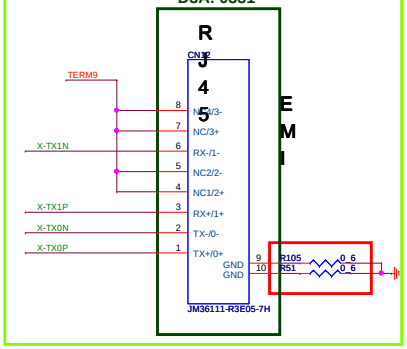




AMDA1008015BL1A-R

TRANSFORMER

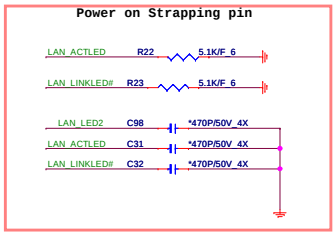
D3A: 0331



EMI

1 RJ45 CONNECTOR

Power on Strapping pin



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EC <KBC>

0.01A(20mils)

0.03A(30mils)

H=1.6mm

D3A: 0328

C3A:0313

CLK 32.768K Hz from PCH

Close to U16

C3A:0317

C3A:0317

C3A:0317

D3A: 0328

D3A: 0328

SKU Strap

MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

SM BUS PU

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap

SHBM

SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID EEPROM

0.003A(20mils)

ADDRESS: A0H

SPI FLASH

0.025A(20mils)

INTERNAL KEYBOARD STRIP SET

HWPG circuit

LED PU/PD

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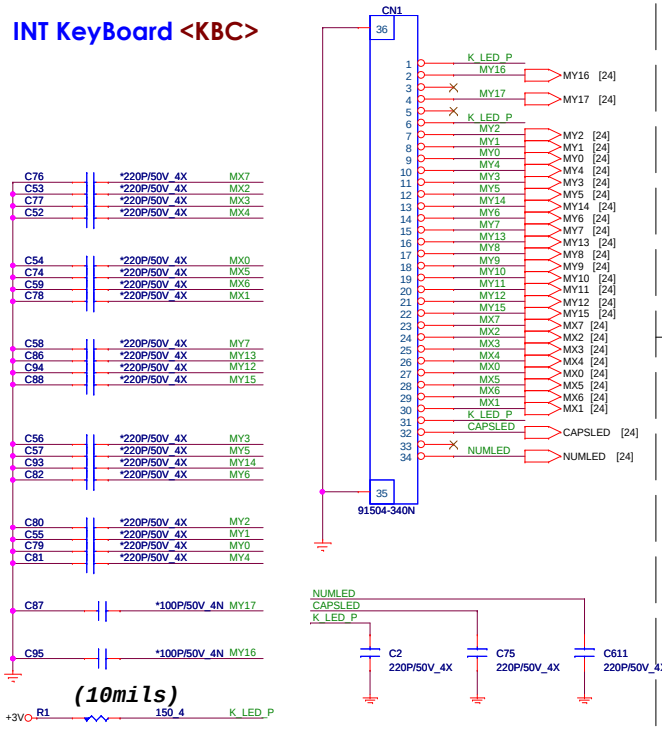
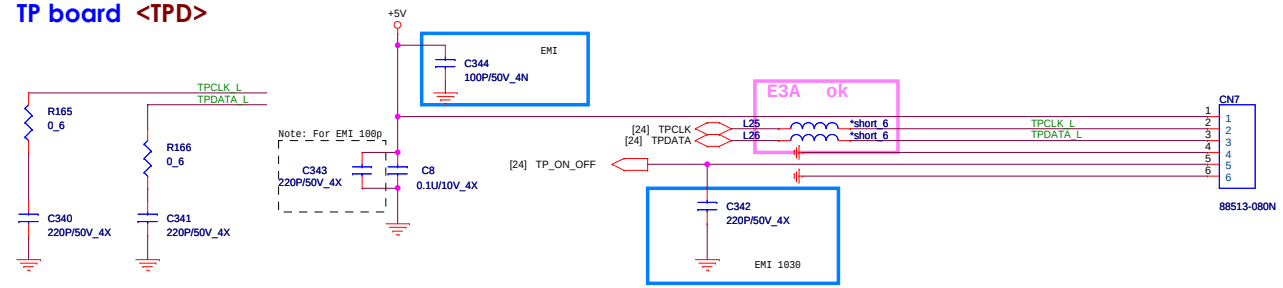
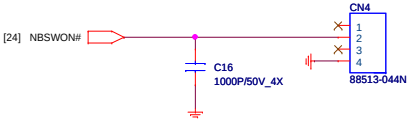
INT KeyBoard <KBC>



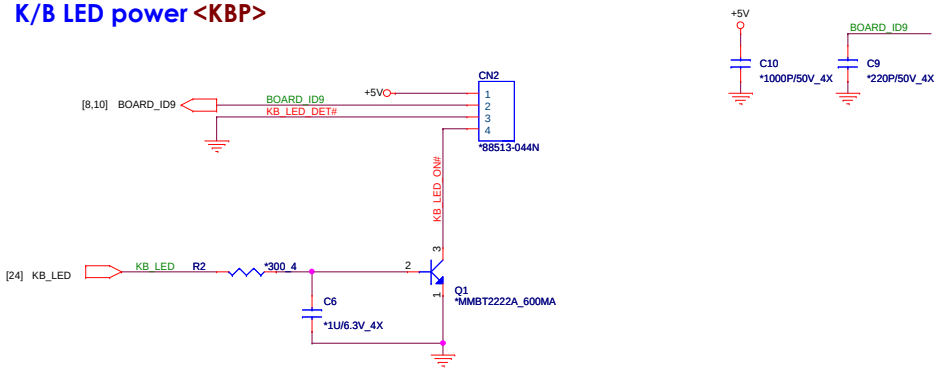
TP board <TPD>



Power board <PSW>



K/B LED power <KBP>



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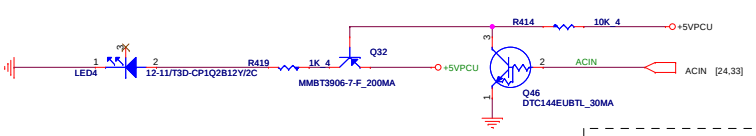
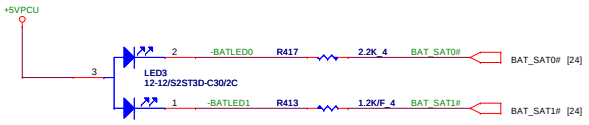
LED <LED>

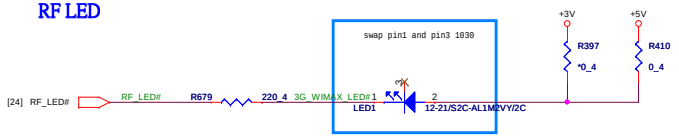
AC-IN



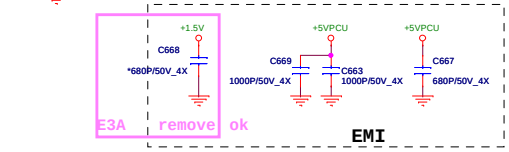
BATERRY



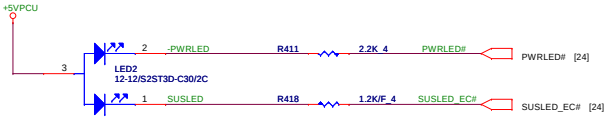
RF LED



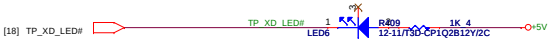
EMI



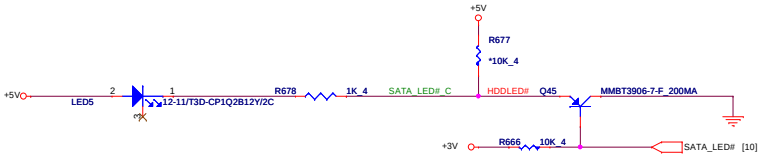
POWER



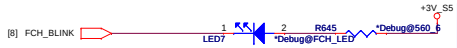
CARDREADER



HDD/ODD

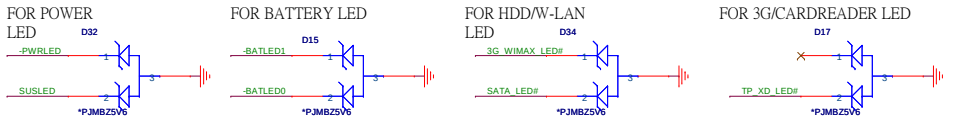


When ON, means in S0
When BLINK, means in S3
When OFF, means in S5

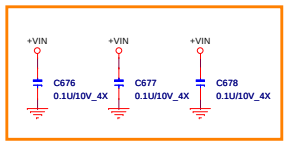


Debug only

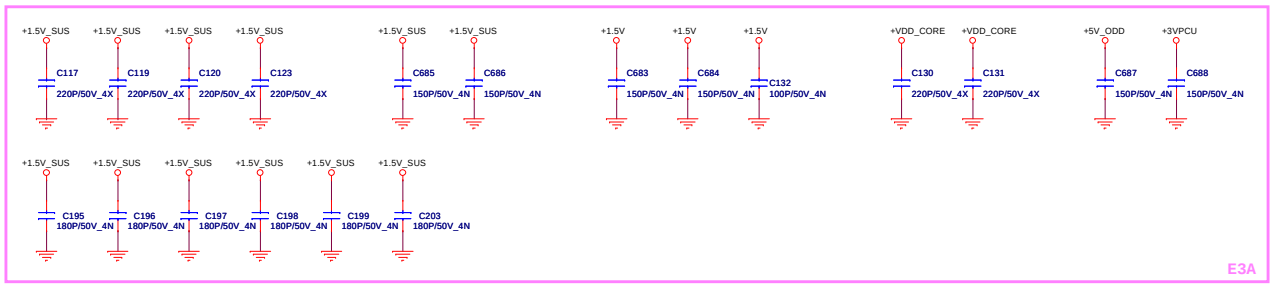
ESD Protect



EMI



C3A: 0314



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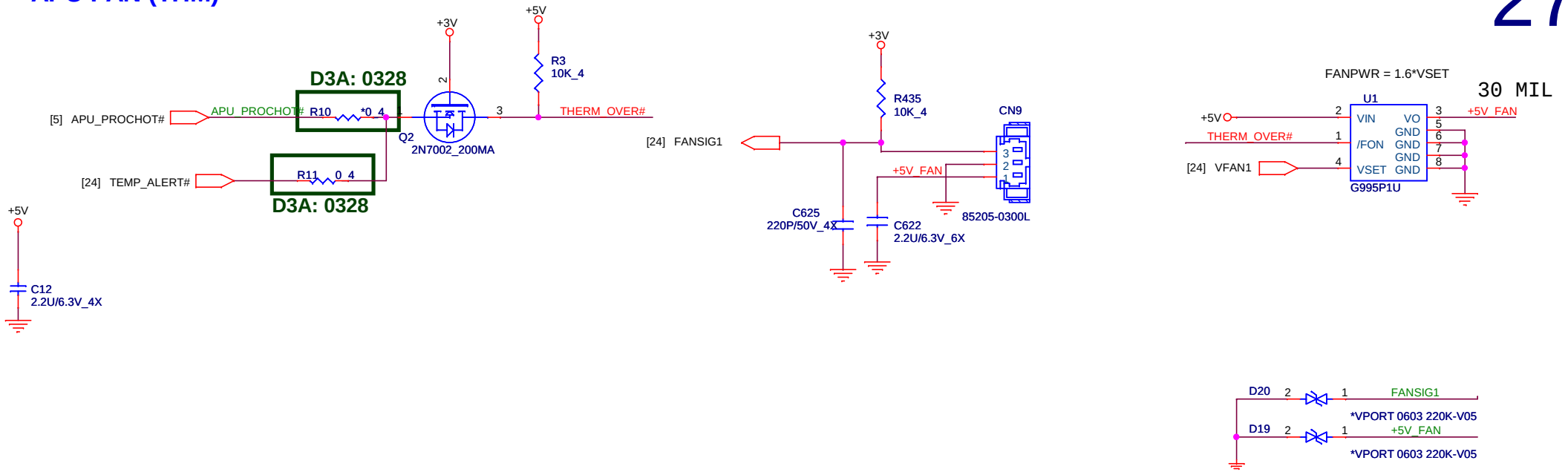
APU FAN (THM)



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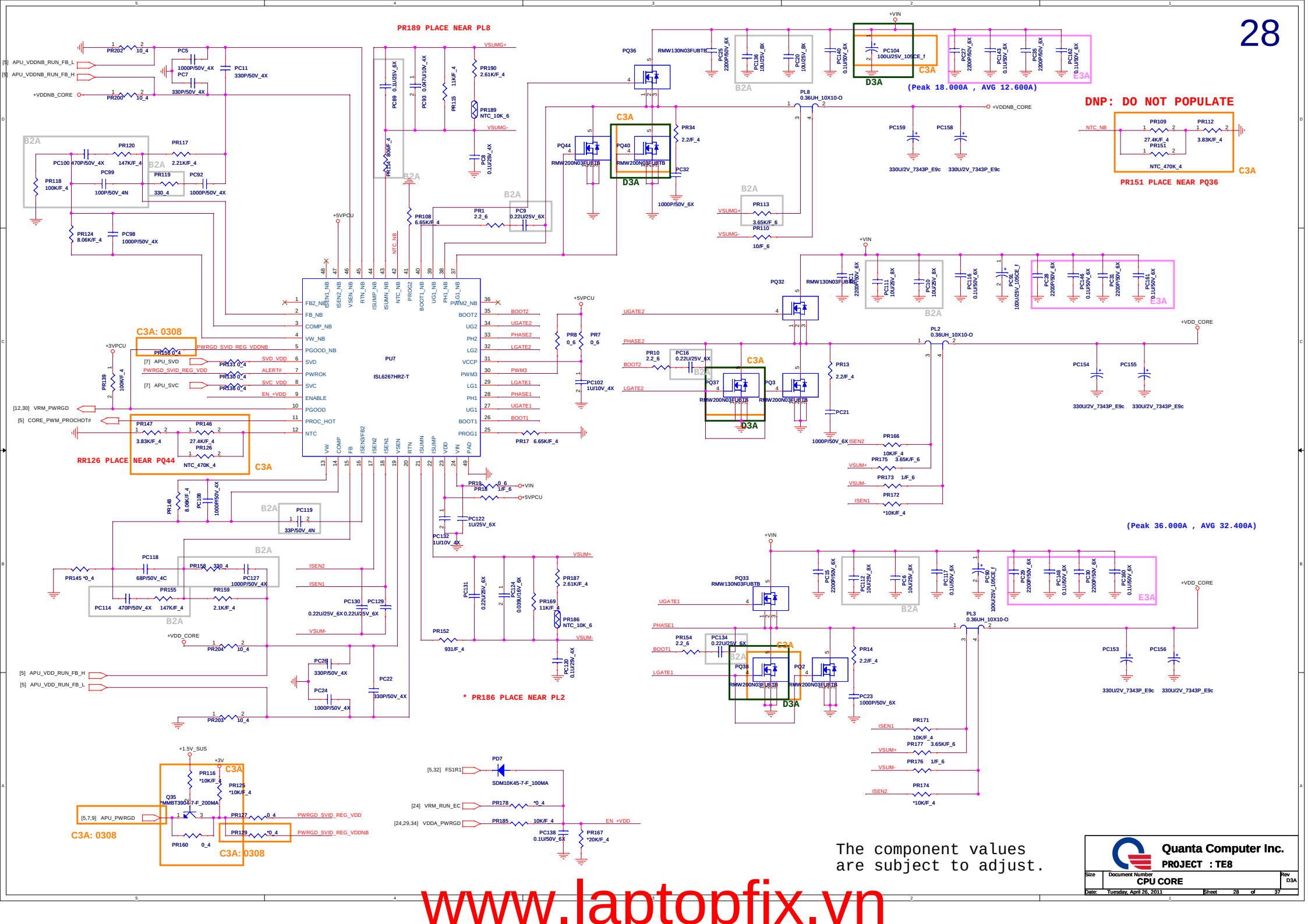

The component values are subject to adjust.

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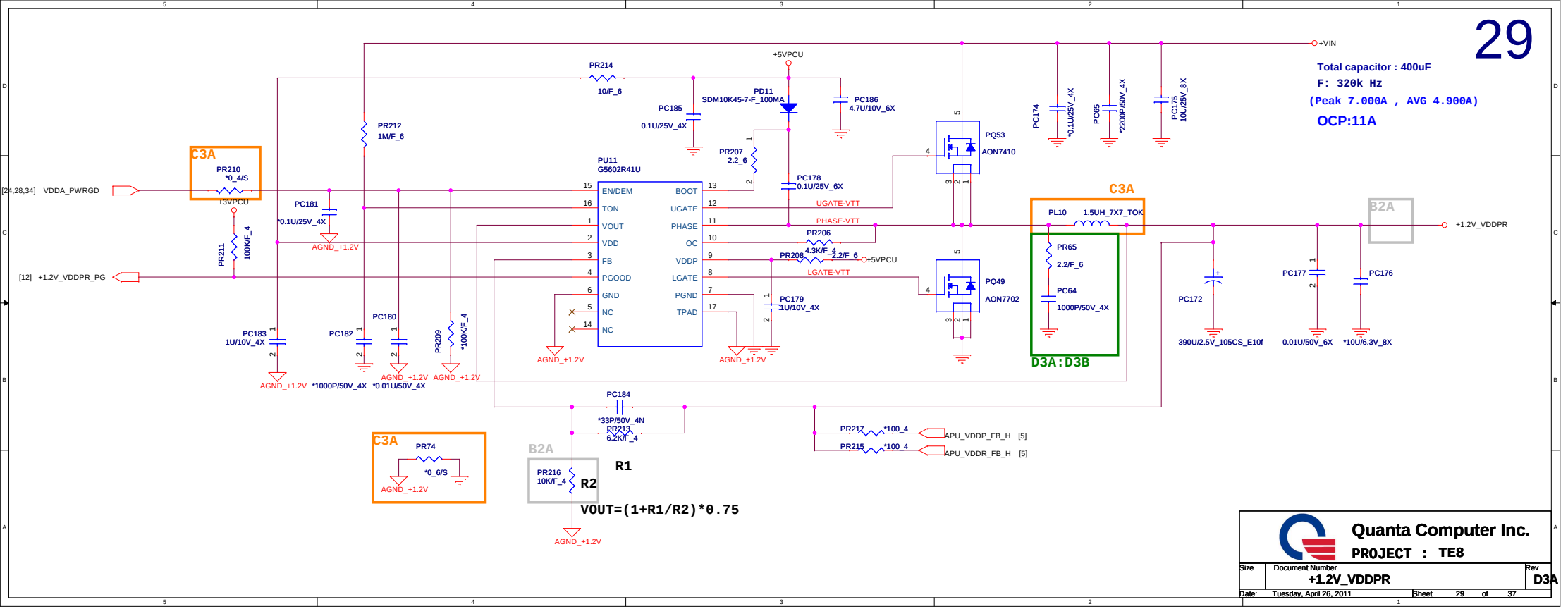

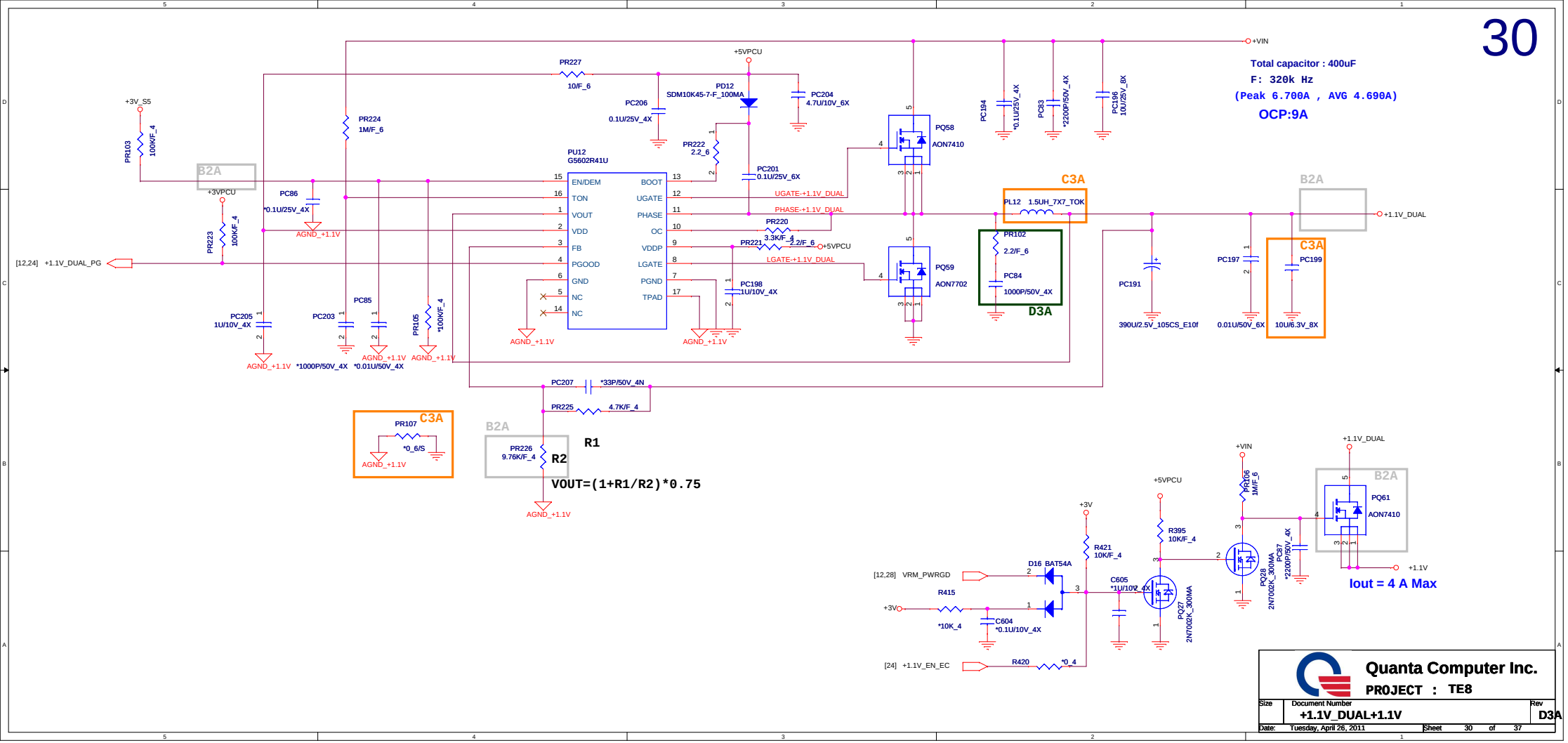

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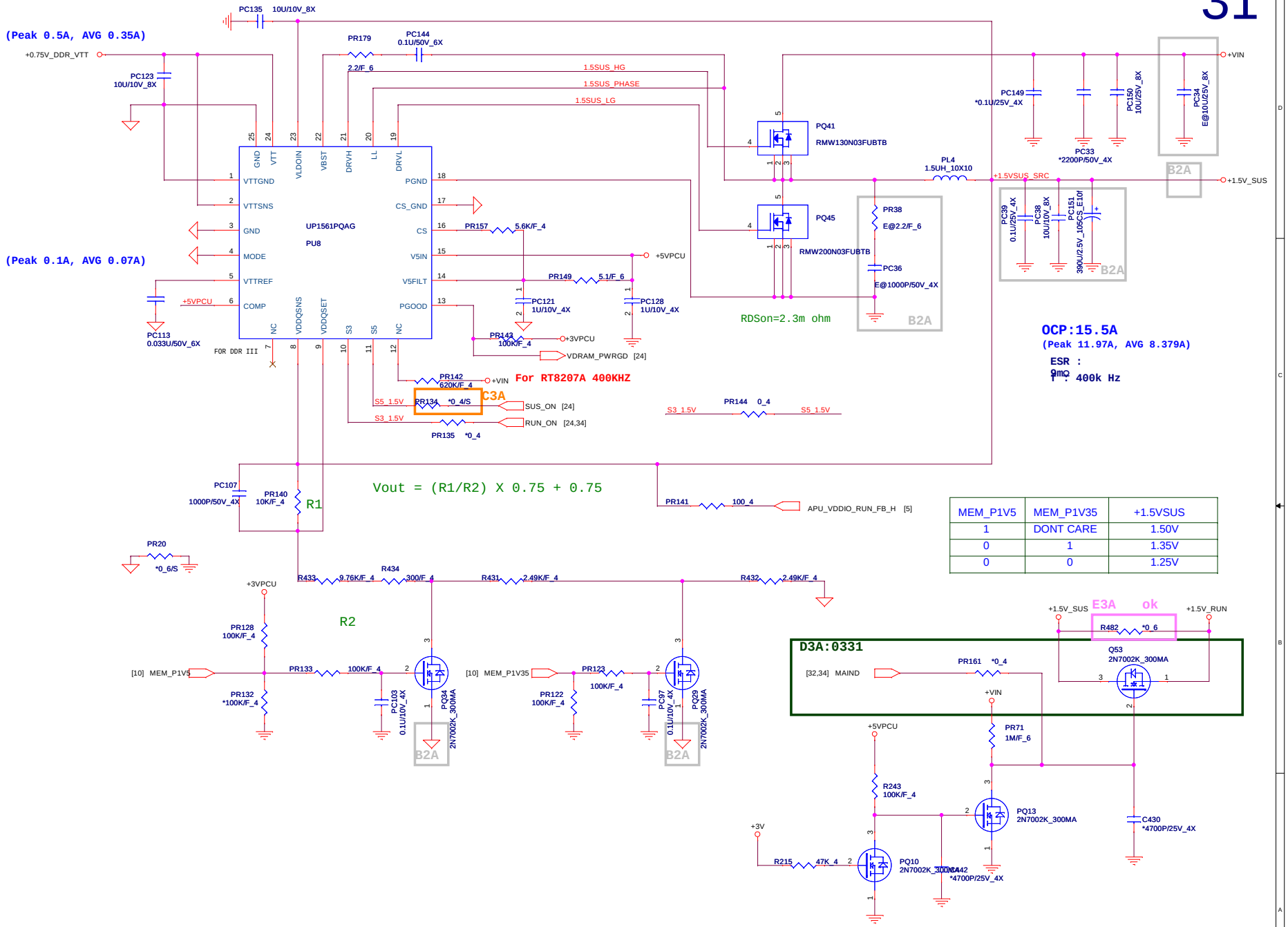

MEM_P1V5	MEM_P1V35	+1.5VSUS
1	DONT CARE	1.50V
0	1	1.35V
0	0	1.25V

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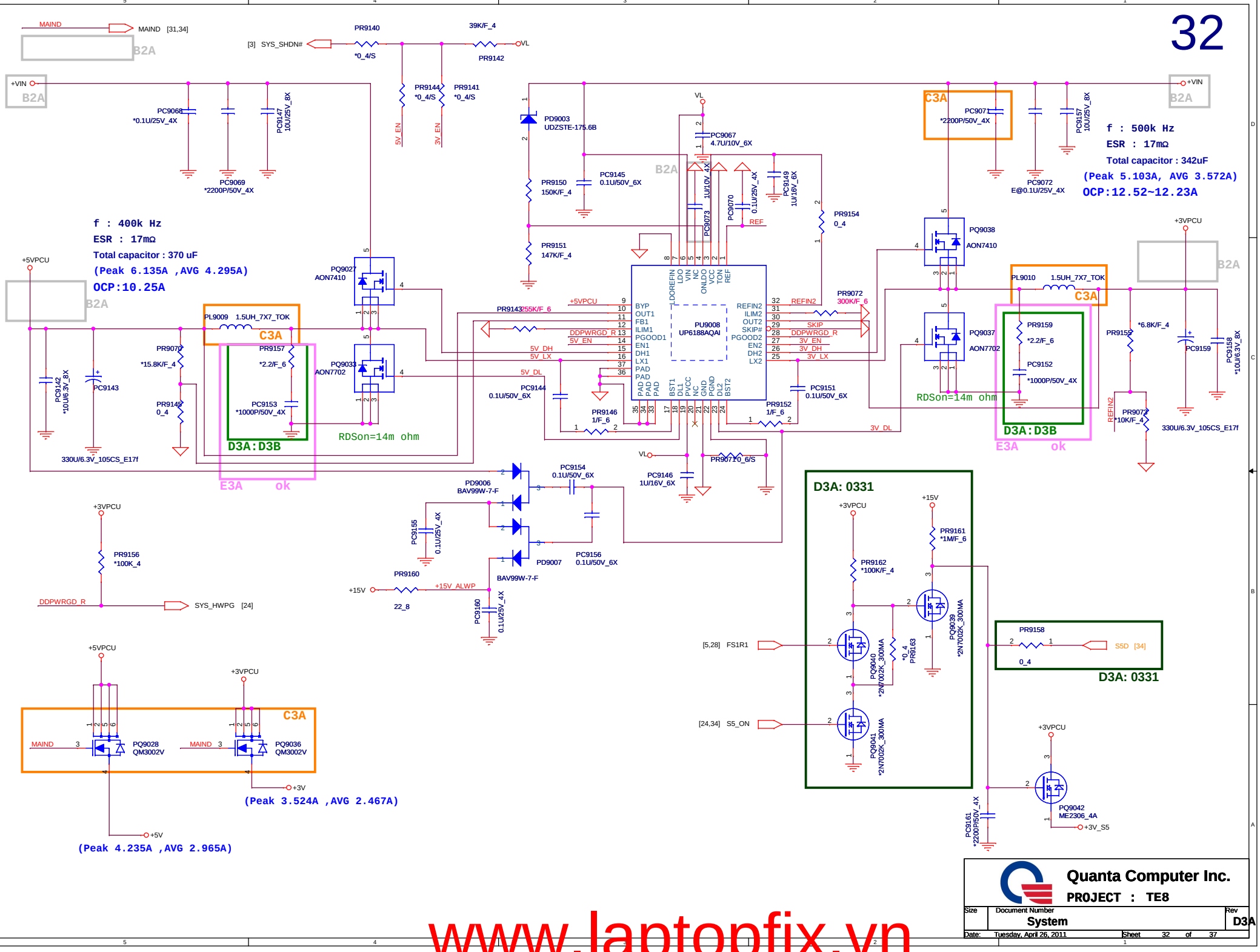

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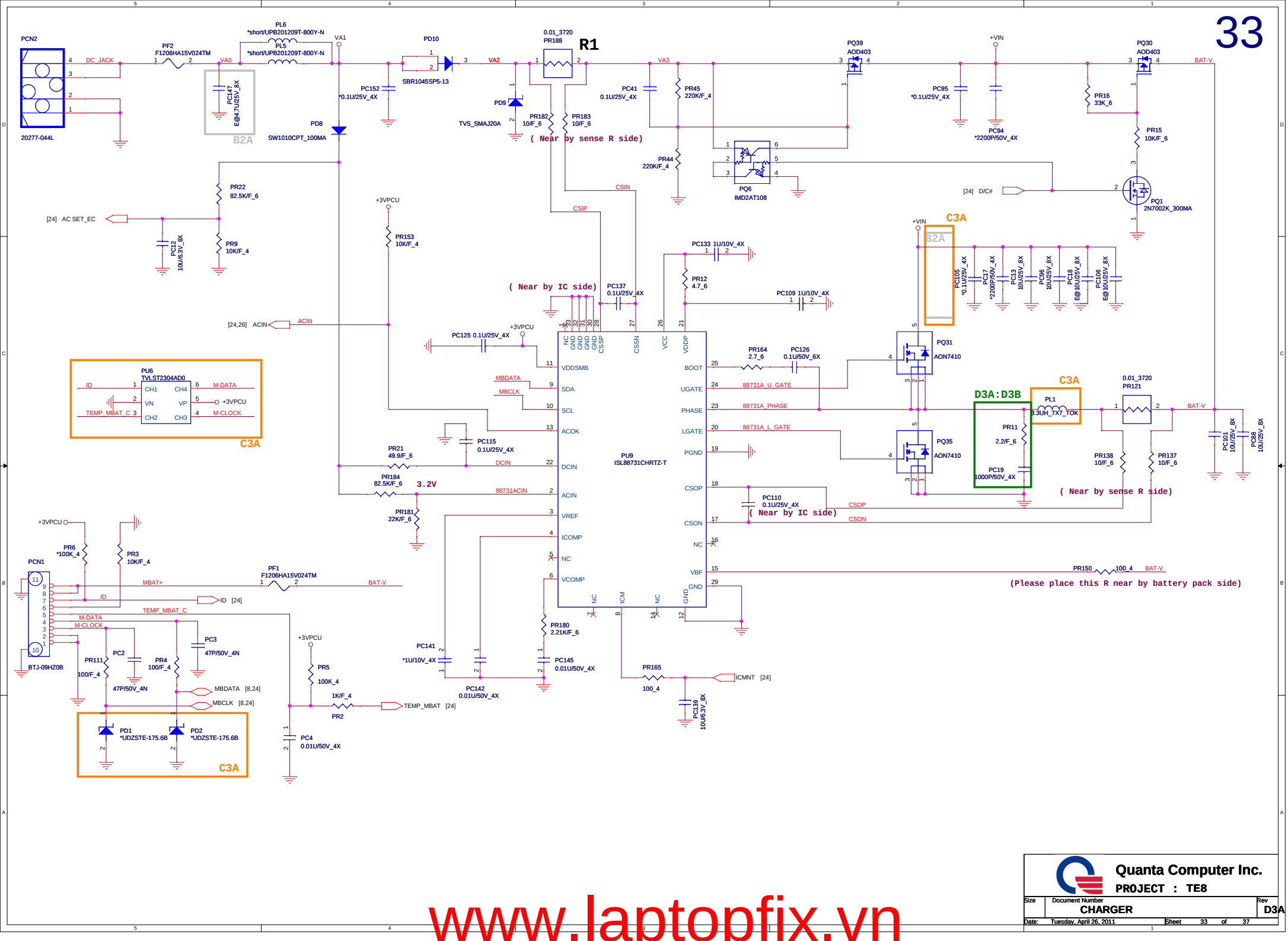
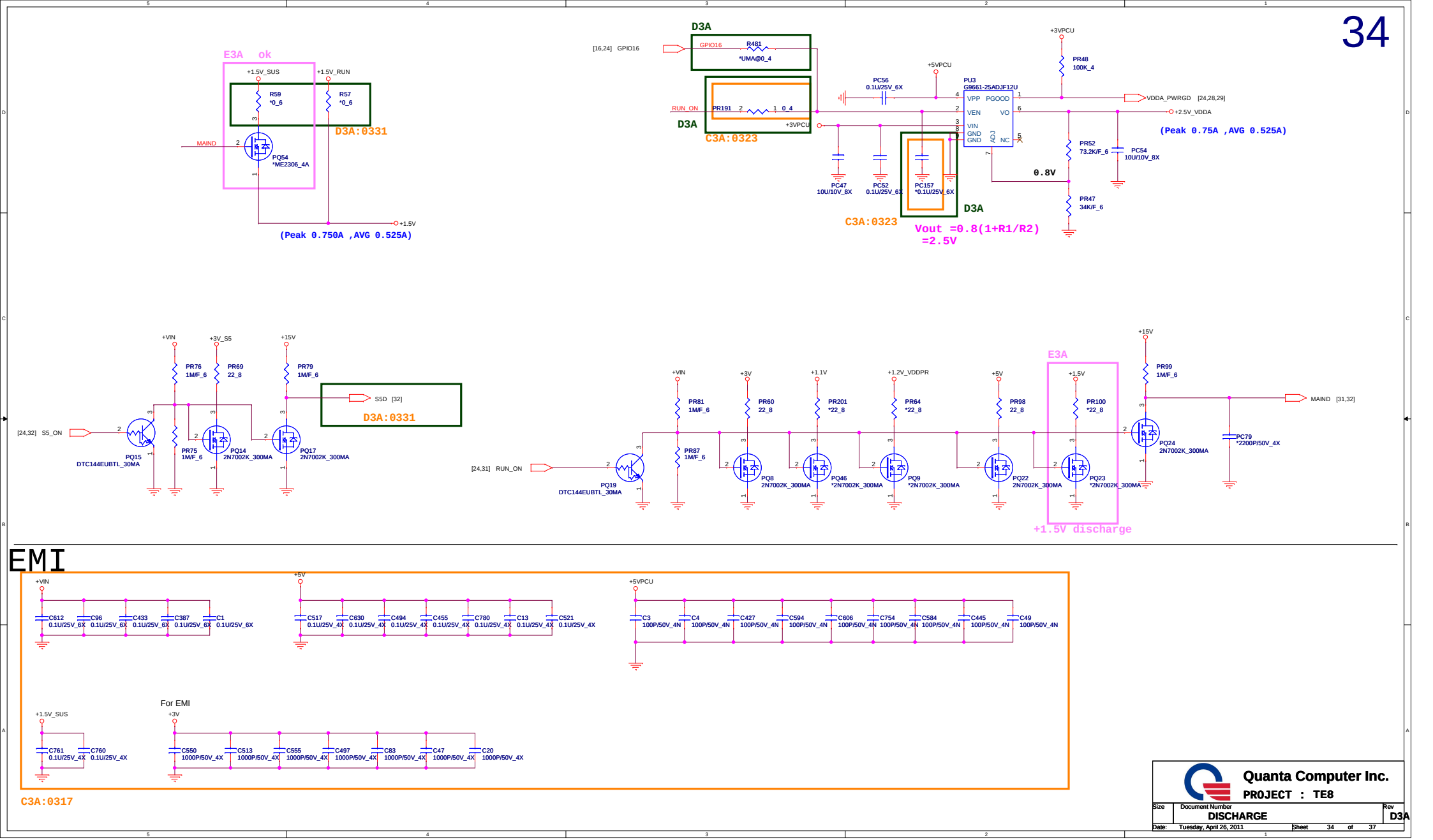
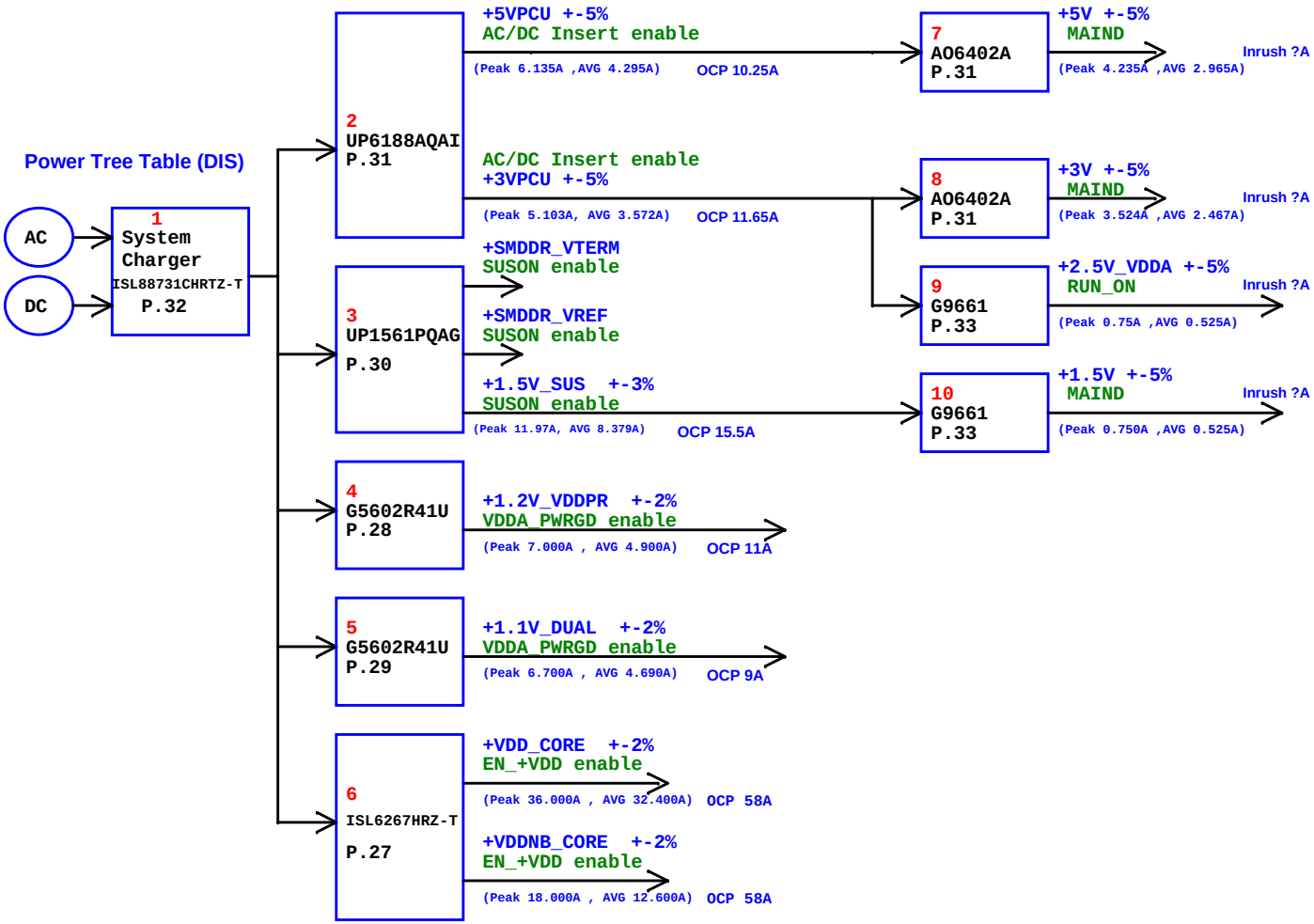




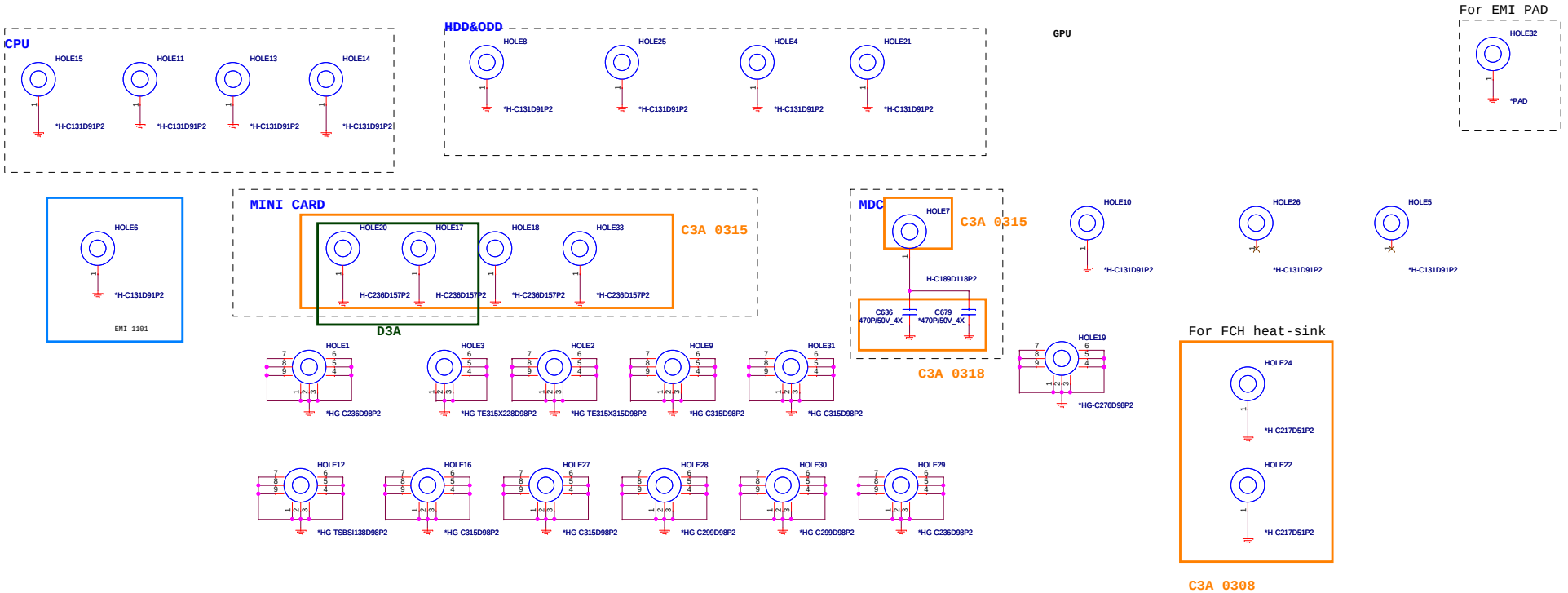
Power Tree Table (DIS)



Power Distribution List

Power	Distribution

HOLE



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	Screw	D3A

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Model	REV	CHANGE LIST	
TE8 MB	B2A	PAGE 10: Change USB DB port from Port2 to Port0 (2011.01.11)	
		PAGE 10: Change USB on board port from Port0 to Port2 (2011.01.11)	
		PAGE 10: Change USB WLAN port from Port3 to Port7 (2011.01.11)	
		PAGE 10: Change USB 3.0/2.0 combo port from Port11 to Port3 (2011.01.11)	
		PAGE 19: De-pop R522 for RAM_CFG0 for RAM setting (2011.01.11)	
		PAGE 23: Add BACO circuit (2011.01.11)	
		PAGE 44: Add PR228 for BACO to control GPU core power (2011.01.11)	
		PAGE 10: Change USB CCD port from Port9 to Port6 (2011.01.14)	
		PAGE 10: Change USB 3G port from Port4 to Port9 (2011.01.14)	
	C2A	PAGE 07: APU_PWRGD ref GND	
		PAGE 21: Add ODD Zero Power Ckt	
		PAGE 24: Protect EC DISPON_O change R125 to 2.2 OHM	
		PAGE 19: add R317, R656 for MINI CARD +3V	

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Change List
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