Compal Confidential

M/B Schematics Document

AMD Kaveri(FP3) + Bolton(M3)

AMD TOPAZ S3

2014-05-07
REV : 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title: Cover Page
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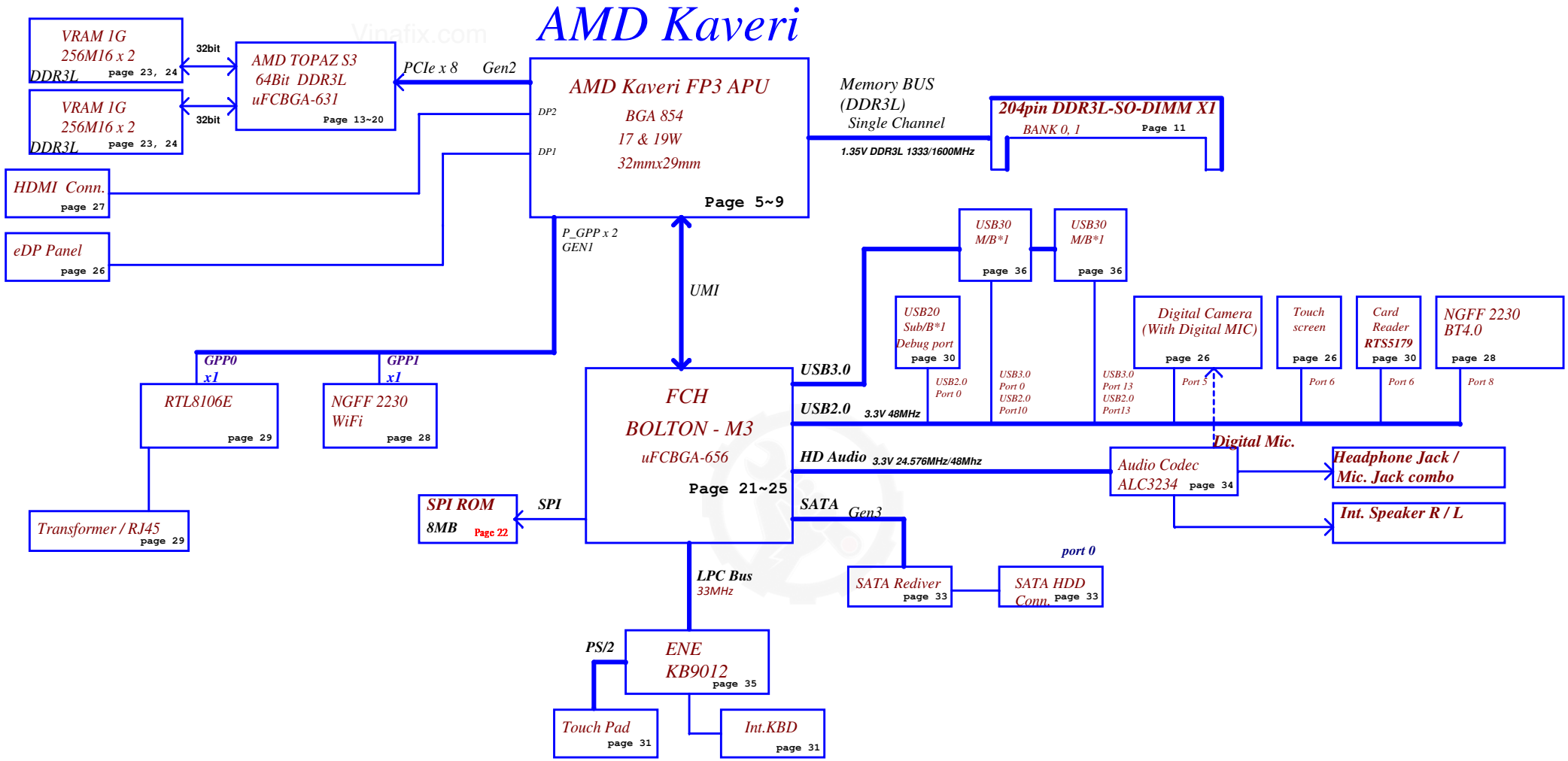
				Date: Friday, May 23, 2014 / Sheet 1 of 50



LED page 30

RTC CKT. page 21 ~ 40

Power On/Off CKT. page 31

Fan Control page 31

DC/DC Interface CKT. page 37

Power Circuit page 40~50

Sub board

LID SW - Power/B page 32

D/B
-USB20 x1
-Card Reader
SD/MMC 2 IN 1
page 30

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Title: Block Diagrams

Size: Custom | Document Number | Rev: 0.1

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Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+VDDCI	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+VGA_PCIE	0.95V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05VS switched power rail for APU	ON	OFF	OFF	OFF
+1.35V	1.35V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF	OFF
+3VGS	3.3V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VS	1.8V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3VALW	3.3V power rail for FCH	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN_NGFF	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

DAX

PCB
Part Number = DA80010O010
<Part Description>

PCBR1@

DAX

PCB
Part Number = DA80010O011
<Part Description>

PCBR3@

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64

BOARD ID Table

Board ID	UMA	DIS(Topaz)
0	SSI	
1		SSI
2	PT	
3		PT
4	ST	
5		ST
6	1.0	
7		1.0

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger IC	0001 001X b	09H

EC SM Bus2 address

Device	Address	HEX
Fintek thermal sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
MINI CARD		

FCH SM Bus 1 address

Device	Address	HEX

BOM Option Table

BOM Structure	Description	UMA 43XX	OPAL 43XX	JET 43XX
9022@	Use EC 9022			
9012@	Use EC 9012	V	V	
UMA@	Display output from APU (UMA only)	V	V	
VGA@	Use VGA (PX or DIS only)		V	
EDP@	Use eDP Panel		V	
AL@	Use Auto load EC code function			
AC@	Support AC Function			
NOAC@	No Support AC Function			
		V	V	
CONN@	Connector (Control by ME)	V	V	
HDT@	Debug Connector			
EMC@	EMC Component			
XEMC@	Reservec for EMC			
X76@	VRAM ID Table (Load By X76J)			
128@	VRAM x 8pcs			
OPAL@	ATI OPAL VGA CONTROLLER			
JET@	ATI JET VGA CONTROLLER			
BL@	ATI JET VGA CONTROLLER			
@	Unpop			
TS@	Touch Screen			
NEMI@	Unpop EMI			
NESD@	Unpop ESD			
AOAC@	AOAC Function			
NAOAC@	Non AOAC Function			

BOM Config

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Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	ZAMB0	0.1

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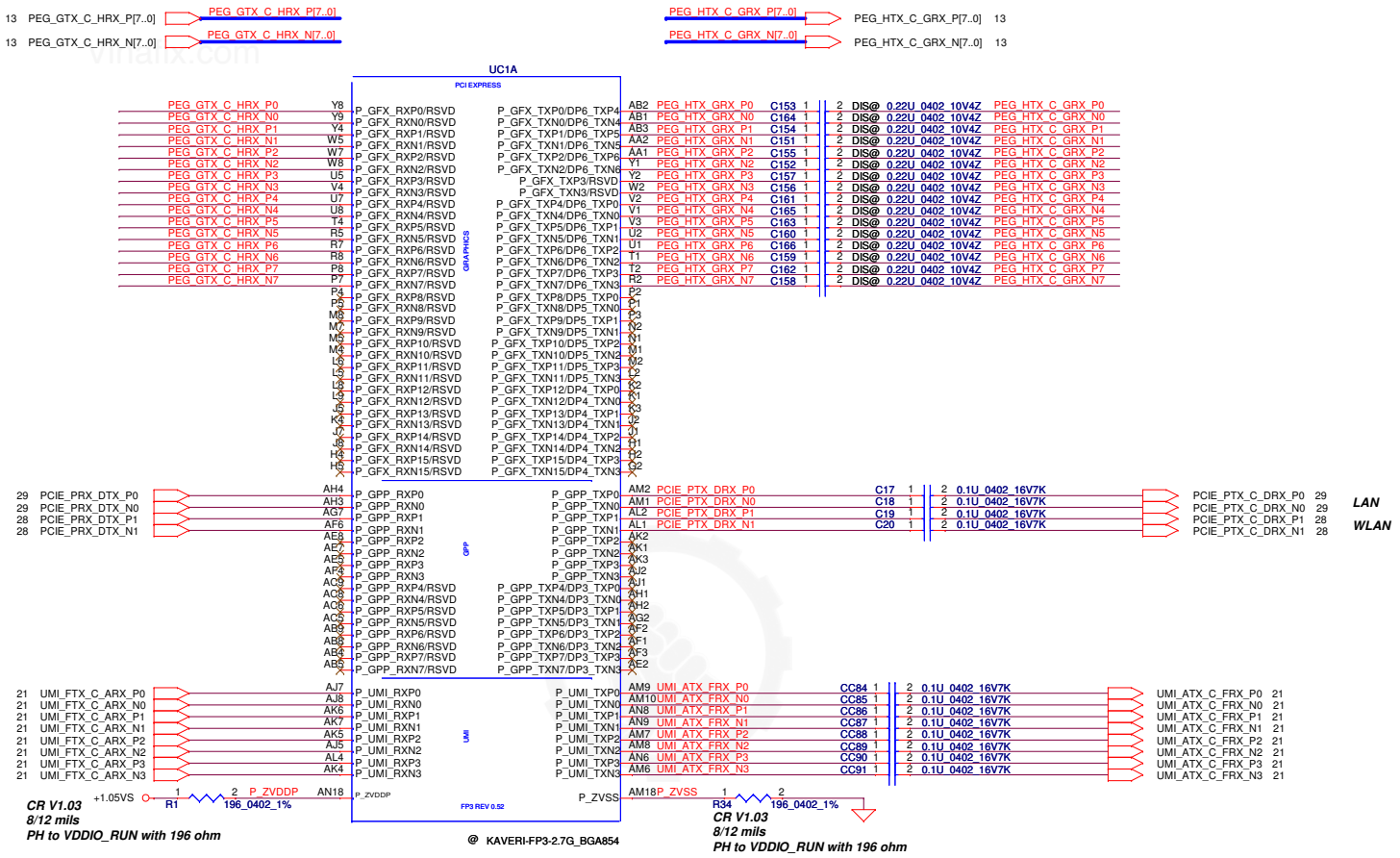

UC1 A8R1@

A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

SA00007S20L

UC1 A10R1@

A10-7300 AM7300ECH44JA 2G BGA 854P APU

SA00007S30L

UC1 FXR1@

FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

SA00007TT0L

UC1 A8R3@

A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

SA00007S21L

UC1 A10R3@

A10-7300 AM7300ECH44JA 2G BGA 854P APU

SA00007S31L

UC1 FXR3@

FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

SA00007TT1L

AMD, FX-7500, KAVERI, PR	SA00007TT0L	S IC FX-7500 FM7500ECH44JA 2.1G BGA 854P APU
AMD,A10-7300, KAVERI, PR	SA00007S30L	S IC A10-7300 AM7300ECH44JA 2G BGA 854P APU
AMD A8-7100, KAVERI, PR	SA00007S20L	S IC A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

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Title: FP3 PCIE/UMI

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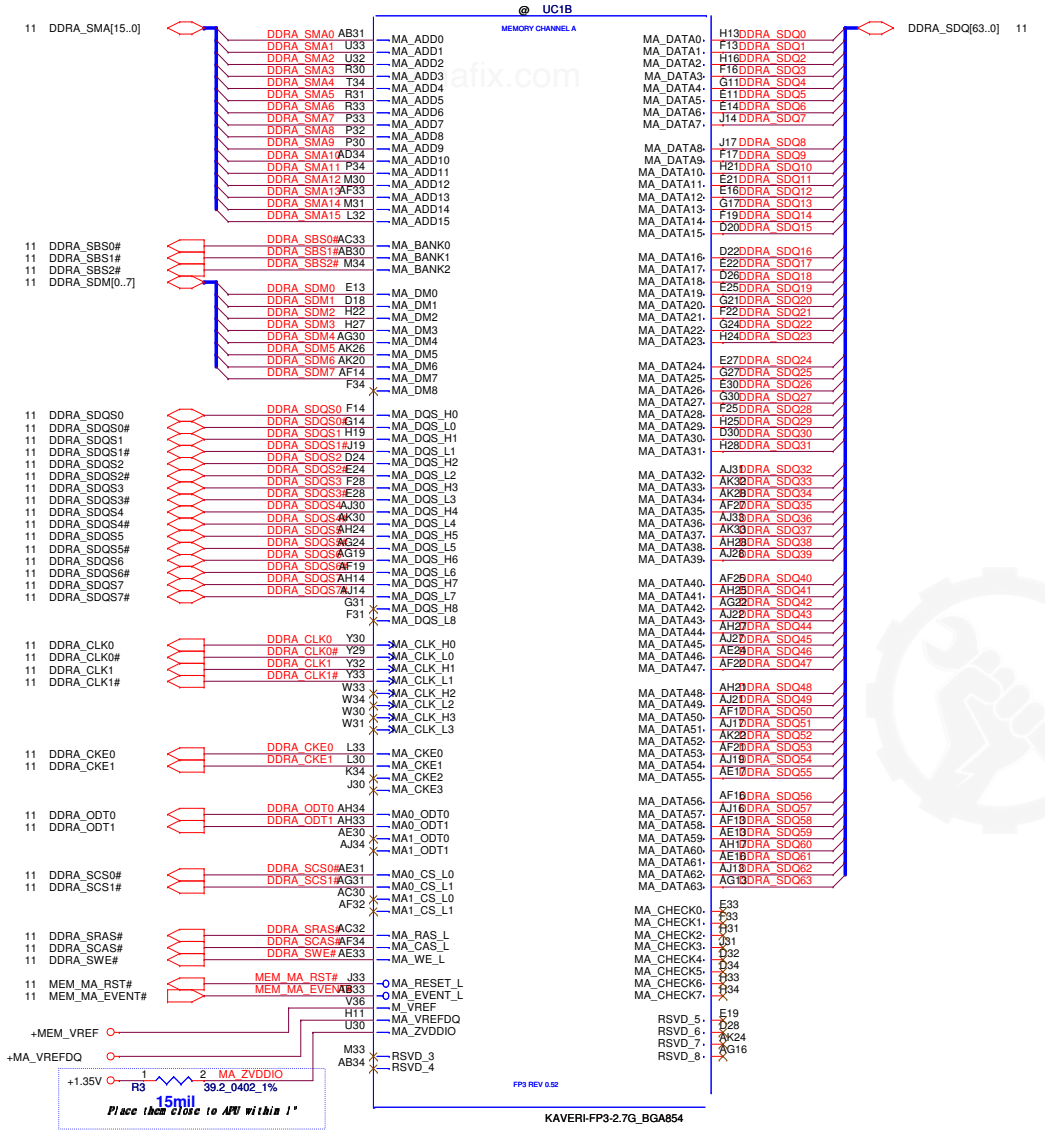
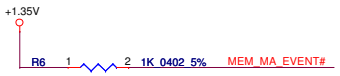
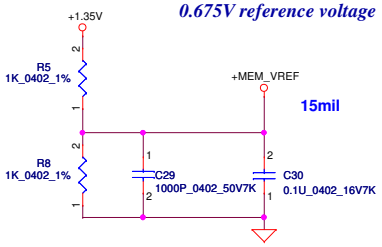


M_VREF (APU)	A	Pull-up resistor to VDDIO	1 kΩ (± 1%)	–	VDDIO
		Pull-down resistor to VSS	1 kΩ (± 1%)	–	VSS
		Decoupling capacitor	0.1 µF	–	VSS
		Decoupling capacitor	1 nF	–	VSS

EVENT# pull high



0.675V reference voltage



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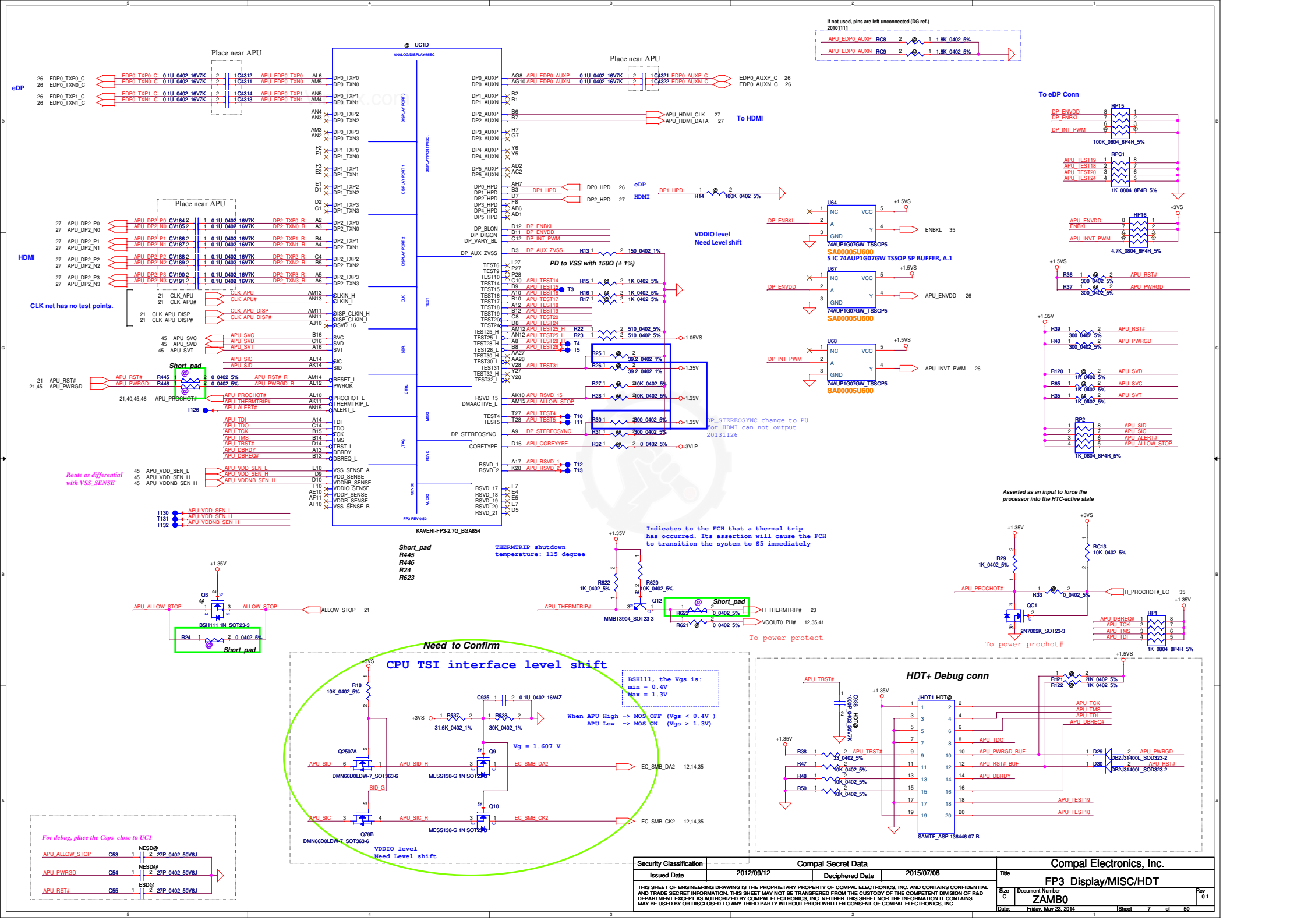

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Compal Electronics, Inc.

Title: FP3 Display/MISC/HDT

Size	Document Number	Rev
C	ZAMB0	0.1

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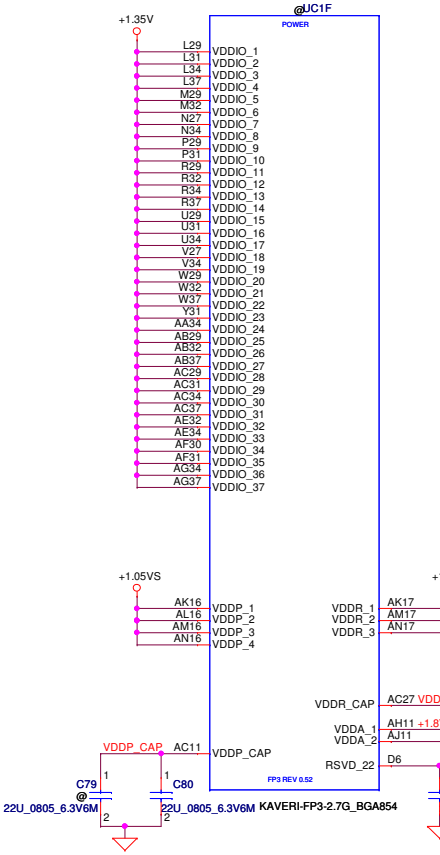
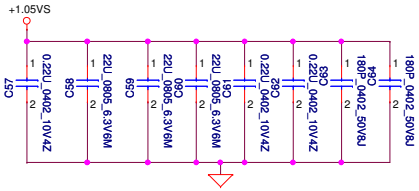
Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.35V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A

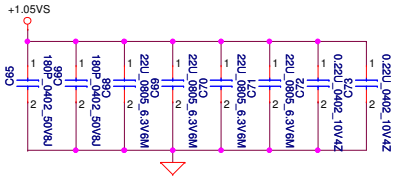
+APU_CORE_NB Decoupling Power Side
22uF x10 @ x2
0.22uF x3
180pF x4

Check list CH47
+APU_CORE Decoupling Power Side
22uF x11 @ x2
0.22uF x2
0.01uF x3
180pF x3

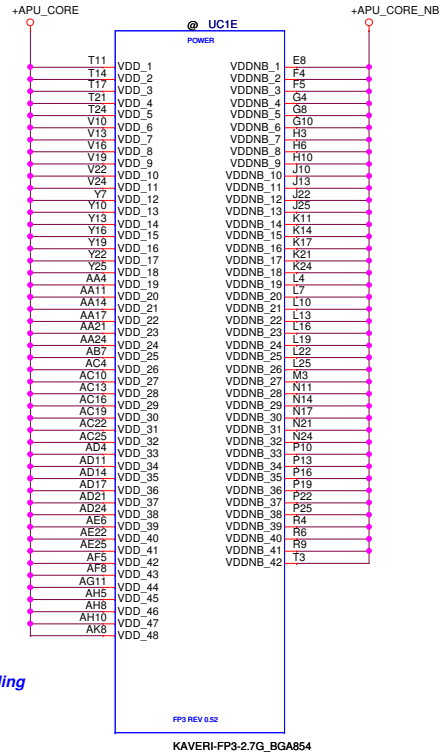




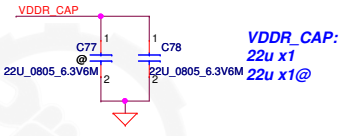
VDDP:
22u x3
0.22u x2
180P x2



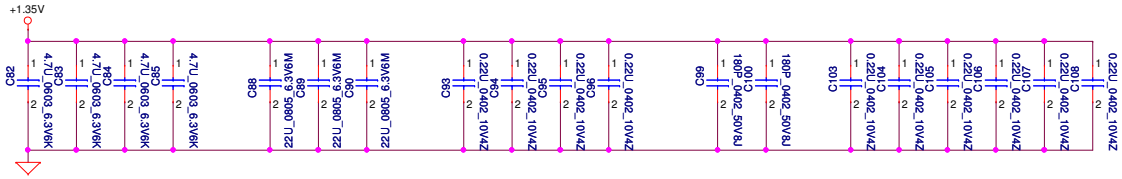
VDDR:
22u x4
0.22u x2
180P x2



VDDA:
4.7u x1
0.22u x1
3.3n x1

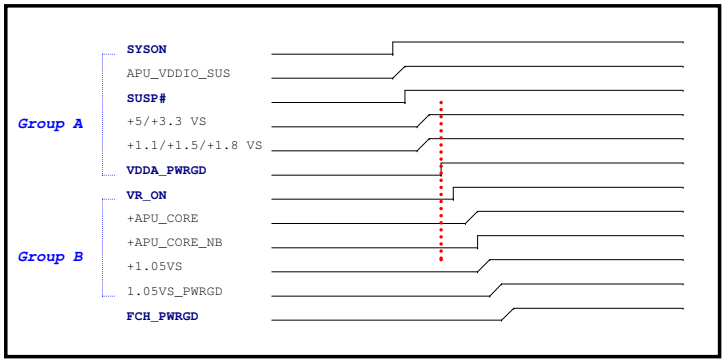


VDDR_CAP:
22u x1
22u x1@



VDDIO Decoupling
22uF x3
4.7uFx4
0.22uF x6
0.22uF x4 (return path)
180pF x2 (return path)

APU sequence : GROUP A need ramp before GROUP B



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Title: FP3 Power

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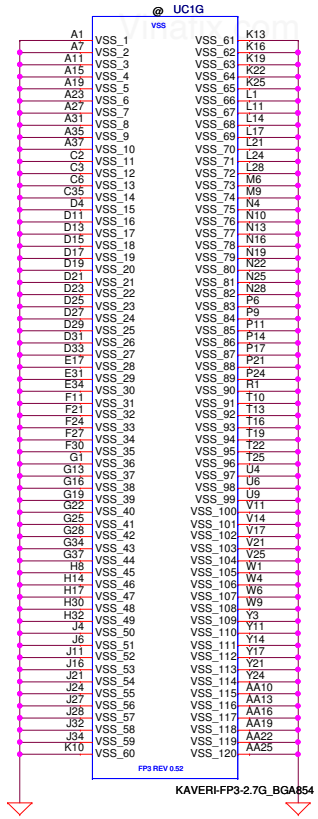

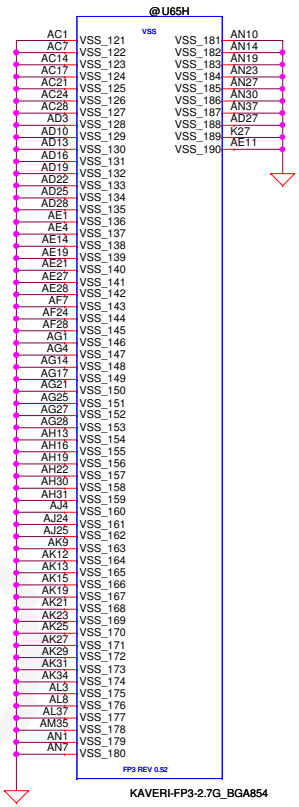

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Title: FP3 GND

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Title: AMD FS1R2 Singal Level Shifter

Size	Document Number	Rev
Custom	ZAMB0	0.1

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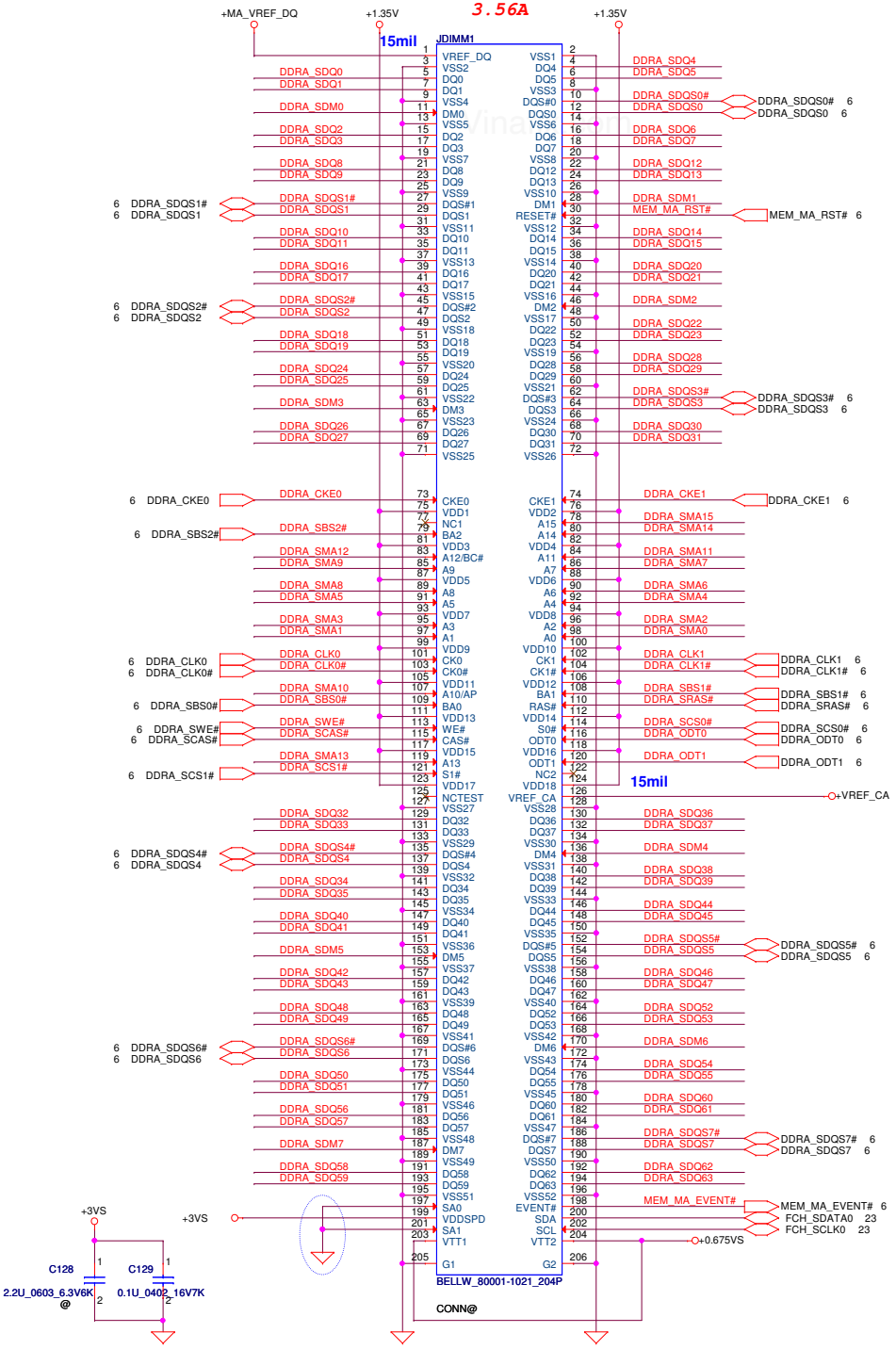
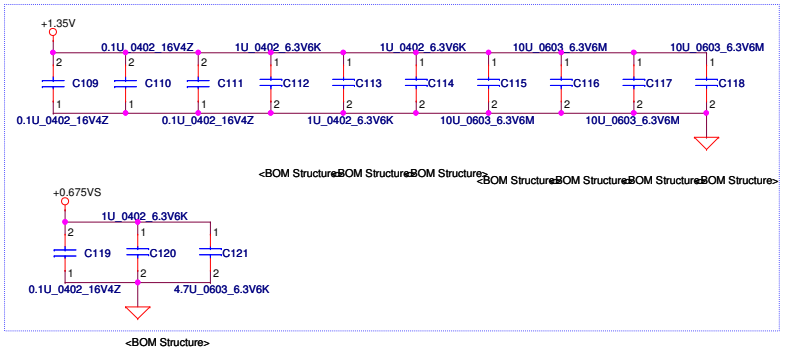
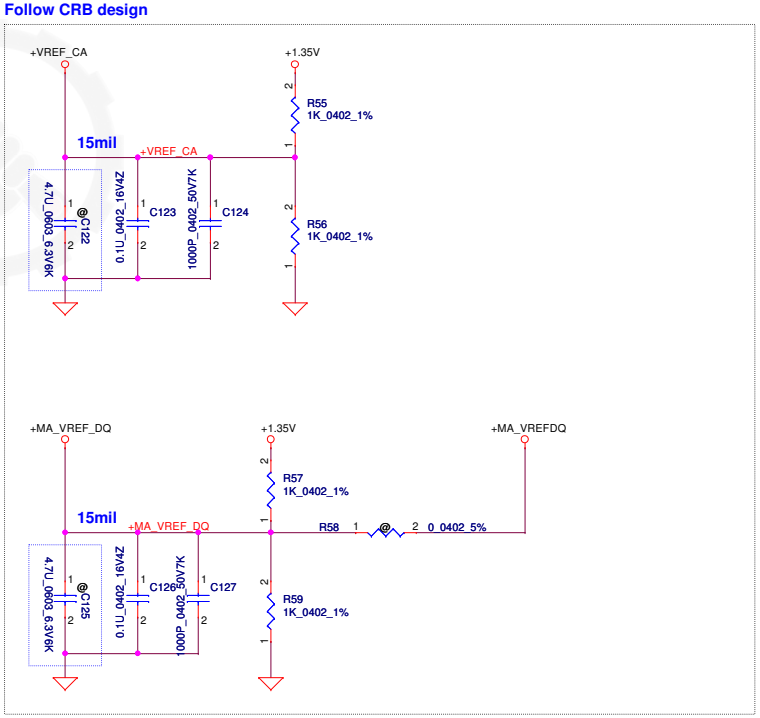


DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 6
DDRA_SDM[0..7] → DDRA_SDM[0..7] 6
DDRA_SMA[0..15] → DDRA_SMA[0..15] 6

Place near DIMM1



Follow CRB design



DIMM_A STD H:4mm

<Address: 00>

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Title: DIMM_A

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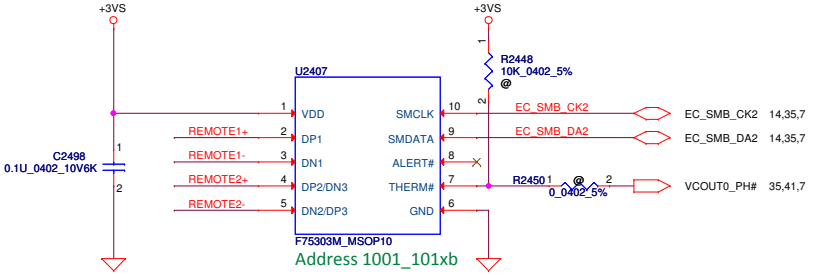
Fintek thermal sensor placed near by DDR3

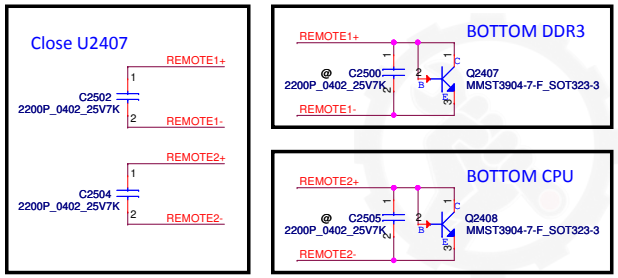
SA000046C00(S IC EMC1403-2-AIZL-TR MSOP 10P SENSOR)



Address 1001_101xb

2nd source

SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

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Title: Thermal Sensor

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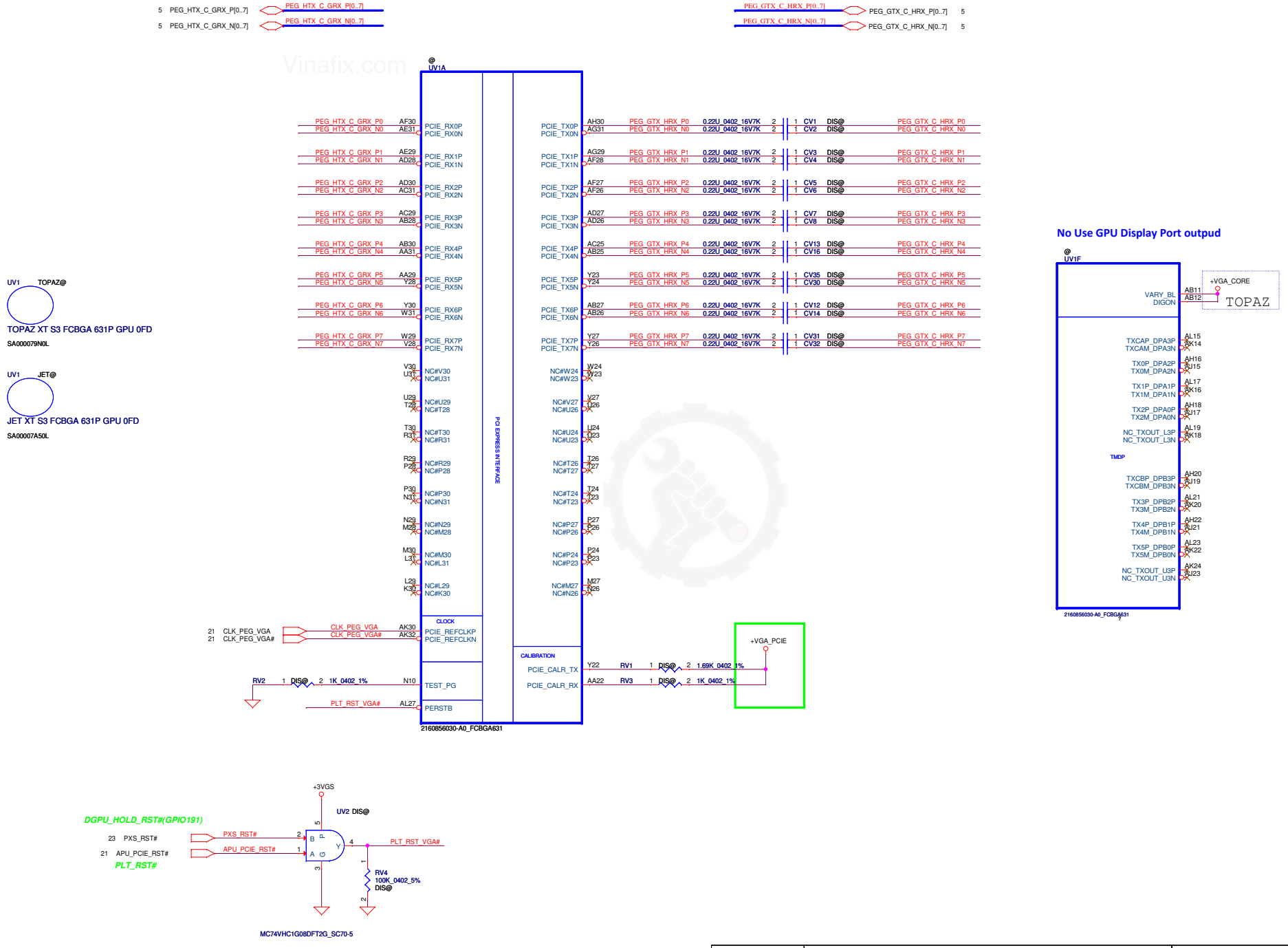

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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Title: TOPAZ_PCIE/DP

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

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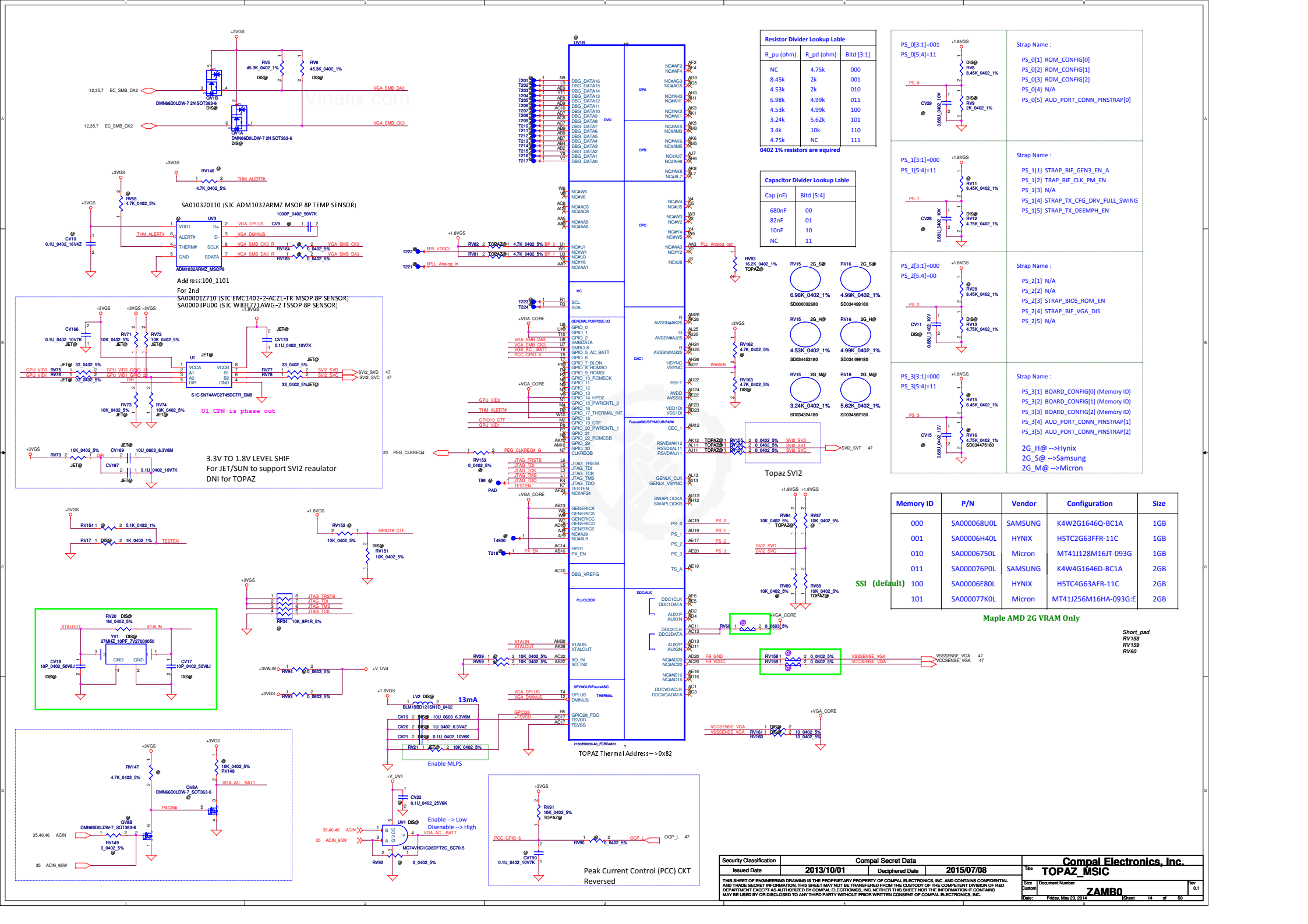
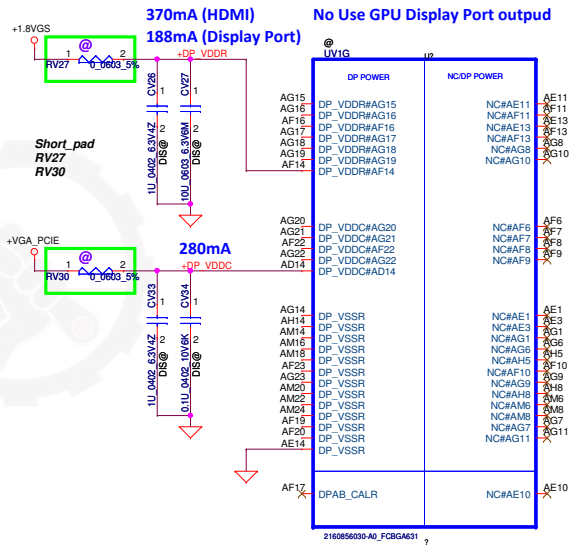
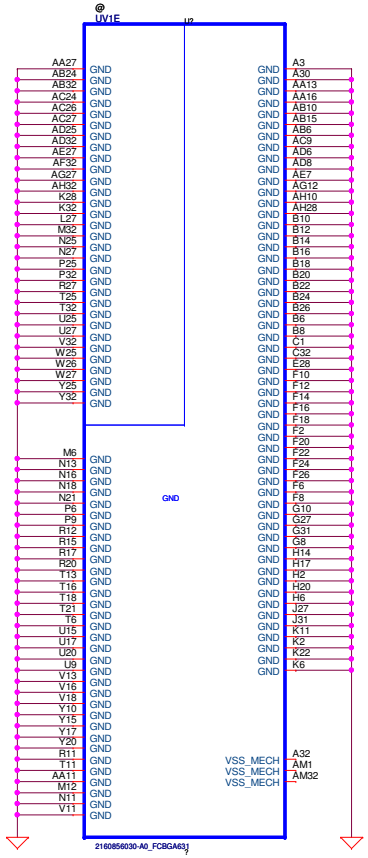

SA010320110 (SIC ADM1032ARMZ MSOP 8P TEMP SENSOR)
Address:100_1101
For 2nd
SA00001Z710 (SIC EMC1402-2-ACZL-TR MSOP 8P SENSOR)
SA00003PU00 (SIC W83L771AWG-2 TSSOP 8P SENSOR)
U1 CPN is phase out
3.3V TO 1.8V LEVEL SHIF
For JET/SUN to support SVI2 reaulator
DNI for TOPAZ
Topaz SVI2
13mA
Enable MLPS
TOPAZ Thermal Address—>0x82
Enable --> Low
Disenable --> High
Peak Current Control (PCC) CKT
Reversed
Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=00
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
2G_H@ -->Hynix
2G_S@ -->Samsung
2G_M@ -->Micron
Memory ID | P/N | Vendor | Configuration | Size
000 | SA000068U0L | SAMSUNG | K4W2G1646Q-BC1A | 1GB
001 | SA00006H40L | HYNIX | H5TC2G63FFR-11C | 1GB
010 | SA00006750L | Micron | MT41J128M16JT-093G | 1GB
011 | SA000076P0L | SAMSUNG | K4W4G1646D-BC1A | 2GB
100 | SA00006E80L | HYNIX | H5TC4G63AFR-11C | 2GB
101 | SA000077K0L | Micron | MT41J256M16HA-093G:E | 2GB
SSI (default)
Maple AMD 2G VRAM Only
Short_pad
RV158
RV159
RV160
Security Classification | Compal Secret Data
Issued Date | 2013/10/01 | Deciphered Date | 2015/07/08
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title: TOPAZ_MSIC
Size: Custom | Document Number: ZAMB0 | Rev: 0.1
Date: Friday, May 23, 2014 | Sheet 14 of 50

+1.35VS_VGA TO +1.35V_MEM_GFX

JP9 DEFAULT SHORT





Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **TOPAZ_Power/GND**

Size: Custom | Document Number: **ZAMB0** | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 15 of 50

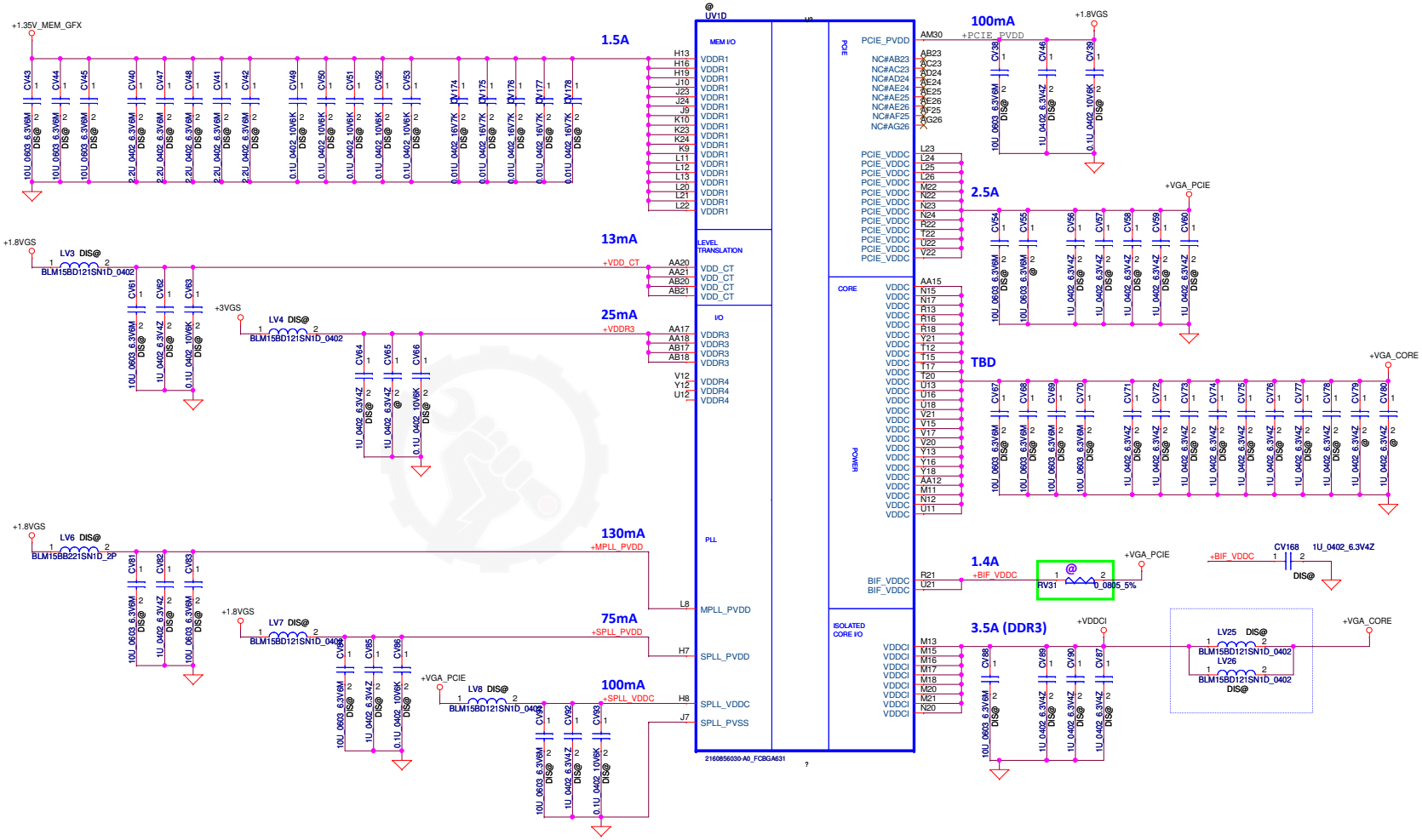
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+VGA_PCIE		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



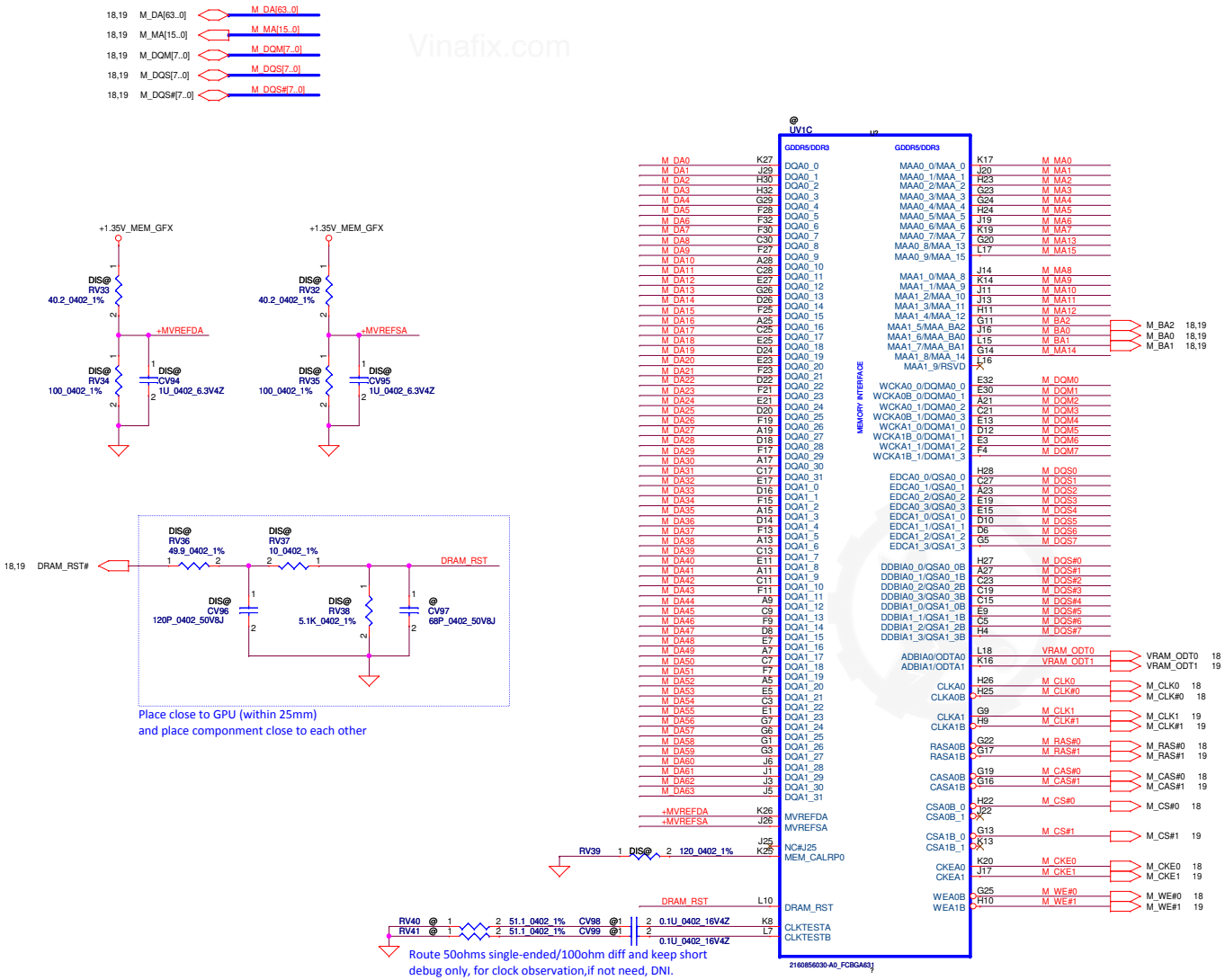
Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: TOPAZ_Power

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 16 of 50



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

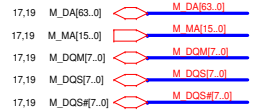
Compal Electronics, Inc.

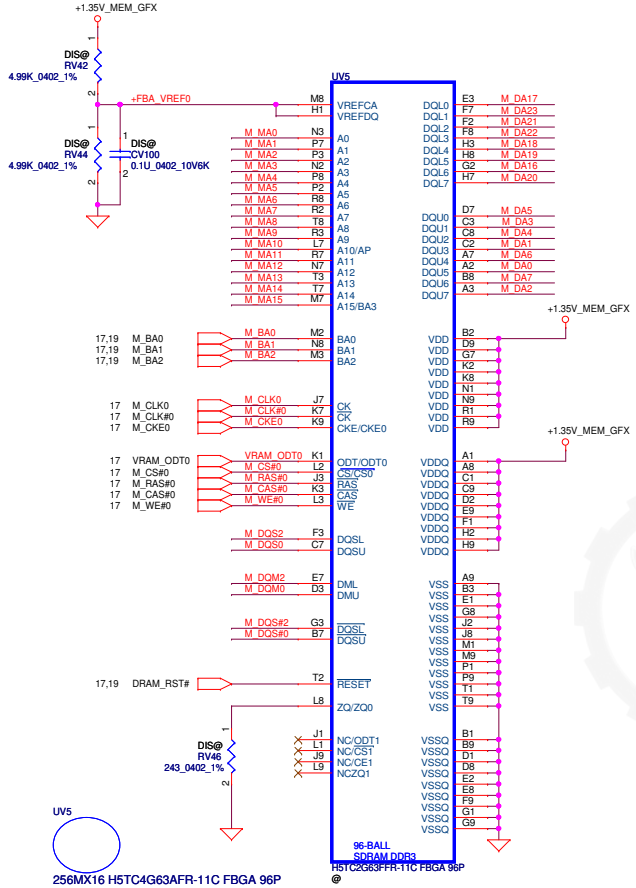
Title: TOPAZ_MEM

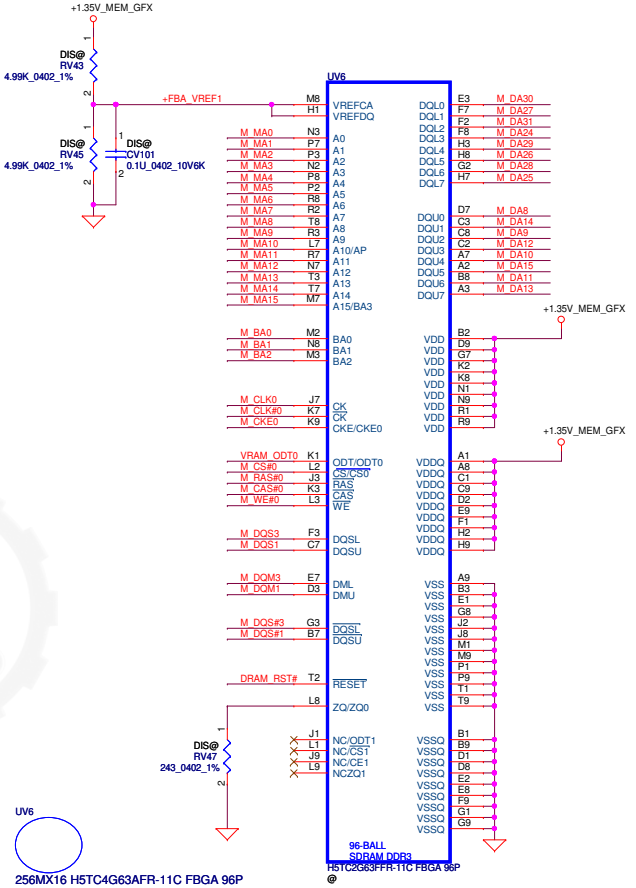
Size: Custom | Document Number: ZAMB0 | Rev: 0.1

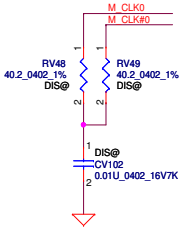
Date: Friday, May 23, 2014 | Sheet 17 of 50

Memory Partition A - Lower 32 bits









UV5

256MX16 H5TC4G63AFR-11C FBGA 96P

SA00006E80L

X76@

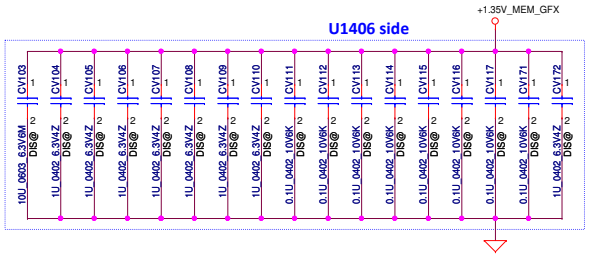
UV6

256MX16 H5TC4G63AFR-11C FBGA 96P

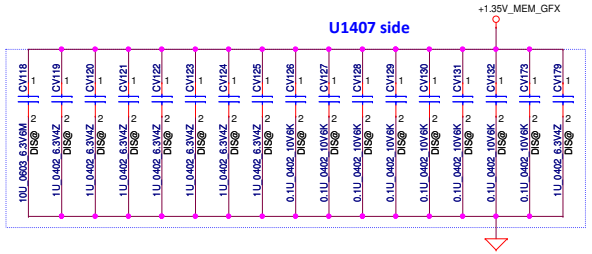
SA00006E80L

X76@

U1406 side



U1407 side



X7655131L04, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design)	
SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design)	
SD034453180, S RES 1/16W 4.53K +-1% 0402, A.1 (Design)	
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)	
X7655131L05, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design)	
SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design)	
SD000002680, S RES 1/16W 6.98K +-1% 0402, A.1 (Design)	
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)	
X7655131L06, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design)	
SA000077K0L, S IC D3 256M16 MT41J256M16HA-093G:E FBGA, A.4 (Design)	
SD034324180, S RES 1/16W 3.24K +-1% 0402, A.1 (Design)	
SD034562180, S RES 1/16W 5.62K +-1% 0402, A.1 (Design)	

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

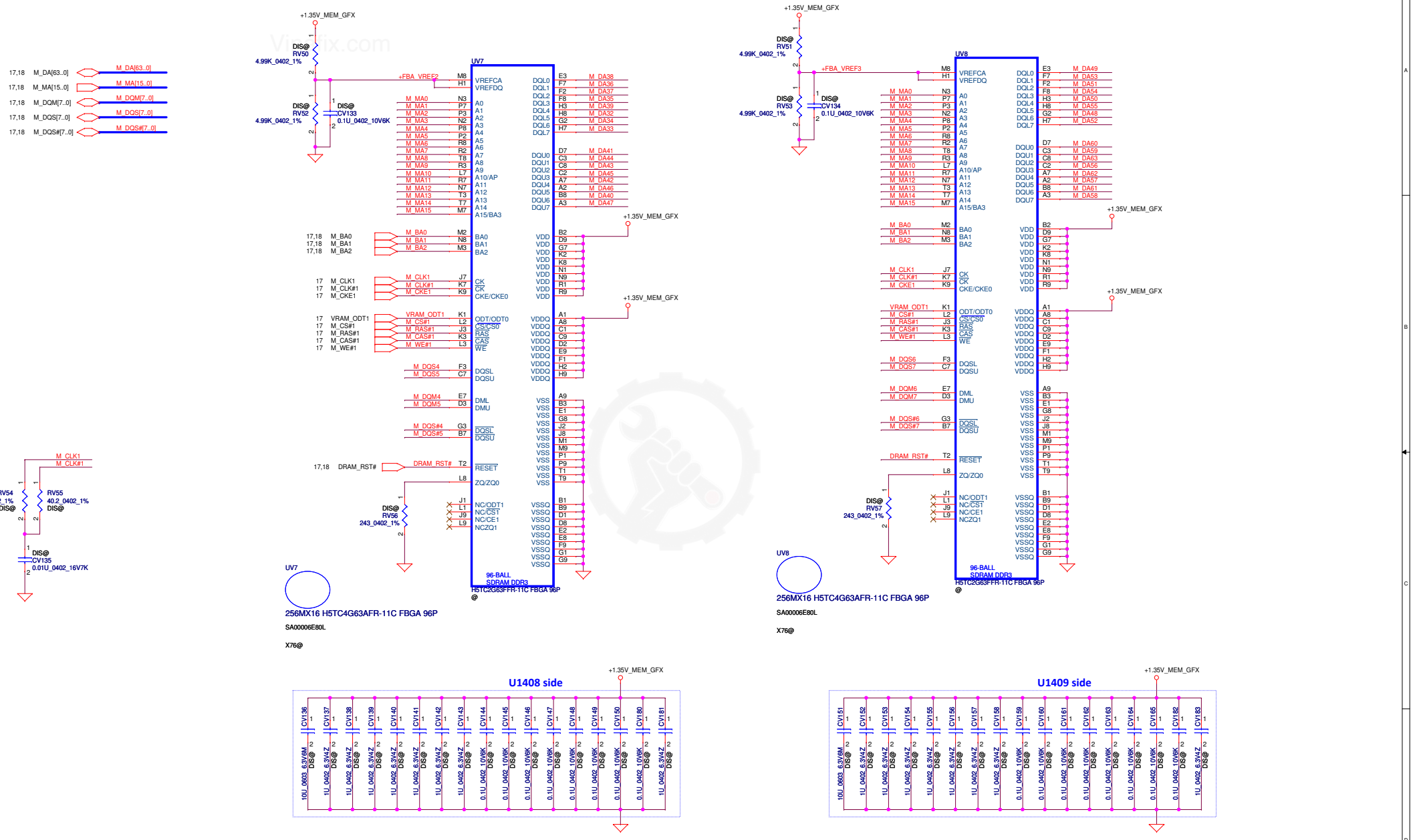
Compal Electronics, Inc.

Title: TOPAZ_VRAM A Lower

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 18 of 50

Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: TOPAZ_VRAM A Upper

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 19 of 50

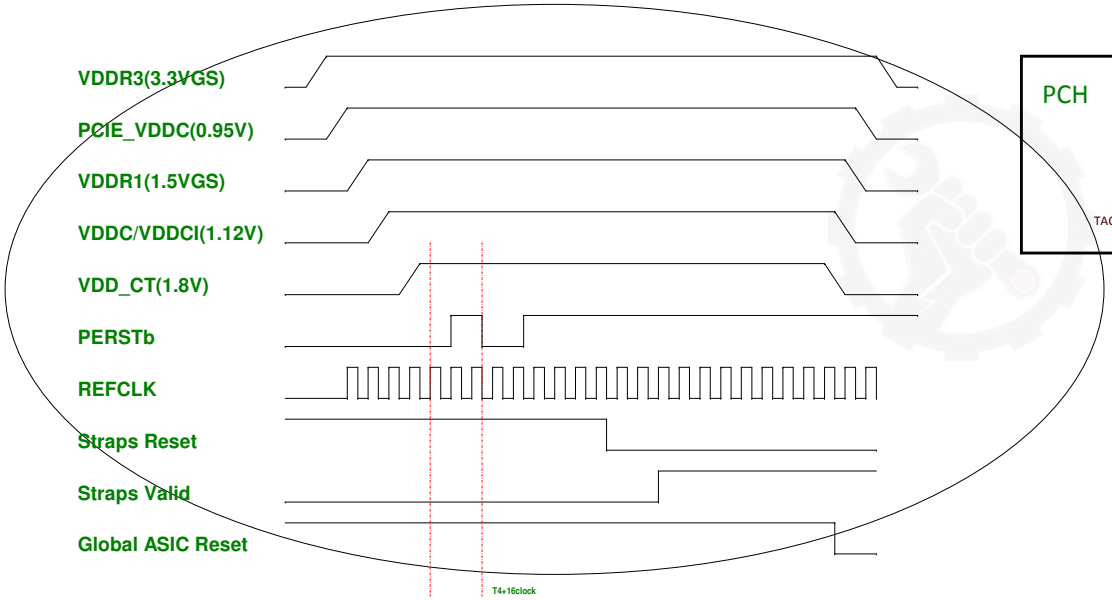
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

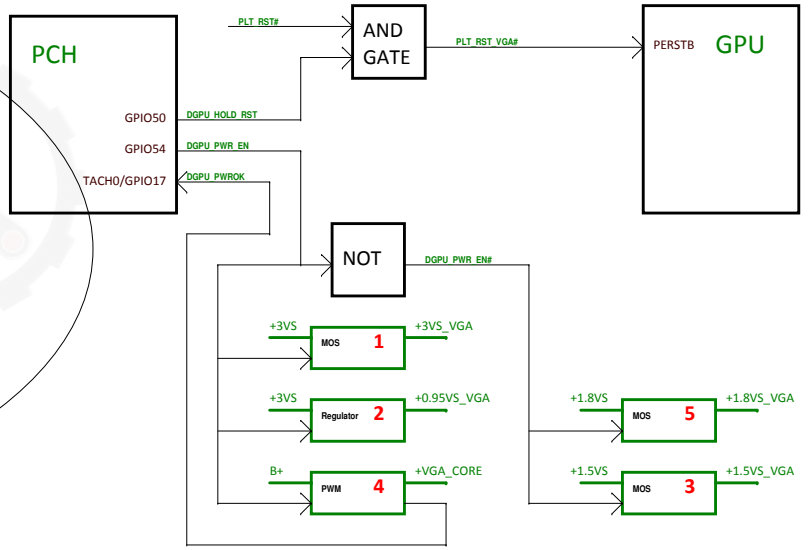
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.

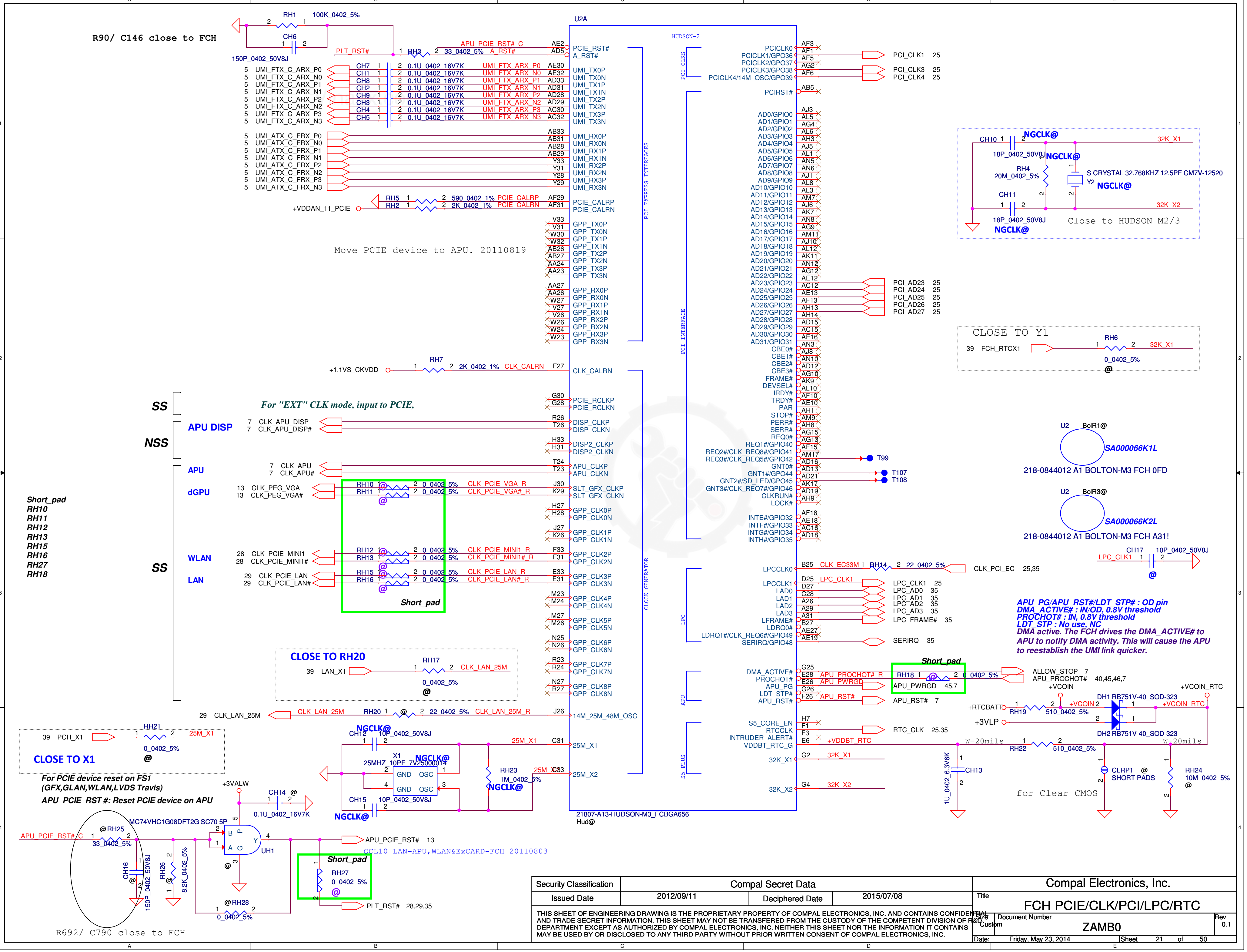


CPU part



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

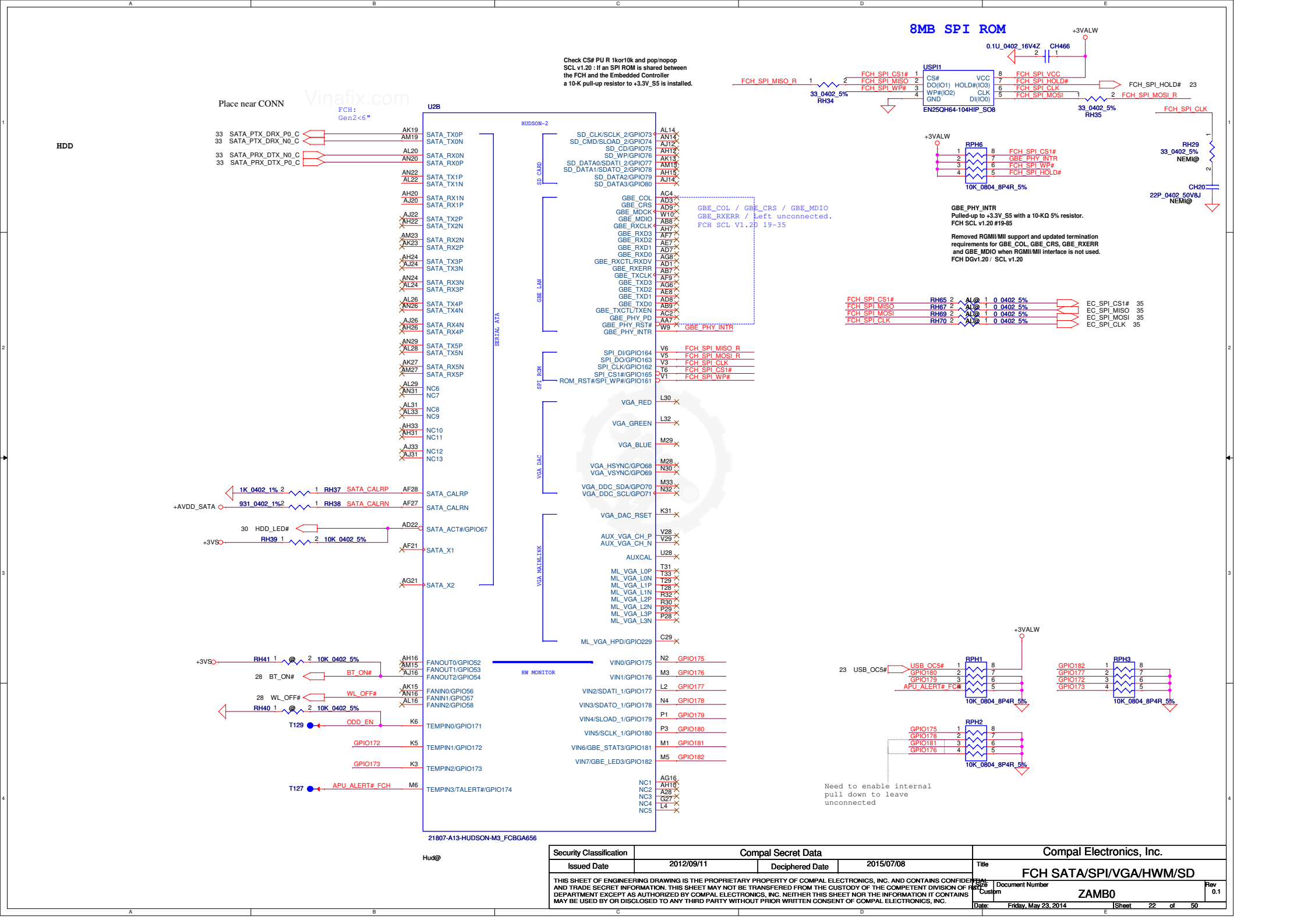
Compal Electronics, Inc.			
Title	TOPAZ_NOTE		
Size	Document Number		Rev
	ZAMB0		0.1
Date:	Friday, May 23, 2014	Sheet	20 of 50



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date: 2012/09/11	Deciphered Date: 2015/07/08		Title: FCH PCIE/CLK/PCI/LPC/RTC

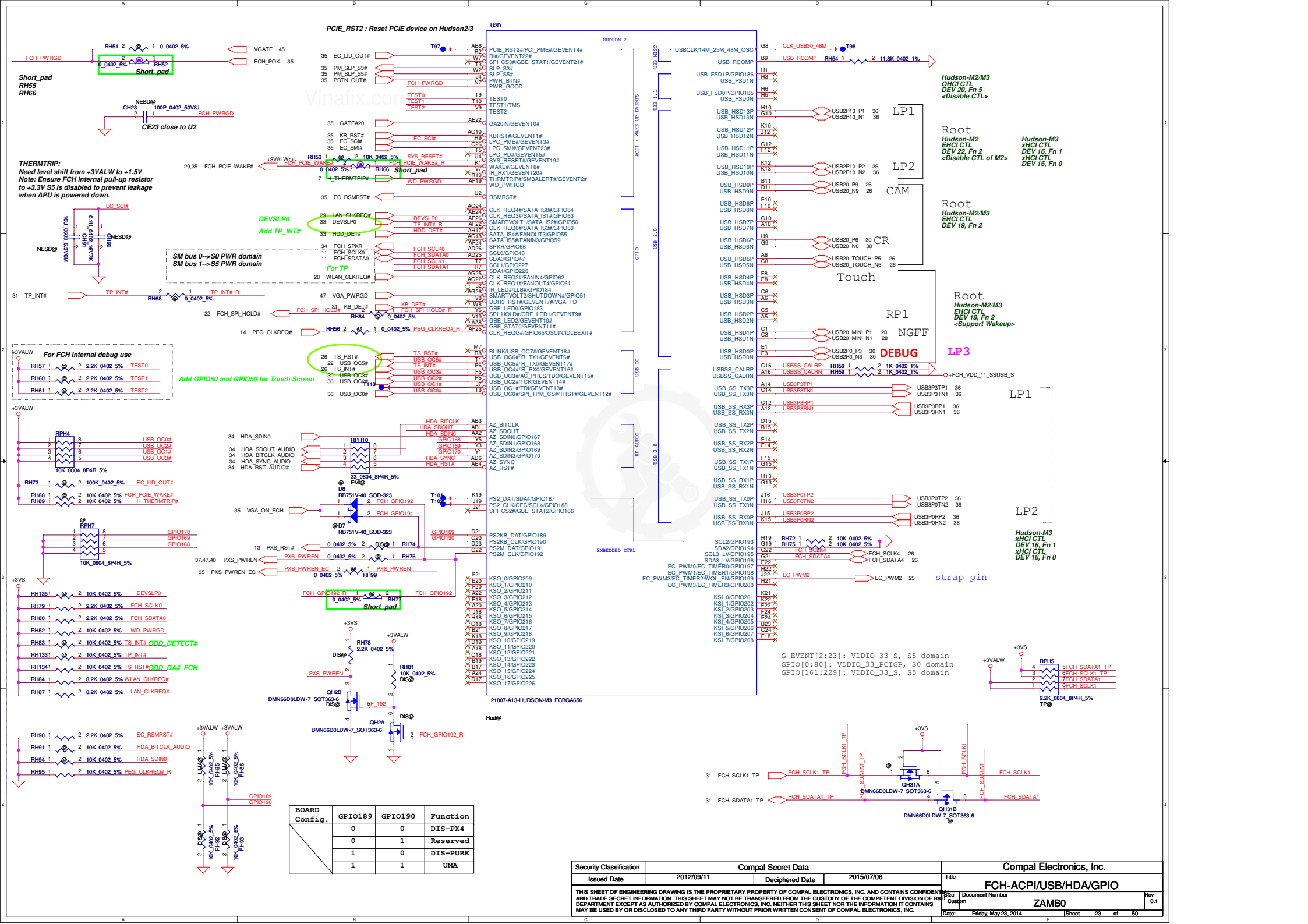
Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 21 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

Compal Electronics, Inc.	
Title	FCH SATA/SPI/VGA/HWM/SD
Size: Custom	Document Number: ZAMB0
Rev	0.1
Date: Friday, May 23, 2014	Sheet 22 of 50



BOARD Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA

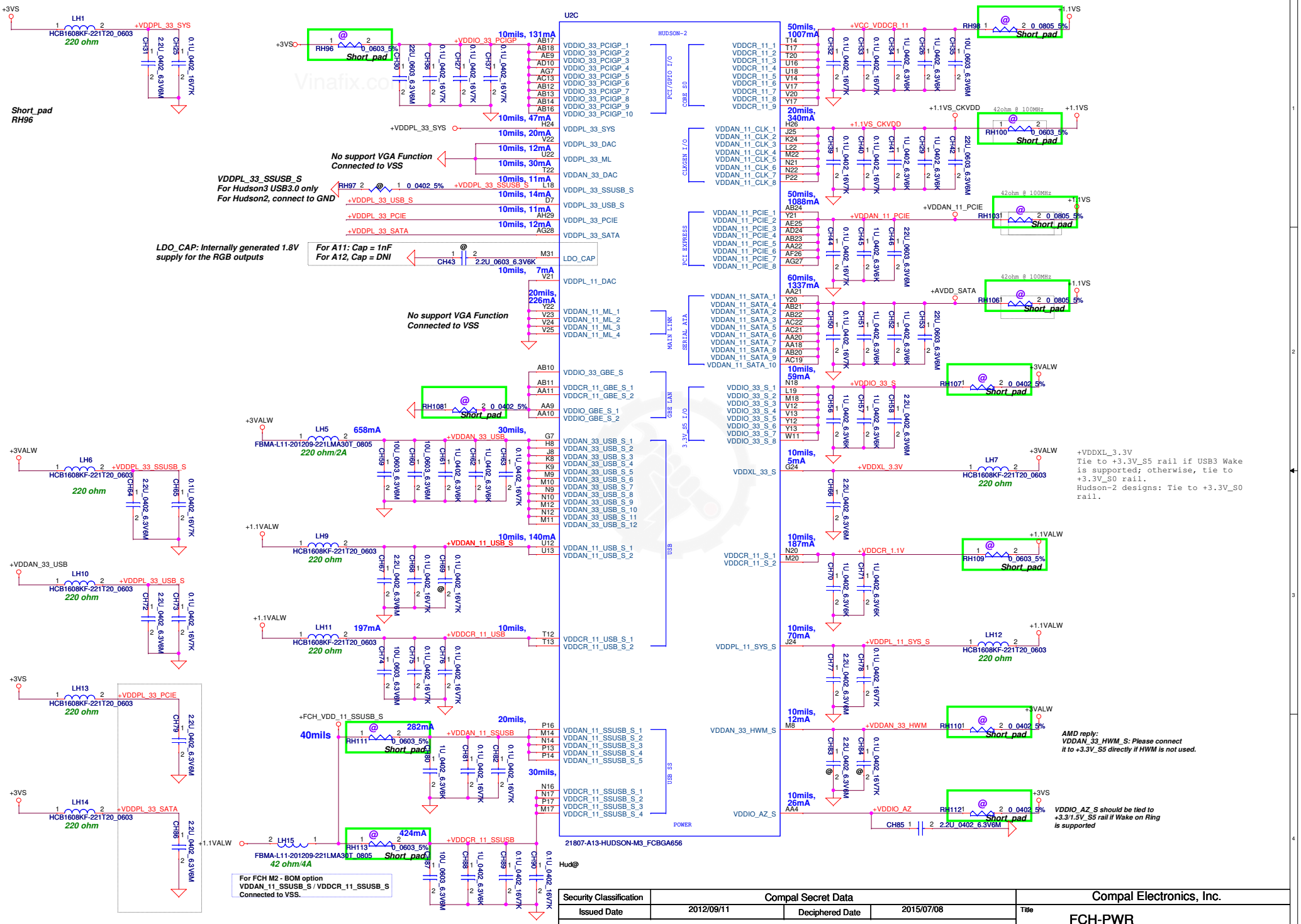
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size	Document Number	Rev
Custom	ZAMB0	0.1

Date: Friday, May 23, 2014 | Sheet 23 of 50



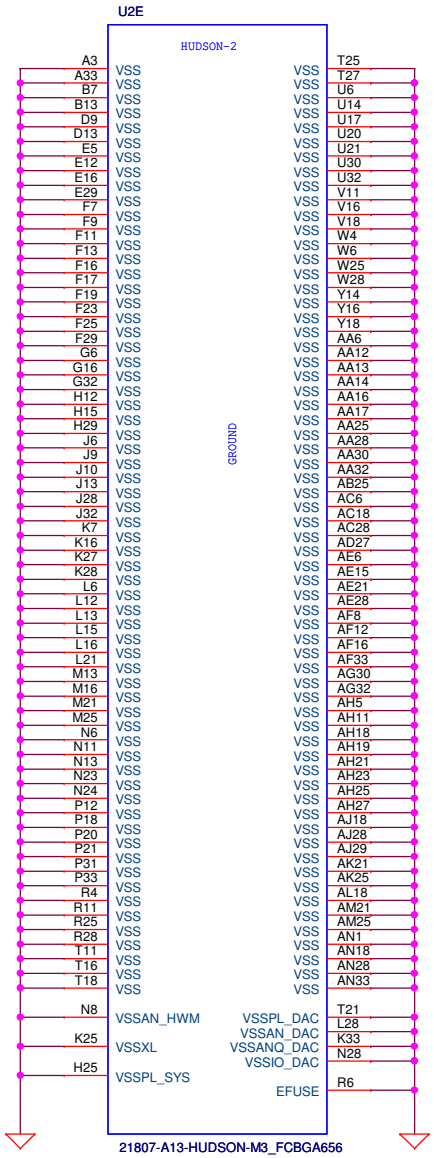
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FCH-PWR

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 24 of 50



Hud@

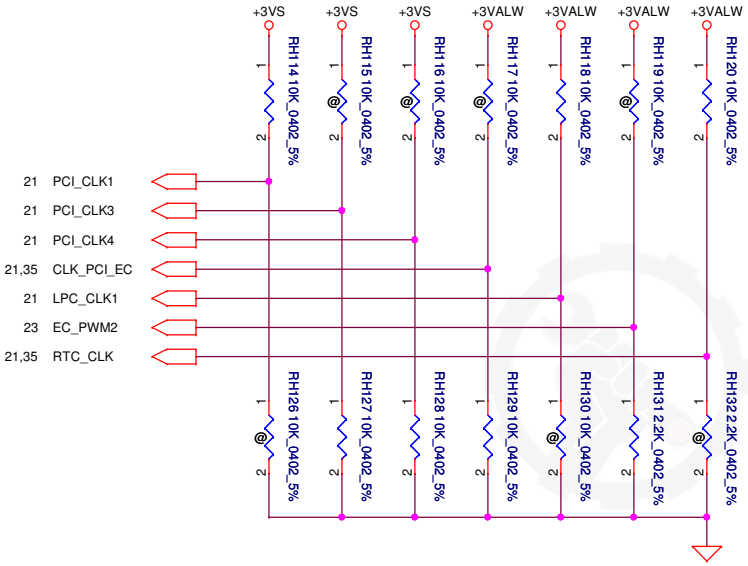
STRAP PINS

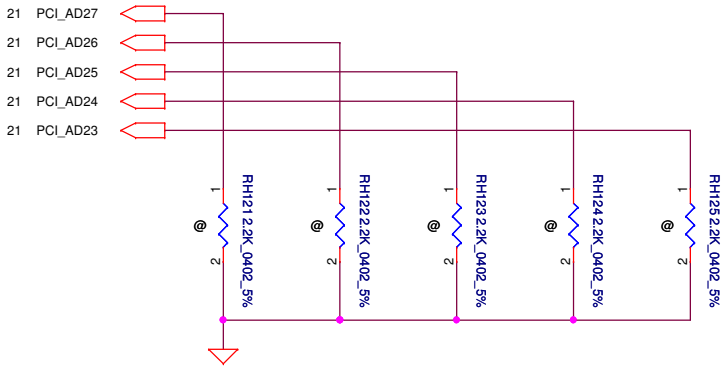
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

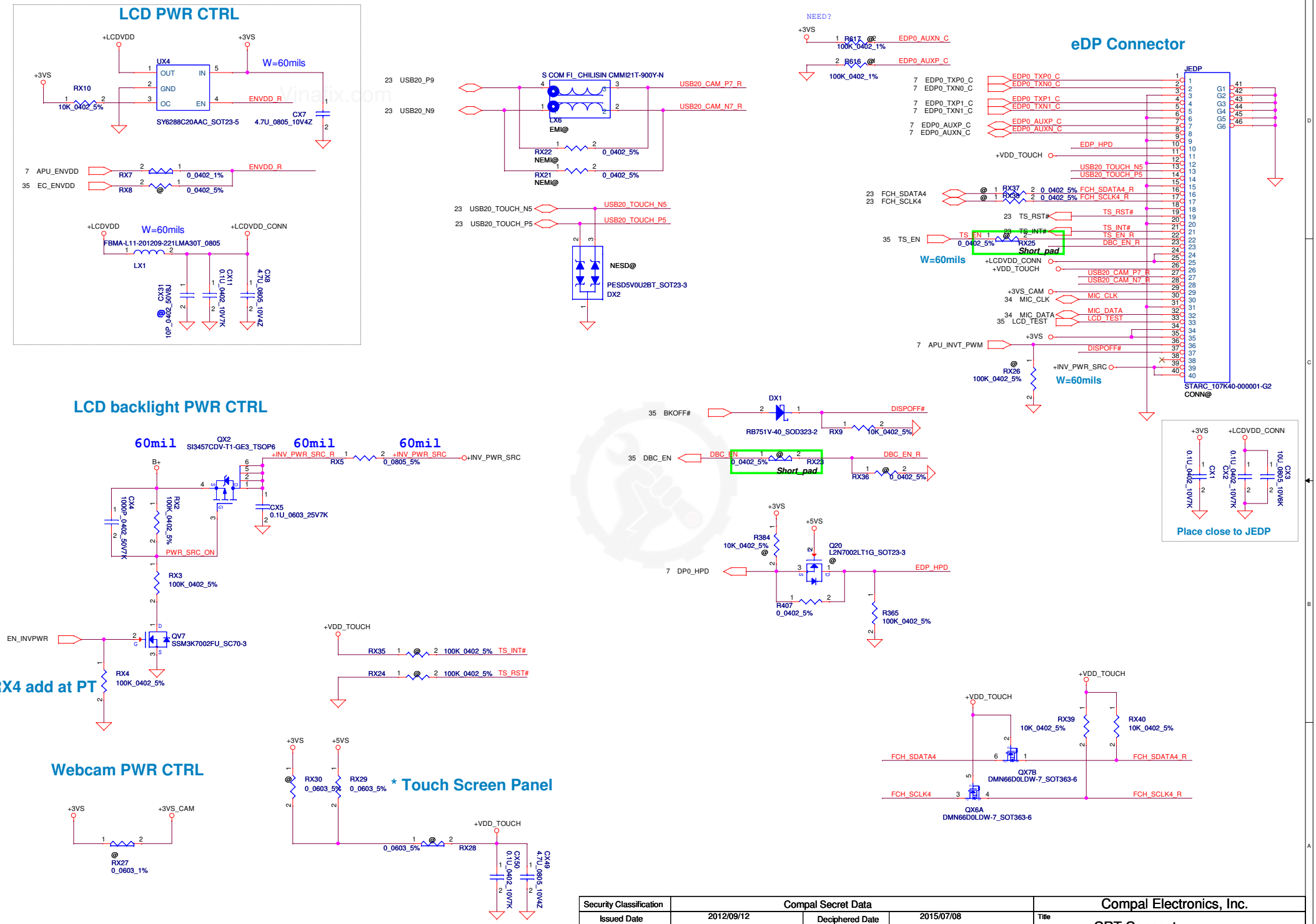
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



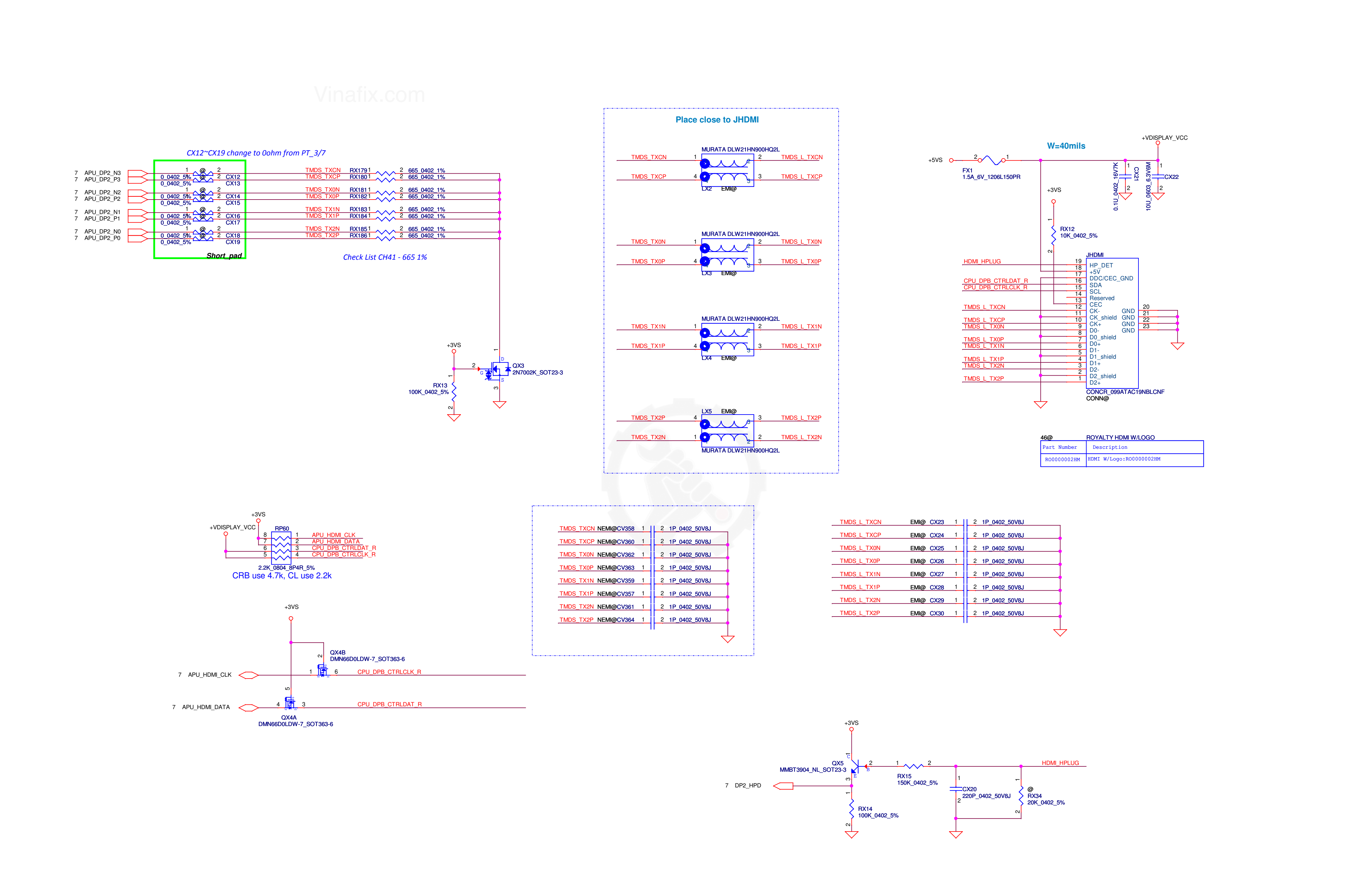


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/11	Deciphered Date 2015/07/08	Title: FCH-VSS/Strap
			Size: B; Document Number: ZAMB0; Rev: 0.1
			Date: Friday, May 23, 2014; Sheet 25 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title: CRT Connector.			
Size: Custom	Document Number: ZAMB0		Rev: 0.1
Date: Friday, May 23, 2014	Sheet 26 of 50		



Place close to JHDMI
CX12~CX19 change to 0ohm from PT_3/7
Short_pad
Check List CH41 - 665 1%
APU_DP2_N3
APU_DP2_P3
APU_DP2_N2
APU_DP2_P2
APU_DP2_N1
APU_DP2_P1
APU_DP2_N0
APU_DP2_P0
0_0402_5%
CX12 CX13 CX14 CX15 CX16 CX17 CX18 CX19
TMDS_TXCN TMDS_TXCP TMDS_TX0N TMDS_TX0P TMDS_TX1N TMDS_TX1P TMDS_TX2N TMDS_TX2P
RX179 RX180 RX181 RX182 RX183 RX184 RX185 RX186
665_0402_1%
MURATA DLW21HN900HQ2L
LX2 EMI@
LX3 EMI@
LX4 EMI@
LX5 EMI@
TMDS_L_TXCN TMDS_L_TXCP TMDS_L_TX0N TMDS_L_TX0P TMDS_L_TX1N TMDS_L_TX1P TMDS_L_TX2N TMDS_L_TX2P
W=40mils
+5VS
FX1
1.5A_6V_1206L150PR
+VDISPLAY_VCC
0.1U_0402_16V7K
CX21
10U_0603_6.3V6M
CX22
+3VS
RX12
10K_0402_5%
HDMI_HPLUG
CPU_DPB_CTRLDAT_R
CPU_DPB_CTRLCLK_R
JHDMI
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
GND
CONCR_099ATAC19NBLCNF
CONN@
QX3
2N7002K_SOT23-3
RX13
100K_0402_5%
46@
ROYALTY HDMI W/LOGO
Part Number
Description
RO0000002HM
HDMI W/Logo:RO0000002HM
RP60
2.2K_0804_8P4R_5%
APU_HDMI_CLK
APU_HDMI_DATA
CRB use 4.7k, CL use 2.2k
NEMI@CV358 NEMI@CV360 NEMI@CV362 NEMI@CV363 NEMI@CV359 NEMI@CV357 NEMI@CV361 NEMI@CV364
1P_0402_50V8J
EMI@ CX23 CX24 CX25 CX26 CX27 CX28 CX29 CX30
QX4B
DMN66D0LDW-7_SOT363-6
QX4A
DMN66D0LDW-7_SOT363-6
QX5
MMBT3904_NL_SOT23-3
DP2_HPD
RX15
150K_0402_5%
RX14
100K_0402_5%
CX20
220P_0402_50V8J
RX34
20K_0402_5%
Vinafix.com

Security Classification	Compal Secret Data	
Issued Date	2013/10/01	Deciphered Date 2015/07/08

Compal Electronics, Inc.

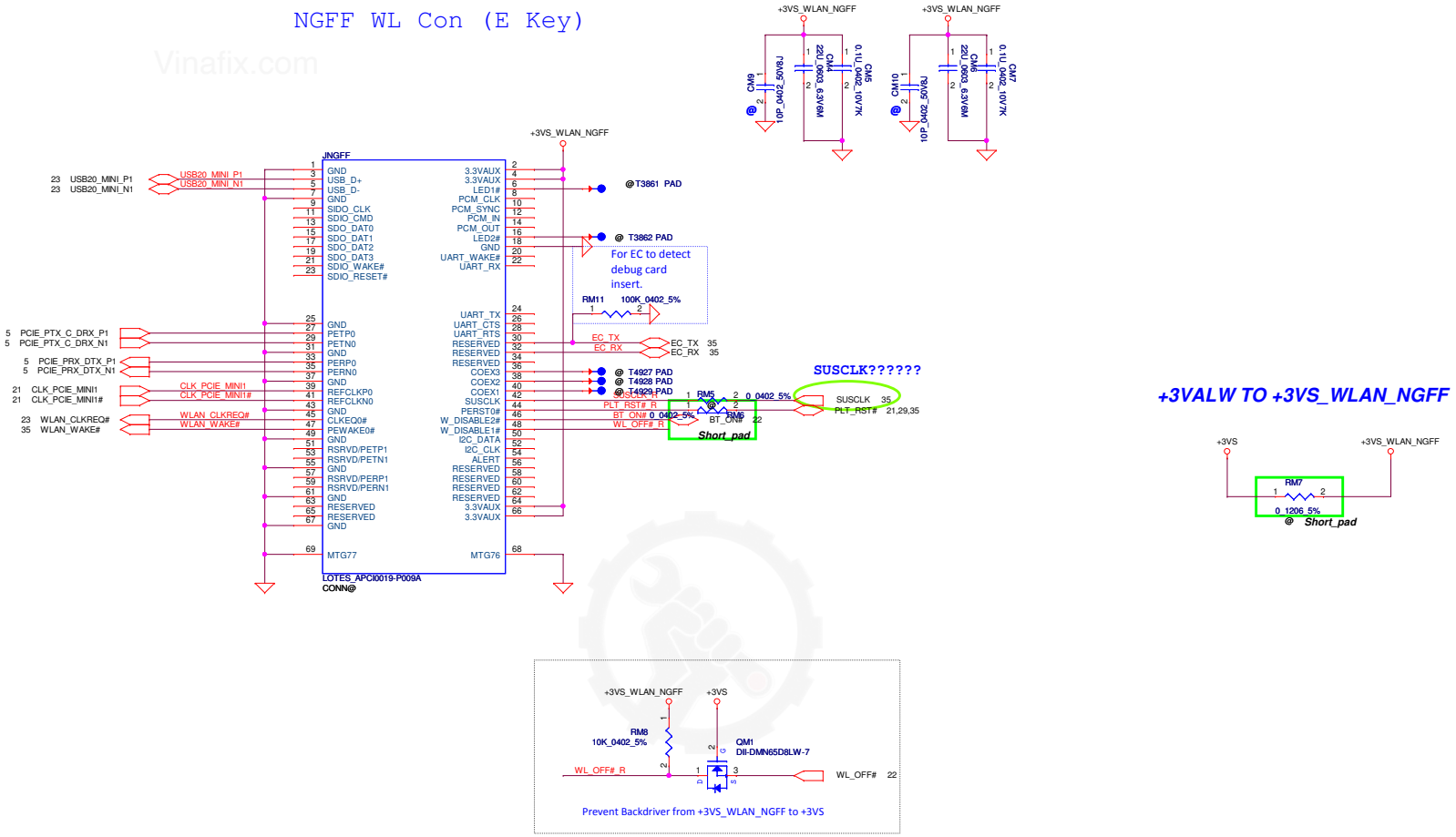
Title: **HDMI**

Size / Document Number: **ZAMB0** — Rev 0.1

NGFF WL Con (E Key)

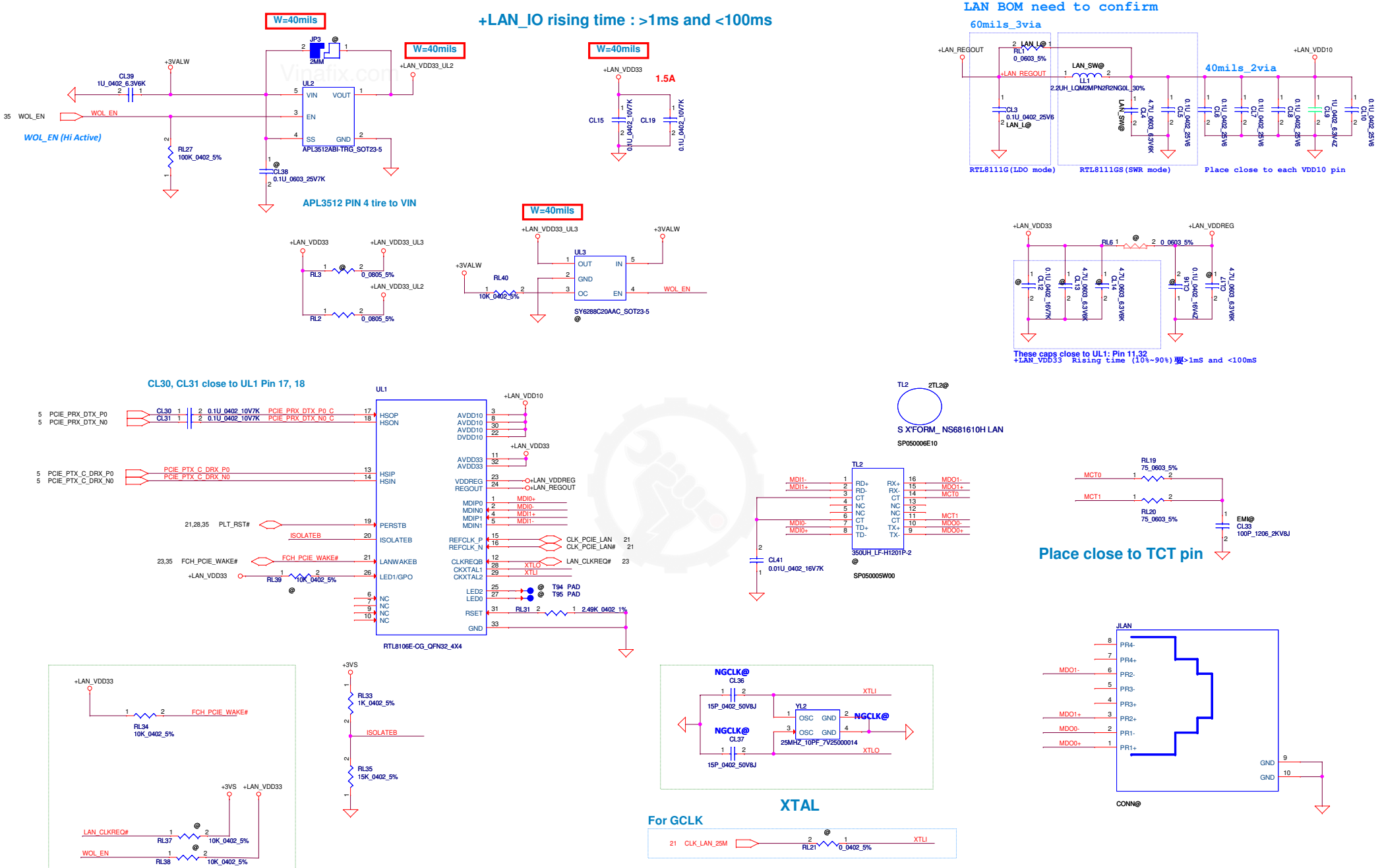
closed to pin 2, 4

closed to pin 64, 66



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title: NGFF WLAN			
Size	Document Number: ZAMB0		Rev: 0.1
Date: Friday, May 23, 2014	Sheet 28 of 50		



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

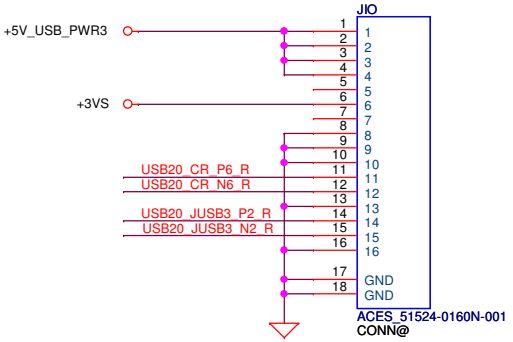
Compal Electronics, Inc.

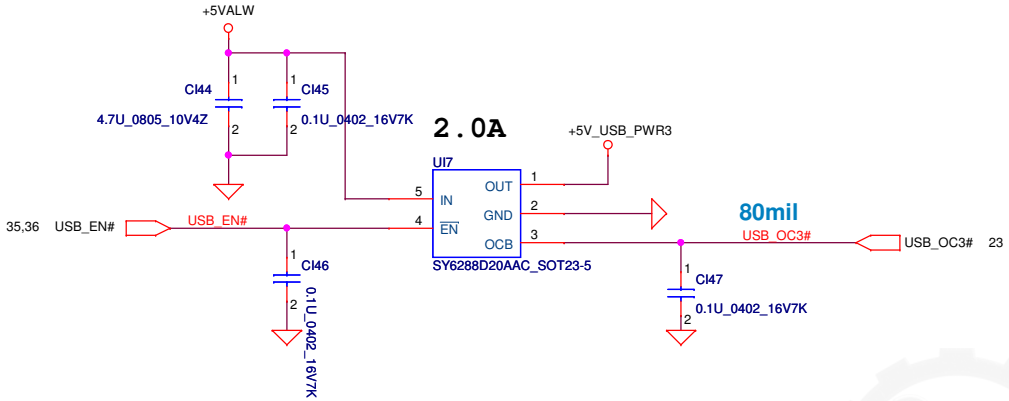
Title: LAN RTL8106EUS

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 29 of 50

IO to MB CONN
Substitute:SP01001FS00

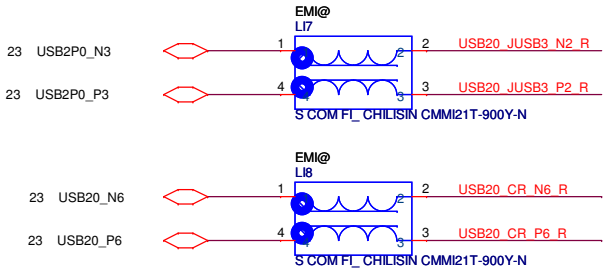




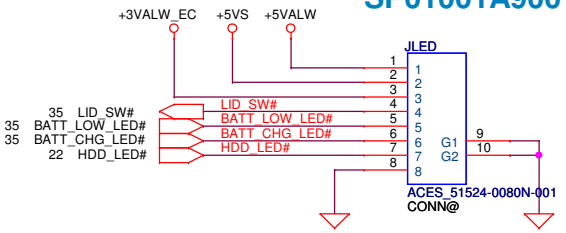
USB Conn

DEBUG Port

Card Reader



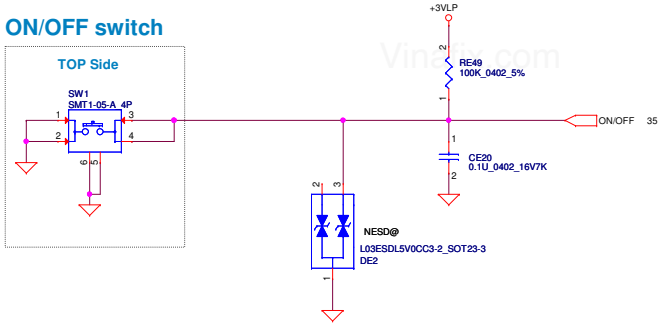
LED/B TO M/B
SP01001A900



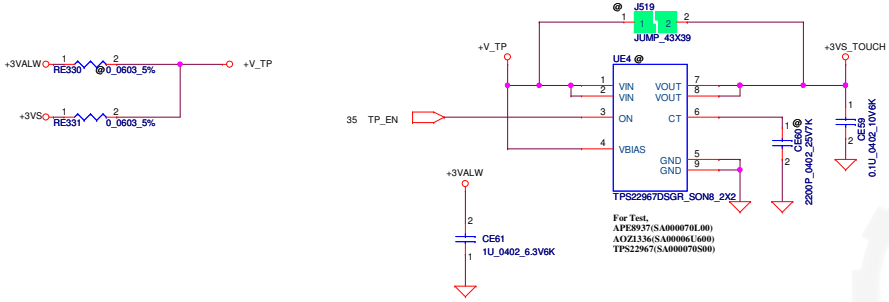
Title	IO/B, LED/B		
Size B	Document Number ZAMB0		Rev 0.1
Date: Friday, May 23, 2014	Sheet 30 of 50		

Power ON Circuit

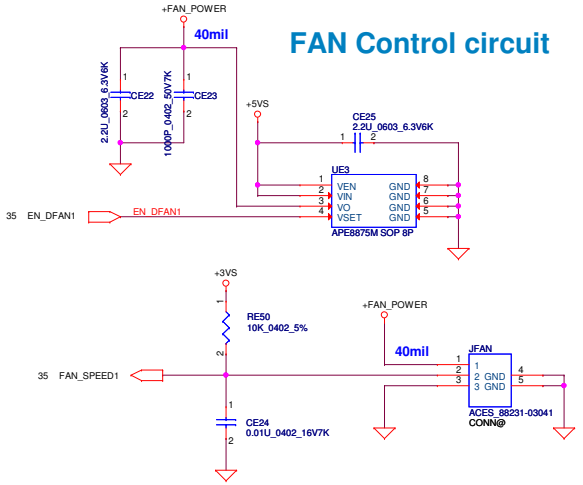
ON/OFF switch



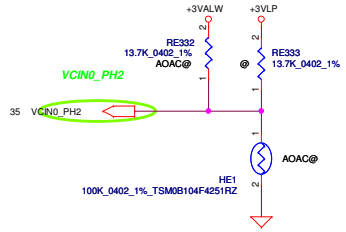
J519 short



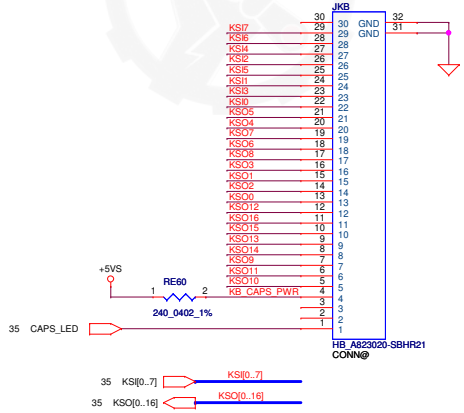
FAN Control circuit



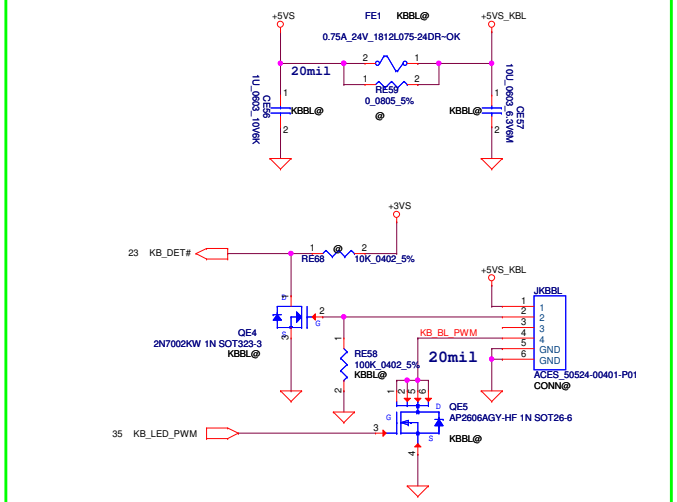
HE1 place around FAN area.



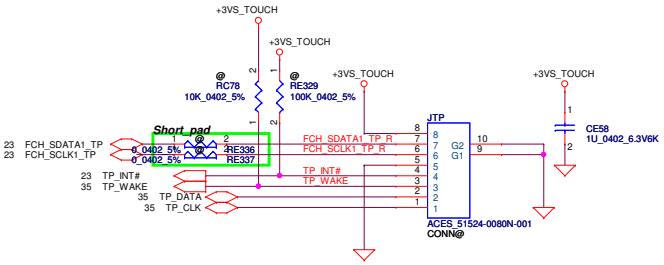
INT_KBD Connector



* Key Board Back Light



Touch pad PS/2 only



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 31 of 50

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

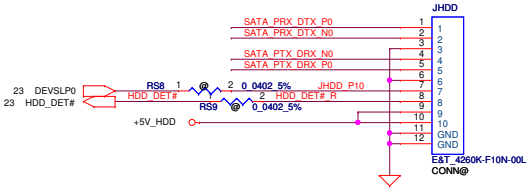
Compal Electronics, Inc.

Title: SMSC thermal sens/FAN/screw

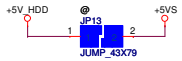
Size	Document Number	Rev
Custom	ZAMB0	0.1

Date: Friday, May 23, 2014 | Sheet 32 of 50

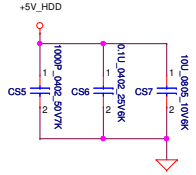
SATA HDD Connector

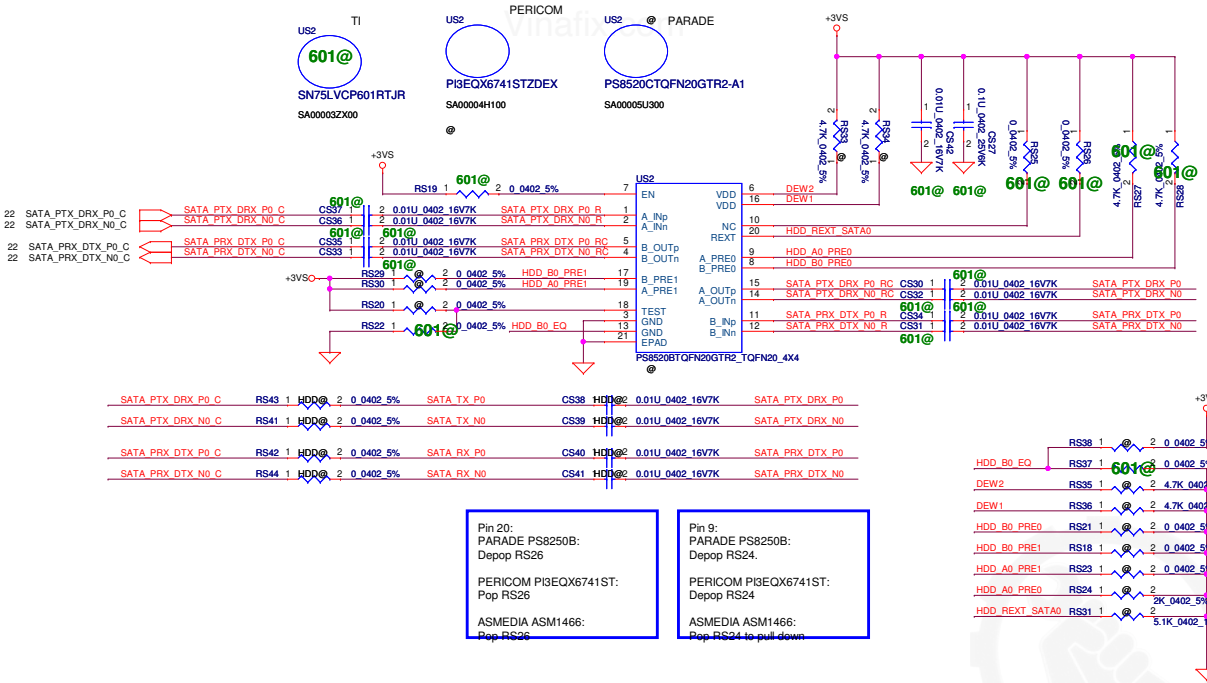


+5V_HDD Source



SHORT DEFAULT





Pin 20:
PARADE PS8250B:
Depop RS26

PERICOM PI3EQX6741ST:
Pop RS26

ASMEDIA ASM1466:
Pop RS26

Pin 9:
PARADE PS8250B:
Depop RS24.

PERICOM PI3EQX6741ST:
Depop RS24

ASMEDIA ASM1466:
Pop RS24 to pull down

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: HDD

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 33 of 50

CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

JACK_PLUG Delay circutis

Reserve for HDA issue

Reserve for cancel Delay circutis

Place on the moat between GND & GNDA.

SM01000BV00 need CIS symbol

EC Beep

MCU Beep

PC Beep

Close to UA1 Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

SCA00001B00

DA10 change P/N from SCA00002900 to SCA00001A00

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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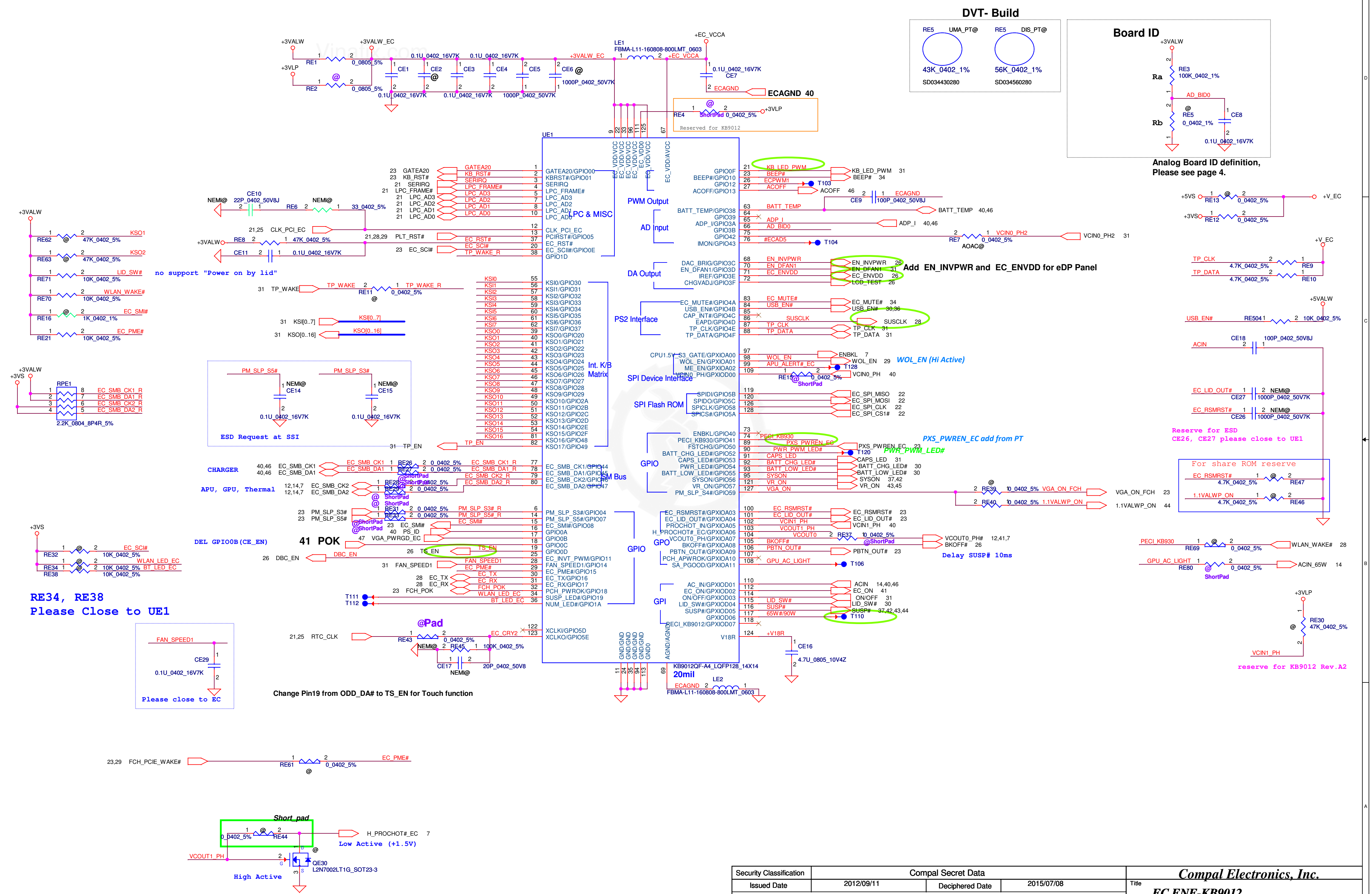
Compal Electronics, Inc.

Title: Audio Codec ALC3234

Document Number: ZAMB0

Rev: 0.1

Date: Friday, May 23, 2014 Sheet 34 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

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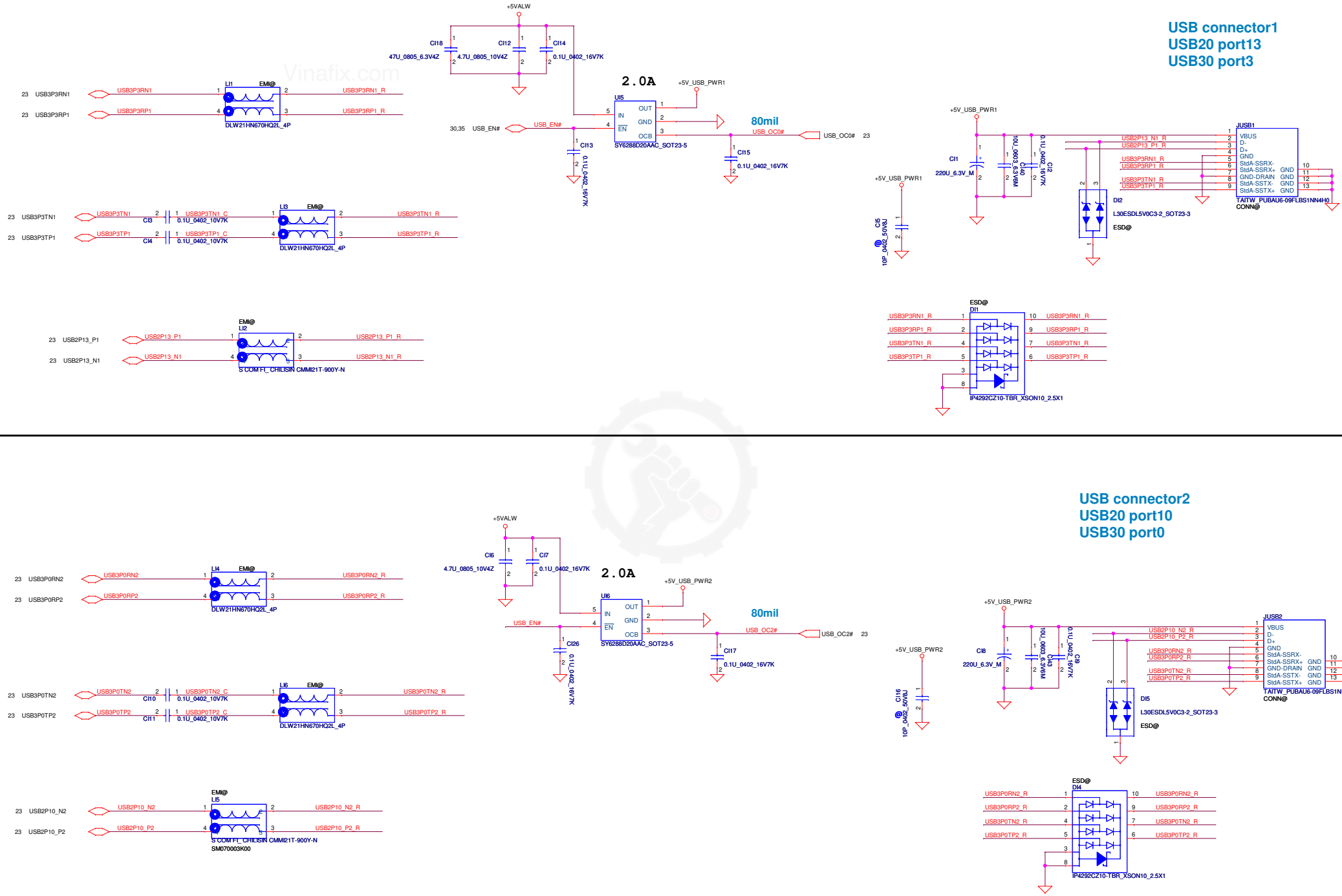
Compal Electronics, Inc.

Title: EC ENE-KB9012

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 35 of 50



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

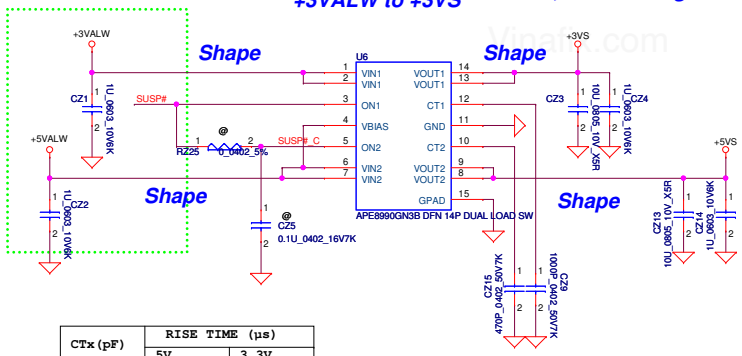
Title: **USB3.0**

Size | Document Number: **ZAMB0** | Rev: 0.1

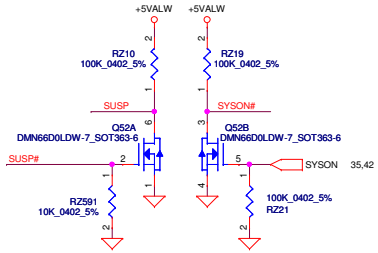
Date: Friday, May 23, 2014 | Sheet 36 of 50

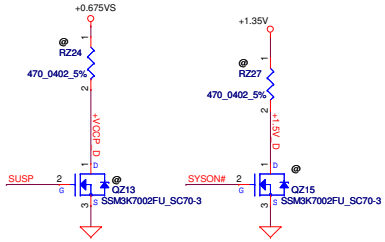
+5VALW to +5VS
+3VALW to +3VS

CZ3, CZ13 Change to H=0.85mm

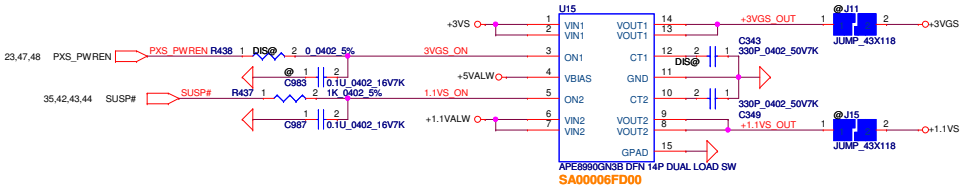


CTx(pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



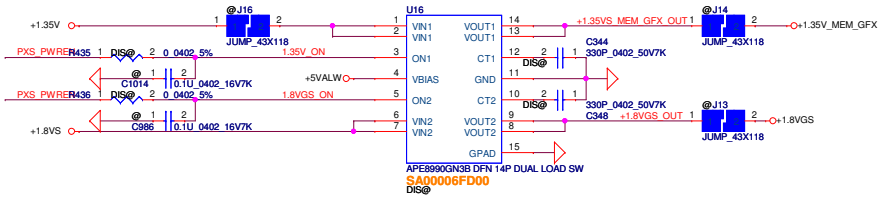


+1.1VALW to +1.1VS
+3VS to +3VGS

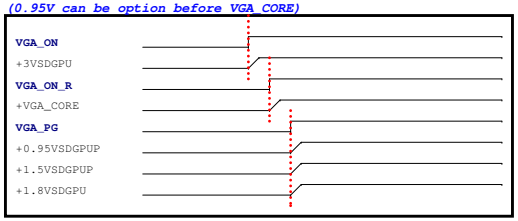


+1.35V to +1.35VS_MEM_GFX_OUT
+1.8VS to +1.8VSDGPU

J13 OPEN DEFAULT



VGA sequence : default same as V5WE2
(0.95V can be option before VGA_CORE)



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.	
Title	DC/DC Interface
Size	Document Number: ZAMB0
Rev	0.1
Date: Friday, May 23, 2014	Sheet 37 of 50

Screw Hole

H1 H_2P8N @
H20 H_2P8N @
H21 H_2P8N @
H22 H_2P8X3P3N @
H23 H_2P8X4P8N @

H2 H_2P8 @
H3 H_2P8 @
H4 H_2P8 @
H5 H_2P8 @
H6 H_2P8 @
H7 H_2P8 @
H8 H_2P8 @
H9 H_2P8 @

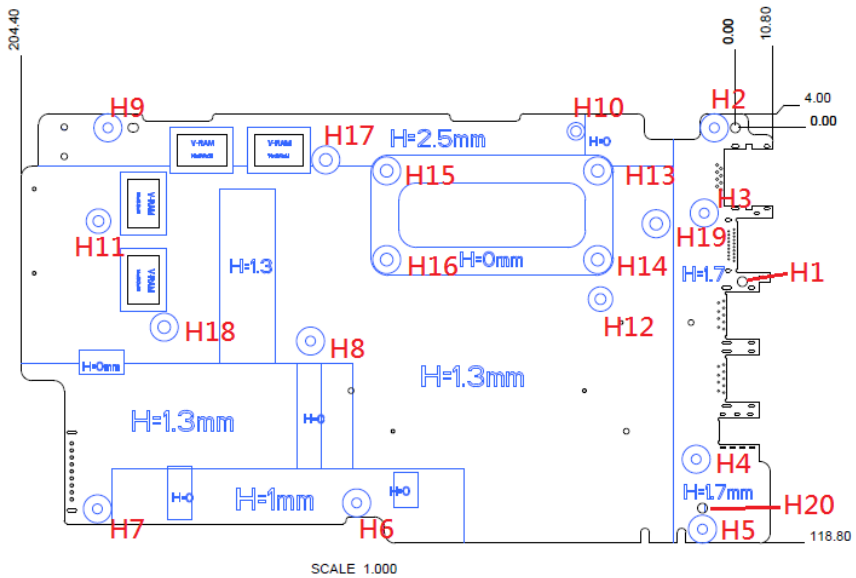
H11 H_2P8 @
H12 H_2P8 @

H13 H_3P6 @
H14 H_3P6 @
H15 H_3P6 @
H16 H_3P6 @
CPU bracket

H17 H_3P3 @
H18 H_3P3 @
VGA stand-off

H19 H_3P3 @
NGFF stand-off

FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

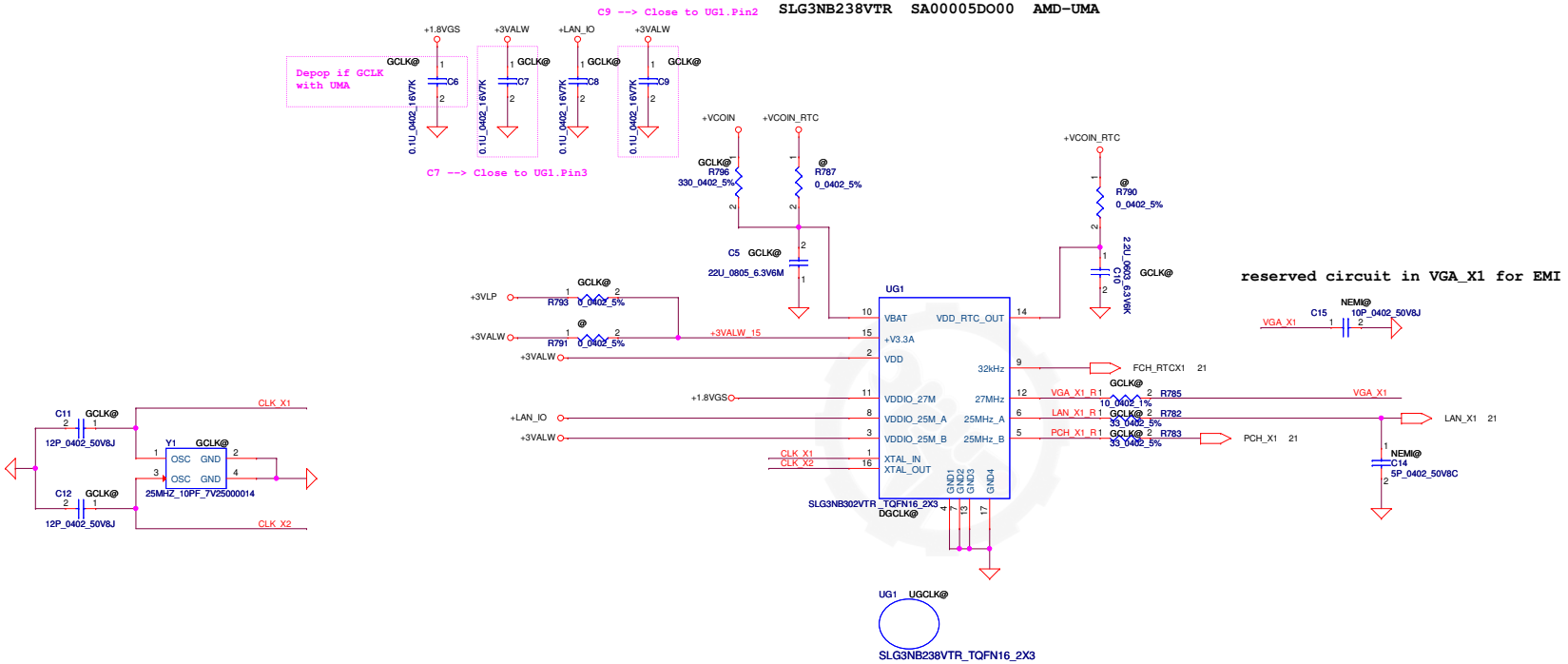
Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **ZAMB0** | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 38 of 50

SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005DO00 AMD-UMA



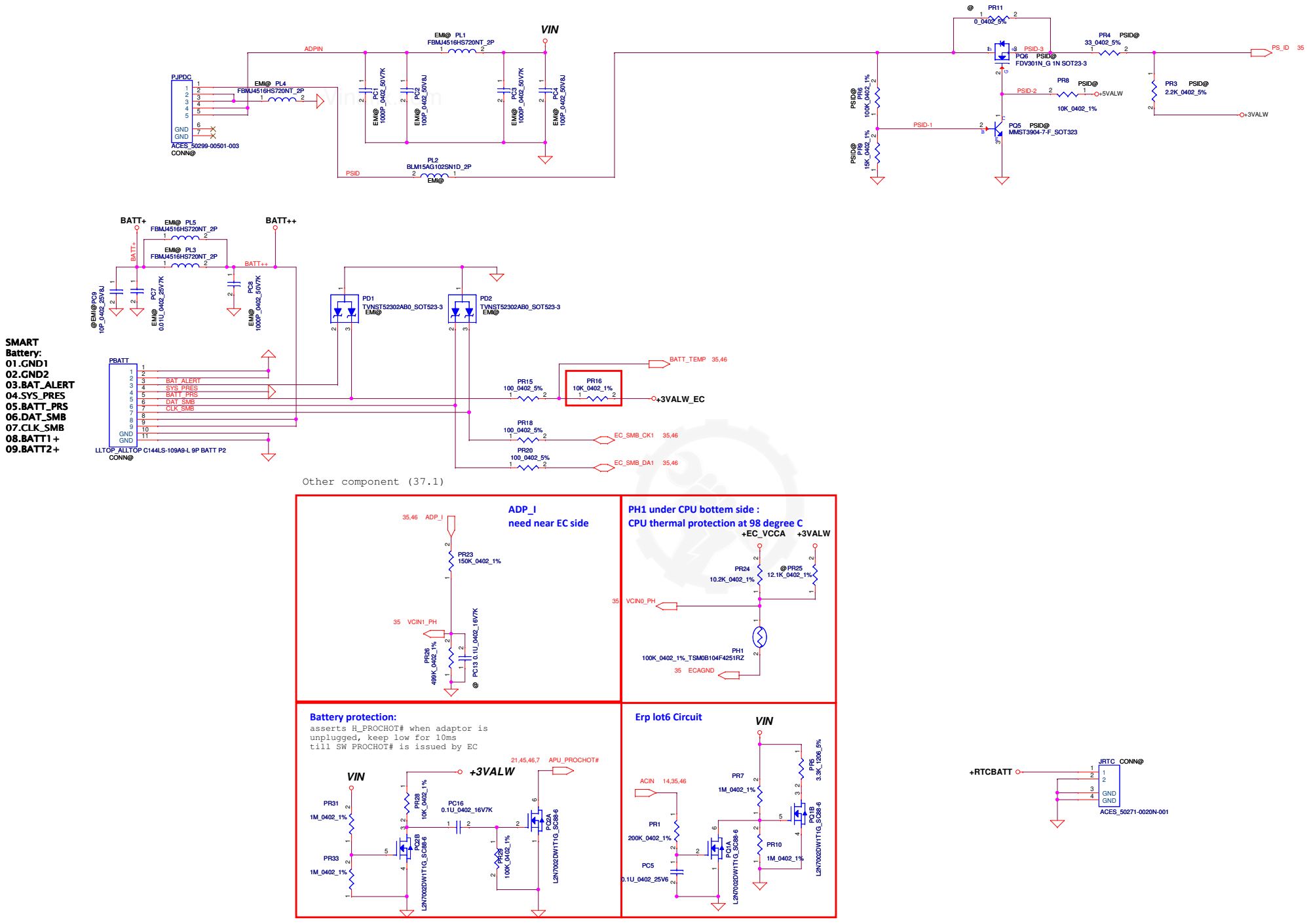
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: GCLK

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 39 of 50



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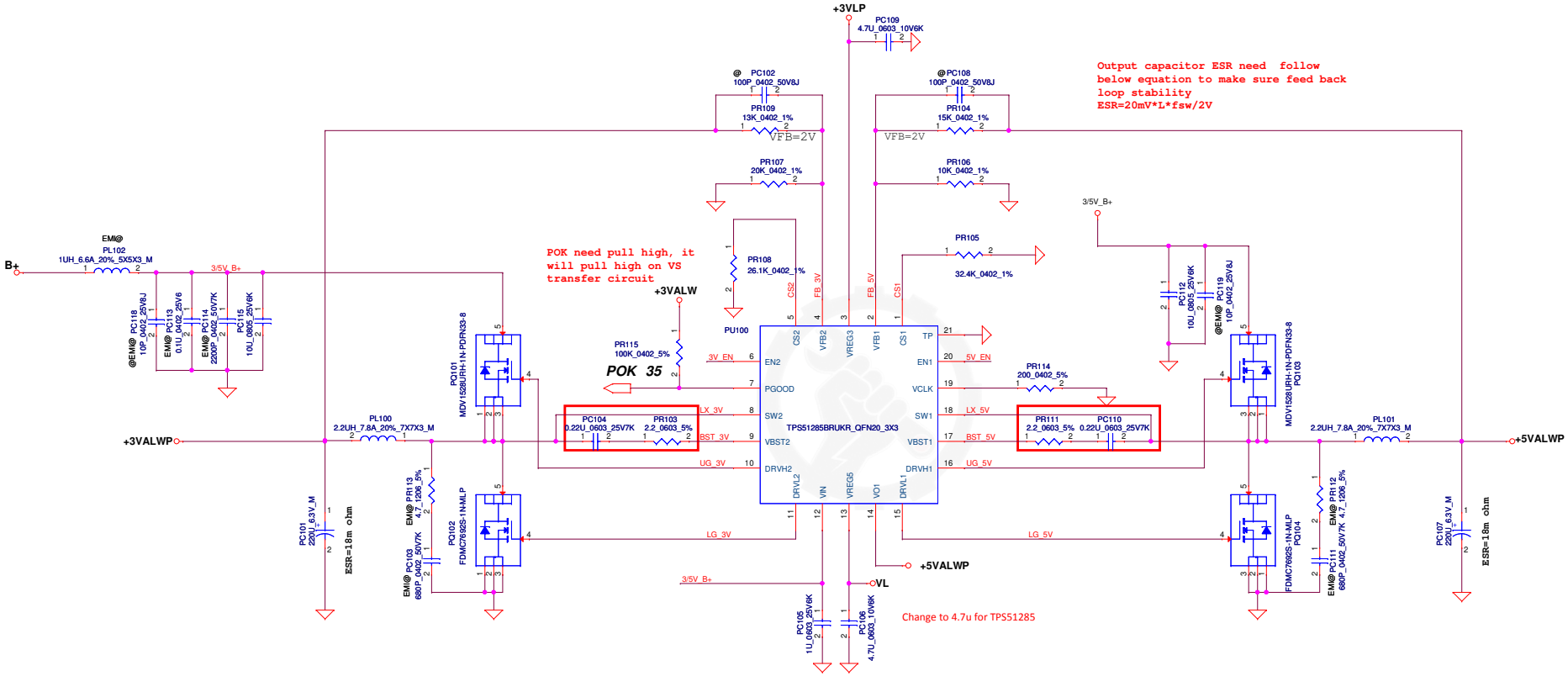
Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

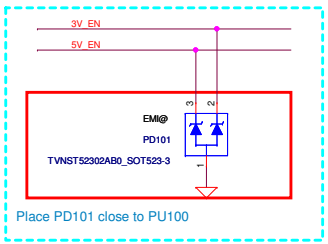
Size	Document Number	Rev
	ZAMB0	0.1

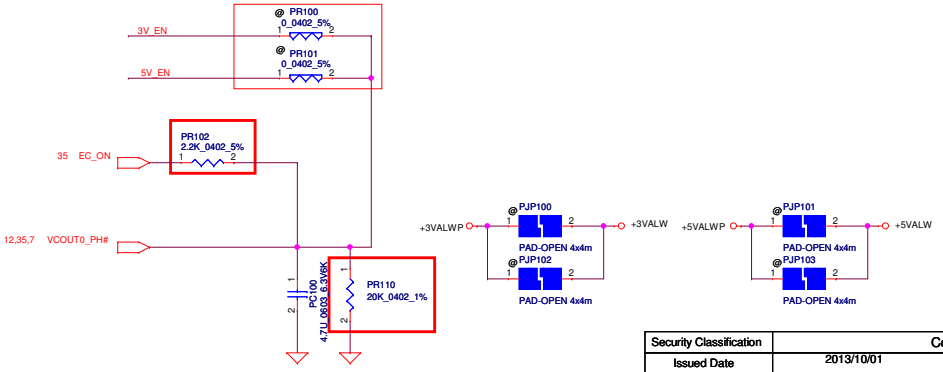
Date: Friday, May 23, 2014 | Sheet 40 of 50



3VALWP
TDC 7.45A
Peak Current 9.34A
OCP current 11.21A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm





5VALWP
TDC 8A
Peak Current 11.42A
OCP current 13.7A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm

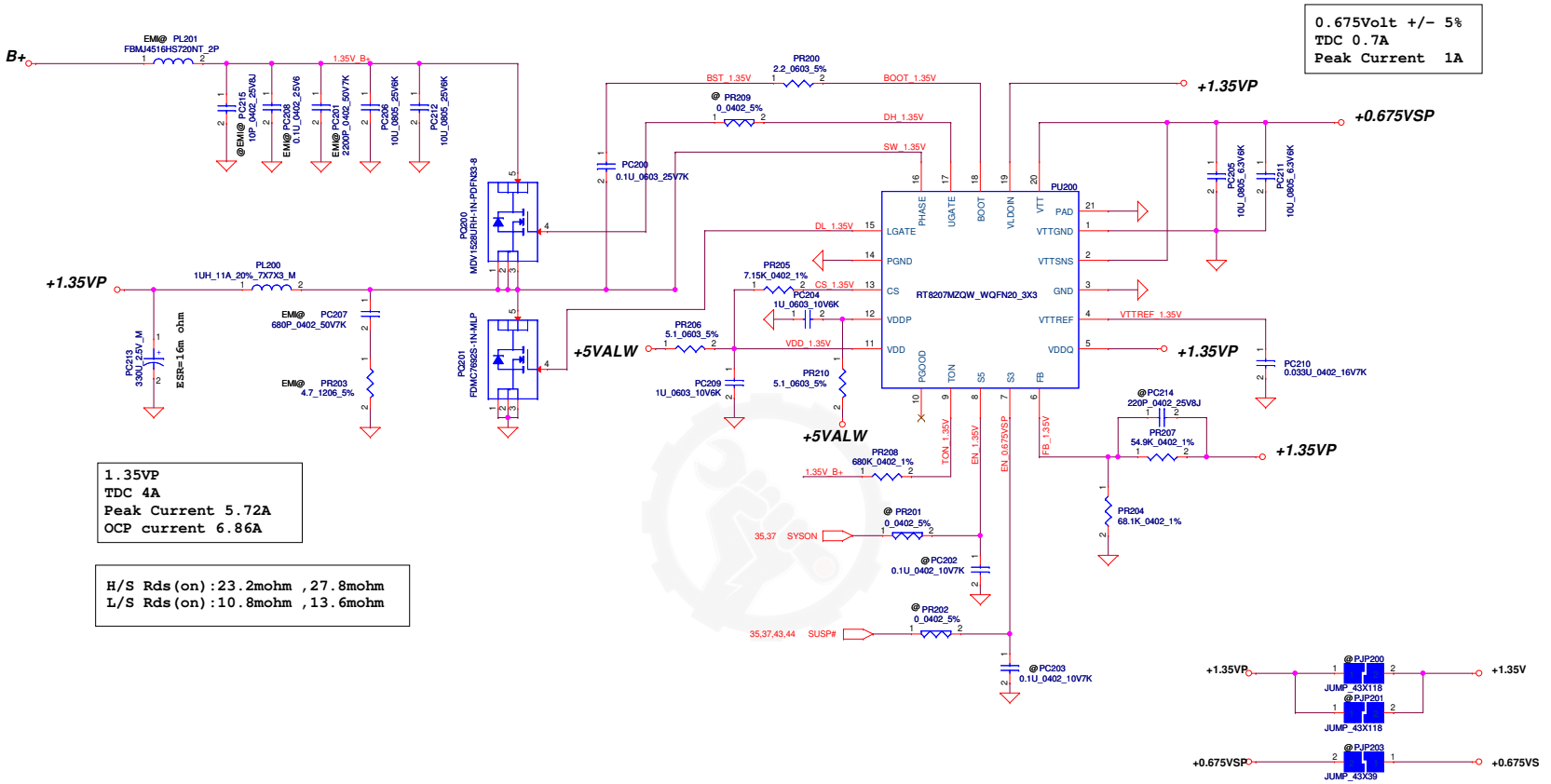
Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, May 23, 2014 | Sheet 41 of 50

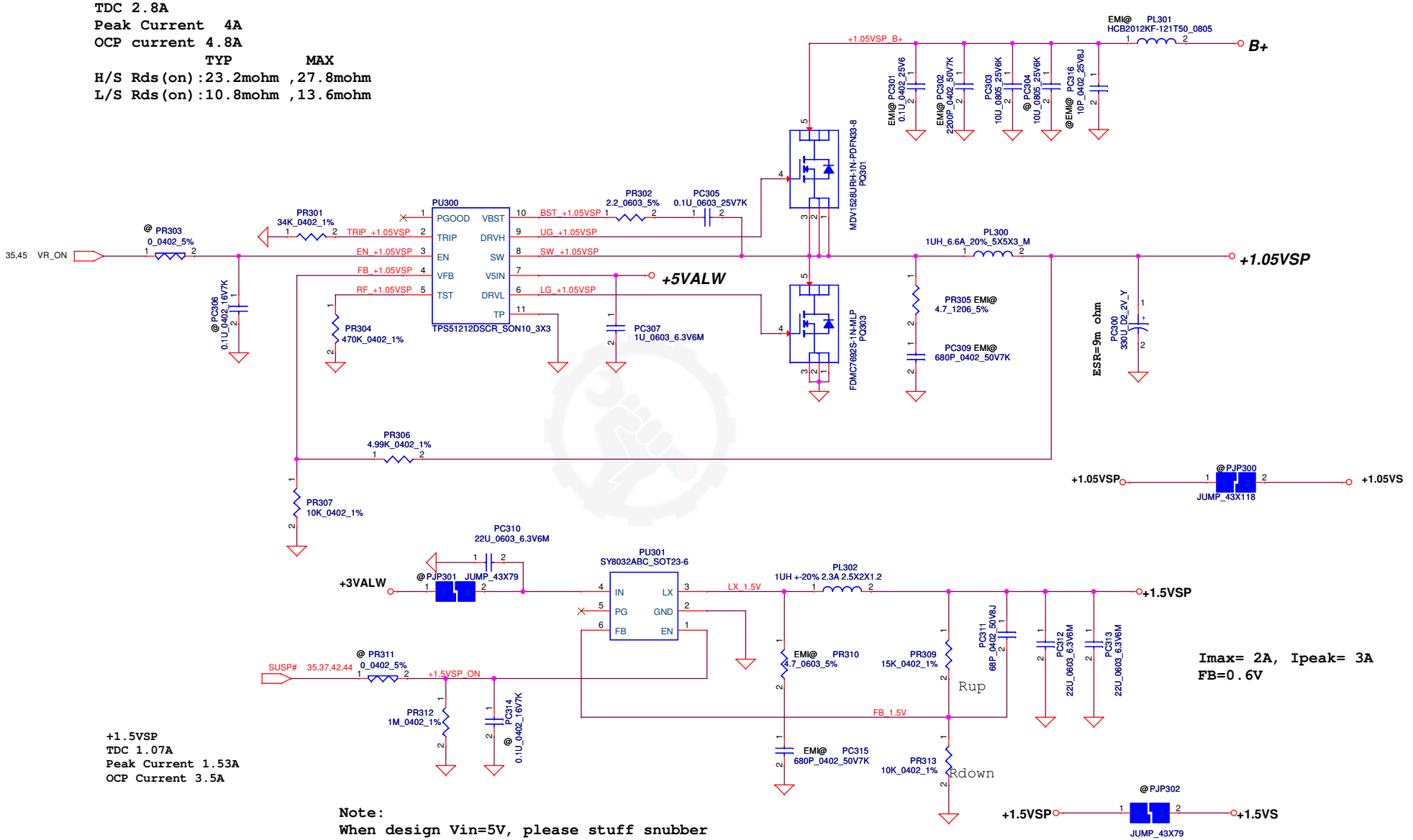


Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title	PWR_+1.35VP/0.675VSP		
Size	Document Number		Rev
	ZAMB0		0.1
Date: Friday, May 23, 2014	Sheet 42 of 50		

1.05VSP
TDC 2.8A
Peak Current 4A
OCP current 4.8A

	TYP	MAX
H/S Rds(on):	23.2mohm	27.8mohm
L/S Rds(on):	10.8mohm	13.6mohm



Imax= 2A, Ipeak= 3A
FB=0.6V

+1.5VSP
TDC 1.07A
Peak Current 1.53A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

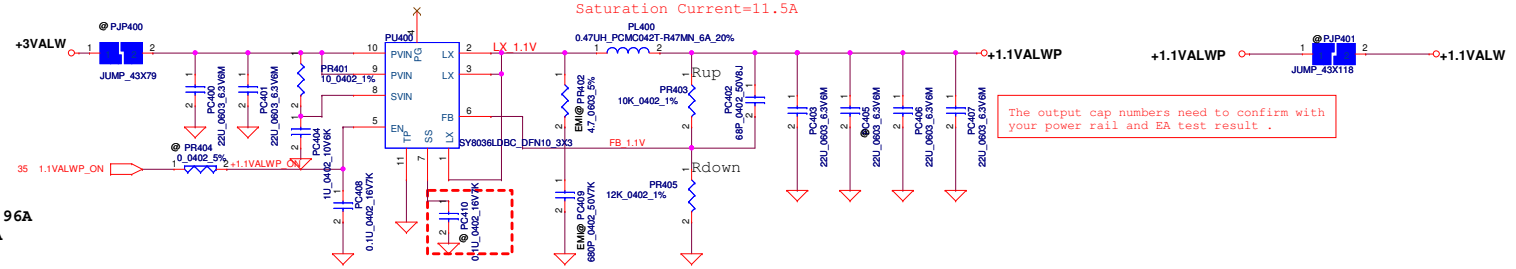
Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	

Title	PWR_+1.05VSP_+1.5VSP		
Size	Document Number		Rev
	ZAMB0		0.1
Date:	Friday, May 23, 2014	Sheet	43 of 50

FB=0.6V
Note:Iload(max)=6A

4*4 DCR 14~15.5mΩ
Heat Rating Current=6A
Saturation Current=11.5A



1.1VALWP
TDC 3.47A
Peak Current 4.96A
OCP current 7.5A

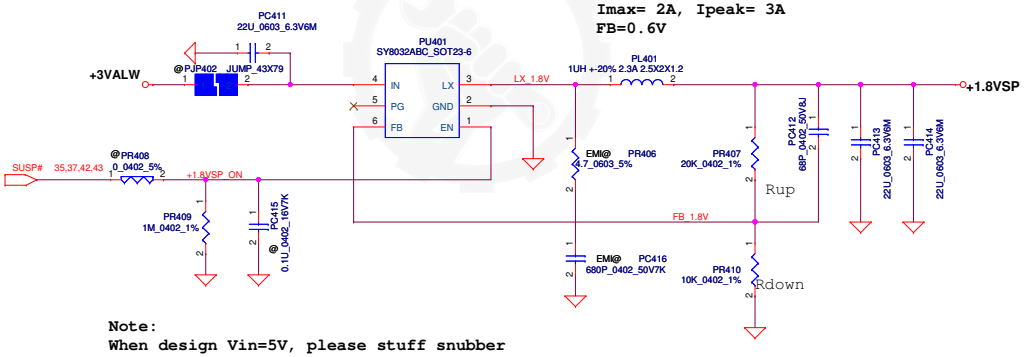
Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

PC7 to set the Soft Start Time:
CSS=100nF 6ms
Without CSS 0.6ms

Vout=0.6V* (1+Rup/Rdown)

Over voltage IC latch off protection threshold
min=115% type=120% max=125 %
Delay time 10us

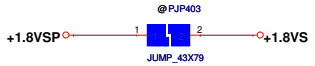
Imax= 2A, Ipeak= 3A
FB=0.6V



+1.8VSP
TDC 1.34A
Peak Current 1.92A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)



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Issued Date	2013/10/01	Deciphered Date 2015/07/08	Title PWR_+1.1ALWP / +1.8VSP
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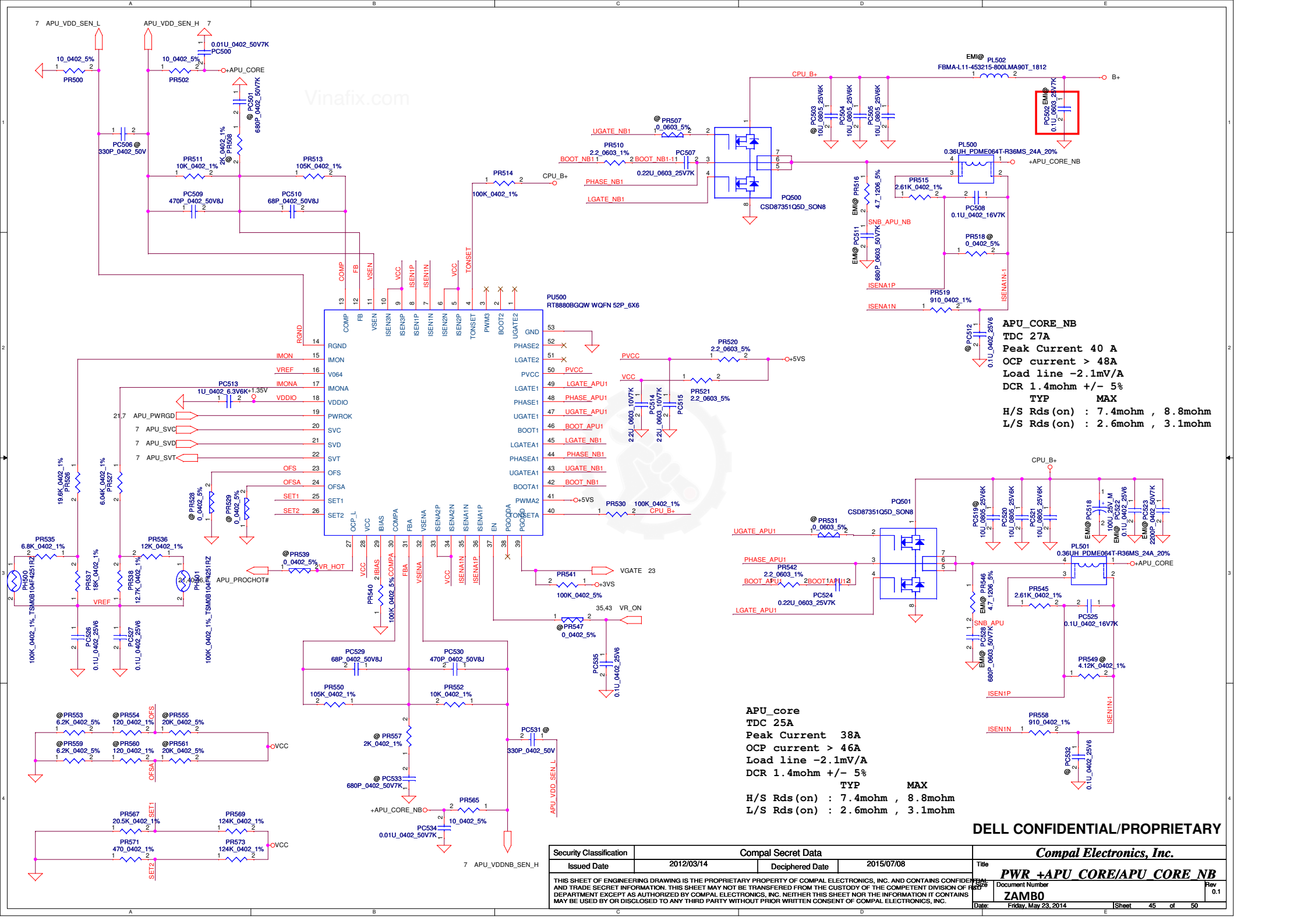
			Date: Friday, May 23, 2014 Sheet 44 of 50


APU_CORE_NB
TDC 27A
Peak Current 40 A
OCP current > 48A
Load line -2.1mV/A
DCR 1.4mohm +/- 5%
TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm
APU_core
TDC 25A
Peak Current 38A
OCP current > 46A
Load line -2.1mV/A
DCR 1.4mohm +/- 5%
TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm
PU500
RT8880BGQW WQFN 52P_6X6
PQ500
CSD87351Q5D_SON8
PQ501
CSD87351Q5D_SON8
PL500
0.36UH_PDME064T-R36MS_24A_20%
PL501
0.36UH_PDME064T-R36MS_24A_20%
PL502
FBMA-L11-453215-800LMA90T_1812
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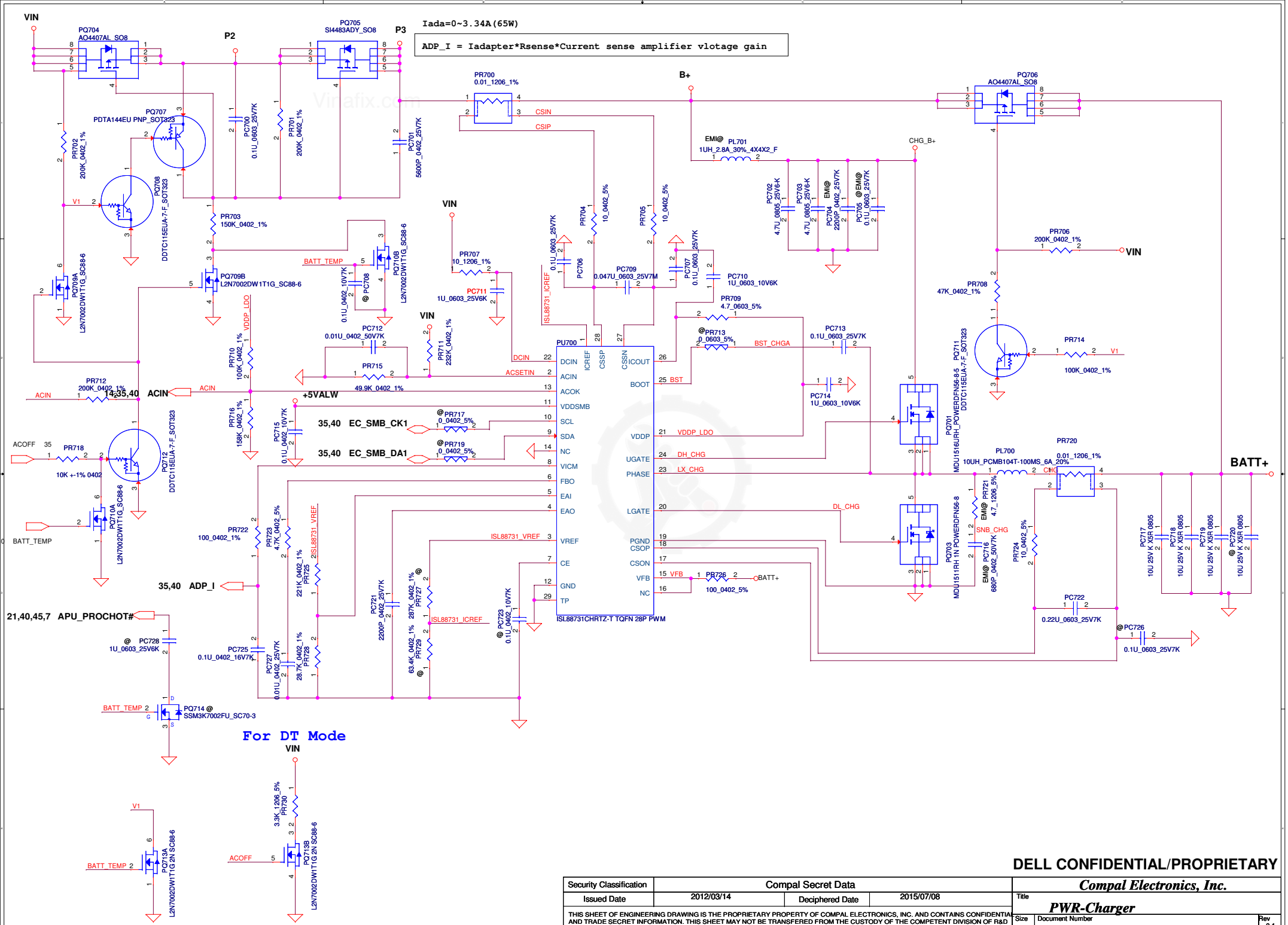
Compal Electronics, Inc.
PWR_+APU_CORE/APU_CORE_NB
ZAMB0
Rev 0.1
Friday, May 23, 2014
Sheet 45 of 50
Security Classification Compal Secret Data
Issued Date 2012/03/14
Deciphered Date 2015/07/08



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Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2015/07/08

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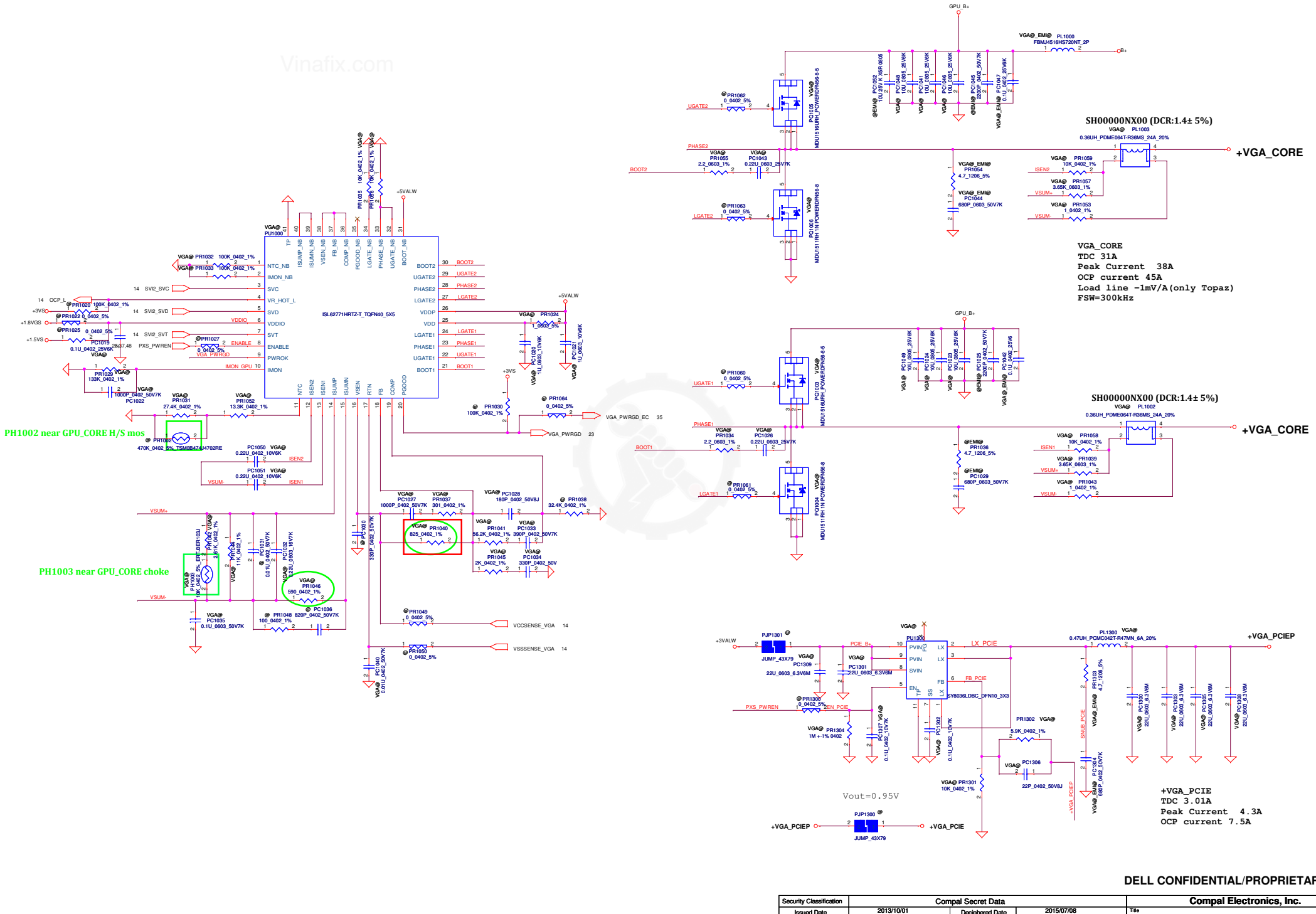
Compal Electronics, Inc.		
Title: PWR-Charger		
Size	Document Number: ZAMB0	Rev: 0.1
Date: Friday, May 23, 2014	Sheet 46 of 50	


GPU_B+
VGA@_EMI@ PL1000 FBMJ4516HS720NT_2P
B+
SH00000NX00 (DCR:1.4± 5%)
VGA@ PL1003 0.36UH_PDME064T-R36MS_24A_20%
+VGA_CORE
VGA_CORE
TDC 31A
Peak Current 38A
OCP current 45A
Load line -1mV/A(only Topaz)
FSW=300kHz
ISL62771HRTZ-T_TQFN40_5X5
PH1002 near GPU_CORE H/S mos
PH1003 near GPU_CORE choke
SH00000NX00 (DCR:1.4± 5%)
VGA@ PL1002 0.36UH_PDME064T-R36MS_24A_20%
+VGA_CORE
PJP1301
JUMP_43X79
PU1300
SY8036LDBC_DFN10_3X3
PL1300 0.47UH_PCMC042T-R47MN_6A_20%
+VGA_PCIEP
Vout=0.95V
+VGA_PCIEP
TDC 3.01A
Peak Current 4.3A
OCP current 7.5A
DELL CONFIDENTIAL/PROPRIETARY
Security Classification
Compal Secret Data
Issued Date
2013/10/01
Deciphered Date
2015/07/08
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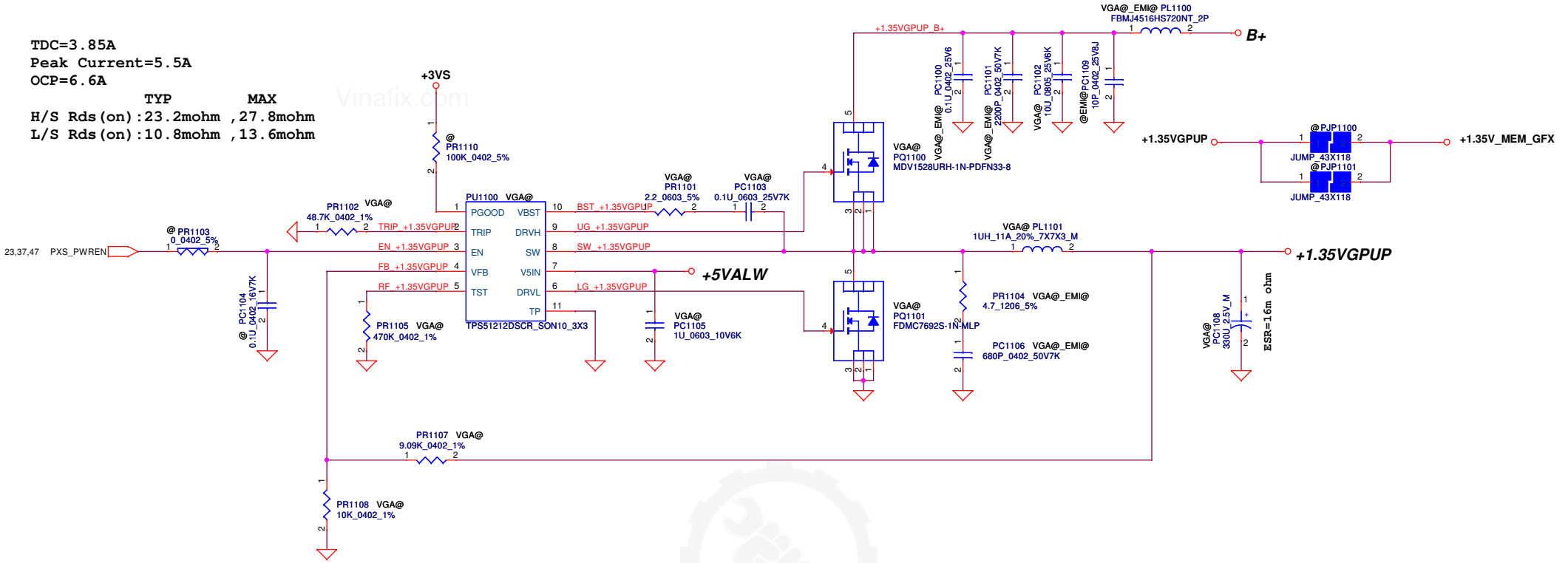
TDC=3.85A
Peak Current=5.5A
OCP=6.6A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm



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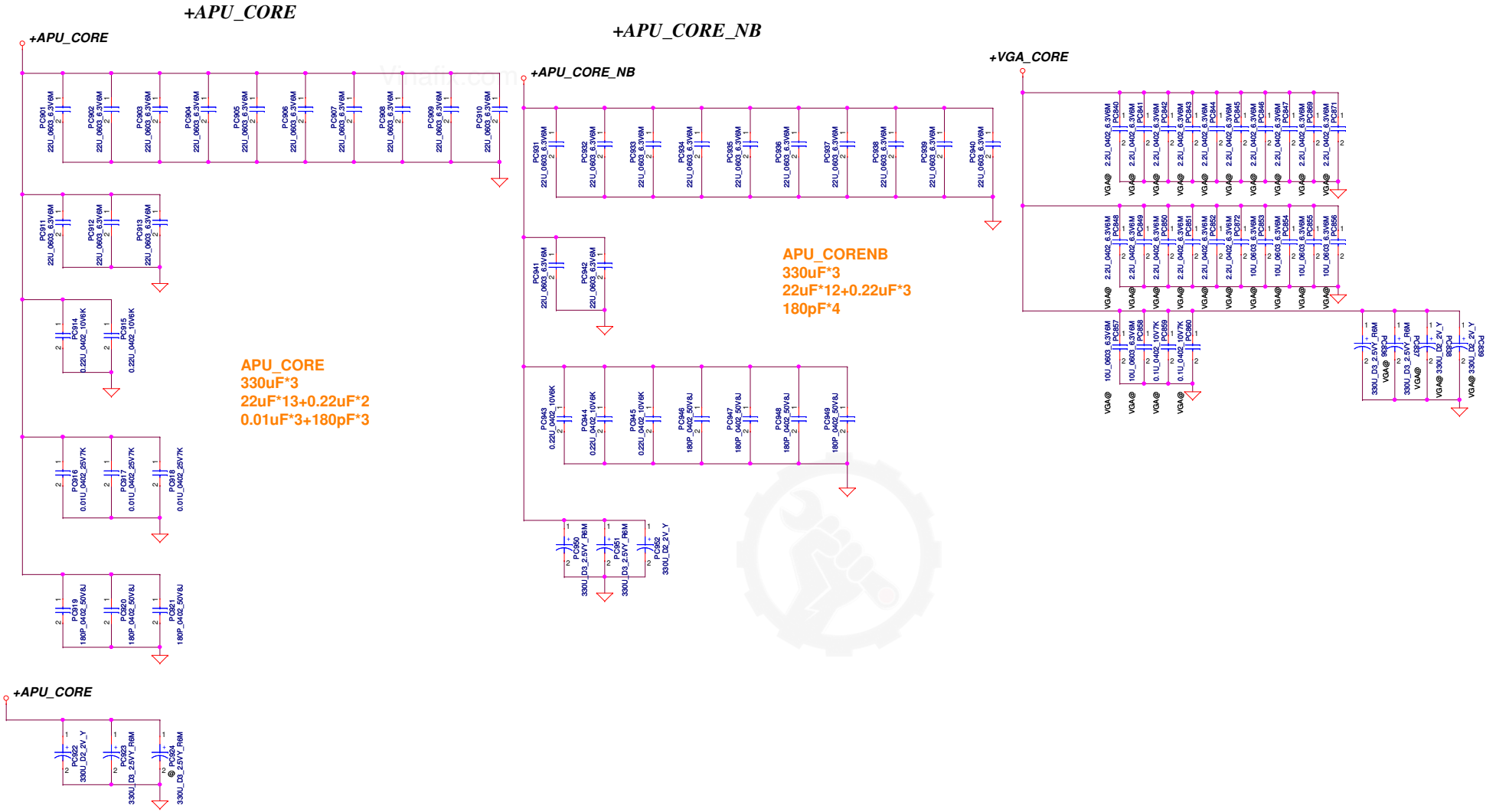

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