Schematic Page Description :

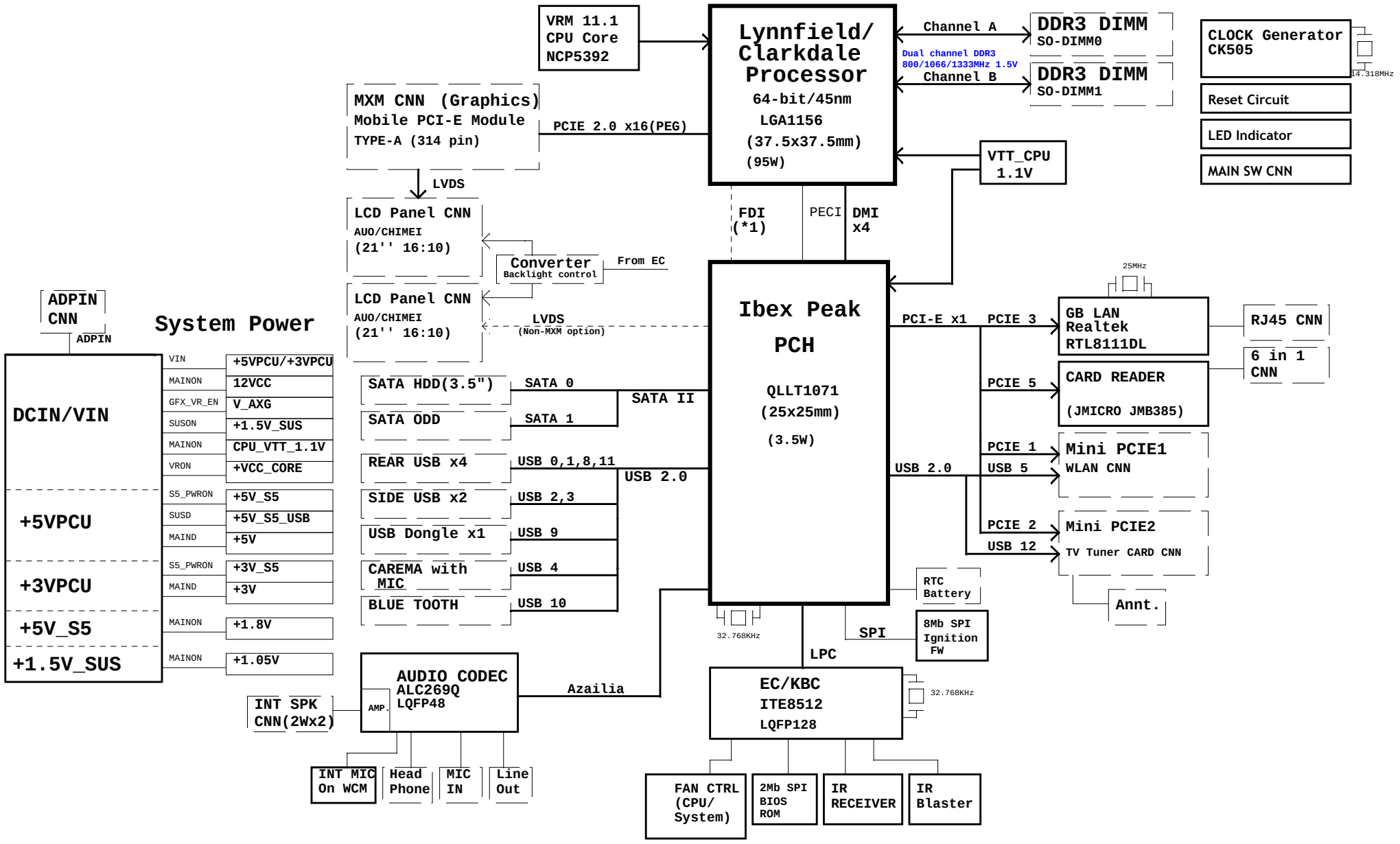
01 -- Page Description
02 -- System Block Diagram
03 -- Power Map
04 -- Power Sequence 1/2
05 -- Power Sequence 2/2
06 -- Clock
07 -- SMBus Block Diagram
08 -- GPIO list
09 -- CLOCK GENERATOR
10 -- MCP 1/7(CLK/CTRL/MISC)
11 -- MCP 2/7(DDR3 CHANNEL A)
12 -- MCP 3/7(DDR3 CHANNEL B)
13 -- MCP 4/7(PCIE/DMI)
14 -- MCP 5/7(VCCP)
15 -- MCP 6/7(MISC/VCC)
16 -- MCP 7/7(GND)
17 -- DDR3 CHA DIMM0
18 -- DDR3 CHB DIMM0
19 -- PCH 1/6 (DMI/FDI/VIDEO)
20 -- PCH 2/6(SATA/RTC/HDA/LPC)
21 -- PCH 3/6(PCIE/USB/CLK/NV)
22 -- PCH 4/6(GPIO/CPU)
23 -- PCH 5/6(POWER)
24 -- PCH 6/6(GND)
25 -- MXM 3.0
26 --AUDIO CODEC ALC269
27 --LINE OUT/CRT
28 --JMB380 (Card Reader/1394)
29 -- SATA HDD/ODD
30 --MINI PCIE(WLAN/TV/IR/BT)
31 --ON BOARD USB
32 --LCD PANEL/INVERTER
33 --LAN(RTL8111DL)
34 --LAN Transformer & RJ45
35 --FAN/D board/CCD/PS2
36 -- EC ITE 8512N/FLASH
37 -- XDP
38 -- SCREW HOLE
39 -- ADP AC IN & HDD12V
41 -- V_AXG (ISL6314)
42 -- DDR3 1.5V(TPS51116)
43 -- CPU_VTT(ISL6314CRZ)
44 -- CPU_CORE (NCP5392)
45 --1.05V_PCH, 1.05V_ME,1.8V
46 -- Discharge Circuit
47 -- CHANGE LIST1
48 -- CHANGE LIST2
49 -- ANNOTATIONS

Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	Page Description	A

Date: Tuesday, March 16, 2010 Sheet 1 of 49

Block Diagram :



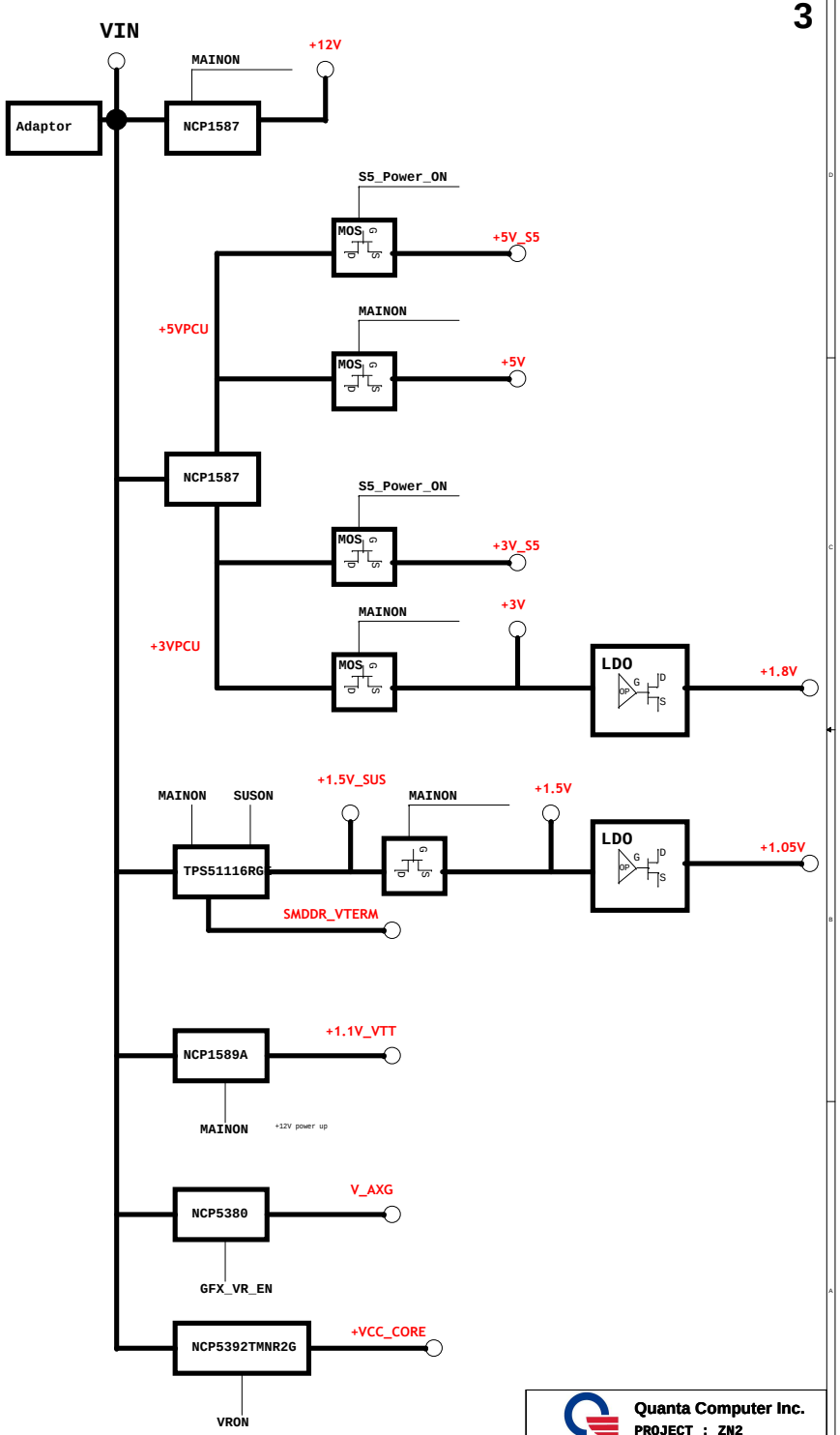
(*1)FDI - Used only for the Clarkdale processor.

Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	Block Diagram	A

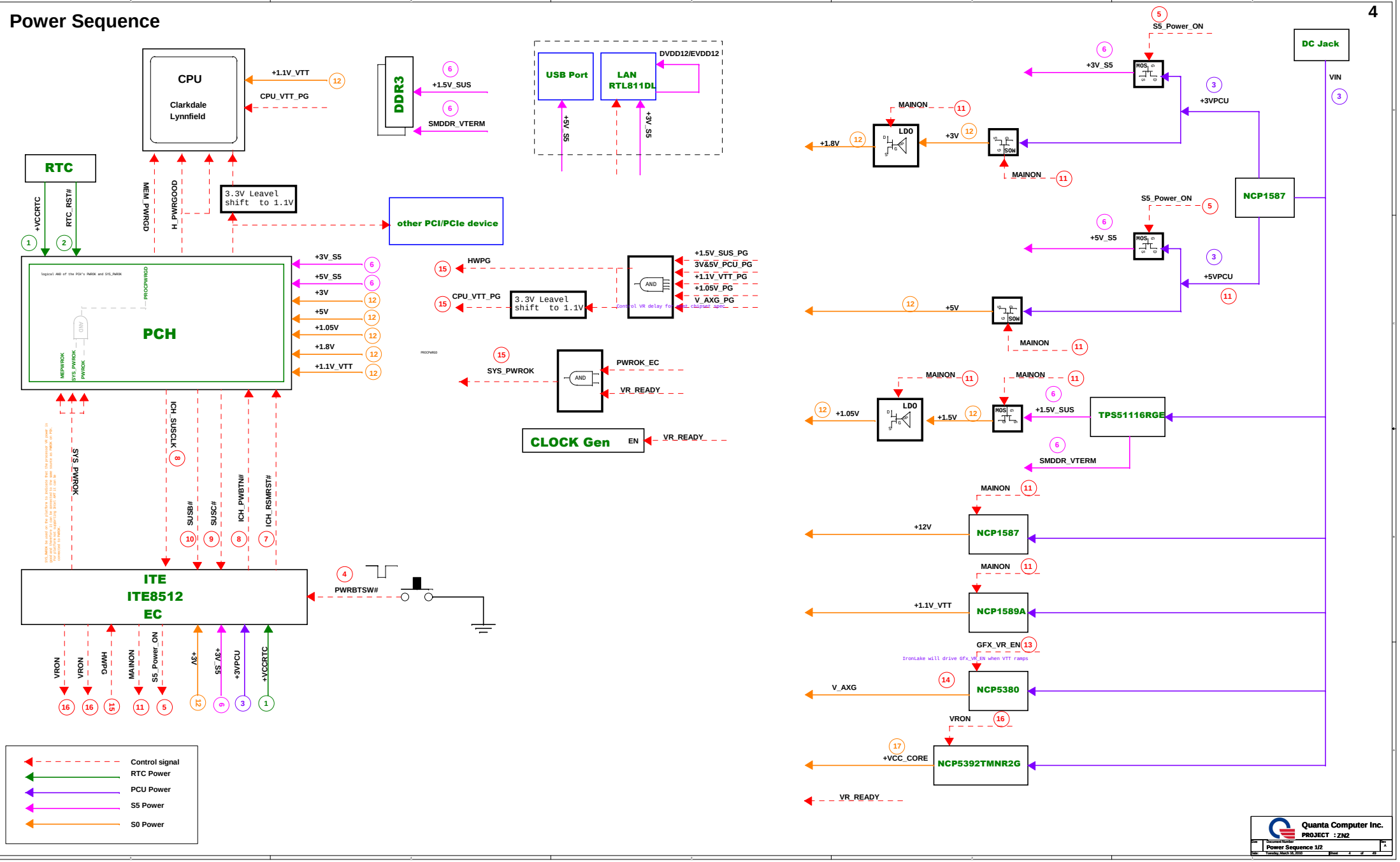
Date: Tuesday, March 16, 2010 Sheet 2 of 49

Power Rail	Destination	Voltage	S0 Current
+VCC_CORE	Lynnfield : Default for initial power up	0.65V~1.4V 1.1V	90A(TDC)
V_AXG	for 92W TDP SKU for 79W TDP SKU	0.5~1.3V	10A (TDC) 16A (TDC)
+1.1V_VTT	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V~1.1V~1.155V 1.1V 1.05V~1.1V~1.16V	30A(TDC) 0.065A 0.001A
+1.8V	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F	1.71V~1.8V~1.89V 1.71V~1.8V~1.89V 1.71V~1.8V~1.89V	1.1A 0.196A 0.156A
+1.5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V~1.5V~1.575V	6A
SMDDR_VTERM	DDRIII Terminator:	0.75V	2A
+1.05V	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power	0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V	1.629A 3.251A 0.065A 0.075A 0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)		
+3V	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CH7308 : LVDD ALC662 : DVDD Mini PCIE : +3.3V(WLAN) CAREMA	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.357A 0.069A
+5V	Ibex Peak : Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) ALC662S : AVDD Touch Screen LCD Panel USB: x 12 ports	4.75V~5V~5.25V 5V	0.001A 6A
MXM_12V HDD_12V			
+3V_S5	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN 82578DM : VDD CLK Gen.CK505 : VDD EC(IT8512) : VSTBY SPI FLASH ROM	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.086A 0.168A 0.006A
+5V_S5	Ibex Peak : Suspend well Ref. Voltage	4.75V~5V~5.25V	0.001A
	INVERTER : Vin FAN_CPU		
+3VPCU			
+5VPCU			
15VPCU			
VIN			



Quanta Computer Inc.
PROJECT : ZN2
Size | Document Number: Power Map | Rev: A
Date: Tuesday, March 16, 2010 | Sheet 3 of 49

Power Sequence



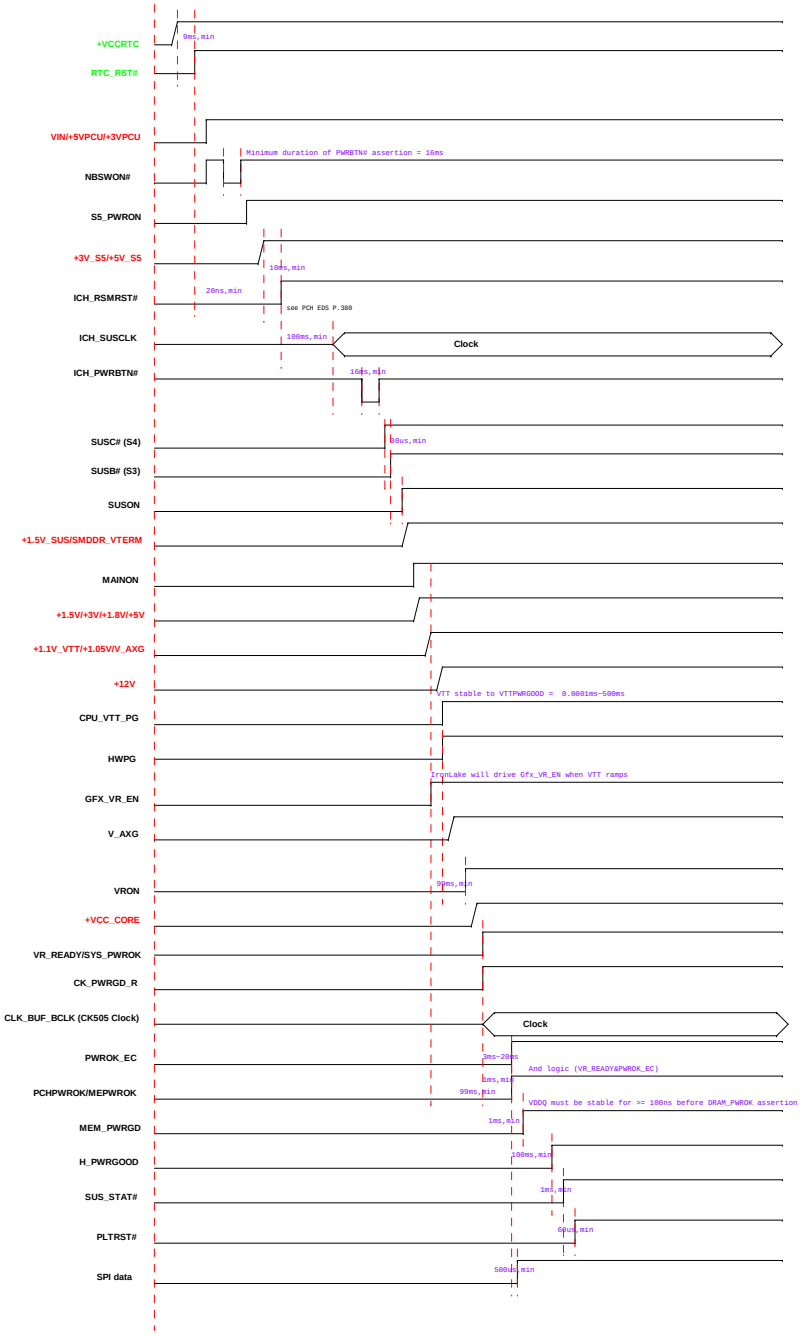
Quanta Computer Inc.
PROJECT : ZN2
Power Sequence 1/2

POWER SEQUENCE

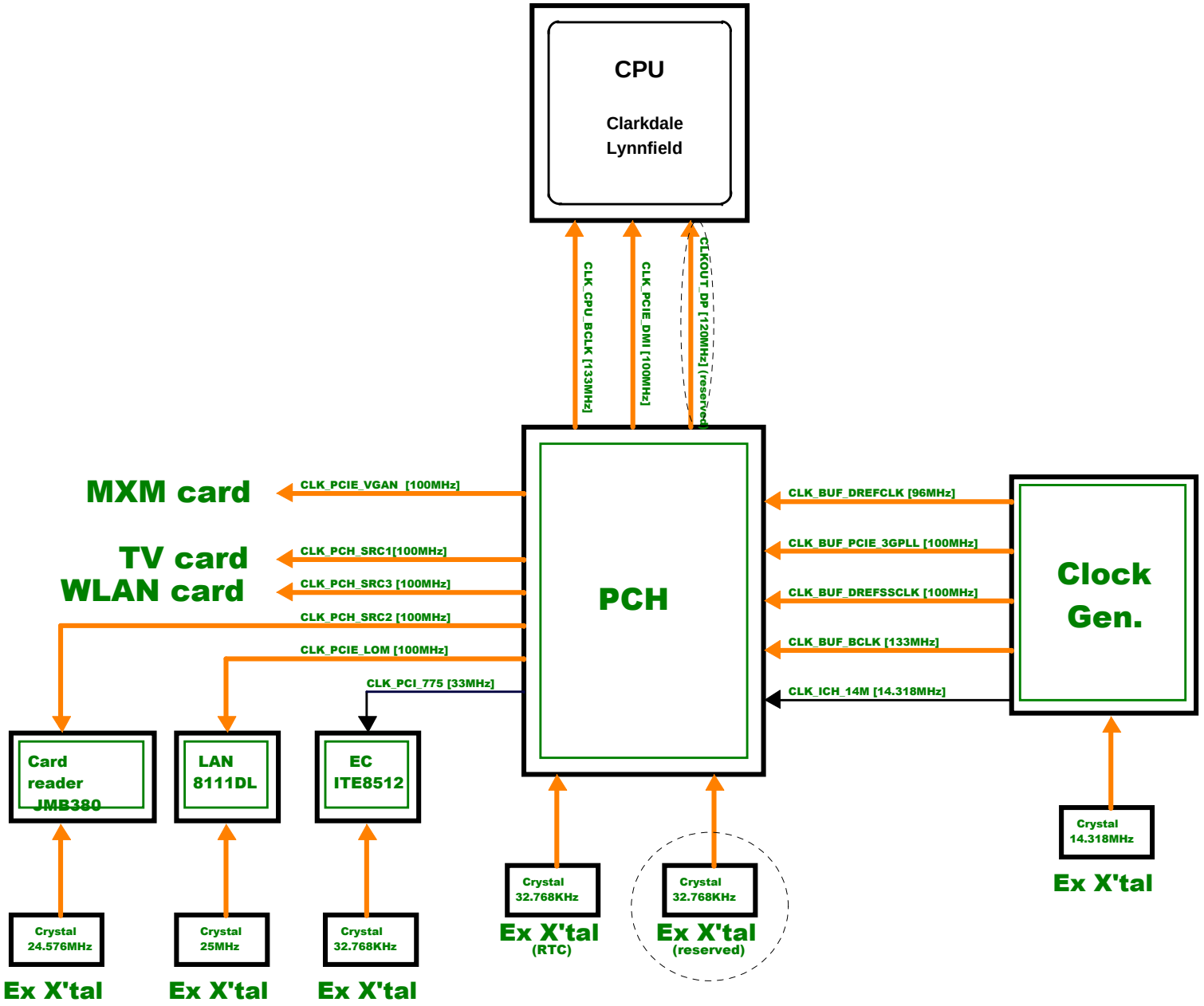
Voltage Rails

Power	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal	
+VCCRTC	3V	ON	ON	ON	ON	ON	ON		
VIN	19.5V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+5VPCU	5V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+3VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adaptor in	EC
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_PWRON	PCH SUS,
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_PWRON	Sys Management, PCH Resume Well, Intel HD Audio, USB, WLAN,
+1.5V_SUS	1.5V	ON	ON	OFF	OFF	OFF	OFF	SUSON	DDR3 Memory
SMDDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	OFF	SUSON	DDR3 Memory
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	SATA, PCI REF
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	PCI Express*, SATA, HV CMOS,CRT, Band Gap voltages, Intel HD Audio
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	mini PCIe, Intel HD Audio
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	PCH core, PCH PLL voltages, PCH CLK Buffer, SATA, USB, PCH fuse,Display Link, Display Port, PCIe
+1.8V	1.8V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	LVDSIO, SFR, FLASH
+1.1V_VTT	1.1V / 1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	CPU VTT, FDLPEG, DMI, VCCTTADDR, PCH DMI,PCH V_CPU_IO
V_AXG	???V	ON	OFF	OFF	OFF	OFF	OFF	GFX_VR_EN	mini PCIe, Intel HD Audio
+VCC_CORE	???V	ON	OFF	OFF	OFF	OFF	OFF	VRON	CPU Core

Power	Voltage	S0	S3	S4	S5	PCU	G3	
VIN_MXM								
+5V_MXM								
+3V_MXM								
USBVCC2								
3VPCU_EC								
LCDVCC								
CCD_PWR								
VIN_LCD								
VDDA_CODEC								



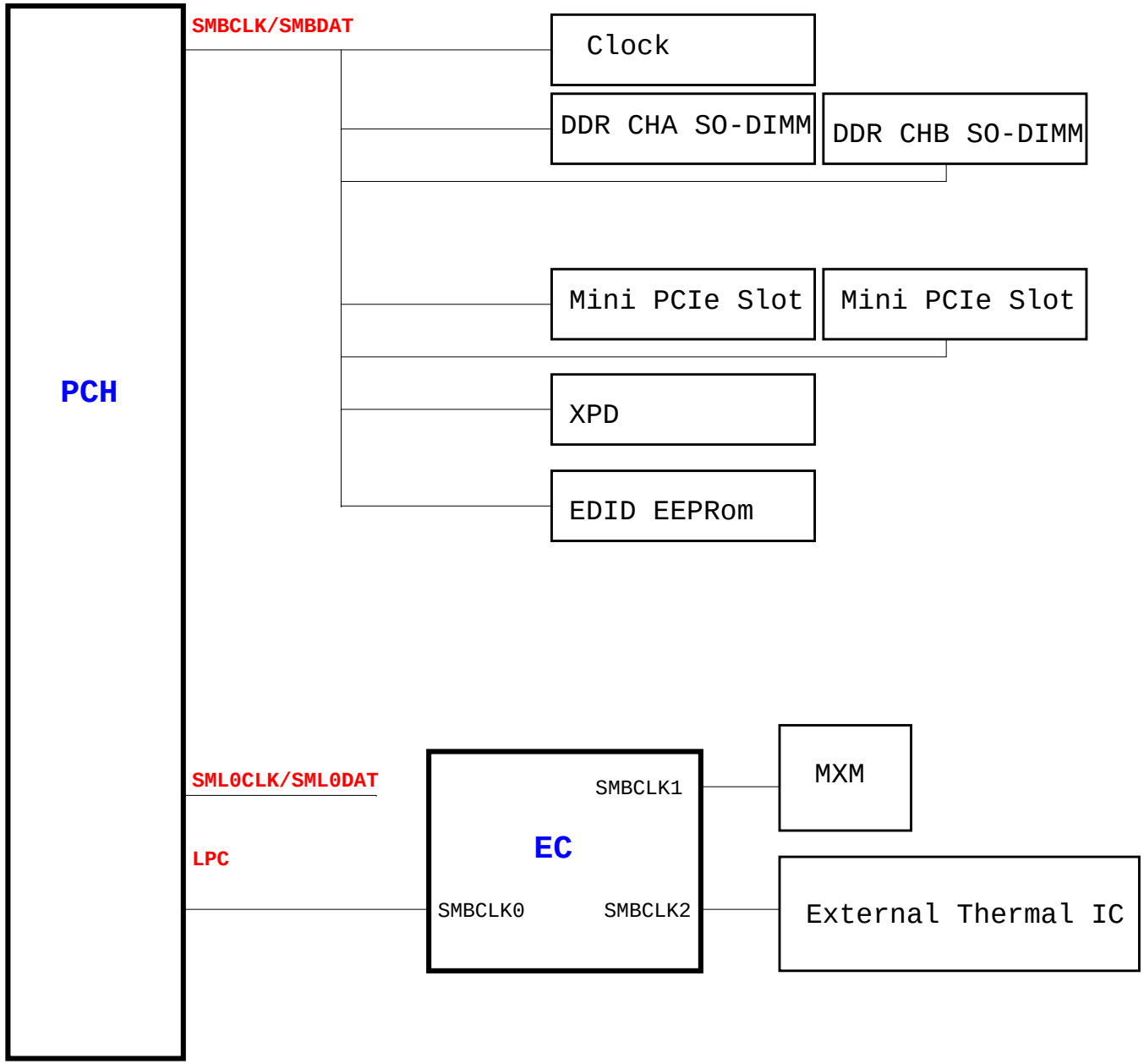
Quanta Computer Inc.
PROJECT : ZIH2
Power Sequence 2/2
Rev A
Date: Tuesday, March 16, 2010 Sheet 5 of 49



Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	Clock	A

Date: Tuesday, March 16, 2010 Sheet 6 of 49



Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	SMBus Block Diagram	A

Date: Tuesday, March 16, 2010 Sheet 7 of 49

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

Quanta Computer Inc.
PROJECT : ZN2

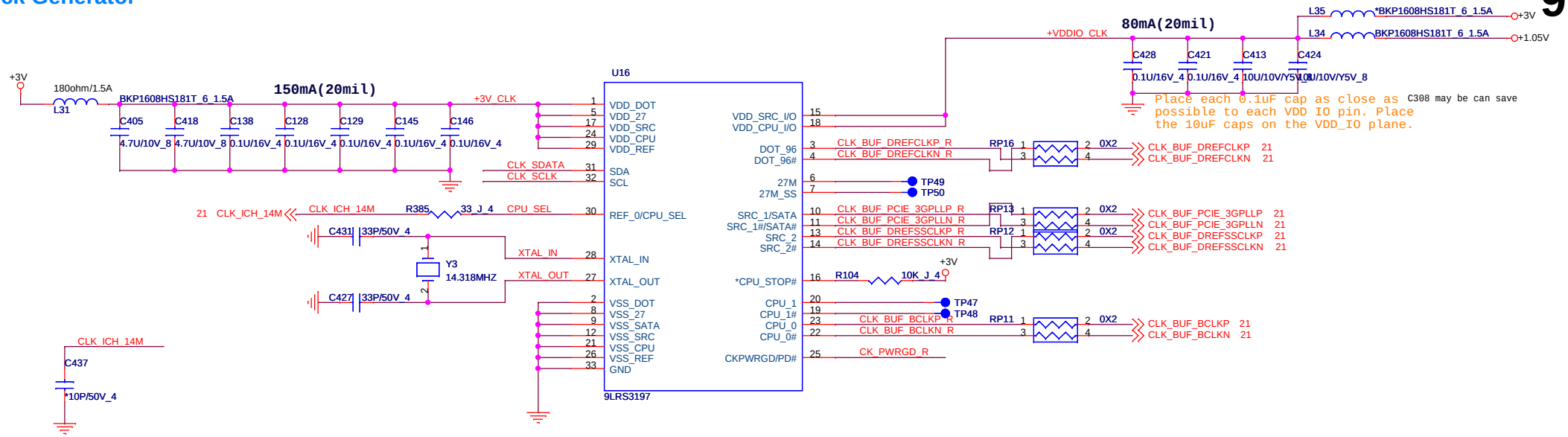
Size	Document Number	Rev
	GPIO List	A

Date: Tuesday, March 16, 2010 Sheet 8 of 49

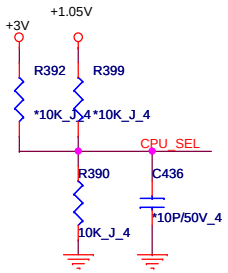
Clock Generator

1.05V to 3.3V from external power supply

9

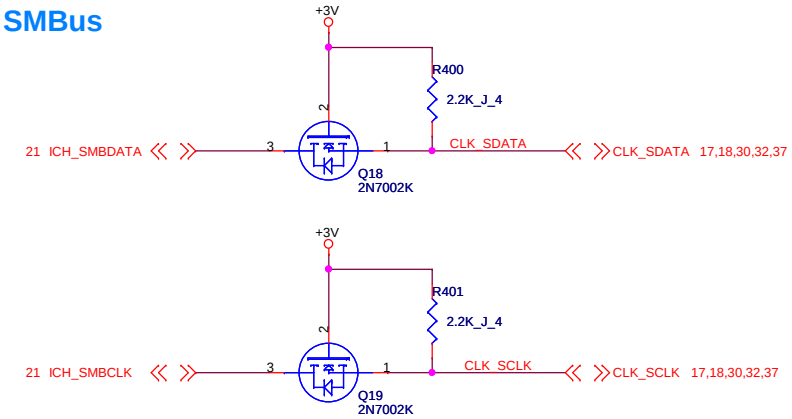


CPU_CLK select

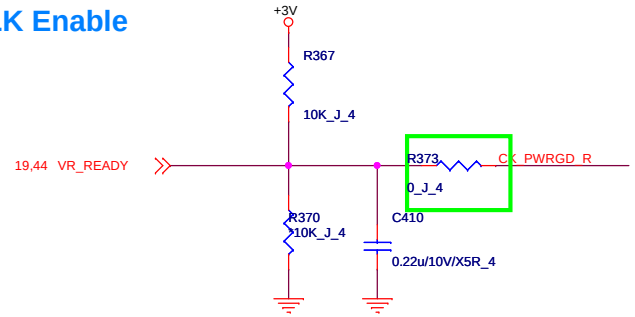


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



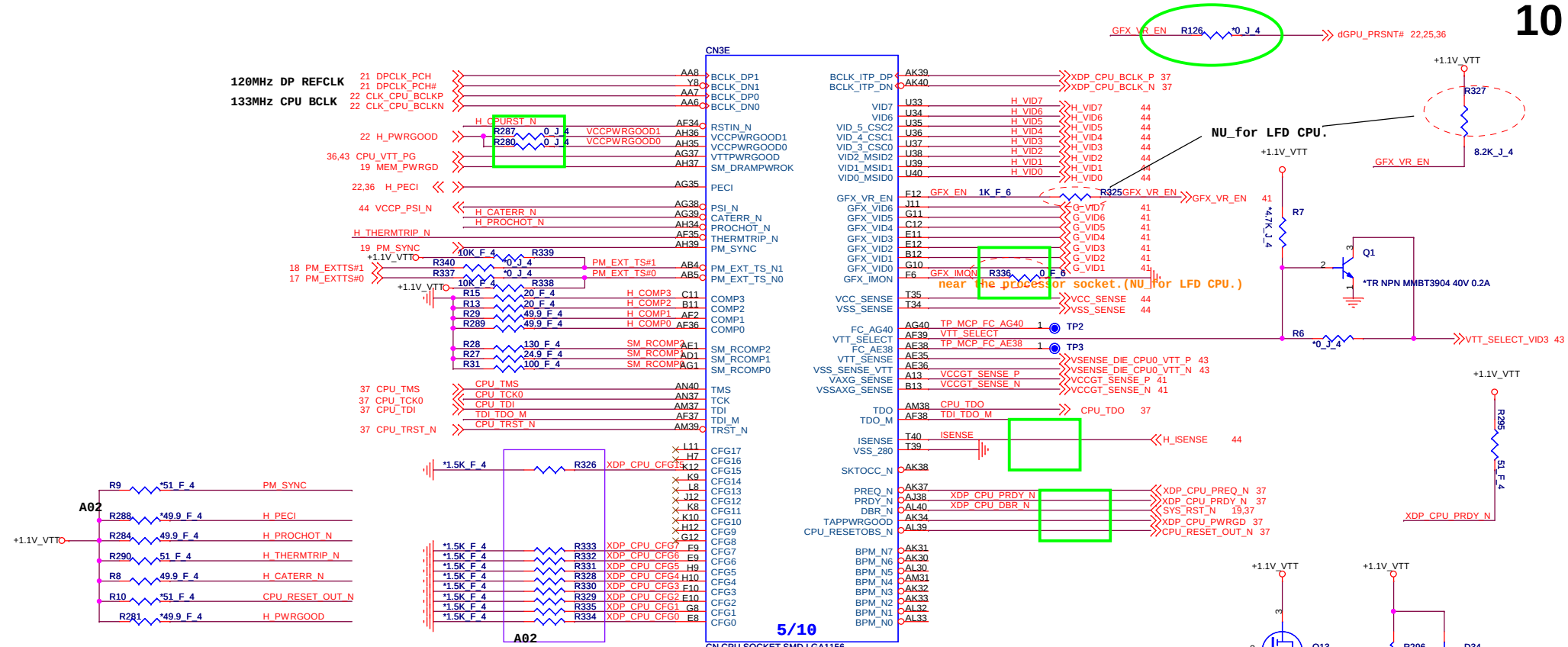
CLK Enable



Quanta Computer Inc.

PROJECT : ZN2

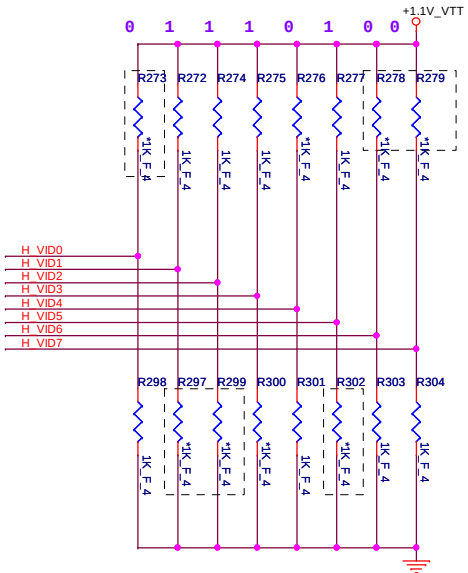
Size	Document Number	Rev
	Clock Generator	A
Date: Tuesday, March 16, 2010	Sheet 9 of 49	



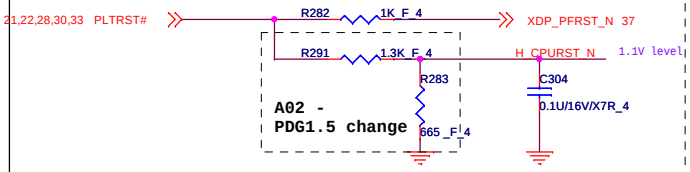
CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

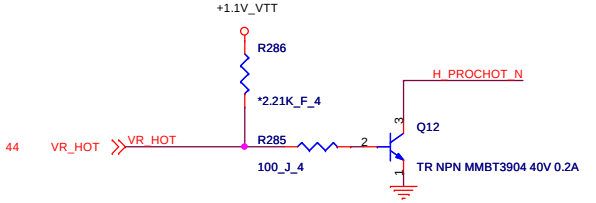
VID[7:0] : 00101110 =>1.325V@VCC,Max
2009B FMB processors supported



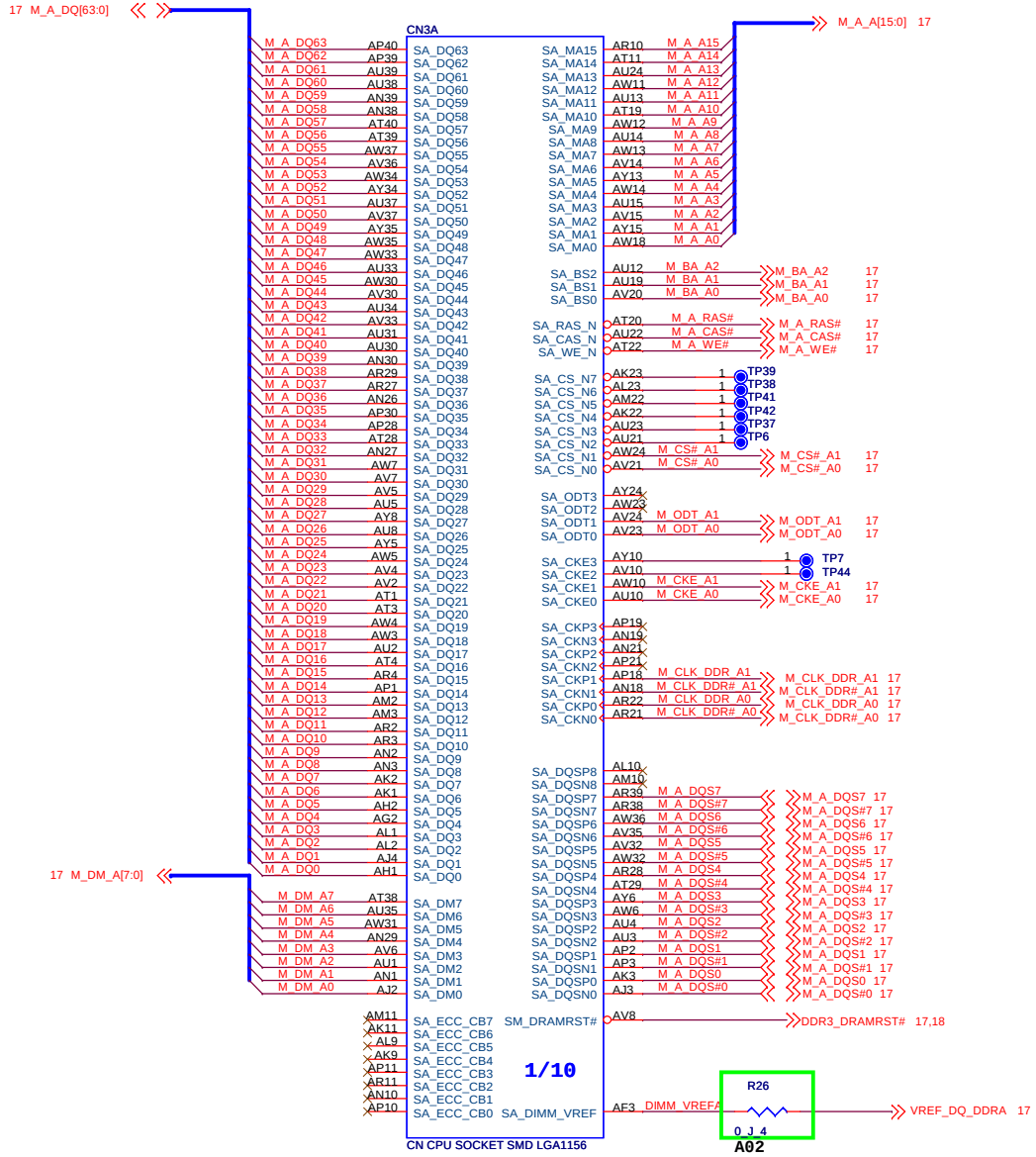
Need to be placed close to processor
to minimize ESD risk



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU



Quanta Computer Inc. PROJECT : ZN2			
Size	Document Number: MCP (CLK/CTRL/MISC)		Rev A
Date: Tuesday, March 16, 2010	Sheet 10 of 49		

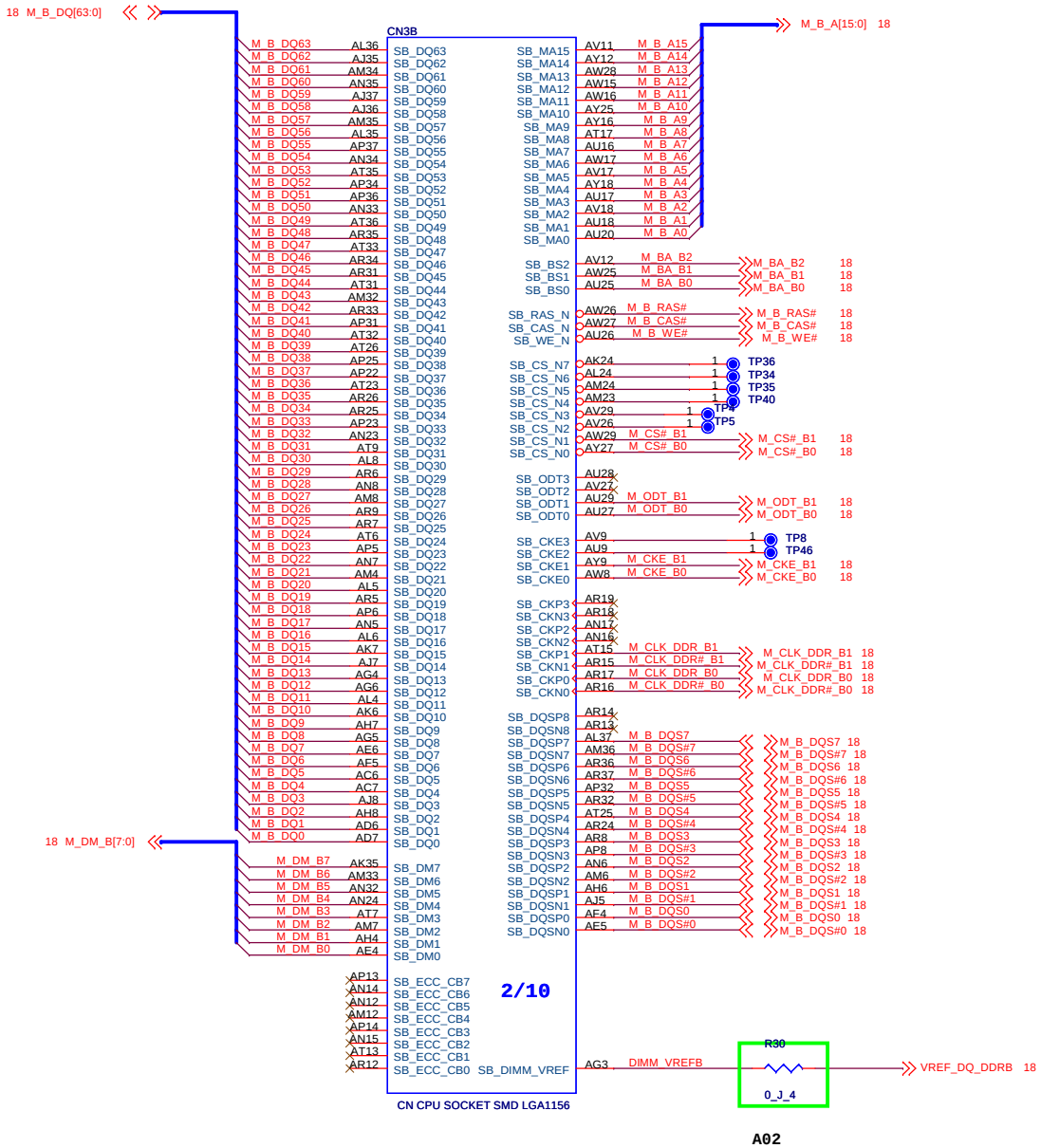


Quanta Computer Inc.

PROJECT : ZN2

Size	Document Number	Rev
	MCP (DDR3 CHANNEL A)	A

Date: Tuesday, March 16, 2010 Sheet 11 of 49

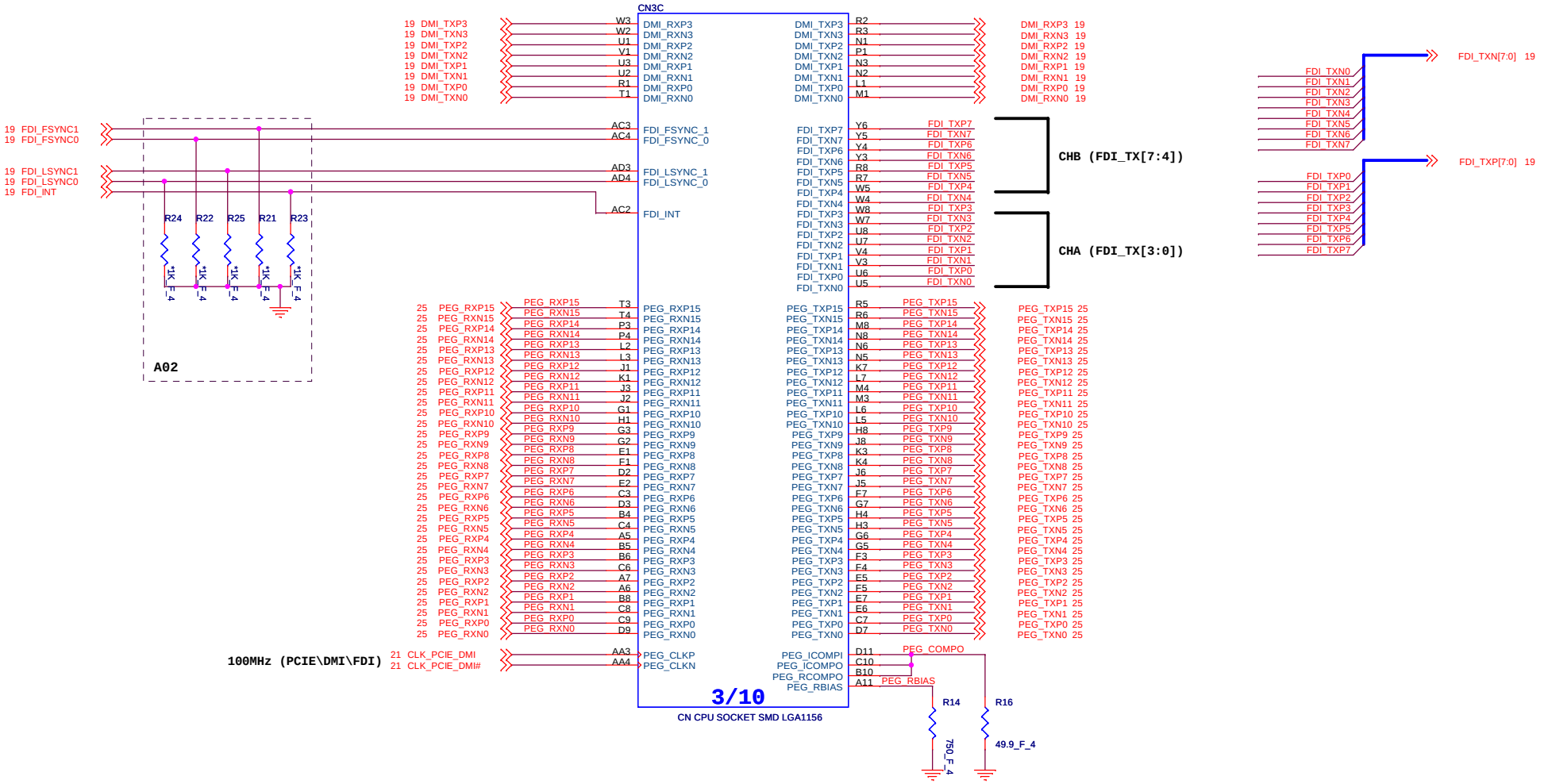


Quanta Computer Inc.

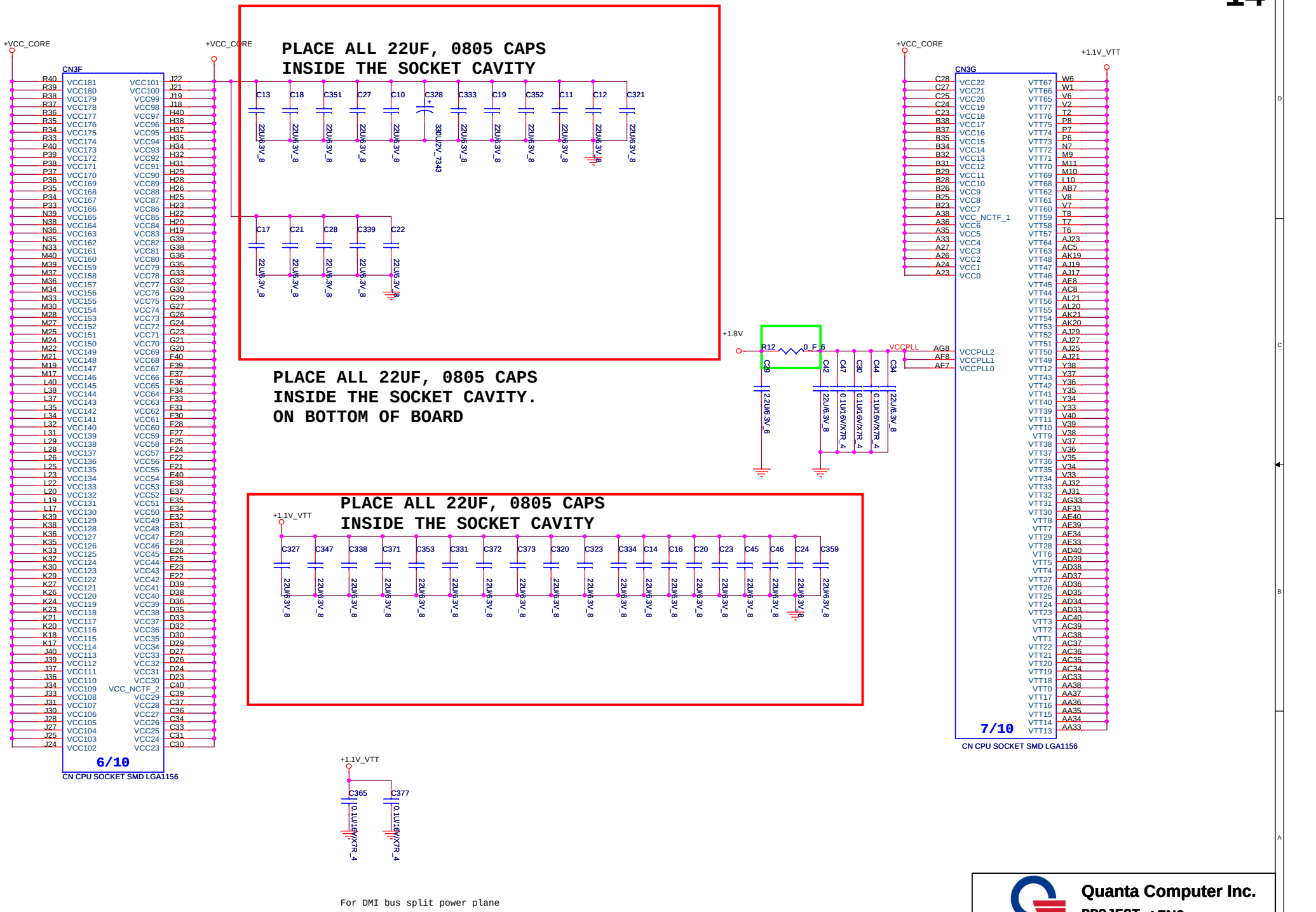
PROJECT : ZN2

Size	Document Number	Rev
	MCP (DDR3 CHANNEL B)	A

Date: Tuesday, March 16, 2010 Sheet 12 of 49



Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: MCP (PCIE/DMI)	Rev: A
Date: Tuesday, March 16, 2010	Sheet 13 of 49	



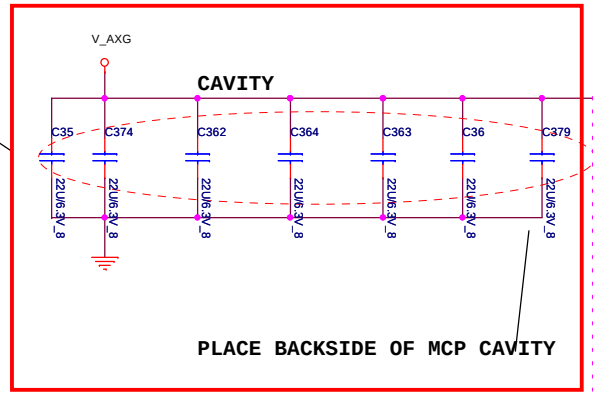
Quanta Computer Inc.

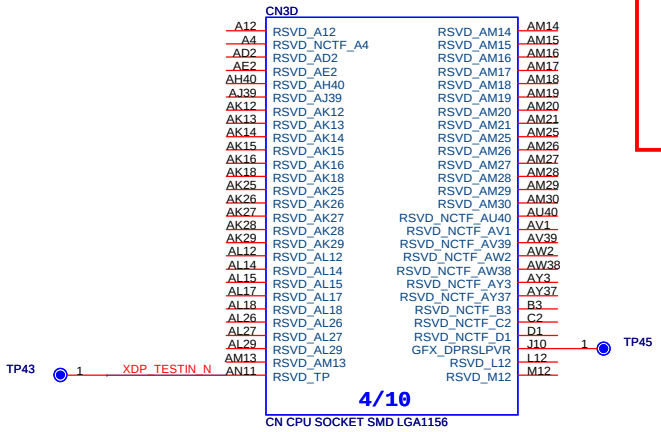
PROJECT : ZN2

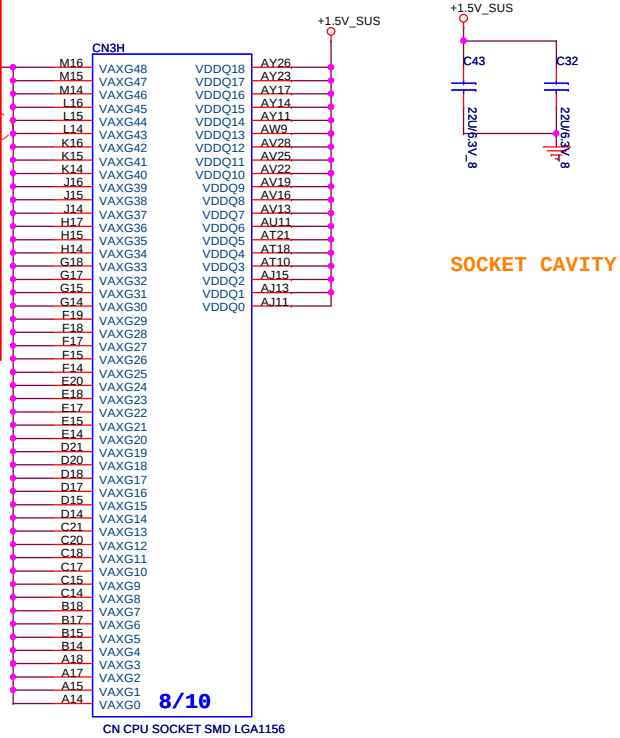
Size	Document Number	Rev
	MCP (VCCP)	A

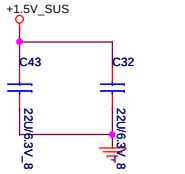
Date: Tuesday, March 16, 2010 Sheet 14 of 49

VAXG tie to GND for LFD CPU.



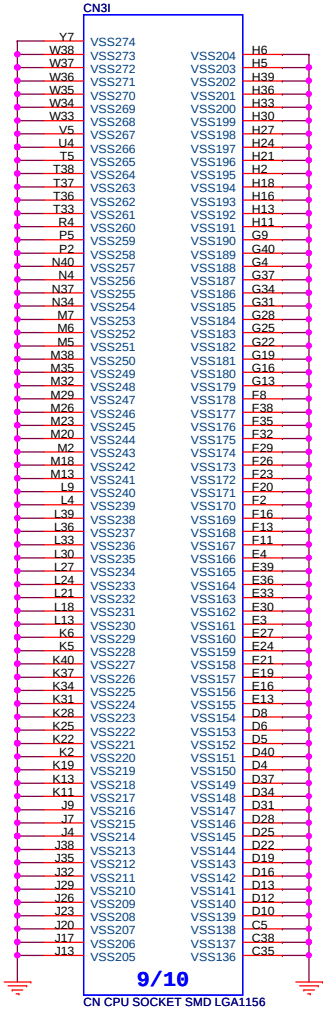


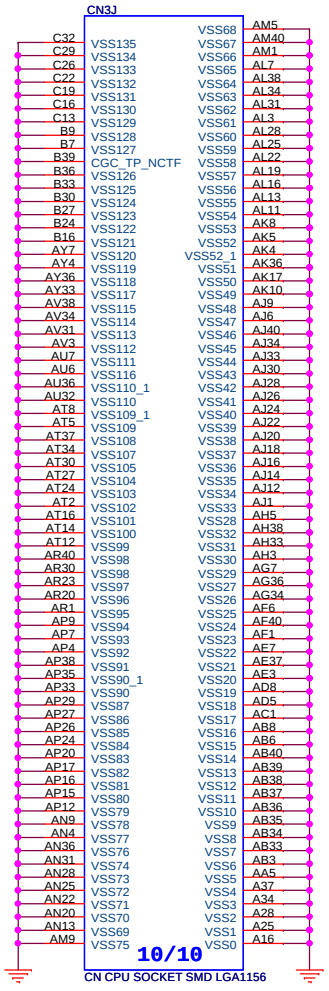




SOCKET CAVITY

Quanta Computer Inc.			
PROJECT : ZN2			
Size	Document Number: MCP (MISC/VCC)		Rev: A
Date: Tuesday, March 16, 2010	Sheet 15 of 49		





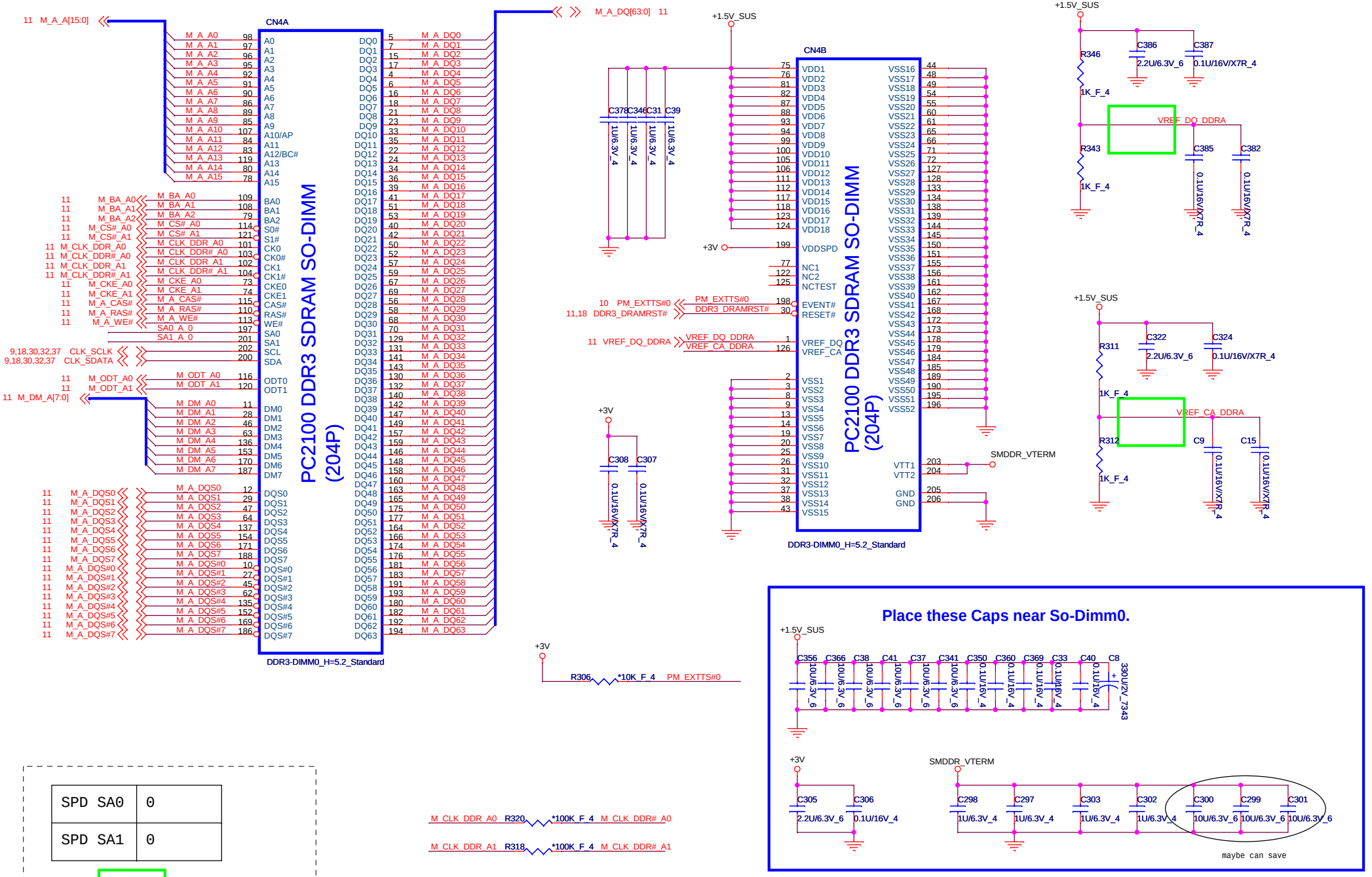
Quanta Computer Inc.

PROJECT : ZN2

Size	Document Number	Rev
	MCP (GND)	A

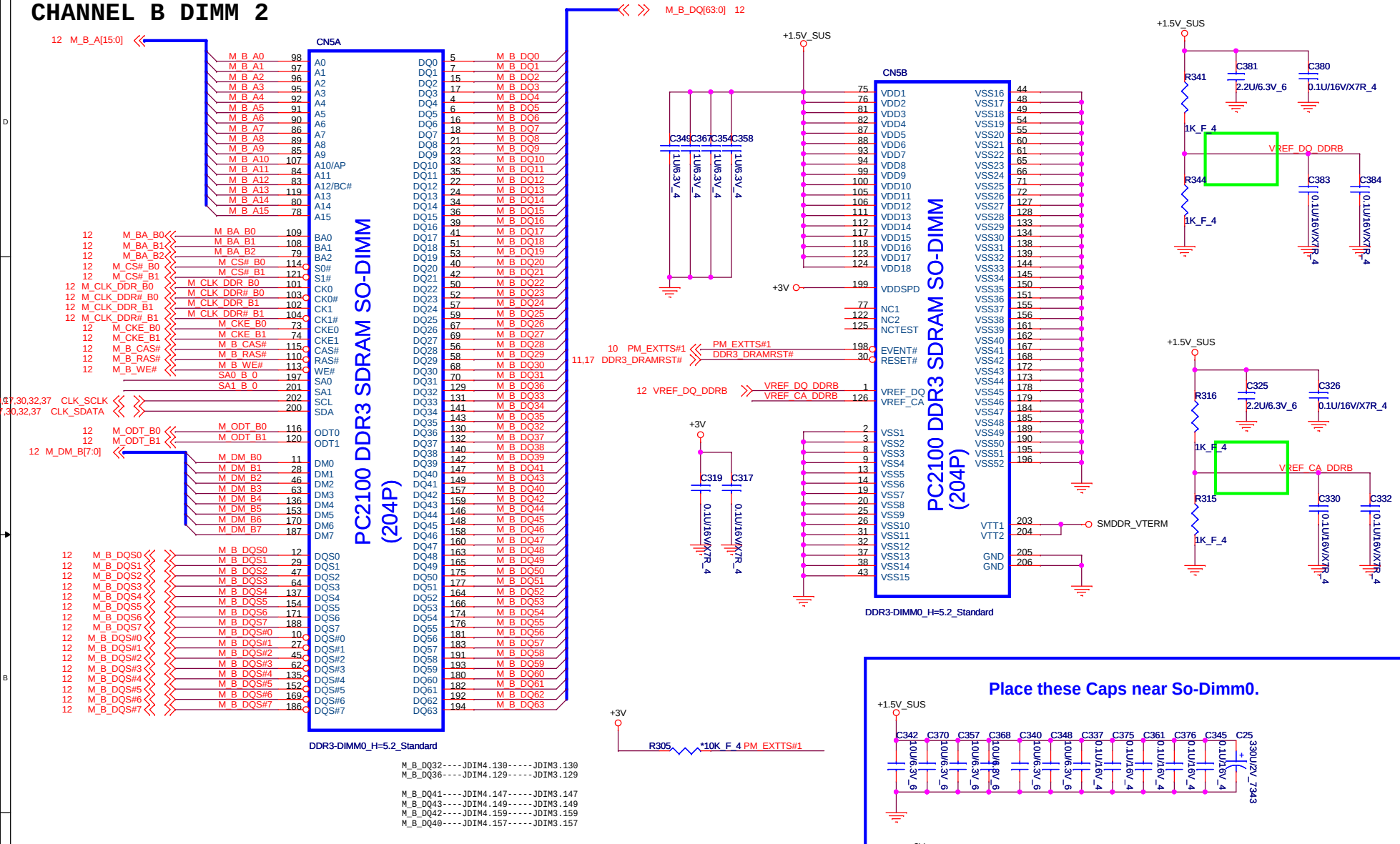
Date: Tuesday, March 16, 2010 Sheet 16 of 49

CHANNEL A DIMM 0

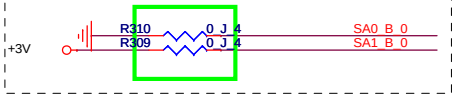


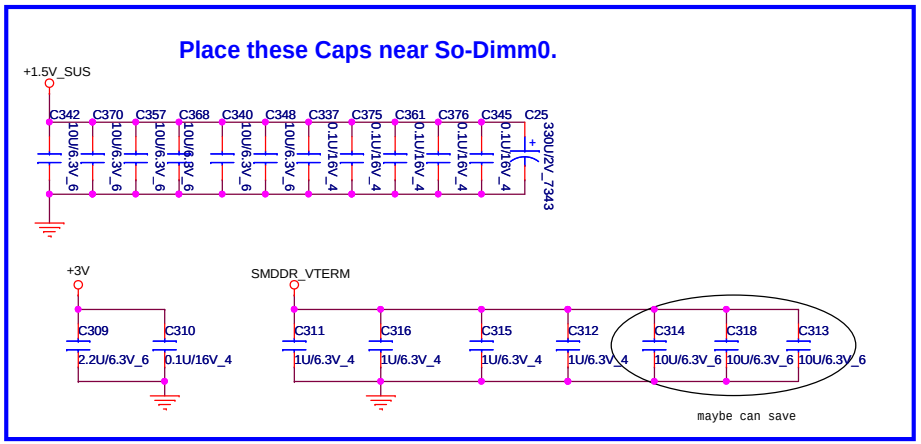
Quanta Computer Inc.	
PROJECT : ZN2	
Size	Document Number: DDR3 CHA DIMM 0 — Rev: A
Date: Tuesday, March 16, 2010	Sheet 17 of 49

CHANNEL B DIMM 2



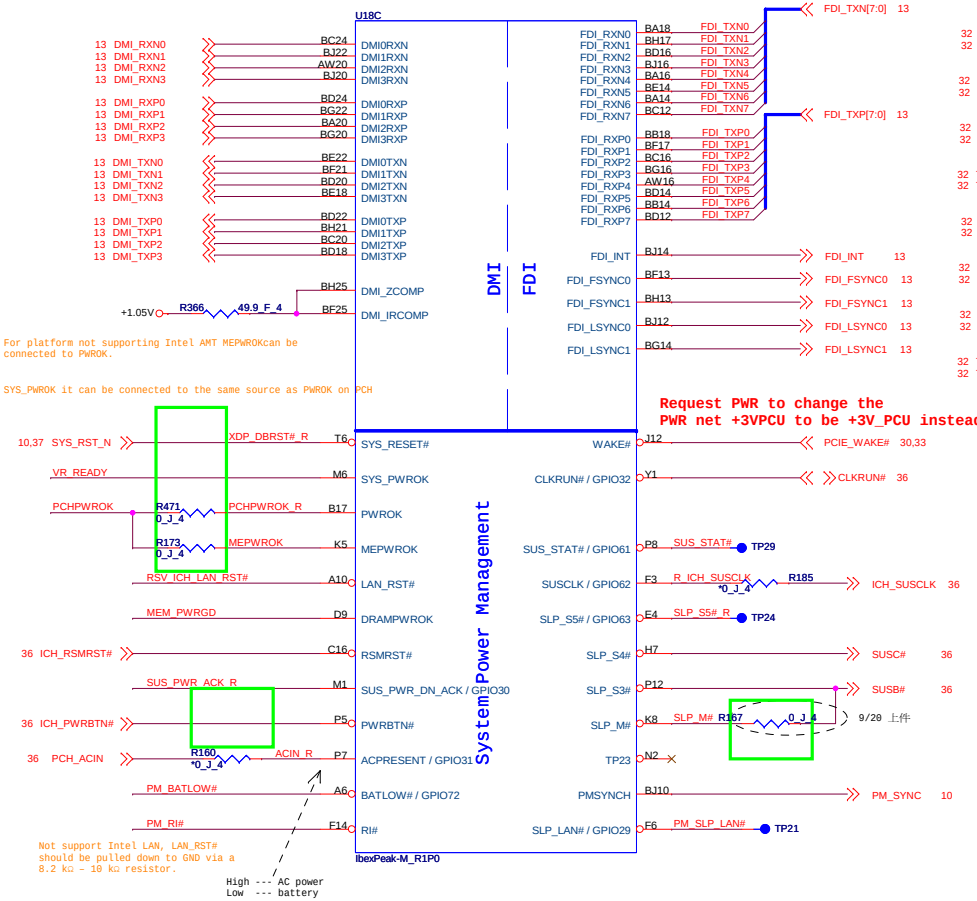
SPD SA0	0
SPD SA1	1



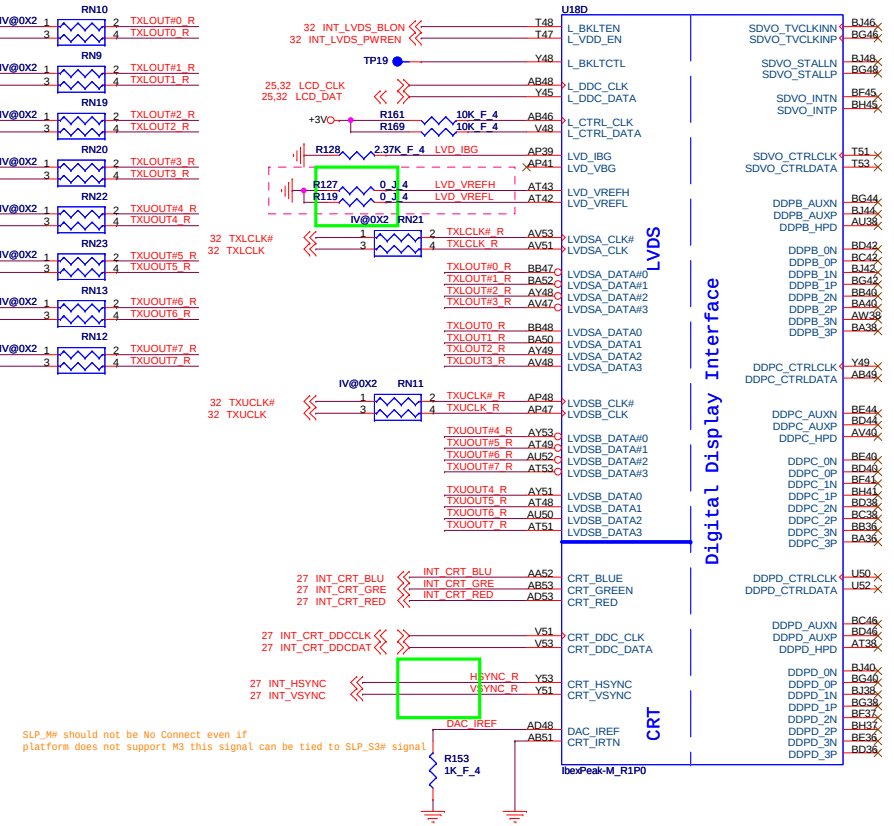


Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: DDR3 CHB DIMM 0	Rev: A
Date: Tuesday, March 16, 2010	Sheet 18 of 49	

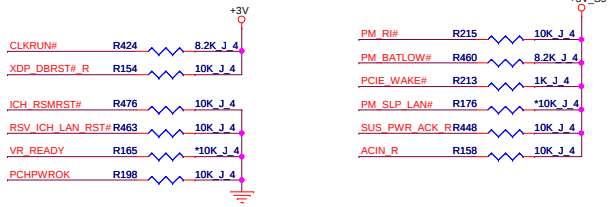
IBEX PEAK-M (DMI,FDI,GPIO)



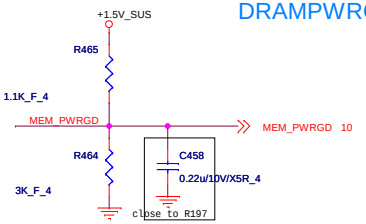
IBEX PEAK-M (LVDS,DDI)



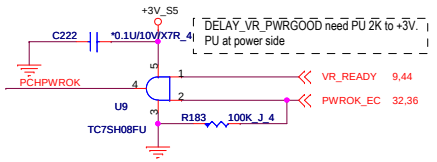
PCH Pull-high/low



DRAMPWROK



System PWR_OK



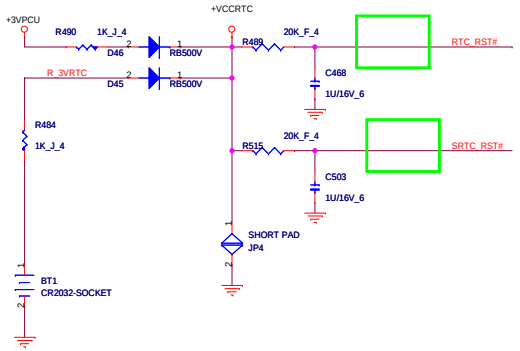
Quanta Computer Inc.

PROJECT : ZN2

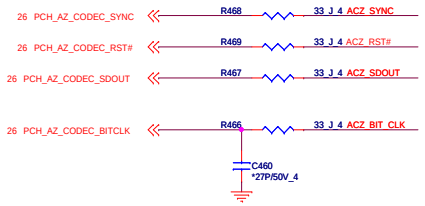
Size	Document Number	Rev
	PCH (DMI/FDI/VIDEO)	A

Date: Tuesday, March 16, 2010 Sheet 19 of 49

RTC Circuitry

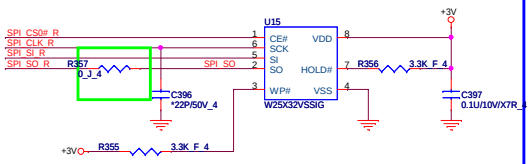


HDA Bus

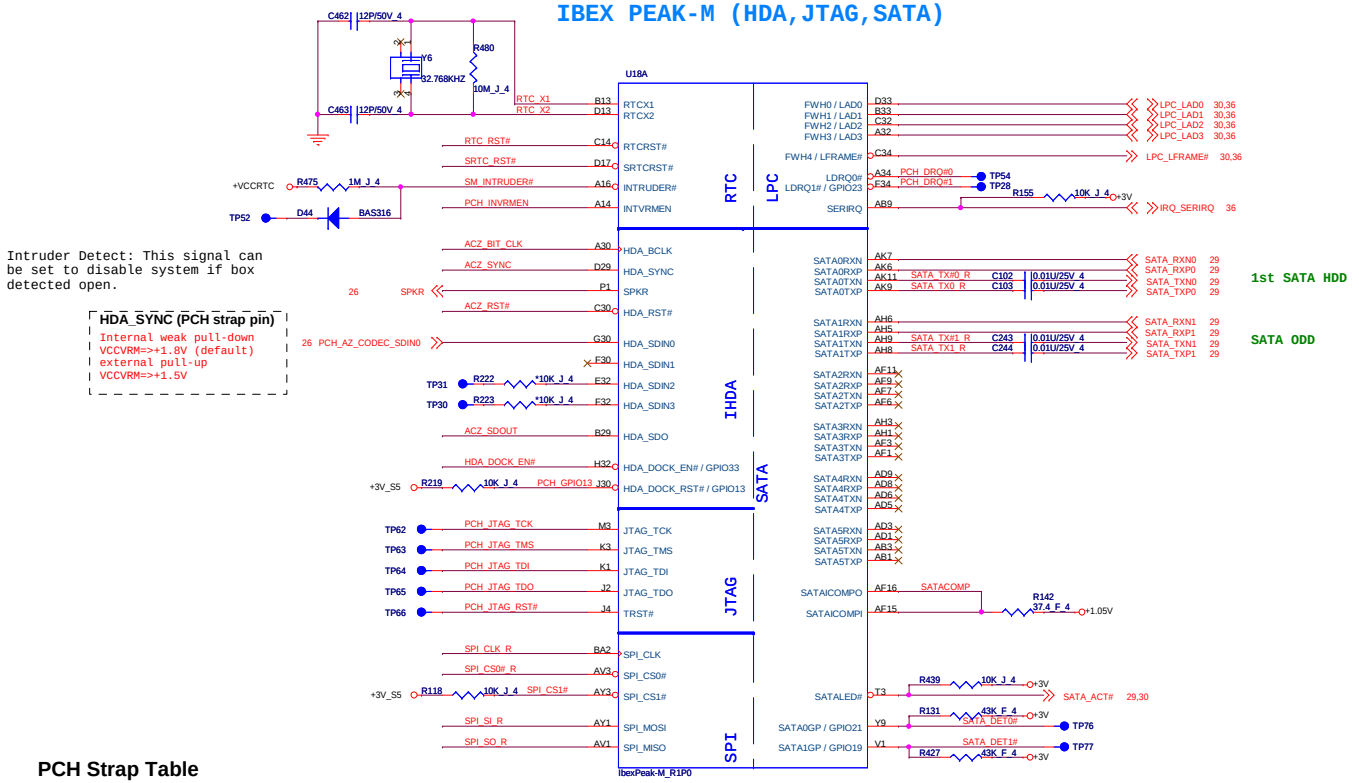


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



Intruder Detect: This signal can be set to disable system if box detected open.

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

PCH Strap Table

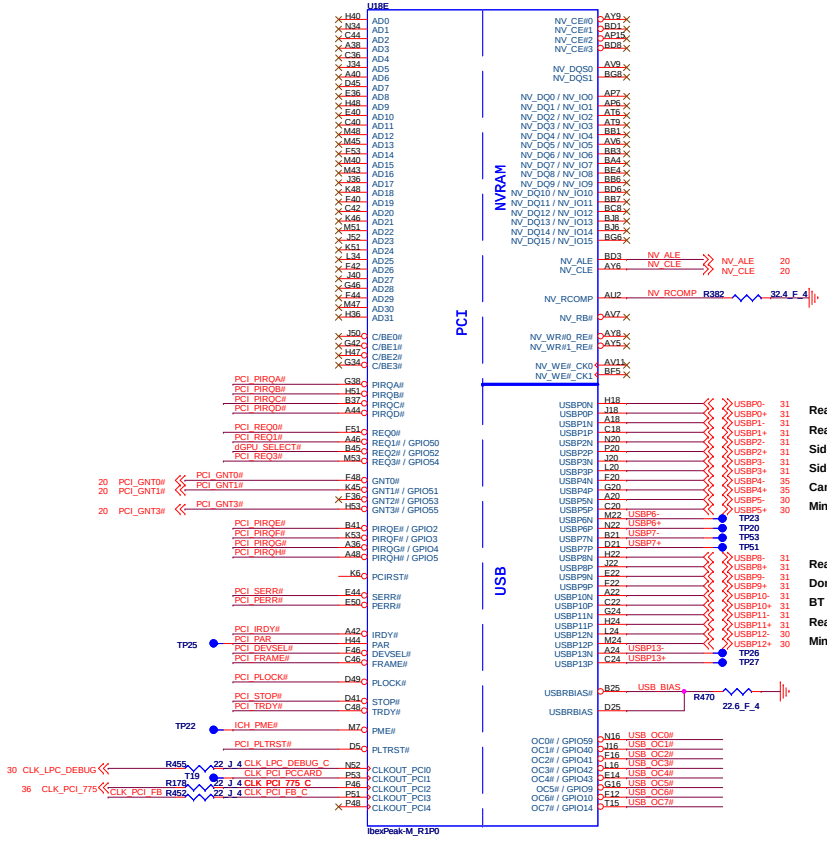
Pin Name	Strap description	Sampled	Configuration	ZN2 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R438 *10K_J_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R461 *10K_J_4 PCI_GNT3# 21
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R477 330K_J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]** +3V R195 *1K_J_4 R188 *1K_J_4 R196 *1K_J_4 R189 *1K_J_4 PCI_GNT0# 21 PCI_GNT1# 21
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R376 *1K_J_4 NV_ALE NV_ALE 21
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R110 *1K_J_4 NV_CLE NV_CLE 21
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R220 *1K_J_4 R221 *10K_J_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R378 *1K_J_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R187 10K_J_4 RSV_GPIO8 22
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R148 1K_J_4 CR_WAKE# 22

Quanta Computer Inc.
PROJECT : ZN2

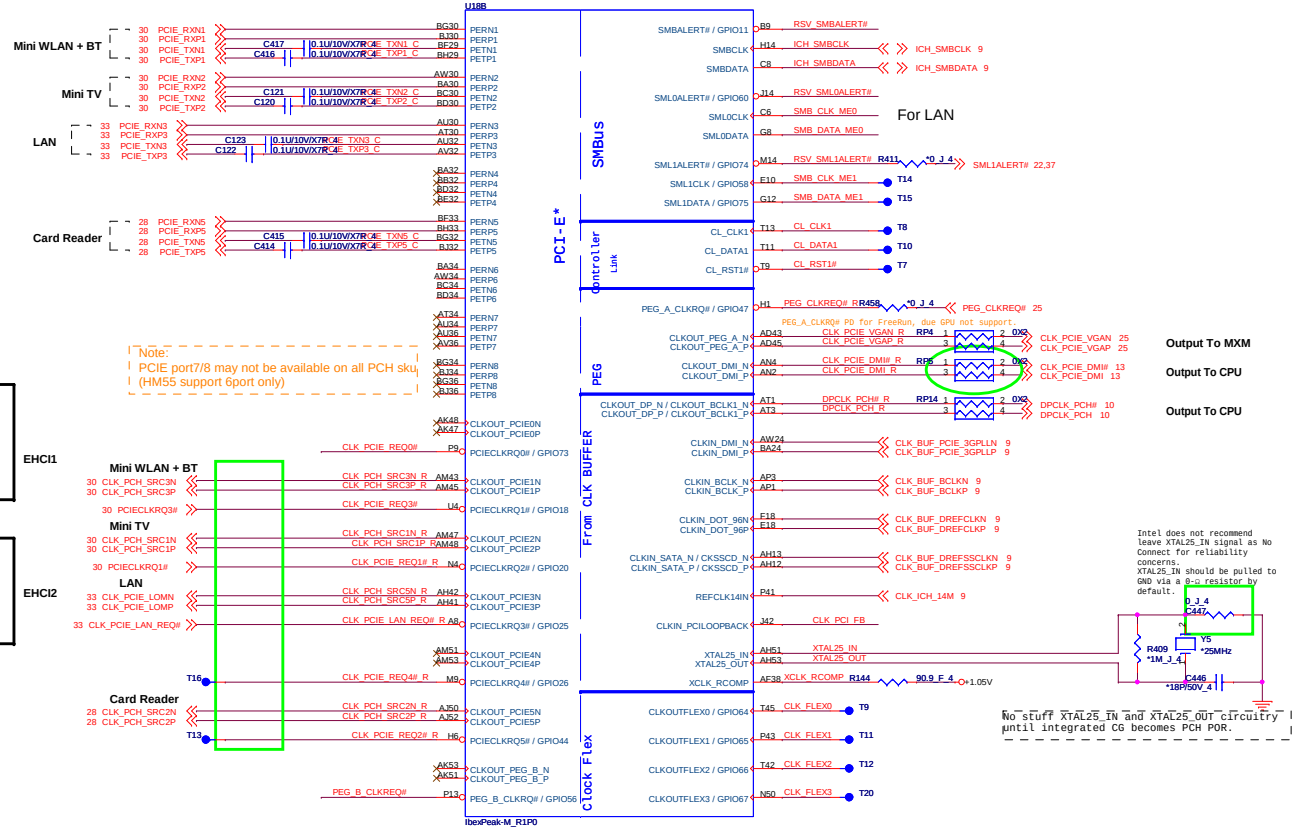
Size	Document Number	Rev
	PCH (SATA/RTC/HDA/LPC)	A

Date: Tuesday, March 16, 2010 Sheet 20 of 49

IBEX PEAK-M (PCI,USB,NVRAM)

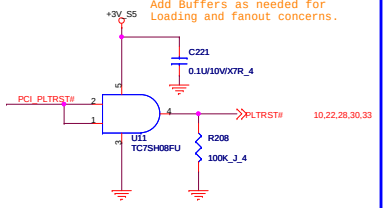


IBEX PEAK-M (PCI-E,SMBUS,CLK)

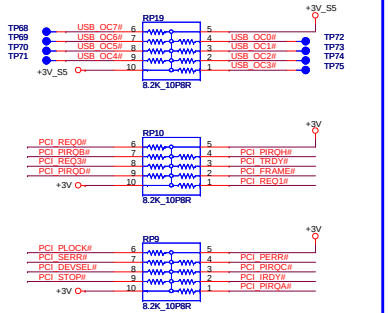


Support PCIe 2.0

PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin

PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap

GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

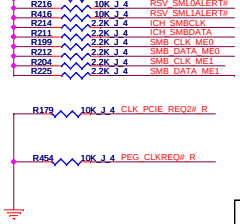
Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

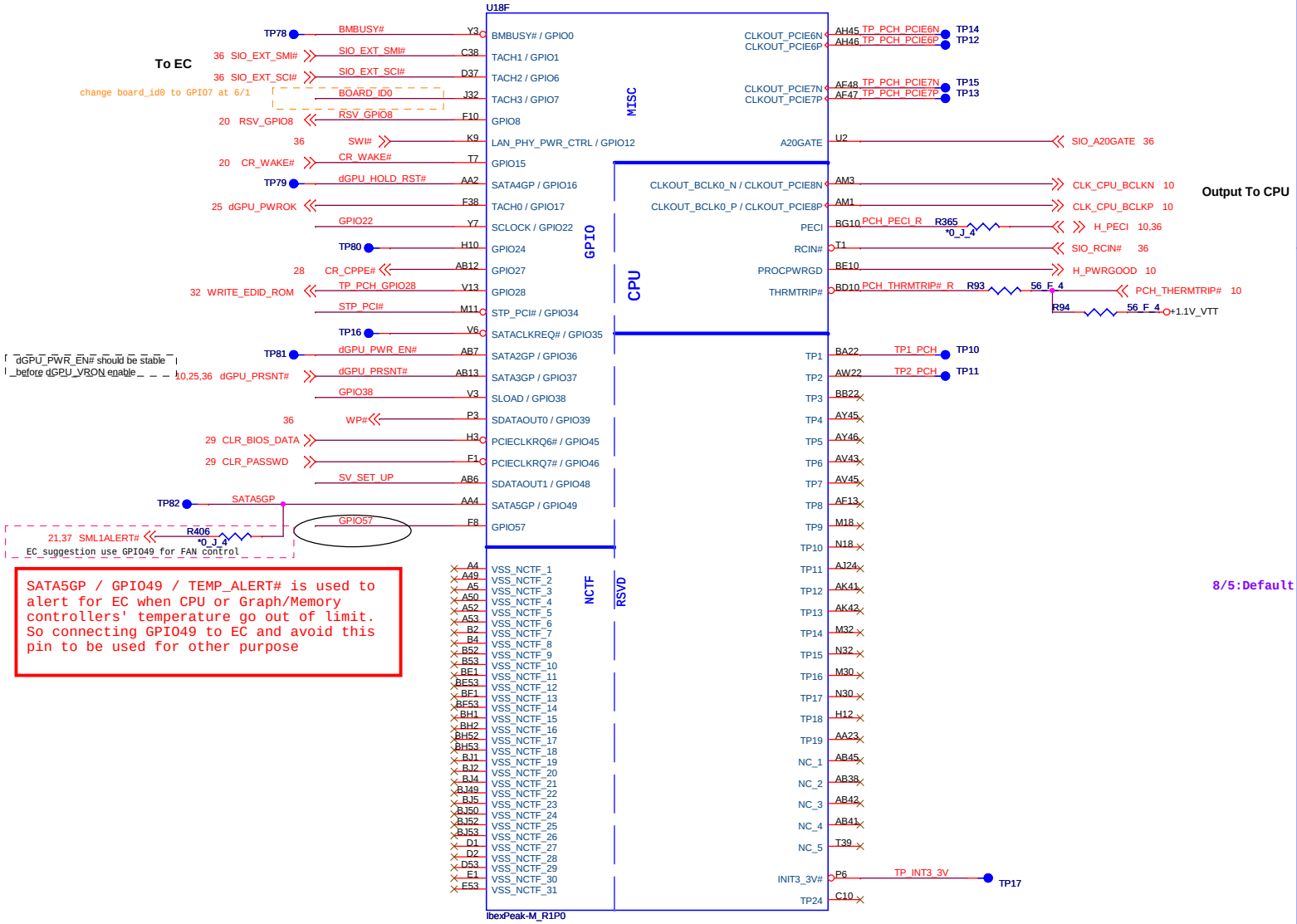
DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

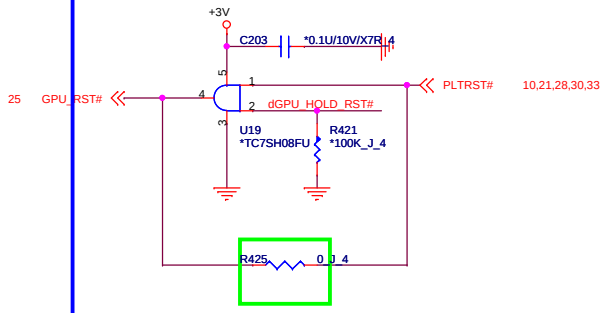
SMBus/Pull-up



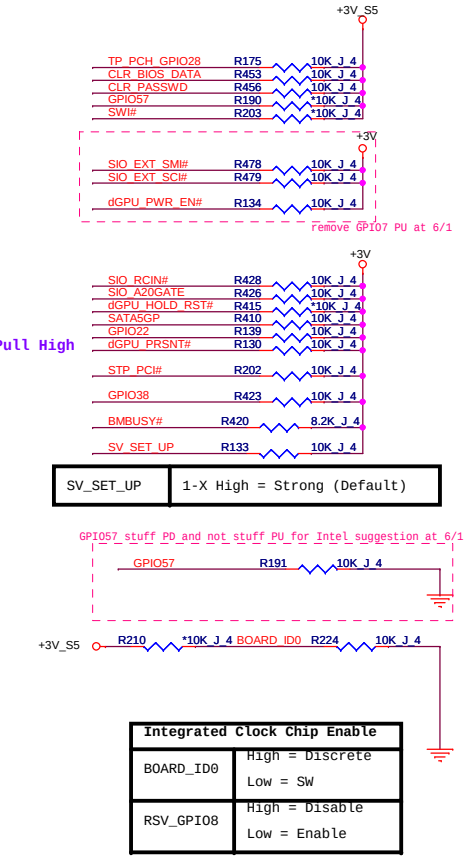
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#



GPIO Pull-up/Pull-down



8/5:Default Pull High

SV_SET_UP	1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1

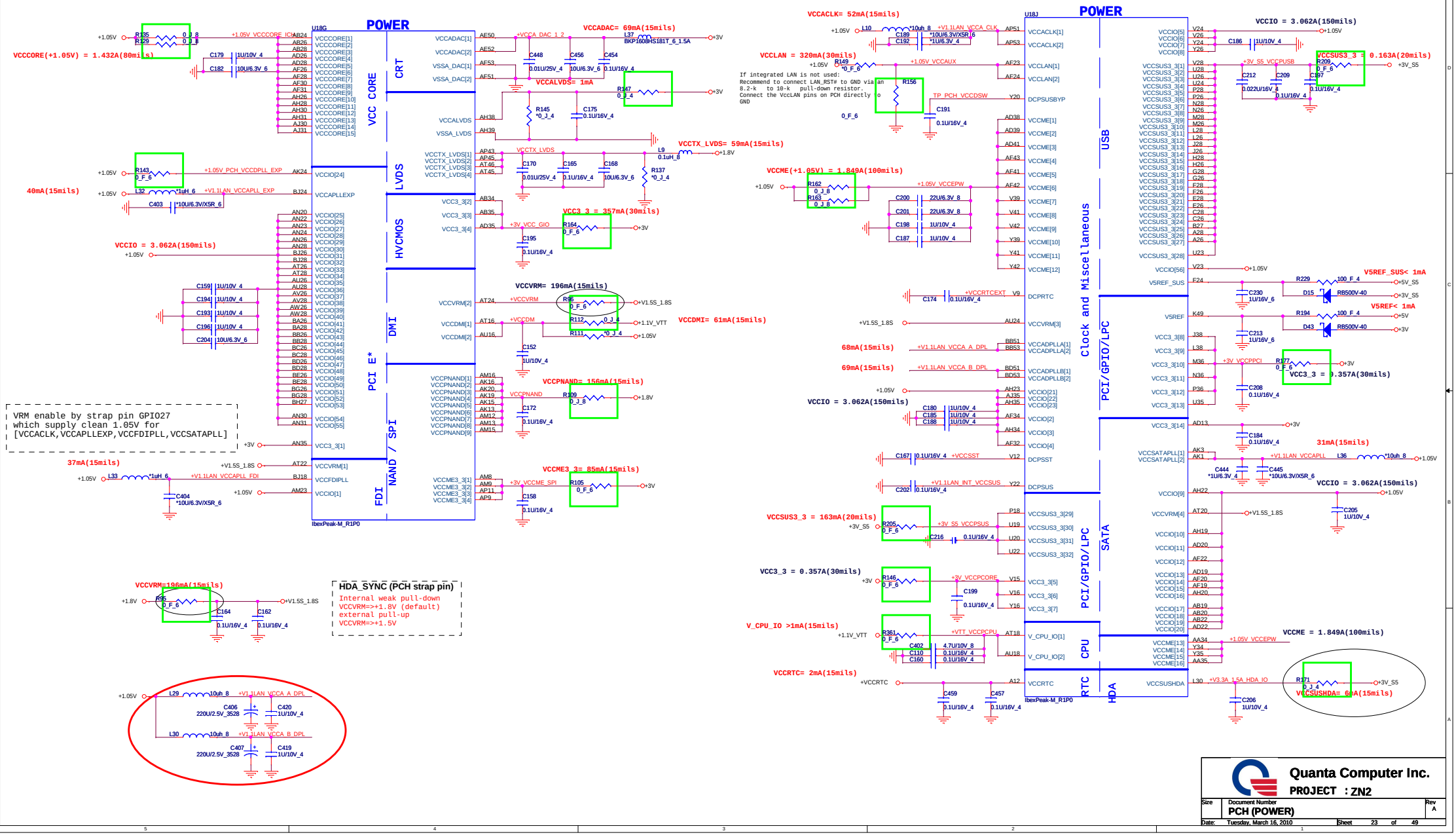
Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	PCH (GPIO/CPU)	A

Date: Tuesday, March 16, 2010 Sheet 22 of 49

IBEX PEAK-M (POWER)



Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	PCH (POWER)	A
Date: Tuesday, March 16, 2010	Sheet 23 of 49	

IBEX PEAK-M (GND)

Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: PCH (GND)	Rev: A
Date: Tuesday, March 16, 2010	Sheet 24 of 49	

6/25 Change CN22 pin define and footprint at C test.

VIN_MXM 7~20V

Check Footprint and P/N

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

At 11/21
update MXM footprint to mxm-mm70-314-310b1-1-270p

CN14A

CN14B

10Amp

2.5Amp

1Amp

These capacitors have to be put near to MXM 3.0.

These capacitors have to be put near to LGA1156.

7/28: add decoupling capacitors for AMD recommendation

7/28: pull-up resistor for AMD recommendation. (AND:10K ohm pull-up resistor)

MXM3_2.0 CONNECTOR

MXM VIN Power switch

10Amp

80ohm/5A

L14 HI0805R800R-00 8

L15 HI0805R800R-00 8

L16 HI0805R800R-00 8

MXM 3V/5V Power switch

1Amp

2.5Amp

At 11/14 Add it

L5 HI0805R800R-00 8

L11 HI0805R800R-00 8

To low power status mode

1 : FULL POWER
0 : LOW POWER

RB500V-40

To EC

U10 TC7SH08FU

MXM_LVDS_CONNECT

CON1

LCD_CON30

87216-300x-30p-ldv

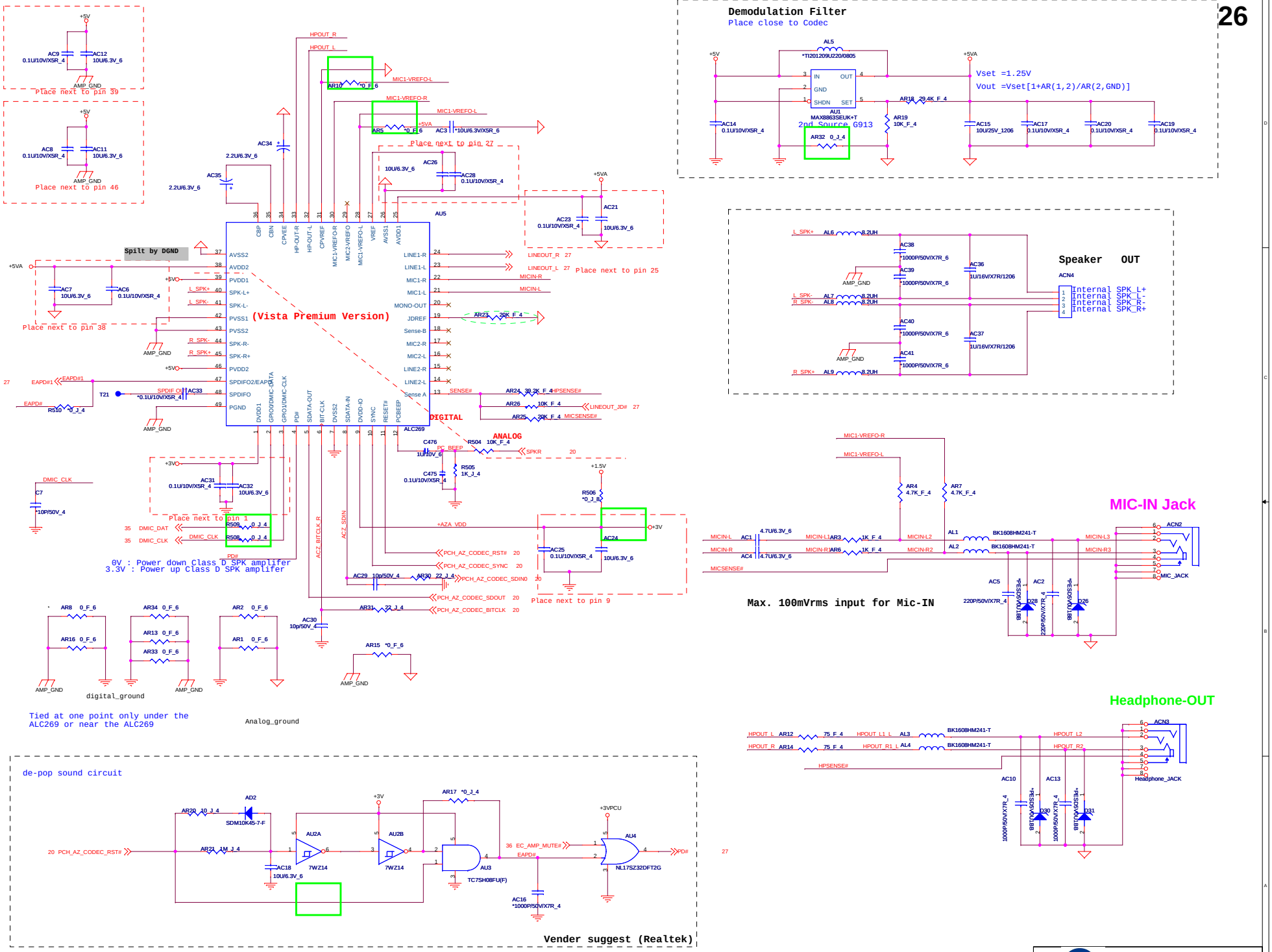
LVDS PIN Swap

Quanta Computer Inc.

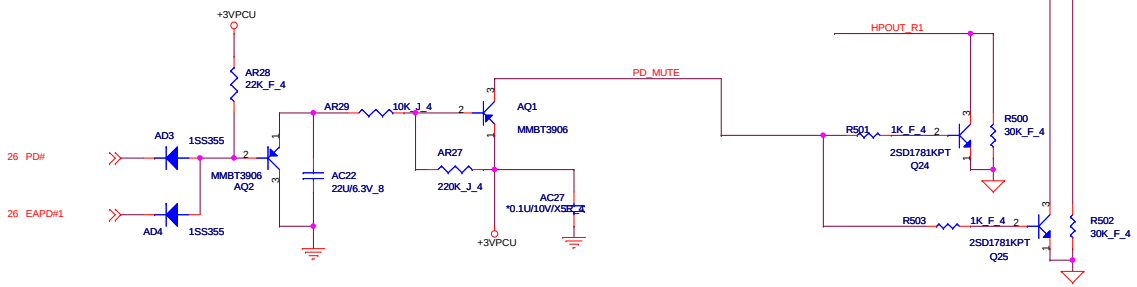
PROJECT : ZN2

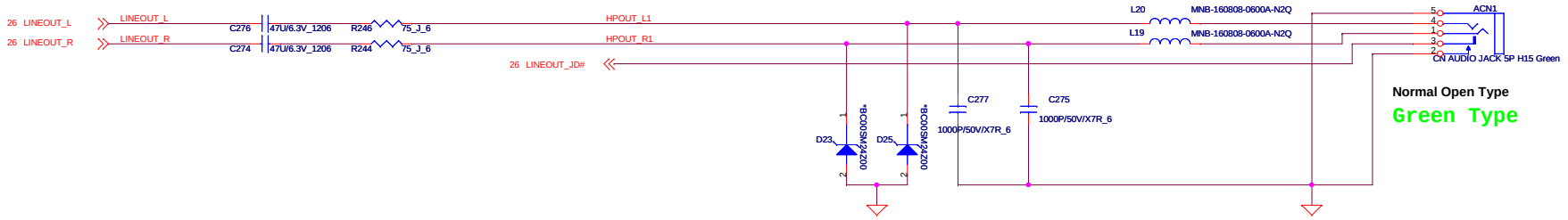
Size	Document Number	Rev
	MXM 3.0	A

Date: Tuesday, March 16, 2010 Sheet 25 of 49

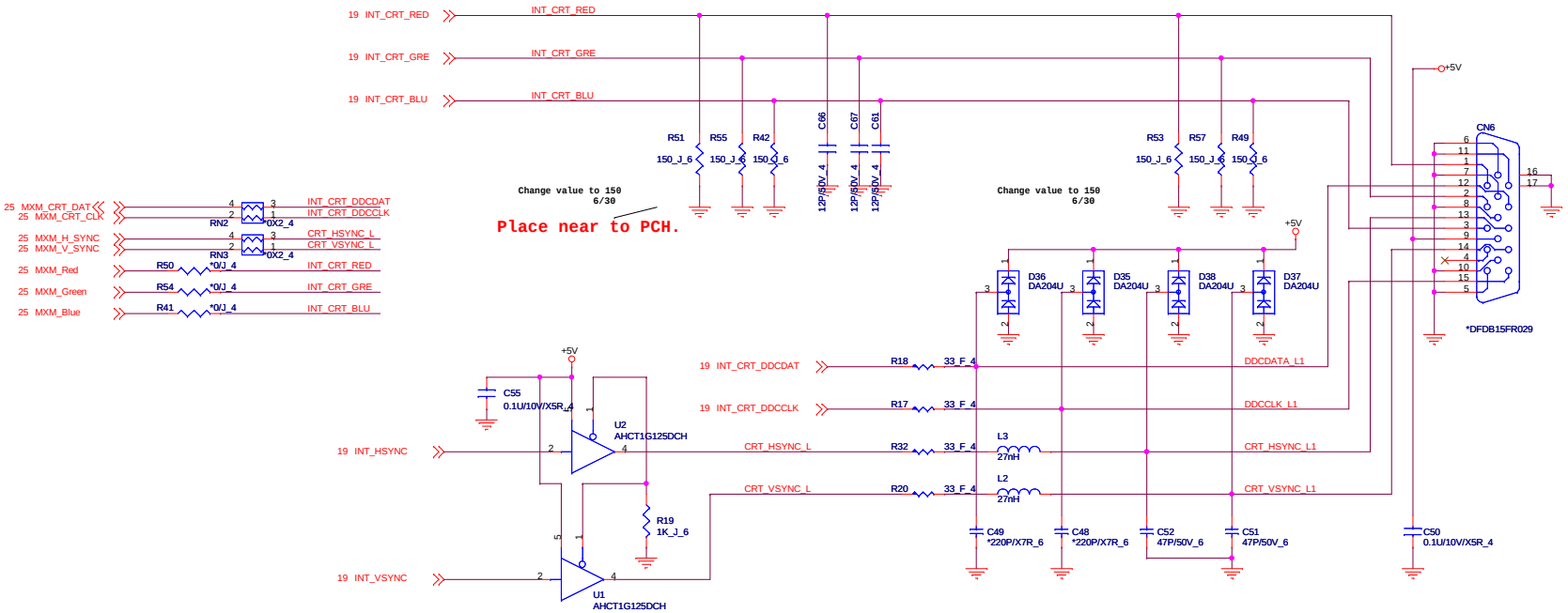


Quanta Computer Inc.			
PROJECT : ZN2			
Size	Document Number		Rev
	AUDIO CODEC AL269		1A
Date: Tuesday, March 16, 2010	Sheet 26 of 49		





Reserve to CRT

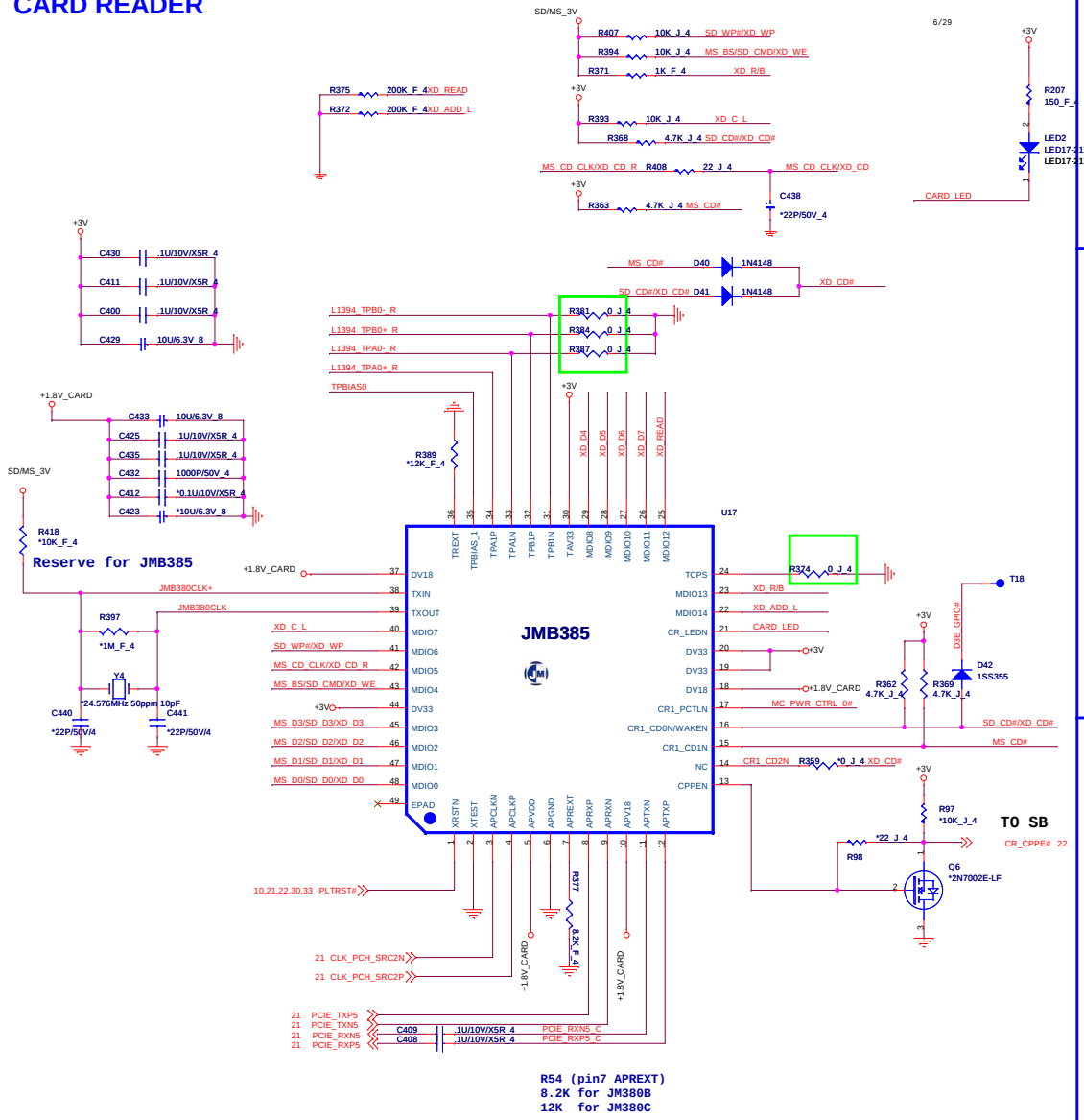


Quanta Computer Inc.

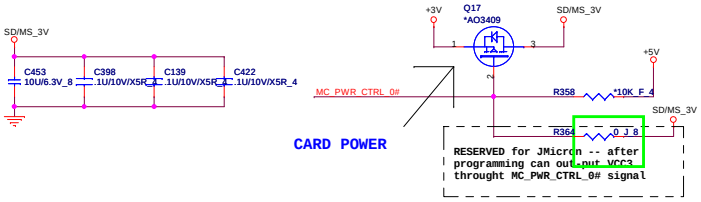
PROJECT : ZN2

Size	Document Number	Rev
	Line Out/CRT	1A
Date: Tuesday, March 16, 2010	Sheet 27 of 49	

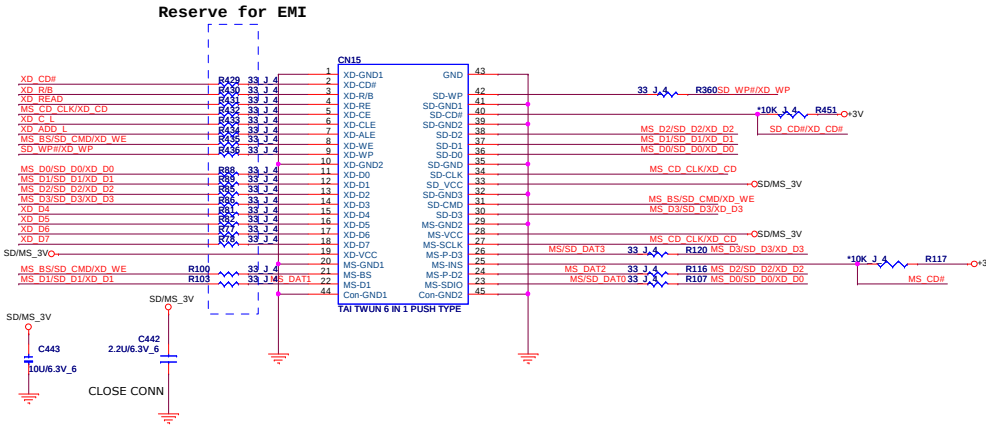
CARD READER



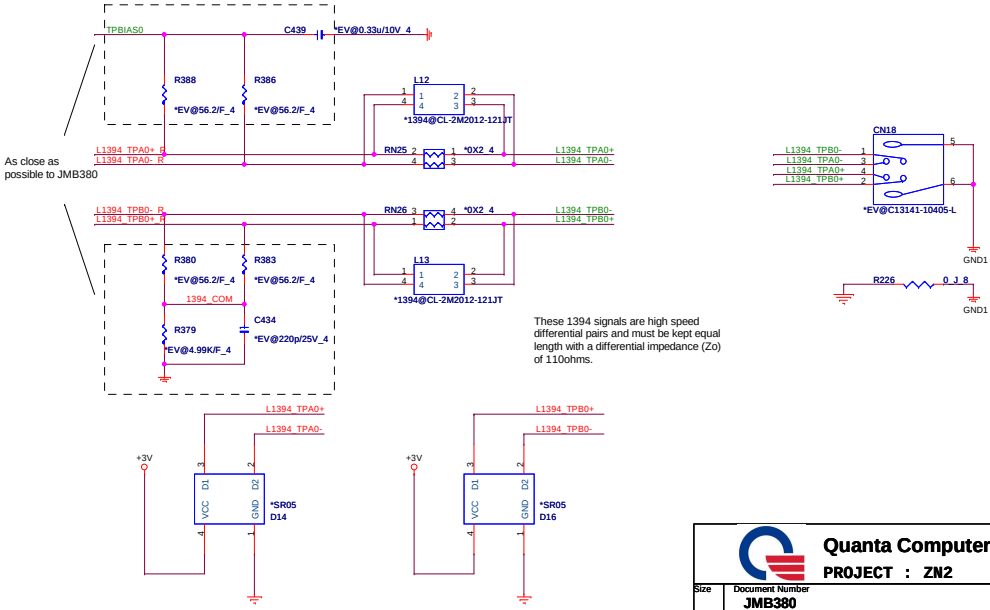
CARDREADER POWER



6 IN 1 CONN



1394



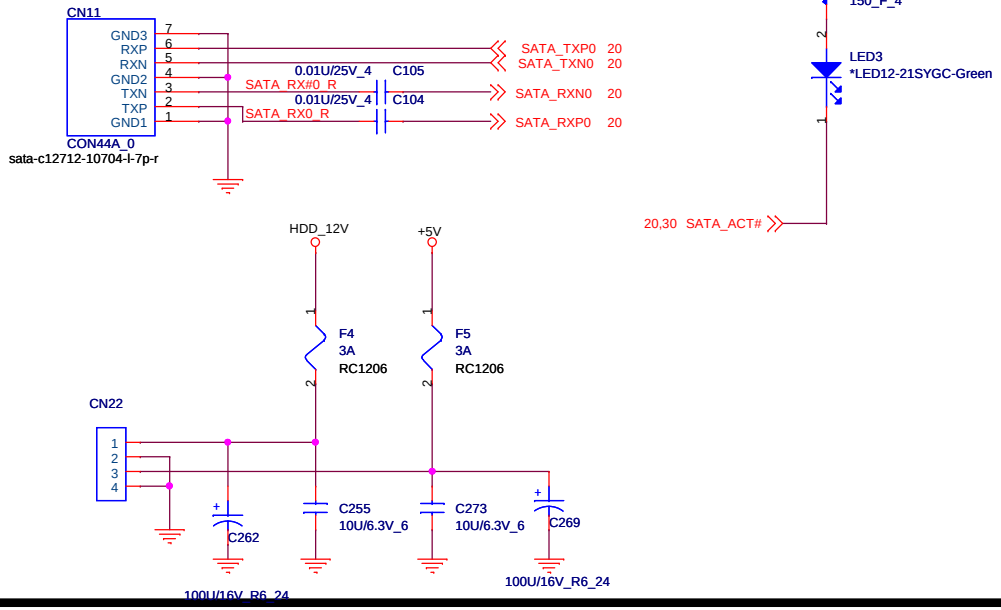
Quanta Computer Inc.
PROJECT : ZN2

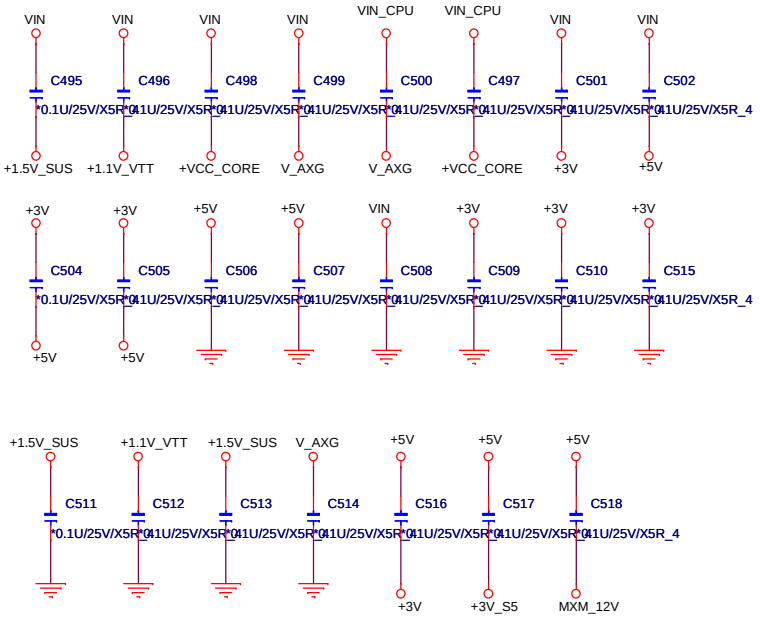
Size	Document Number	Rev
	JMB380	1A

Date: Tuesday, March 16, 2010 Sheet 28 of 49

SATA HDD(3.5")

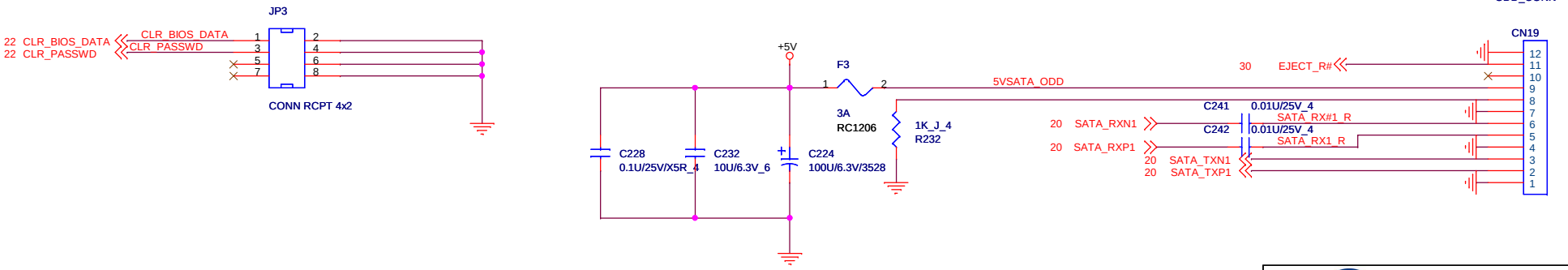
SATA HDD CONNECT





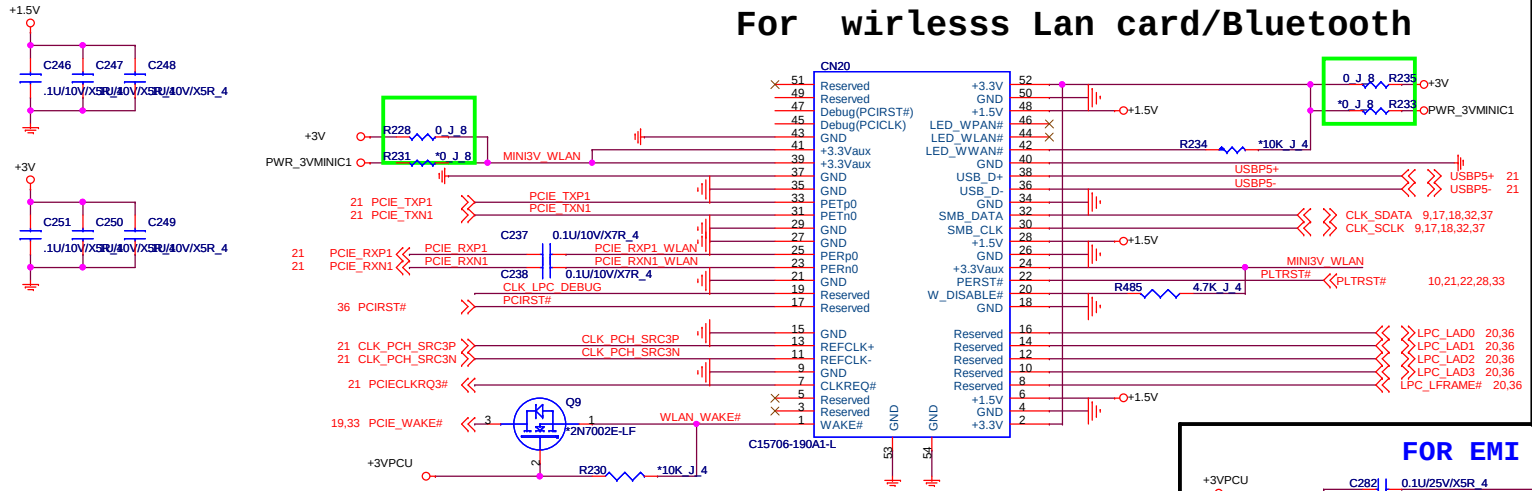
FOR EMI DEMAND

SATA ODD CONNECTOR

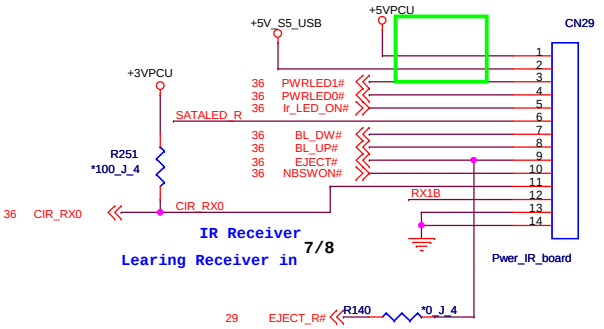


Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: SATA HDD/ODD	Rev: 1A
Date: Tuesday, March 16, 2010	Sheet 29 of 49	

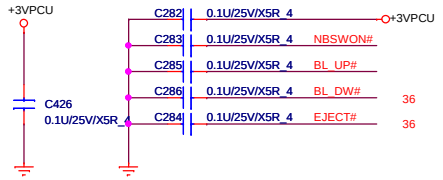
For wirelesss Lan card/Bluetooth



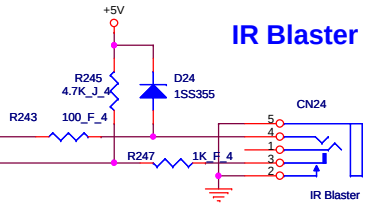
TO POWER BUTTON & LED LIGHT& IR



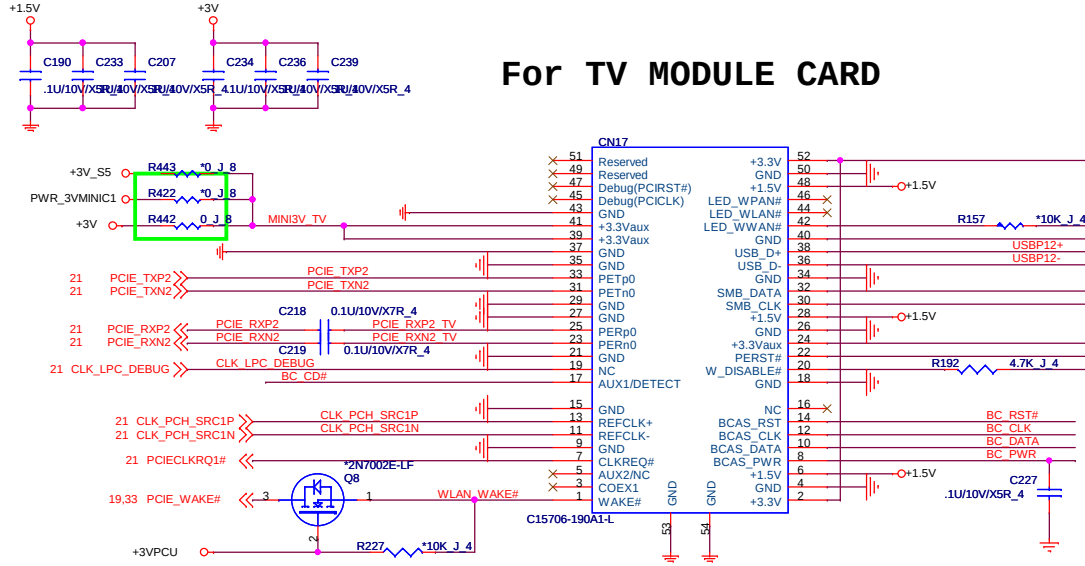
FOR EMI

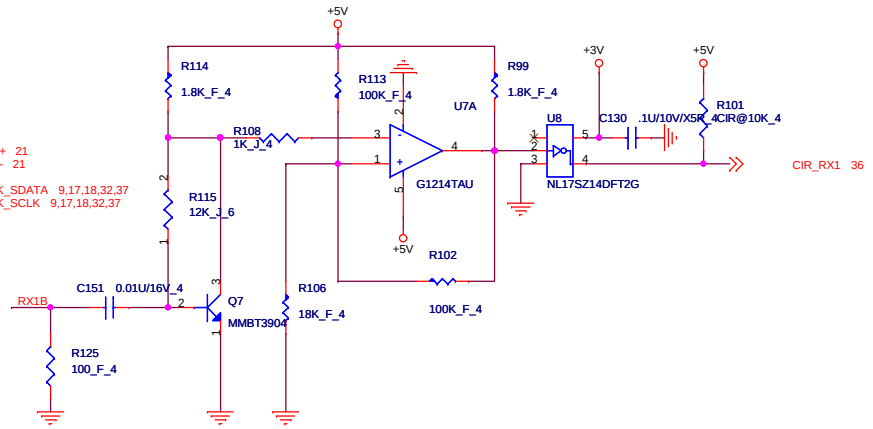


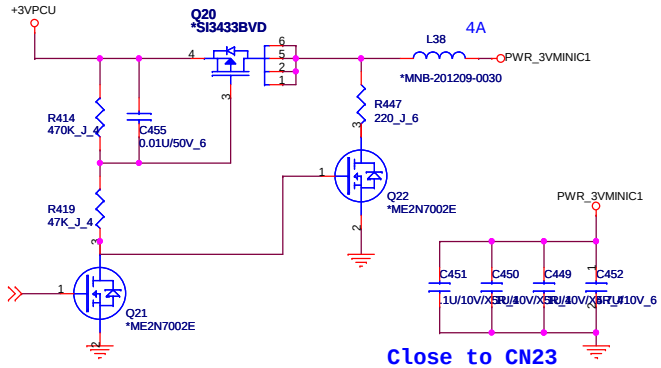
IR Blaster



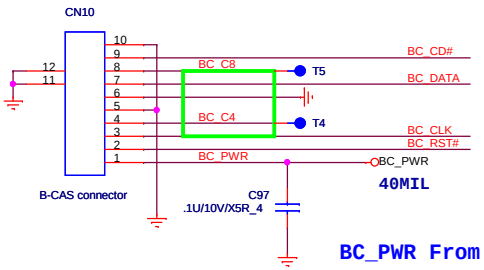
For TV MODULE CARD

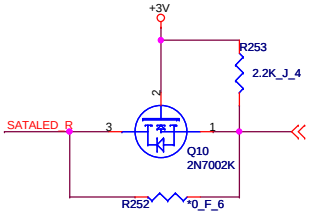






B-CAS CONN

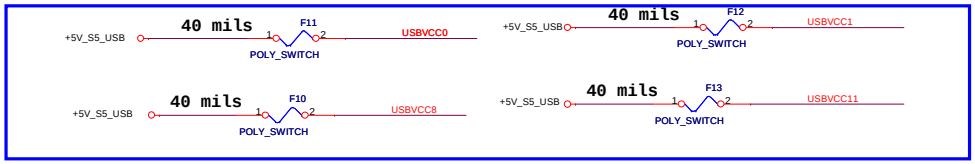


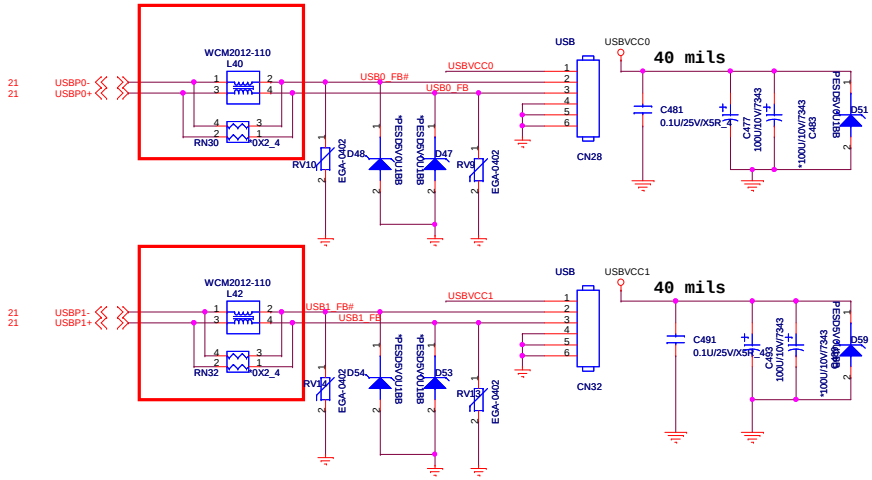


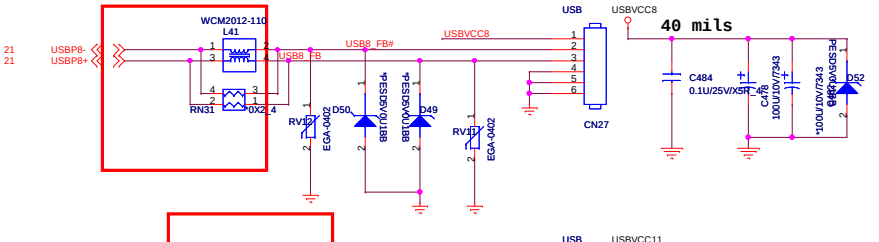
Quanta Computer Inc.
PROJECT : ZN2

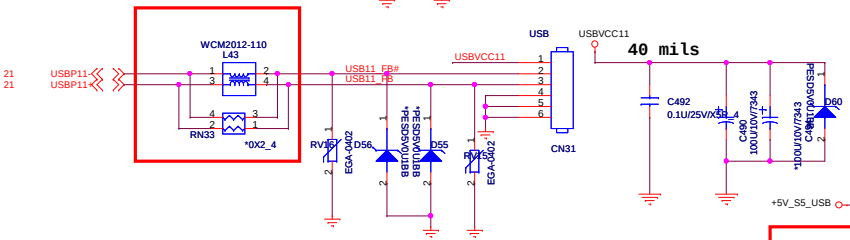
Size	Document Number	Rev
	MINI PCIE(WLAN/TV/IR)	1A
Date: Tuesday, March 16, 2010	Sheet 30 of 49	

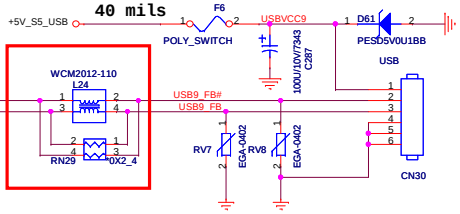
Rear USB

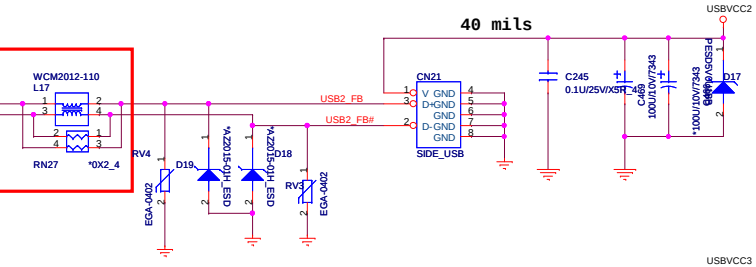


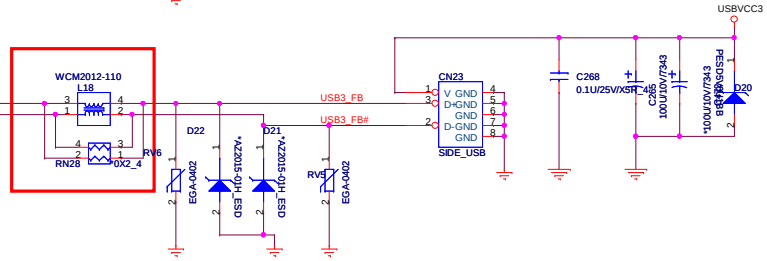


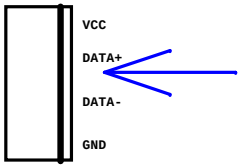


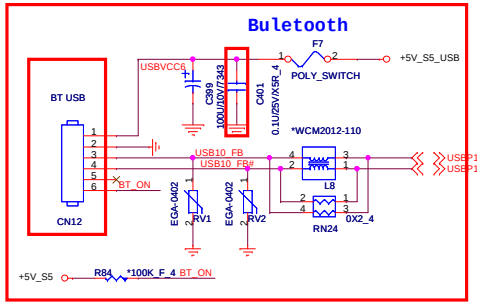










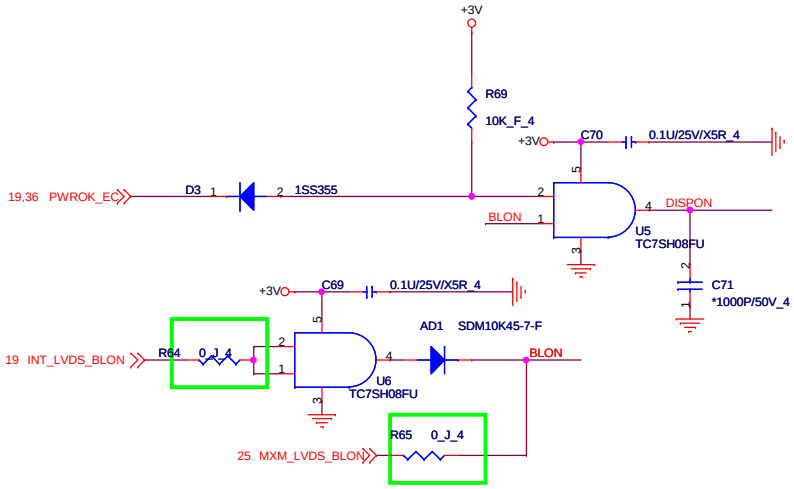


Quanta Computer Inc.
PROJECT : ZN2

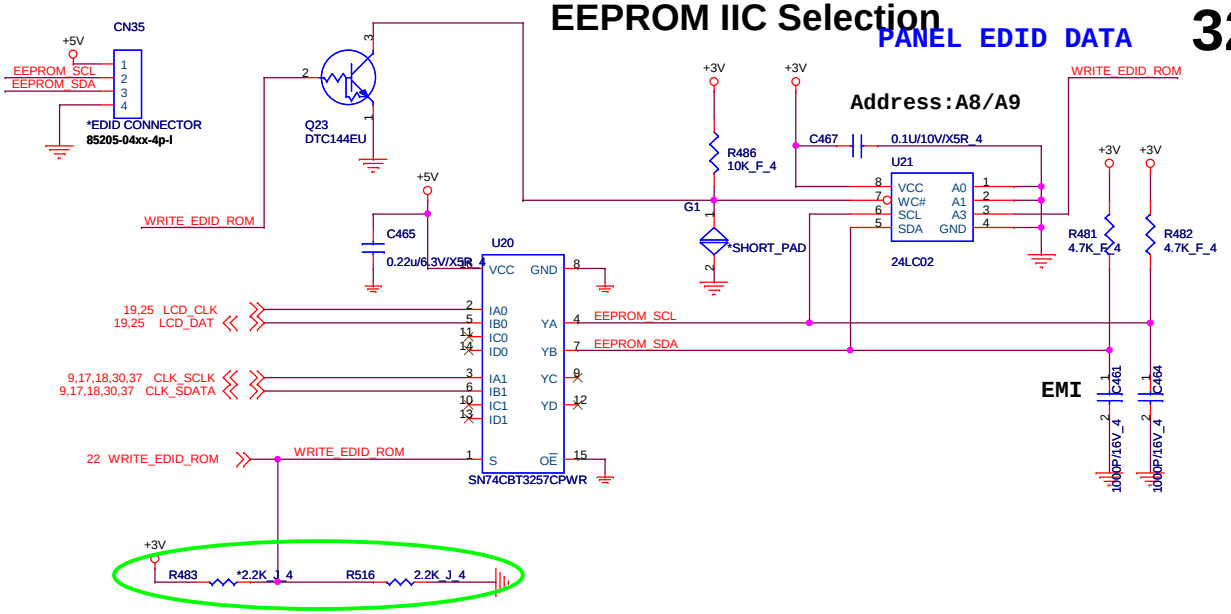
Size	Document Number	Rev
	ON BOARD USB	A

Date: Tuesday, March 16, 2010 Sheet 31 of 49

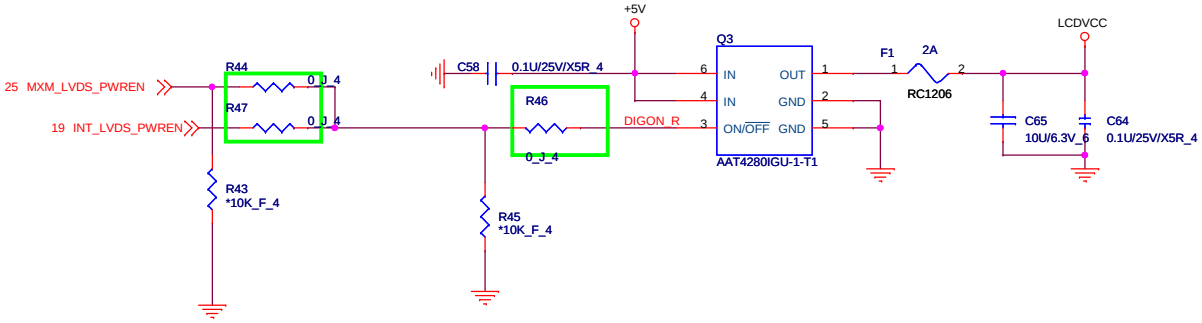
BACKLIGHT CONTROL



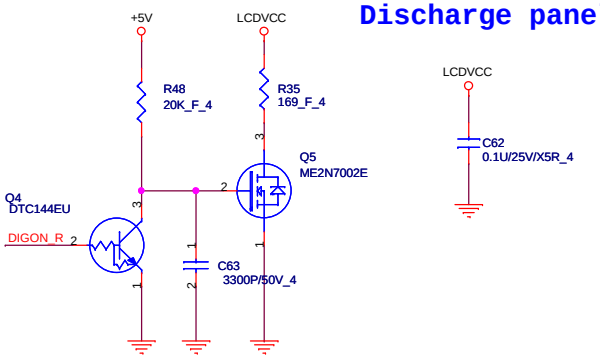
EEPROM IIC Selection



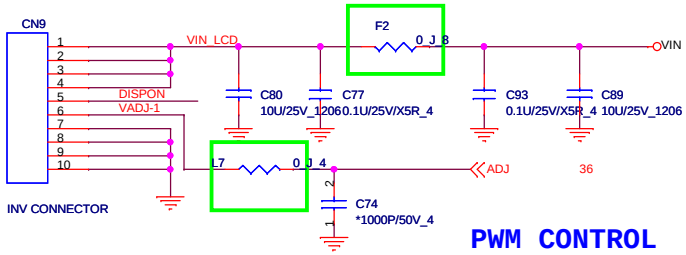
PANEL VCC CONTROL



Discharge panel power

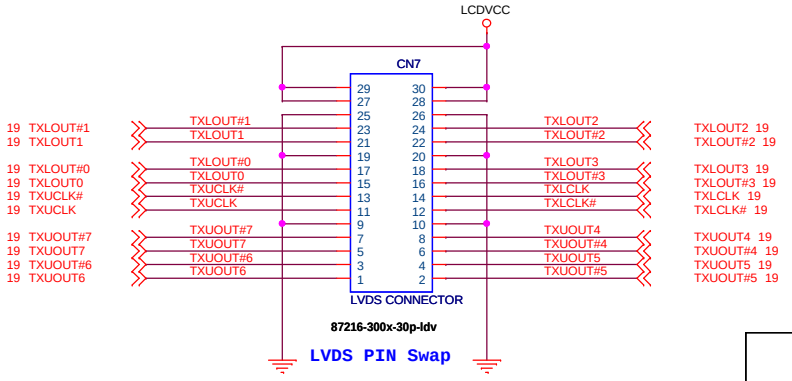


TO INVERTER CONNECT



PWM CONTROL

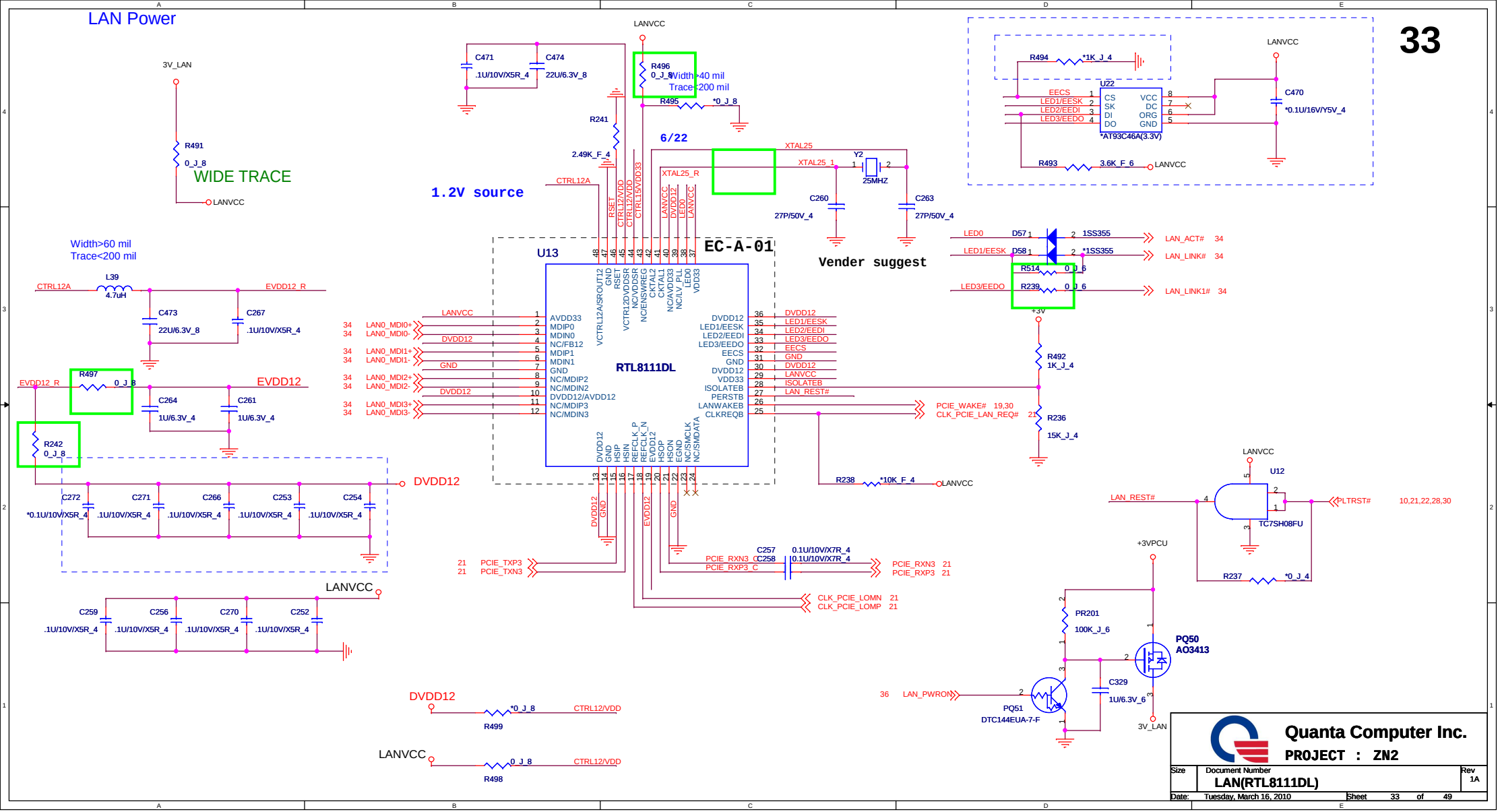
LCD PANEL CONNECTOR



Quanta Computer Inc.

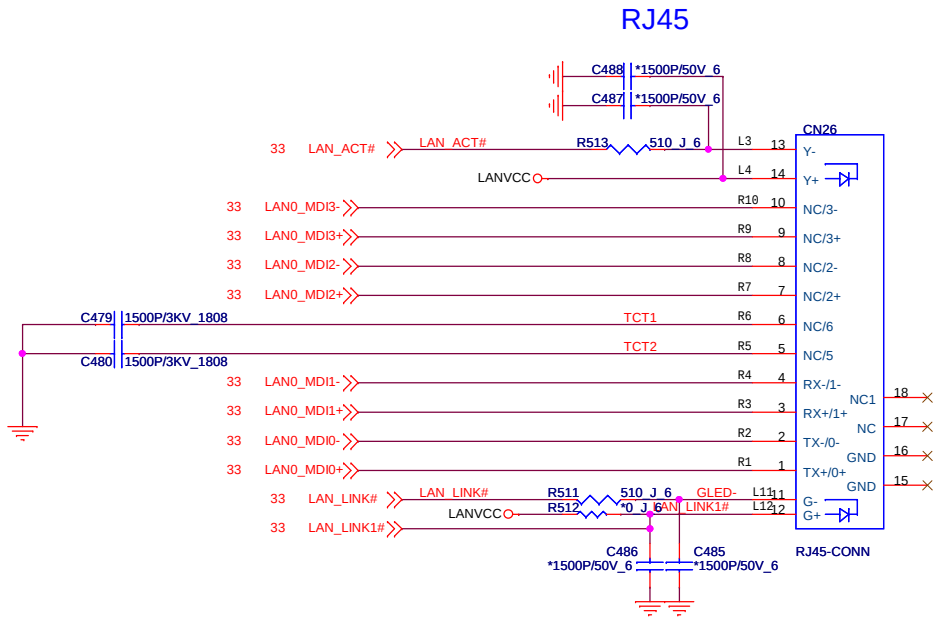
PROJECT : ZN2

Size	Document Number	Rev
	LCD PANEL/INVERTER	A
Date: Tuesday, March 16, 2010	Sheet 32 of 49	



LAN Power
33
3V_LAN
R491
0_J_8
WIDE TRACE
LANVCC
Width>60 mil
Trace<200 mil
L39
4.7uH
CTRL12A
EVDD12_R
C473
22U/6.3V_8
C267
.1U/10V/X5R_4
R497
0_J_8
EVDD12
C264
1U/6.3V_4
C261
1U/6.3V_4
R242
0_J_8
DVDD12
C272
*0.1U/10V/X5R_4
C271
.1U/10V/X5R_4
C266
.1U/10V/X5R_4
C253
.1U/10V/X5R_4
C254
.1U/10V/X5R_4
C259
.1U/10V/X5R_4
C256
.1U/10V/X5R_4
C270
.1U/10V/X5R_4
C252
.1U/10V/X5R_4
C471
.1U/10V/X5R_4
C474
22U/6.3V_8
R496
0_J_8
Width>40 mil
Trace<200 mil
R495
*0_J_8
R241
2.49K_F_4
1.2V source
6/22
XTAL25
XTAL25_1
XTAL25_R
Y2
25MHZ
C260
27P/50V_4
C263
27P/50V_4
Vender suggest
U13
EC-A-01
RTL8111DL
AVDD33
MDIP0
MDIN0
NC/FB12
MDIP1
MDIN1
GND
NC/MDIP2
NC/MDIN2
DVDD12/AVDD12
NC/MDIP3
NC/MDIN3
VCTRL12A/SROUT12
GND
RSET
VCTR12DVDDSR
NC/VDDSR
NC/ENSWREG
CKTAL2
CKTAL1
NC/AVDD33
NC/LV_PLL
LED0
VDD33
DVDD12
LED1/EESK
LED2/EEDI
LED3/EEDO
EECS
GND
DVDD12
VDD33
ISOLATEB
PERSTB
LANWAKEB
CLKREQB
DVDD12
GND
HSIP
HSIN
REFCLK_P
REFCLK_N
EVDD12
HSOP
HSON
GND
NC/SMCLK
NC/SMDATA
34 LAN0_MDI0+
34 LAN0_MDI0-
34 LAN0_MDI1+
34 LAN0_MDI1-
34 LAN0_MDI2+
34 LAN0_MDI2-
34 LAN0_MDI3+
34 LAN0_MDI3-
21 PCIE_TXP3
21 PCIE_TXN3
C257
0.1U/10V/X7R_4
C258
0.1U/10V/X7R_4
PCIE_RXN3_C
PCIE_RXP3_C
PCIE_RXN3 21
PCIE_RXP3 21
CLK_PCIE_LOMN 21
CLK_PCIE_LOMP 21
R238
*10K_F_4
PCIE_WAKE# 19,30
CLK_PCIE_LAN_REQ# 21
R494
*1K_J_4
U22
EECS
LED1/EESK
LED2/EEDI
LED3/EEDO
CS
SK
DI
DO
VCC
DC
ORG
GND
*AT93C46A(3.3V)
R493
3.6K_F_6
C470
*0.1U/16V/Y5V_4
LED0
D57
1SS355
LAN_ACT# 34
LED1/EESK
D58
*1SS355
LAN_LINK# 34
R514
0_J_6
LED3/EEDO
R239
0_J_6
LAN_LINK1# 34
+3V
R492
1K_J_4
R236
15K_J_4
U12
TC7SH08FU
LAN_REST#
PLTRST#
10,21,22,28,30
R237
*0_J_4
+3VPCU
PR201
100K_J_6
PQ50
AO3413
C329
1U/6.3V_6
36 LAN_PWRON
PQ51
DTC144EUA-7-F
3V_LAN
R499
*0_J_8
CTRL12/VDD
R498
0_J_8
CTRL12/VDD
Quanta Computer Inc.
PROJECT : ZN2
Size
Document Number
LAN(RTL8111DL)
Rev
1A
Date: Tuesday, March 16, 2010
Sheet 33 of 49

LAN Transformer & EOS CONN to RJ45



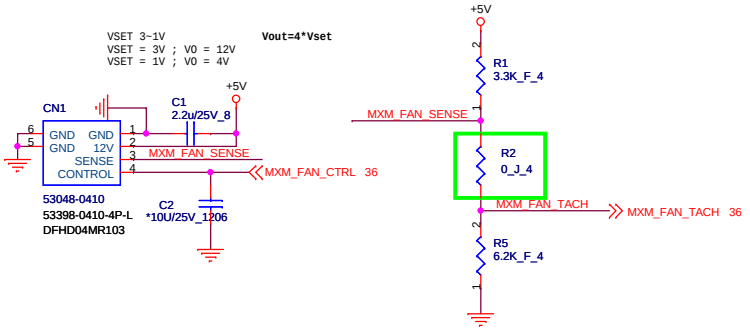
Quanta Computer Inc.

PROJECT : ZN2

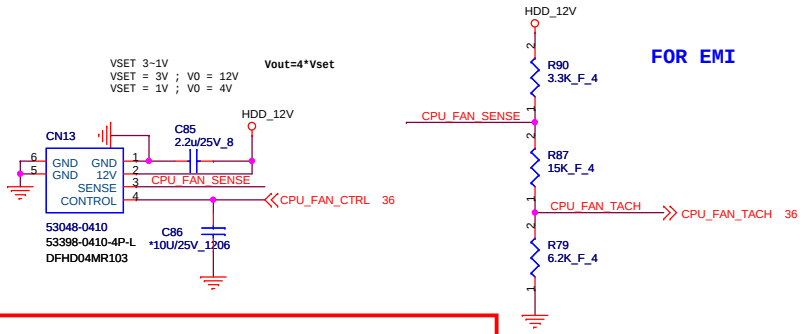
Size	Document Number	Rev
	LAN Transformer & RJ45	1A

Date: Tuesday, March 16, 2010 Sheet 34 of 49

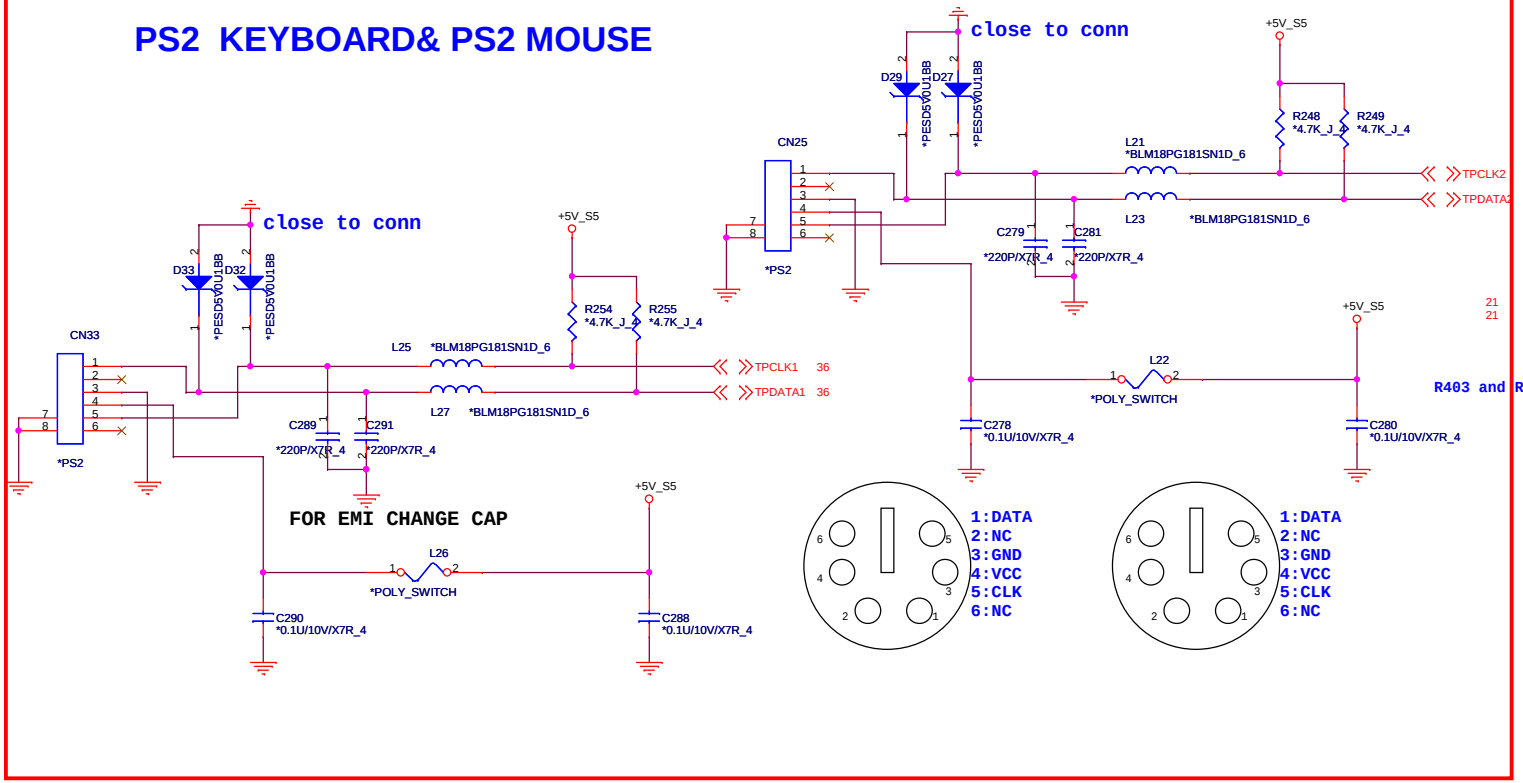
2nd FAN CONN



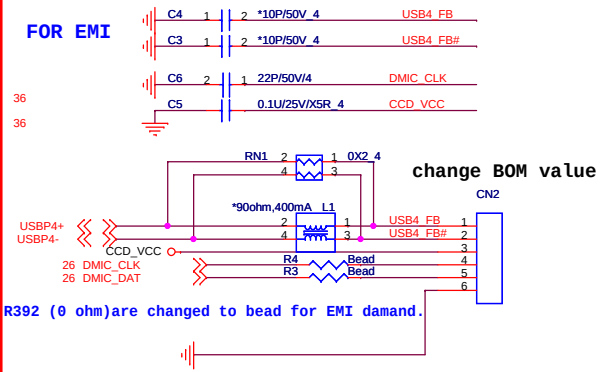
SYSTEM FAN CONN



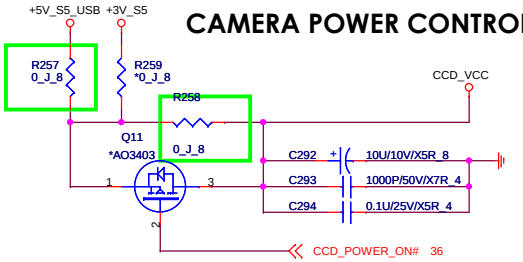
PS2 KEYBOARD& PS2 MOUSE



TO WEB CAM MODULE



CAMERA POWER CONTROL

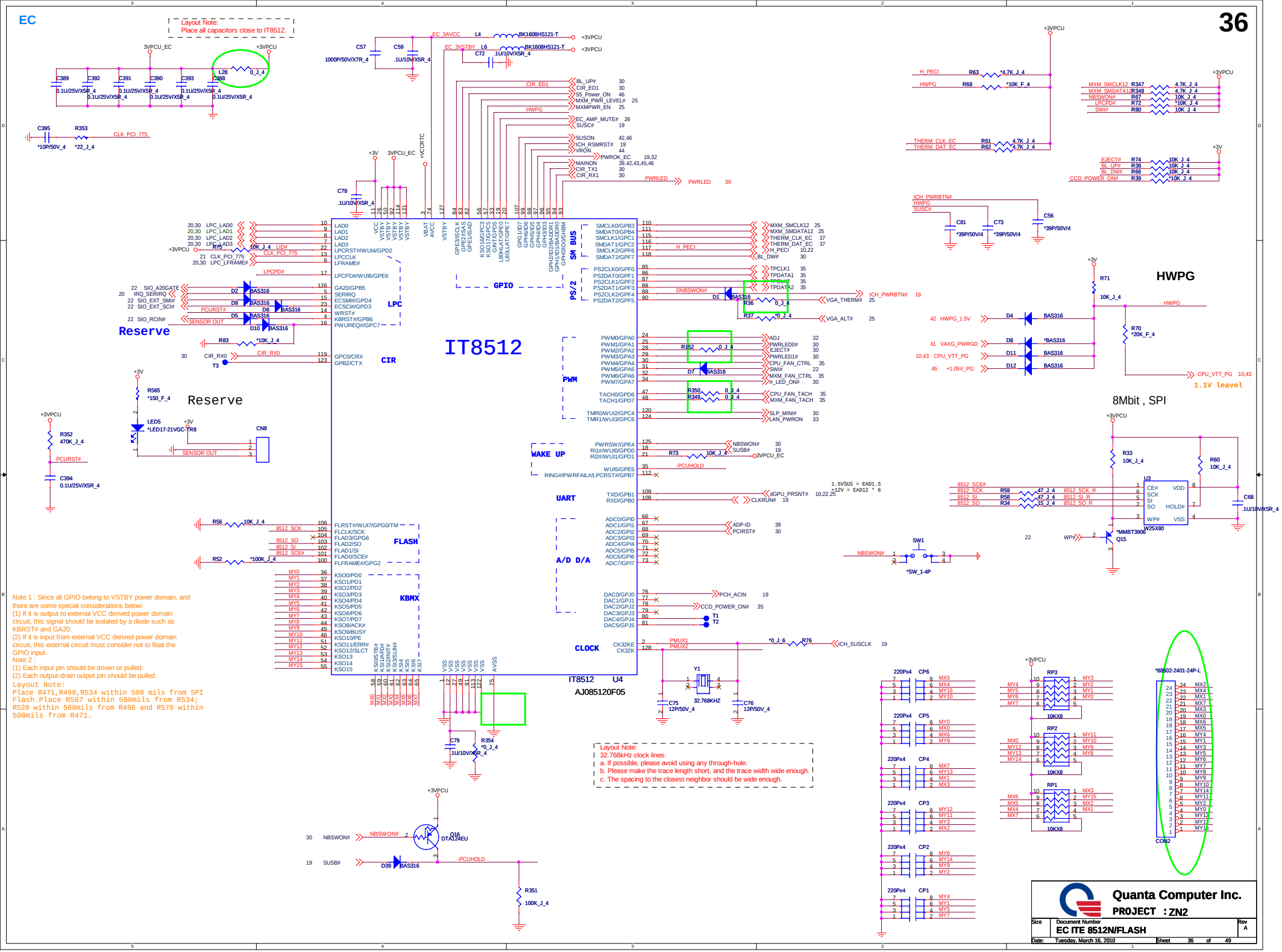


Quanta Computer Inc.

PROJECT : ZN2

Size	Document Number	Rev
	FAN/Webcam/PS2	A

Date: Tuesday, March 16, 2010 Sheet 35 of 49

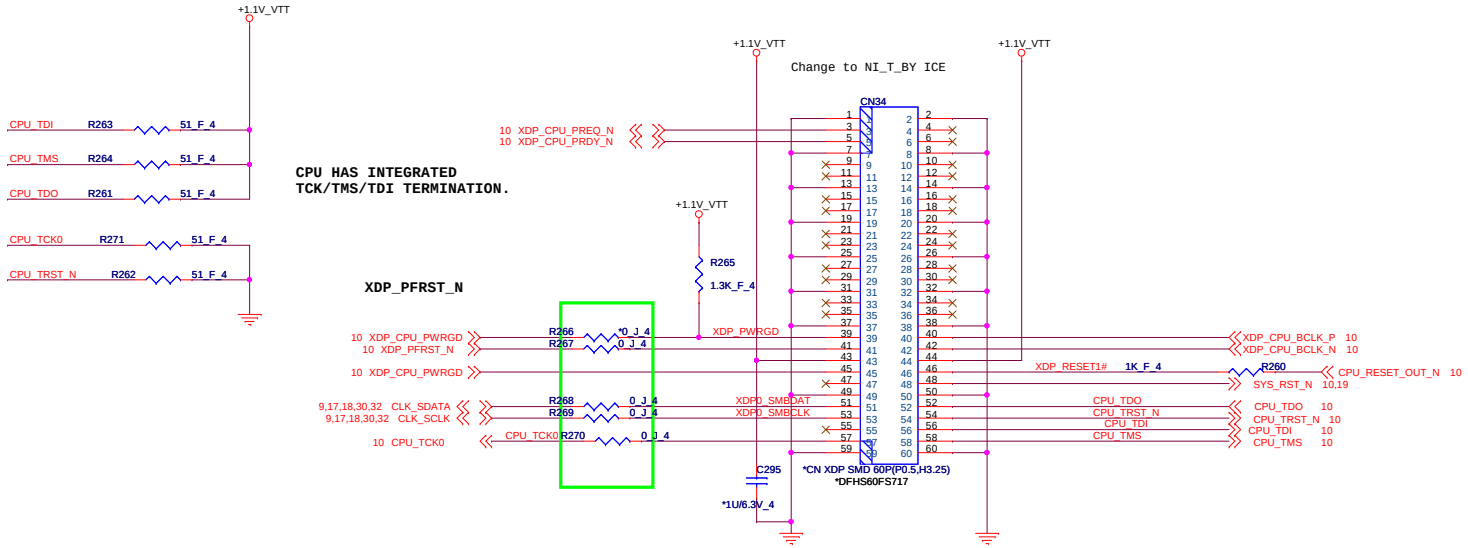


EC
36
Layout Note:
Place all capacitors close to IT8512.
IT8512
IT8512 U4
AJ085120F05
GPIO
SM BUS
PS/2
LPC
CIR
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
Reserve
Reserve
HWPG
8Mbit , SPI
1.1V leavel
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534;
R520 within 500mils from R498 and R570 within 500mils from R471.
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
Quanta Computer Inc.
PROJECT : ZN2
Size
Document Number
EC ITE 8512N/FLASH
Rev
A
Date: Tuesday, March 16, 2010
Sheet 36 of 49

CPU XDP Connector

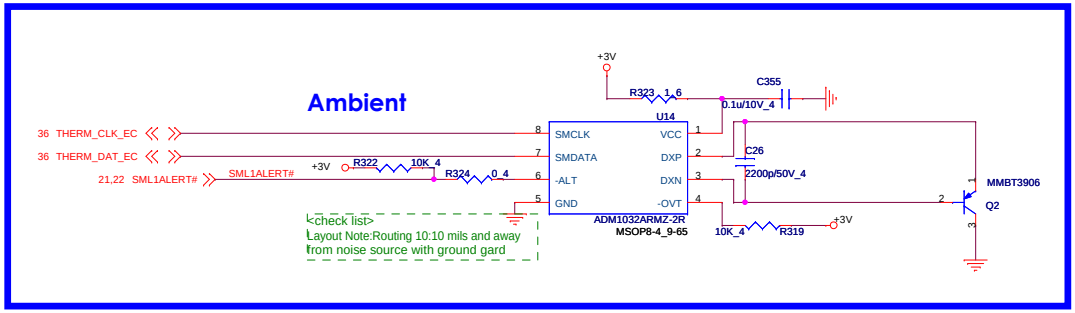
XDP0 - CPU

bsh-060-01-l-d-60p-ldv
bsh-060-01-l-d-60p-ldv



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

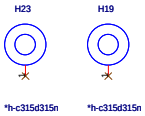
PCH XDP Connector



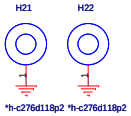
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	XDP	A
Date: Tuesday, March 16, 2010	Sheet 37 of 49	

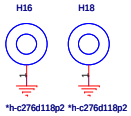
Coaxil conn



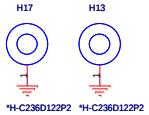
WLAN



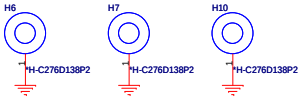
TV



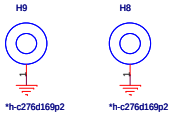
MXM



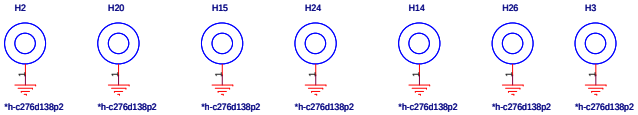
CPU frame



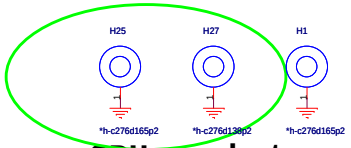
CPU fan



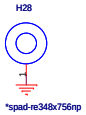
Board screw holes



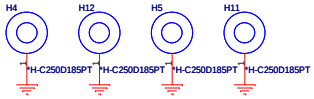
GND SHAPE for EMI in DDR3



Delete



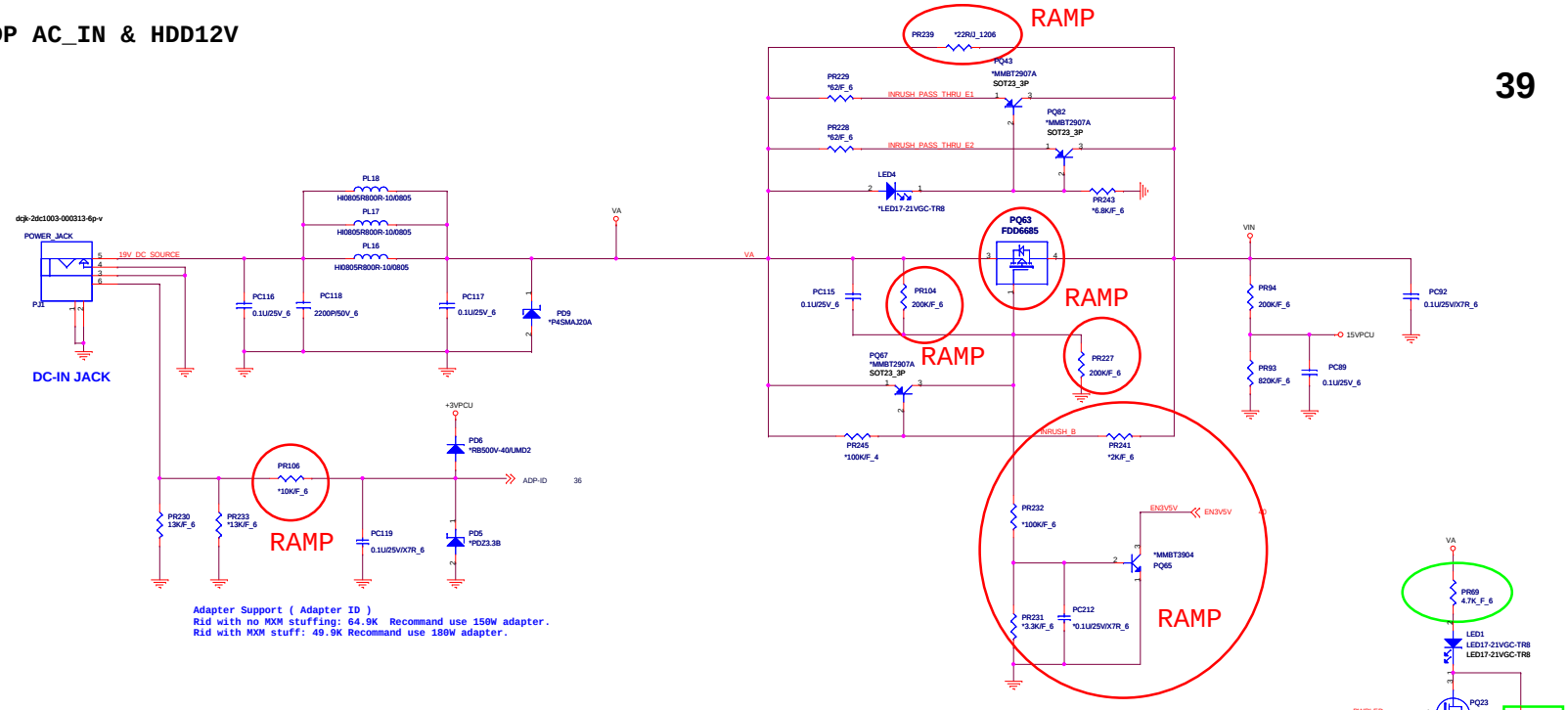
CPU socket



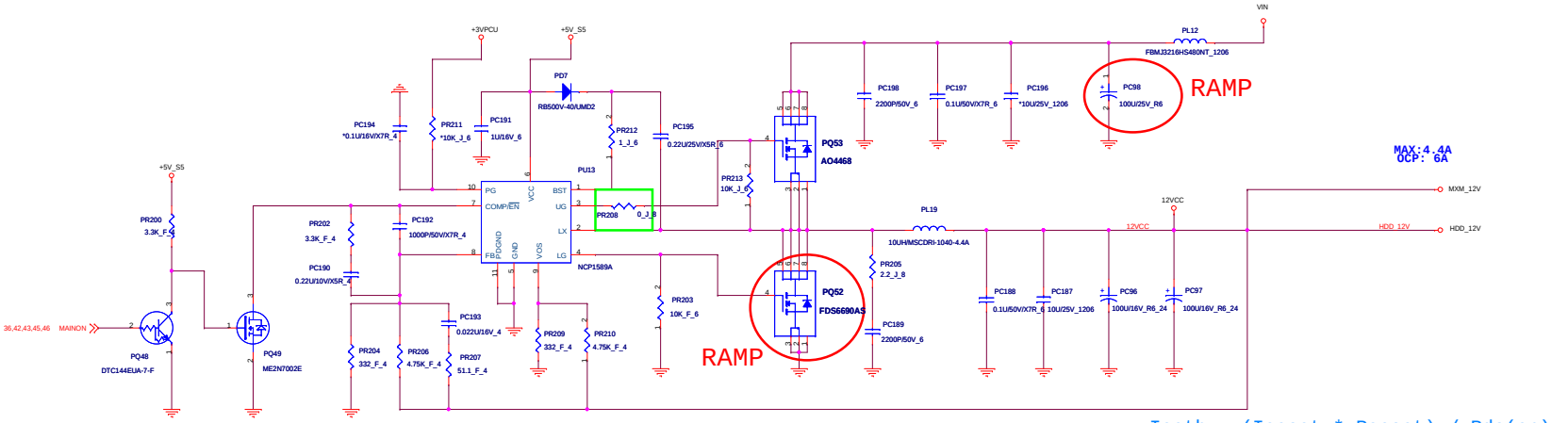
Need discuss with ME/EMI

Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: Screw Hole	Rev: 1A
Date: Tuesday, March 16, 2010	Sheet 38 of 49	

ADP AC_IN & HDD12V



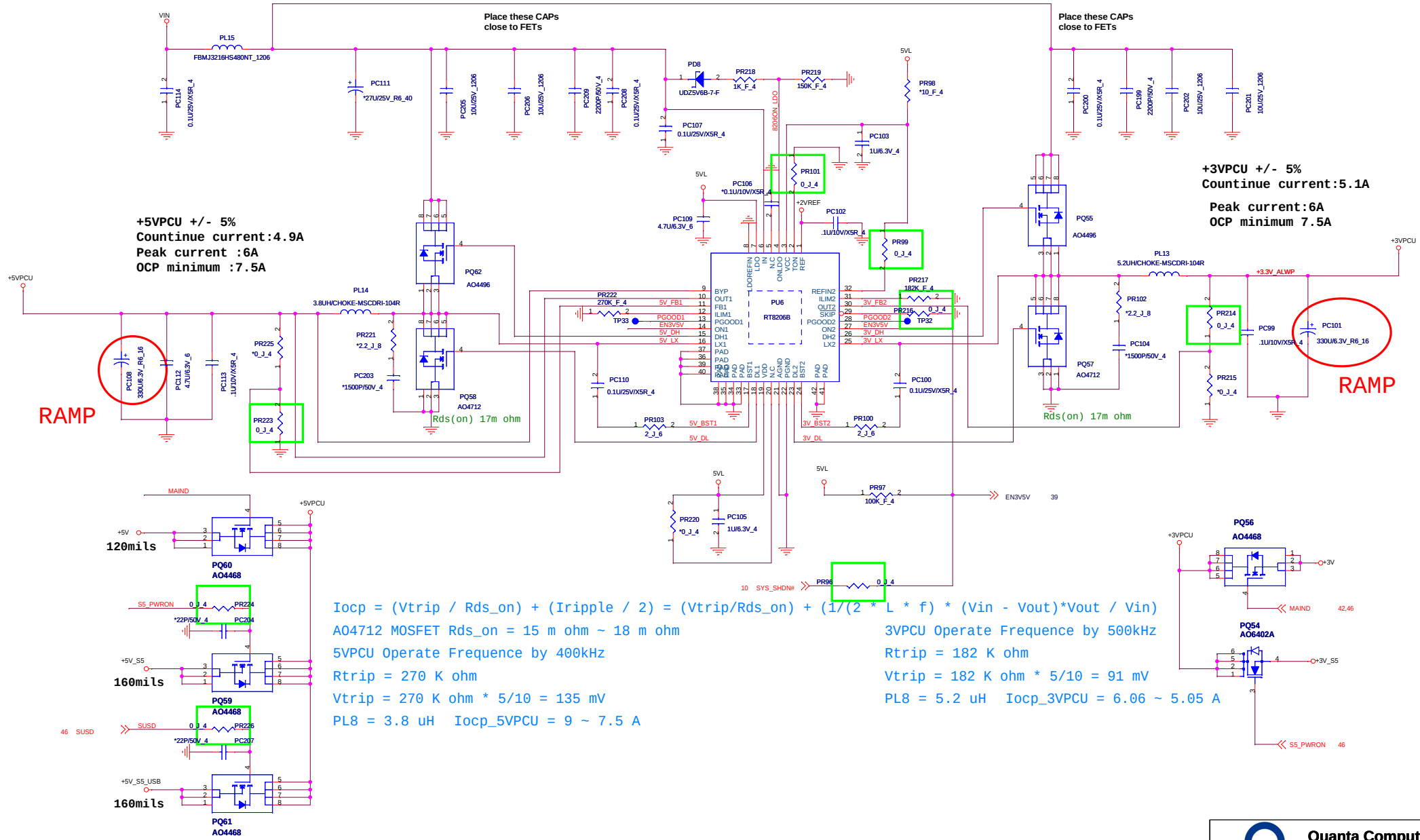
Adapter Support (Adapter ID)
Rid with no MXM stuffing: 64.9K Recommand use 150W adapter.
Rid with MXM stuff: 49.9K Recommand use 180W adapter.



Iocth = (Iocset * Rocset) / Rds(on)
FDS6690AS Rds(on) = 15 m ohm
Iocset = 10 uA
Rocset(R266) = 10 k ohm
Iocth = (10 uA * 10 k) / 15 m ohm = 6.667A

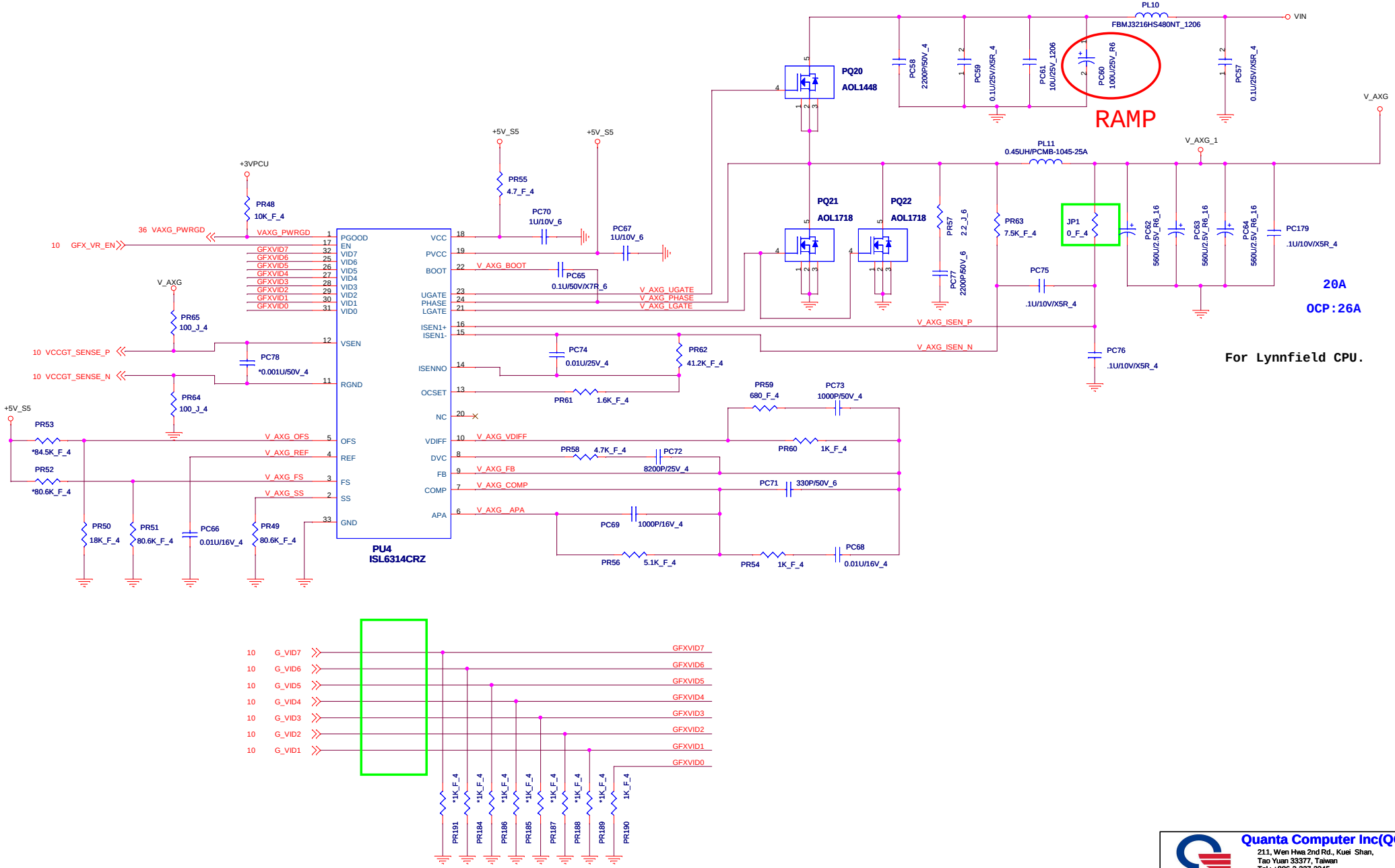
Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number	Rev
	AC in & HDD12V	1A
Date: Tuesday, March 16, 2010	Sheet 39 of 49	

SYSTEM POWER +3V_VPCU/+5V_VPCU/+5V/+3V/+5V_S5/+3V_S5



Quanta Computer Inc.			
PROJECT : ZN2			
Size	Document Number		Rev
	+5V_VPCU/+3V_VPCU (RT8206B)		1A
Date: Tuesday, March 16, 2010		Sheet 40 of 49	

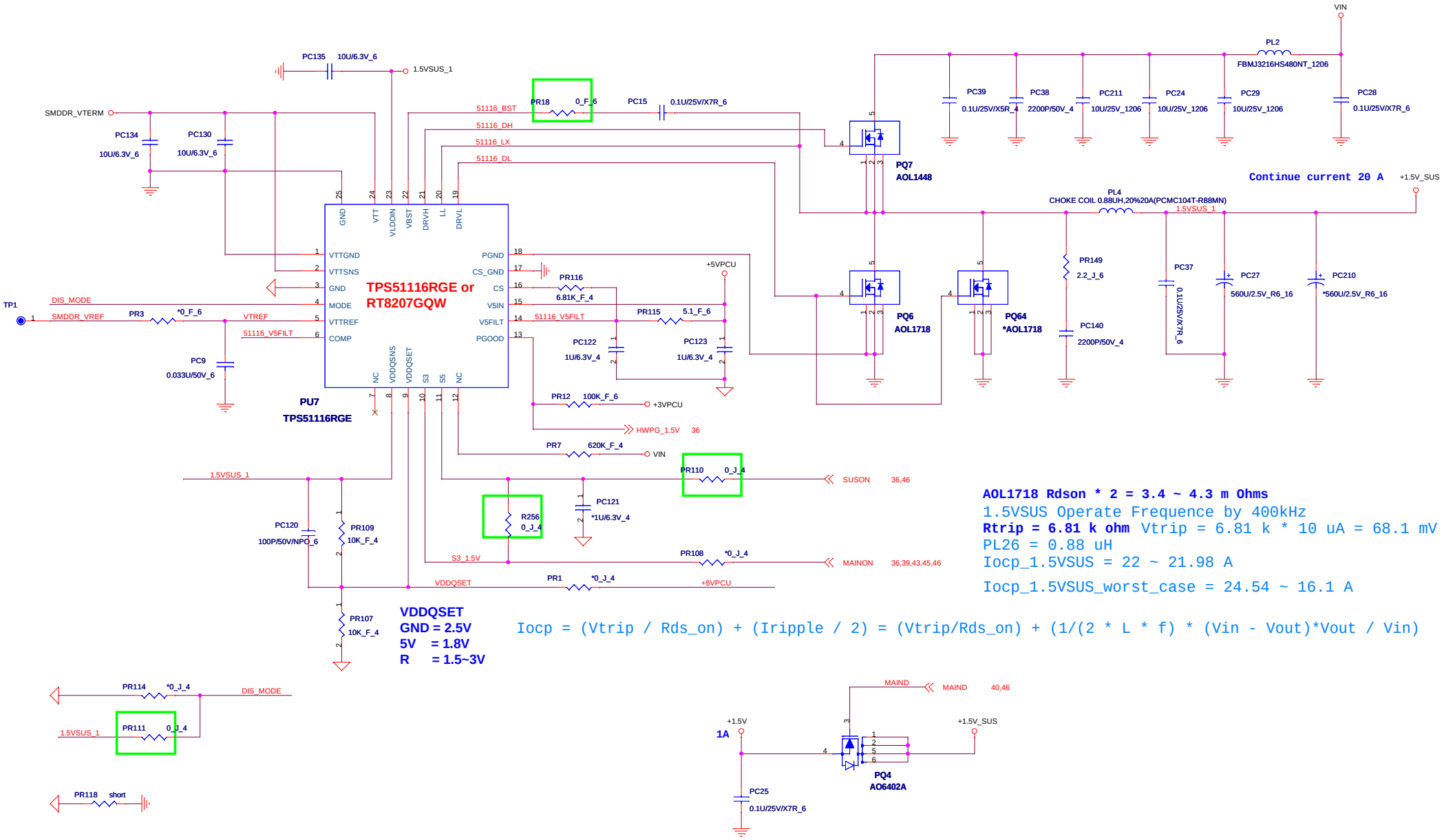
V_AXG



Quanta Computer Inc(QCI).
211, Wen Hwa 2nd Rd., Kuei Shan,
Tao Yuan 33377, Taiwan
Tel : +886-3-327-2345

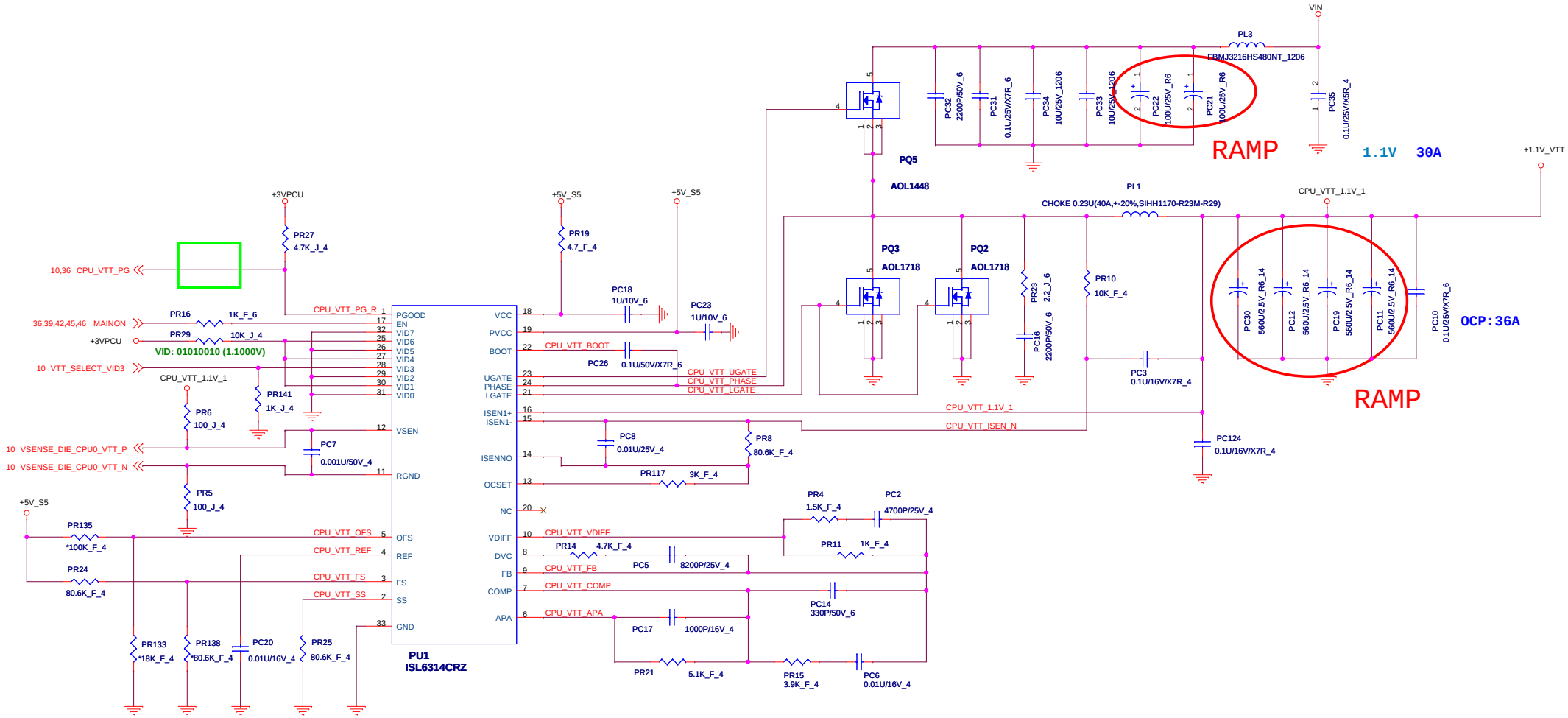
Title	ZN2	
Size: Custom	Document Number: V_AXG(GFX)	Rev: A01
Date: Tuesday, March 16, 2010	Sheet 41 of 49	

DDR3_1.5V(TPS51116)



Quanta Computer Inc.			
PROJECT : ZN2			
Size	Document Number		Rev
	DDR3 1.5V(TPS51116)		1A
Date: Tuesday, March 16, 2010	Sheet 42 of 49		

CPU_VTT(1.1V)



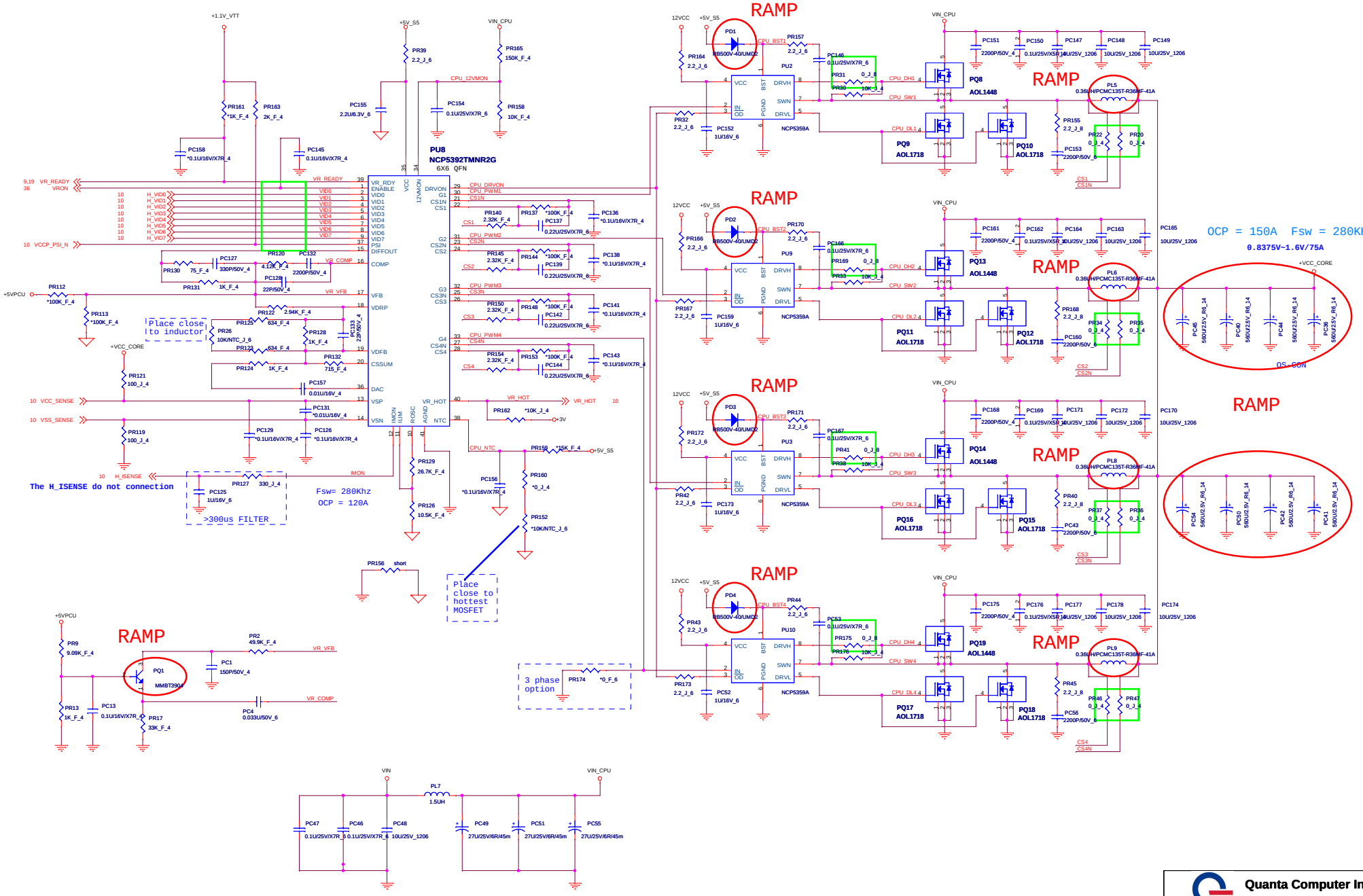
Quanta Computer Inc.

PROJECT : ZN2

Size	Document Number	Rev
	CPU_VTT_1.1V	1A

Date: Tuesday, March 16, 2010 Sheet 43 of 49

CPU_CORE(NCP5392)

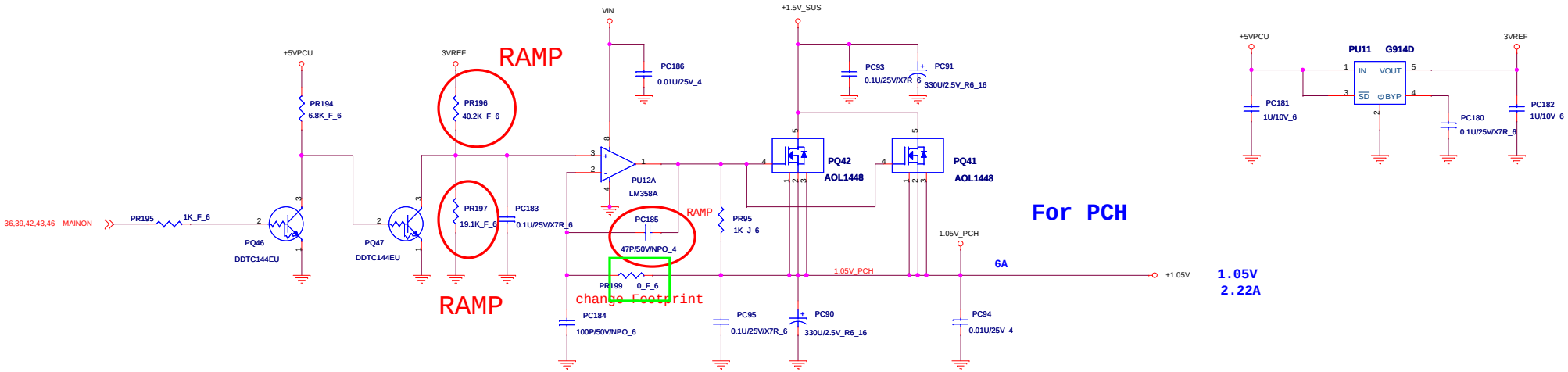


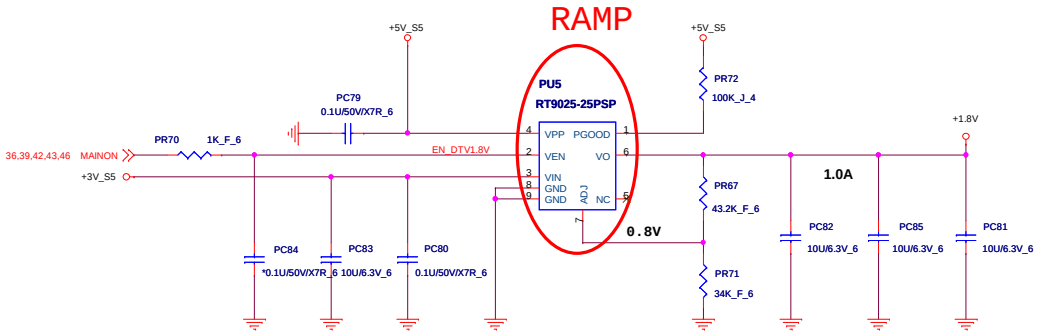
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	CPU_CORE(VCC_CORE)	1A

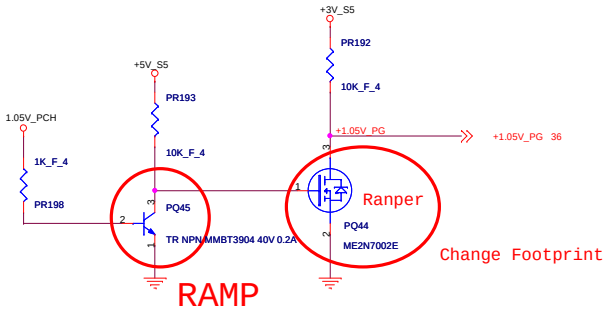
Date: Tuesday, March 16, 2010 Sheet 44 of 49

1.05V_PCH, 1.05V_ME, 1.8V_SRF



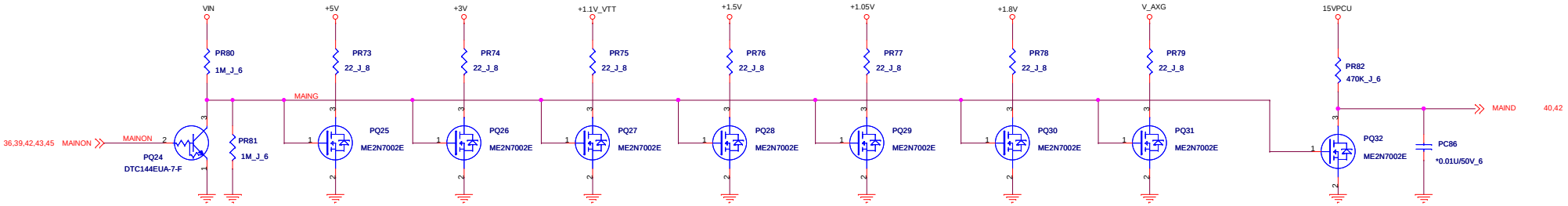


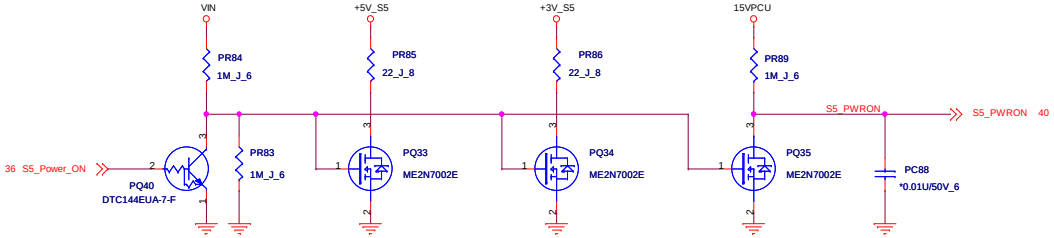
Vout =0.8(1+R1/R2) =1.8V

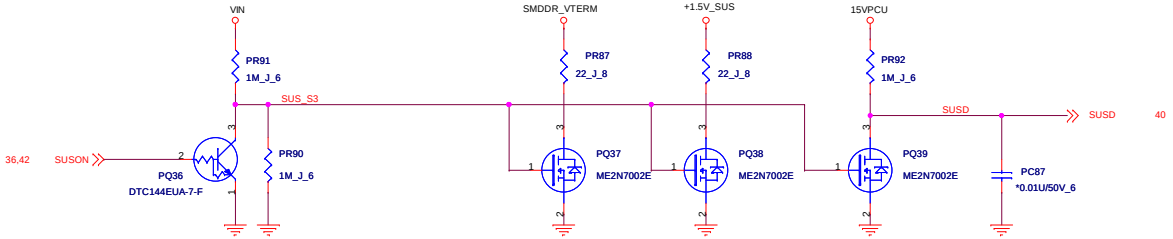


Quanta Computer Inc.		
PROJECT : ZN2		
Size	Document Number: 1.05V_PCH, 1.05V_ME,1.8V	Rev: 1A
Date: Tuesday, March 16, 2010	Sheet 45 of 49	

Discharge







Quanta Computer Inc.

PROJECT : ZN2

Size	Document Number	Rev
	Discharge Circuit	1A

Date: Tuesday, March 16, 2010 Sheet 46 of 49

DATE	ZN2 Schematic file	ZN2 Board file	Revision

DATE	Schematic Change Description
10.Oct.2009	1. Add +3V pull up trace to CPU_SEL (page 09)
10.Oct.2009	2. Add the VTT_Select circuit as EL5 does. (page 10)
10.Oct.2009	3. Change the off page symbol of FDI Sync and Int as output from PCH to Processor. (Page 19)
10.Oct.2009	4. Populate the series resistance with ICH_PWRBTN# to EC. (Page 19)
10.Oct.2009	5. Add the CLKRUN# net from EC to ICH. (Page 36)
10.Oct.2009	6. Change the off page symbol of PMSYNC as the output type from PCH. (Page 19)
10.Oct.2009	7. Add the test point for L_BKLTCTL (Page 19)
10.Oct.2009	8. Correct the connection of the following net names: PWROK_EC, MXM_LVDS_BLON, MXM_LVDS_PWREN, (Page 32)
10.Oct.2009	9. Correct the connection of LCD_CLK and LCD_DAT. (Page 19)
10.Oct.2009	10. Remove the nets of CRT function and HDMI audio on MXM (Page 25)
11.Oct.2009	11. Remove the redudant enable for unused port and add the switch IC for DP dual mode. (Page 19)
11.Oct.2009	12. Add the capacitors for SATA transmitor. (Page 20)
11.Oct.2009	13. Add GPIO WRITE_EDID_ROM for L10 EDID update (Page 22)
11.Oct.2009	14. Remove the HDMI audio from PCH to MXM (Page 20)
11.Oct.2009	15. Reserve the GPIO CR_CPPE# of PCH. (Page 22)
11.Oct.2009	16. Add the function for CLR_BIOS_DATA and CLR_PASSWD. (Page 22)
11.Oct.2009	17. Correct the symbol of CLR_BIOS_DATA and CLR_PASSWD. (Page 29)
11.Oct.2009	18. Correct the STAT capacitors of ODD to receiver. (Page 29)
11.Oct.2009	19. Use 5V_PCU and +5V_S5 to CN21. (Page 30)
11.Oct.2009	20. Reserve the GPIO control of CCD_POWER_ON#. (Page 36)
11.Oct.2009	21. Delete CRT debug from MXM. (Page 25)
12.Oct.2009	22. Correct the power net for 3VPCU and 5VPCU. (Page 30, 26, 27, 36)
12.Oct.2009	23. Correct the connection of M_A_DQ46 and M_A_DQ47. (Page 17)
12.Oct.2009	24. Correct the net name to VR_HOT. (Page 10)
12.Oct.2009	25. Change the net name of USB4_FB and USB4_FB#. (Page 35)
12.Oct.2009	**26. Change the net name of DDR3 VTT to DDR_VTERM. (Page 17, 18) ==> no change~!!!**
12.Oct.2009	27. Reserve the resistnaces for CK0 and CK1 pairs of CHA and CHB. (Page 17, 18)
12.Oct.2009	28. Change the MXM_12V on MXM page. (Page 25)
27.Nov.2009	29. Change net VR_ready Pull High(Page 9)
27.Nov.2009	30. Delete MXM to VGA port circuit(Page 25/27)
27.Nov.2009	31. Change ACN4 to right angle typy(Page26)
27.Nov.2009	32. Delete CN16 XDP connect (Page37)
27.Nov.2009	33. Swap USB2, USB3, USB10, differential signal(Page31)
27.Nov.2009	34. Delete all JP connection
27.Nov.2009	35. CN14 LCD_Clk & LCD_Data swap(Page25)
27.Nov.2009	36. CLK_LPC_DEBUG net change to CN17 pin19(Page30)
27.Nov.2009	37. PEG_CLKREQ#_R pull low,Change R457 resistor to R454(Page21)

DATE	ZN2 Schematic file	ZN2 Board file	Revision

DATE	Schematic Change Description
27.Nov.2009	38. Change ACin Soft start Function and add Adaptor ID to identify Function and disable ID to identify and delete Short Pad JP5, JP6 (Page 39)
27.Nov.2009	39. Delete Short Pad PJP7, PJP8, PJP9, PJP10, PJP11, PJP12 (Page 40)
27.Nov.2009	40. Delete short Pad PJP4, PJP5 and Place up PR190 for V_AXG initial setting Voltage Place up PR48 for V_AXG PG Pull high (Page 41)
27.Nov.2009	41. Change PR116 Value to 6.81K ohm and PL4 Value to 0.88uH and add Location PC210, PC211, PQ64 and delete Short Pad PJP1 (Page 42)
27.Nov.2009	42. Delete Short Pad PJP2, PJP3 (Page 43)
27.Nov.2009	43. Change CPU core Value PR132, PR122, PR140, PR145, PR150, PR154 (Page 44)
27.Nov.2009	44. Delete Short Pad PJP6 (Page 45)
27.Nov.2009	45. Place up PQ27, PQ28, PQ29, PQ30, PQ31, PQ38, PR88 (Page 46)
29.Nov.2009	46. MOVE EC circuit (PAGE 36)'s LED indicate circuit to (Page 39) ACin circuit
2.Dec.2009	47. Connect GFX_VR_EN to dGPU_PRSNT# (Page 10)
2.Dec.2009	48. Add RC circuit for SRTC_RST# (Page 20)
2.Dec.2009	49. Change CLK_PCIE_DMI# differential pair RP15 to L44/L45 (Page 21)
2.Dec.2009	50. Change C328 to 330uF and Delete C329,C335,C336,C343,C344(Page 14)
2.Dec.2009	51. Remove R174 10Kohm(Page 25)
2.Dec.2009	52. Remove R389 , place R374 to 0 ohm, 1394 component, Change U17 to JMB385 (Page 28)
2.Dec.2009	53. Change CN11 to right angle type(Page 29)
2.Dec.2009	54. Place the SATA_ACT circuit component(Page 30)
2.Dec.2009	55. Remove the hall sensor component and add LED5(Page 36)
2.Dec.2009	56. Add SW1 (Page 36)
7.Dec.2009	57. Reverse HDD connect pin (Page 29)
26.Jan.2010	58. Change Write_EDID_ROM to GPIO28 (Page 22)
26.Jan.2010	59. Reserve MXM to CRT function (Page 25/27)
26.Jan.2010	60. Reserve R395 for PEG_CLKREQ pull high (Page 25)
26.Jan.2010	61. Change C274/C276 to 47u (Page 27)
26.Jan.2010	62. Change CN29 Pin2 power to +5V_S5_USB (Page 30)
26.Jan.2010	63. Change F7/F8/F9 power to +5V_S5_USB (Page 31)
26.Jan.2010	64. Change C447,C483,C493,C489,C478,C482,C490,C494,,C287,C399,C265,C472,C469,C466 to 100u/7343 type (Page 31)
26.Jan.2010	65. Add D61 (Page 31)
26.Jan.2010	66. Reserve R232 for Write_EDID_ROM pull low function (Page 32)
26.Jan.2010	67. Add C329 for Lan loss solution (Page 33)
26.Jan.2010	68. CN29 Pin15/16 floating (Page 34)
26.Jan.2010	69. Change R257 power to +5V_S5_USB (Page 35)
26.Jan.2010	70. Reserve R63 (Page 36)
26.Jan.2010	71. Add ADP-ID to EC ADC1 (Page 36/39)
26.Jan.2010	72. Change Screw H23,H19,H2,H4,H5,H11,H28 (Page 38)
26.Jan.2010	73. Change ACin Adaptor ID to identify Function circuit and add delay time for EN3V5V enable circuit(Page 39)

4. Nat name Description :

Voltage Rails

VIN	Primary DC system power supply
+5VPCU	5.0V always on power rail by LATCH or ACIN
+3VPCU	3.3V always on power rail by LATCH or ACIN
+5V_S5	5.0V always on power rail by DCON
+3V_S5	3.3V always on power rail by DCON
+5V_S5_USB	5.0V power rail by SUSD
+3V	3.3V switched power rail by MAIND
+5V	5.0V switched power rail by MAIND
+VCC_CORE	Core Voltage for CPU
CPU_VTT_1.1V	1.1V power rail for AGTL+ termination/Core for GMCH by MAINON
1.05V_PCH	1.05V power rail for PCH Core Power by MAINON
+1.8V	1.8V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for VRM/NVRAM by MAINON
+1.5V	1.5V power rail for MiniPCI by MAIND
+1.5V_SUS	1.5V power rail for DDRIII by SUSON
SMDDR_VTERM	0.75V DDRIII Termination Voltage by MAINON

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Normal Signal / Ground 1 Plane
Layer 5		Power Plane
Layer 6		Solder Side,Microstrip signal Layer

Layers : 6 Depth 1.6mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

Quanta Computer Inc(QCI).
211, Wen Hwa 2nd Rd., Kuei Shan,
Tao Yuan 33377, Taiwan
Tel : +886-3-327-2345
Confidential

Title	ZN2	
Size C	Document Number ZN6C	Rev A02
Date: Tuesday, March 16, 2010	Sheet 49 of 49	