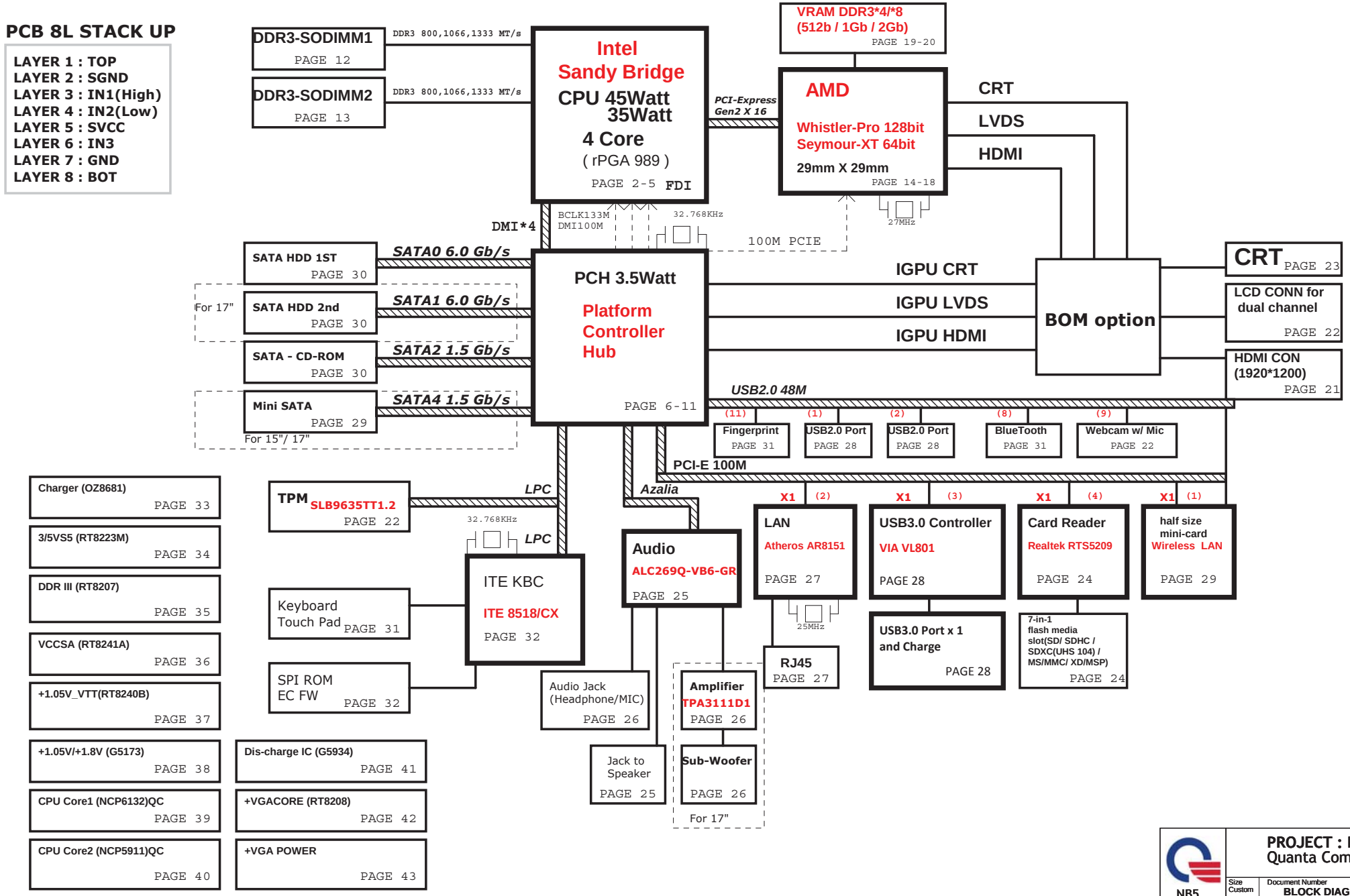
LG2/4 (14"/15.6") MUXLESS and Dis. BLOCK DIAGRAM

01

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

Date: Wednesday, May 18, 2011 Sheet 1 of 47

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U25A

DMI

DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 F20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

Intel(R) FDI

FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]
FDI_FSYNC0 J18 FDI0_FSYNC
FDI_FSYNC1 J17 FDI1_FSYNC
FDI_INT H20 FDI_INT
FDI_LSYNC0 J19 FDI0_LSYNC
FDI_LSYNC1 H17 FDI1_LSYNC

eDP

eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0..15] [14]

PEG_RX#[0] K33 PEG_RX#0
PEG_RX#[1] M35 PEG_RX#1
PEG_RX#[2] L34 PEG_RX#2
PEG_RX#[3] J35 PEG_RX#3
PEG_RX#[4] J32 PEG_RX#4
PEG_RX#[5] H34 PEG_RX#5
PEG_RX#[6] H31 PEG_RX#6
PEG_RX#[7] G33 PEG_RX#7
PEG_RX#[8] G30 PEG_RX#8
PEG_RX#[9] F35 PEG_RX#9
PEG_RX#[10] E34 PEG_RX#10
PEG_RX#[11] E32 PEG_RX#11
PEG_RX#[12] D33 PEG_RX#12
PEG_RX#[13] D31 PEG_RX#13
PEG_RX#[14] B33 PEG_RX#14
PEG_RX#[15] C32 PEG_RX#15

PEG_RX[0..15] [14] [32,39] H_PROCHOT#

PROCTHOT# with two VR topology ..75ohm
PROCTHOT# with one VR topology ..56 ohm

R8217 56.2/F_4 H_PROCHOT#_R AL32
C462 43P/50V_4

[9,32] PM_THRMTRIP# R8221 *0_4/S PM_THRMTRIP#_R AN32

PEG_RX[0] J33 PEG_RX0
PEG_RX[1] L35 PEG_RX1
PEG_RX[2] K34 PEG_RX2
PEG_RX[3] H35 PEG_RX3
PEG_RX[4] H32 PEG_RX4
PEG_RX[5] G34 PEG_RX5
PEG_RX[6] G31 PEG_RX6
PEG_RX[7] F33 PEG_RX7
PEG_RX[8] F30 PEG_RX8
PEG_RX[9] E35 PEG_RX9
PEG_RX[10] E33 PEG_RX10
PEG_RX[11] F32 PEG_RX11
PEG_RX[12] D34 PEG_RX12
PEG_RX[13] E31 PEG_RX13
PEG_RX[14] C33 PEG_RX14
PEG_RX[15] B32 PEG_RX15

PEG_TX#[0] M29 C_PEG_TX#0
PEG_TX#[1] M32 C_PEG_TX#1
PEG_TX#[2] M31 C_PEG_TX#2
PEG_TX#[3] L32 C_PEG_TX#3
PEG_TX#[4] L29 C_PEG_TX#4
PEG_TX#[5] K31 C_PEG_TX#5
PEG_TX#[6] K28 C_PEG_TX#6
PEG_TX#[7] J30 C_PEG_TX#7
PEG_TX#[8] J28 C_PEG_TX#8
PEG_TX#[9] H29 C_PEG_TX#9
PEG_TX#[10] G27 C_PEG_TX#10
PEG_TX#[11] E29 C_PEG_TX#11
PEG_TX#[12] F27 C_PEG_TX#12
PEG_TX#[13] D28 C_PEG_TX#13
PEG_TX#[14] F26 C_PEG_TX#14
PEG_TX#[15] E25 C_PEG_TX#15

PEG_TX[0] M28 C_PEG_TX0
PEG_TX[1] M33 C_PEG_TX1
PEG_TX[2] M30 C_PEG_TX2
PEG_TX[3] L31 C_PEG_TX3
PEG_TX[4] L28 C_PEG_TX4
PEG_TX[5] K30 C_PEG_TX5
PEG_TX[6] K27 C_PEG_TX6
PEG_TX[7] J29 C_PEG_TX7
PEG_TX[8] J27 C_PEG_TX8
PEG_TX[9] H28 C_PEG_TX9
PEG_TX[10] G28 C_PEG_TX10
PEG_TX[11] E28 C_PEG_TX11
PEG_TX[12] F28 C_PEG_TX12
PEG_TX[13] D27 C_PEG_TX13
PEG_TX[14] E26 C_PEG_TX14
PEG_TX[15] D25 C_PEG_TX15

U25B

MISC

[7] H_SNB_IVB# C26 SNB_IVB#
SNB_IVB# N.A at SNB EDS #27637 0.7v1
TP8203 SKTOCC# AN34 SKTOCC#

THERMAL

TP8200 TP_CATERR# AL33 CATERR#
Placement close to EC.
[32] EC_PECI R8463 43_4 H_PECI AN33 PECI
PROCHOT# AL32
THERMTRIP#

PWR MANAGEMENT

[6] PM_SYNC R8222 *0_4/S PM_SYNC_R AM34 PM_SYNC
[9] H_PWRGOOD R8225 *0_4/S H_PWRGOOD_R AP33 UNCOREPWRGOOD
R8226 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
CPU RESET#
U8204 GND OUT IN NC VCC *74LVC1G07GW
+1.05V_VTT R8229 *75_4
CPU_PLTRST# R8252 *43_4 CPU_PLTRST#_R AR33 RESET#
PLTRST# [9,11,22,24,27,28,29,32]
+3VS5 C8236 *0.1U/10V_4
R9113 750/F_4
R9114 1.5K/F_4

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

CLOCKS

BCLK A28 CLK_CPU_BCLKP [8]
BCLK# A27 CLK_CPU_BCLKN [8]
DPLL_REF_SSCLK A16 CLK_DPLL_SSCLKP_R R8215 1K_4
DPLL_REF_SSCLK# A15 CLK_DPLL_SSCLKN_R R10867 1K_4 +1.05V_VTT

DDR3 MISC

SM_DRAMRST# R8 CPU_DRAMRST#
R8219 Change to 25.5 ohm for intel DG.
SM_RCOMP[0] AK1 SM_RCOMP_0 R8218 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R8219 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R8220 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM

CPU XDP
PRDY# AP29 XDP_PRDY# TP9008
PREQ# AP27 XDP_PREQ# TP9009
TCK AR26 XDP_TCLK TP9010
TMS AR27 XDP_TMS TP9011
TRST# AP30 XDP_TRST# TP9012
TDI AR28 XDP_TDI_R TP9013
TDO AR26 XDP_TDO TP9014
R9029 *1K_4 +3V
DBR# AL35 XDP_DBRST# XDP_DBRST# [6]
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

SM_DRAMPWROK Processor Input.

+3VS5 R8560 *10K_4
PM_DRAM_PWRGD_PU
U8203 NC VCC IN GND OUT *74LVC1G07GW
C8235 *0.1U/10V_4
+1.5V_CPU R8232 200/F_4
PM_DRAM_PWRGD_C R8233 130/F_4 PM_DRAM_PWRGD_R
R9030 *39_4
R9051 *0_4
PM_DRAM_PWRGD [6]
MAIN_ONG [4,41]
R9115 *0_4/S PM_DRAM_PWRGD_C
R9116 *3K/F_4
Q8200 *2N7002

DDR3 DRAM RESET

+1.5VSUS R8250 1K_4 R8251 *0_4
[12,13] DDR3_DRAMRST# R9031 1K_4 CPU_DRAMRST#
CPU_DRAMRST#_R
[8,12,13] DRAMRST_CNTRL_PCH R8254 *0_4/S
Q8205 2N7002
C8245 0.047U/10V_4
R8255 4.99K/F_4

[6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[6,7,8,9,10,27,29,32,34,37,38,41,43] +3VS5
[4,10,29] +1.5V_CPU
[4,6,7,8,10,28,32,37,38,39] +1.05V_VTT

FDI disable (DIS only stuff)

FDI_INT
R8235 0_4 FDI_FSYNC0
R8236 0_4 FDI_FSYNC1
R8237 0_4 FDI_LSYNC0
FDI_LSYNC1
R8240 1K_4
R8234 1K_4

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

[14] PEG_TX[0..15]

C_PEG_TX0	C8227	0.1U/10V_4	PEG_TX0
C_PEG_TX1	C8228	0.1U/10V_4	PEG_TX1
C_PEG_TX2	C8229	0.1U/10V_4	PEG_TX2
C_PEG_TX3	C8230	0.1U/10V_4	PEG_TX3
C_PEG_TX4	C8231	0.1U/10V_4	PEG_TX4
C_PEG_TX5	C8232	0.1U/10V_4	PEG_TX5
C_PEG_TX6	C8233	0.1U/10V_4	PEG_TX6
C_PEG_TX7	C8237	0.1U/10V_4	PEG_TX7
C_PEG_TX8	C8234	0.1U/10V_4	PEG_TX8
C_PEG_TX9	C8238	0.1U/10V_4	PEG_TX9
C_PEG_TX10	C8239	0.1U/10V_4	PEG_TX10
C_PEG_TX11	C8240	0.1U/10V_4	PEG_TX11
C_PEG_TX12	C8241	0.1U/10V_4	PEG_TX12
C_PEG_TX13	C8242	0.1U/10V_4	PEG_TX13
C_PEG_TX14	C8243	0.1U/10V_4	PEG_TX14
C_PEG_TX15	C8244	0.1U/10V_4	PEG_TX15

0.22uF AC coupling Caps for PCIE GEN1/2/3

[14] PEG_TX#[0..15]

C_PEG_TX#0	C8212	0.1U/10V_4	PEG_TX#0
C_PEG_TX#1	C8213	0.1U/10V_4	PEG_TX#1
C_PEG_TX#2	C8214	0.1U/10V_4	PEG_TX#2
C_PEG_TX#3	C8215	0.1U/10V_4	PEG_TX#3
C_PEG_TX#4	C8216	0.1U/10V_4	PEG_TX#4
C_PEG_TX#5	C8217	0.1U/10V_4	PEG_TX#5
C_PEG_TX#6	C8218	0.1U/10V_4	PEG_TX#6
C_PEG_TX#7	C8219	0.1U/10V_4	PEG_TX#7
C_PEG_TX#8	C8220	0.1U/10V_4	PEG_TX#8
C_PEG_TX#9	C8221	0.1U/10V_4	PEG_TX#9
C_PEG_TX#10	C8222	0.1U/10V_4	PEG_TX#10
C_PEG_TX#11	C8223	0.1U/10V_4	PEG_TX#11
C_PEG_TX#12	C8224	0.1U/10V_4	PEG_TX#12
C_PEG_TX#13	C8225	0.1U/10V_4	PEG_TX#13
C_PEG_TX#14	C8226	0.1U/10V_4	PEG_TX#14
C_PEG_TX#15	C8200	0.1U/10V_4	PEG_TX#15

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+1.05V_VTT R9016 10K_4 INT_eDP_HPD_Q
+1.05V_VTT R8243 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT R8244 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

PROCTHOT# with two VR topology ..100ohm
PROCTHOT# with one VR topology ..62 ohm

+1.05V_VTT

H_PROCHOT#	R8239	62_4
XDP_TDO	R9022	51_4
XDP_TMS	R8241	51_4
XDP_TDI_R	R8242	51_4
XDP_PREQ#	R8245	*51_4
XDP_TCLK	R8246	51_4
XDP_TRST#	R8247	51_4

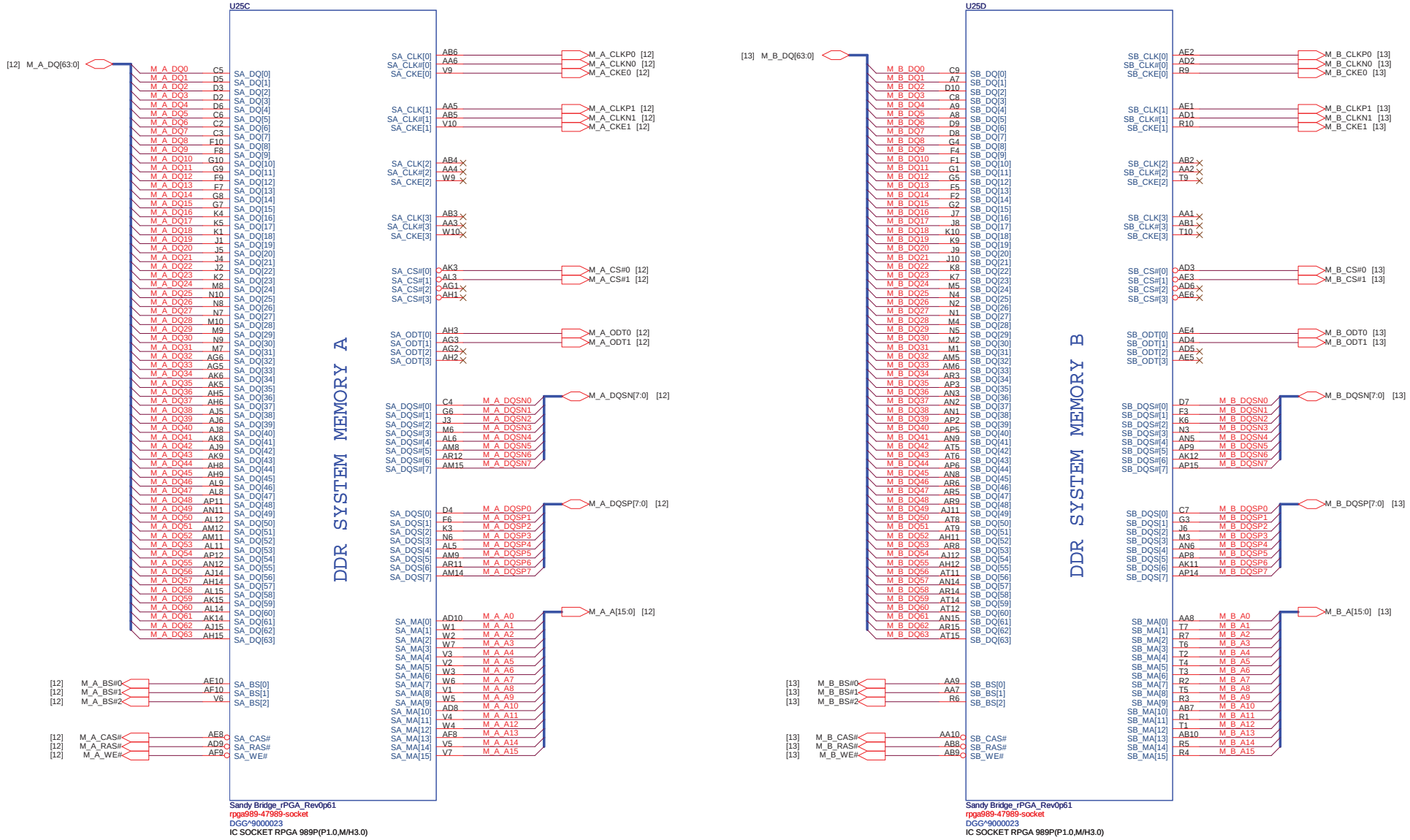
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	3A

Date: Wednesday, May 18, 2011 Sheet 2 of 47

Sandy Bridge Processor (DDR3)



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	3A

Date: Wednesday, May 18, 2011 Sheet 3 of 47

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

U25F

SNB: 55A

+VCC_CORE

C8289 22U/6.3VS_8 C8290 22U/6.3VS_8 C8327 22U/6.3VS_8
C8335 22U/6.3VS_8 C8348 22U/6.3VS_8 C8328 22U/6.3VS_8
C8285 22U/6.3VS_8 C8314 *22U/6.3VS_8 C8315 22U/6.3VS_8
C8311 22U/6.3VS_8 C8312 22U/6.3VS_8 C8313 22U/6.3VS_8
C8329 22U/6.3VS_8 C8309 22U/6.3VS_8 C8310 22U/6.3VS_8
C8326 22U/6.3VS_8 C8295 22U/6.3VS_8 C8288 22U/6.3VS_8
C8325 22U/6.3VS_8 C8339 22U/6.3VS_8 C8340 22U/6.3VS_8
C8336 *22U/6.3VS_8 C8337 22U/6.3VS_8 C8338 22U/6.3VS_8
C8345 22U/6.3VS_8 C8346 22U/6.3VS_8 C8347 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SNB: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C8269 22U/6.3VS_8 C8279 22U/6.3VS_8 C8282 22U/6.3VS_8
C8302 22U/6.3VS_8 C8318 22U/6.3VS_8 C8284 22U/6.3VS_8
C8298 *22U/6.3VS_8 C8319 22U/6.3VS_8 C8316 22U/6.3VS_8
C8303 *22U/6.3VS_8 C8301 *22U/6.3VS_8 C8317 *22U/6.3VS_8
C8280 22U/6.3VS_8 C8270 22U/6.3VS_8 C8271 *22U/6.3VS_8
C8253 *22U/6.3VS_8 C8254 22U/6.3VS_8 C8256 *22U/6.3VS_8
C8257 *22U/6.3VS_8 C8258 22U/6.3VS_8 C8272 *22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT_40 R8257 *0_4/S

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE AJ35
VSS_SENSE AJ34

R8263 100_4 +VCC_CORE
VCC_SENSE [39]
VSS_SENSE [39]
R8265 100_4

Add for intel CRB

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCP_SENSE [37]
VSSP_SENSE [37]
+1.05V_VTT
VCCP_SENSE R10863 *10_4
VSSP_SENSE R10864 *10_4

[2,12,13,35,36,43] +1.5VSUS
[2,10,29] +1.5V_CPU
[2,6,7,8,10,28,32,37,38,39] +1.05V_VTT
[36] +VCCSA
[40] +VCC_GFX
[40] +VCC_CORE

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

U25G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

C8267 *22U/6.3VS_8 C8259 *22U/6.3VS_8
C8276 *22U/6.3VS_8 C8277 *22U/6.3VS_8
C8278 *22U/6.3VS_8 C8307 *22U/6.3VS_8
C8275 *22U/6.3VS_8 C8306 *22U/6.3VS_8
C8321 *22U/6.3VS_8 C8323 *22U/6.3VS_8
C8260 *22U/6.3VS_8 C8322 *22U/6.3VS_8

Ra R8258 0_4

	DIS	Muxless/UMA
Ra	Stuff	NC

+1.8V SNB: 1.5A

C8341 10U/6.3V_8 C8342 1U/6.3V_4 C8343 1U/6.3V_4

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

1.8V RAIL

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R8408 10/F_4 +VCC_GFX
VCC_AXG_SENSE [39]
VSS_AXG_SENSE [39]
R8346 10/F_4

VREF

SM_VREF AL1

+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
R8271 *0_8 DDR_VTTREF [12,13,35]
R8269 100K_4
Q8207 2N7002
MAIND MAIND [41]

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A +1.5V_CPU

C8291 10U/6.3V_8 C8292 10U/6.3V_8 C8293 10U/6.3V_8 C8294 10U/6.3V_8
C8299 10U/6.3V_8 C8300 10U/6.3V_8 C8308 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 J26
VCCSA4 J25
VCCSA5 J24
VCCSA6 H26
VCCSA7 H25
VCCSA8 H25

SNB: 6A +VCCSA

C8330 10U/6.3V_8 C8331 10U/6.3V_8 C8332 10U/6.3V_8 C8333 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23
VCCUSA_SENSE_R R8566 *0_4/S VCCUSA_SENSE [36]
VCCSA_SEL0 [36]
R8259 10K_4
VCCSA_SEL [36]
R9157 10K_4
VCCSA_SEL0 for intel CRB

FC_C22 C22
VCCSA_VID1 C24

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK [39]

+1.05V_VTT

Place PU resistor close to CPU

R8266 130/F_4

SVID DATA

H_CPU_SVIDDAT VR_SVID_DATA [39]

Place PU resistor close to CPU

SVID ALERT

+1.05V_VTT R8270 75_4
H_CPU_SVIDALRT# R8272 43_4 VR_SVID_ALERT# [39]

+1.5VSUS JP8200 *SOLDERJUMPER-2 +1.5V_CPU +1.5VSUS

Q8206 AON7410

R8207 220_8

C9036 0.1U/10V_4
C9037 0.1U/10V_4
C9038 0.1U/10V_4
C9039 0.1U/10V_4

MAIND

C8350 *470P/50V_4

Q8202 2N7002

MAIN_ONG [2,41]

CPU VDDQ

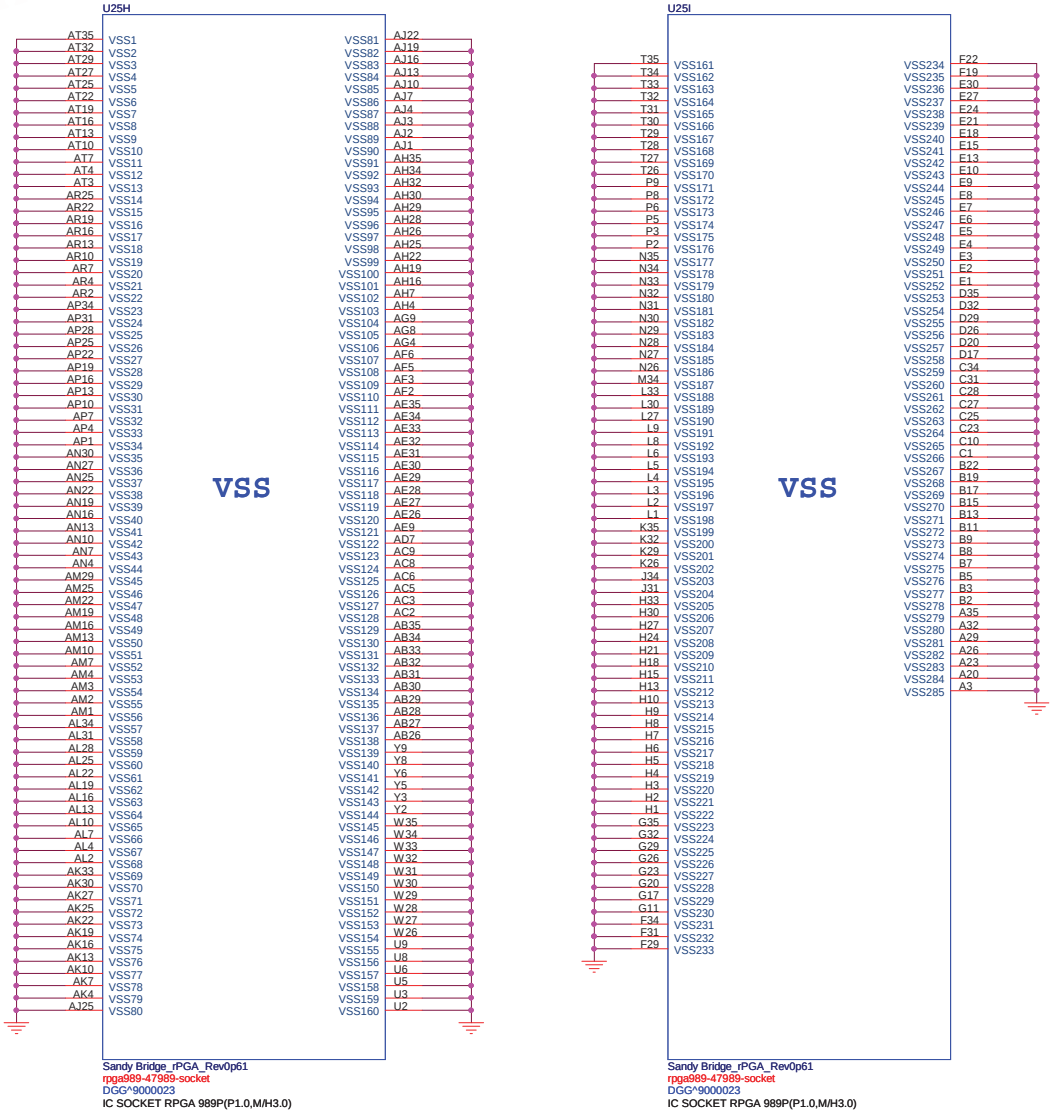
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

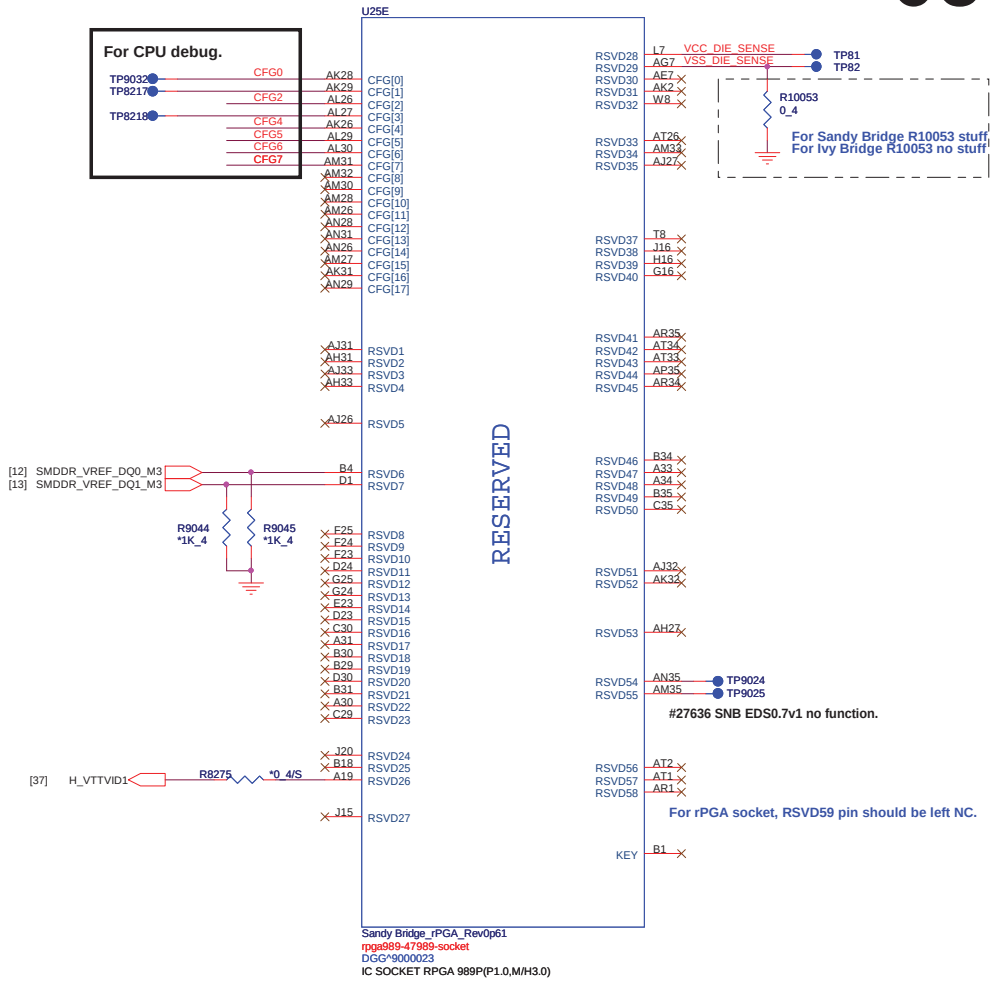
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	3A

Date: Wednesday, May 18, 2011 Sheet 4 of 47

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



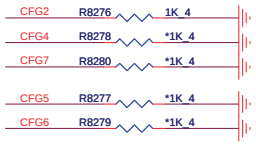
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



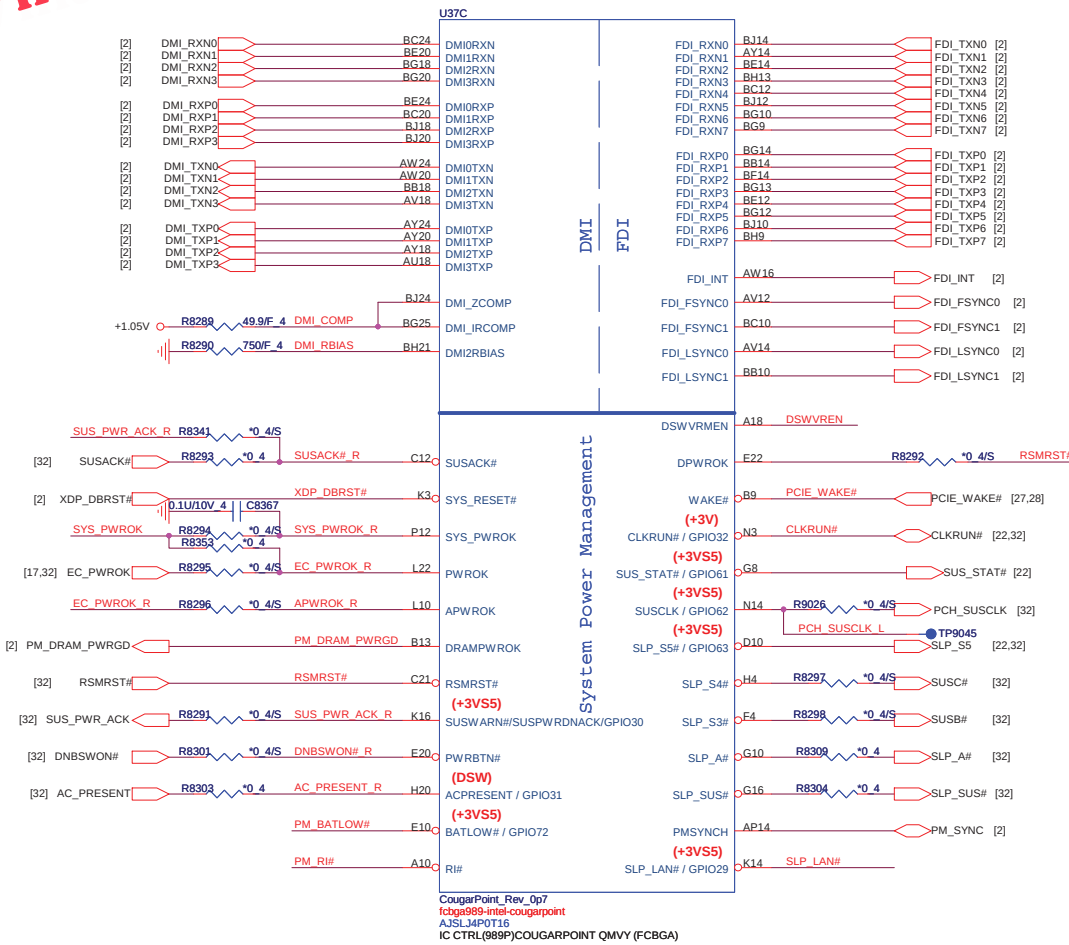
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	3A

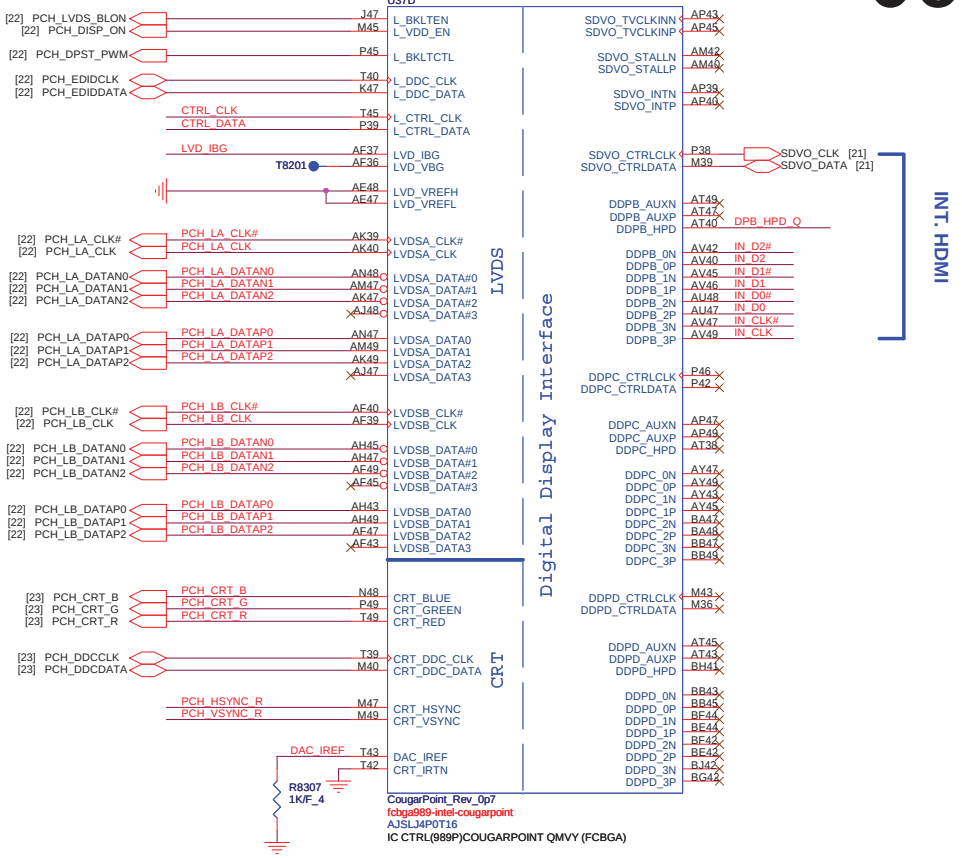
Date: Thursday, May 19, 2011 | Sheet 5 of 47

Cougar Point (DMI,FDI,PM)



CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

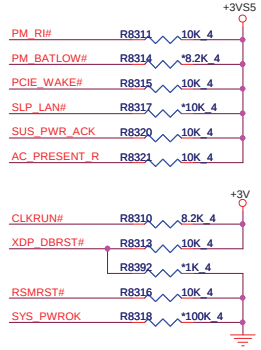
Cougar Point (LVDS,DDI)



CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

[7,10,17,21,22,23,25,29,30,31,41] +5V
[2,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[2,7,8,9,10,27,29,32,34,37,38,41,43] +3VS5
[7,22,31,32,33,34] +3VPCU
[7,10,32] +3V_RTC
[2,4,7,8,10,28,32,37,38,39] +1.05V

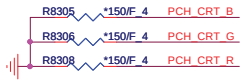
PCH Pull-high/low(CLG)



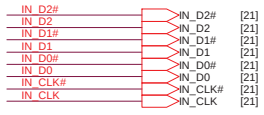
INT LVDS & CRT disable (DIS only remove)

PD Res place close to PCH

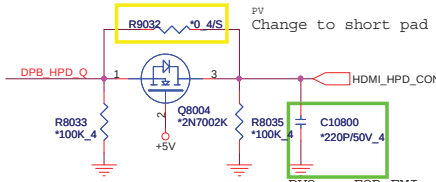
PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



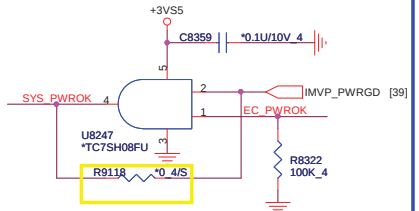
INT HDMI disable (DIS only remove)



INT HDMI Detect Function



System PWR_OK(CLG)



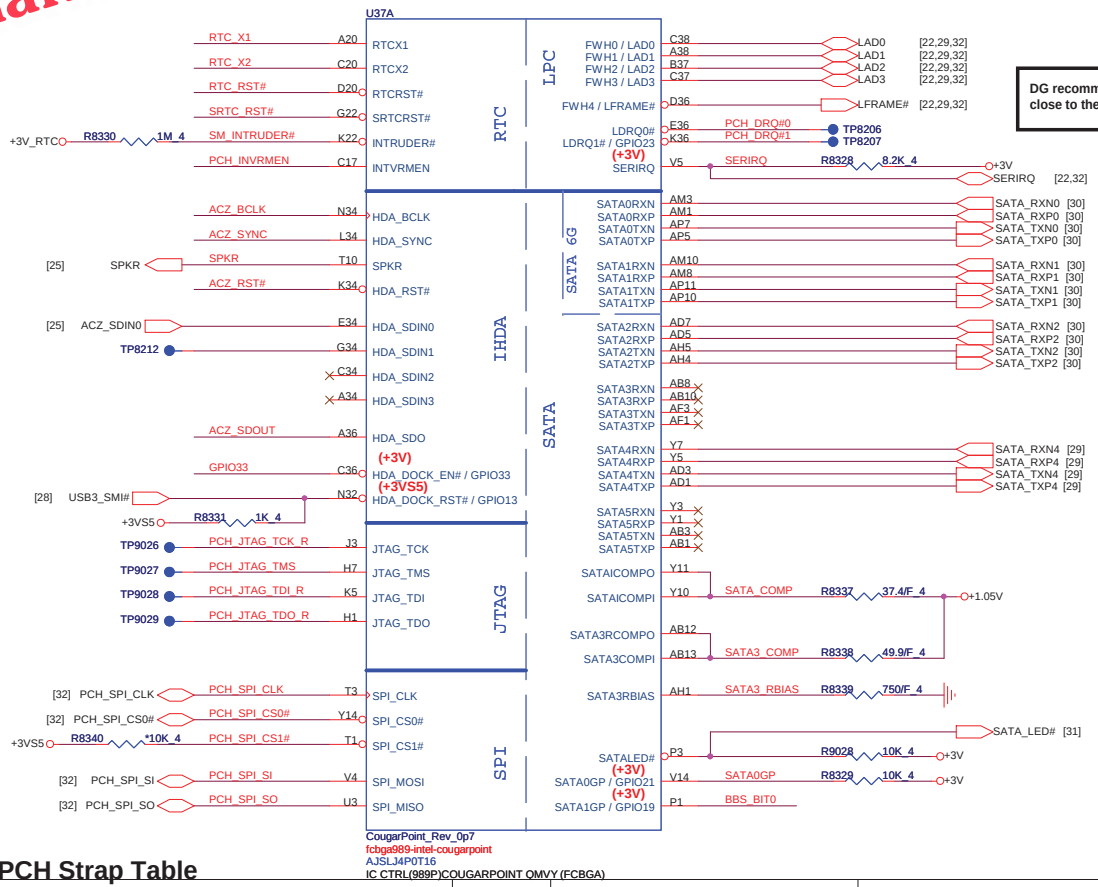
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	3A
Date: Wednesday, May 18, 2011	Sheet 6 of 47	

Cougar Point (HDA,JTAG,SATA)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

HDD0 (SATA3 6.0Gb/s)

2nd HDD0 (SATA3 6.0Gb/s)

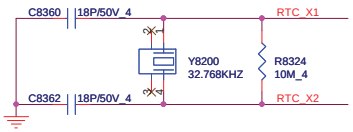
ODD

MINISATA (SATA1 1.5Gb/s)

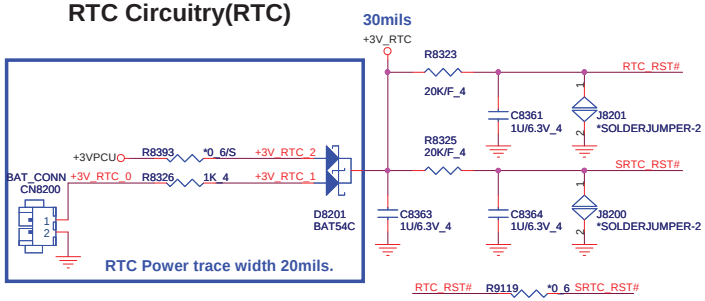
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8349 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R8350 *1K_4 R9139 10K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R8355 *1K_4 ACZ_SDOUT [32]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → SPI GNT1# 1, GNT0# 0 → LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R8358 *1K_4 BBS_BIT0 R8357 *1K_4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K_4 R8361 1K_4 NV_CLE [8] H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R9146 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[32] ACZ_SDOUT ACZ_SDOUT R8362 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R8365 *1K_4 ICC_EN# [9]
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R8366 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R8398 1K_4 +3V

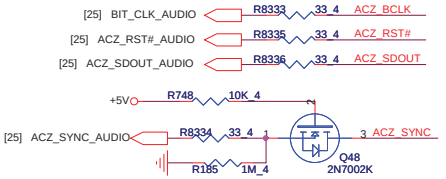
RTC Clock 32.768KHz



RTC Circuitry(RTC)



HDA Bus(CLG)



[10] +V3.3A_1.5A_HDA_IO
[6,10,17,21,22,23,25,29,30,31,41] +5V
[2,6,8,9,10,27,29,32,34,37,38,41,43] +3VS5
[22,31,32,33,34] +3VPCU
[2,6,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

[6,10,32] +3V_RTC
[4,10,38] +1.8V
[2,4,6,8,10,28,32,37,38,39] +1.05V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	3A

Date: Thursday, May 19, 2011 Sheet 7 of 47

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

SMBus/Pull-up(CLG)

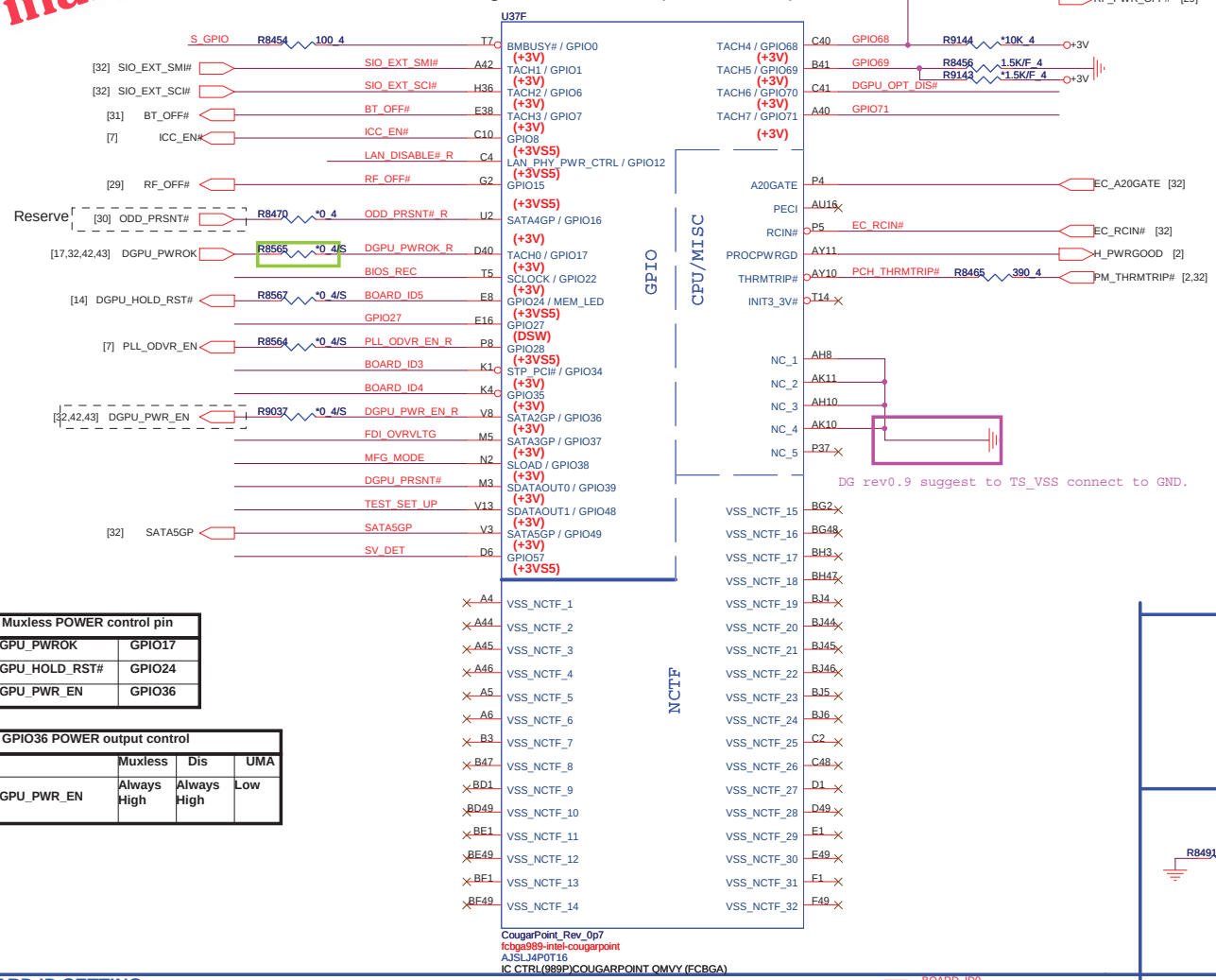
CLK_REQ/Strap Pin(CLG)

PLTRST#(CLG)

SMBus/Pull-up(CLG)

PCIE Clock

Cougar Point (GPIO,VSS_NCTF,RSVD)



Muxless POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

GPIO36 POWER output control			
	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

	Ra	Rb
UMA/Muxless	NC	Stuff
DIS	Stuff	NC

DGPU_OPT_DIS#:
High : Muxless.
Low: Discrete.

MFG-TEST

SGPIO

GPIO Pull-up/Pull-down(CLG)

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present

	DIS/Muxless	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID6	ID7	GPIO70	GPIO39
LG/CB	0=LG 1=CB								
15.6"/ 14"			ID2 14"=1 15"=0	ID3 17"=0 LG6=1					
17"			ID2 14"=0 15"=0	ID3 17"=1 LG6=1					
dobly					1=YES 0=NO				
DIS/Muxless								1= Muxless 0=DIS	
UMA/VGA									1= VGA 0=UMA

Add Board_ID6, Board_ID7 FOR CB Project

PROJECT	LG2/4 DIS
Quanta Computer Inc.	
Size: Custom	Document Number: PCH 4/6 (GPIO/MISC)
Rev: 3A	
Date: Wednesday, May 18, 2011	Sheet 9 of 47
NB5	

Cougar Point-M (POWER)

COUGAR POINT (POWER)

U37J

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA

U37G

VCC CORE
CRT
LVDS
HVCMOS
VCCIO
DMI
SPI
NAND / SPI
FDI

Near PCH

1.3 A (60mils)
2.925 A (140mils)
1.01A (60mils)
119mA (20mils)
119mA (15mils)
266mA (20mils)
3mA (10mils)
PCH_VCCDSW
+VCCPDSW
+VCCPDPLL_CPY
+VCCSUS1
+3V_SUS_CLKF33
+VCCAFDI_VRM
160mA (20mils)
+1.05V_VCCA_A_DPL
65mA (10mils)
+1.05V_VCCA_B_DPL
8mA (10mils)
+VCCDIFFCLK
+VCCDIFFCLKN
55mA (10mils)
+V1.05V_SSCVCC
95mA (10mils)
+VCCSST
+VTT_VCCPCPU
V_PROC_IO=1mA
(10mils)
+3V_RTC
VCCRTC<1mA
(10mils)
20mA (10mils)
+1.1V_VCC_DMI_CCI
L8012
10uH/100mA_8
+1.05V_VCCEPW
10mA (10mils)
+V3.3A_1.5A_HDA_IO
+1.05V_VCCUSBCORE
+3VCCPUSB
+3VCCAUBG
+VCCAUPLL
+5V_PCH_VCC5REFSUS
+VCCA_USBSUS
+3V_VCCPSUS
+5V_PCH_VCC5REF
+3V_VCCPCORE
+V1.05S_SATA3
+1.05V_VCCIO1
+VCCAFDI_VRM
+1.05V_PCH_VCC
+1.05V_PCH_VCCDPLL_EXP
+1.05V_VCCAPLL_EXP
+1.05V_VCCIO
+3V_VCC_EXP
+1.05V_VCCAPLL_FDI
+1.05V_VCCDPLL_FDI
+1.05V_VTT
+1.5V_CPU
+5V_PCH_VCC5REF
+5V_S5_PCH
+3VS5
+5VS5
+3V
+1.05V
+1.8V
+5V
PV
Change to short pad
VCC5REFSUS=1mA
V5REF= 1mA
(Mobile 1.5V)
DV2 add for +5V_S5 leakage issue
1mA (10mils)
60mA (10mils)
42mA (10mils)
190 mA (15mils)
20mA (10mils)
+VCCA_DAC_1_2
+VCCALVDS
+VCC_TX_LVDS
+3V_VCC_GIO
+VCCAFDI_VRM
+1.1V_VCC_DMI
+1.1V_VCC_DMI_CCI
+VCCP_NAND
+VCCME_SPI
Muxless : Ra
UMA : Ra
DIS : Rb
UMA & Muxless Only, If have power noise issue then stuff it.

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

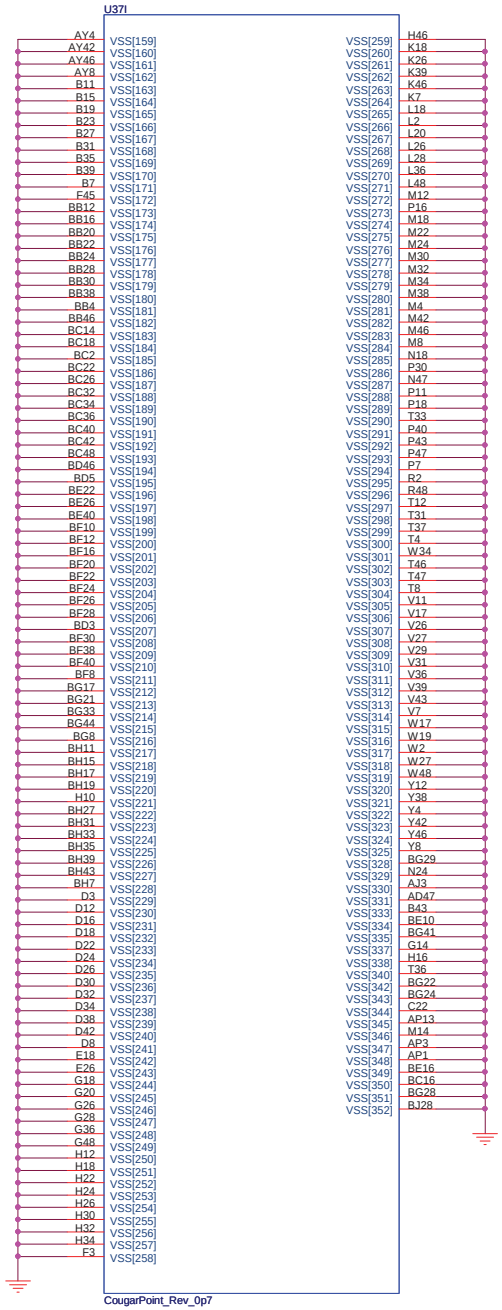
PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

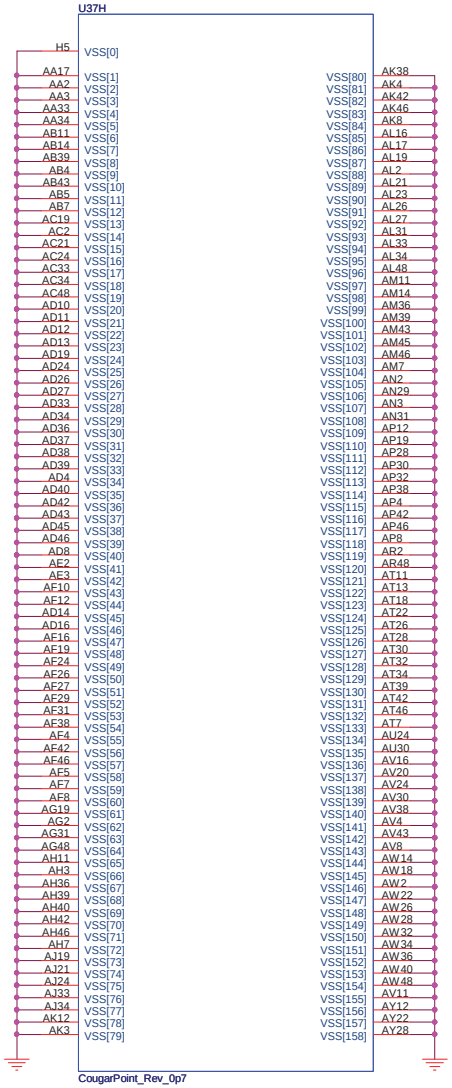
Size: Custom | Document Number: PCH 5/6 (POWER) | Rev: 3A

Date: Wednesday, May 18, 2011 | Sheet 10 of 47

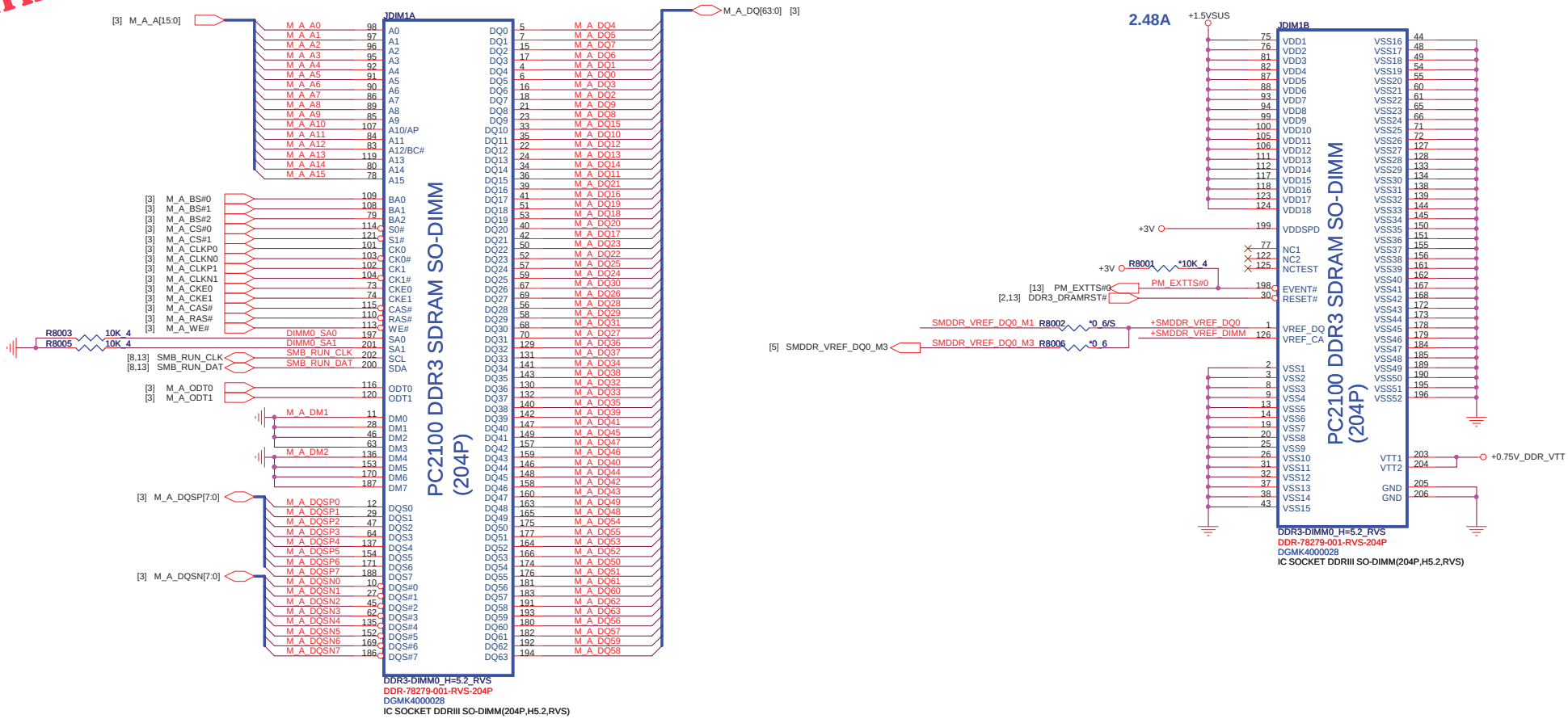
IBEX PEAK-M (GND)



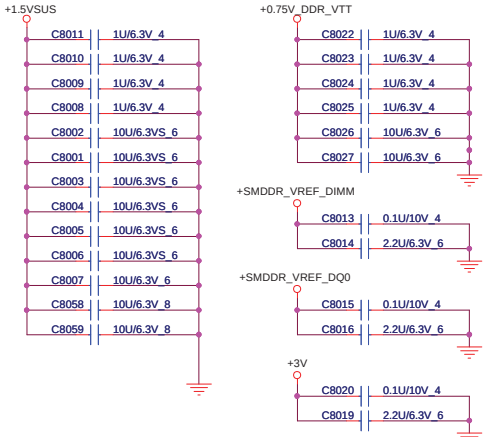
IBEX PEAK-M (GND)



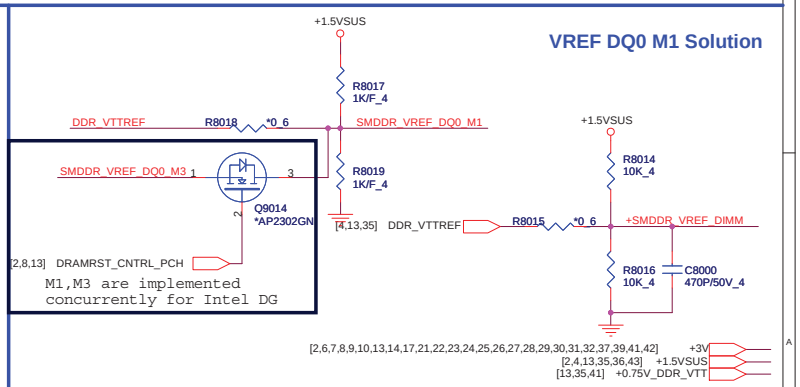
NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.	
Size: Custom	Document Number: PCH 6/6 (GND)	Rev: 3A
Date: Wednesday, May 18, 2011	Sheet 11 of 47	



Place these Caps near So-Dimm0.



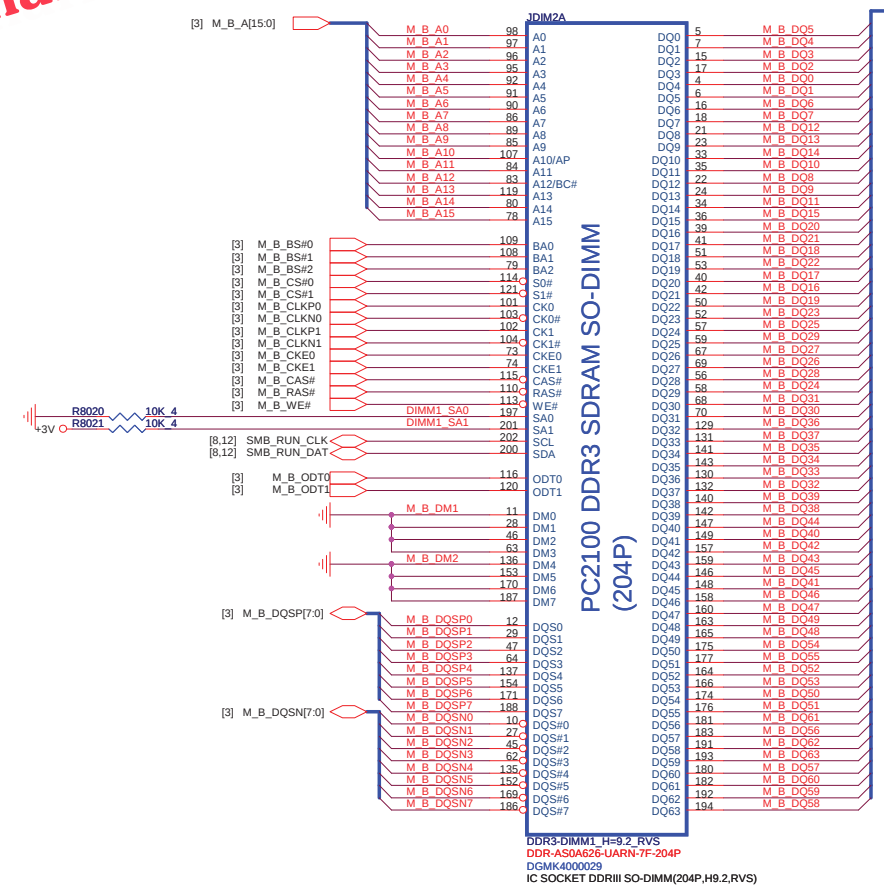
VREF DQ0 M1 Solution

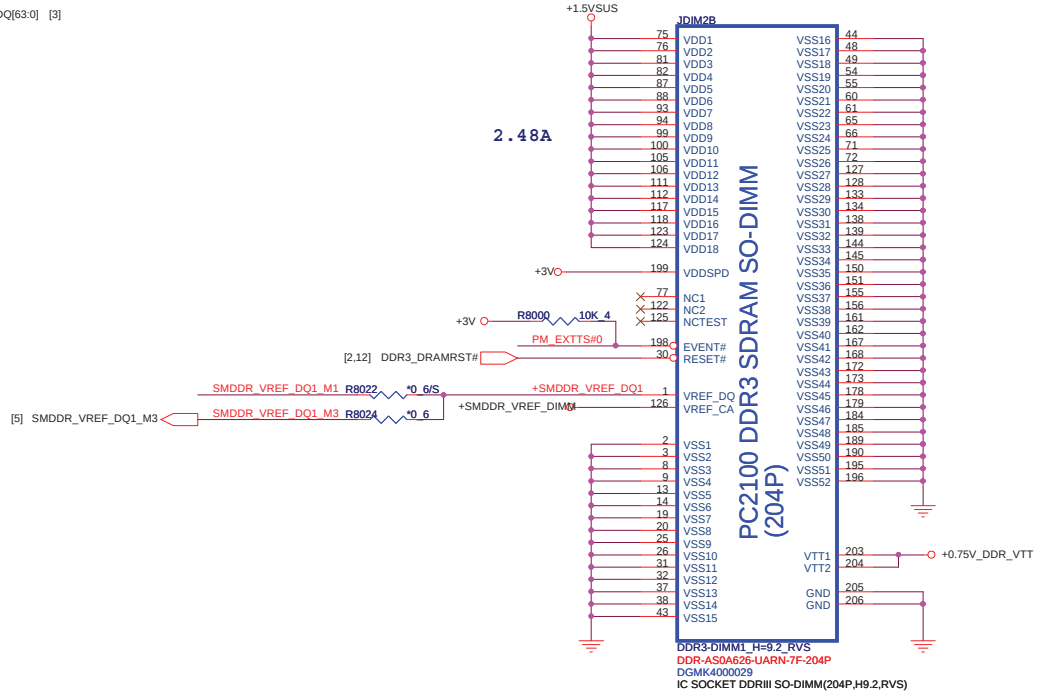


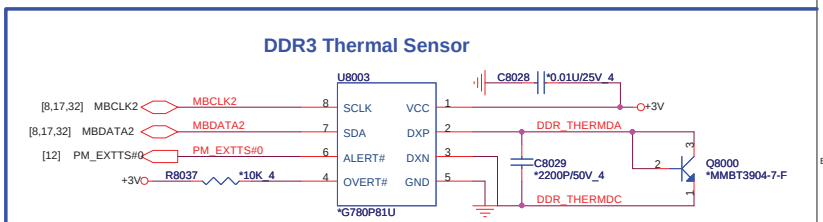
NB5

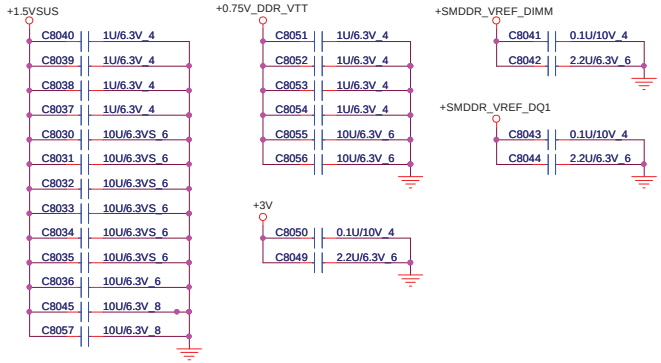
PROJECT : LG2/4 DIS
Quanta Computer Inc.

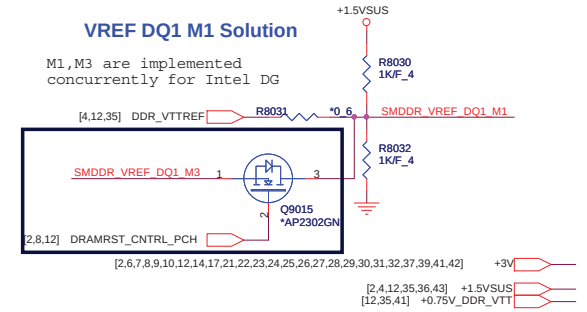
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	3A
Date: Wednesday, May 18, 2011	Sheet 12 of 47	









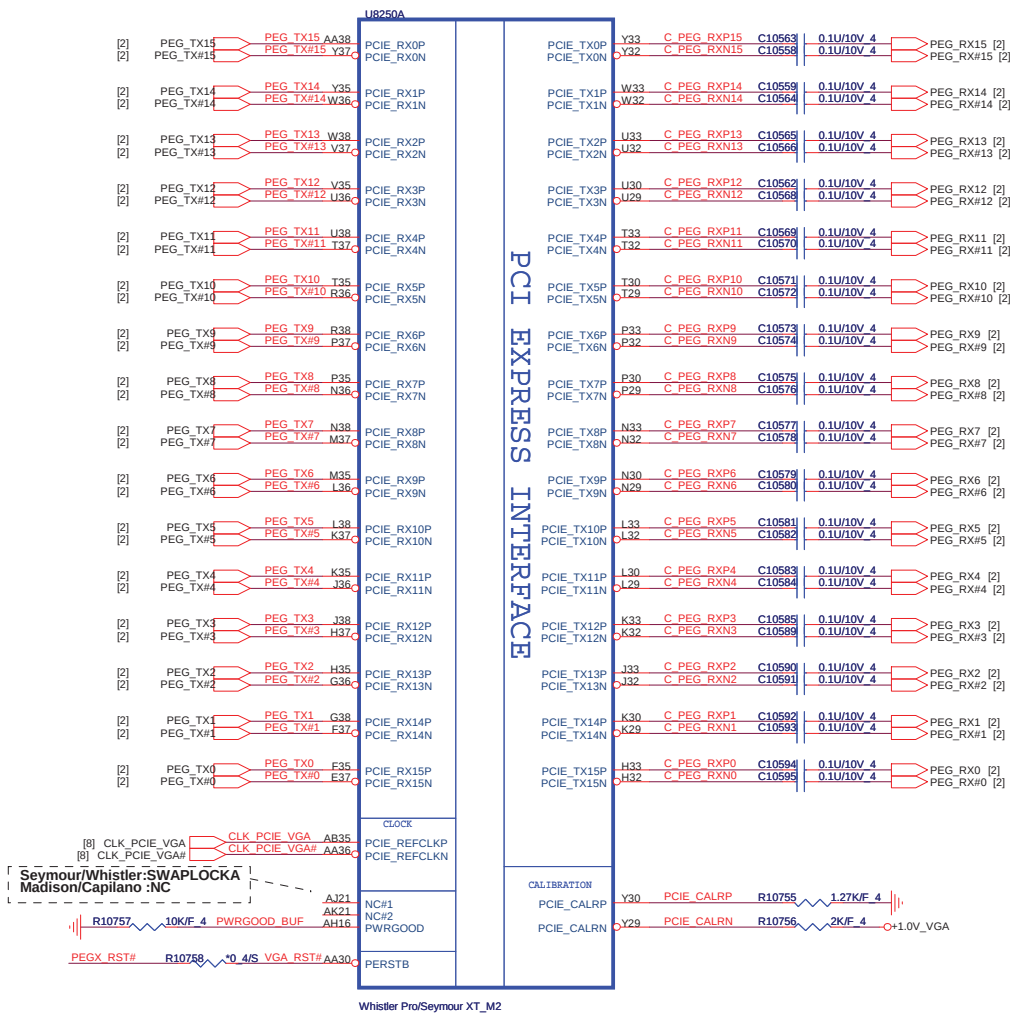


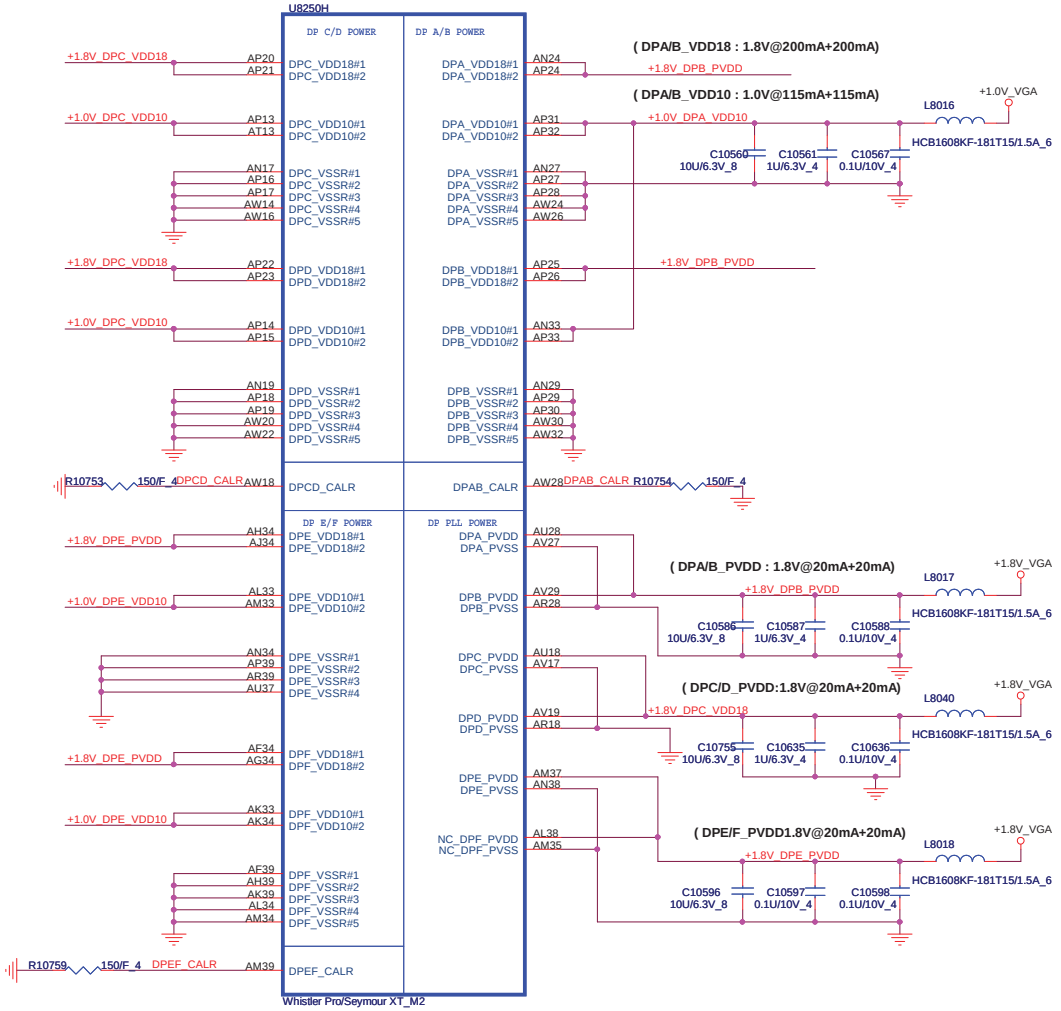
NB5

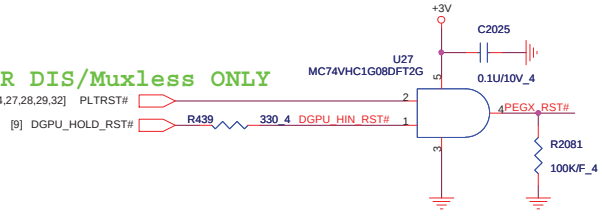
PROJECT : LG2/4 DIS
Quanta Computer Inc.

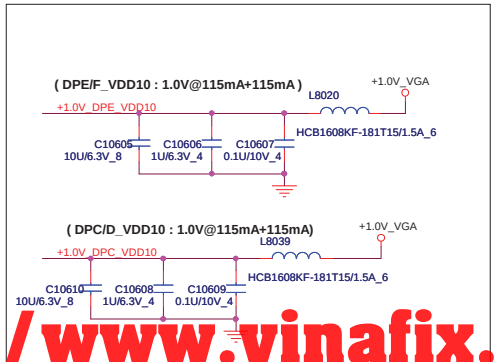
Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	3A

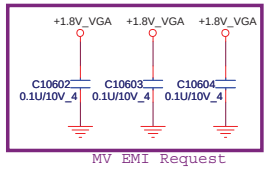
Date: Wednesday, May 18, 2011 Sheet 13 of 47











[2,6,7,8,9,10,12,13,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[16,18,43] +1.8V_VGA
[16,17,18,43] +1.0V_VGA

PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	AMD Whistler (MEM)1/5	3A

Date: Wednesday, May 18, 2011 Sheet 14 of 47

Seymour Use Channel B Memory Interface Only

[19] VMA_DQ[63..0] [19] VMA_DM[7..0] [19] VMA_WDQS[7..0] [19] VMA_RDQS[7..0]

[20] VMB_DQ[63..0] [20] VMB_DM[7..0] [20] VMB_WDQS[7..0] [20] VMB_RDQS[7..0]

U8250C — MEMORY INTERFACE A — Whistler Pro/Seymour XT_M2

U8250D — MEMORY INTERFACE B — Whistler Pro/Seymour XT_M2

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	For Whistler	For Seymour
MEM_CALRNP0	stuff	NC
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	NC
MVREFDA	stuff	NC
MVREFSA	stuff	NC

Designator	
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

5/6: change R68 from 10k to 5.11k for AMD
_MV del R567 add R68 in BOM

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

[18,19,20,43] +1.5V_VGA

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size: Custom | Document Number: AMD Whistler (MEM)2/5 | Rev: 3A

Date: Wednesday, May 18, 2011 | Sheet 15 of 47

U8250B

NC on Park/Robson/Seymour

SI Add for AMD request

NC on Park/Robson/Seymour

Access to SCL and SDA is mandatory on BACO designs for debug purposes

RA

RA for DIS only

GPIO0: option to control PSI in future products - not currently qualified

DP Channel D is NC on Park, Robson and Seymour

CAP EMI request

	Ra
DIS	Stuff
Muxless	NC

DV2 Clock REQ FOR Muxless

Seymour/Whistler: Stereo sync output

GenericF/G is NC on PARK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

GND Option If XO_IN/XO_IN2 not used
For M97, XO_IN and XO_IN2 should be grounded

Seymour/Whistler: DAC2 is NC
Madison/Capilano:DAC2 Output-C
Madison/Capilano:DAC2 Output-Y

For FL/GL support on Seymour/Whistler only
Seymour/Whistler: GENCLK_CLK
Seymour/Whistler: GENCLK_VSYNC

Seymour/Whistler:TSVSSQ Temperature sensor quiet ground. Madison/Capilano: A2VSSQ.

DDCxx_AUX4x is NC on M92M2 and Park/Robson/Seymour

DDCxx_AUX7x is NC on M9x and Park/Robson/Seymour

Whistler Pro/Seymour XT_M2

U8250G

Whistler Pro/Seymour XT_M2

(1.8V@150mA DPLL_PVDD)

(1.0V@300mA DPLL_VDDC)

(1.8V@20mA TSVDD)

(DAC1_AVDD: 1.8V@70mA+42mA)

(A2VDDQ: 1.8V@1mA)

(DAC1_VDD1DI:1.8V@100mA)

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	Ra --> 15K-ohm
1.0V	0	1	Rb --> 10K-ohm
			default 1.15V

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
1.1V	1	0	
1.15V	1	1	default

MEM_ID	3	2	1	0	DDR3 Type	Configuration	Size
MEM_ID0	0	0	0	1	Samsung K4W2G1646C-HC11 (2G bits)	128 * 16 x 8 pcs	2G
Pull High					Quanta P/N: AKD5MGWT500	128 * 16 x 4 pcs	1G
MEM_ID1	0	0	1	0	Hynix H5TQ2G63BFR-11C (2G bits)	128 * 16 x 8 pcs	2G
Pull High					Quanta P/N: AKD5MGWTW00	128 * 16 x 4 pcs	1G
MEM_ID2	0	1	0	0	Sansung K4W1G1646G-BC11 (1G bits)	64 * 16 x 8 pcs	1G
Pull High					Quanta P/N: AKD5EGGT500	64 * 16 x 4pcs	512M
MEM_ID3	1	0	0	0	Hynix H5TQ1G63DFR-11C (1G bits)	64 * 16 x 8 pcs	1G
Pull High					Quanta P/N: AKD5LZWTW02	64 * 16 x 4pcs	512M

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size: Custom | Document Number: AMD Whistler DISPLAY3/5 | Rev: 3A

Date: Thursday, May 19, 2011 | Sheet 16 of 47

U8250F

PCIE_VSS#1 AB39
PCIE_VSS#2 E39
PCIE_VSS#3 F34
PCIE_VSS#4 F39
PCIE_VSS#5 G33
PCIE_VSS#6 G34
PCIE_VSS#7 H31
PCIE_VSS#8 H34
PCIE_VSS#9 H39
PCIE_VSS#10 J31
PCIE_VSS#11 J34
PCIE_VSS#12 K31
PCIE_VSS#13 K34
PCIE_VSS#14 K39
PCIE_VSS#15 L31
PCIE_VSS#16 L34
PCIE_VSS#17 M34
PCIE_VSS#18 M39
PCIE_VSS#19 N31
PCIE_VSS#20 N34
PCIE_VSS#21 P31
PCIE_VSS#22 P34
PCIE_VSS#23 P39
PCIE_VSS#24 R34
PCIE_VSS#25 T31
PCIE_VSS#26 T34
PCIE_VSS#27 T39
PCIE_VSS#28 U31
PCIE_VSS#29 U34
PCIE_VSS#30 V34
PCIE_VSS#31 V39
PCIE_VSS#32 W31
PCIE_VSS#33 W34
PCIE_VSS#34 Y34
PCIE_VSS#35 Y39

GND

GND#100 F15
GND#101 F17
GND#102 F19
GND#103 F21
GND#104 F23
GND#105 F25
GND#106 F27
GND#107 F29
GND#108 F31
GND#109 F33
GND#110 F7
GND#111 F9
GND#112 G2
GND#113 G6
GND#114 H9
GND#115 J2
GND#116 J27
GND#117 J6
GND#118 J8
GND#119 K14
GND#120 K7
GND#121 L11
GND#122 L17
GND#123 L2
GND#124 L22
GND#125 L24
GND#126 L6
GND#127 M17
GND#128 M22
GND#129 M24
GND#130 N16
GND#131 N18
GND#132 N2
GND#133 N21
GND#134 N23
GND#135 N26
GND#136 N6
GND#137 R15
GND#138 R17
GND#139 R2
GND#140 R20
GND#141 R22
GND#142 R24
GND#143 R27
GND#144 R6
GND#145 T11
GND#146 T13
GND#147 T16
GND#148 T18
GND#149 T21
GND#150 T23
GND#151 T26
GND#153 U15
GND#154 U17
GND#155 U2
GND#156 U20
GND#157 U22
GND#158 U24
GND#159 U27
GND#160 U6
GND#161 V11
GND#163 V16
GND#164 V18
GND#165 V21
GND#166 V23
GND#167 V26
GND#168 W2
GND#169 W6
GND#170 Y15
GND#171 Y17
GND#172 Y20
GND#173 Y22
GND#174 Y24
GND#175 Y27
GND#152 U13
GND#162 V13

GND#1 A3
GND#2 A37
GND#3 AA16
GND#4 AA18
GND#5 AA2
GND#6 AA21
GND#7 AA23
GND#8 AA26
GND#9 AA28
GND#10 AA6
GND#11 AB12
GND#12 AB15
GND#13 AB17
GND#14 AB20
GND#15 AB22
GND#16 AB24
GND#17 AB27
GND#18 AC11
GND#19 AC13
GND#20 AC16
GND#21 AC18
GND#22 AC2
GND#23 AC21
GND#24 AC23
GND#25 AC26
GND#26 AC28
GND#27 AC6
GND#28 AD15
GND#29 AD17
GND#30 AD20
GND#31 AD22
GND#32 AD24
GND#33 AD27
GND#34 AD9
GND#35 AE2
GND#36 AE6
GND#37 AE10
GND#38 AE16
GND#39 AF18
GND#40 AF21
GND#41 AG17
GND#42 AG2
GND#43 AG20
GND#44 AG22
GND#45 AG6
GND#46 AG9
GND#47 AH21
GND#48 AJ10
GND#49 AJ11
GND#50 AJ2
GND#51 AJ28
GND#52 AJ6
GND#53 AK11
GND#54 AK31
GND#55 AK7
GND#56 AL11
GND#57 AL14
GND#58 AL17
GND#59 AL2
GND#60 AL20
GND/PX_EN#61 AL21 PX_EN_1
GND#62 AL23
GND#63 AL26
GND#64 AL32
GND#65 AL6
GND#66 AL8
GND#67 AM11
GND#68 AM31
GND#69 AM9
GND#70 AN11
GND#71 AN2
GND#72 AN30
GND#73 AN6
GND#74 AN8
GND#75 AP11
GND#76 AP7
GND#77 AP9
GND#78 AR5

GND#80 B11
GND#81 B13
GND#82 B15
GND#83 B17
GND#84 B19
GND#85 B21
GND#86 B23
GND#87 B25
GND#88 B27
GND#89 B29
GND#90 B31
GND#91 B33
GND#92 B7
GND#93 B9
GND#94 C1
GND#95 C39
GND#96 E35
GND#97 E5
GND#98 F11
GND#99 F13

VSS_MECH#1 A39
VSS_MECH#2 AW1
VSS_MECH#3 AW39

Whistler Pro/Seymour XT_M2

STRAPS

DV2 Change R10806 non stuff

+3V_VGA

[16] VGA_GPIO0 R10806 *10K/F_4
[16] VGA_GPIO1 R10807 *10K/F_4
[16] VGA_GPIO2 R10808 *10K/F_4
[16] VGA_GPIO8 R10809 *10K/F_4
[16] VGA_GPIO9 R10810 *10K/F_4
[16] VGA_GPIO13 R10811 10K/F_4, R10812 *10K/F_4
[16] VGA_GPIO12 R10813 10K/F_4, R10814 *10K/F_4
[16] VGA_GPIO11 R10815 *10K/F_4, R10816 10K/F_4
[16] VGA_GPIO10 R10817 *10K/F_4 — GPIO10 for EEPROM.
[16] GENERICC R10818 *10K/F_4 — GPIO22 for Enable EEPROM
[16] VGA_GPIO22 R10819 *10K/F_4

Re
[16,23] GPU_VSYNC R10827 *10K/F_4, R10820 10K/F_4
Rf
Rg
[16,23] GPU_HSYNC R10828 *10K/F_4, R10821 10K/F_4
Rh
[16] VSYNC_DAC2 R10822 *10K/F_4
[16] HSYNC_DAC2 R10823 *10K/F_4

[16,22] GPU_LVDS_BLON R10824 10K/F_4
[16,42] GFX_CORE_CNTRL0 R10825 *3K/F_4
[16,42] GFX_CORE_CNTRL1 R10826 *3K/F_4

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

	Re	Rf	Rg	Rh
PX4.0	Stuff	NC	Stuff	NC
Discrete	NC	Stuff	NC	Stuff

Reserve for support BACO mode

Rb
PX_EN_1 R10829 0_4 PX_EN

	Ra	Rb
BACO Functions	Stuff	Stuff 5.1k
NO BACO Functions	NC	Stuff 0 ohm

Ra

Support BACO Mode : Stuff All Location
NO Support BACO Mode : No Stuff All Location

PX_MODE=1, for Normal Operation (Default)
PX_MODE=0, for BACO MODE

PX_EN=1, for BACO MODE
PX_EN=0, for Normal Operation (Default)

C889 *0.1U/10V_4
[9,32,42,43] DGPU_PWROK
PX_MODE
U40 *TC7SH08FU
BACO_EN
R10865 *100K/F_4
PX_EN#
Q9016 *2N7002
Q9017 *2N7002
[6,32] EC_PWROK
[42] PX_MODE
Q9009 *2N7002
PX_EN
R10838 *1K_4
R10839 *1K_4
PX_EN##
PX_EN#2
Q9008 *2N7002
Q9007 *2N7002
[43] PX_MODE1
Q9018 *2N7002
+1.0V_VGA
+VGACORE
Q9010 *AO3404
Q9012 *AO3404
Q9011 *AO3404
Q9013 *AO3404
BIF_VDDC
C10729 *22U/6.3VS_8

GFx SMBus Isolation

[16] G_SMBCLK
R481 4.7K_4
Q55 2N7002
MBCLK2 [8,13,32]
+3V_VGA
DV2 Change to +3V_VGA
R485 4.7K_4
Q43 2N7002
[16] G_SMBDAT
MBDATA2 [8,13,32]

[15,16] +3V_VGA

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Whistler (GD&Str)4/5	3A
Date: Wednesday, May 18, 2011	Sheet 17 of 47	

U8250E

(VDDR1: 1.5V@9.1A)

(1.8V@500mA PCIE_VDDR)

(1.0V@2000mA PCIE_VDDC)

(1.8V@136mA VDD_CT)

(3.3V@60mA VDDR3)

VDDR4 for DVPDATA[12..23]

(VDDR4_5 : 1.8V@20/170mA)

VDDR5 for DVPDATA[0..11]

(1.8V@40mA PCIE_PVDD)

(SPV10 :1.0V@120mA)

(For MP7, 1.12V@4A VDDCI).

POWER

Whistler Pro/Seymour XT_M2

	Rc	Rd
BACO Functions	NC	Stuff
NO BACO Functions	Stuff	NC

Rc

For non-BACO designs, connect BIF_VDDC to VDDC.
For BACO designs - see BACO reference schematics (ref138)

VGA Chip Pin N27,T27 don't use short pad ,use 0 ohm

Rd

BACO Functions Stuff

[42] VGACORESENSE

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[6,7,10,17,21,22,23,25,29,30,31,41] +5V
[14,16,17,43] +1.0V_VGA
[17,42] +VGACORE
[15,19,20,43] +1.5V_VGA
[14,16,43] +1.8V_VGA
[15,16] +3V_VGA

PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size: Custom | Document Number: AMD Whistler (POWER) 5/5 | Rev: 3A

Date: Wednesday, May 18, 2011 | Sheet 18 of 47

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

VRAM1 / VRAM2 / VRAM3 / VRAM4

*K4W1G1646E-HC12

100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

+1.5V_VGA

R10705 *243/F_4
R10706 *243/F_4
R10707 *243/F_4
R10708 *243/F_4

R10709 *4.99K/F_4
R10710 *4.99K/F_4
R10711 *4.99K/F_4
R10712 *4.99K/F_4
R10713 *4.99K/F_4
R10714 *4.99K/F_4
R10715 *4.99K/F_4
R10716 *4.99K/F_4

VREFC_VMA1 / VREFD_VMA1 / VREFC_VMA2 / VREFD_VMA2 / VREFC_VMA3 / VREFD_VMA3 / VREFC_VMA4 / VREFD_VMA4

R10717 *4.99K/F_4 C10454 *.1U/10V_4
R10718 *4.99K/F_4 C10455 *.1U/10V_4
R10719 *4.99K/F_4 C10456 *.1U/10V_4
R10720 *4.99K/F_4 C10457 *.1U/10V_4
R10721 *4.99K/F_4 C10458 *.1U/10V_4
R10722 *4.99K/F_4 C10459 *.1U/10V_4
R10723 *4.99K/F_4 C10460 *.1U/10V_4
R10724 *4.99K/F_4 C10461 *.1U/10V_4

VMA_CLK0 / VMA_CLK0_COMM
R10725 *56.2/F_4
C10478 *.01U/16V_4
R10726 *56.2/F_4
VMA_CLK0# / VMA_CLK1
R10727 *56.2/F_4
VMA_CLK1_COMM
C10495 *.01U/16V_4
R10728 *56.2/F_4
VMA_CLK1#

C10462 C10463 C10464 C10465 C10466 C10467 C10468 C10469 *1U/6.3V_4
C10470 C10471 C10472 C10473 C10474 C10475 C10476 C10477 *1U/6.3V_4
C10479 C10480 C10481 C10482 C10483 C10484 C10485 C10486 *1U/6.3V_4
C10487 C10488 C10489 C10490 C10491 C10492 C10493 C10494 *1U/6.3V_4
C10496 C10497 C10498 C10499 C10500 C10501 C10502 C10503 C10504 C10505 10U/6.3V_6S

[15,18,20,43] +1.5V_VGA

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

Date: Wednesday, May 18, 2011 Sheet 19 of 47

CHANNEL B: 256MB/512MB DDR3

[15] VMB_DQ[63..0]
[15] VMB_DM[7..0]
[15] VMB_WDQS[7..0]
[15] VMB_RDQS[7..0]

VRAM5 / VRAM6 / VRAM7 / VRAM8

100-BALL SDRAM DDR3
K4W1G1646E-HC12

Should be 240 Ohms +-1%

R10729 243/F_4
R10730 243/F_4
R10731 243/F_4
R10732 243/F_4

+1.5V_VGA

R10733 4.99K/F_4
R10734 4.99K/F_4
R10735 4.99K/F_4
R10736 4.99K/F_4
R10737 4.99K/F_4
R10738 4.99K/F_4
R10739 4.99K/F_4
R10740 4.99K/F_4

VREFC_VMB1 / VREFD_VMB1
VREFC_VMB2 / VREFD_VMB2
VREFC_VMB3 / VREFD_VMB3
VREFC_VMB4 / VREFD_VMB4

R10741 4.99K/F_4 C10506 .1U/10V_4
R10742 4.99K/F_4 C10507 .1U/10V_4
R10743 4.99K/F_4 C10508 .1U/10V_4
R10744 4.99K/F_4 C10509 .1U/10V_4
R10745 4.99K/F_4 C10510 .1U/10V_4
R10746 4.99K/F_4 C10511 .1U/10V_4
R10747 4.99K/F_4 C10512 .1U/10V_4
R10748 4.99K/F_4 C10513 .1U/10V_4

VMB_CLK0
VMB_CLK0_COMM
R10749 56.2/F_4
C10530 .01U/16V_4
R10750 56.2/F_4
VMB_CLK0#
VMB_CLK1
R10751 56.2/F_4
VMB_CLK1_COMM
C10547 .01U/16V_4
R10752 56.2/F_4

C10520 C10521 C10522 C10523 C10524 C10525 C10527 C10528 1U/6.3V_4
C10531 C10532 C10533 C10534 C10535 C10536 C10537 C10538 1U/6.3V_4
C10514 C10515 C10516 C10517 C10518 C10519 C10526 C10529 1U/6.3V_4
C10539 C10540 C10541 C10542 C10543 C10544 C10545 C10546 1U/6.3V_4
C10548 C10549 C10550 C10551 C10552 C10553 C10554 C10555 C10556 C10557 10U/6.3V_6S

[15,18,19,43] +1.5V_VGA

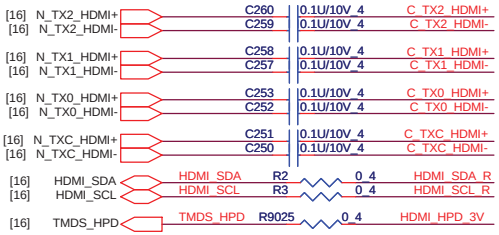
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	3A

Date: Thursday, May 19, 2011 Sheet 20 of 47

For DIS HDMI Only



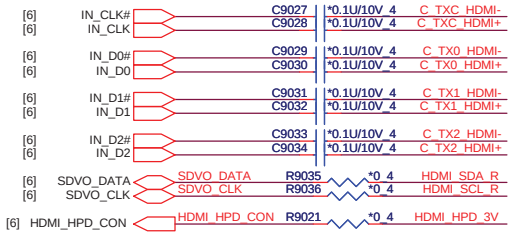
	Select
Dis	Ra
muxless	Rb

Ra

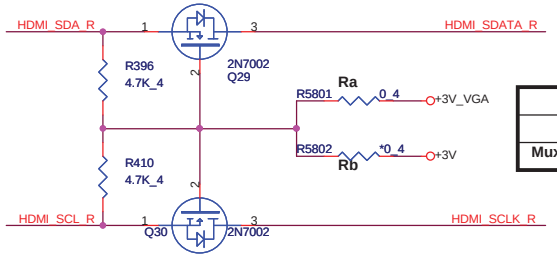
	Select
Dis	Ra
Muxless	Rb

Rb

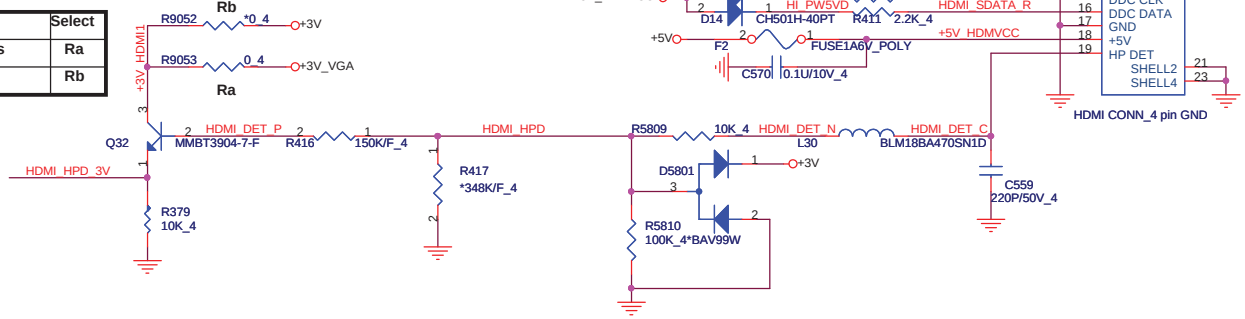
For Muxless/UMA HDMI function



DIS: 4.7K
UMA/Muxless: 2.2K

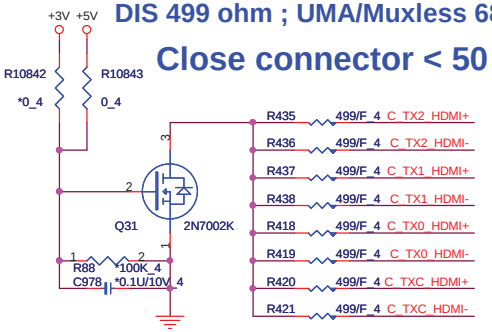


	Select
Dis	Ra
Muxless	Rb



DIS 499 ohm ; UMA/Muxless 680 ohm

Close connector < 50 mil



Close connector < 50 mil

EMI

DV2 Change to 150 ohm

+5VCRT

[6,7,10,17,22,23,25,29,30,31,41] +5V

[2,6,7,8,9,10,13,14,17,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI and connector	3A

Date: Friday, May 20, 2011 Sheet 21 of 47

	Select
Dis	Ra
muxless	Rb

Rb MUXLESS

[6] PCH_LA_CLK	PCH_LA_CLK	R54	*0_4	TXLCLKOUT+	
[6] PCH_LA_CLK#	PCH_LA_CLK#	R55	*0_4	TXLCLKOUT-	
[6] PCH_LA_DATAP0	PCH_LA_DATAP0	R57	*0_4	TXLOUT0+	
[6] PCH_LA_DATAN0	PCH_LA_DATAN0	R56	*0_4	TXLOUT0-	
[6] PCH_LA_DATAP1	PCH_LA_DATAP1	R41	*0_4	TXLOUT1+	
[6] PCH_LA_DATAN1	PCH_LA_DATAN1	R40	*0_4	TXLOUT1-	
[6] PCH_LA_DATAP2	PCH_LA_DATAP2	R38	*0_4	TXLOUT2+	
[6] PCH_LA_DATAN2	PCH_LA_DATAN2	R39	*0_4	TXLOUT2-	
[6] PCH_LB_CLK	PCH_LB_CLK	R50	*0_4	TXUCLKOUT+	
[6] PCH_LB_CLK#	PCH_LB_CLK#	R51	*0_4	TXUCLKOUT-	
[6] PCH_LB_DATAP0	PCH_LB_DATAP0	R36	*0_4	TXUOUT0+	
[6] PCH_LB_DATAN0	PCH_LB_DATAN0	R37	*0_4	TXUOUT0-	
[6] PCH_LB_DATAP1	PCH_LB_DATAP1	R52	*0_4	TXUOUT1+	
[6] PCH_LB_DATAN1	PCH_LB_DATAN1	R53	*0_4	TXUOUT1-	
[6] PCH_LB_DATAP2	PCH_LB_DATAP2	R34	*0_4	TXUOUT2+	
[6] PCH_LB_DATAN2	PCH_LB_DATAN2	R35	*0_4	TXUOUT2-	

Ra DIS

[16] GPU_TXLCLKOUT+	GPU_TXLCLKOUT+	R46	0_4	TXLCLKOUT+
[16] GPU_TXLCLKOUT-	GPU_TXLCLKOUT-	R47	0_4	TXLCLKOUT-
[16] GPU_TXLOUT0+	GPU_TXLOUT0+	R49	0_4	TXLOUT0+
[16] GPU_TXLOUT0-	GPU_TXLOUT0-	R48	0_4	TXLOUT0-
[16] GPU_TXLOUT1+	GPU_TXLOUT1+	R32	0_4	TXLOUT1+
[16] GPU_TXLOUT1-	GPU_TXLOUT1-	R31	0_4	TXLOUT1-
[16] GPU_TXLOUT2+	GPU_TXLOUT2+	R29	0_4	TXLOUT2+
[16] GPU_TXLOUT2-	GPU_TXLOUT2-	R30	0_4	TXLOUT2-
[16] GPU_TXUCLKOUT+	GPU_TXUCLKOUT+	R42	0_4	TXUCLKOUT+
[16] GPU_TXUCLKOUT-	GPU_TXUCLKOUT-	R43	0_4	TXUCLKOUT-
[16] GPU_TXUOUT0+	GPU_TXUOUT0+	R27	0_4	TXUOUT0+
[16] GPU_TXUOUT0-	GPU_TXUOUT0-	R28	0_4	TXUOUT0-
[16] GPU_TXUOUT1+	GPU_TXUOUT1+	R44	0_4	TXUOUT1+
[16] GPU_TXUOUT1-	GPU_TXUOUT1-	R45	0_4	TXUOUT1-
[16] GPU_TXUOUT2+	GPU_TXUOUT2+	R25	0_4	TXUOUT2+
[16] GPU_TXUOUT2-	GPU_TXUOUT2-	R26	0_4	TXUOUT2-

Rb MUXLESS

[6] PCH_LVDS_BLON	R298	*0_4	LVDS_BLON
[6] PCH_DISP_ON	R323	*0_4	DISP_ON
[6] PCH_DPST_PWM	R305	*0_4	DPST_PWM

Ra DIS

[16,17] GPU_LVDS_BLON	R297	0_4	LVDS_BLON
[16] GPU_DISP_ON	R324	0_4	DISP_ON
[16] GPU_DPST_PWM	R303	0_4	DPST_PWM

Rb MUXLESS

+3V

	R13	*2.2K_4	PCH_EDIDCLK	
	R14	*2.2K_4	PCH_EDIDDATA	
[6] PCH_EDIDCLK	PCH_EDIDCLK	R11	*0_4	EDIDCLK
[6] PCH_EDIDDATA	PCH_EDIDDATA	R12	*0_4	EDIDDATA

Ra DIS

[16] GPU_EDIDCLK	GPU_EDIDCLK	R8	0_4	EDIDCLK
[16] GPU_EDIDDATA	GPU_EDIDDATA	R9	0_4	EDIDDATA

+VIN_BLIGHT

+VIN — L1 UPB201209T-330Y-N — +VIN_BLIGHT

C2 *.1U/50V_6 | C441 .1U/50V_6 | C6 .01U/25V_4 | C4 .1U/50V_6

EDIDCLK C13 *10P/50V_4
EDIDDATA C14 *10P/50V_4

DIGITAL_D1 C11 10P/50V_4
DIGITAL_CLK_L C8 10P/50V_4
for EMI issue

R300 100K/F_4
C444 22P/50V_4

[32] LID_CONTROL — R9079 *0_4/S_PN_BLON — D8 RB501V-40 — BLON_CON

LVDS_BLON R294 1K/F_4 — D7 *RB501V-40 — LID_EC# [31,32]
R295 100K/F_4 — R299 47K_4 — +3VPCU

[8] LCD_BK — Q20 *DTC144EUA

+3V — C453 1000P/50V_4

LVDS1 — +3VLCD_CON

EDIDCLK
EDIDDATA
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

L2 SBK160808T-601Y-N
[25] DIGITAL_D1 — L3 SBK160808T-601Y-N — DIGITAL_D1_CN
[25] DIGITAL_CLK — DIGITAL_CLK_L
+5V_CAM
[8] USBP9- — L22 WCM2012-90 — USBP9- L
[8] USBP9+ — USBP9+ L
Webcam
DPST_PWM
BLON_CON
+VIN_BLIGHT
C445 22P/50V_4
GS12401-1011-9F

+3V — C10763 1U/6.3V_4 — U8254 IC(5P) G5243AT11U — +LCDVCC
DISP_ON — R10885 100K/F_4
IN, IN, ON/OFF, OUT, GND
L8041 HCB2012KF-600T30/3A_8
C10764 *0.01U/25V_4 | C10765 0.1U/10V_4 | C10766 10U/6.3V_8

+5V — L28 HCB2012KF-600T30 — +5V_CAM
C447 0.01U/16V_4
C449 10U/6.3V_8
+3VPCU — C443 0.1U/10V_4

U8253 SLB9635

[7,29,32] LAD0
[7,29,32] LAD1
[7,29,32] LAD2
[7,29,32] LAD3
[8] CLK_PCI_TPM
[7,29,32] LFRAME#
[2,8,14,24,27,28,29,32] PLTRST#
[7,32] SERIRQ
[6,32] CLKRUN#

LAD0 LAD1 LAD2 LAD3 CLK_PCI_TPM LFRAME# PLTRST# LPCPD#_TPM SERIRQ CLKRUN#
LCLK LFRAME# LRESET# LPCPD# SERIRQ TEST/BADD CLKRUN# NC NC NC
VDD VDD VDD VSB GND GND GND GND GPIO GPIO2 PP TESTI XTALI/32K IN XTALO

C10756 C10757 C10758 C10759 0.1U
R10874 R10875 R10876 R10879 R10880 *4.7K
R10877 *0 R10878 0/4
TPM_XIN TPM_XOUT 32.768KHZ
Y8024
C10761 18P | C10762 18P

+3V — R450 4.7K/F_4 — LPCPD#_TPM
+3V — R10881 4.7K — R10882 *4.7K

[6,32] SLP_S5
[6] SUS_STAT#
R10883 *0 | R10884 *0 — LPCPD#_TPM

TPM (1.2)

[2,6,7,8,9,10,12,13,14,17,21,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[10,28,29,31,34,35,36,37,38,39,40,41,42,43] +5VS5
[6,7,10,17,21,23,25,29,30,31,41] +5V
[26,29,33,34,35,36,37,40,41,42,43] +VIN
[7,31,32,33,34] +3VPCU
[30,41,43] +12VALW

NB5

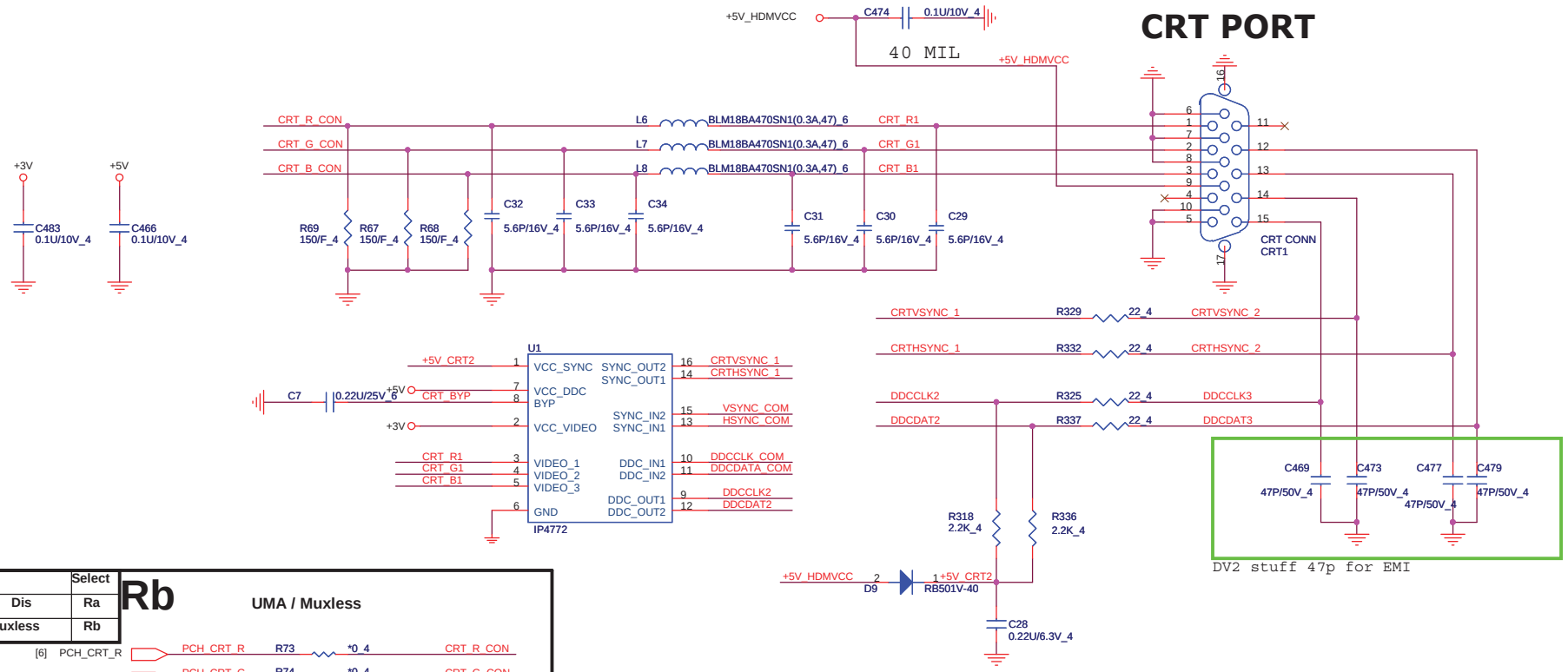
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	3A

Date: Thursday, May 19, 2011 | Sheet 22 of 47

22

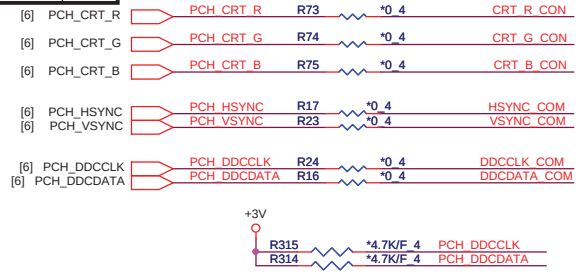
CRT PORT



Rb

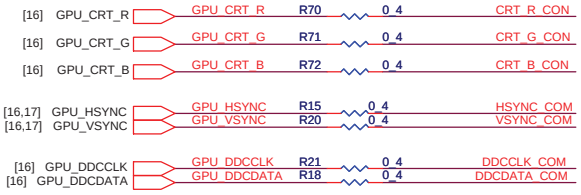
UMA / Muxless

	Select
Dis	Ra
muxless	Rb



Ra

DIS Only



DIS Only / Muxless stuff

+5VCRT

[6,7,10,17,21,22,25,29,30,31,41] +5V

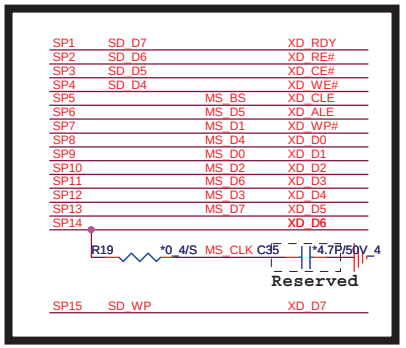
[2,6,7,8,9,10,12,13,14,17,21,22,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

NB5

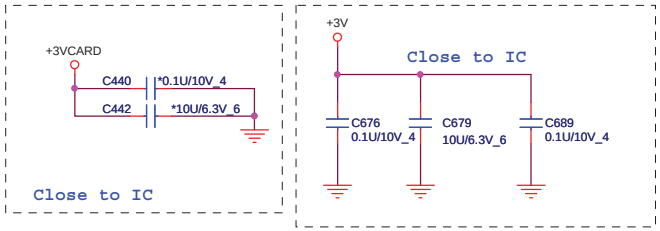
PROJECT : LG2/4 DIS
Quanta Computer Inc.

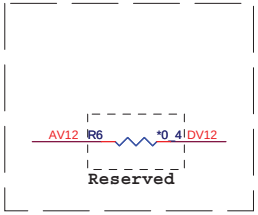
Size	Document Number	Rev
Custom	CRT/HDMI Conn	3A

Date: Wednesday, May 18, 2011 Sheet 23 of 47

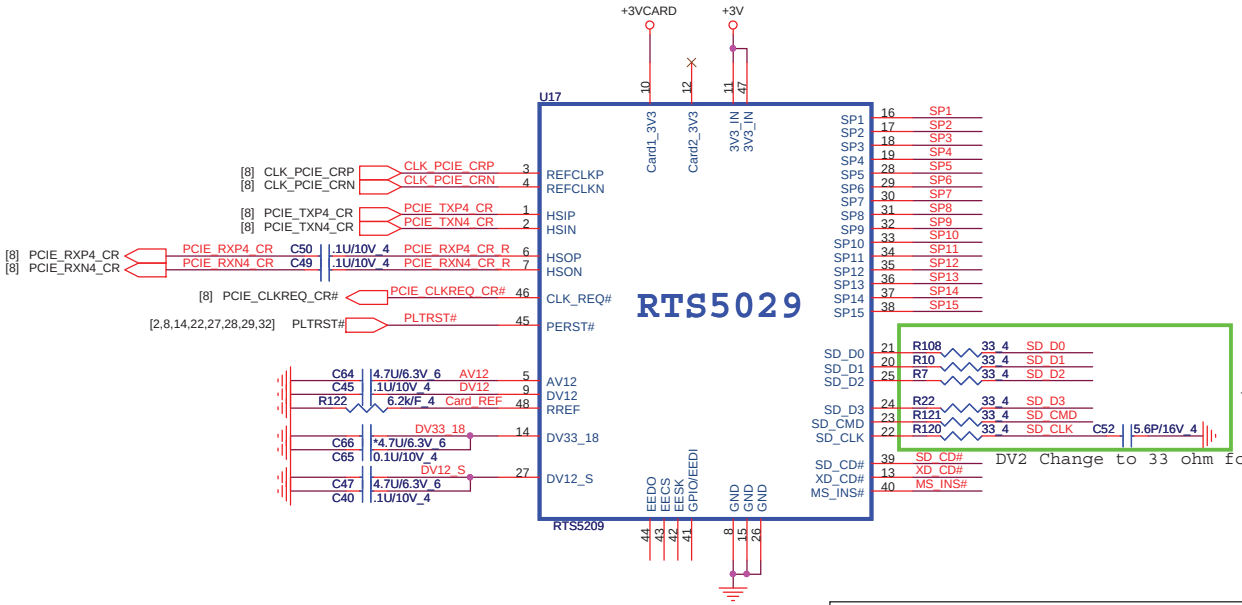


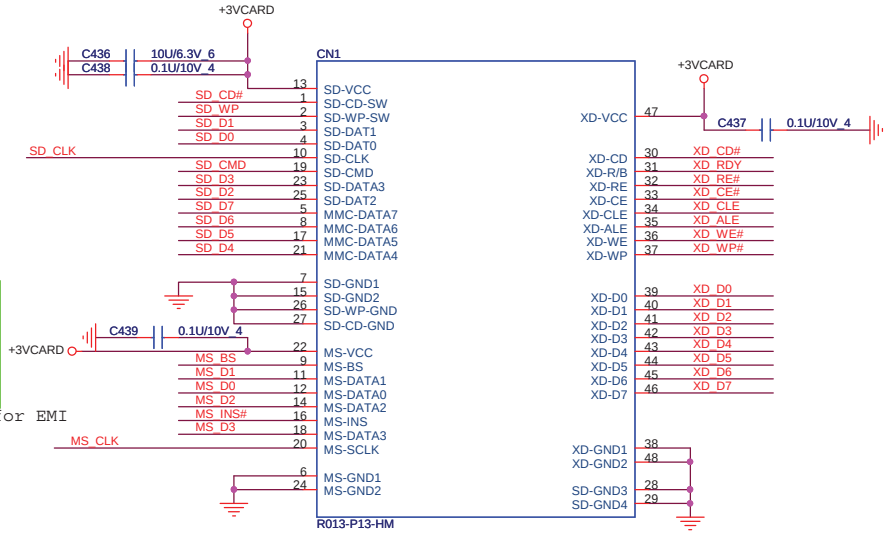
Share Pin

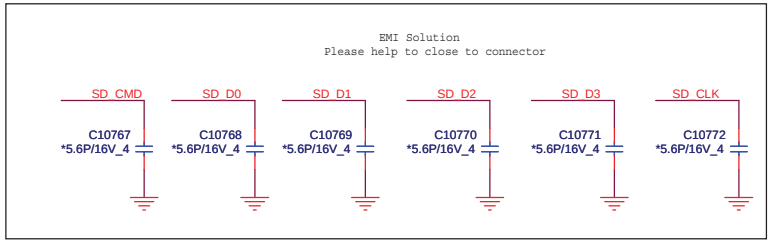




7-in-1
flash media
slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)





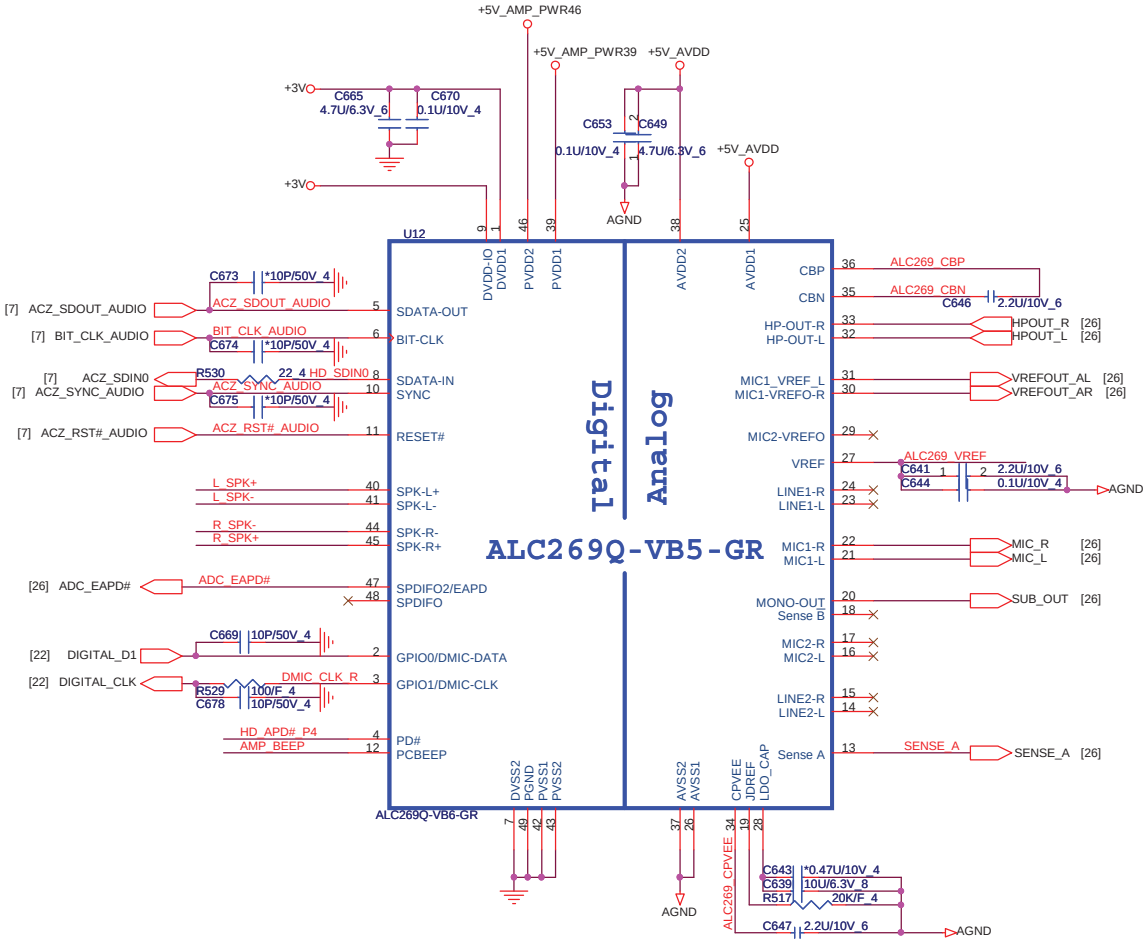


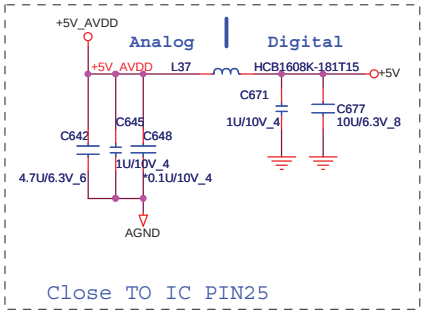
[2,6,7,8,9,10,12,13,14,17,21,22,23,25,26,27,28,29,30,31,32,37,39,41,42] +3V

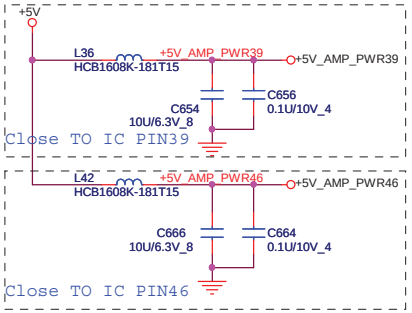
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card reder (RTS5029)	3A
Date: Wednesday, May 18, 2011	Sheet 24 of 47	

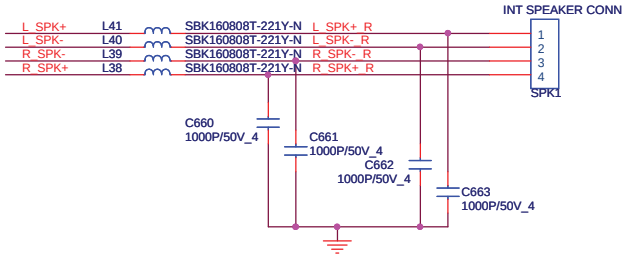
NB5

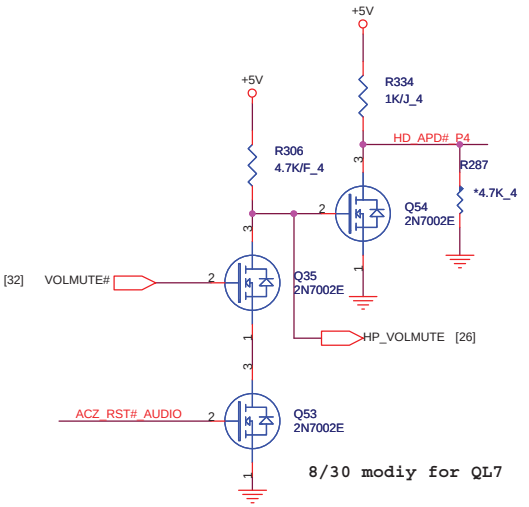






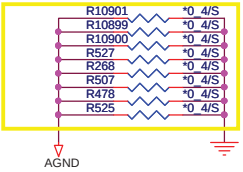
INT. SPEAKER





8/30 modiy for QL7

PV
Change to Shortpad



[6,7,10,17,21,22,23,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,26,27,28,29,30,31,32,37,39,41,42] +3V

NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.		
	Size: Custom	Document Number: HDA Azalia ALC269	Rev: 3A
	Date: Thursday, May 19, 2011	Sheet 25 of 47	

Line out

Normal Open Jack

HPO1

HP-JACK-BLACK

AGND SHIELD

[25] HPOUT_L — HPOUT_L — R504 75_4 — HPOUT_L1 — L35 SBK160808T-301Y-N — HPOUT_L2

[25] HPOUT_R — HPOUT_R — R500 75_4 — HPOUT_R1 — L34 SBK160808T-301Y-N — HPOUT_R2

R512 *0_4 — R513 *0_4

C640 150P/50V_4 — C637 150P/50V_4 — C638 *150P/50V_4 — C634 *150P/50V_4

+3V

R508 *220K_4 — Q47 *ME2303T1

[25] ADC_EAPD#

[25] HP_VOLMUTE — R514 *0_4 — R515 *4.7K_4

R510 *1K/F_4 — Q49 *AP2302GN

R511 *1K/F_4 — Q51 *AP2302GN

R516 *4.7K_4 — C504 *1U/10V_4

Reduce headphone POP

SENSE_PHONE — R506 39.2K/F_4 — SENSE_A — SENSE_A [25]

HPOUT_L2 — CD3 — CD4 — Clamp-Diode — Clamp-Diode

HPOUT_R2 — CD3 — CD4 — Clamp-Diode — Clamp-Diode

MIC_IN_R — CD2 — CD1 — Clamp-Diode — Clamp-Diode

MIC_IN_L — CD2 — CD1 — Clamp-Diode — Clamp-Diode

SENSE_PHONE — CD5 — Clamp-Diode

SENSE_MIC — CD6 — Clamp-Diode

MIC

Normal Open Jack

MIC1 HP-JACK-BLACK

[25] VREFOUT_AR — VREFOUT_AR

[25] VREFOUT_AL — VREFOUT_AL

R258 4.7K/F_4 — R229 4.7K/F_4 — C348 *1U/10V_4

C406 *1U/10V_4

C361 100P/50V_4 — C337 100P/50V_4

C389 4.7U/6.3V_6

[25] MIC_L — MIC_L — MIC_L1_RC — R252 1K/F_4 — MIC_L1 — L24 SBK160808T-301Y-N — MIC_IN_L

[25] MIC_R — MIC_R — C354 4.7U/6.3V_6 — MIC_R1_RC — R228 1K/F_4 — MIC_R1 — L23 SBK160808T-301Y-N — MIC_IN_R

SENSE_A 20K/F_4 — R505 — SENSE_MIC

Sub-Woofer for 17"

+VIN — R10849 *0_8/S short0805 — PVCC2

PV change to short pad

U8252 *HPA00836

Pin	Name	Pin	Name
1	SD	28	PVCCL
2	FAULT	27	PVCCL
3	NC_3	26	BSN_26
4	NC_4	25	OUTN_25
5	GAIN0	24	PGND
6	GAIN1	23	OUTN_23
7	AVCC	22	BSN_22
8	AGND	21	BSP_21
9	GVDD	20	OUTP_20
10	PLIMIT	19	PGND
11	INN	18	OUTP_18
12	INP	17	BSP_17
13	NC_13	16	PVCC
14	AVCC	15	PVCC
29	GND		

+3V — R10845 *100K_4 — ADC_EAPD# — [25] ADC_EAPD#

+3V — R10848 *100K_4

PVCC2 — R10850 *100K_6

R10852 *100K_6

SUB_GND — R10851 *0_6/S

R10854 *0_6/S

PVCC2 — R10856 *10_6 — C10735 *1U/25V_6

SUB_GND — C10737 *1U/25V_6

R10858 *47.5K/F_6

SUB_GND — C10738 *1U/25V_6 — R10859 *27.4K/F_6

SUB_GND — C10741 *1U/25V_6 — R8034 *0_6

[25] SUB_OUT — SUB_OUT — C10742 *1U/25V_6 — R8036 *0_6

PVCC2 — R10860 *10K_6

C10730 *1000P/50V_6 — C10731 *0.1U/50V_6 — C10732 *100U/25V L-F — SUB_GND — PVCC2

C10733 *0.22U/50V_8

SUB_GND

C10734 *0.22U/50V_8 — C10736 *0.22U/50V_8

SUB_GND

C10743 *0.22U/50V_8

PVCC2

C10744 *1000P/50V_6 — C10745 *0.1U/50V_6 — SUB_GND

L8037 *PBY160808T-151Y-N — SUB_OUT+

L8038 *PBY160808T-151Y-N — SUB_OUT-

CN8202 *88266-020L

C10739 *1000P/50V_4 — C10740 *1000P/50V_4

SUB_GND

R10844 *0_4 — L8036 *0_8 — R10846 *0_6 — R10847 *0_4 — SUB_GND

R10853 *0_8 — R10855 *0_8 — SUB_GND

R10857 *0_8 — SUB_GND

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

[22,29,33,34,35,36,37,40,41,42,43] +VIN

[6,7,10,17,21,22,23,25,29,30,31,41] +5V

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,32,37,39,41,42] +3V

NB5

PROJECT : LG2/4 DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio Jack/Accelerometer	3A

Date: Wednesday, May 18, 2011 — Sheet 26 of 47

Atheros Lan

placed 0.1U within 200 mil close to AR8151

placed VDD33 CAP within 400 mil close to AR8151

PLACE NEAR LAN IC PIN6

Add R139 for LAN POWER issue

Atheros AR8151

AR8151-AL1A-R

TP9056

RJ45C1

RJ45

PLACE NEAR LAN IC SIDE

TRANSFORMER

U28 NS892405

PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LAN AR8151/RJ45	3A

Date: Wednesday, May 18, 2011 Sheet 27 of 47

VIA VL801

U8248

PORT1 PORT2 PORT3 PORT4

USB3.0/USB2.0 x1 COMBO

Del USB3 from Chipset

CN8201 USB3.0 CONN

D32 *SP3010-04UTG

PV for USB3.0 ESD

Clamp-Diode

CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define Battery % and wake up from USB		SDP		OFF

	Select
USB3.0	Ra
USB2.0	Rb

Charger USB

Add R10911,R10912,R10596 for TPS2543

80 mils (Iout=2A) high active

Ios = 48000/RILIM0 default: Auto-detect

TPS2540/41

	Power switch select
LG	Rc
CB	Rd

PV USB Power switch for CB

U2 *G545A2PU8

Add NET Charger_ON and R10893 to U8249 Pin5

DV2 ...FOR EMI

To Host

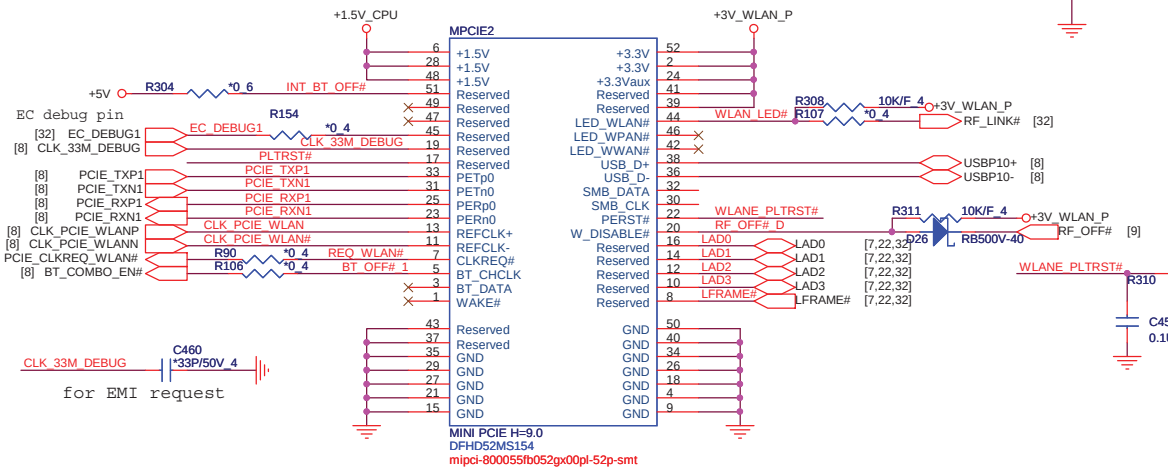
NB5

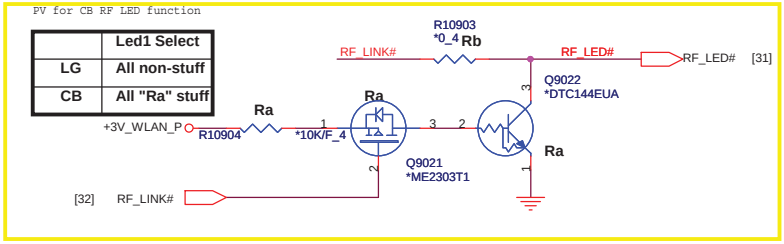
PROJECT : LG2/4 DIS
Quanta Computer Inc.

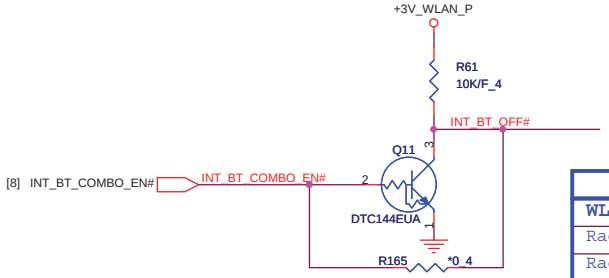
Size: Custom | Document Number: USB 3.0 Controller (VIA_VL801) | Rev: 3A

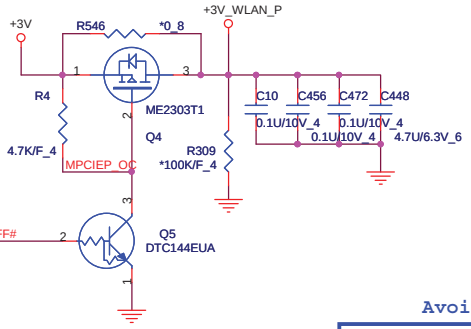
Date: Thursday, May 19, 2011 | Sheet 28 of 47

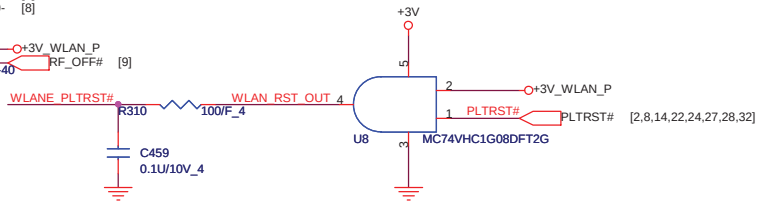
Mini PCI-E Card 1 - Half WLAN

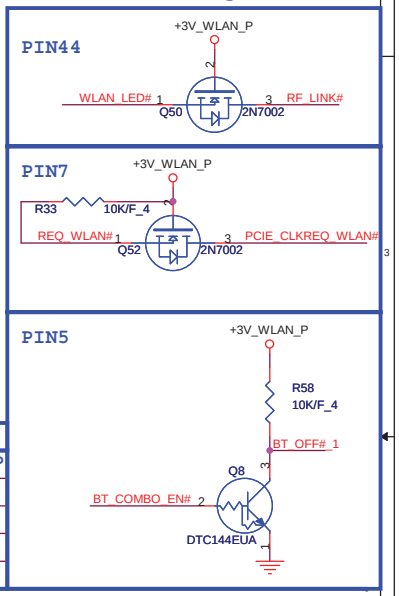






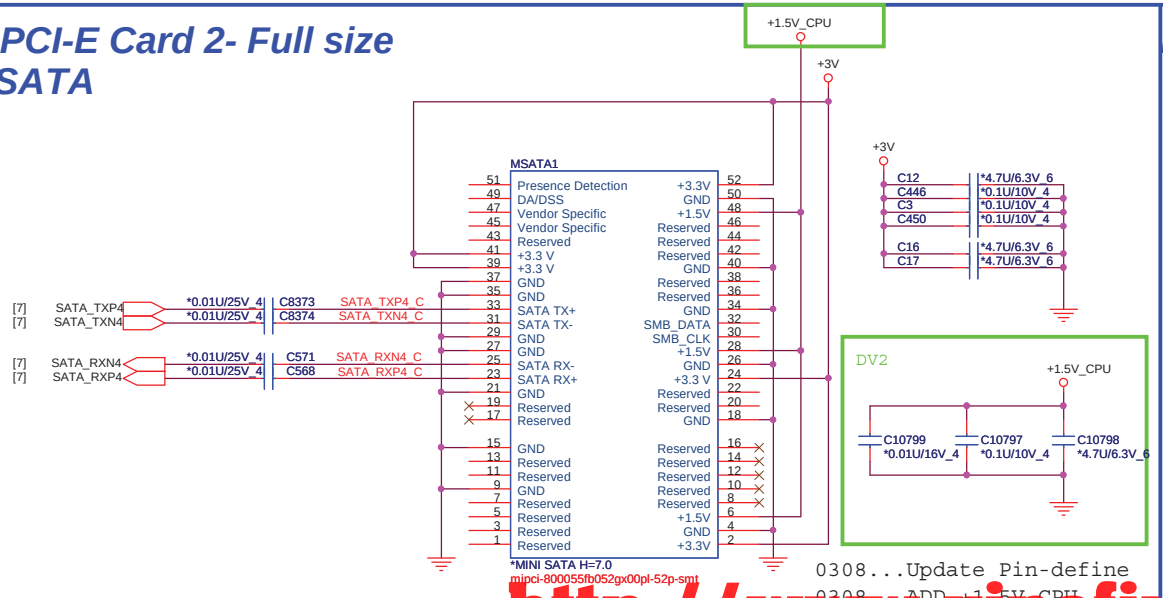




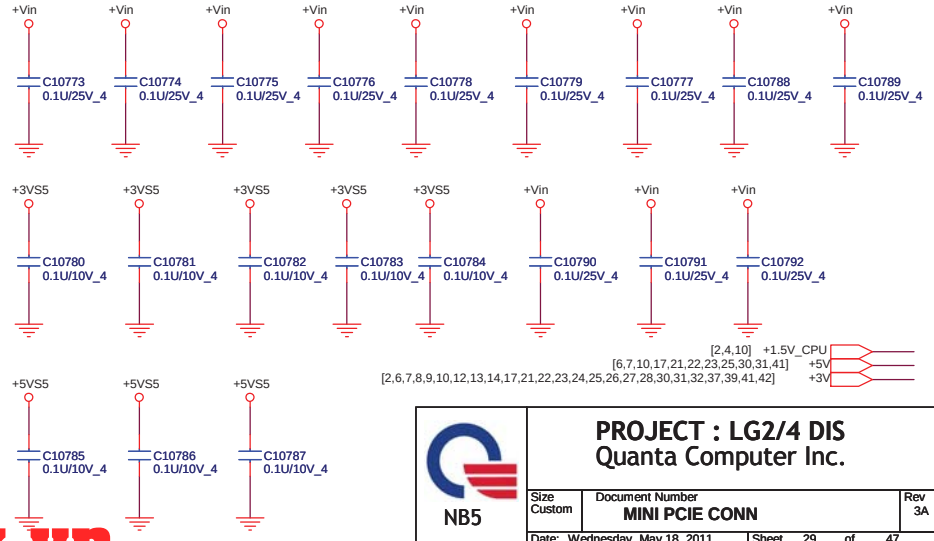


LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

Mini PCI-E Card 2- Full size MINISATA



Power Plan Cap for EMI



NB5

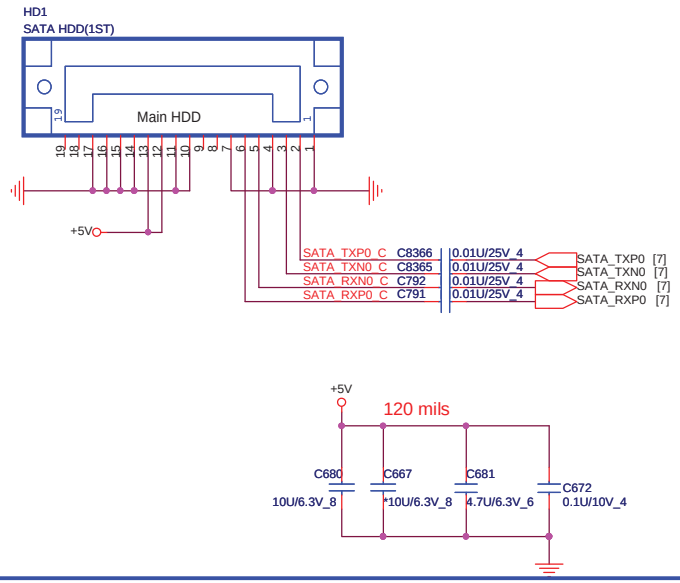
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN	3A

Date: Wednesday, May 18, 2011 Sheet 29 of 47

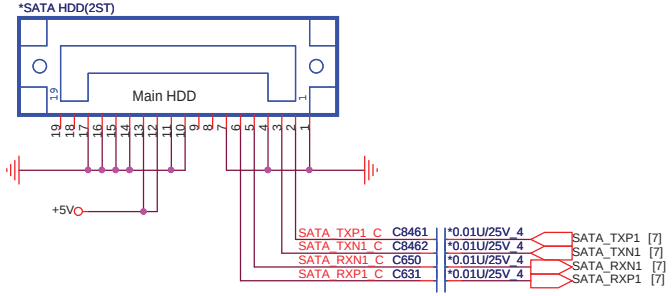
MAIN SATA HDD

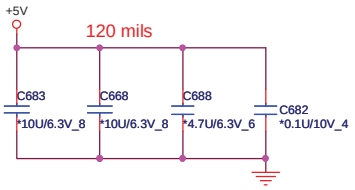
DC Current rating: 0.5 A



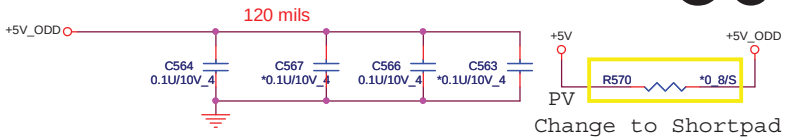
2nd SATA HDD for 17"

DC Current rating: 0.5 A



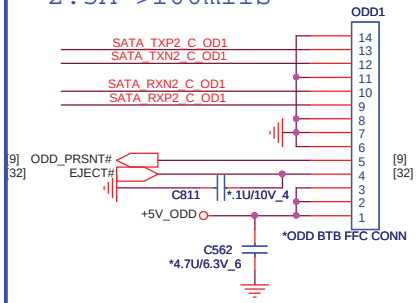


SATA CD-ROM To ODD Board



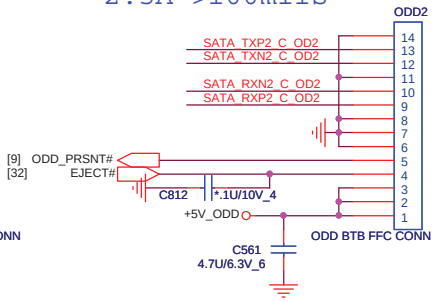
For 17" place

2.5A >100mils



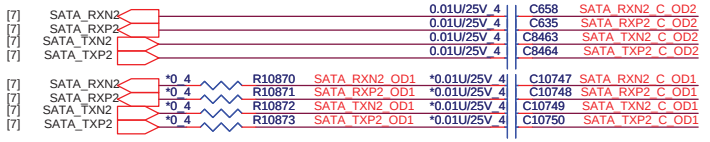
For 14"/15" place

2.5A >100mils



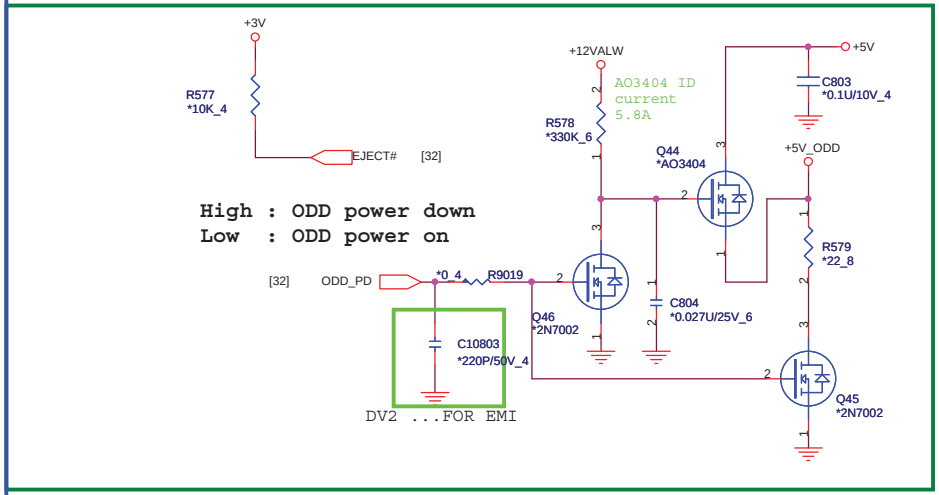
Ra FOR 14"/15"
Rb FOR 17"

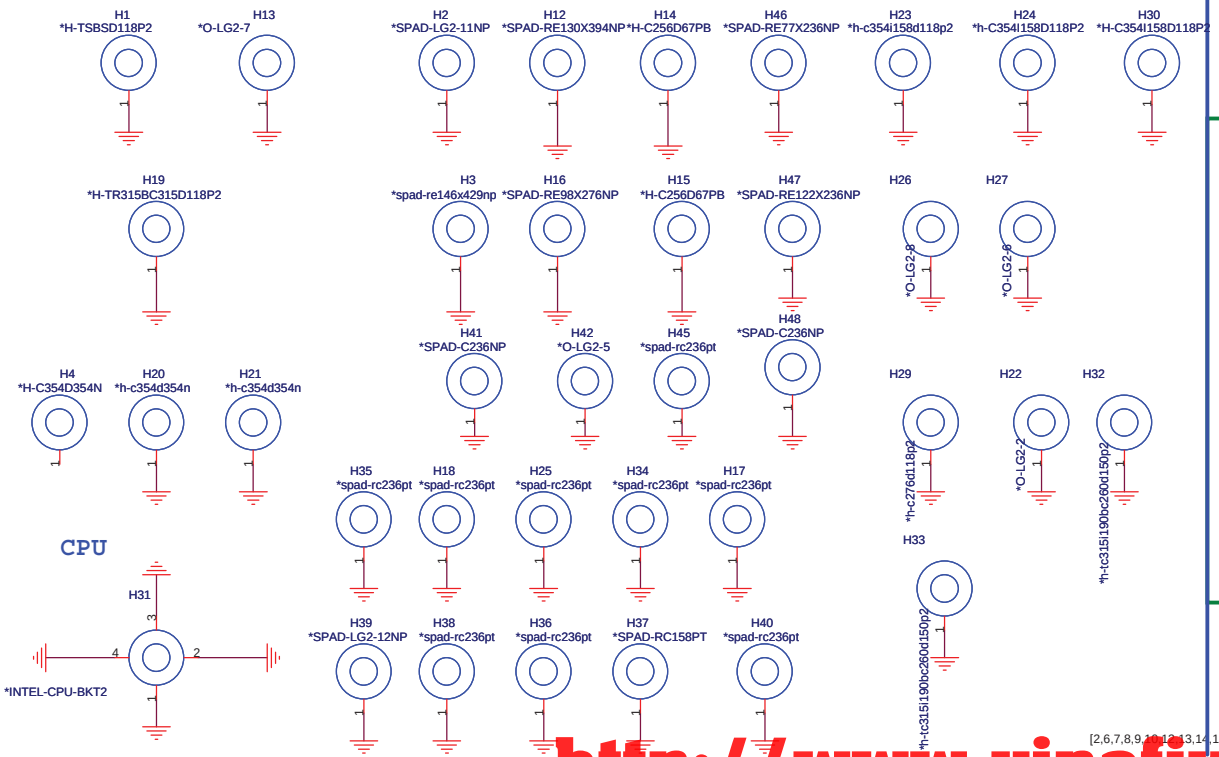
Ra



Rb

Rb





[41,43] +12VALW
[6,7,10,17,21,22,23,25,29,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,31,32,37,39,41,42] +3V

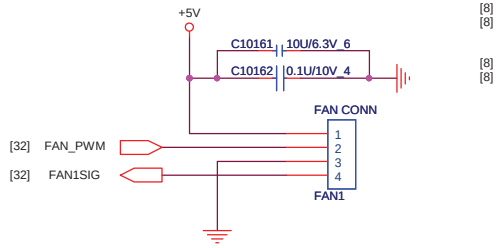
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

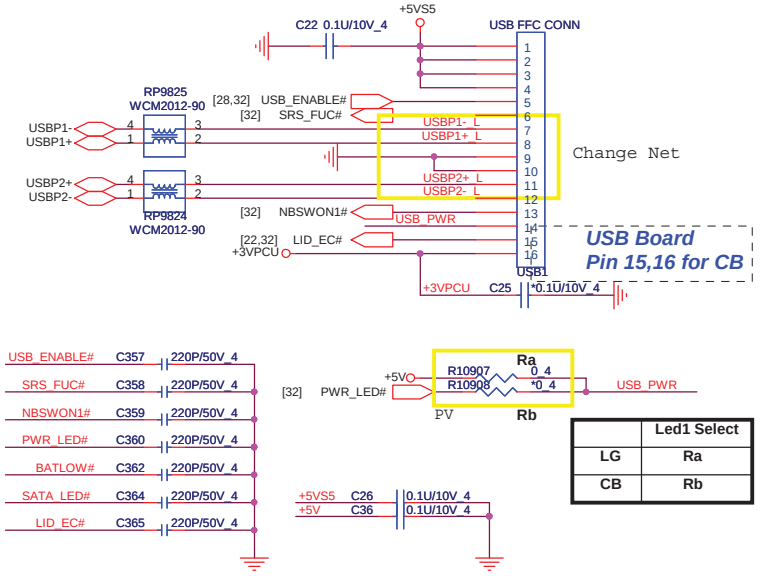
Size	Document Number	Rev
Custom	ODD/HDD/HOLES	3A

Date: Thursday, May 19, 2011 Sheet 30 of 47

CPU FAN

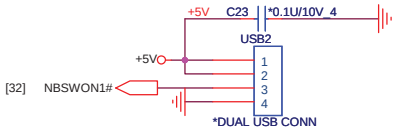


USB / Power LED & SW for 14"/15"/17" To USB Board



	Led1 Select
LG	Ra
CB	Rb

Power SW for 17"



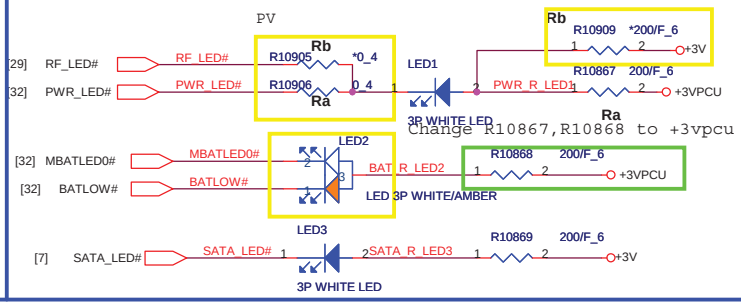
LED

Select Pin

	Led1 Select
LG	Ra
CB	Rb

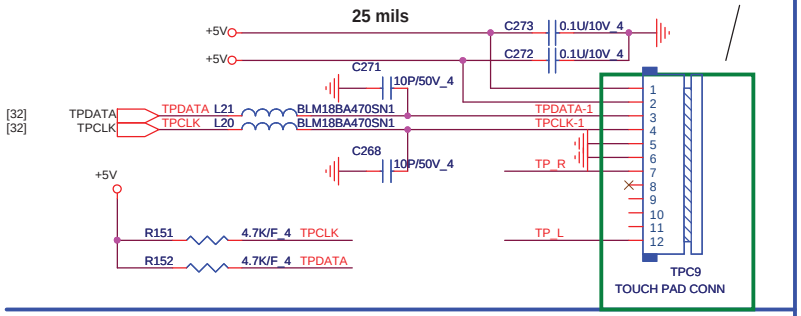
	Led2 P/N
LG	BEWH0051Z00
CB	BEWY0007ZA0

10 mils (250mA)

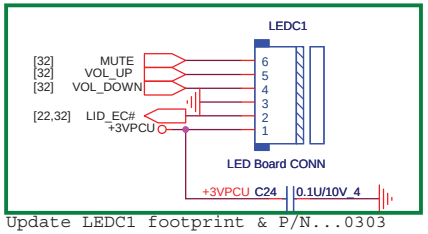


TOUCH PAD CONNECTOR To Click Board & FP

Update TPC9 footprint & P/N...0303

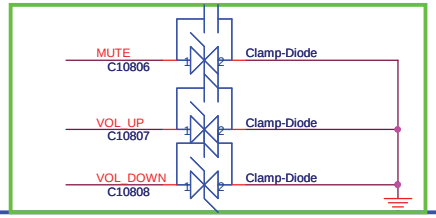


LID / MUTE / VU UP / VU DO To AD Function Board

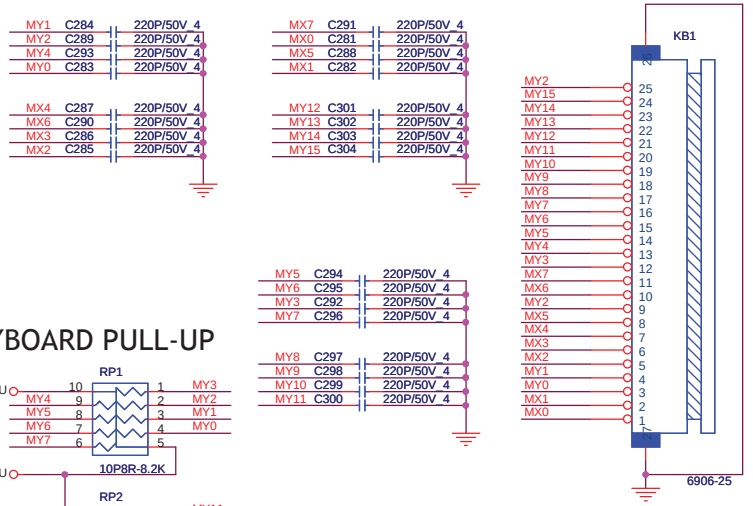


Update LEDC1 footprint & P/N...0303

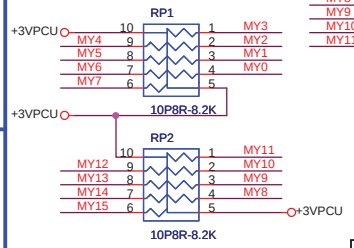
DV2 ...FOR EMI



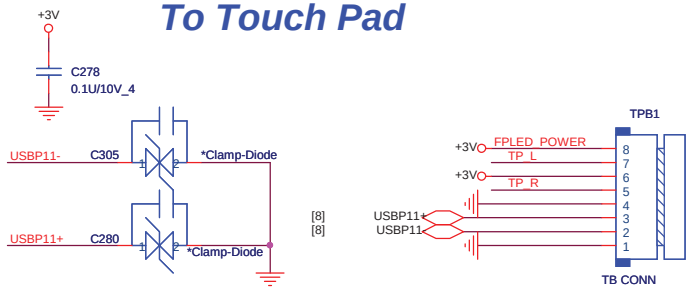
KEYBOARD Con.



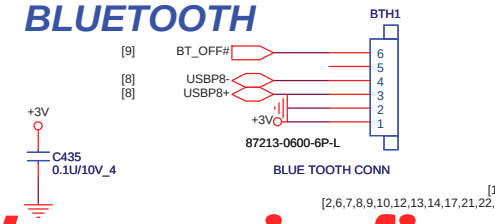
KEYBOARD PULL-UP



TP Button CONNECTOR To Touch Pad



BLUETOOTH



[6,7,10,17,21,22,23,25,29,30,41] +5V
[10,28,29,34,35,36,37,38,39,40,41,42,43] +5VS5
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,32,37,39,41,42] +3V
[7,22,32,33,34] +3VPCU

[32] MY[0..15]
[32] MX[0..7]

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USB/eSATA	3A

Date: Wednesday, May 18, 2011 Sheet 31 of 47

DV2 ... FOR EMI

LAD0 C10809 *220P/50V_4
LAD1 C10810 *220P/50V_4
LAD2 C10811 *220P/50V_4
LAD3 C10812 *220P/50V_4
PLTRST# C10813 *220P/50V_4

+VCC_RTC R270 *0_4 +3V +3VPCU R271 *0_4/S
+3V_ECACC L7001 BK1608HS220-T +3VPCU
C7008 1U/6.3V_4 C7009 1000P/50V_4
IT8502_AGND IT8502_AGND
+3v_STBY L7002 BK1608HS121-T +3VPCU
C7011 0.1U/10V_4
C7012 0.1U/10V_4

+3V_RTC R7001 *0/short_4 +VCC_RTC
C7010 0.1U/10V_4

+3VPCU 12 MILS
C7002 0.1U/10V_4 C7003 0.1U/10V_4 C7004 0.1U/10V_4 C7005 0.1U/10V_4 C7006 0.1U/10V_4 C7007 0.1U/10V_4

Layout Note:
Place all capacitors close to IT8502N.

+3VPCU R7006 470K/J_4 EC_WRST C7013 0.1U/10V_4

U7001

IT8518/CX

LPC: LAD0 LAD1 LAD2 LAD3 LPCRST#/WUI4/GPD2 LPCCLK LFRAME# LPCPD#/WUI6/GPE6
GPIO: GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/BBO/GPC7 GPC0 TMA0/GPB2
PS/2: PS2DAT0/TMB1/GPF1 PS2CLK0/TMB0/GPF0 PS2DAT2/WUI21/GPF5 PS2CLK2/WUI20/GPF4
UART: DAC4/DCD0#/GPJ4 DSR0#/GPG6 GINT/CTS0#/GPD5 PS2DAT1/RTS0#/GPF3 DAC5/RIG0#/GPJ5 PS2CLK1/DTR0#/GPF2 RXD/SIN0/GPB0 TXD/SOUT0/GPB1
FLASH: GPG0 FSCK FMISO FMOSI FSCE# SSCE0#/GPG2
KBMX: KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7
CLOCK: CK32K CK32KE
SM_BUS: SMCLK2/WUI22/GPF6/PECI SMDAT2/WUI23/GPF7 SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2
PWM: PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/GPA7 TACH0/GPD6 TACH1/TMA1/GPD7 TMR0/WUI2/GPC4 TMR1/WUI3/GPC6
WAKE UP: PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1 WUI5/GPE5 RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
A/D D/A: ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/WUI29/GPI5 ADC6/WUI30/GPI6 ADC7/WUI31/GPI7 DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3
VCC VSTBY VBAT AVCC VSS VCORE
IT8518E

[7,22,29] LAD0 LAD1 LAD2 LAD3 [2,8,14,22,24,27,28,29] PLTRST# [8] CLK_33M_KBC [7,22,29] LFRAME# [6,22] SLP_S5
[9] EC_A20GATE [7,22] SERIRQ [9] SIO_EXT_SMI# [9] SIO_EXT_SC# [9] EC_RCIN# T7009
D7009 D7001 D7000 D7012 RB501V-40 EC_WRST
[33] D/C# [6] RSMRST#
DV2 [28] Charger_ON H_PROCHOT# EC
[31] TPDATA [31] TPCLK
CB/LG [30] ODD_PD [28] USB_CHR_C3 [34,35,36,37,38] HWPG [22] LID_CONTROL
D5 need to close PCH. TP9040 [7] ACZ_SDOUT D5 RB501V-40 [29] EC_DEBUG1 GPIO33_E_R
[28,31] USB_ENABLE# EC_SCK EC_SCK_L SBY100505T-121Y-N L8042
C10822 22P_50v
EC_SO EC_SI EC_CE# [3] EJECT# [3] MY[0..15]
[31] MX[0..7]
[6] PCH_SUSCLK R7020 *0/J_4 EC_CK32K *0_4/S R331
L7000 BK1608HS121-T IT8502_AGND
IT8502_AGND C7015 0.1U/10V_4

EGCLK/WUI27/GPE3 EGCS#/WUI26/GPE2 BATLOW VRON [39]
EGAD/WUI25/GPE1 SLP_A# [6]
KSO16/SMOSI/GPC3 KSO17/SMISO/GPC5 EC_PWROK [6,17] SUSACK# [6]
L80HLAT/BAO/WUI24/GPE0 L80LLAT/WUI7/GPE7 SUSON [35,41] SRS_FUC# [31]
SBUSY/GPG1/ID7 HMOSIGPH6/ID6 HMISO/GPH5/ID5 HSCK/GPH4/ID4 HSCE#/WUI19/GPH3/ID3 CTX1/WUI18/GPH2/SMDAT3/ID2 CRX1/WUI17/GPH1/SMCLK3/ID1 CLKRUN#/WUI16/GPH0/ID0
MBATLED0 H_SI R7002 *0_4/S H_SO R7003 *0_4/S H_CLK R7004 *0_4/S H_SCE# R7005 *0_4/S
PCH_SPI_SI [7] PCH_SPI_SO [7] PCH_SPI_CLK [7] PCH_SPI_CS0# [7] MAINON [33,35,36,37,38,41] RF_LINK# [29] CLKRUN# [6,22]
SMCLK2/WUI22/GPF6/PECI SMDAT2/WUI23/GPF7 SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2
EC_PECI_R R7014 *0_4/S EC_PECI [2]
MBCLK MBDATA MBCLK2 MBDATA2
SLP_SUS# [6] MBCLK [33] MBDATA [33] MBCLK2 [8,13,17] MBDATA2 [8,13,17]
For Battery charge/charge and cap board
For PCH SMB/DDR Thermal IC/VGA
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/GPA7
Num LK SATA5GP
LAN_POWER [41] T7008 AC_PRESENT [6] SATA5GP [9] SUS_PWR_ACK [3] VOLMUTE# [25] T7012
TACH_FAN_IN_R D7003 RB501V-40 FAN1SIG [31]
3VS5_ON [34]
SUSC# [6] 5VS5_ON [34]
C7019 0.1U/10V_4
NBSWON1# NBSWON1# [31] LID_EC# [22,31] ACIN [33] SUSB# [6] PWR_LED
DGPU_PWROK [9,17,42,43] GFX_HWPG [39] SYS_I [33] AD_AIR [33] TEMP_MBAT [33] MUTE [31] VOL_UP [31] VOL_DOWN [31]
USB_CHR_C1 [28] DGPU_PROCHOT [16] DNBSWON# [6]
D7002 RB501V-40 R181 10K/F_4 +3VS5
FOR UMA R7015 *10K/J_4 DGPU_PWR_EN [9,42,43]
DV2 add DGPU_PWROK for muxless no thermal

Select Pin
Rb R8499 *10K_4 CB/LG Ra R8496 10K_4 +3VPCU

LG Select	
LG	Ra
CB	Rb

Led1 Select	
LG	non-stuff
CB	Rc

H_PROCHOT# Q R7061 *0_4/S H_PROCHOT# [2,39]
H_PROCHOT# EC Q7004 2N7002E R7017 100K/J_4
+3VPCU R7013 10K/J_4 NBSWON1# C7014 0.1U/10V_4
Rc MBATLED0# [31] MBATLED0 Q9023 *2N7002
PWR_LED# [31] PWR_LED Q38 2N7002E
BATLOW# [31] BATLOW Q40 2N7002E

0330....add FAN PWM control at pin30
R10894 *0_4/S FAN_PWM [31]

thermal shutdown circuit
EC_WRST EC_CT_UP R130 *4.7K/F_4 +1.05V_VTT C238 220P/50V_4 PV Change PM_THRMTRIP# [2,9]
Q14 *MMBT3904-7-F

MBCLK R7009 10K/J_4 MBDATA R7007 10K/J_4 SRS_FUC# R7016 10K/J_4
TPCLK R7011 *10K/J_4 TPDATA R7012 *10K/J_4 MBCLK2 R7010 10K/J_4 MBDATA2 R7008 10K/J_4 TACH_FAN_IN_R R10185 10K/F_4 MUTE R10896 10K/J_4 VOL_UP R10897 10K/J_4 VOL_DOWN R10898 10K/F_4
0330....audio function button need add pull-high Res

SPI FLASH EN25Q32B-104HIP: AKE39ZN0Q02
MX25L3206EM2I-12G: AKE39FP0Z02
Socket: DG008000031
U7002 CE# SCK SI SO WP# HOLD# VSS VDD
EC_CE# EC_SCK R7023 47/J_4 EC_SCK_R EC_SI R7024 47/J_4 EC_SI_R EC_SO R7025 15/J_4 EC_SO_R
+3VPCU R7027 10K/J_4 R7026 10K/J_4 C7018 0.1U/10V_4
EC_SCK_R R10910 47_4 C10823 22P
SPI Flash Socket

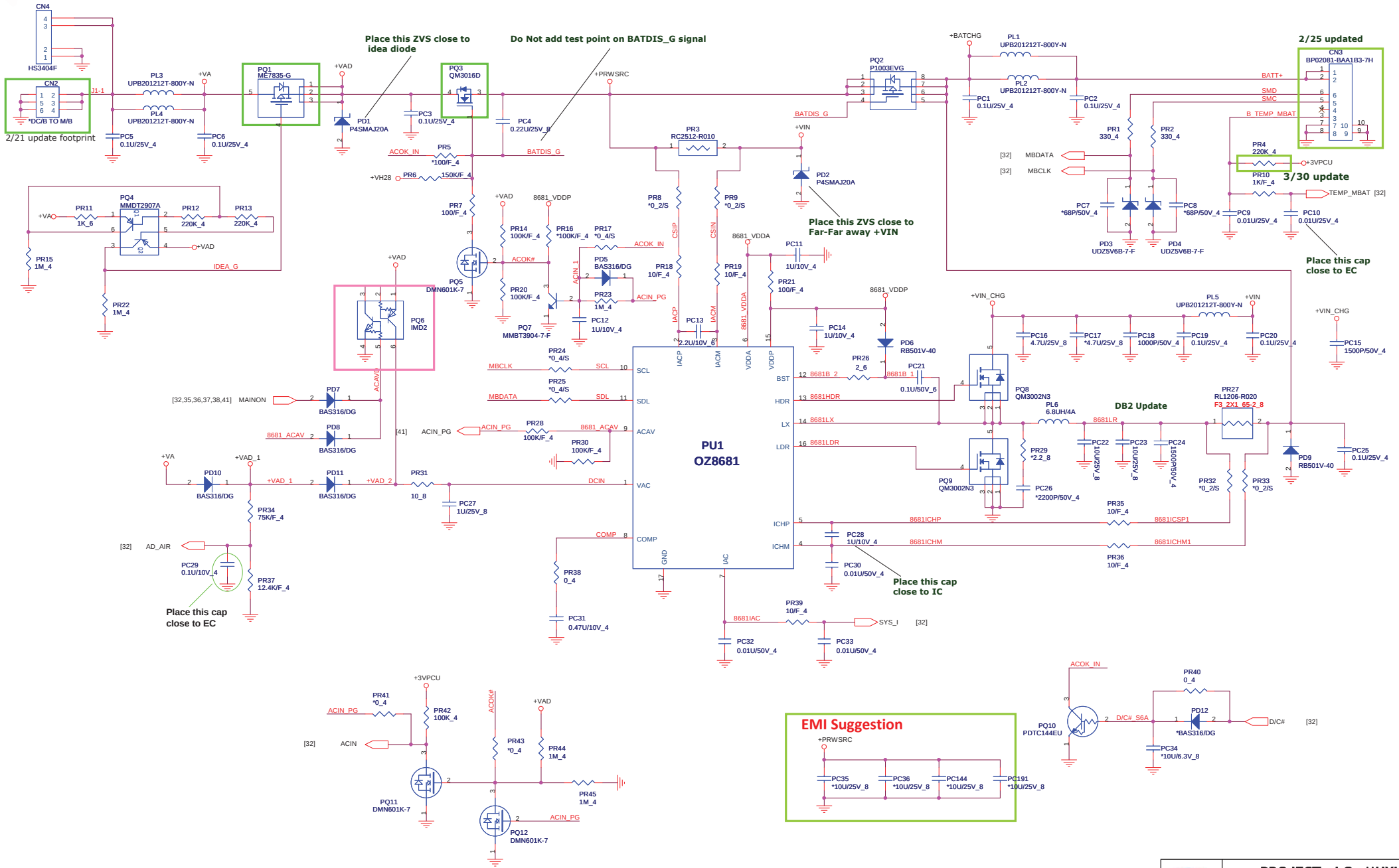
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IT8515/CX/FLASH	3A
Date: Friday, May 20, 2011	Sheet 32 of 47	

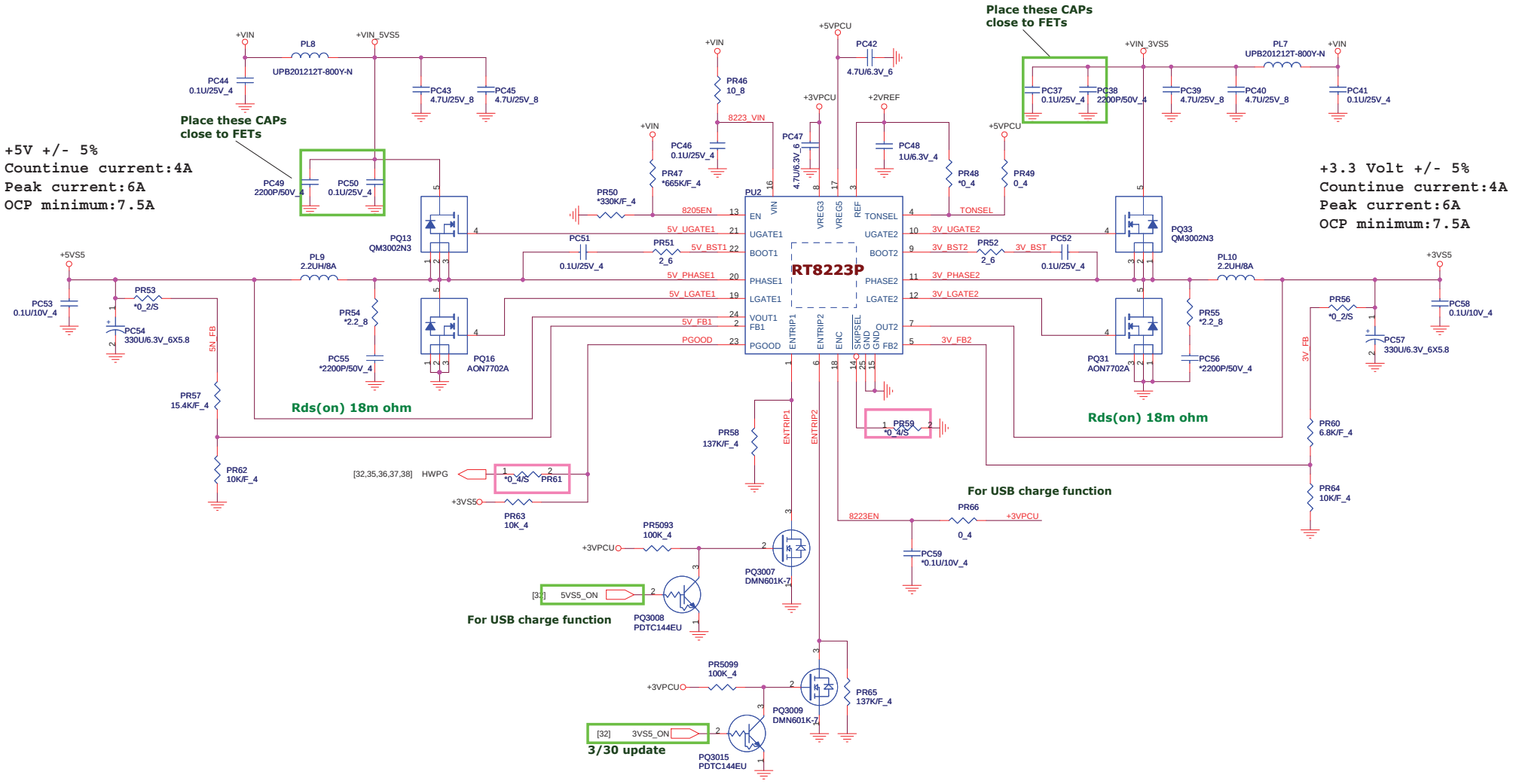
LG2_DIS only

TOP DC JACK
90W/120W(QC)



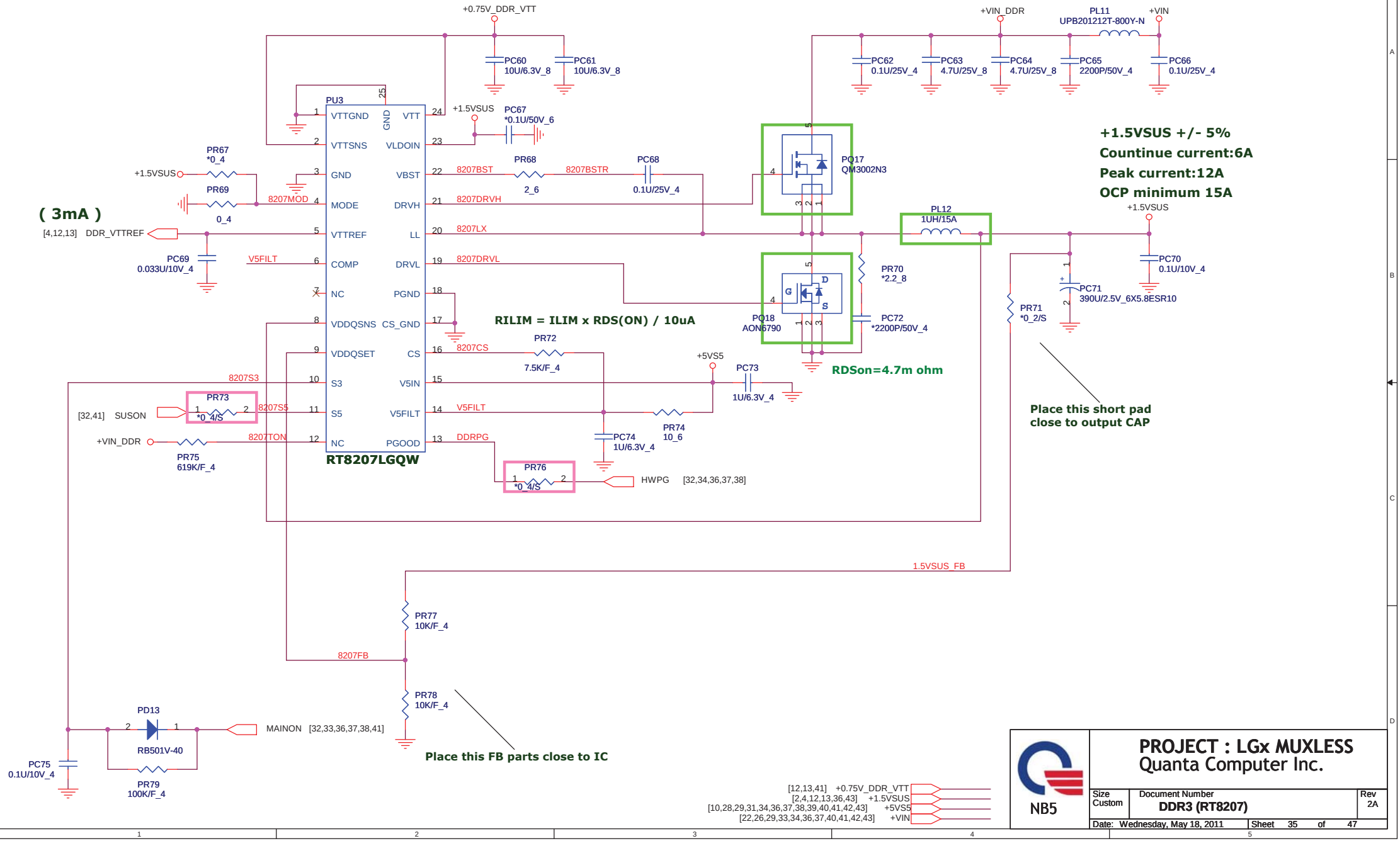
NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.		
Size: Custom	Document Number: Charger (OZ8681)		Rev: 2A
Date: Thursday, May 19, 2011	Sheet 33 of 46		

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

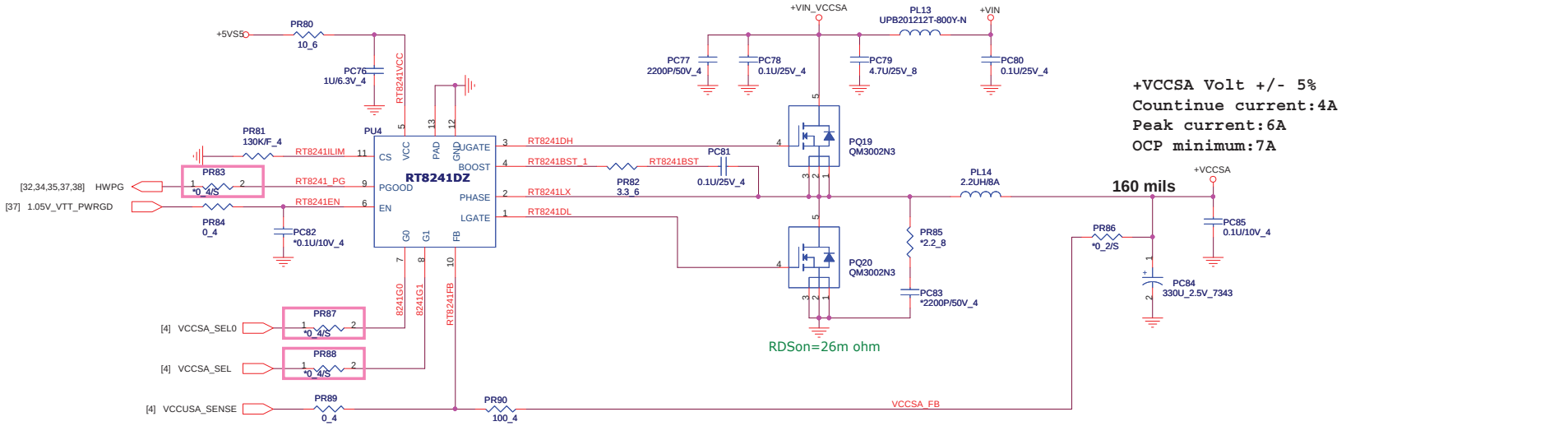


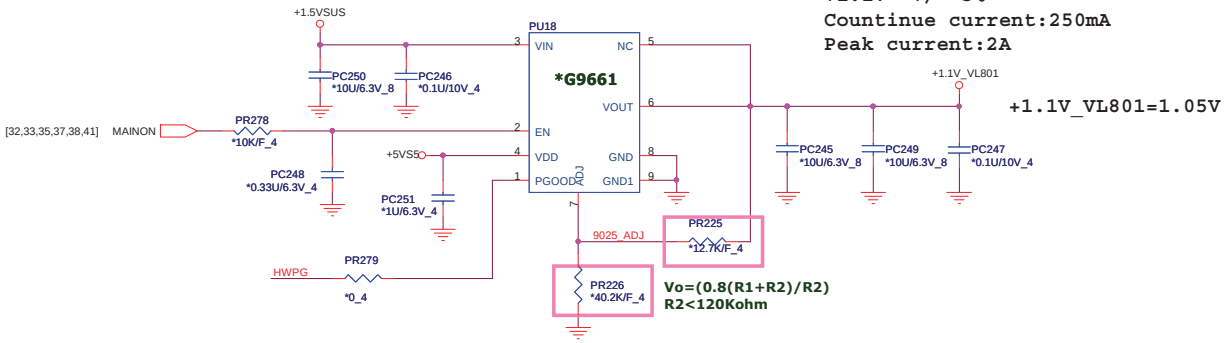
NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.		
	Size: Custom	Document Number: 3/5VS5 (RT8223M)	Rev: 2A
	Date: Wednesday, May 18, 2011	Sheet 34 of 47	

(VTT/2A)

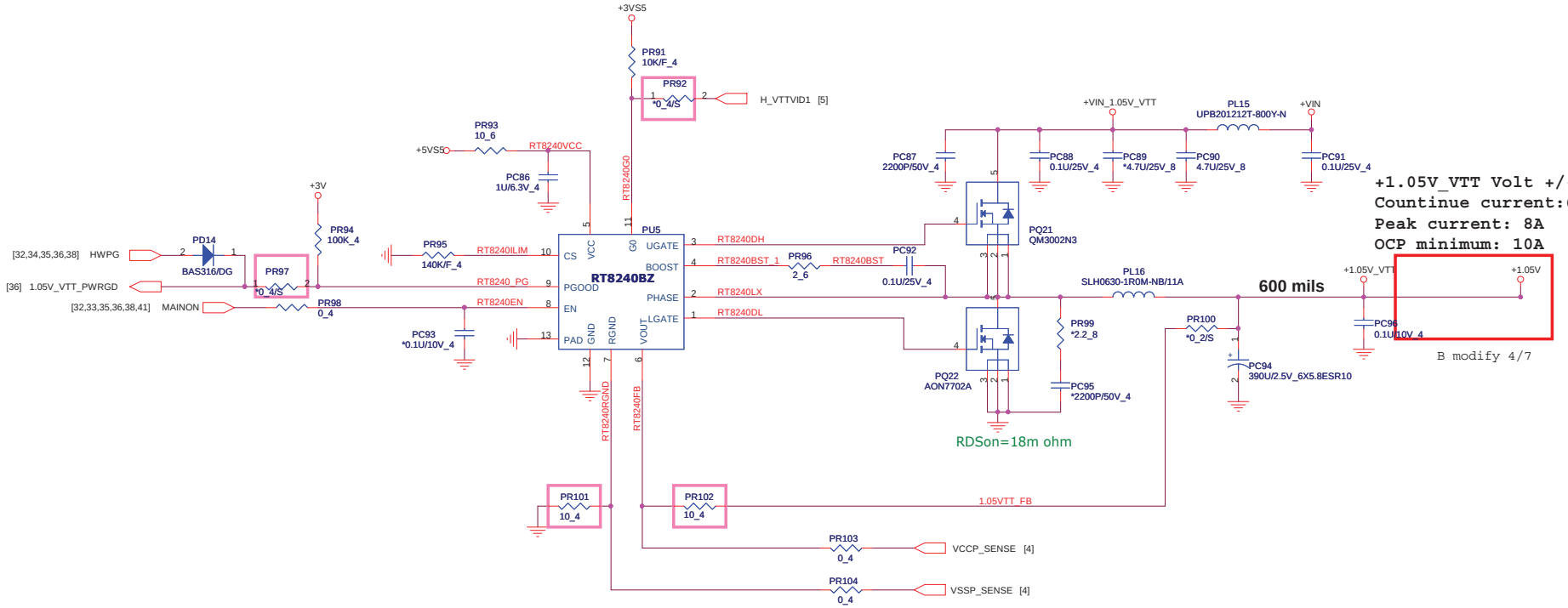


NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 35 of 47	

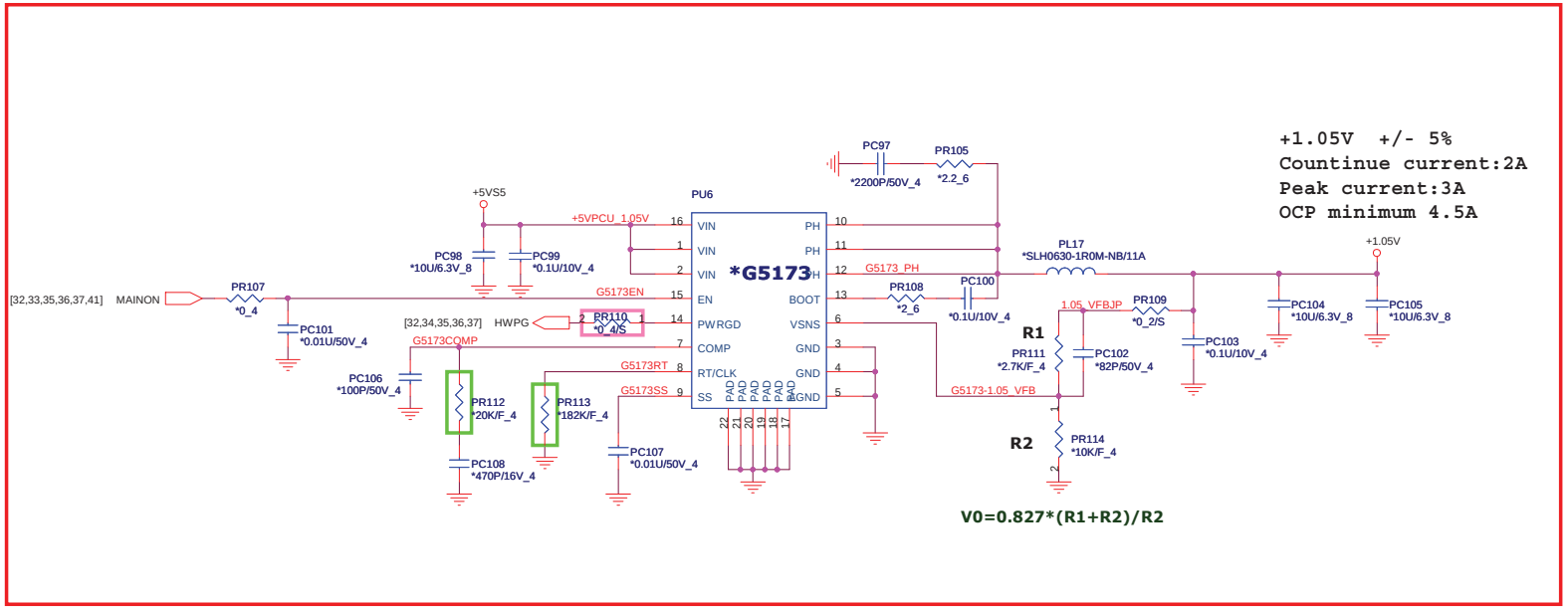


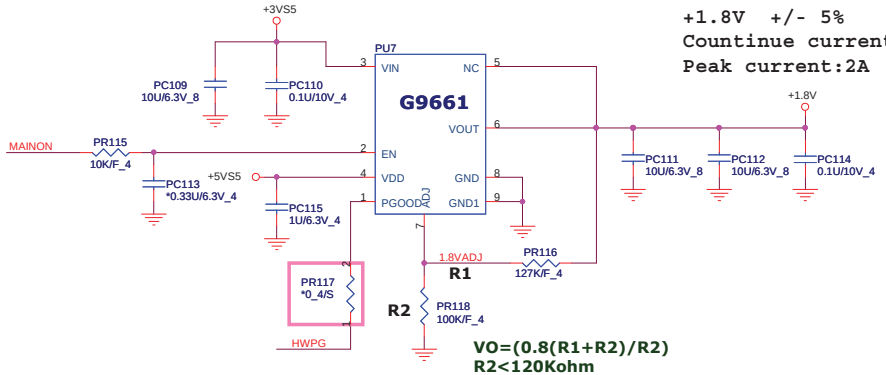


NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: VCCSA (RT8241A)	Rev: 2A
Date: Thursday, May 19, 2011	Sheet 36 of 47	



NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V_VTT(RT8240B)	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 37 of 46	





NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V/+1.8V (G5173)	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 38 of 47	

sky blue color is disable GT setting

B modify 4/15

+5VS5
PR139 *0_4
TRBSTA#

PC133 *0.1U/10V_4
PR136 0_4
6132AGND
IMONA
PC136 0_4
PC137 *470P/50V_4
PR134 *75K/F_4
PR135 *220K_6 NTC
PR140 *165K/F_4
Place close with GT Inductor

PR141 *10/F_4
PR142
PC138 *33P/50V_4
*1K/F_4
PC139 0_4
PR143 *4.3K/F_4
PC140 *3300P/50V_4

B modify 4/13
PR145 *68K_6
SWN1A
SWN1A [40]
6132AGND
Change size to RC0402
PR147 *14K/F_4

[4] VCC_AXG_SENSE
[4] VSS_AXG_SENSE
PR146 *0_4
PC142 0_4
PR150 0_4
PC143 0_4
CSREFA [40]

PR132 *1K/F_4
PC134 *100P/50V_4
PR133 *0_4
PC135 *1000P/50V_4
CSCOMPA
PR137 0_4
DROOPA
PR138 *4.7K/F_4
CSREFA

CSREFA
PC141 *47n/10V_4
CSP1A
PR148 *6.98K/F_4
SWN1A

TSENSEA
PR149 *8.25K/F_4
PR151 *100K_4 NTC
Place close with V_GT hot spot

+1.05V_VTT
PR154 75/F_4
[2,32] H_PROCHOT#
+3V
PR155 10K/F_4
[6] IMVP_PWRGD
+3V
PR156 10K/F_4
GFX_HWPG
PR152 *0_4/S
6132AGND
PC145 0_4
6132AGND
PU9 NCP81018B
PR157 *25.5K/F_4
6132_PWMA [40]

Alert# signal must be routed between the Clock and Data lines to reduce the cross talk

[32] GFX_HWPG
[32] VRON
[4] VR_SVID_DATA
[4] VR_SVID_ALERT#
[4] VR_SVID_CLK

+5VS5
PR158 2_6
PC147 2.2U/6.3V_6
6132AGND
PR160 0_4
PR161 0_4/S
PR163 0_4/S
PR164 10K/F_4
PR165 95.3K/F_4
6132AGND
+VIN_VCC_CORE
PR169 1K/F_4
PC151 0.01U/50V_4
6132AGND

PR159 *2_6
PC146 *0.22U/25V_6
For 35W Dummy PR159 and PC146
PC148 0.22U/25V_6
PC150 2.2U/6.3V_6
PR172 2_6
PC152 0.22U/25V_6
BST_1
BST2_1
BST1_1

SW1A [40]
HG1A [40]
LG1A [40]
SW2 [40]
HG2 [40]
LG2 [40]
LG1 [40]
HG1 [40]
SW1 [40]

+1.05V_VTT
PR165 130/F_4
PR166 *75/F_4
PR167 54.9/F_4
PC149 0.1U/10V_4
SDIO
VR_SVID_ALERT#
SCLK

PR171 change to 0 R
PR170 0_4
Rd
PR171 0_4
Rd POP
For GT 1-phase operation
CSP1A
CSP2A

+5VS5
Rc
PR174 0_4
POP Rc for 2 phase CPU
CSP3

CPU	PR173
35W	41.2K
45W	73.2K

PR173 41.2K/F_4
6132_PWM
DRVEN [40]
PC155 0.1U/10V_4
6132AGND

[4] VSS_SENSE
[4] VCC_SENSE
PR175 0_4
PC153 1000P/50V_4
PR177 0_4

CSP1
PR176 6.98K/F_4
SWN1
PC154 47n/10V_4
CSREF
CSP2
PR179 6.98K/F_4
SWN2
PC157 47n/10V_4
CSREF
CSP3
PR183 *6.98K/F_4
SWN3
PC162 *47n/10V_4
CSREF
For 35W Dummy PR183 and PC162

CPU	PR178
35W	11.5K
45W	21K

PR178 11.5K/F_4
PC156 33P/50V_4
PR180 1K/F_4
PR181 49.9/F_4
PC158 100P/50V_4
PR182 4.3K/F_4
PC159 3300P/50V_4
B modify 4/15
CSREF [40]
PC161 1000P/50V_4
6132AGND
B modify 4/15

PR184 10/F_4
PC160 680P/50V_4
TRBST#
PR187 1.21K/F_4
PR188 24.9K/F_4
PC163 4700P/25V_4
6132AGND
B modify 4/15

PR189 22.6K/F_4
PC164 0.1U/10V_4
6132AGND 6132AGND
CSSUM
PC165 1200P/50V_4
PC166 470P/50V_4
PR194 75K/F_4
PR195 165K/F_4
PR190 140K_6
PR191 140K_6
PR196 *140K_6
SWN1 SWN1 [40]
SWN2 SWN2 [40]
SWN3 SWN3 [40]
For 35W Dummy PR196
B modify 4/15

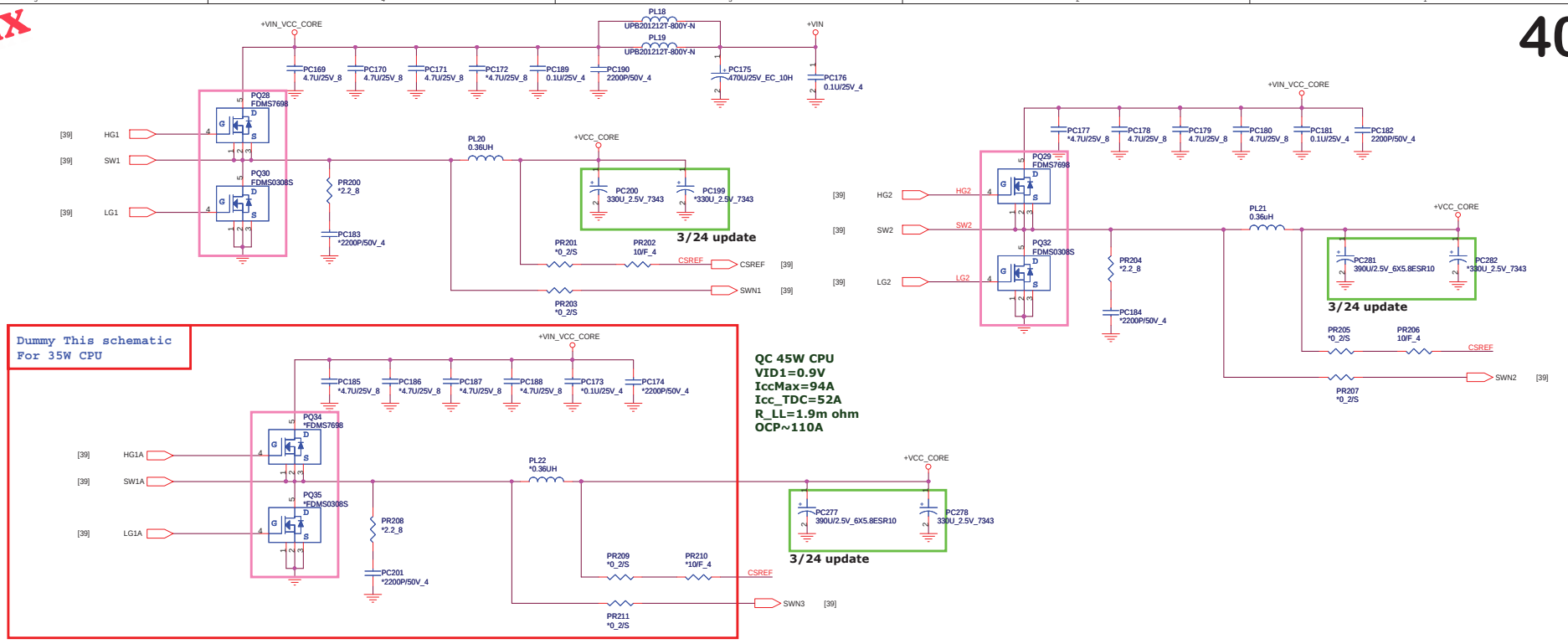
CPU	PR189
35W	22.6K
45W	23.7K

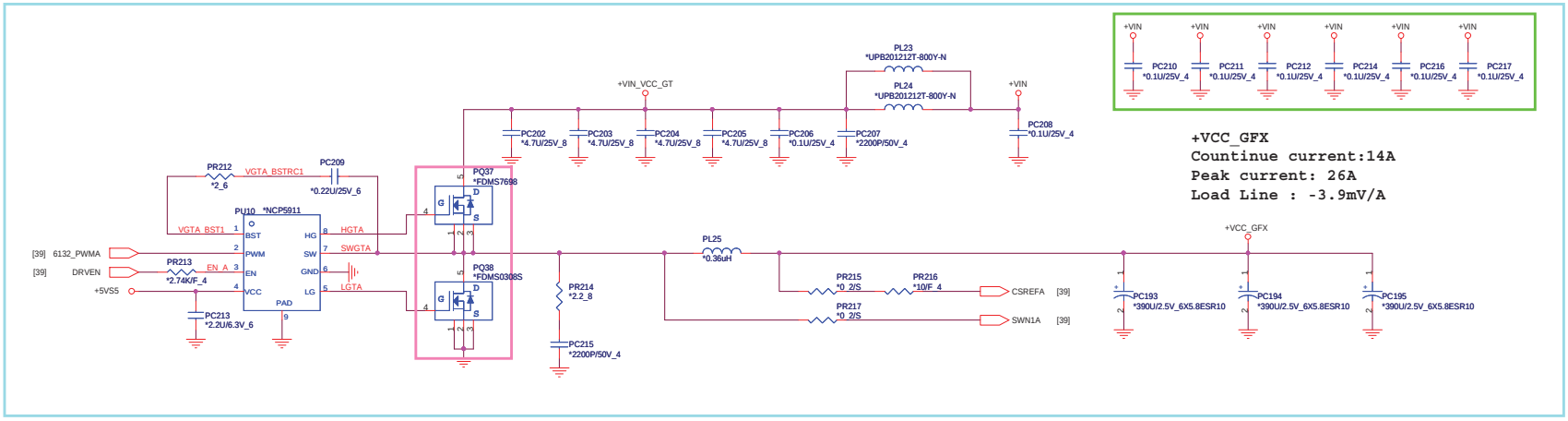
PR199 220K_6 NTC
Place close with VCORE Phase 1 Inductor

PR192 *1K/F_4
PC167 *820P/50V_4
PR193 *0_4
PC168 *1000P/50V_4
CSCOMP
PR197 0_4
DROOP
PR198 *4.7K/F_4
CSREF
B modify 4/15

TSENSE
PR185 8.25K/F_4
PR186 100K_4 NTC
Place close with VCORE hot spot

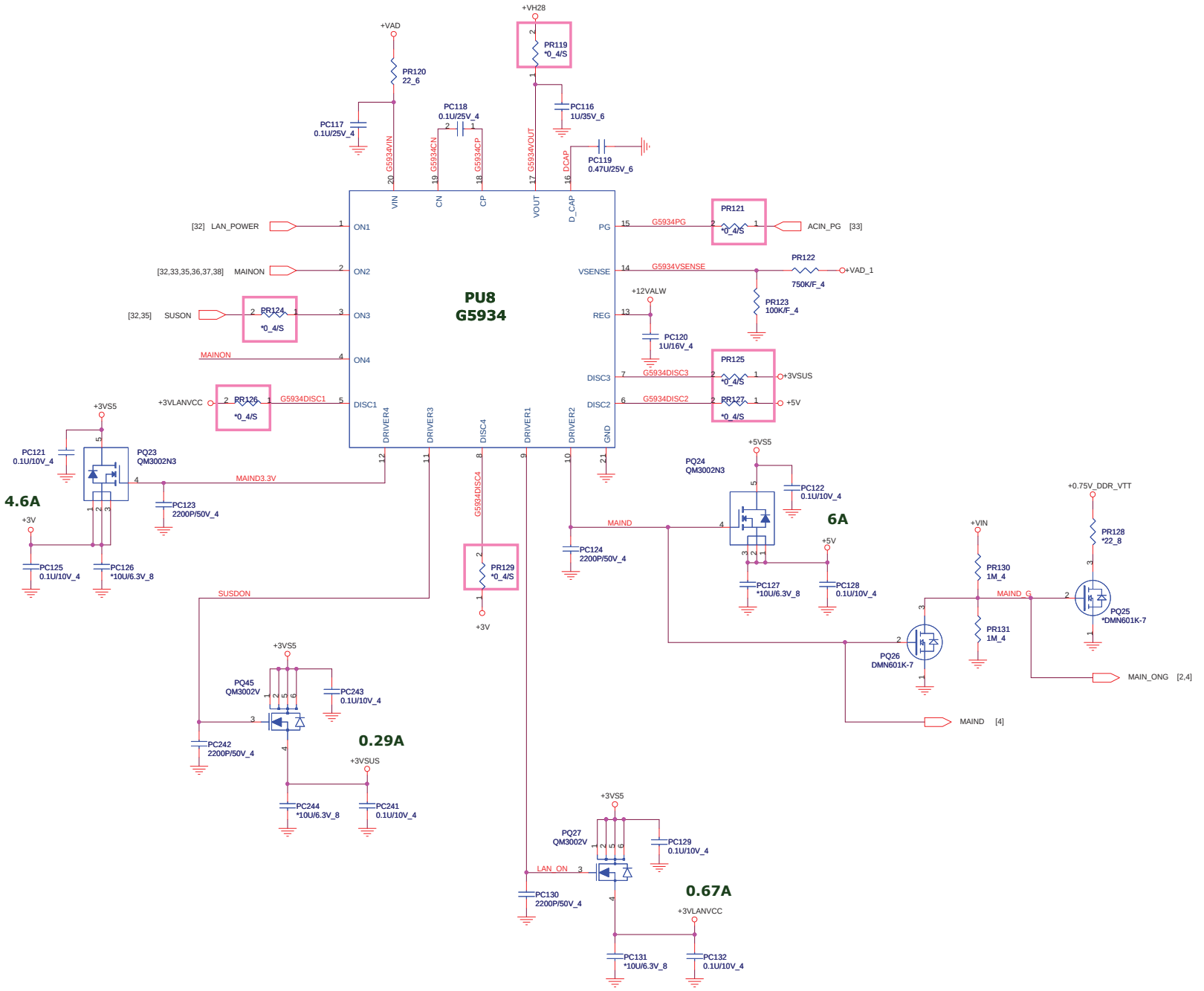
NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core1 (NCP6132)QC	Rev: 2A
Date: Thursday, May 19, 2011	Sheet 39 of 46	





sky blue color is disable GT setting

NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: C	Document Number: CPU Core2 (NCP5911)QC	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 40 of 46	



NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	2A

Date: Wednesday, May 18, 2011 | Sheet 41 of 47

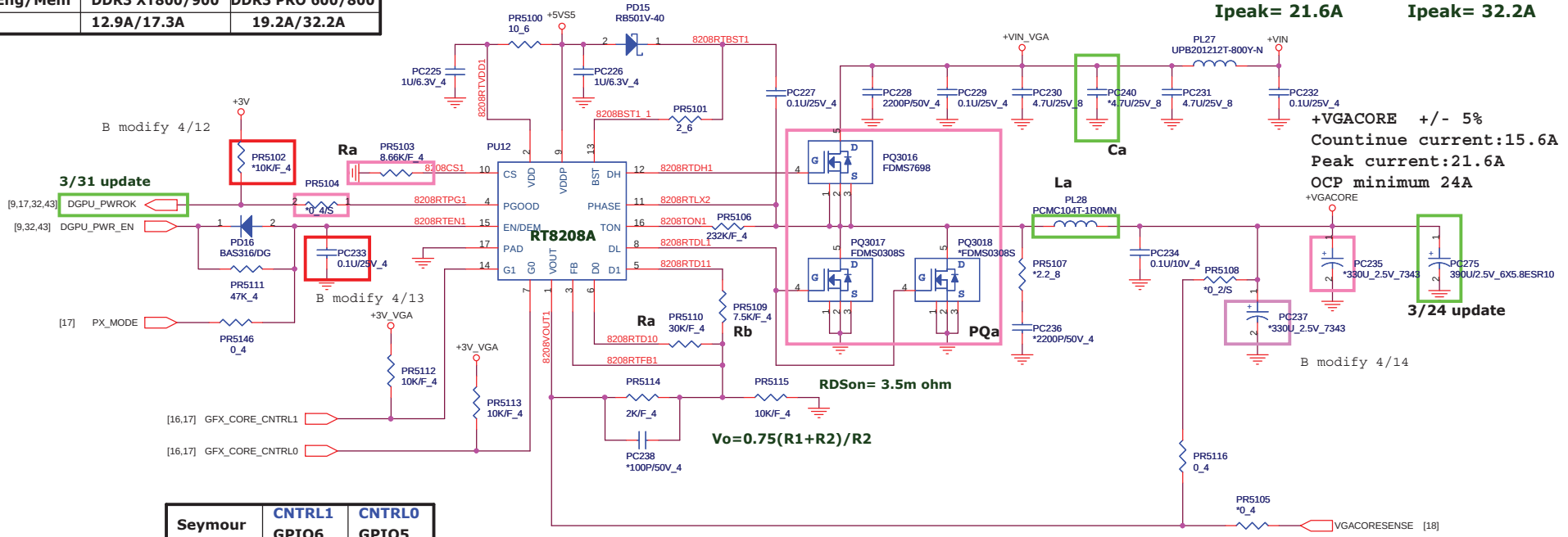
VGA Core

LG2_DIS only
VGA chip only Seymour

	Seymour (OCP 24A)	Whistler
Ca	PC240 X	V
Cb	PC235 PC237 X	V
PQa	PQ3018 X	V
La	1U/15A	0.45U25A
Ra	8.66K-ohm	8.66K-ohm
Eng/Mem	DDR3 XT800/900	DDR3 PRO 600/800
	12.9A/17.3A	19.2A/32.2A

Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Whistler
Irms= 19.2A
Ipeak= 32.2A



Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
0.95V	0	1	
1.1V	1	0	
1.15V	1	1	default

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
1.0V	0	1	Ra --> 15K-ohm
1.05V	1	0	Rb --> 10K-ohm
1.15V	1	1	

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41] +3V
+3V_GFX
[10,28,29,31,34,35,36,37,38,39,40,41,43] +5VSS
[17,18] +VGACORE
[22,26,29,33,34,35,36,37,40,41,43] +VIN

NB5

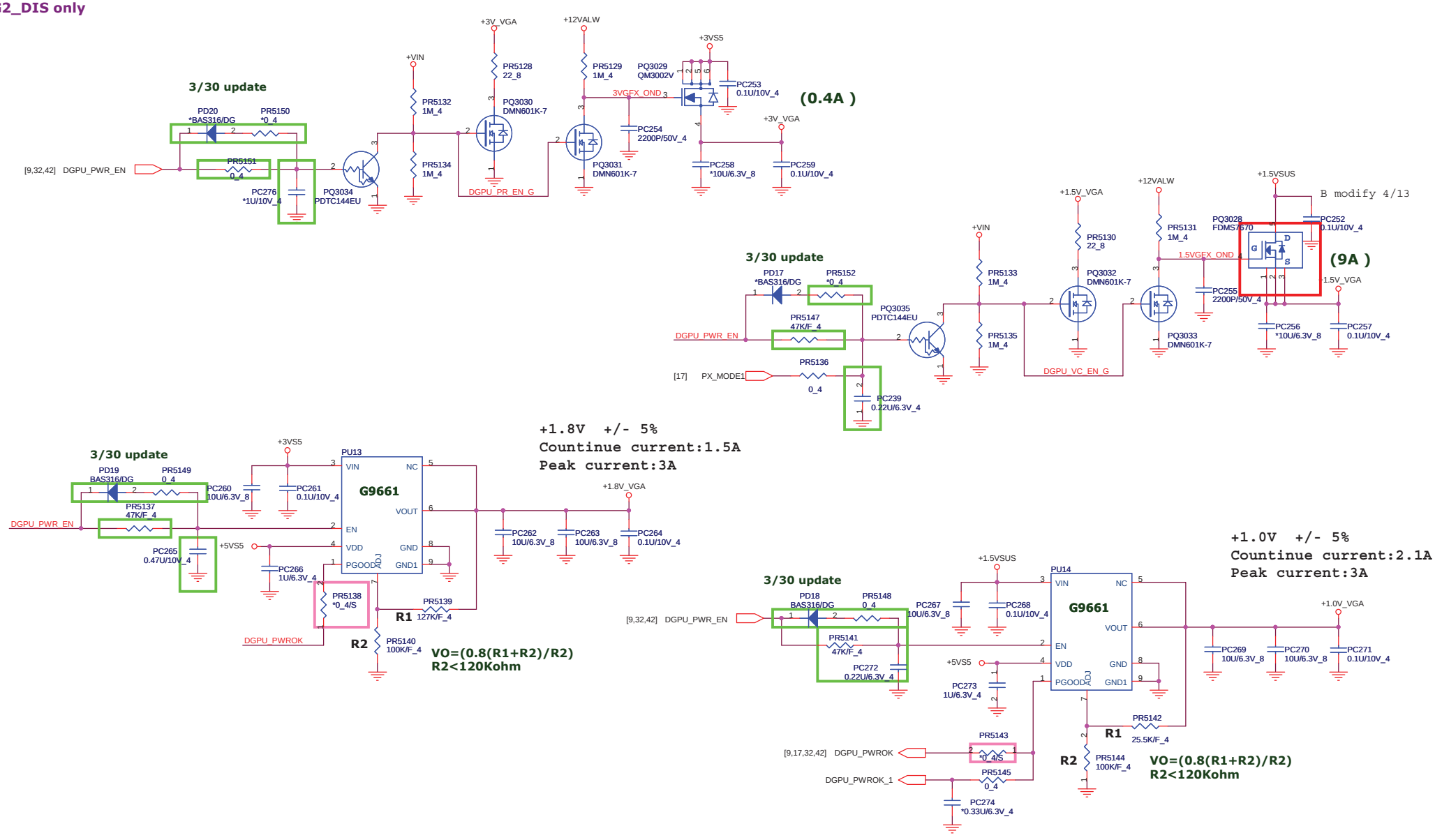
PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208)	2A

Date: Wednesday, May 18, 2011 | Sheet 42 of 46

VGA Core

LG2_DIS only



[2,4,12,13,35,36] +1.5VSUS
[2,6,7,8,9,10,27,29,32,34,37,38,41] +3VS5
[15,16] +3V_VGA
[14,16,18] +1.8V_VGA
[15,18,19,20] +1.5V_VGA
[14,16,17,18] +1.0V_VGA
[30,41] +12VALW
[22,26,29,33,34,35,36,37,40,41,42] +VIN

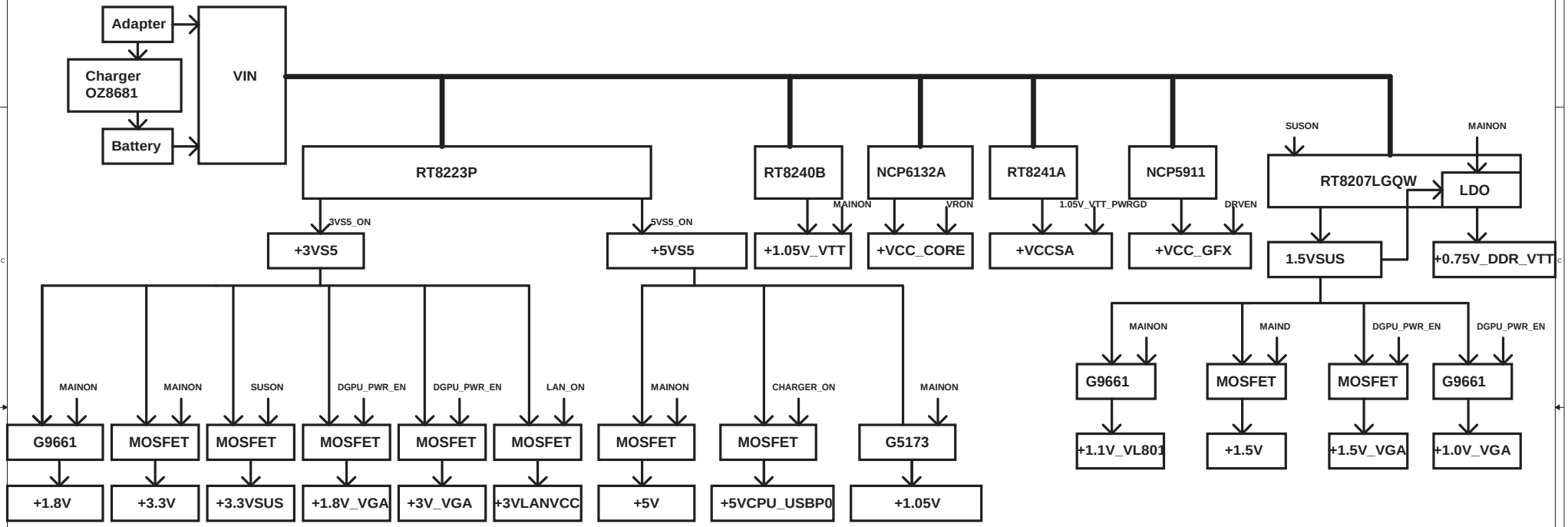
NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	2A

Date: Thursday, May 19, 2011 | Sheet 43 of 47

LG2/4
Power rail map

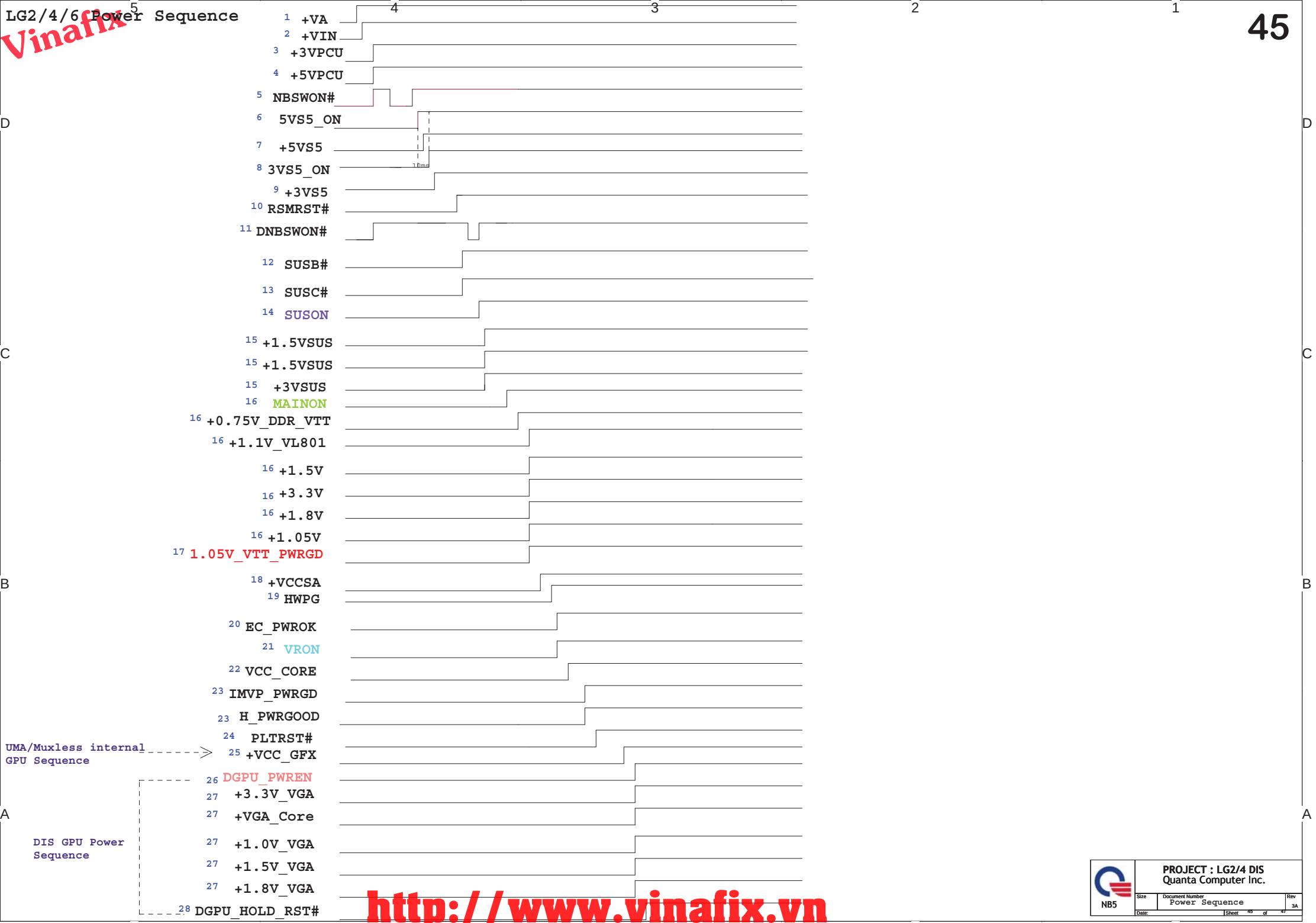


NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
	Power Block Diagram	3A

Date: Wednesday, May 18, 2011 | Sheet 44 of 47



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size | Document Number: Power Sequence | Rev: 3A

Date: | Sheet 45 of 47