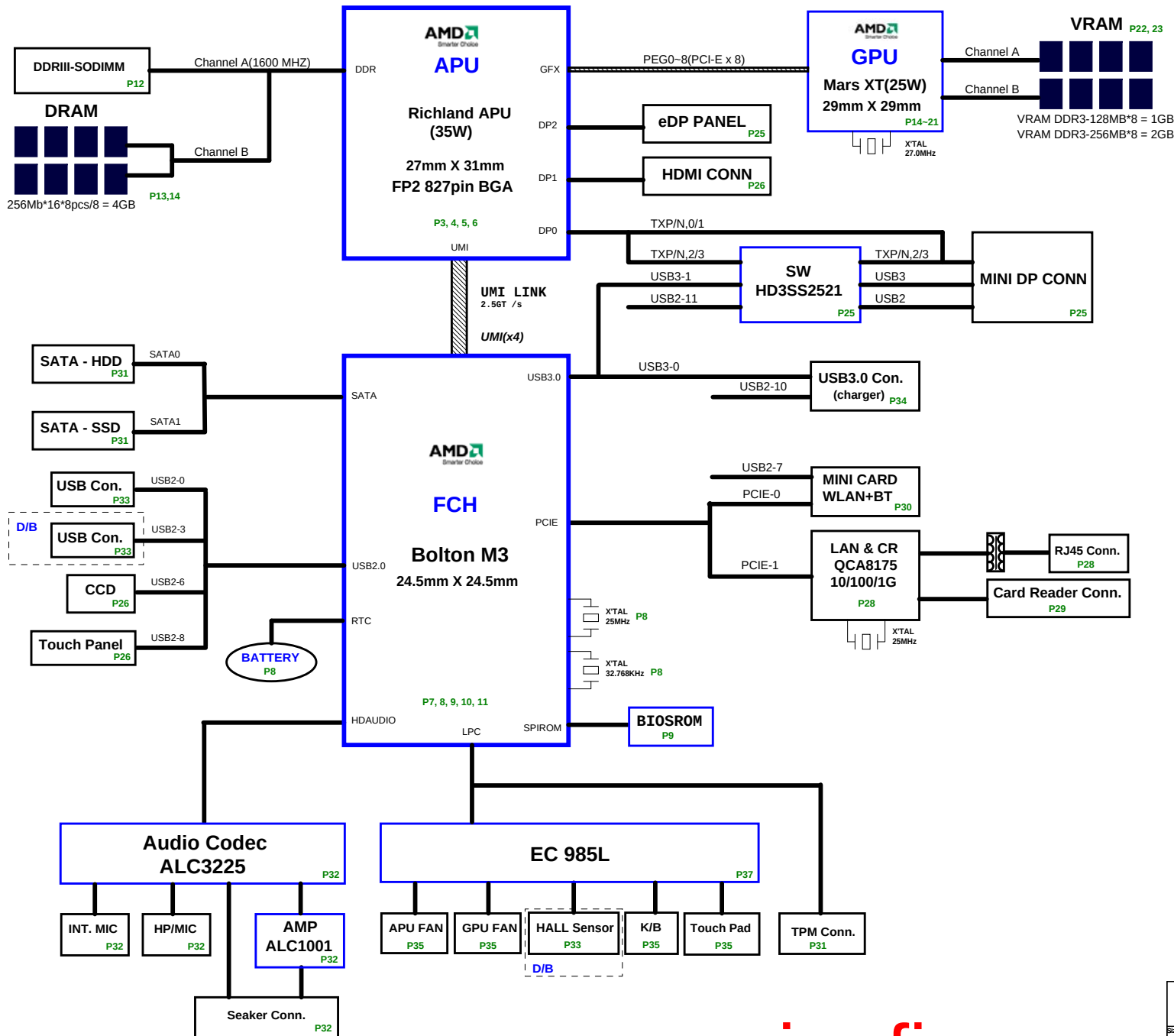


# ZRI/ZQI Block Diagram



## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 6 : GND
- LAYER 8 : BOT

|                             |     |
|-----------------------------|-----|
| Charger (BQ24737RGRR)       | P38 |
| SYSTEM 5V/3V (TPS51225RUKR) | P39 |
| +1.5VSUS(TPS51216)          | P40 |
| +1.2V(TPS51211) / +2.5V     | P41 |
| 1.1V_DUAL(TPS51211)         | P42 |
| +VDD_CORE (ISL62771)        | P43 |
| +VGPU_CORE(TPS51728)        | P44 |
| +PCIE_VDDC_GFX(TPS51211)    | P45 |
| +1.8V_GFX(TPS54318RTER)     | P46 |
| Discharge /Thermal          | P47 |

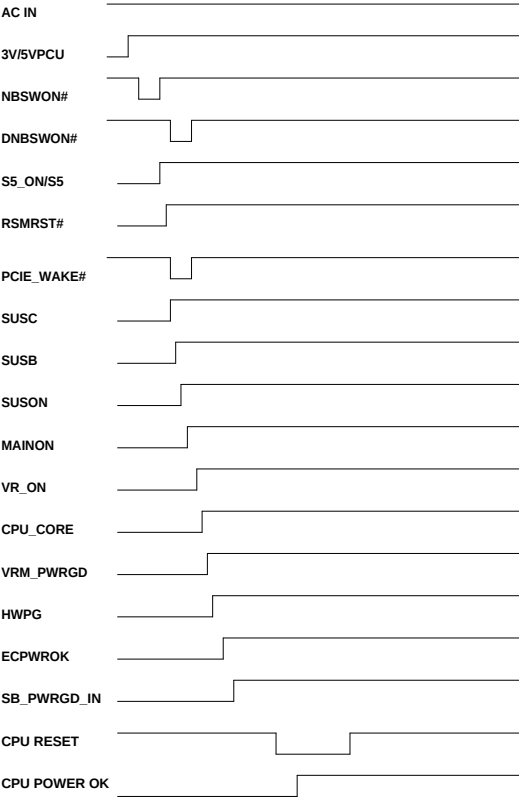
BOM Option

| ITEM | DESCRIPTION                                               | MARK      |
|------|-----------------------------------------------------------|-----------|
| 1    | LVDS Panel Sku                                            | LVDS@     |
| 2    | eDP Panel Sku                                             | eDP@      |
| 3    | VGA Sku                                                   | EV@       |
| 4    | VGA Thames Sku                                            | EV_T@     |
| 5    | VGA Mars Sku                                              | EV_M@     |
| 6    | VGA Sku for Thames and Mars stuff different value parts   | EV_SP@    |
| 7    | GPU 128bit Sku                                            | EV_128@   |
| 8    | GPU 128bit Sku of Special part value change               | EV_128SP@ |
| 9    | USB Charge Functions Sku                                  | CH@       |
| 10   | No USB Charge Functions Sku                               | NCH@      |
| 11   | USB3.0 Re-Driver Sku                                      | RD@       |
| 12   | No USB3.0 Re-Driver Sku                                   | NRD@      |
| 13   | Always connect functions Sku                              | AC@       |
| 14   | No Always connect functions Sku                           | NAC@      |
| 15   | Special part value change or modify for different BOM sku | SP@       |
| 16   | Key Board Back light Sku                                  | KBL@      |
| 17   | SSD Sku                                                   | SSD@      |
| 18   | Touch panel Sku                                           | TP@       |

Page 9 GPIO strap pin

| ITEM | DESCRIPTION          | MARK  |
|------|----------------------|-------|
| 1    | Synaptics touch pad  | SYNP@ |
| 2    | ELAN touch pad       | ELAN@ |
| 3    | For UMA Sku          | UMA@  |
| 4    | ELPIDA on board DRAM | ELP@  |
| 5    | HYNIX on board DRAM  | HYN@  |

Power Sequence



Hudson M3 SMBUS

| FCH SMBUS                                             | Pin NO.      | SMBUS Function Define |
|-------------------------------------------------------|--------------|-----------------------|
| PCLK_SMB<br>PDAT_SMB<br>(+3V)                         | AD26<br>AD25 | DDR / WLAN            |
| SCLK1<br>SDATA1<br>(+3V_S5)                           | T7<br>R7     | Touch Pad             |
| SMB_EC_CLK (SCLK2)<br>SMB_EC_DAT (SDATA2)<br>(+3V_S5) | H19<br>G19   | EC                    |
| SCLK3<br>SDATA3<br>(+3VPCU)                           | G22<br>G21   | Not used              |
| SCL4<br>SDATA4<br>(+3V_S5)                            | J19<br>K19   | Not used              |

EC SMBUS

| KBC SMBUS                            | Pin NO.    | SMBUS Function Define |
|--------------------------------------|------------|-----------------------|
| MBCLK<br>MBDATA<br>(+3VPCU)          | 70<br>69   | Battery, FCH          |
| APU_SIC_EC<br>APU_SID_EC<br>(+3V_S5) | 67<br>68   | APU                   |
| GPU_T_CLK<br>GPU_T_DATA<br>(+3V_GFX) | 119<br>120 | GPU                   |
| TPCLK<br>TPDATA<br>(+3V)             | 72<br>71   | Touch Pad             |

| EC         | FCH        | Device I2C_Device(S) |         |              |        |
|------------|------------|----------------------|---------|--------------|--------|
| I2Ce_1 (M) | I2Cf_2 (M) | Charger              | Battery |              | ALL/S5 |
| I2Ce_2 (M) |            | APU                  |         |              | ALL    |
| I2Ce_3 (M) |            |                      |         |              |        |
|            | I2Cf_3 (M) | APU                  |         |              | S5     |
|            | I2Cf_1 (M) |                      |         |              | S5     |
|            | I2Cf_0 (M) | DDR                  | WLAN/3G | Image Sensor | S0     |

EC will Conflict with FCH.  
Do not mount

PEG X 8

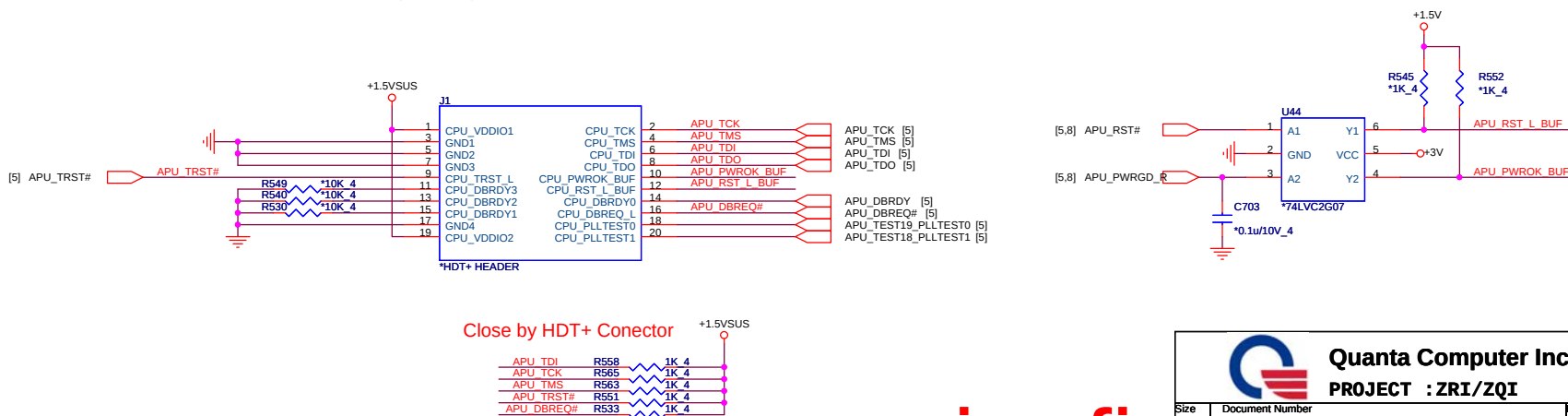
PEG X 8

FP2 only support PEG X 8

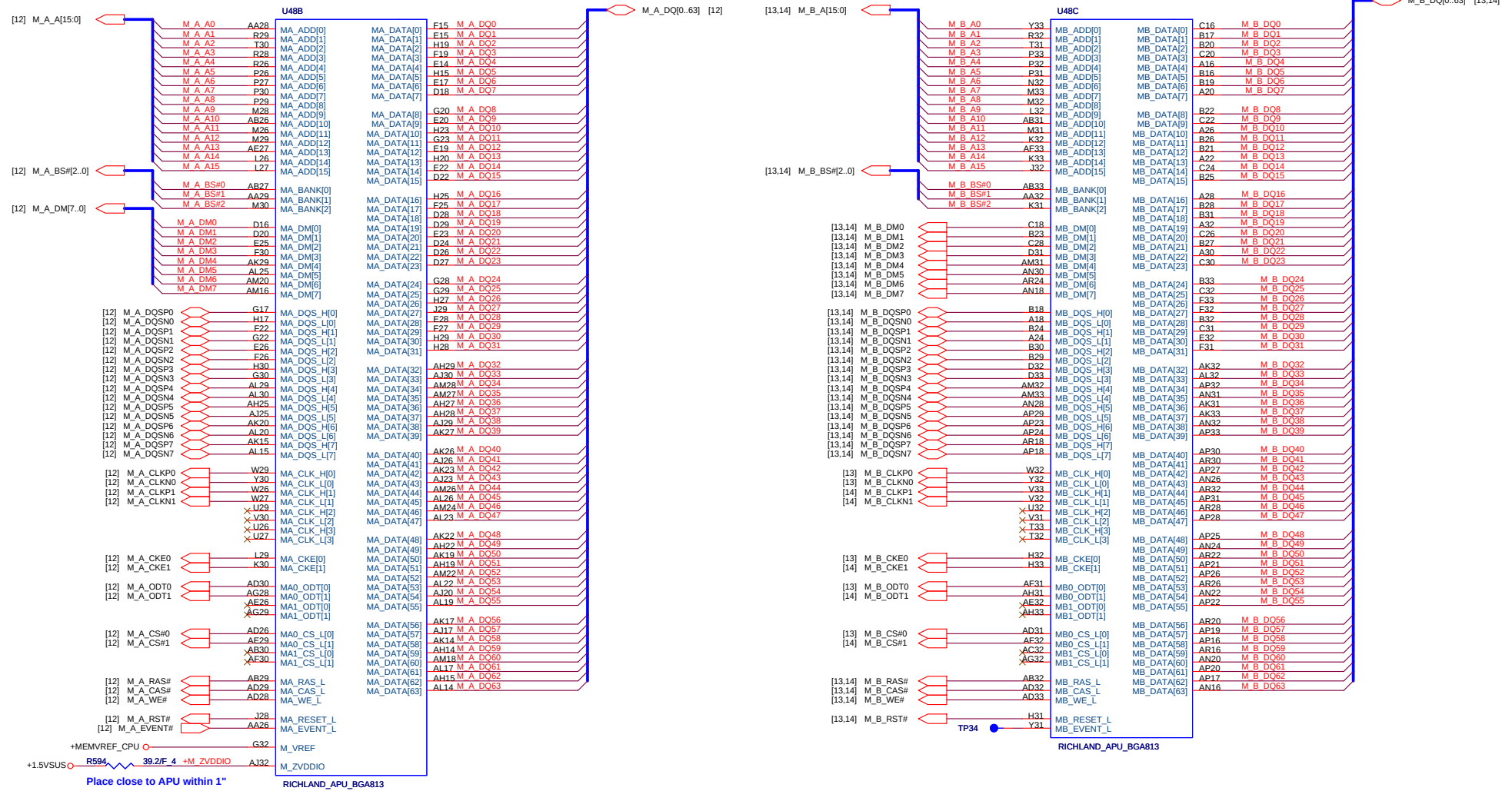
FP2 only support PEG X 8

|     |             |
|-----|-------------|
| A10 | AJ05757RT01 |
| A8  | AJ05557UT01 |
| A6  | AJ053578T01 |

## HDT+ Connector for Debug only



Soldermask openings for all bottom side vias/TPs under FS1



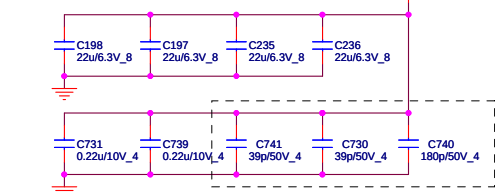
|     |             |
|-----|-------------|
| A10 | AJ05757RT01 |
| A8  | AJ05557UT01 |
| A6  | AJ053578T01 |



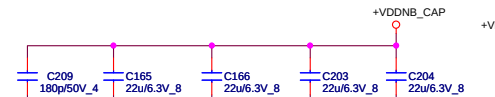
| Size  | Document Number           | Rev           |
|-------|---------------------------|---------------|
|       | APU 2/4(DDR3 MEM I/F)     | A1A           |
| Date: | Wednesday, April 24, 2013 | Sheet 4 of 50 |



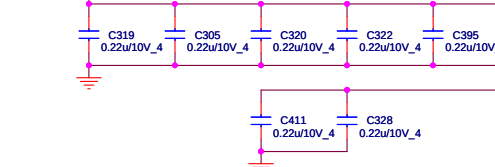
## 22A Maximum IDDNBSpike 33A



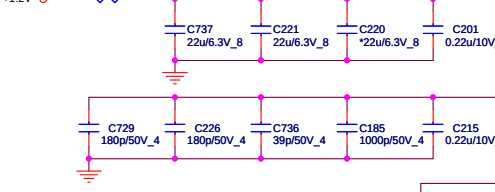
For EMI



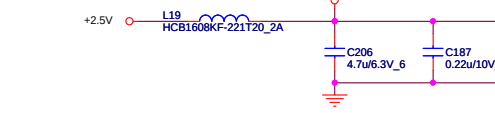
## 2.3A Up to DDR3-1333 @ 1.5V VDDIO



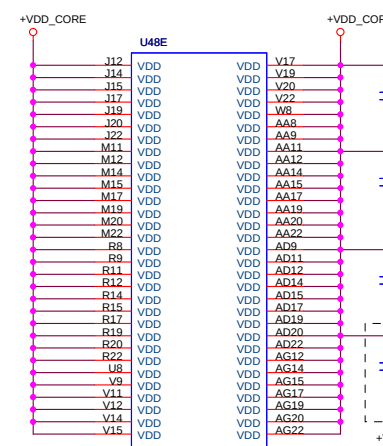
## VDDP = 3.5A



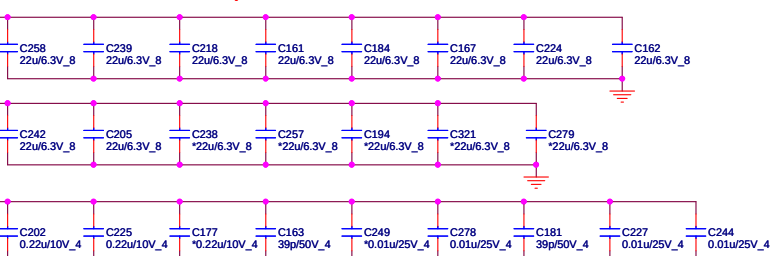
## VDDA = 0.75A



|     |             |
|-----|-------------|
| A10 | AJ05757RT01 |
| A8  | AJ05557UT01 |
| A6  | AJ053578T01 |



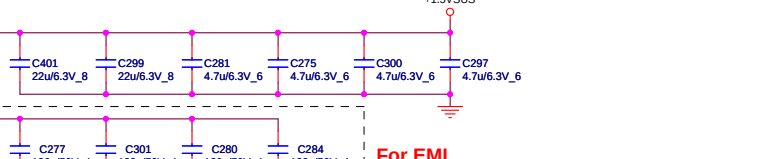
## 22A Maximum IDDSpike 35A



For EMI

## APU POWER TABLE

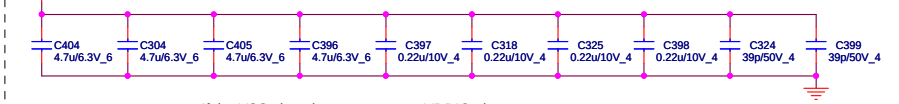
| PIN NAME | NET NAME    | VOLTAGE        |
|----------|-------------|----------------|
| VDD      | +VDD_CORE   | 1.0V ~ 1.3V    |
| VDDNB    | +VDDNB_CORE | 1.05V ~ 1.325V |
| VDDIO    | +1.5VSUS    | 1.5V           |
| VDDP     | +1.2V_VDDP  | +1.2V          |
| VDDR     | +1.2V_VDDR  | +1.2V          |
| VDDA     | +2.5V_VDDA  | +2.5V          |



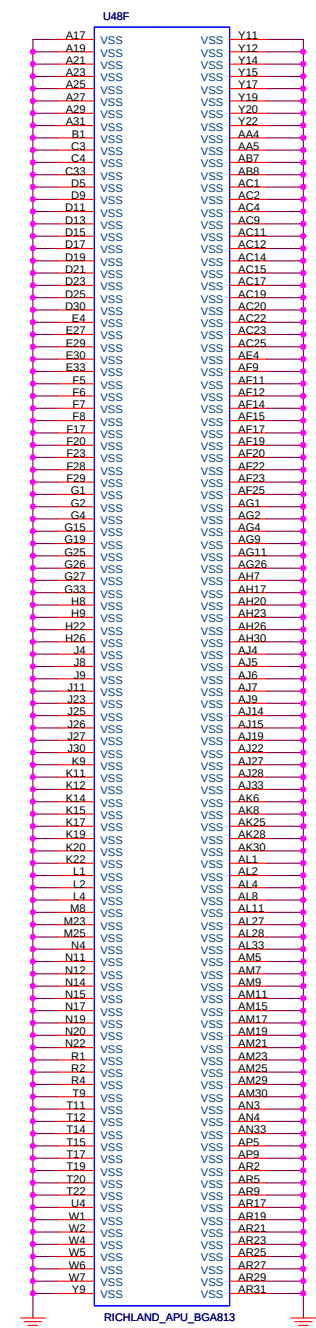
For EMI

## DECOUPLING between PROCESSOR and DIMMs

### Across VDDIO and VSS split



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows



**Quanta Computer Inc.**  
PROJECT : ZRI/ZQI

| Size  | Document Number           | Rev           |
|-------|---------------------------|---------------|
|       | APU 4/4(Power/GND)        | A1A           |
| Date: | Wednesday, April 24, 2013 | Sheet 6 of 50 |









SATA0 HDD

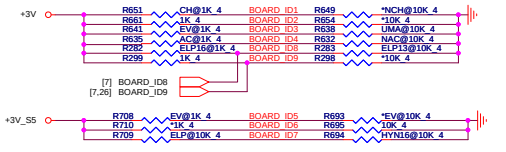
SATA1 SSD



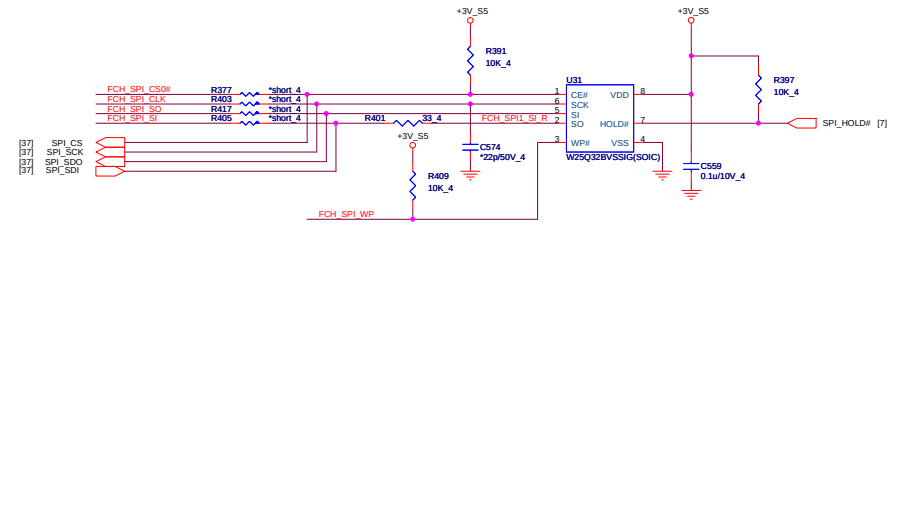
Integrated Clock Mode: SATA\_X1, SATA\_X2 leave unconnect.



Initial BIOS set internal pull down



## HUDSON-M3



## BOARD ID SETTING

| Board ID        | ID1 | ID2 | ID3 | ID4 | ID5 | ID9 |
|-----------------|-----|-----|-----|-----|-----|-----|
| USB Charge      | H   | L   |     |     |     |     |
| No USB Charge   |     |     |     |     |     |     |
| Reserved        |     | H   |     |     |     |     |
| VGA SKU         |     |     | H   |     |     |     |
| UMA SKU         |     |     | L   |     |     |     |
| AC              |     |     |     |     |     |     |
| No AC           |     |     |     | H   | L   |     |
| VRAM 2G         |     |     |     |     |     | H   |
| VRAM 4G         |     |     |     |     |     | L   |
| Non Touch Panel |     |     |     |     |     | H   |
| Touch Panel     |     |     |     |     |     | L   |

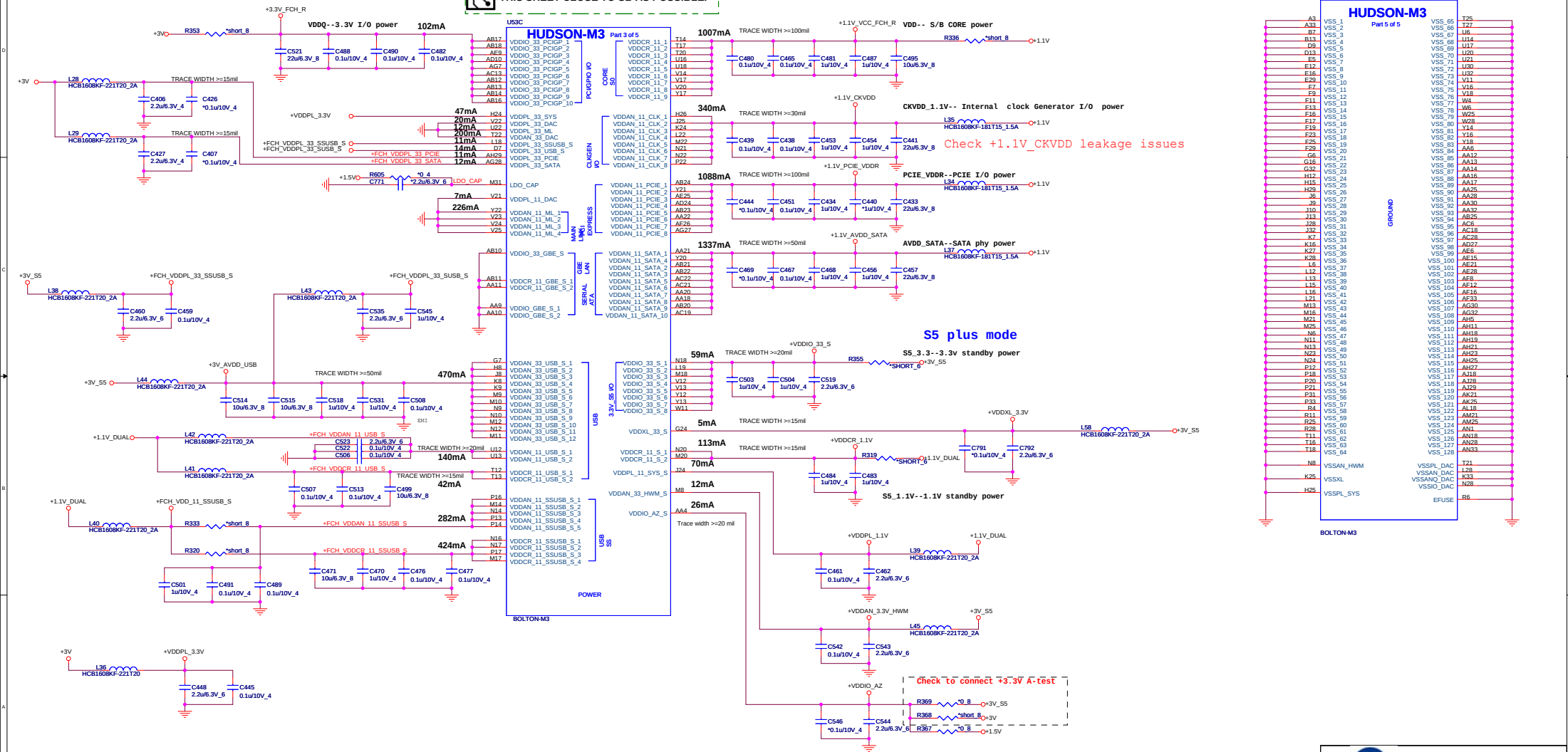
<= PD by cable

## OnBorad RAM SETTING

| ID6 | ID7 | ID8 |                                         |
|-----|-----|-----|-----------------------------------------|
| 0   | 0   | 1   | HYNIX DDR3L 1600 4GB H5TC4663AFR-PBA    |
| 0   | 1   | 0   | ELPIDA DDR3L 1333 4GB EDJ4216EB8G-DJ-F  |
| 0   | 1   | 1   | ELPIDA DDR3L 1600 4GB EDJ4216EF8G-GNL-F |
| 1   | 0   | 0   | Disable OnBorad RAM                     |



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



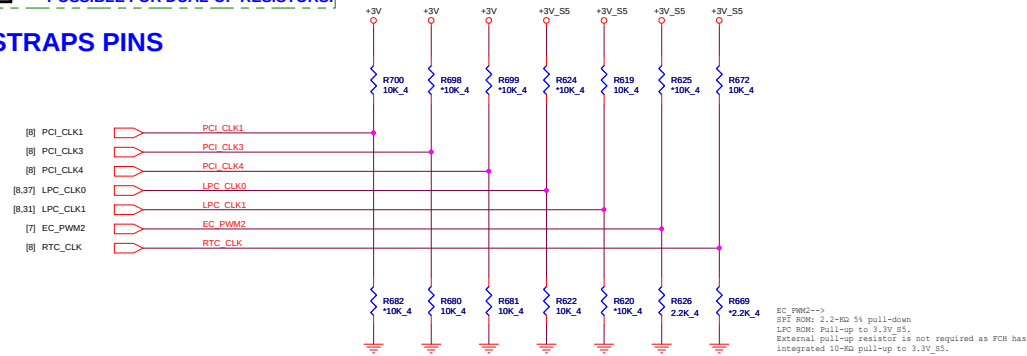
Quanta Computer Inc.  
PROJECT : ZR1/ZQ1

Size Document Number  
FCH 4/5(POWER)  
Date: Wednesday, April 24, 2013 Sheet 10 of 50



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## STRAPS PINS

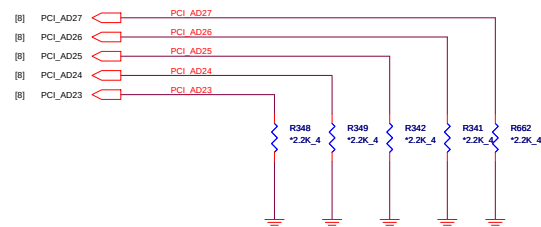


## REQUIRED STRAPS

|           | ***** | PCI_CLK1                   | PCI_CLK2 | PCI_CLK3                      | PCI_CLK4                        | LPC_CLK0                  | LPC_CLK1                     | EC_PWM2            | RTC_CLK                             |
|-----------|-------|----------------------------|----------|-------------------------------|---------------------------------|---------------------------|------------------------------|--------------------|-------------------------------------|
| PULL HIGH | ***** | ALLOW PCIE Gen2<br>DEFAULT | *****    | USE DEBUG STRAP               | non_Fusion<br>CLOCK MODE        | EC<br>ENABLED             | CLKGEN<br>ENABLED<br>DEFAULT | LPC ROM            | S5 PLUS MODE<br>DISABLED<br>DEFAULT |
| PULL LOW  | ***** | FORCE PCIE Gen1            | *****    | IGNORE DEBUG STRAP<br>DEFAULT | FUSION<br>CLOCK MODE<br>DEFAULT | EC<br>DISABLED<br>DEFAULT | CLKGEN<br>DISABLED           | SPI ROM<br>DEFAULT | S5 PLUS MODE<br>ENABLED             |

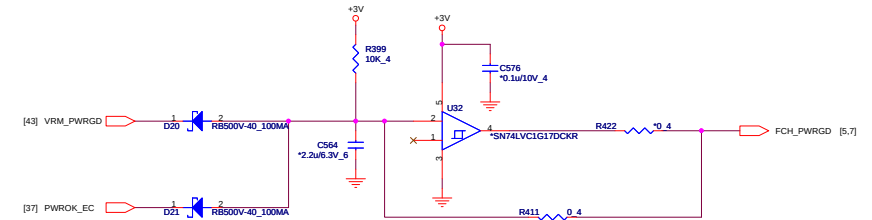
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



|           | PCI_AD27               | PCI_AD26                          | PCI_AD25              | PCI_AD24                              | PCI_AD23                           |
|-----------|------------------------|-----------------------------------|-----------------------|---------------------------------------|------------------------------------|
| PULL HIGH | USE PCI PLL<br>DEFAULT | DISABLE ILA<br>AUTORUN<br>DEFAULT | USE FC PLL<br>DEFAULT | USE DEFAULT<br>PCIE STRAPS<br>DEFAULT | DISABLE PCI<br>MEM BOOT<br>DEFAULT |
| PULL LOW  | BYPASS PCI PLL         | ENABLE ILA<br>AUTORUN             | BYPASS FC<br>PLL      | USE EEPROM<br>PCIE STRAPS             | ENABLE PCI<br>MEM BOOT             |

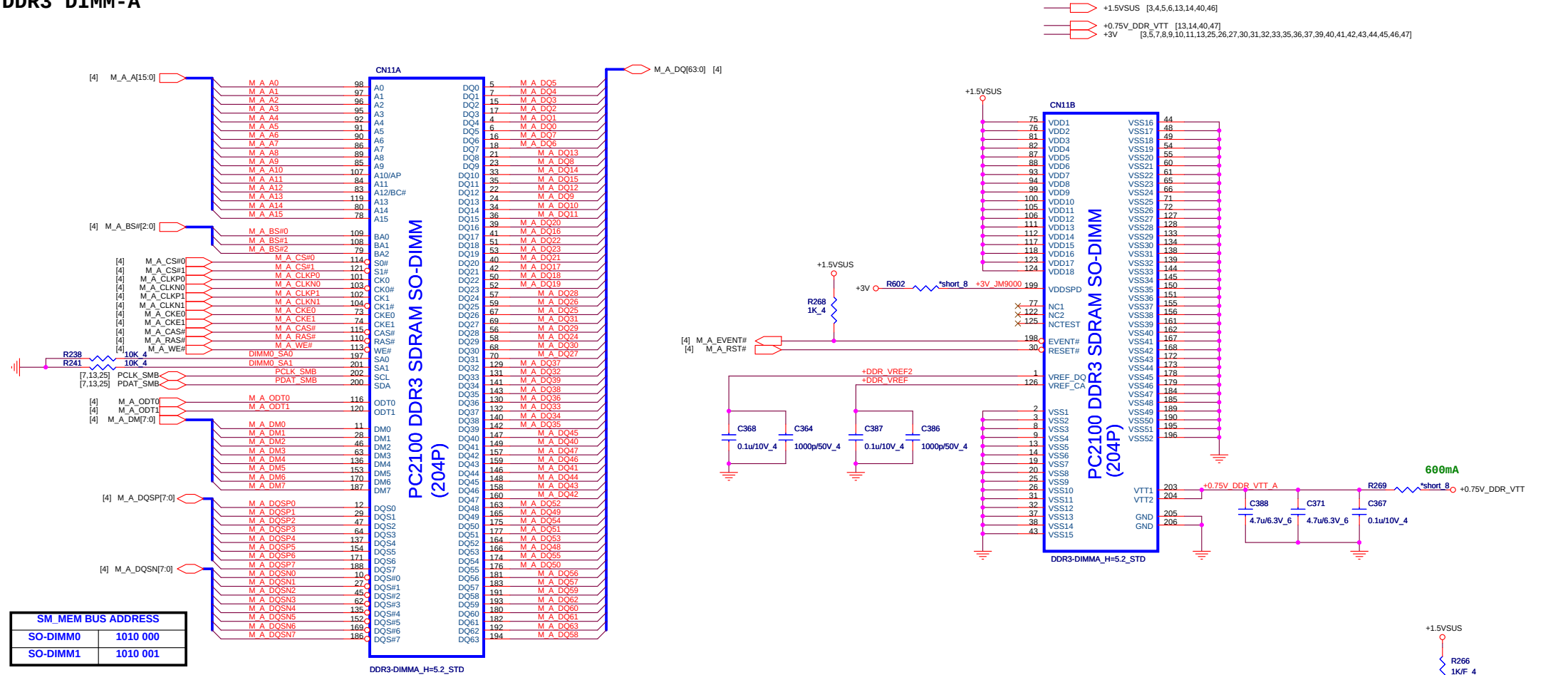
## FCH PWRGD CKT



Quanta Computer Inc.  
PROJECT : ZRI/ZQI

| Size  | Document Number           | Rev            |
|-------|---------------------------|----------------|
|       | FCH 5/5(STRAP & PWRGD)    | A1A            |
| Date: | Wednesday, April 24, 2013 | Sheet 11 of 50 |

DDR3 DIMM-A





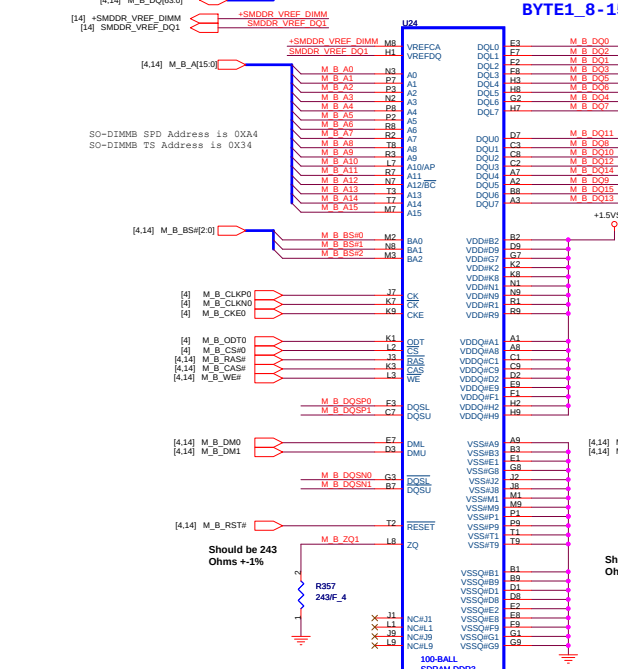
**Quanta Computer Inc.**  
**PROJECT : ZRI/ZQI**

| Size | Document Number       | Rev        |
|------|-----------------------|------------|
|      | <b>DDR3 SO-DIMM A</b> | <b>A1A</b> |

Date: Wednesday, April 24, 2013

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<DDR>

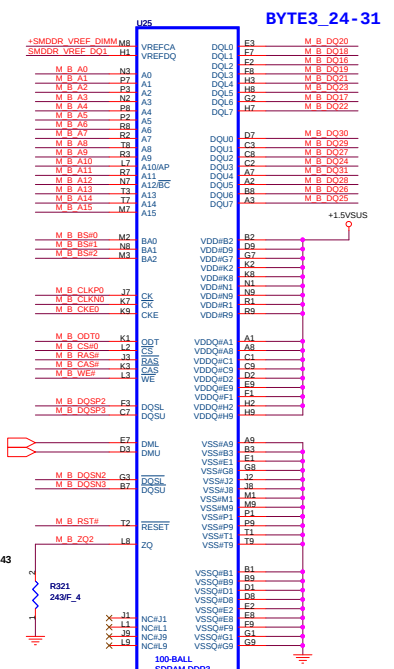


BYTE0\_0-7

BYTE1\_8-15

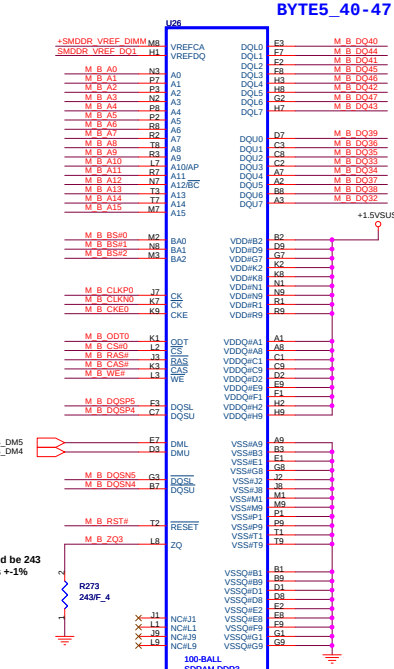
BYTE2\_16-23

BYTE3\_24-31



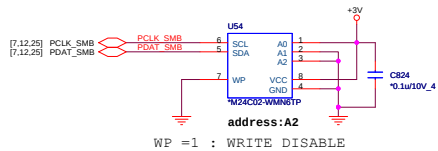
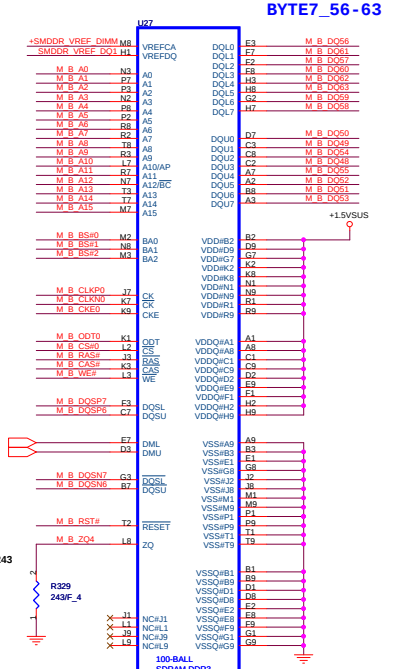
BYTE4\_32-39

BYTE5\_40-47

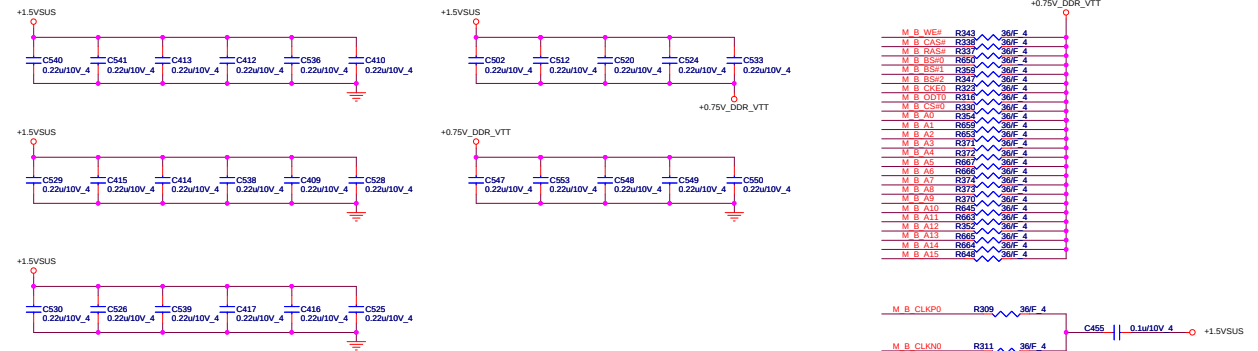


BYTE6\_48-55

BYTE7\_56-63



Place these Caps near Memory Down

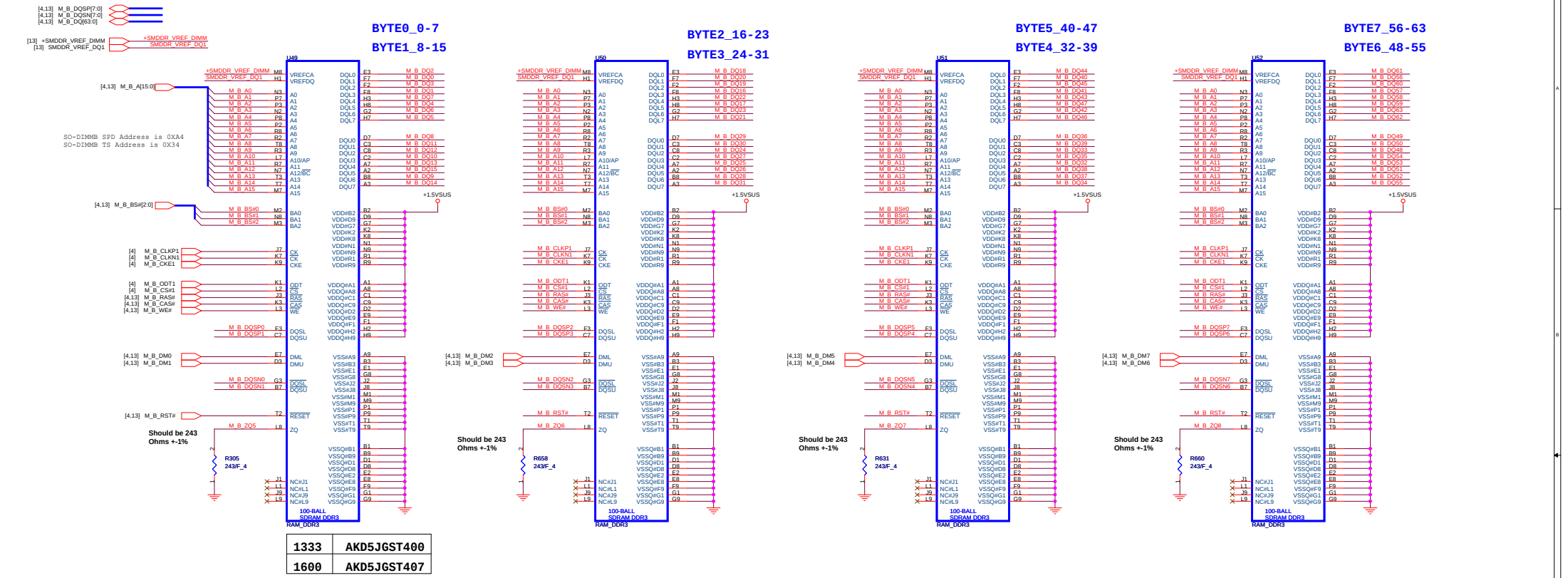


Quanta Computer Inc.  
PROJECT : ZRI/ZQI

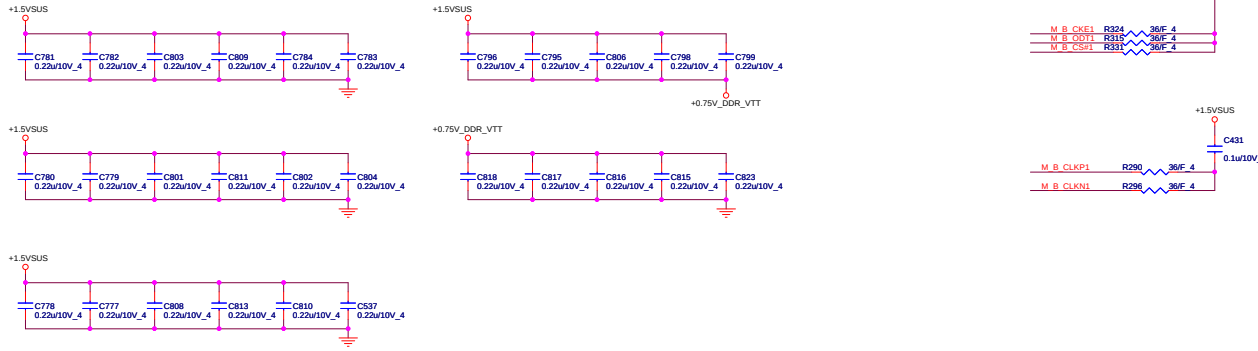
Size Document Number  
DDR3 MEMORY DOWNx16 B-1

Date: Wednesday, April 24, 2013 Sheet 13 of 30

<DDR>



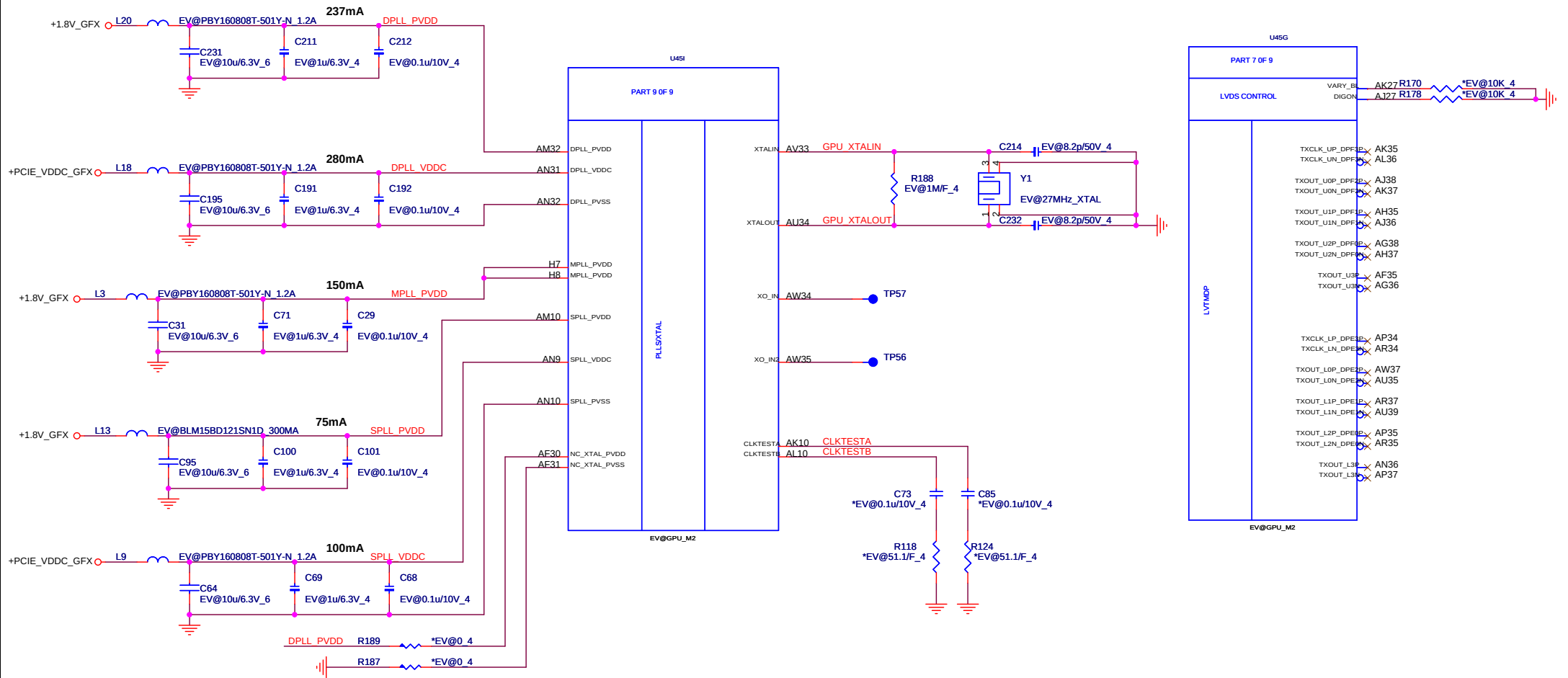
Place these Caps near Memory Down



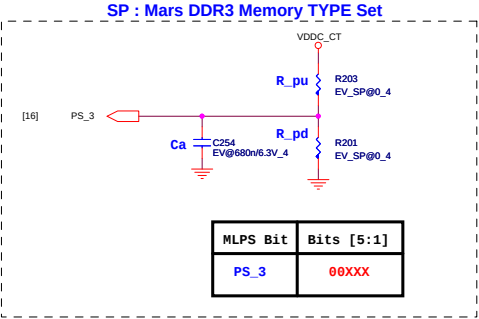








| Mars USE |                                 |                 |      |      |
|----------|---------------------------------|-----------------|------|------|
| Vendor   | Vendor P/N                      | STN B/S P/N     | Size | MLPS |
| Hynix    | H5TQ2G63DFR-11C<br>(128M*16)    | AKD5MGWTW17 * 8 | 2GB  | 000  |
|          | H5TC2G63FFR-11C<br>(128M*16)    | AKD5MZDTW05 * 8 | 2GB  | 001  |
|          |                                 |                 |      |      |
| Micron   | MT41K256M16HA-107G<br>(256M*16) | AKD5PGSTL05 * 8 | 4GB  | 011  |



## MLPS

| R_pu  | R_pd  | Bits [3:1] |
|-------|-------|------------|
| NC    | 4.75K | D 000      |
| 8.45K | 2K    | F 001      |
| 4.53K | 2K    | B 010      |
| 6.98K | 4.99K | 011        |
| 4.53K | 4.99K | 100        |
| 3.24K | 5.62K | 101        |
| 3.4K  | 1M    | 110        |
| 4.75K | NC    | 111        |

| Ra    | P/N         |
|-------|-------------|
| 2K    | CS22002FB19 |
| 3.24K | CS23242FB09 |
| 3.4K  | CS23402FB08 |
| 4.53K | CS24532FB08 |
| 4.75K | CS24752FB12 |
| 4.99K | CS24992FB26 |
| 5.62K | CS25622FB18 |
| 6.98K | CS26982FB01 |
| 8.45K | CS28452FB12 |
| 1M    | CS51002FB11 |

| Ca    | Bits [5:4] | P/N         |
|-------|------------|-------------|
| 680nF | 00         | CH4681K9B00 |
| 82nF  | 01         | CH3823K1B00 |
| 10nF  | 10         | CH31003KB11 |
| NC    | 11         |             |

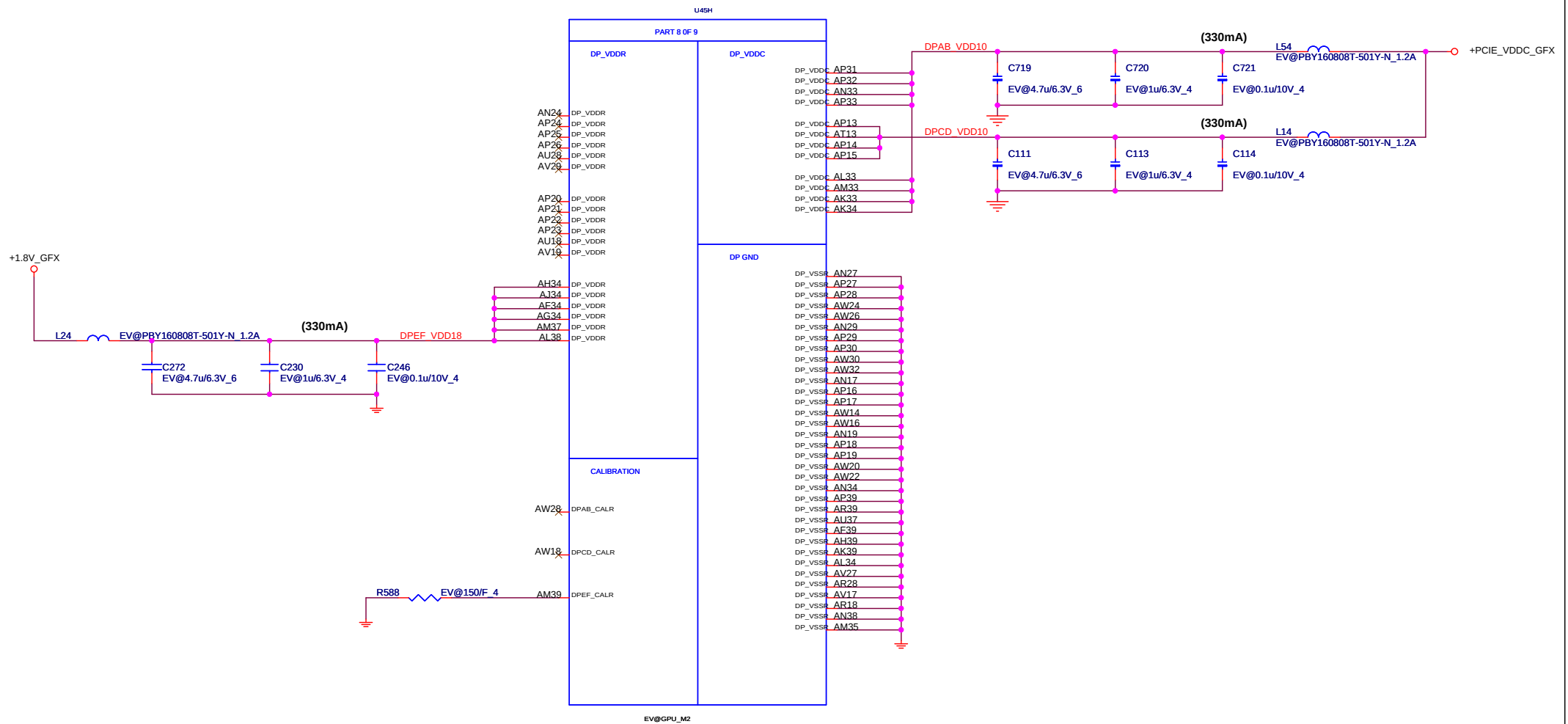
| CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS<br>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |                                |                                          |                                                                                                                                                                                                                                                                                                                                                         |                  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| STRAPS                                                                                                                                                                | MLPS                           | GPIO PIN                                 | DESCRIPTION OF DEFAULT SETTINGS                                                                                                                                                                                                                                                                                                                         | Default Setting  |
| MLPS_DISABLE                                                                                                                                                          | NA                             | GPIO_28_FDO                              | Enable MLPS, NA for Thames/Whistler/Seymour<br>0: Enable MLPS, disable GPIO PINSTRAP<br>1: Disable MLPS, enable GPIO PINSTRAP                                                                                                                                                                                                                           | X                |
| TX_PWR5_ENB                                                                                                                                                           | PS_1[4]                        | GPIO0                                    | Transmitter Power Savings Enable<br>0: 50% Tx output swing<br>1: Full Tx output swing                                                                                                                                                                                                                                                                   | X                |
| TX_DEEMPH_EN                                                                                                                                                          | PS_1[5]                        | GPIO1                                    | PCIe Transmitter De-emphasis Enable<br>0: Tx de-emphasis disabled<br>1: Tx de-emphasis enabled                                                                                                                                                                                                                                                          | X                |
| BIF_GEN3_ENA_A                                                                                                                                                        | PS_1[1]                        | GPIO2                                    | PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour)<br>0: GEN3 not supported at power-on<br>1: GEN3 supported at power-on                                                                                                                                                                                                                     | 1                |
| BIF_VGA_DIS                                                                                                                                                           | PS_2[4]                        | GPIO9                                    | VGA Control<br>0: VGA controller capacity enabled<br>1: VGA controller capacity disabled (for multi-GPU)                                                                                                                                                                                                                                                | 0                |
| ROMIDCFG[2:0]                                                                                                                                                         | PS_0[3..1]                     | GPIO[13:11]                              | Serial ROM type or Memory Aperture Size Select<br><br>If GPIO22 = 0, defines memory aperture size<br>If GPIO22 = 1, defines ROM type<br>100 - 512Kbit M25P05A (ST)<br>101 - 1Mbit M25P10A (ST)<br>101 - 2Mbit M25P20 (ST)<br>101 - 4Mbit M25P40 (ST)<br>101 - 8Mbit M25P80 (ST)<br>100 - 512Kbit Pm25LV512 (Chingis)<br>101 - 1Mbit Pm25LV010 (Chingis) | XXX              |
| BIOS_ROM_EN                                                                                                                                                           | PS_2[3]                        | GPIO22                                   | Enable external BIOS ROM device<br>0: Disabled<br>1: Enabled                                                                                                                                                                                                                                                                                            | X                |
| AUD[1]<br>AUD[0]                                                                                                                                                      | NA<br>NA                       | HSYNC<br>VSYNC                           | 00 - No audio function<br>01 - Audio for DP only<br>10 - Audio for DP and HDMI if dongle is detected<br>11 - Audio for both DP and HDMI<br>HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.                               | XX               |
| CEC_DIS                                                                                                                                                               | PS_0[4]                        | GENLK_VSYNC                              | Enable CEC function. Reserved for Thames/Whistler/Seymour<br>0: Disabled<br>1: Enabled                                                                                                                                                                                                                                                                  | X                |
| RESERVED<br>RESERVED<br>RESERVED<br>RESERVED                                                                                                                          | PS_1[3]<br>PS_1[2]<br>NA<br>NA | GENLK_CLK<br>GPIO8<br>GPIO21<br>GENERICC | NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET<br><br>Reserved<br>Reserved<br>Reserved<br>Reserved (for Thames/Whistler/Seymour only)                                                                                                        | 0<br>0<br>0<br>0 |
| AUD_PORT_CONN_PINSTRAP[2]<br>AUD_PORT_CONN_PINSTRAP[1]<br>AUD_PORT_CONN_PINSTRAP[0]                                                                                   | PS_3[5]<br>PS_3[4]<br>PS_0[5]  | NA<br>NA<br>NA                           | STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS<br>111 = 0 usable endpoints<br>110 = 1 usable endpoints<br>101 = 2 usable endpoints<br>100 = 3 usable endpoints<br>011 = 4 usable endpoints<br>010 = 5 usable endpoints<br>001 = 6 usable endpoints<br>000 = all endpoints are usable                                                    | XXX              |

## System Memory Aperture size

| GPIO9<br>BIOSROM |      | GPIO11<br>ROMIDCFG0 | GPIO12<br>ROMIDCFG1 | GPIO13<br>ROMIDCFG2 |
|------------------|------|---------------------|---------------------|---------------------|
| 0                | 128M | 0                   | 0                   | 0                   |
| 0                | 256M | 1                   | 0                   | 0                   |
| 0                | 64M  | 0                   | 1                   | 0                   |
| 0                | 32M  | 1                   | 1                   | 0                   |

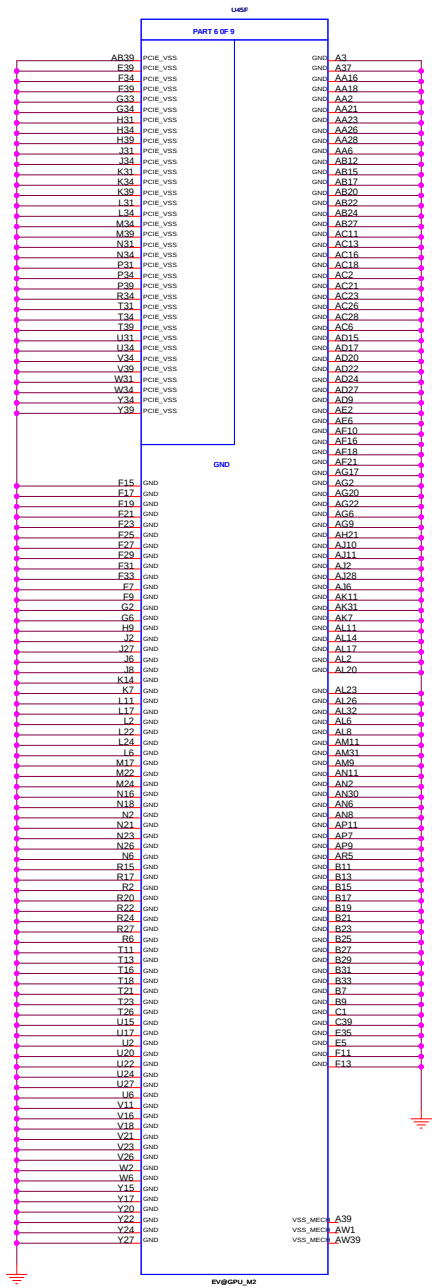


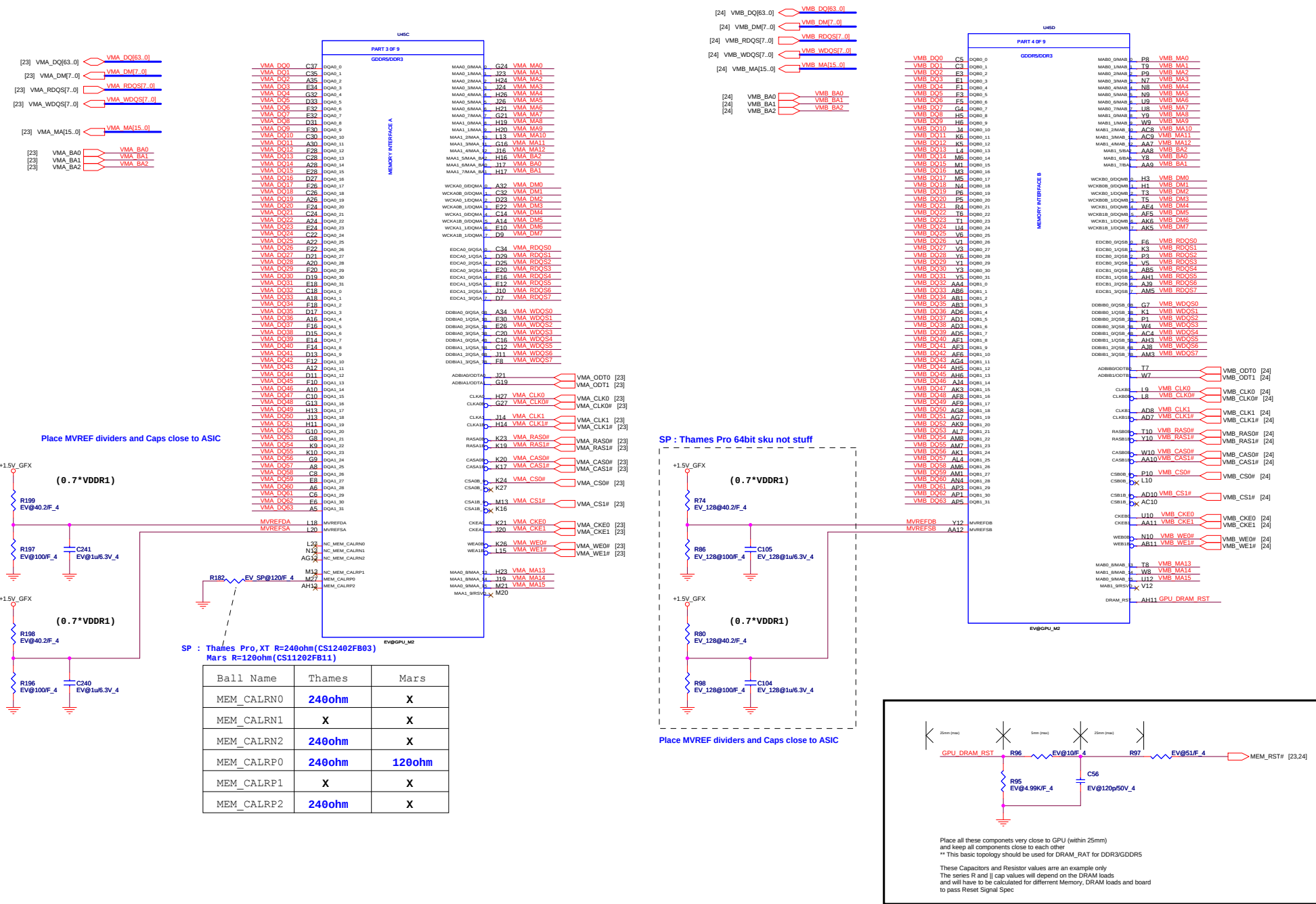




**Quanta Computer Inc.**  
**PROJECT : ZRI/ZQI**

| Size  | Document Number           | Rev            |
|-------|---------------------------|----------------|
|       | Thames_M2/ DP_Powers      | A1A            |
| Date: | Wednesday, April 24, 2013 | Sheet 20 of 50 |

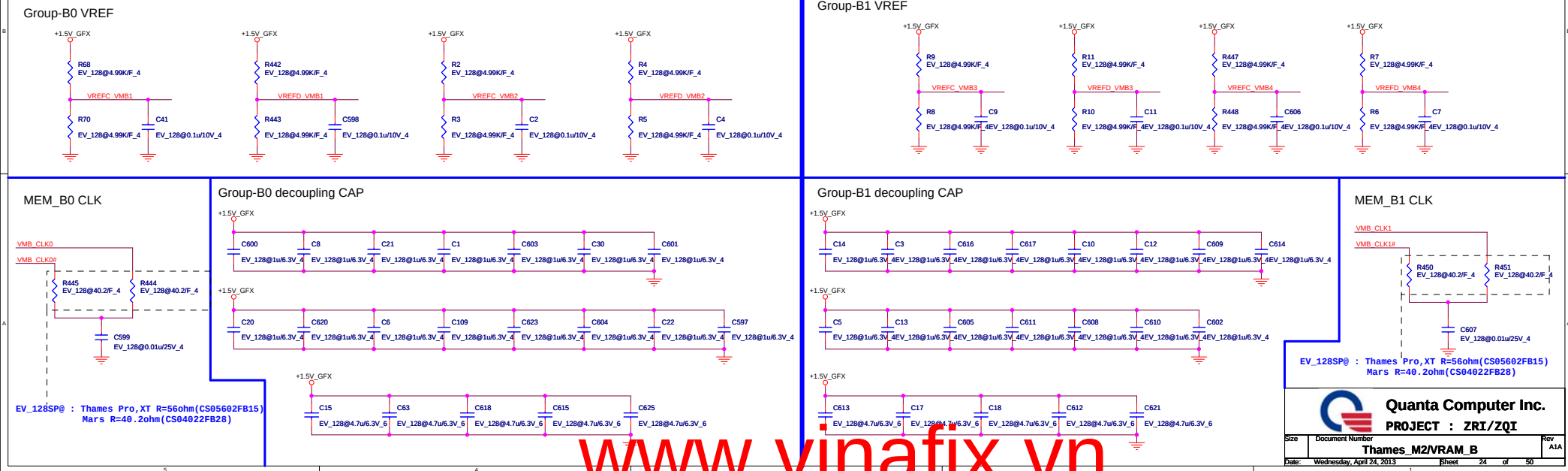
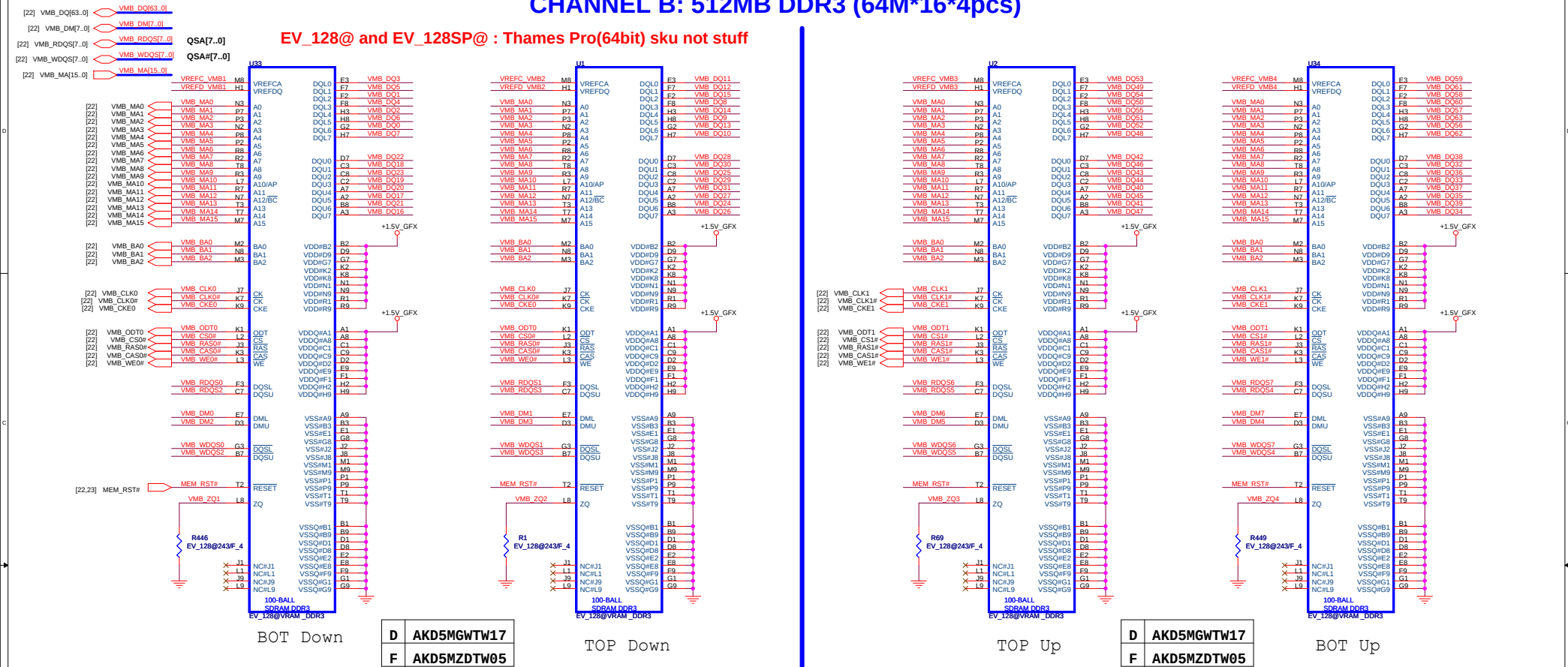




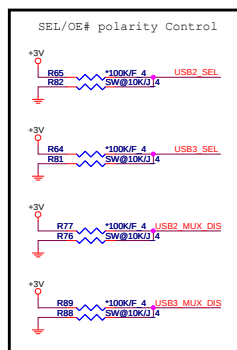
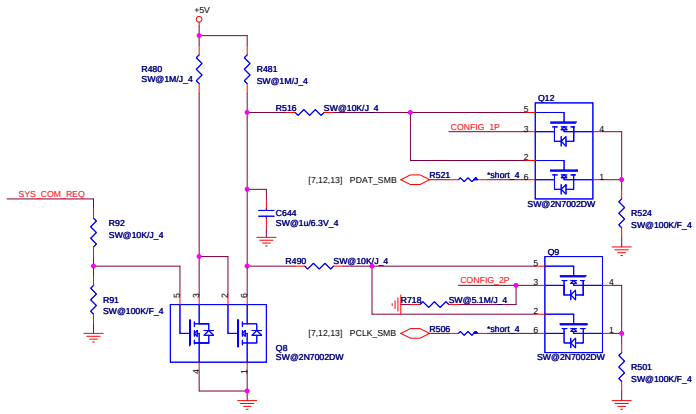




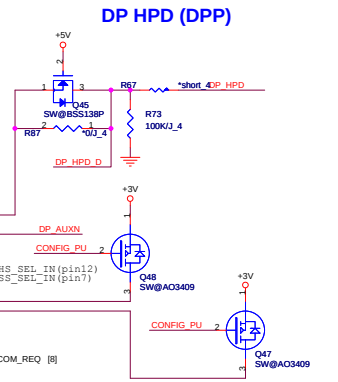
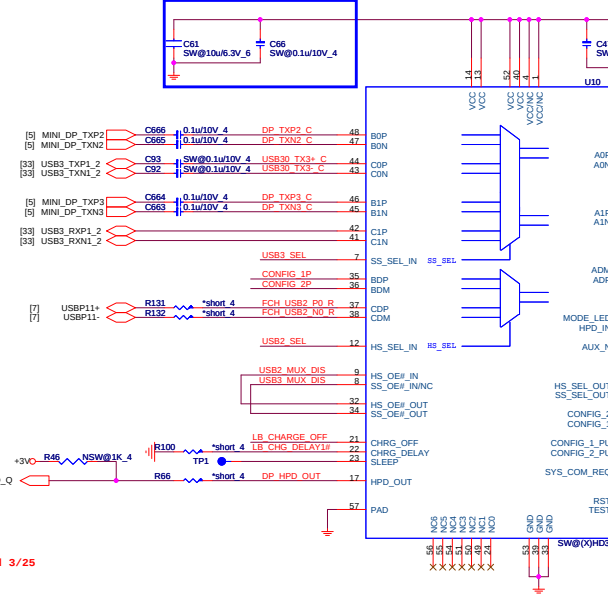
**CHANNEL B: 512MB DDR3 (64M\*16\*4pcs)**



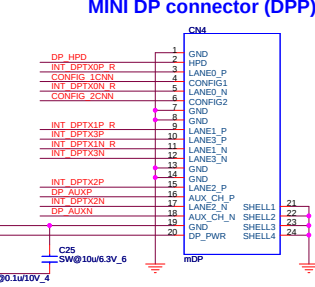
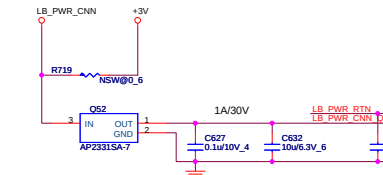
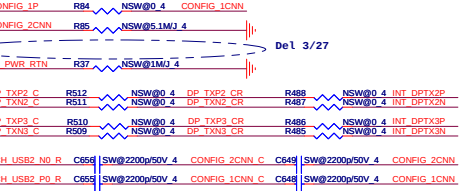
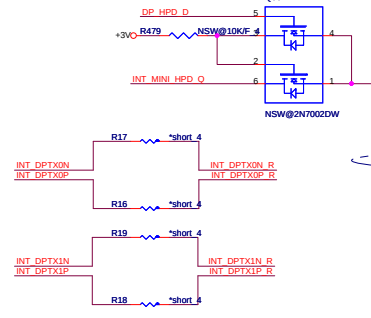
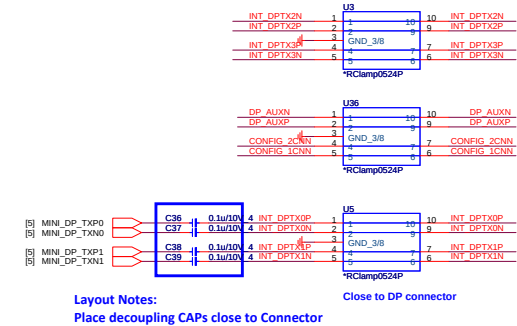
mini DP ML (DPP)



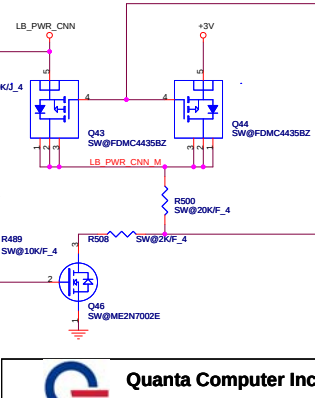
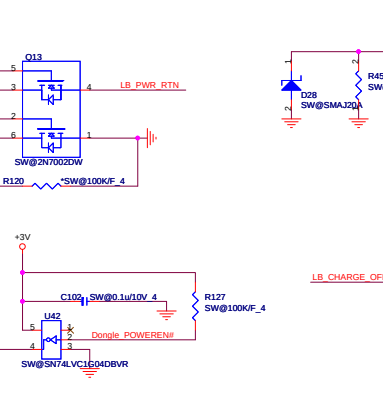
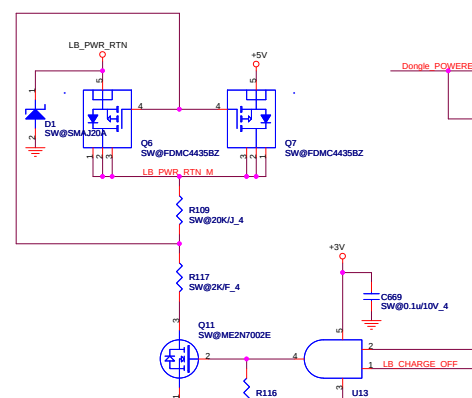
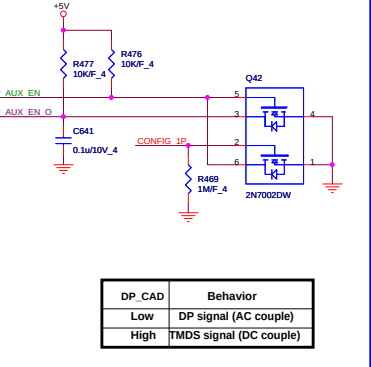
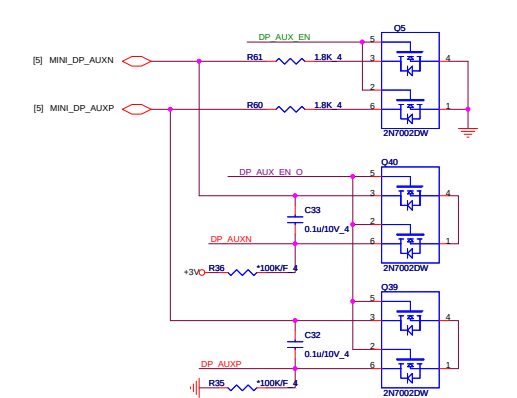
Layout Notes:  
Place near Pin13 and Pin14



ESD Protect (EMC)



mDP AUX (DPP)



| DP_CAD | Behavior                |
|--------|-------------------------|
| Low    | DP signal (AC couple)   |
| High   | TMDS signal (DC couple) |

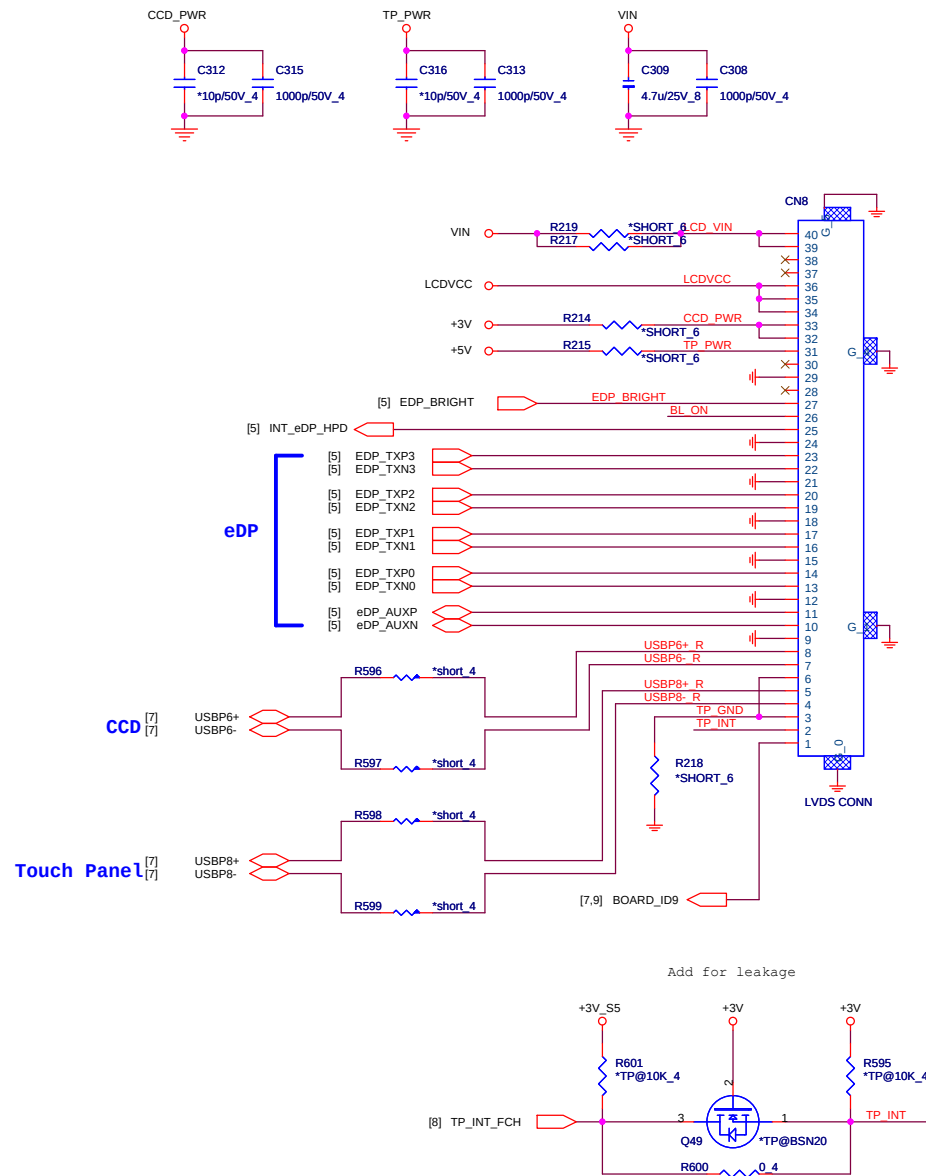


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PROJECT : ZRI/ZQI

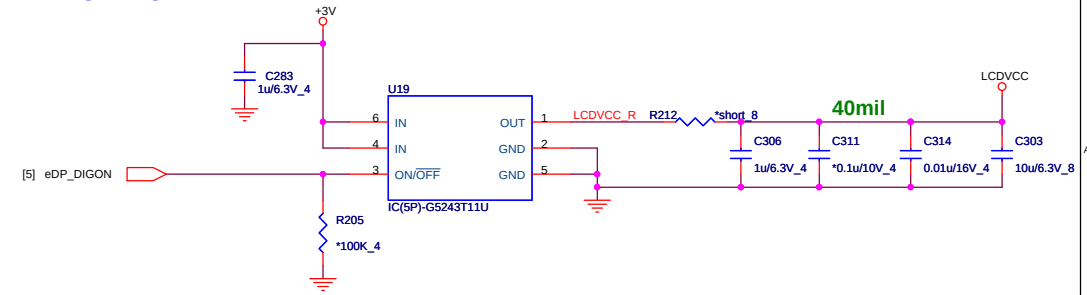
Site:   
Documen Number:   
Mini DP  
Date: Wednesday, April 22, 2013  
Sheet: 25 of 50

Rev: A1A

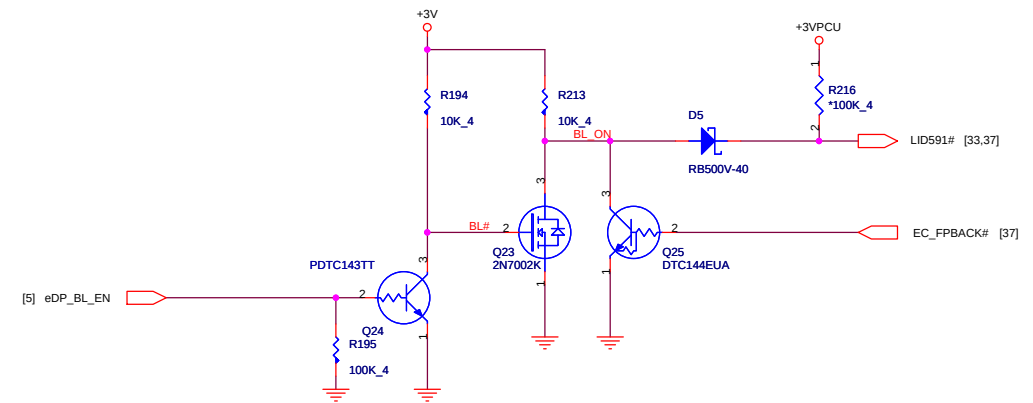
## eDP(LDS)



## LCD PW(LDS)

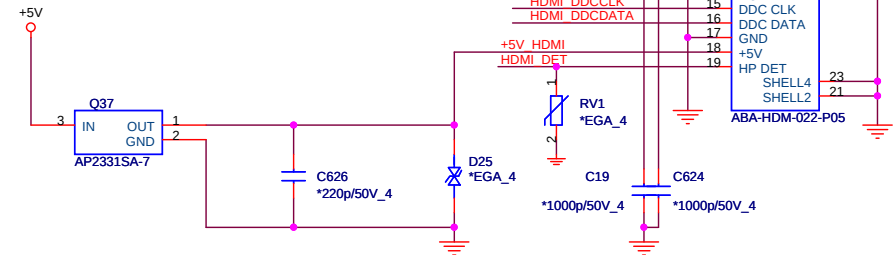
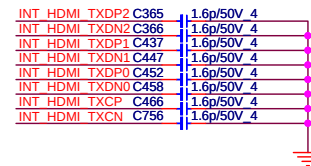
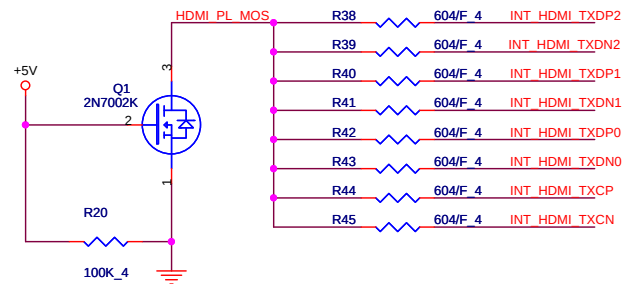
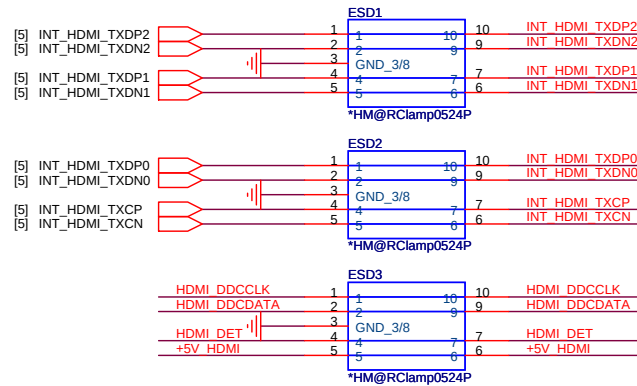


## Backlight Control(LDS)



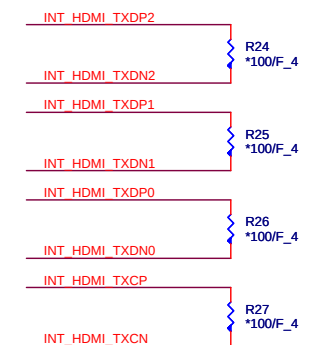
# HDMI

## ESD

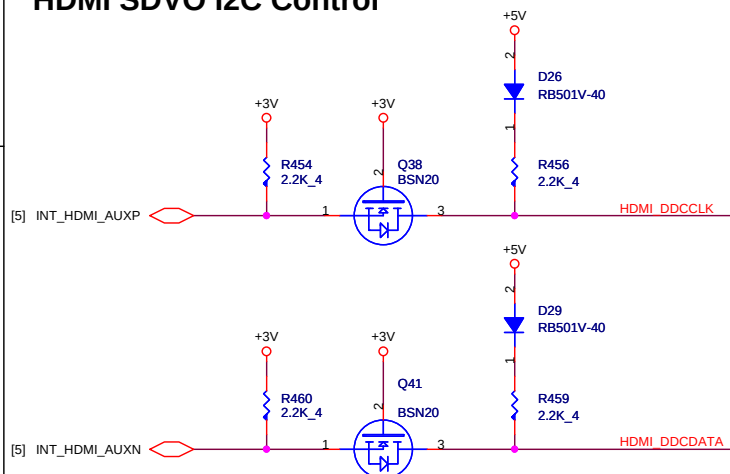


## EMI reserve for HDMI(EMC)

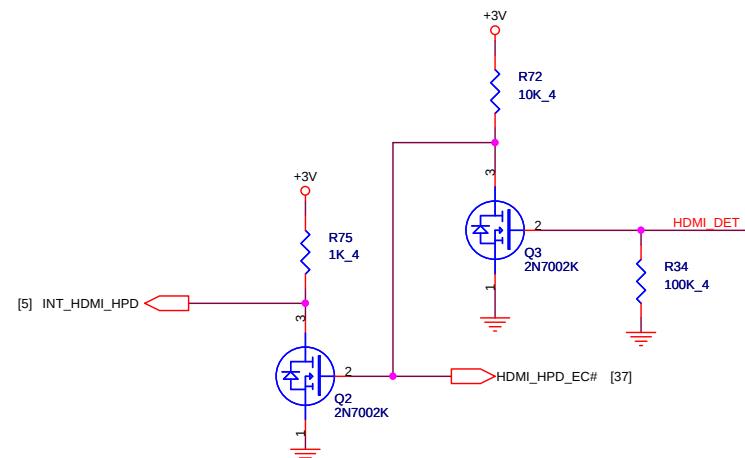
Close connector



## HDMI SDVO I2C Control



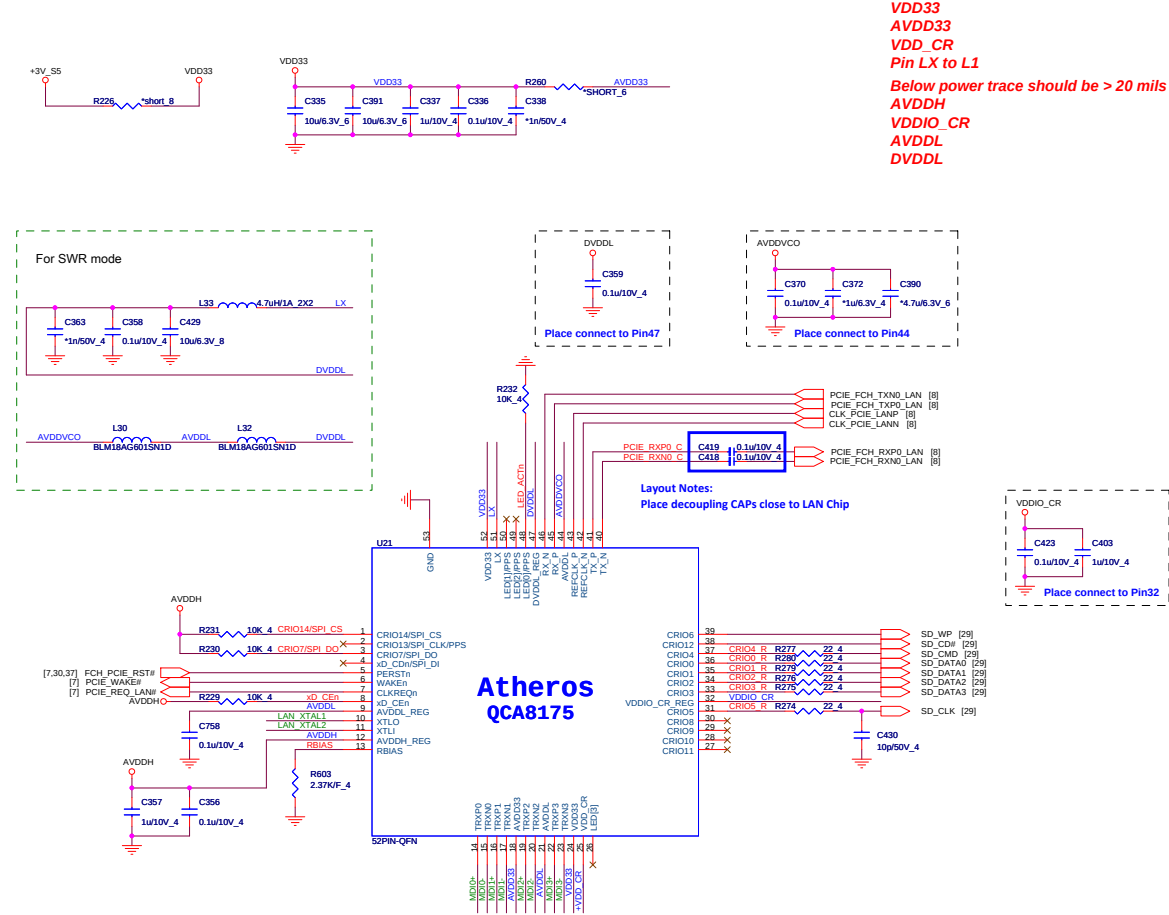
## HDMI HPD SENSE



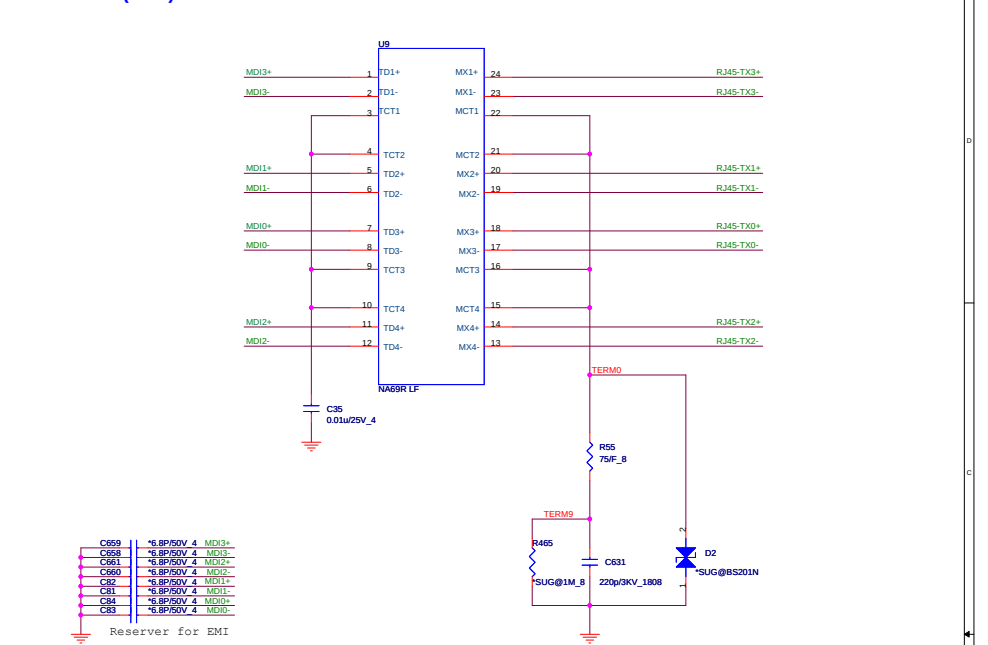
Quanta Computer Inc.  
PROJECT : ZRI/ZQI

| Size                            | Document Number | Rev |
|---------------------------------|-----------------|-----|
|                                 | HDMI            | A1A |
| Date: Wednesday, April 24, 2013 | Sheet 27 of 50  |     |

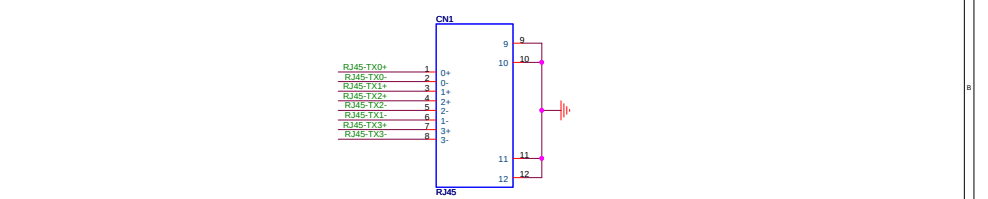
LAN/Card reader (LAN)



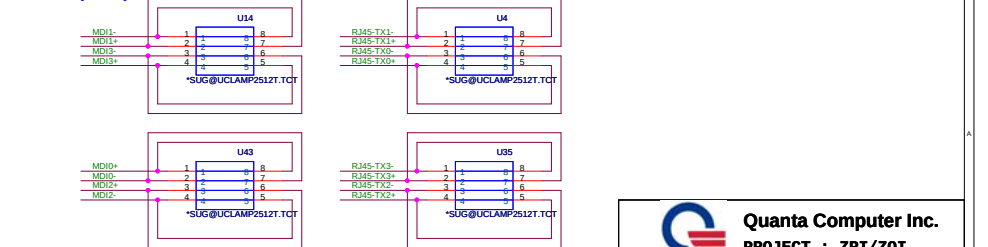
Transformer (LAN)



RJ45 CONNECTOR (LAN)

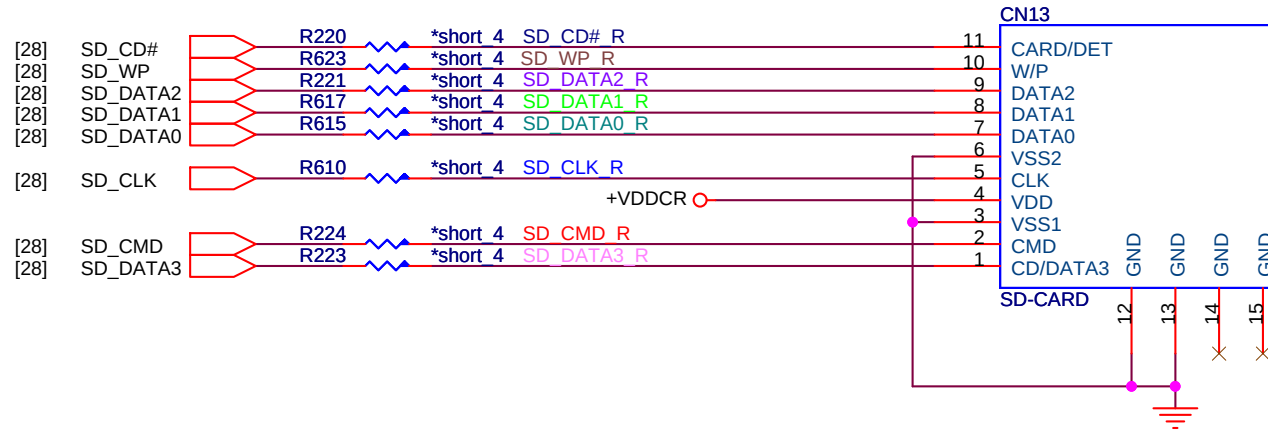


SURGE (LAN)

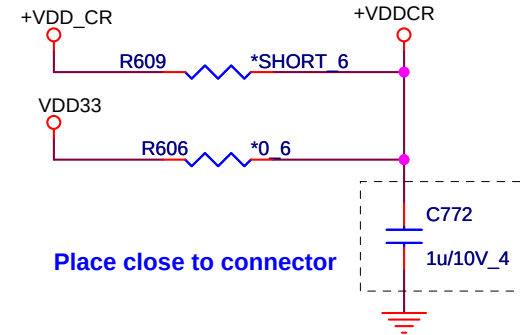
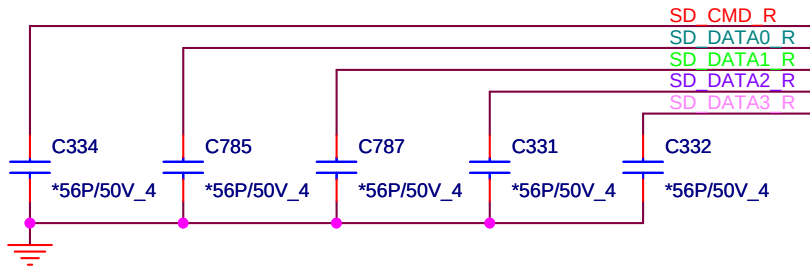


# CARD READER CONNECTOR (MMC)

## SD/MMC CARD READER (MMC)



### EMI



**Quanta Computer Inc.**  
PROJECT : ZRI/ZQI

| Size  | Document Number              | Rev            |
|-------|------------------------------|----------------|
|       | <b>CARD READER CONNECTOR</b> | A1A            |
| Date: | Wednesday, April 24, 2013    | Sheet 29 of 50 |

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

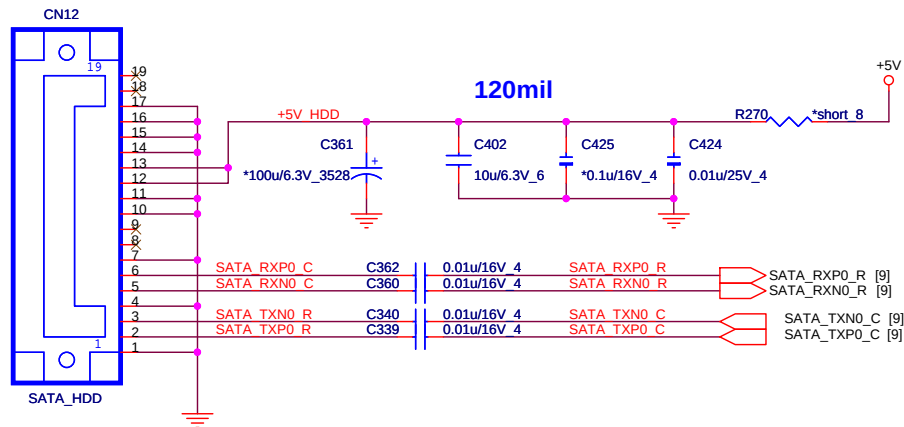


EC: +3VPCU

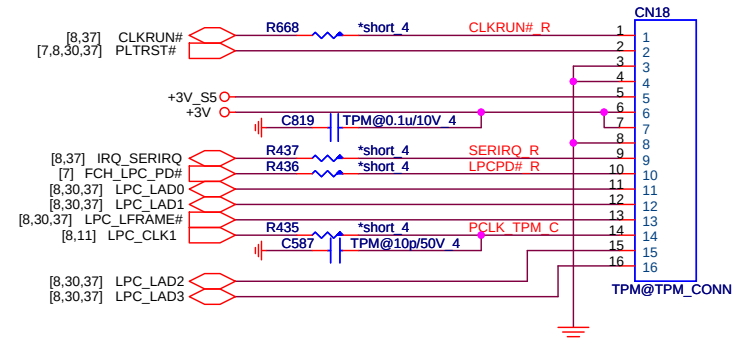




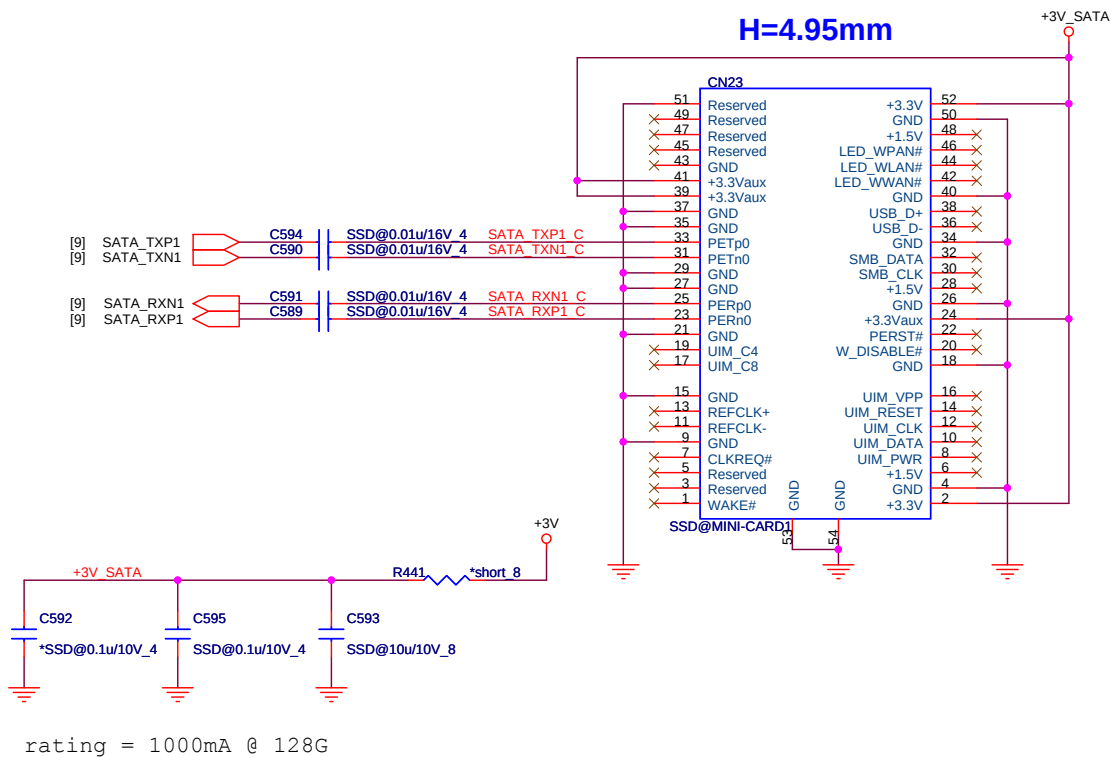
## SATA HDD



## TPM



## MINI-CARD SSD

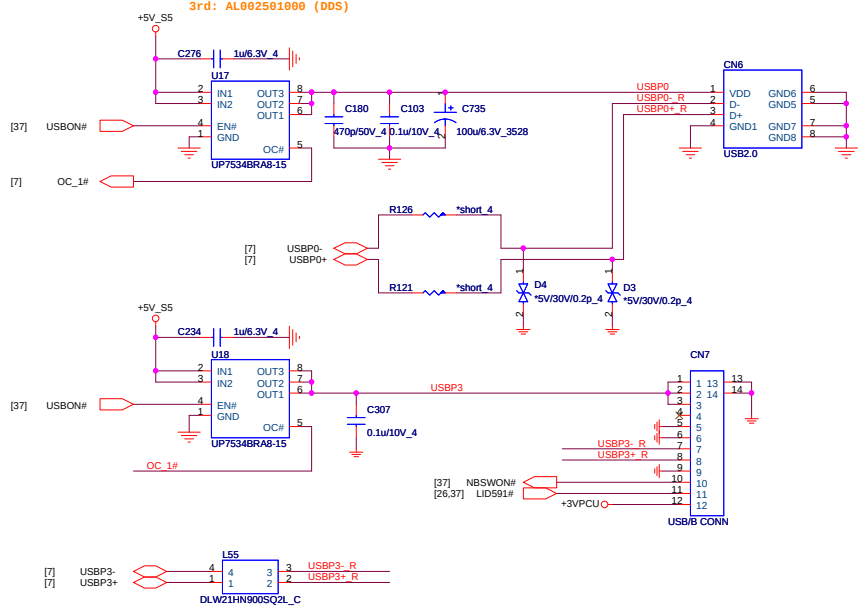


## SATA Re-driver

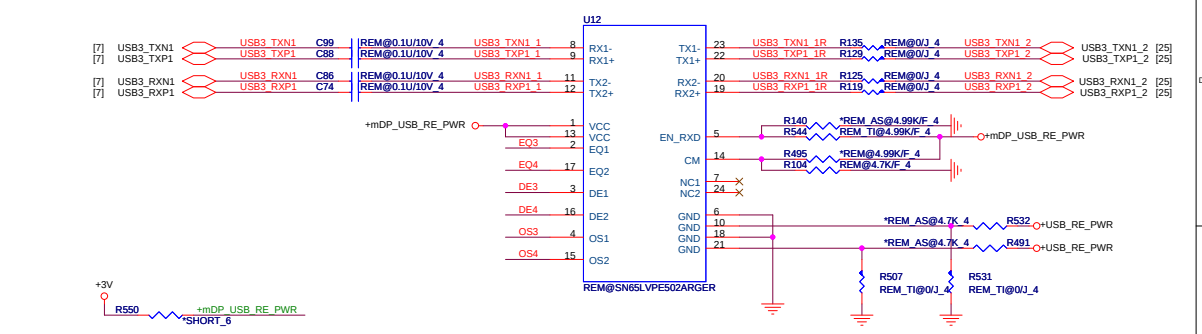


INT & EXT USB2.0

Active Low:  
1st: AL007534009 (Promate)  
2nd: AL000547005 (GMT)  
3rd: AL002501000 (DDS)

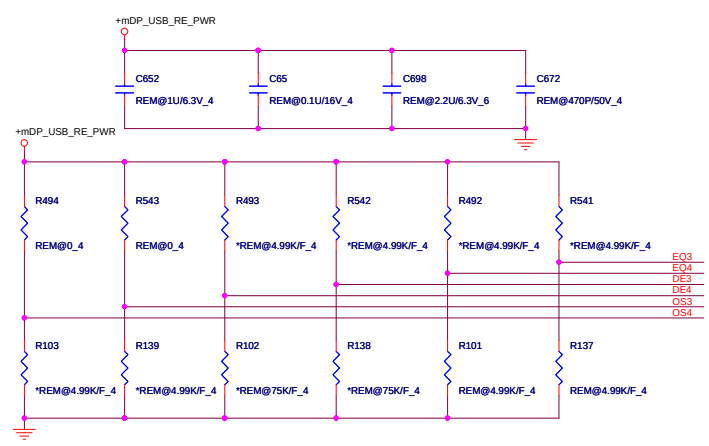


mDP USB3.0 re-driver IC



USB3\_RXP1 R515 NREM@0/0\_4 USB3\_RXP1\_2  
USB3\_RXN1 R510 NREM@0/0\_4 USB3\_RXN1\_2  
USB3\_TXN1 R525 NREM@0/0\_4 USB3\_TXN1\_2  
USB3\_TXP1 R522 NREM@0/0\_4 USB3\_TXP1\_2

| Control pins setting |                  |            |                      |
|----------------------|------------------|------------|----------------------|
| EN_RXD               | Device function  | CM         | Device function      |
| 1(default)           | Normal Operation | 0(default) | Normal Operation     |
| 0                    | Sleep Mode       | 1          | Compliance Test Mode |

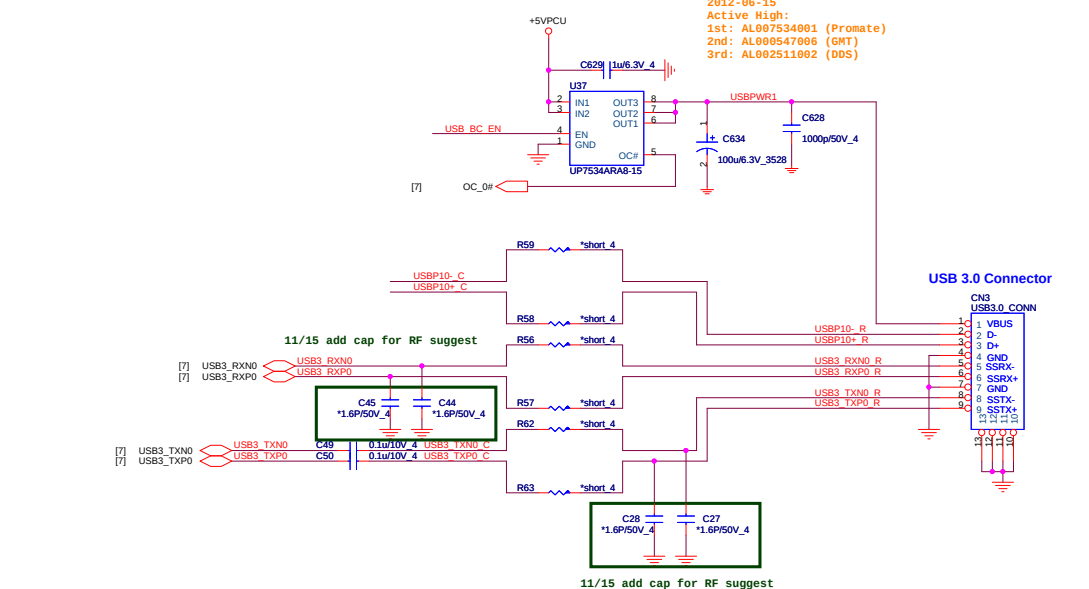




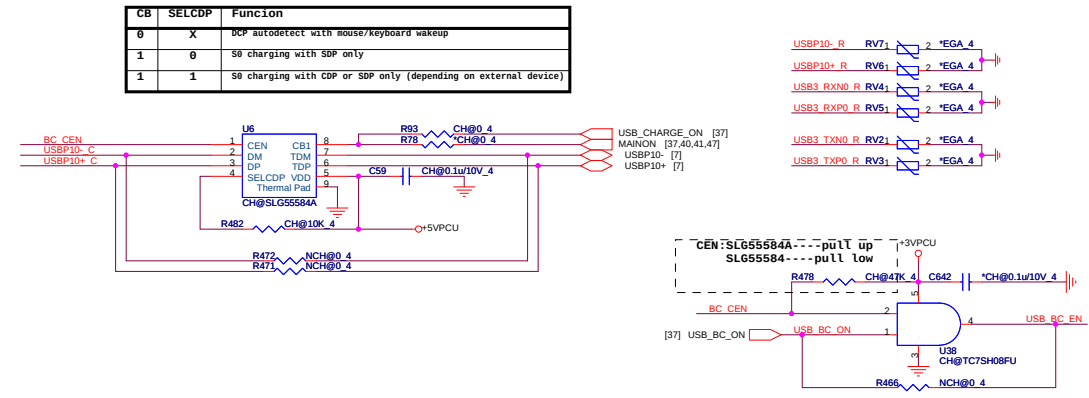
**Quanta Computer Inc.**  
**PROJECT : ZRI/ZQI**

|       |                           |                |
|-------|---------------------------|----------------|
| Size  | Document Number           | Rev            |
|       | <b>INT&amp;EXT USB</b>    | A1A            |
| Date: | Wednesday, April 24, 2013 | Sheet 33 of 50 |

USB3.0/2.0



USB Charger to 3.0



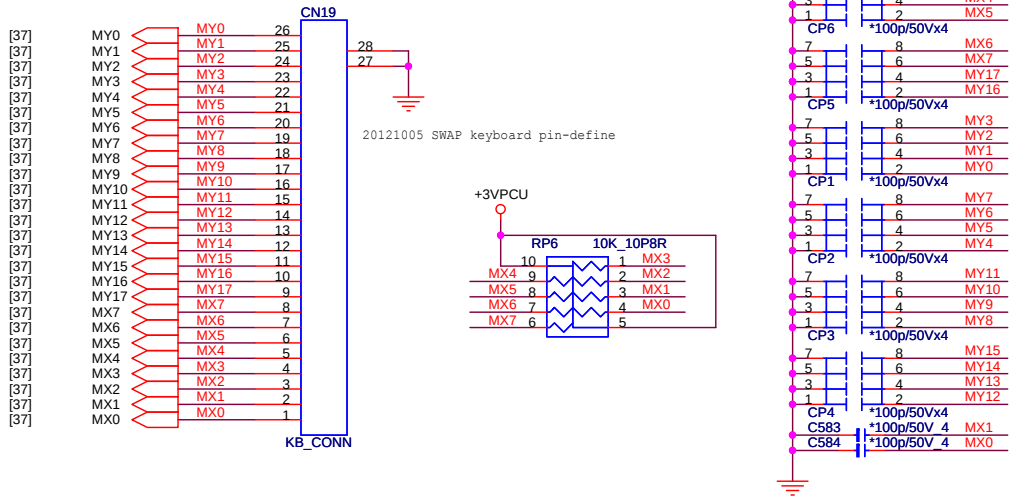
USB3.0 re-driver IC

Quanta Computer Inc.  
PROJECT : ZRI/ZQI

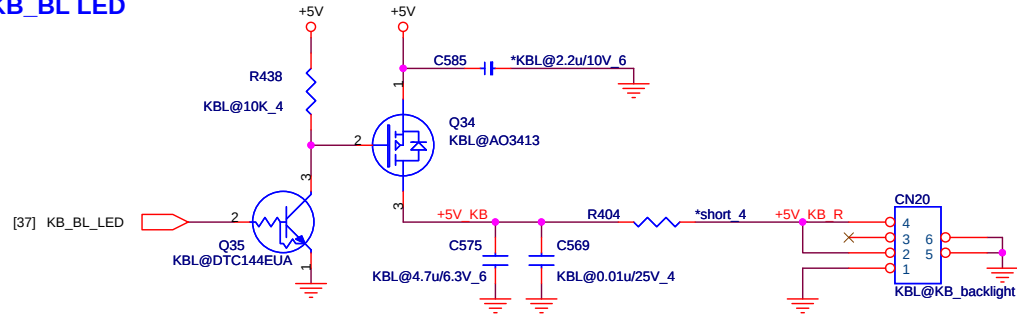
| Size | Document Number | Rev |
|------|-----------------|-----|
|      | INT&EXT USB     | A1A |

Date: Wednesday, April 24, 2013 1 Sheet 34 of 50

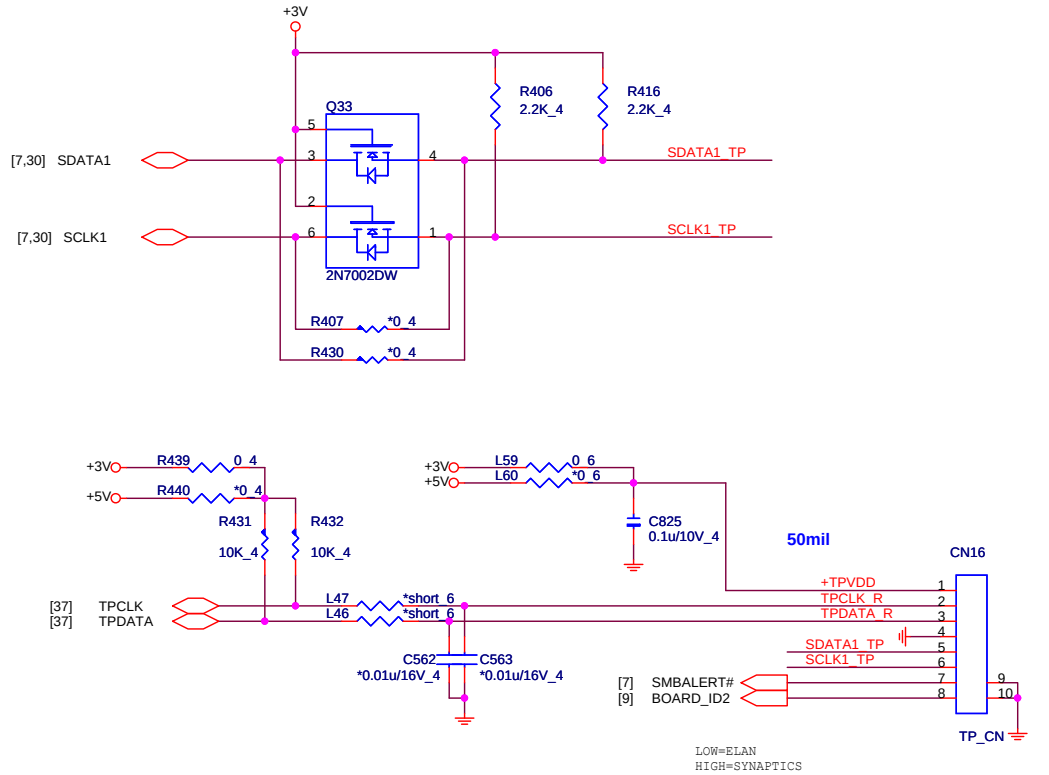
## K/B(KBC)



## KB\_BL LED

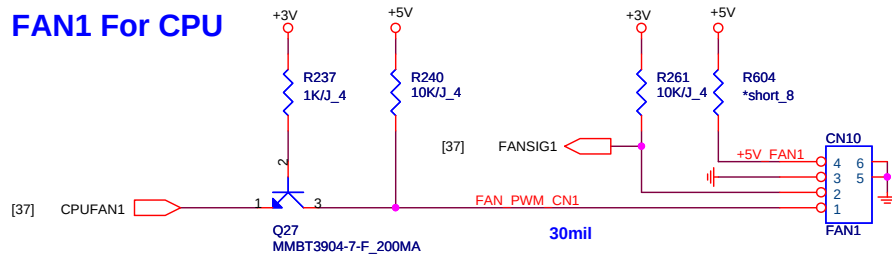


## TOUCHPAD BOARD CONN(TPD)



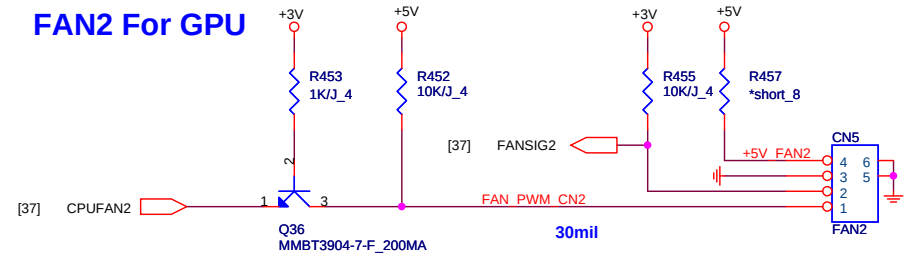
## CPU FAN(THM)

### FAN1 For CPU



If need to support XT(25) GPU, need check with thermal

### FAN2 For GPU



Quanta Computer Inc.

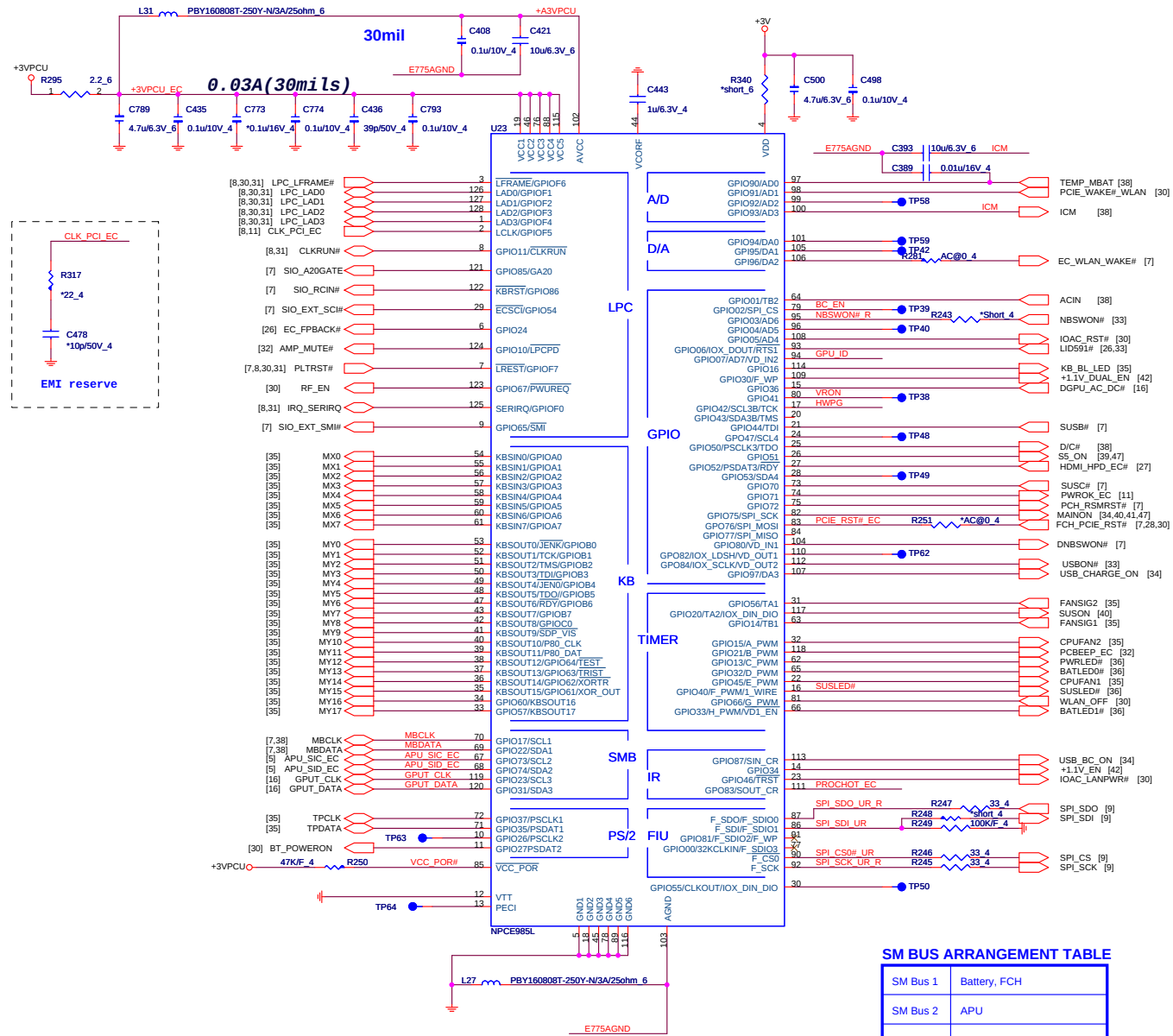
PROJECT : ZRI/ZQI

| Size | Document Number | Rev |
|------|-----------------|-----|
|      | KB/TP/FAN       | A1A |

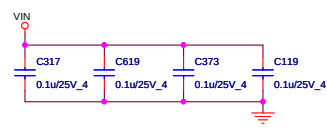
Date: Wednesday, April 24, 2013 Sheet 35 of 50



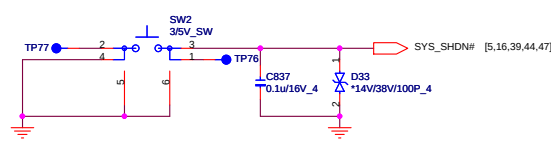
EC(KBC)



Placement for EC of VIN power plan

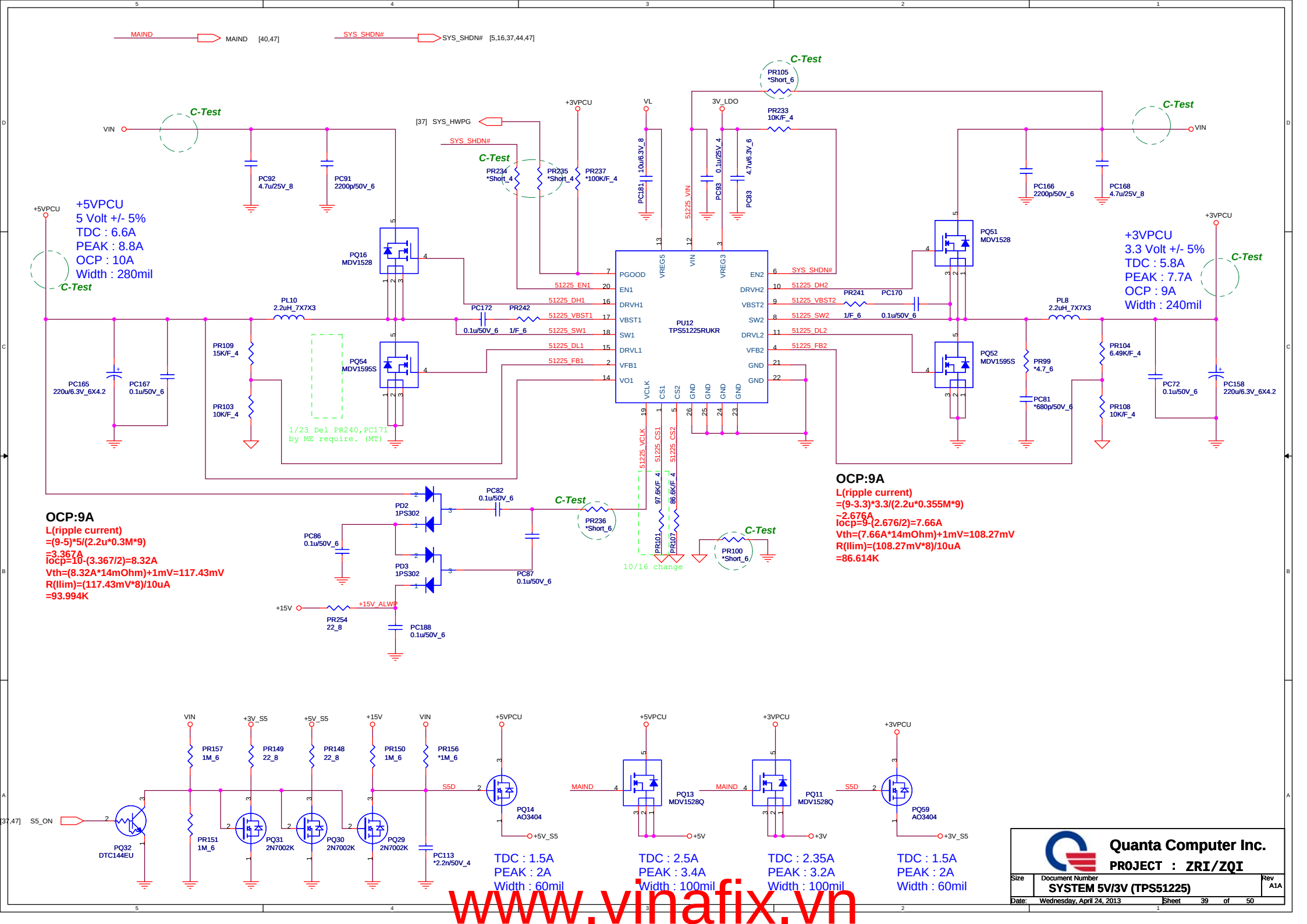


3/5VPCU reset switch (CLG)









TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

TDC : 0.75A  
PEAK : 1A  
Width : 40mil

+SMDDR\_VREF

PC184  
0.22u/10V\_4

+3V

PR126  
100K/F\_4

[37] HWPV\_VDDR

[34,37,41,47] MAINON

[37] SUSON

VREF=1.8V

51216 S3

51216 S5

PC186  
0.1u/10V\_4

PR248  
10K/F\_4

PR251  
51K/F\_4

PC187  
0.01u/25V\_4

OCP=18A  
L ripple current  
= $(19-1.5) \cdot 1.5 / (0.68 \mu \cdot 400 \text{k} \cdot 19)$   
=5.079A  
Vtrip=18- $(5.079/2) \cdot 4.3 \text{mohm}$   
=0.06647V  
Rlimit=0.06647/10uA\*8=53.183Kohm

| Mode | Frequency | Discharge mode     |
|------|-----------|--------------------|
| 200K | 400K      | Tracking Discharge |
| 100K | 300K      | Tracking Discharge |

|                 | S3 | S5 | +1.5VSUS | REF | VTT |
|-----------------|----|----|----------|-----|-----|
| S0              | 1  | 1  | ON       | ON  | ON  |
| S3 (mainon off) | 0  | 1  | ON       | ON  | OFF |
| S4/S5           | 0  | 0  | OFF      | OFF | OFF |

Close to IC

Greater than or equal 40mil

+5V\_S5

PC176  
10u/6.3V\_8

PC103  
1u/10V\_4

PQ21  
RJK03J6DPA

51216 DRVH

51216 VBSL

51216 SW

51216 DRVL

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

51216 S3

51216 S5

RDSon=4.3mohm

Close to output cap

C-Test

C-Test

+1.5VSUS  
1.5 Volt +/- 5%  
TDC : 11.3A  
PEAK : 15A  
OCP : 18A  
Width : 480mil

+1.5VSUS

+1.5V

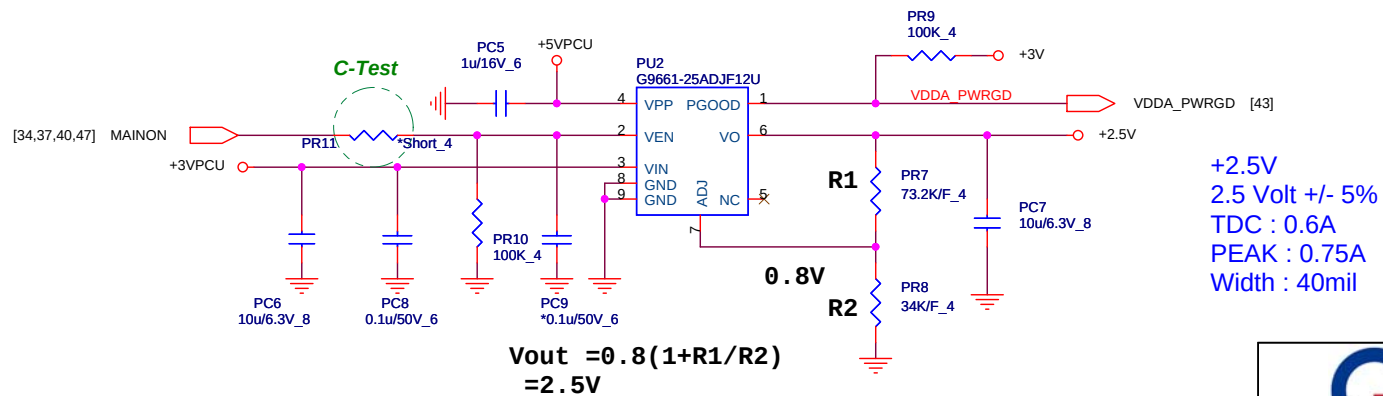
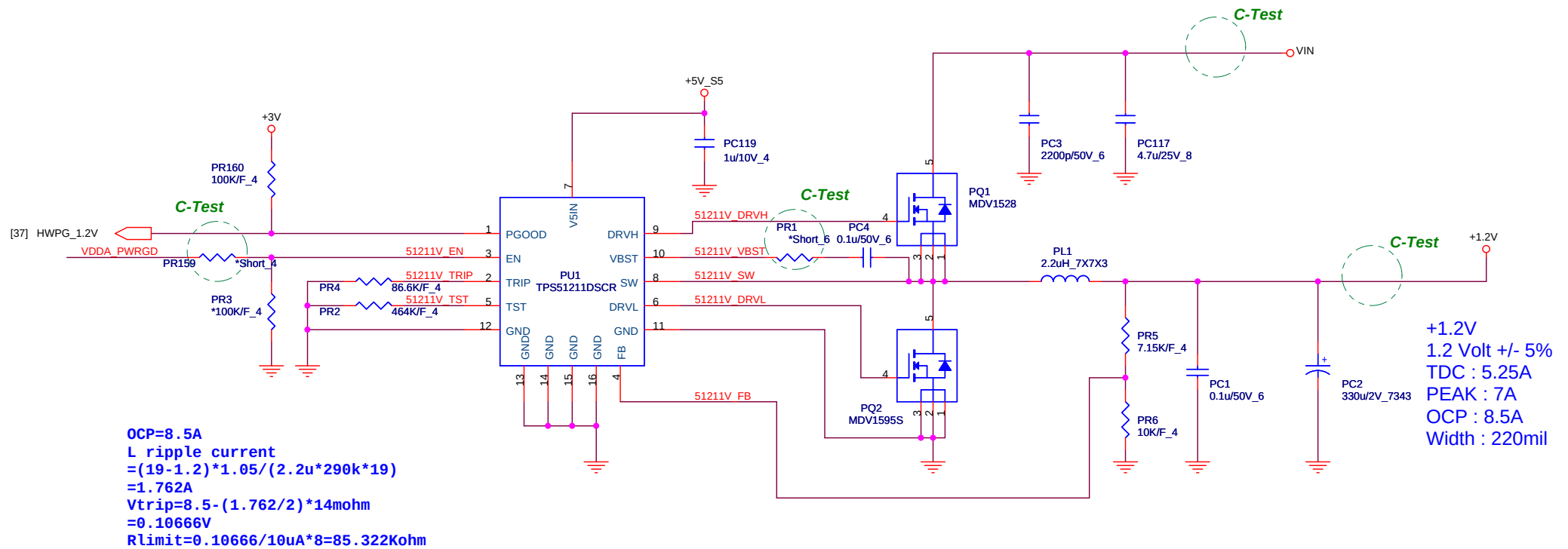
TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

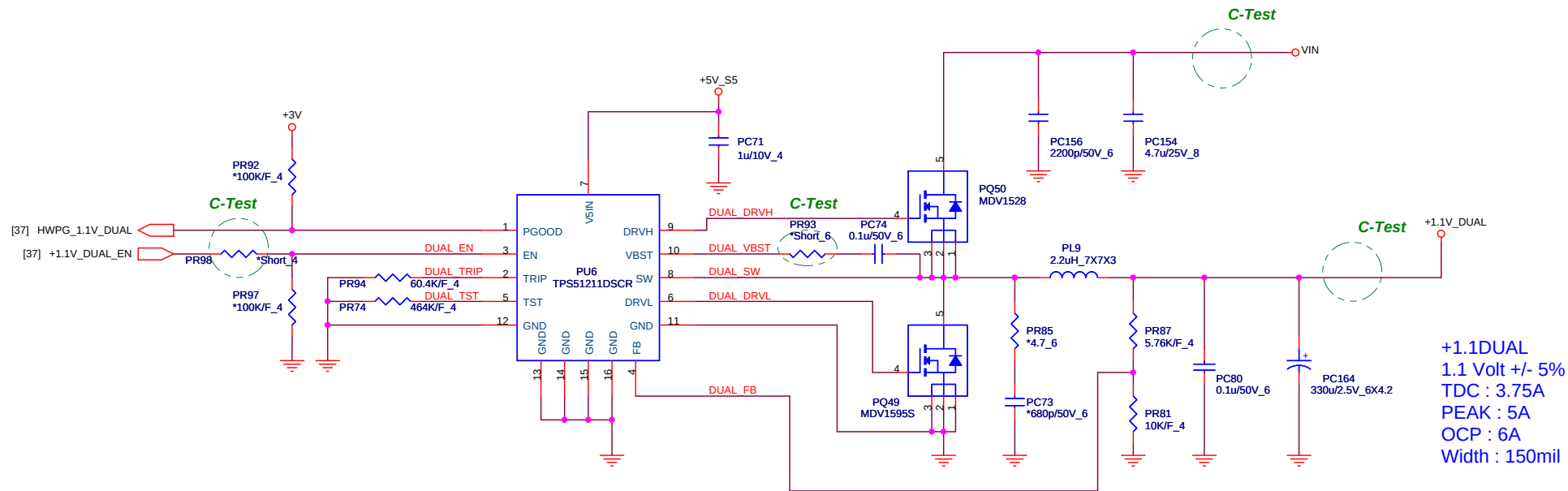


Quanta Computer Inc.  
PROJECT : ZRI/ZQI

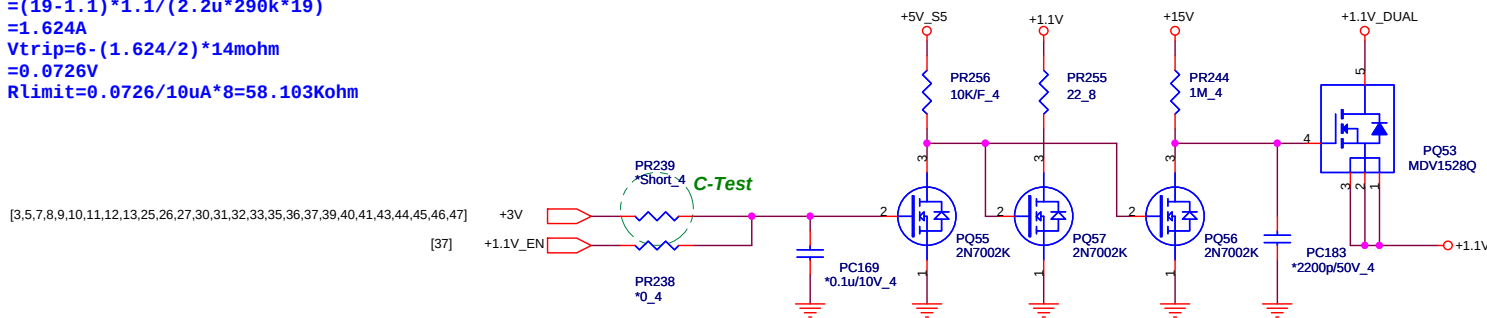
| Size | Document Number    | Rev |
|------|--------------------|-----|
|      | DDR 1.5V(TPS51216) | A1A |

Date: Wednesday, April 24, 2013 Sheet 40 of 50





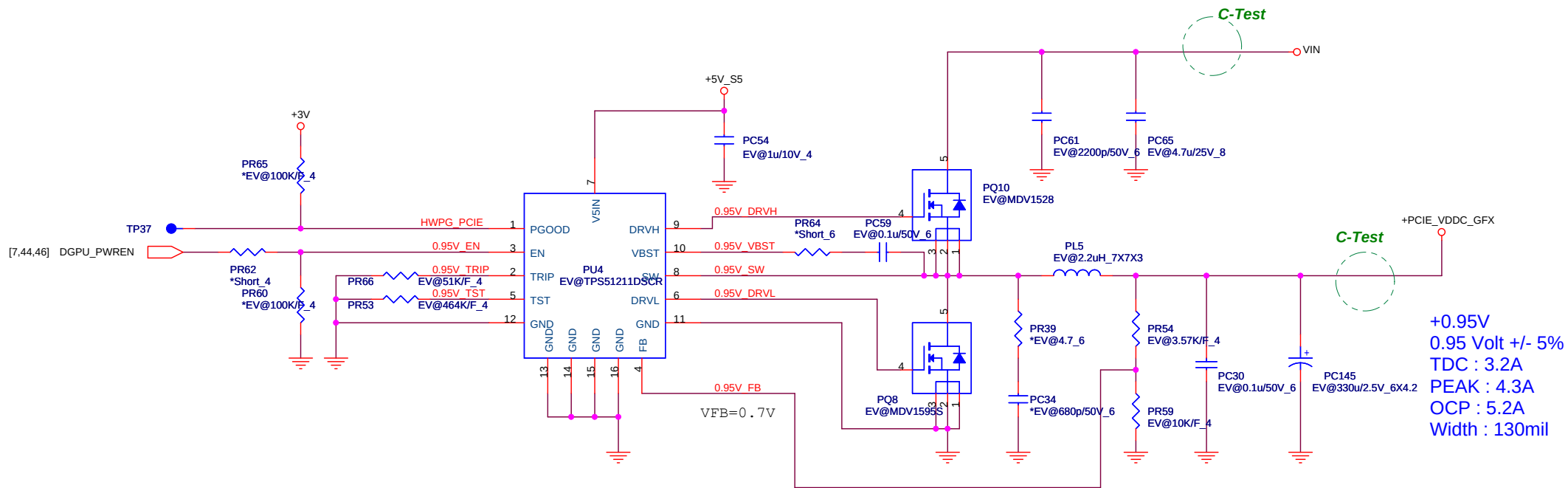
OCP=6A  
 L ripple current  
 $= (19-1.1) * 1.1 / (2.2u * 290k * 19)$   
 $= 1.624A$   
 $V_{trip} = 6 - (1.624/2) * 14mohm$   
 $= 0.0726V$   
 $R_{limit} = 0.0726 / 10uA * 8 = 58.103Kohm$



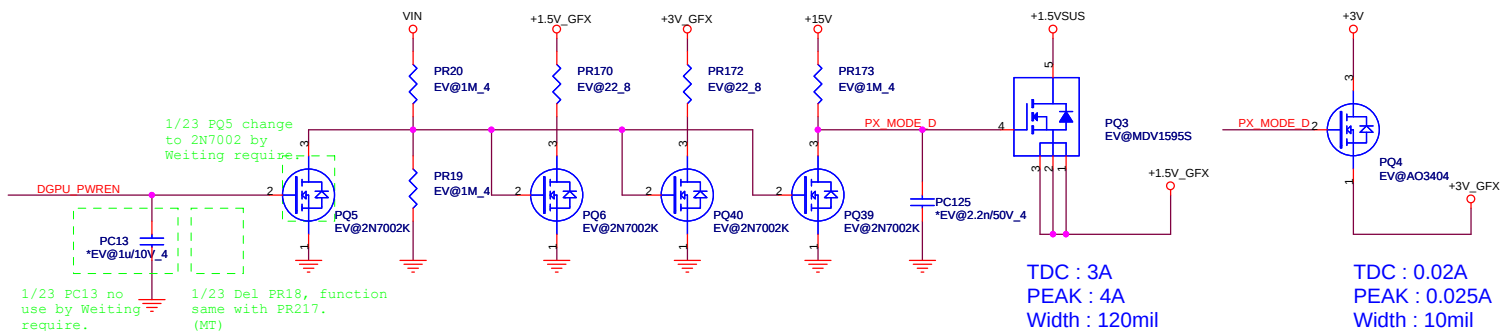
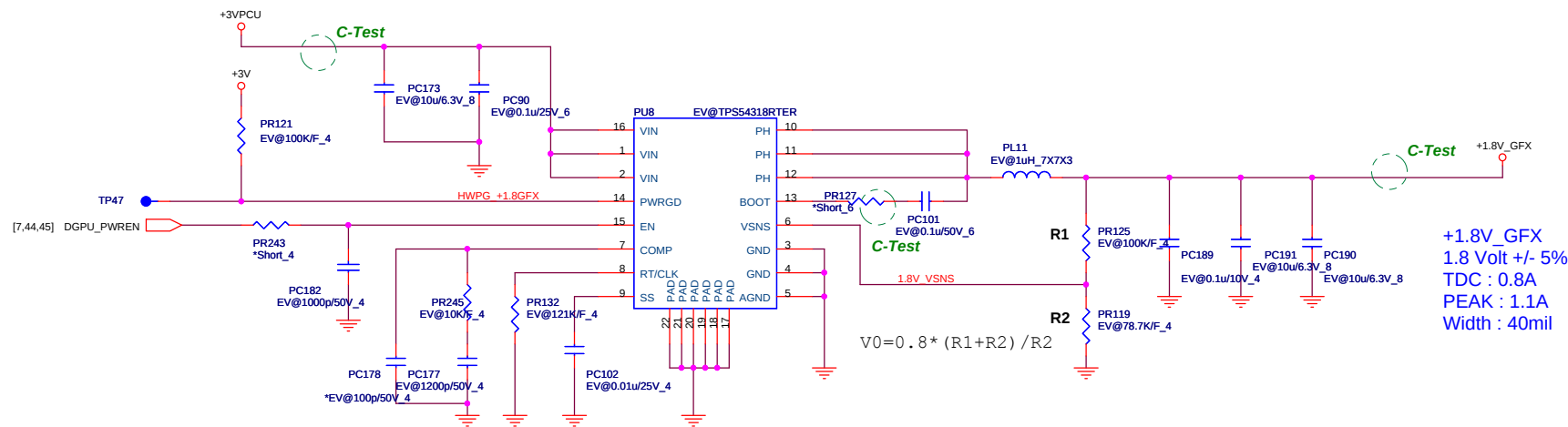
|                                                                                                                                               |                             |                |
|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZRI/ZQI</b> |                             |                |
| Size                                                                                                                                          | Document Number             | Rev            |
|                                                                                                                                               | <b>+1.1V_DUAL(TPS51211)</b> | A1A            |
| Date:                                                                                                                                         | Wednesday, April 24, 2013   | Sheet 42 of 50 |





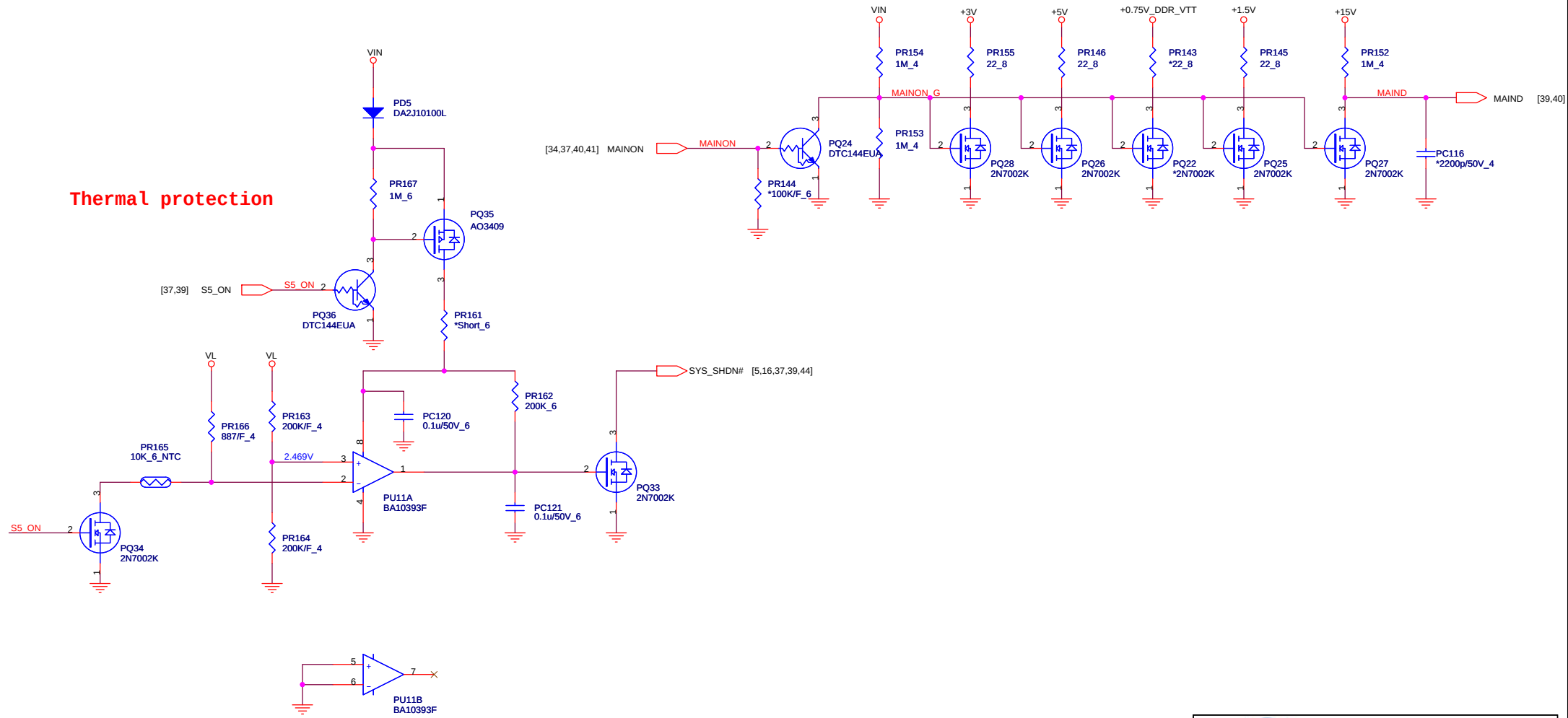


OCP=5.2A  
 L ripple current  
 $= (19 - 0.95) * 0.95 / (2.2u * 290k * 19)$   
 $= 1.415A$   
 $V_{trip} = 5.2 - (1.415 / 2) * 14mohm$   
 $= 0.06289V$   
 $R_{limit} = 0.06289 / 10uA * 8 = 50.318Kohm$





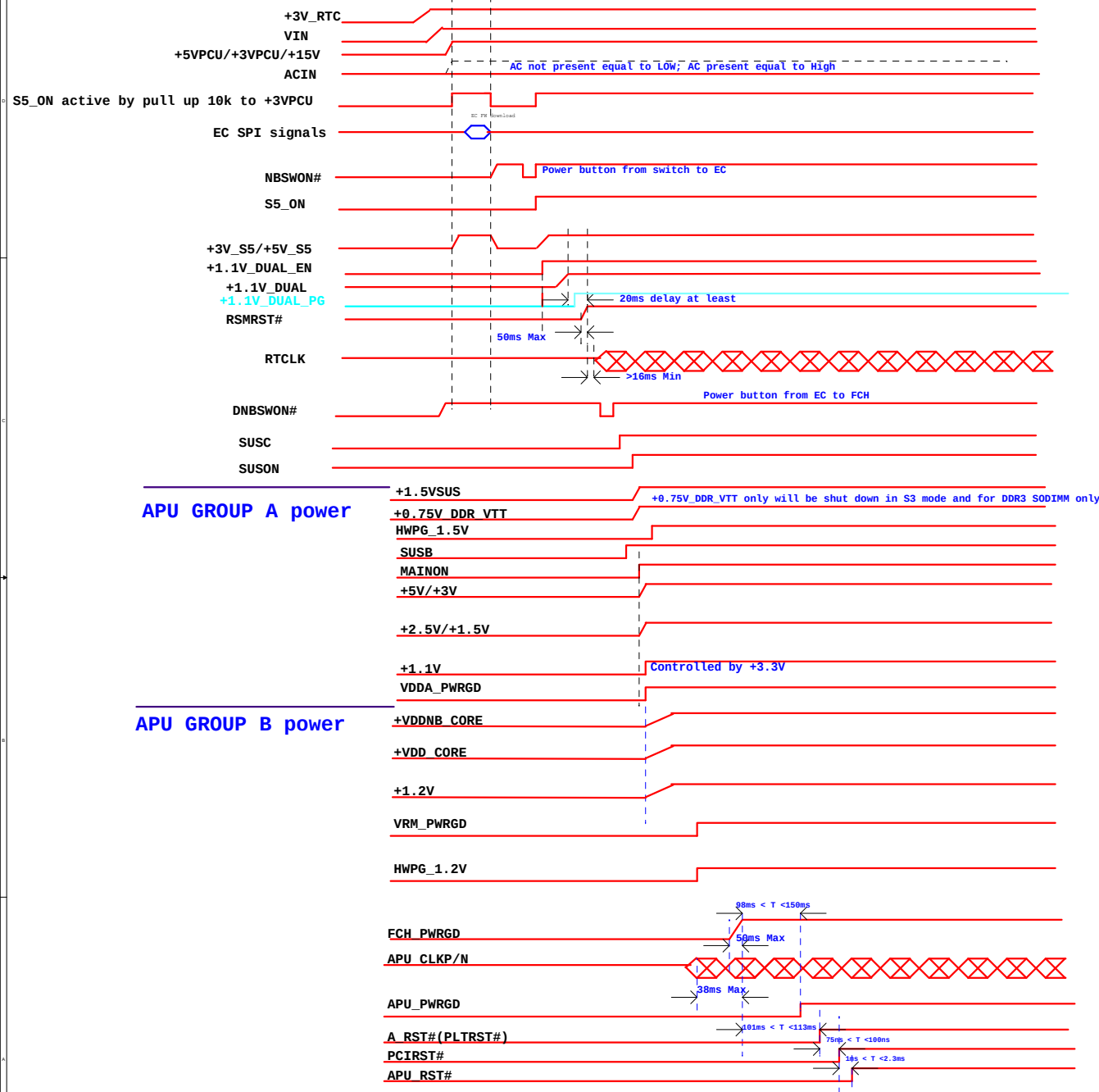
Thermal protection



For EC control thermal protection (output 3.3V)

|                                                                                       |                           |                             |          |
|---------------------------------------------------------------------------------------|---------------------------|-----------------------------|----------|
|  |                           | <b>Quanta Computer Inc.</b> |          |
|                                                                                       |                           | <b>PROJECT : ZRI/ZQI</b>    |          |
| Size                                                                                  | Document Number           | Rev A1A                     |          |
|                                                                                       |                           | <b>Discharge/Thermal</b>    |          |
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## ZRP Power On Sequence: S5 &gt; S0



## APU Power on sequence required:

## Llano APU:

1.Group A ( +1.5VSUS, +2.5V\_VDDA ) ramp before Group B  
( +VDD\_CORE, +VDDNB\_CORE, +1.2V\_VDDPR )

## HUDSON-M3:

1.+3V\_S5 ramp before +1.1V\_DUAL  
2.+3V ramp before +1.1V  
3.+3V\_S5,+3V ramping down time > 300us  
4.100us <= +3V\_S5,+3V <= 40ms  
5.100us <= All power rails except +3V\_S5,+3V <= 40ms

## Power Tree Table

