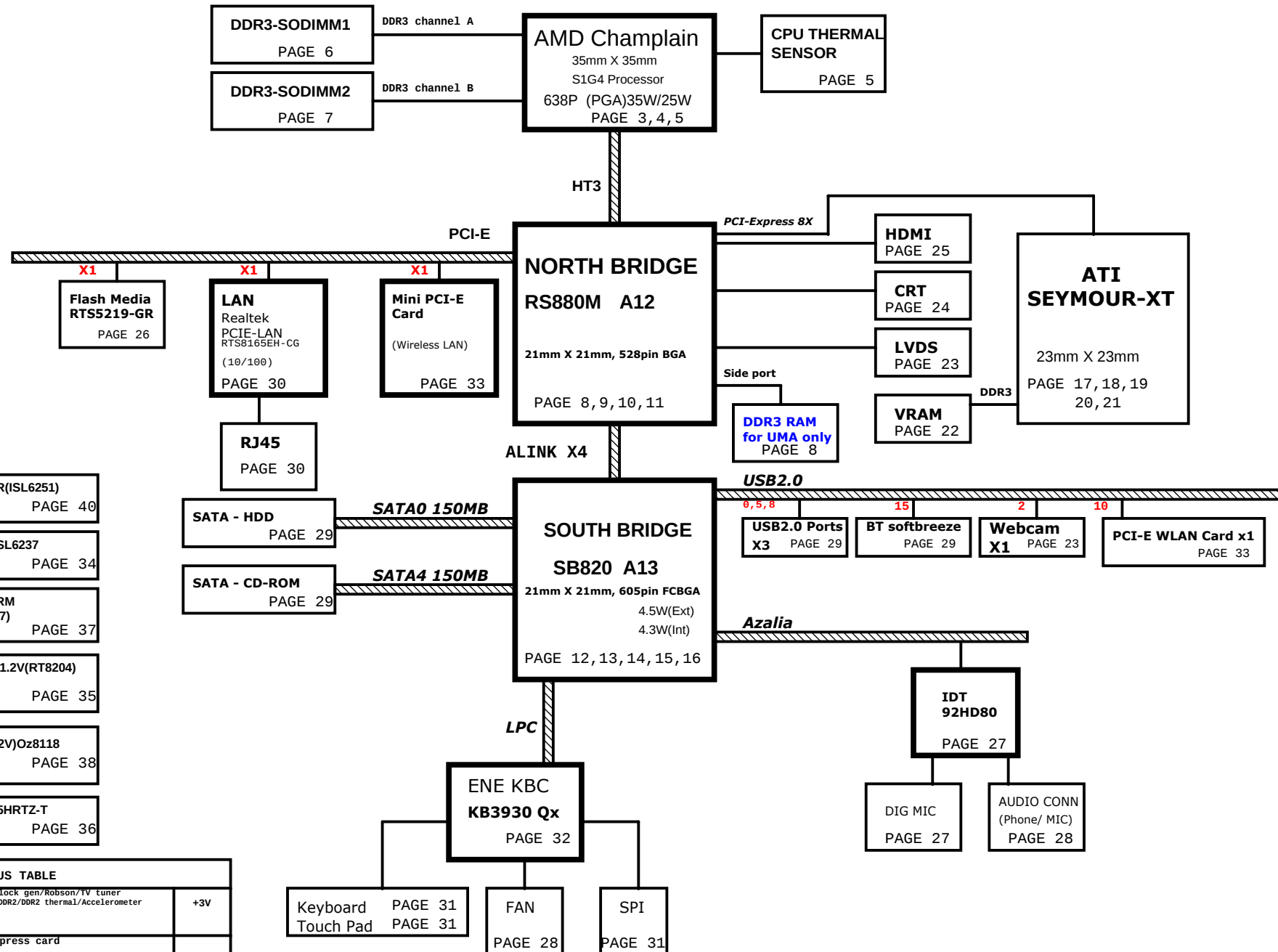


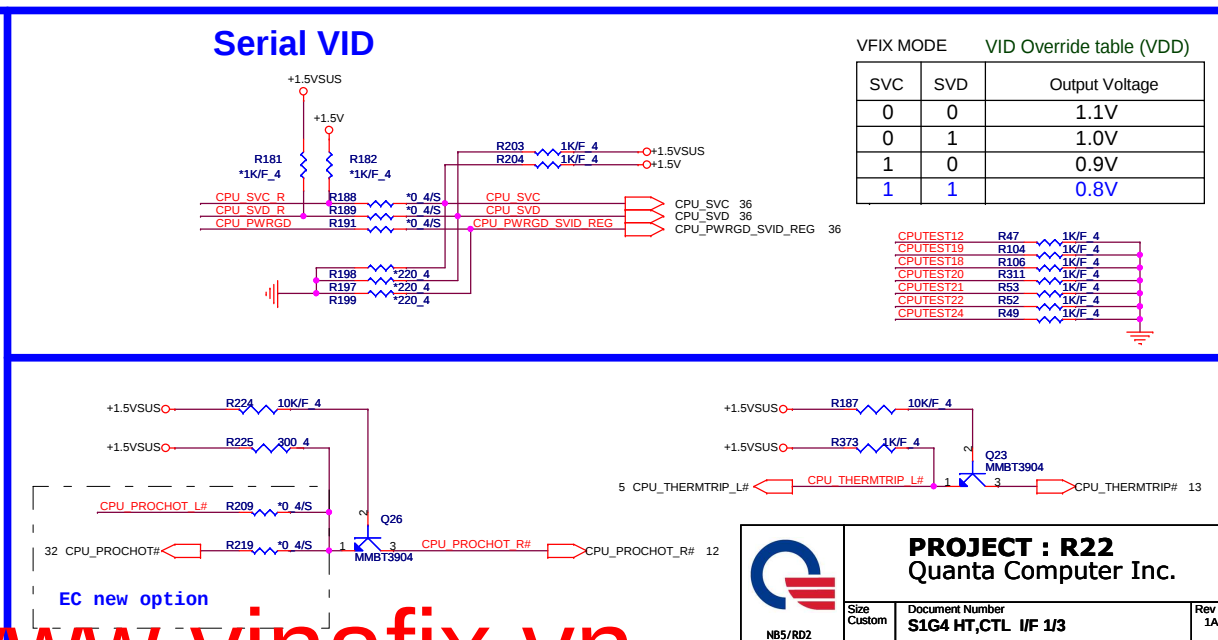
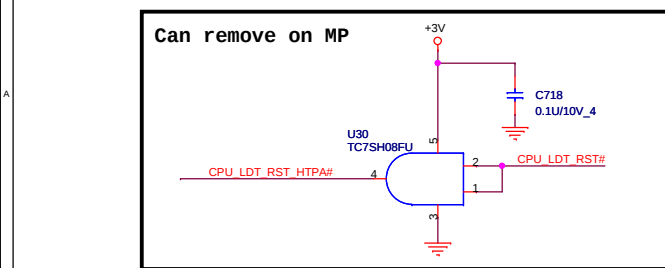
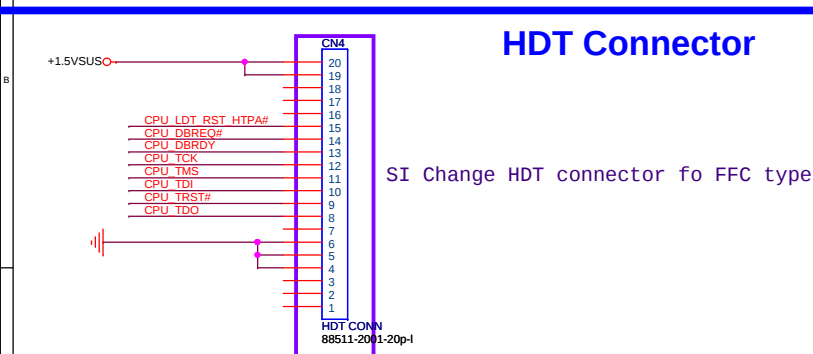
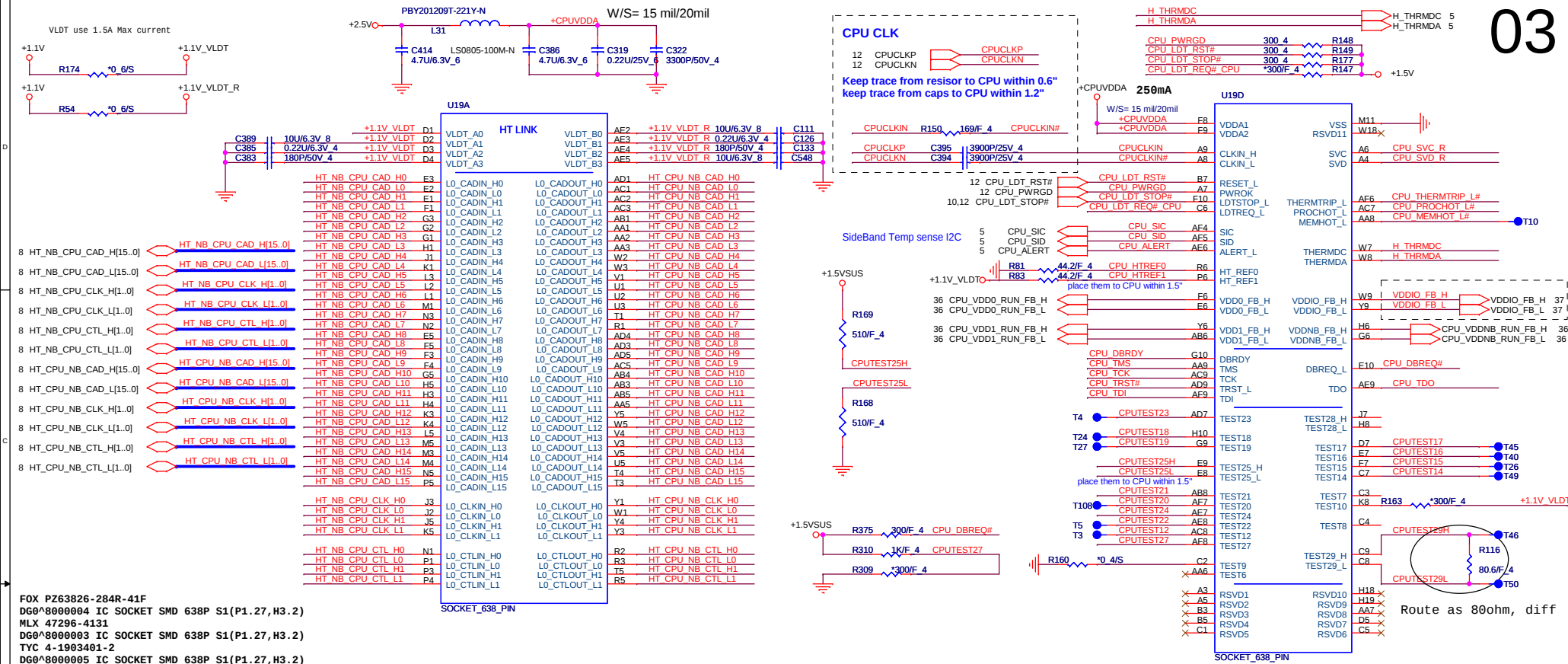
R22 SYSTEM DIAGRAM

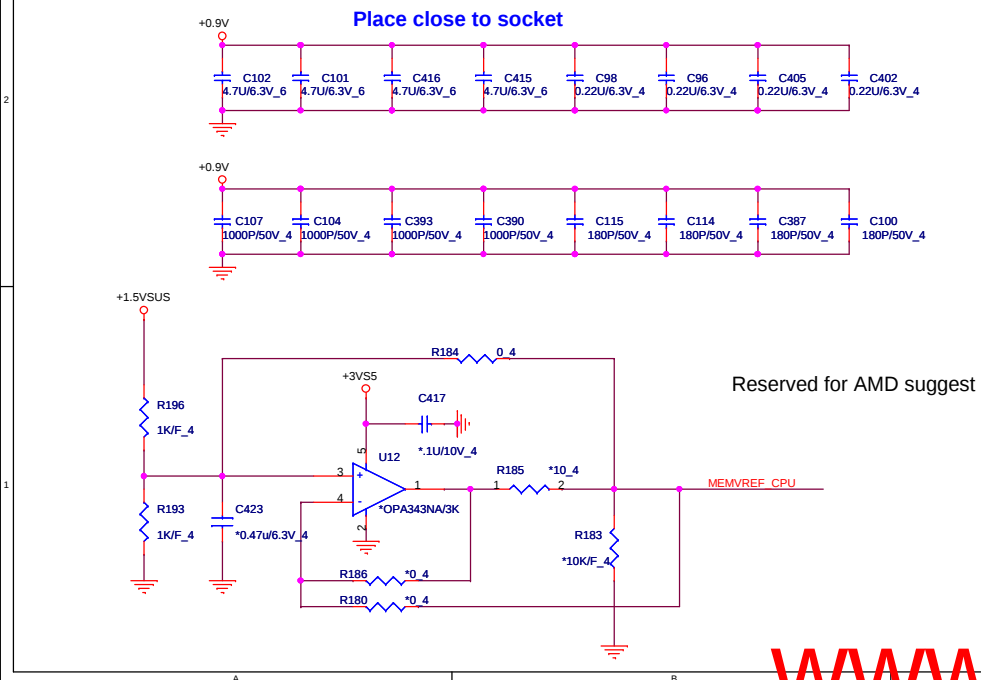
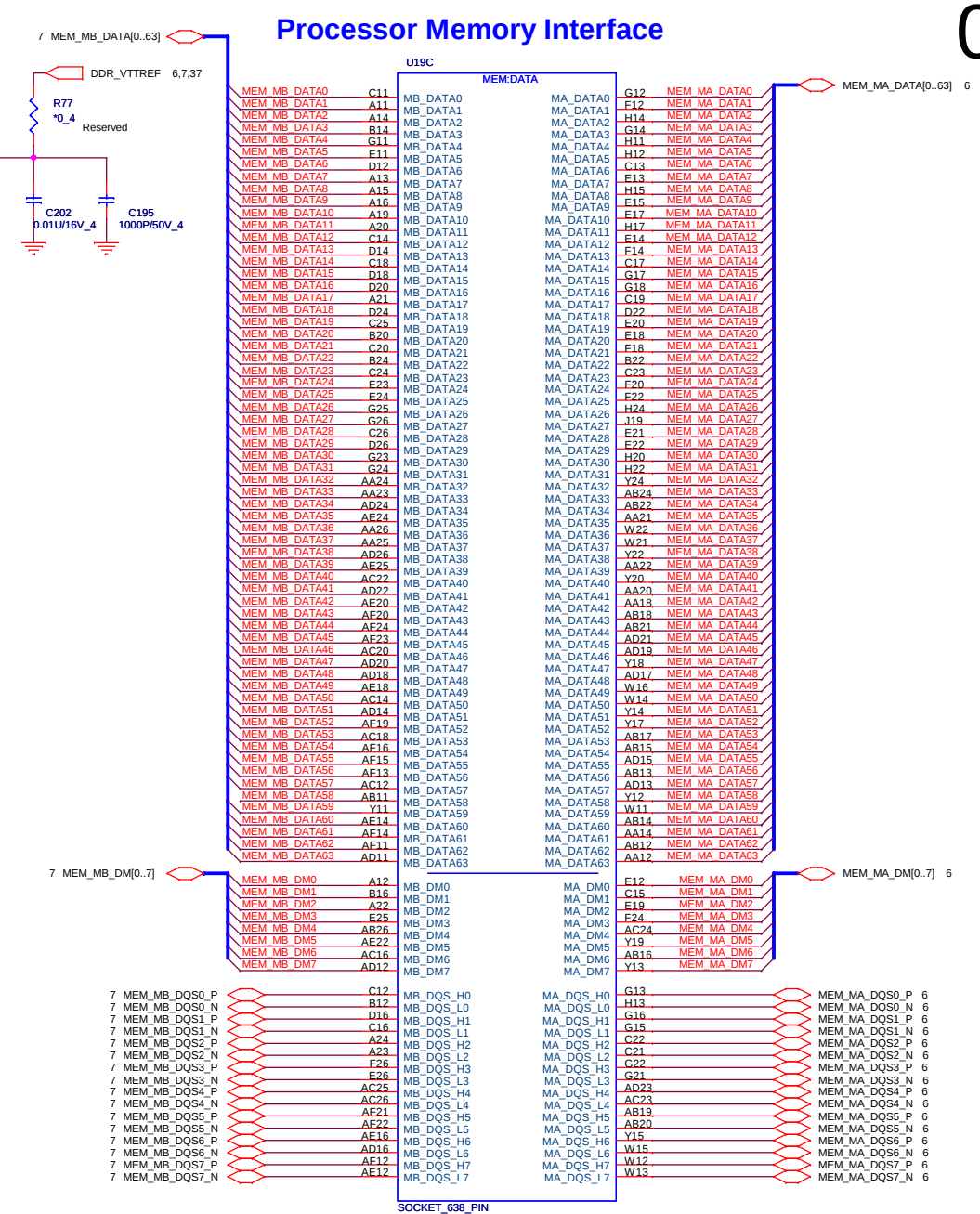
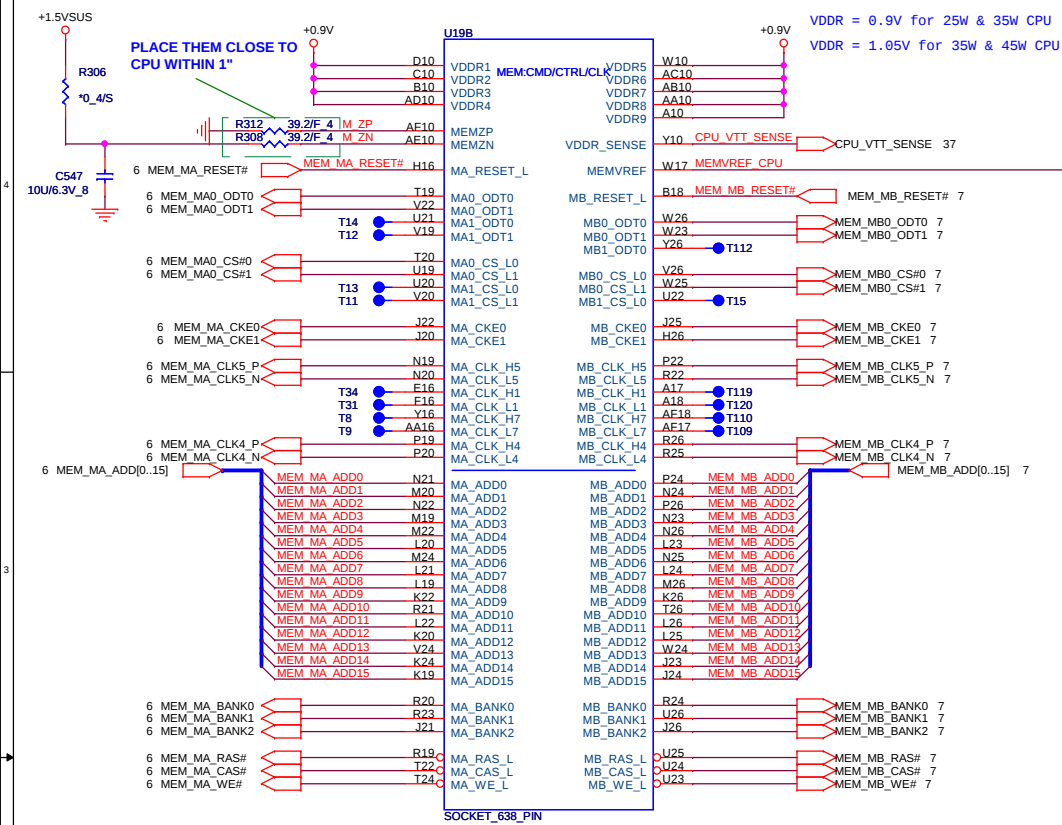


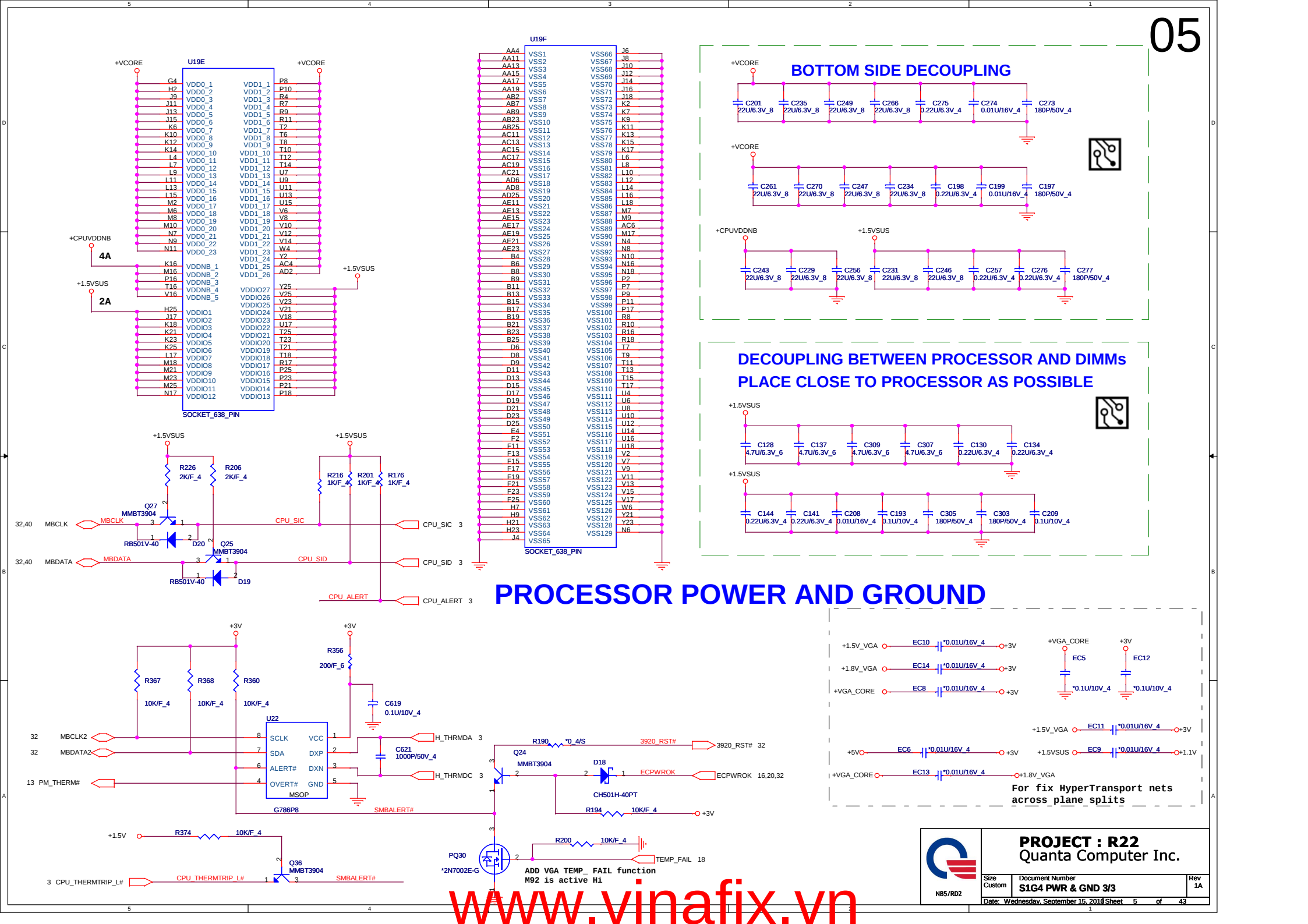
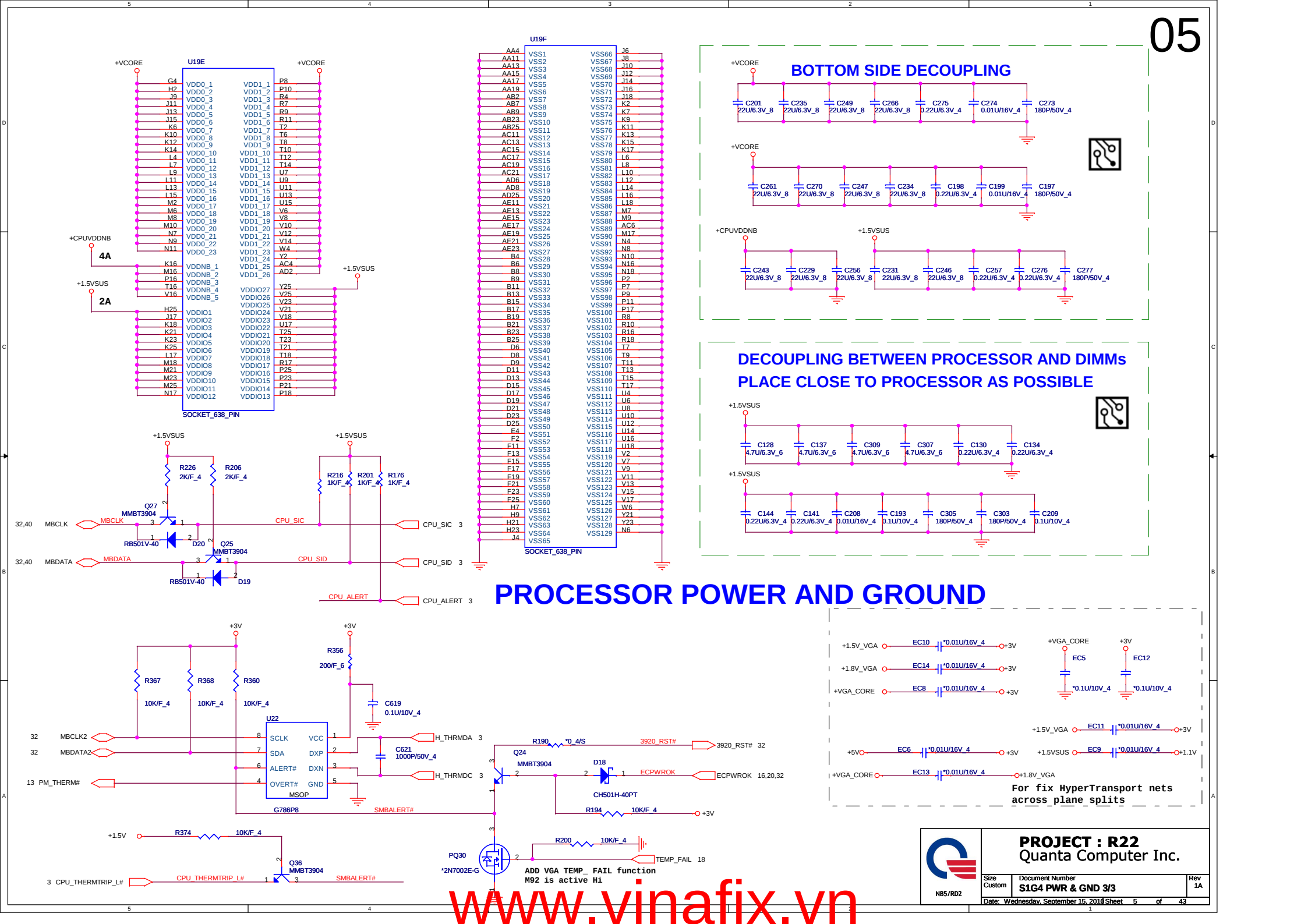
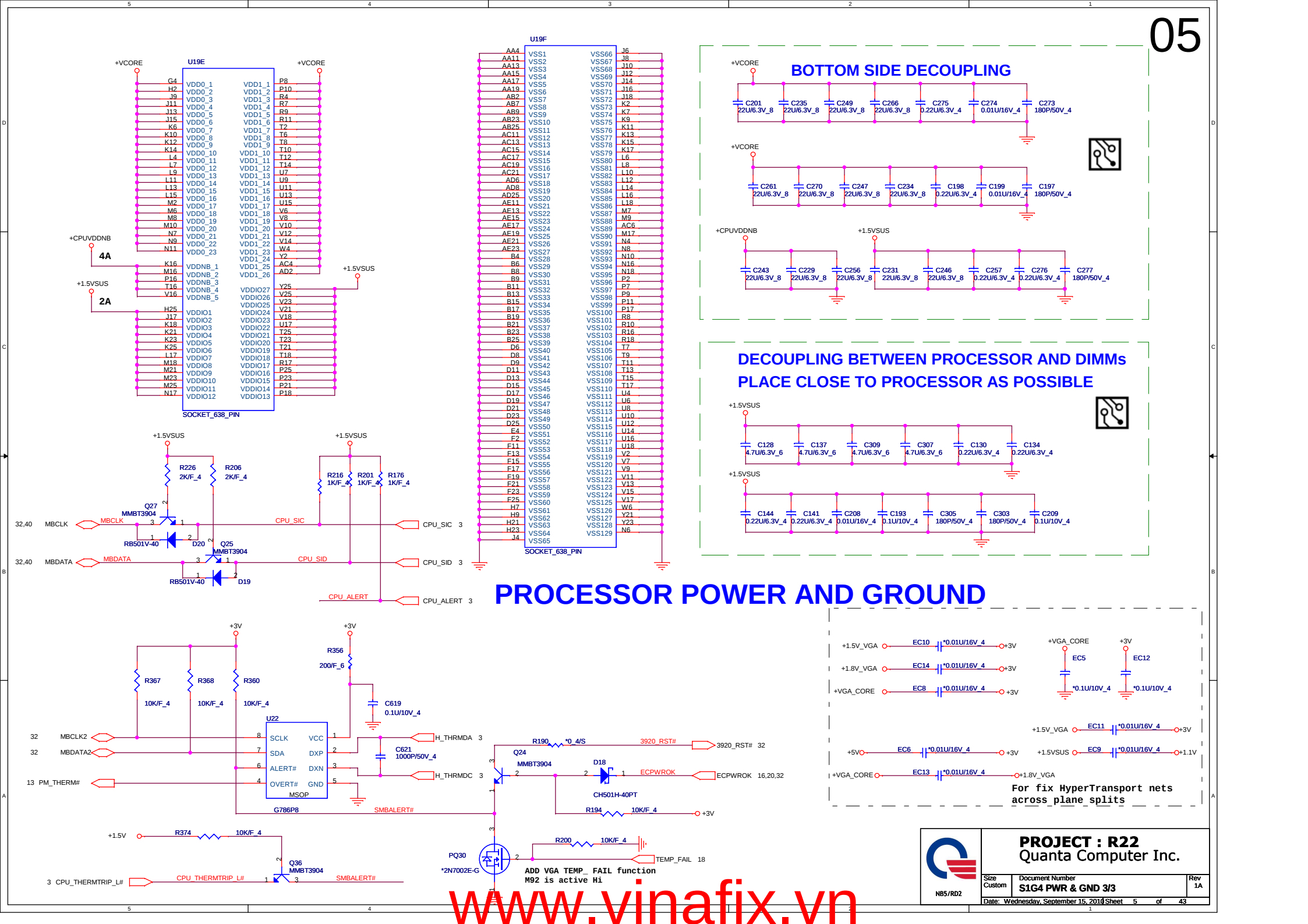
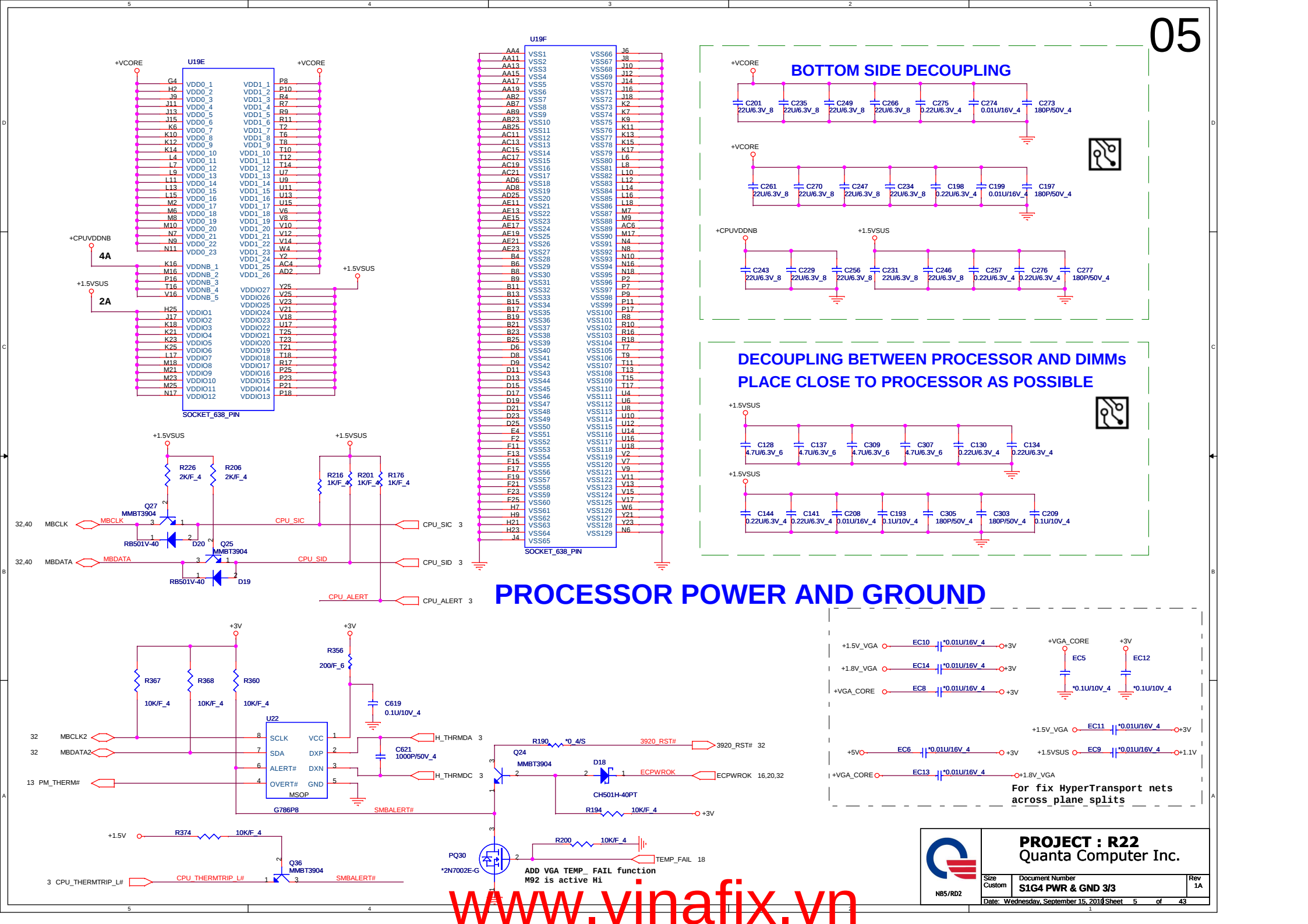
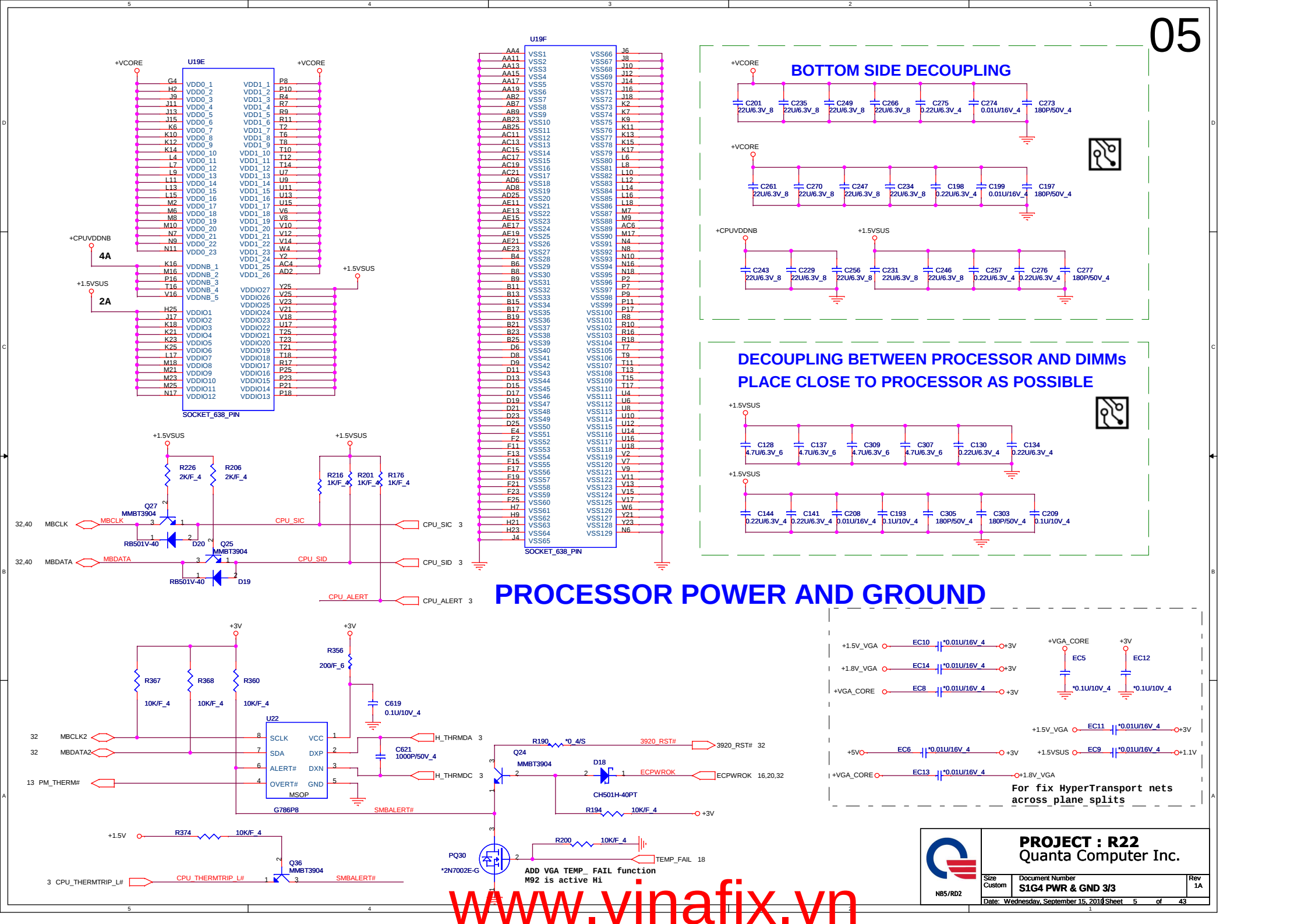
01



Use internal CLK GEN





[illegible][illegible]

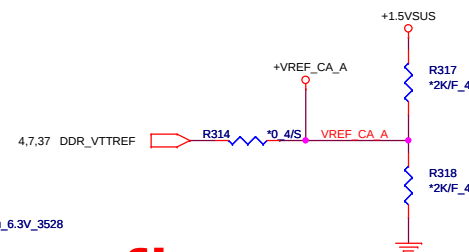
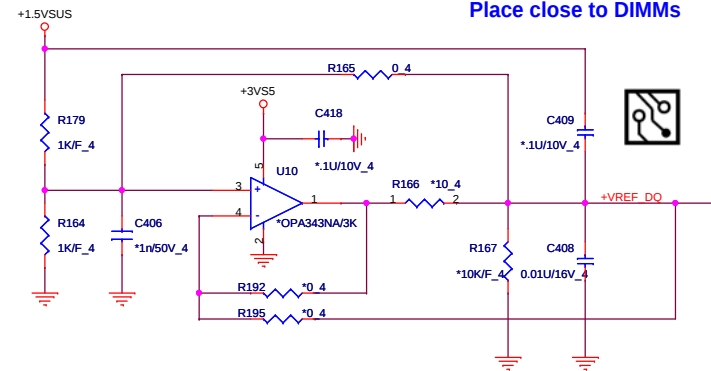


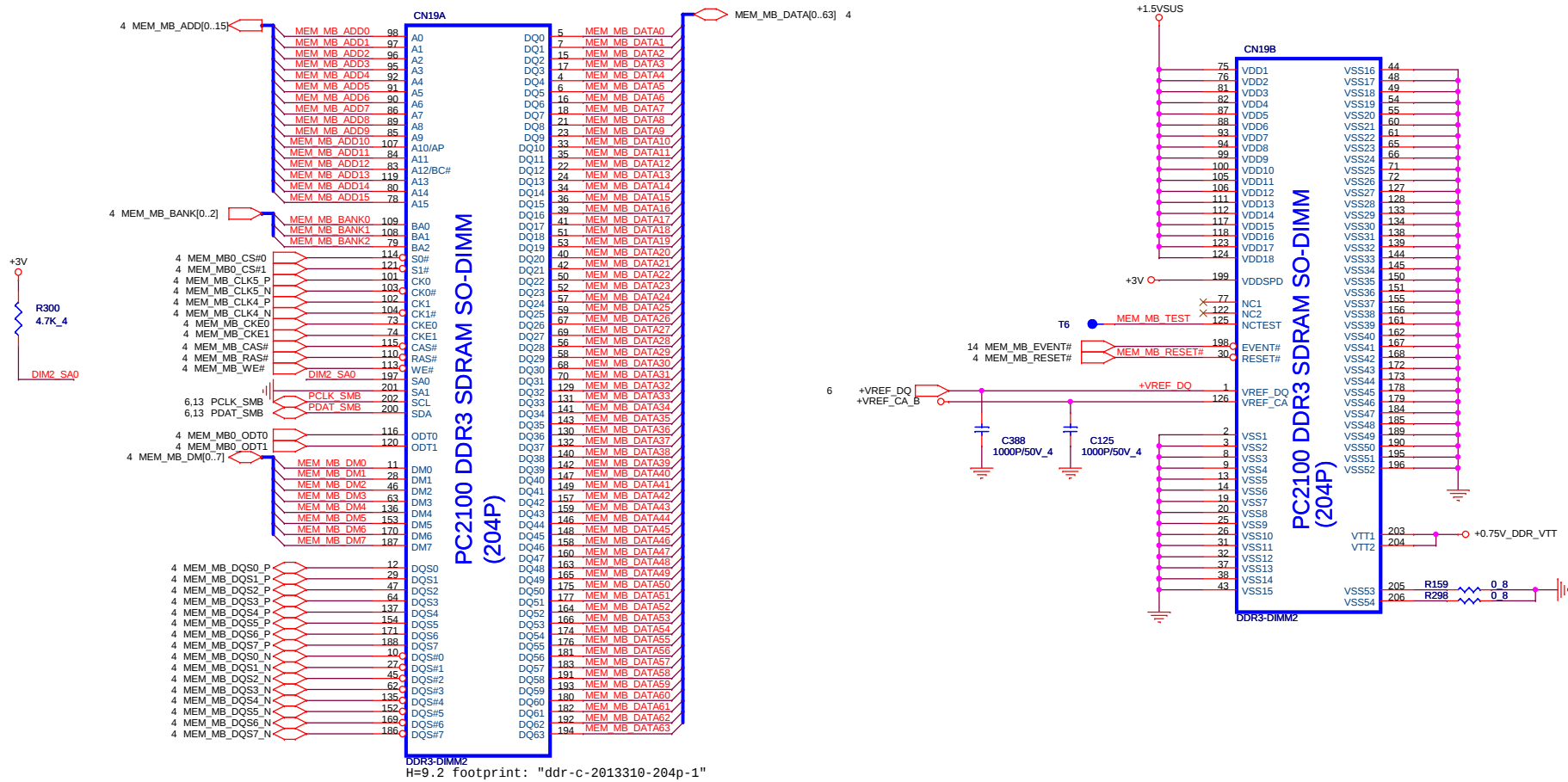
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

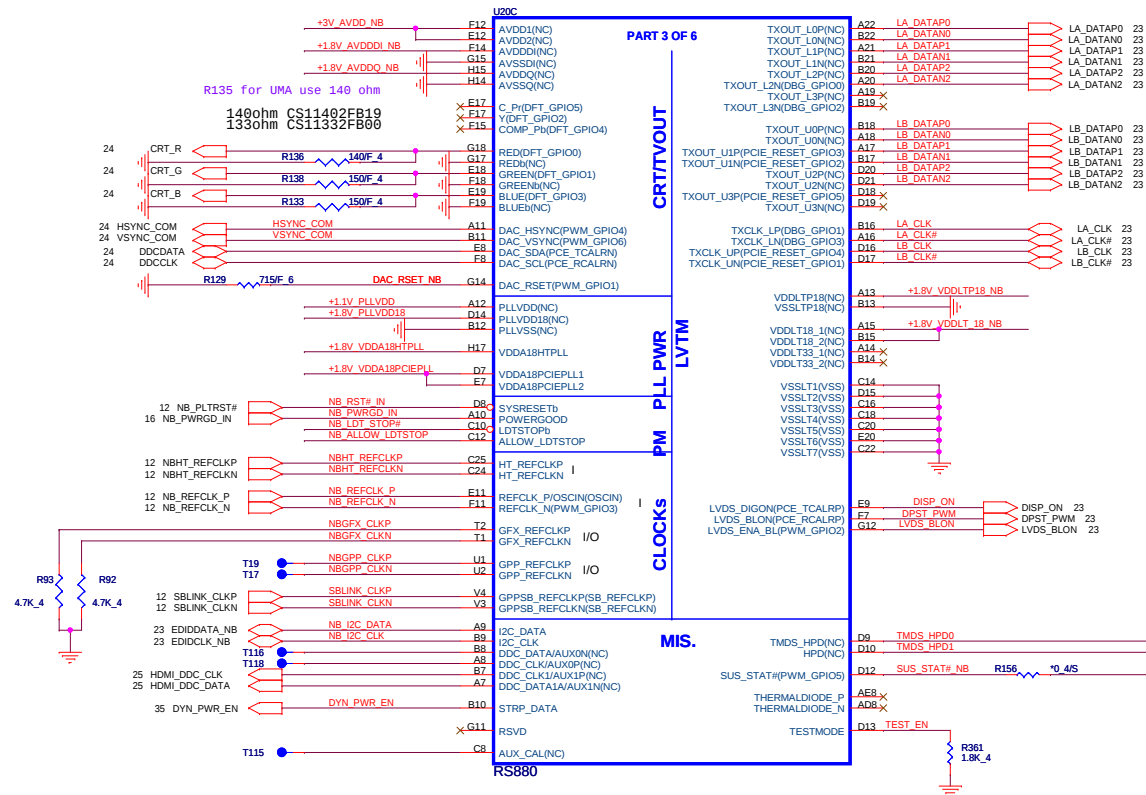
The diagram illustrates a decoupling circuit for DIMM1, showing a +1.5V supply connected to a series of capacitors (C588, C578, C550, C140, C272, C218, C552, C583, C557, C306, C245, C152) connected to ground. Each capacitor is labeled with its value: .1U/10V_4.



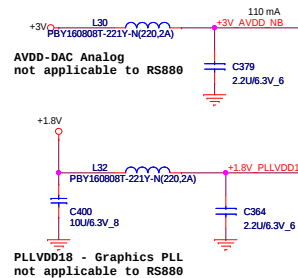








MUXLESS need add PLL power for LVDS



VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RS880

PLLVDD - Graphics PLL not applicable to RS880

AVDDI-DAC Digital not applicable to RS880

AVDDQ-DAC Bandgap Reference not applicable to RS880

VDDLTP18 - LVDS or DVI/HDMI digital not applicable to RS880

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	
0 Enable	



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



For external EEPROM Debug only

RS780/RX780

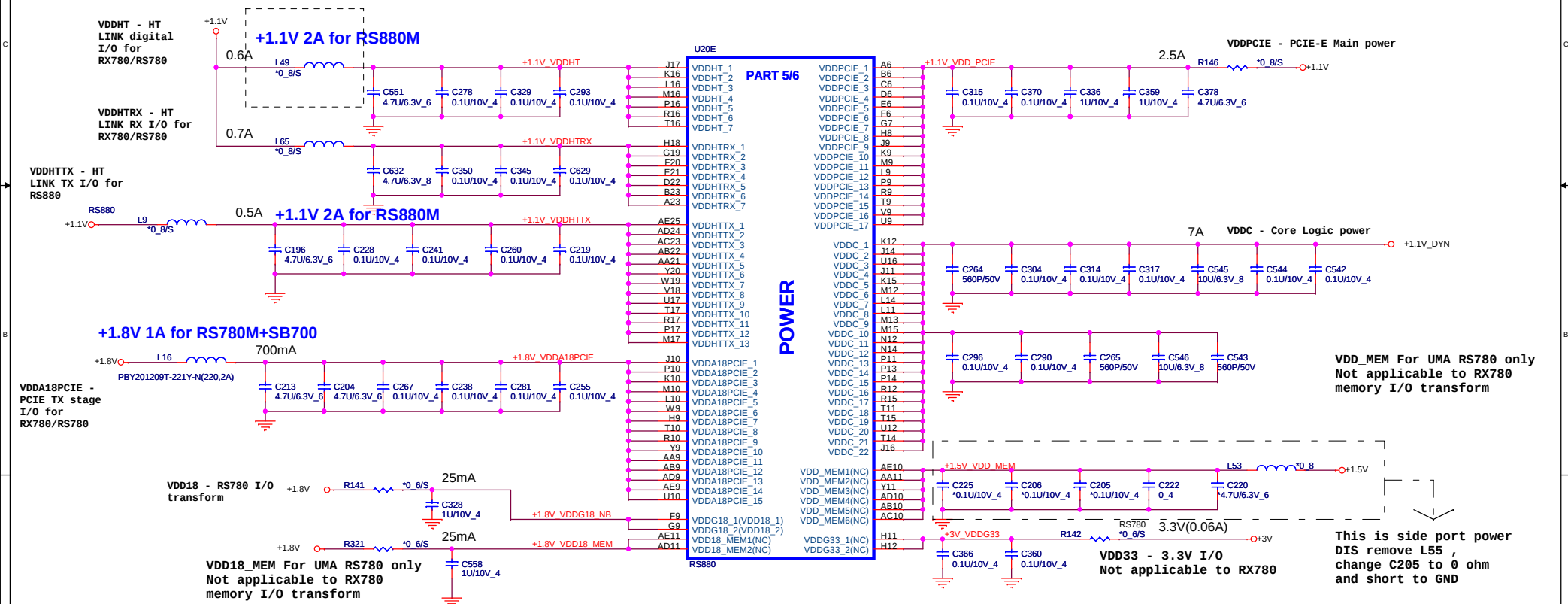
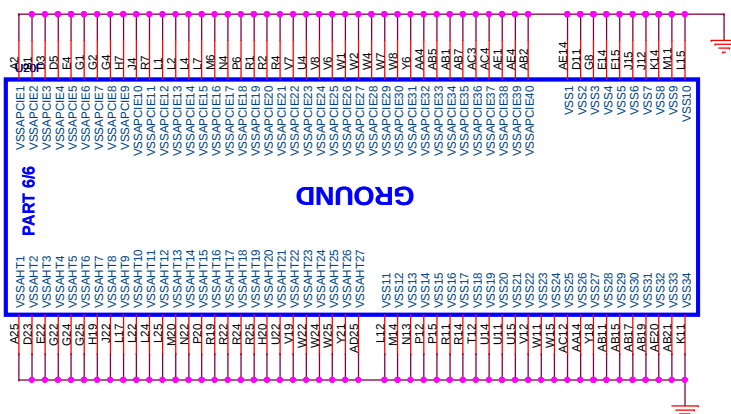


PROJECT : R22
Quanta Computer Inc.

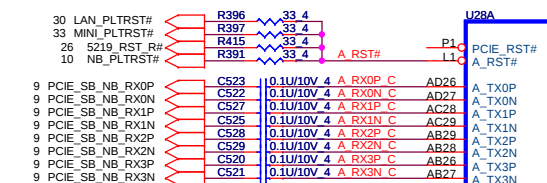
Size Custom	Document Number RS880-SYSTEM I/F 3/5	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 10 of 43	

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLT18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD18	+1.8V	VDDLT33	NC

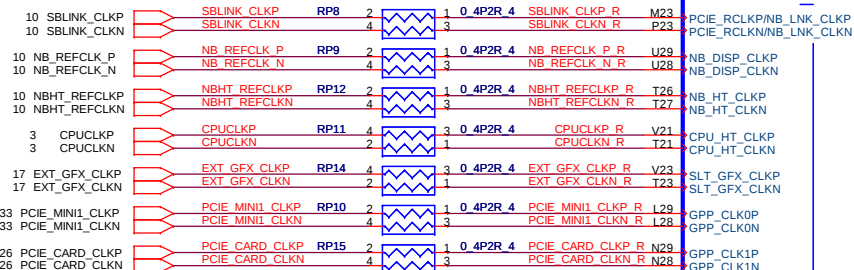


PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB

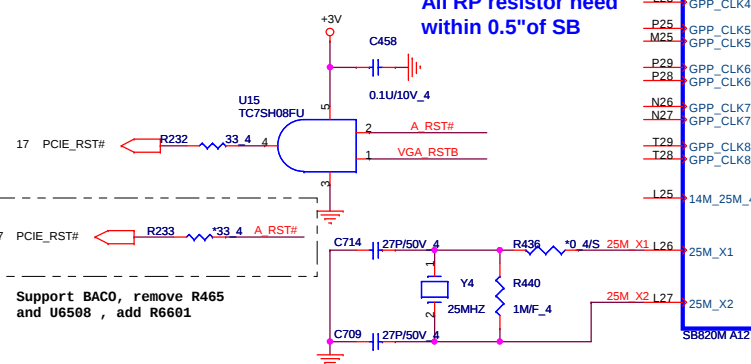


To RS880

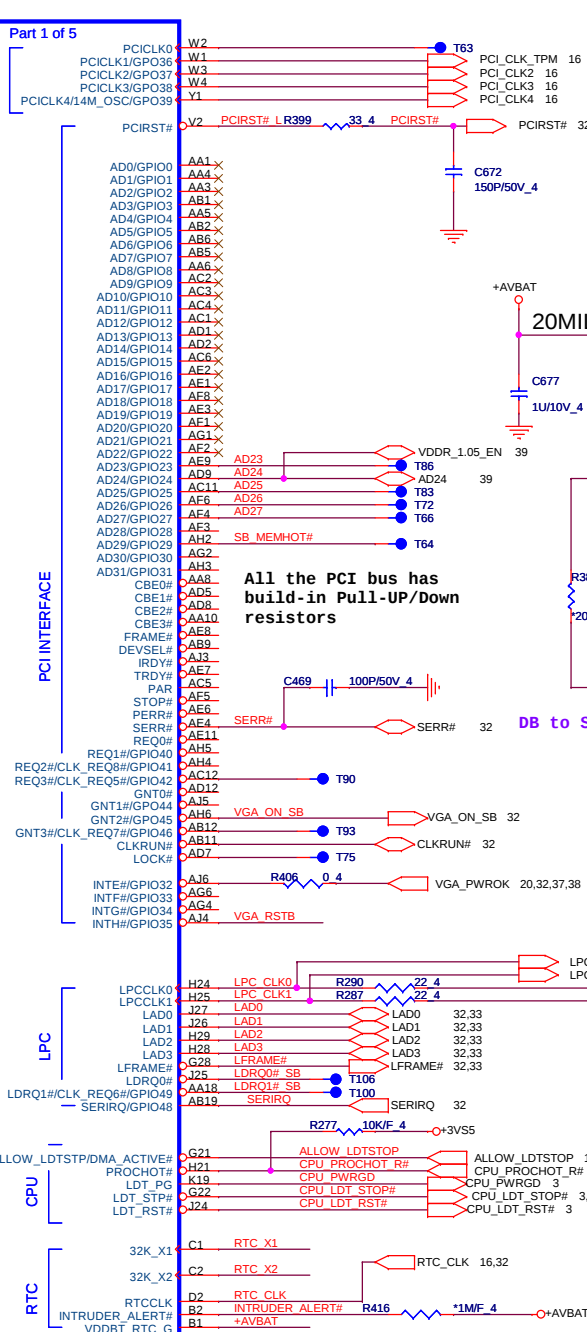
PCI EXPRESS INTERFACES



All RP resistor need
within 0.5" of SB



CLOCK GENERATOR



All the PCI bus has
build-in Pull-Up/Down
resistors

DB to SI Change C673,C675 to 33P

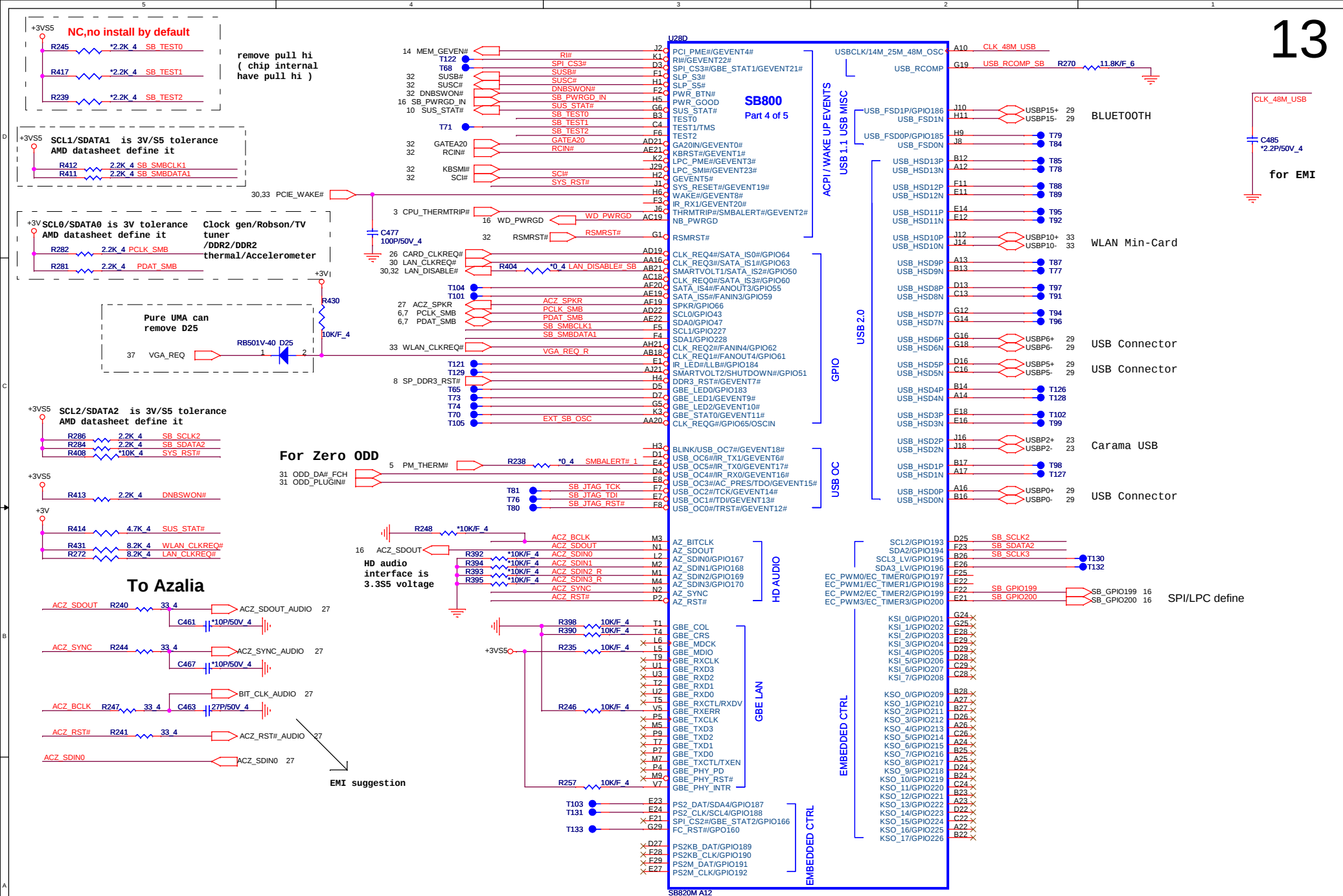
DB to SI CN27 Change PN
PN : DFWF02MS022
Footprint : 50273-0027N-001-2P-L

EMI suggestion



PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PCIE/PCI/CPU/LPC 1/4	1A
Date: Wednesday, September 15, 2010 Sheet 12 of 43		



SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SATA1

SATA ODD

PLVDD_SATA--
SATA PLL
POWER

XTLVDD_SATA-- SATA
crystal power



PLACE SATA CAL
RES VERY CLOSE
TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

+1.1V_AVDD_SATA

SB SATA LED#

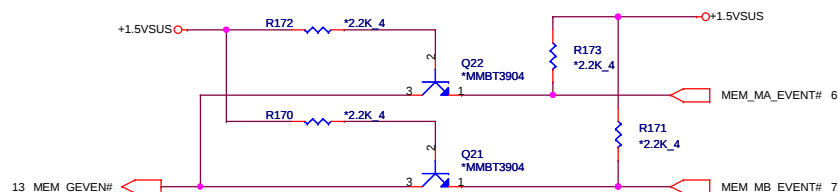
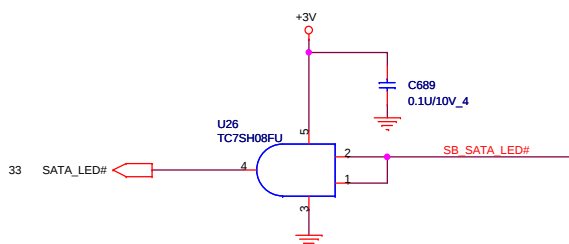
+3V R428 10K/F 4

T1 AD16 SATA_X1

T2 AC16 SATA_X2

T69 ROM_RST#

SB820M A12



SB800

Part 2 of 5

SERIAL ATA

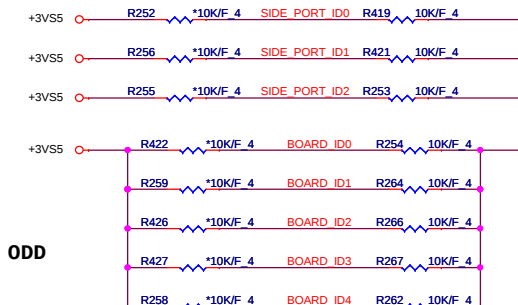
HW MONITOR

SPI ROM

Item	Board ID Hardware setting
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

Side port ID H/W setting



For Zero ODD

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	S6 / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



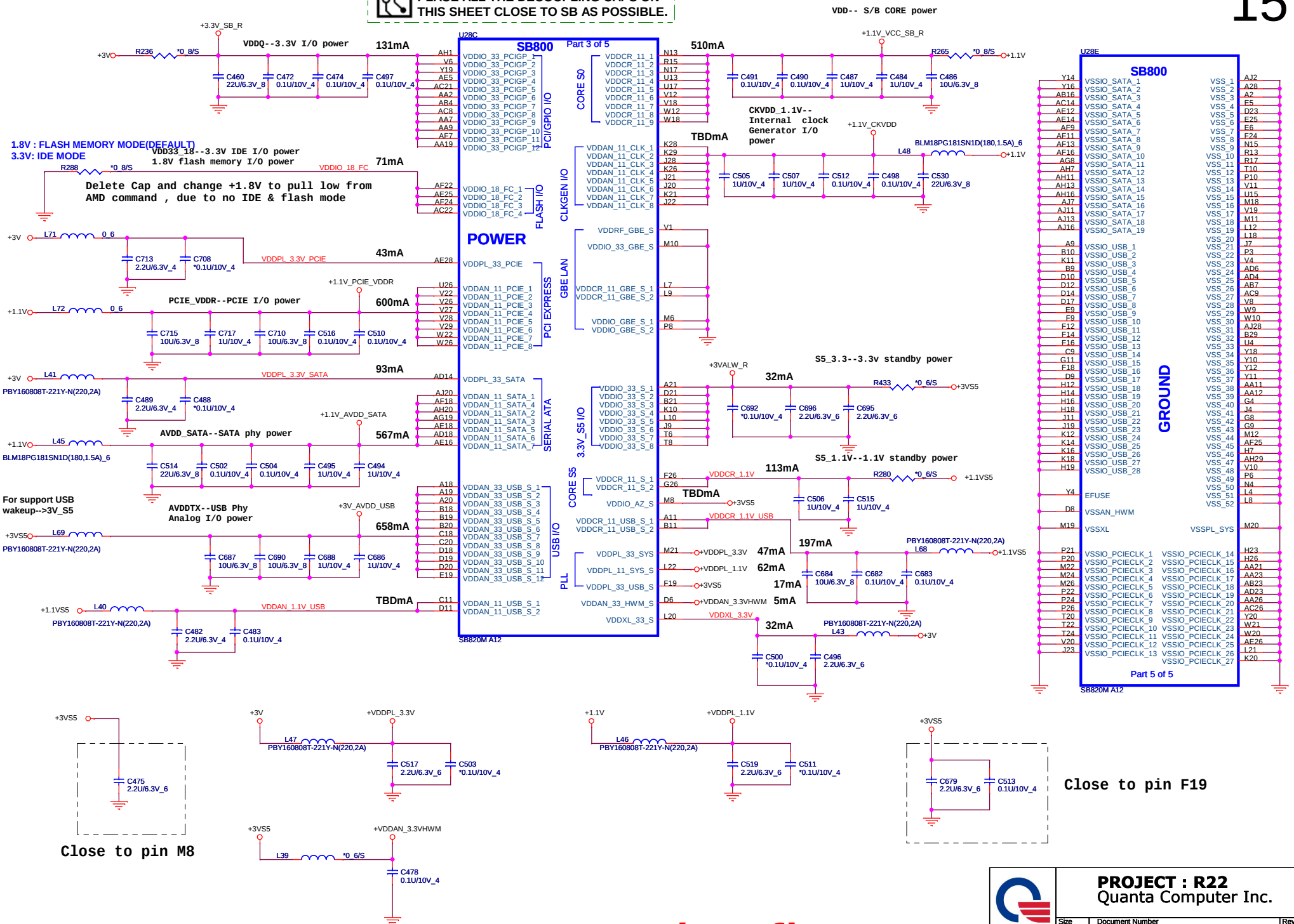
PROJECT : R22
Quanta Computer Inc.

Size Custom Document Number SB820-ACPI/GPIO/USB 2/4 Rev 1A
Date: Wednesday, September 15, 2010 Sheet 14 of 43



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

15

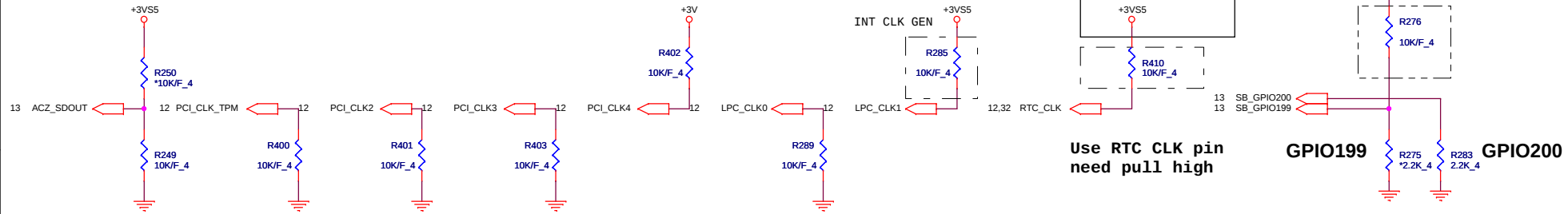




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

REQUIRED STRAPS



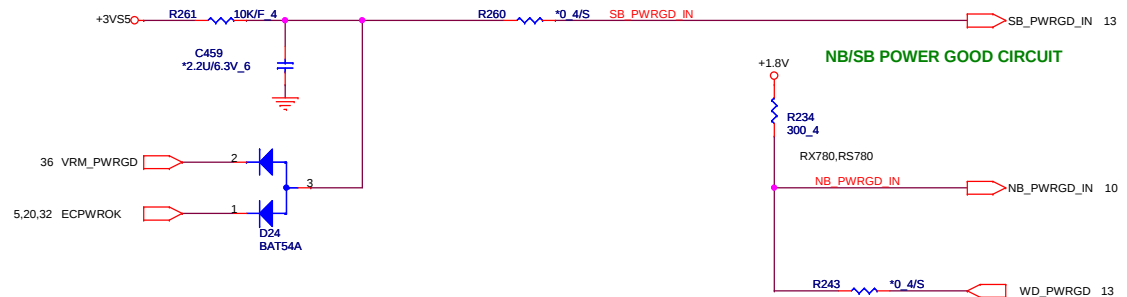
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

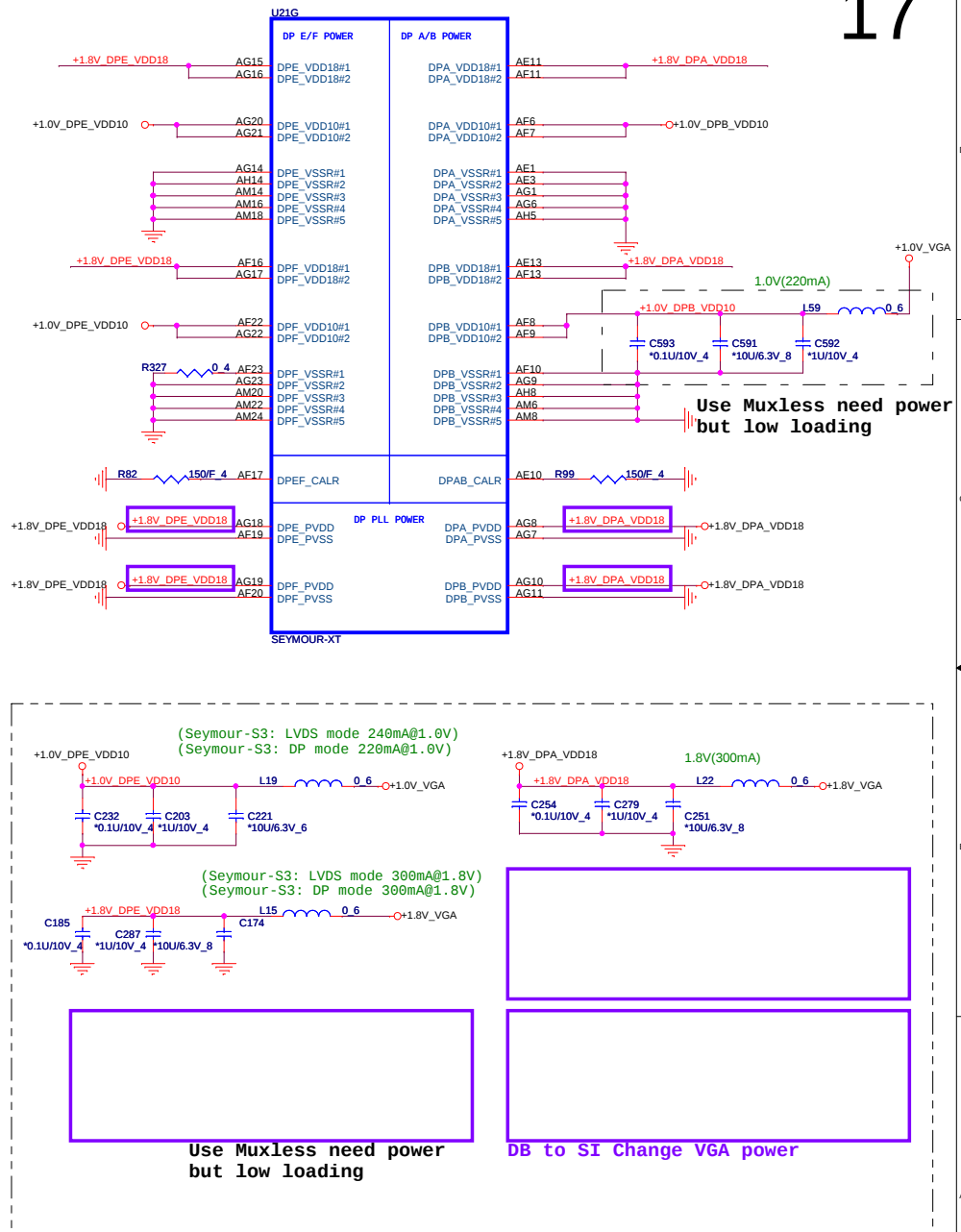
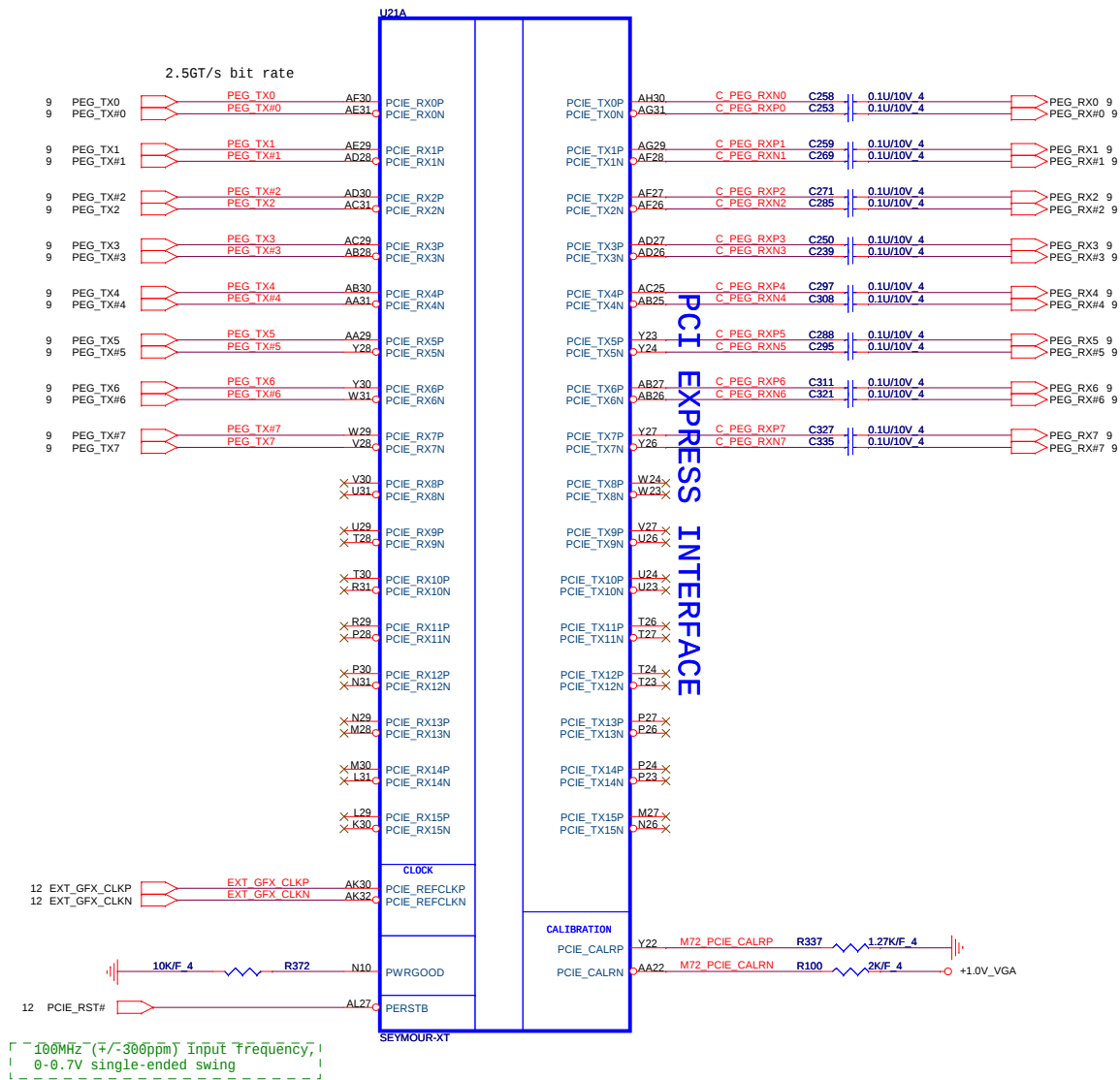
NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

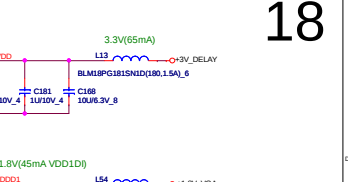
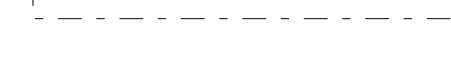
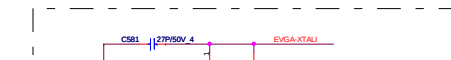
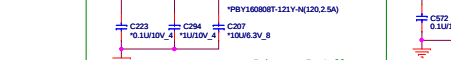
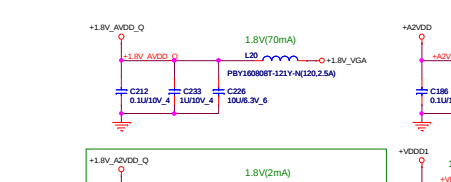
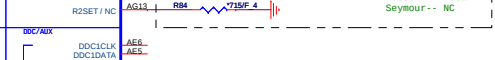
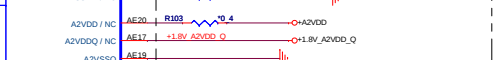
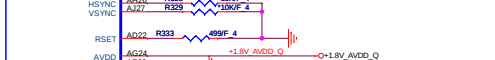
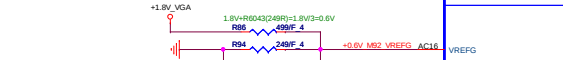
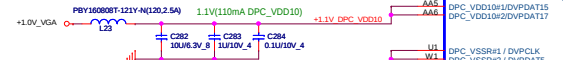
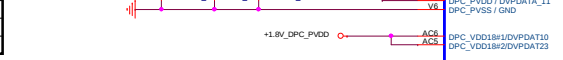
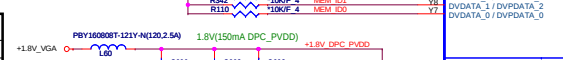
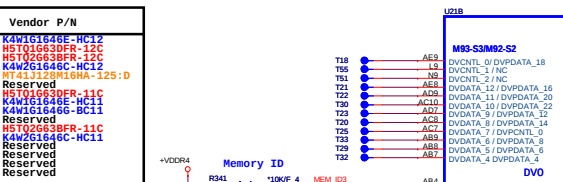
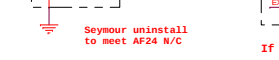
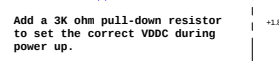
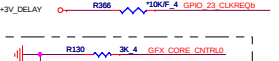
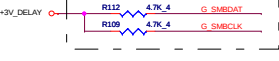
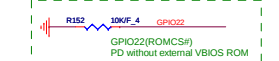
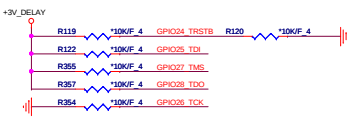
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

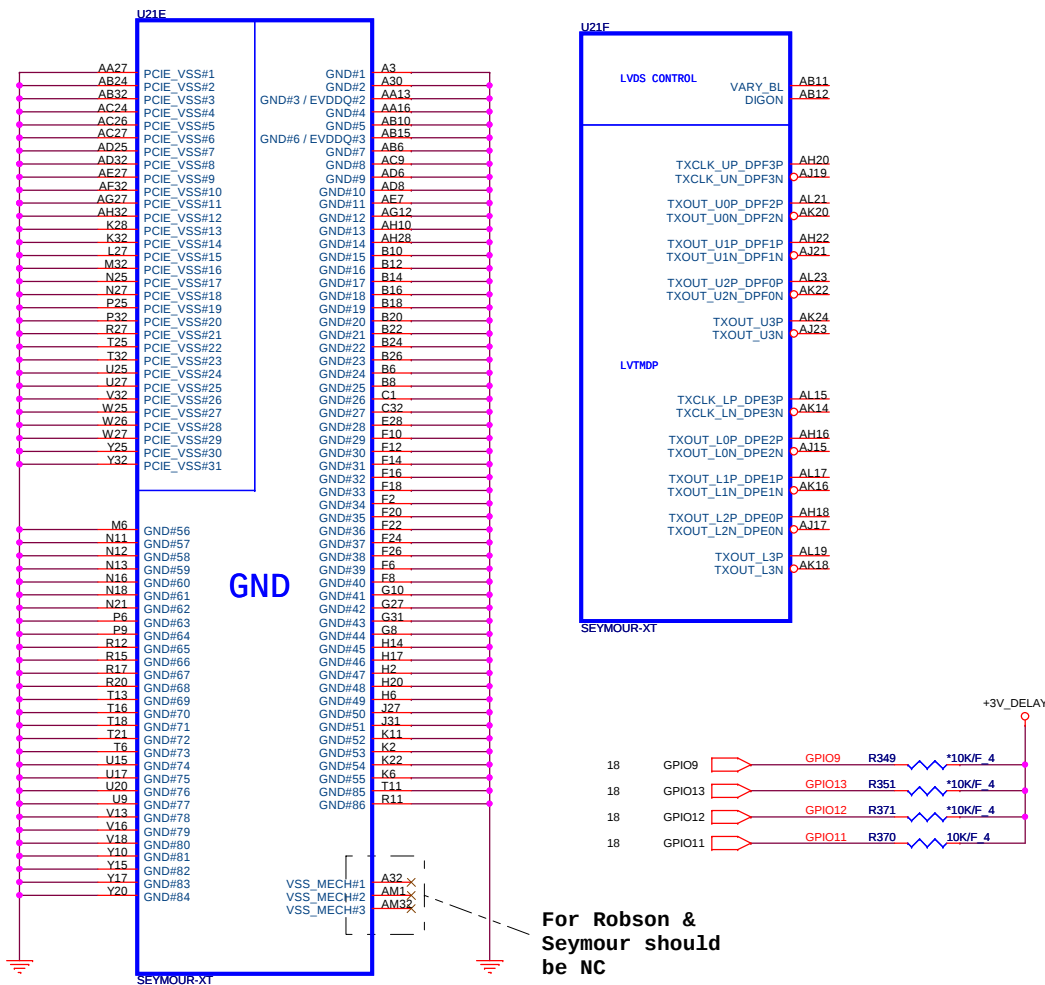
	PROJECT : R22	
	Quanta Computer Inc.	
	Size Custom	Document Number SB820-STRAPS
NB5/RD2	Date: Wednesday, September 15, 2010	Sheet 16 of 43
		Rev 1A



MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-NC12
0001	Hynix- Vega die	64*16-800MHZ	H5T01683DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5T02683DFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-NC12
0100	Reserved	Reserved	Reserved
0101	Hynix- Vega die	64*16-800MHZ	H5T01683DFR-11C
0110	Samsung- E die	64*16-800MHZ	K4W1G1646E-NC11
0111	Samsung- E die	64*16-800MHZ	K4W1G1646E-BC11
1000	Reserved	Reserved	Reserved
1001	Hynix- Vega die	128*16-800MHZ	H5T02683DFR-11C
1010	Samsung- C die	128*16-800MHZ	K4W2G1646C-NC11
1011	Reserved	Reserved	Reserved
1100	Reserved	Reserved	Reserved
1101	Reserved	Reserved	Reserved
1110	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved

MEM_ID[3:0]	31 Level BOM	H/W setting
0000	TBD	TBD
0001	TBD	TBD
0010	TBD	TBD
0011	TBD	TBD
0100	TBD	TBD





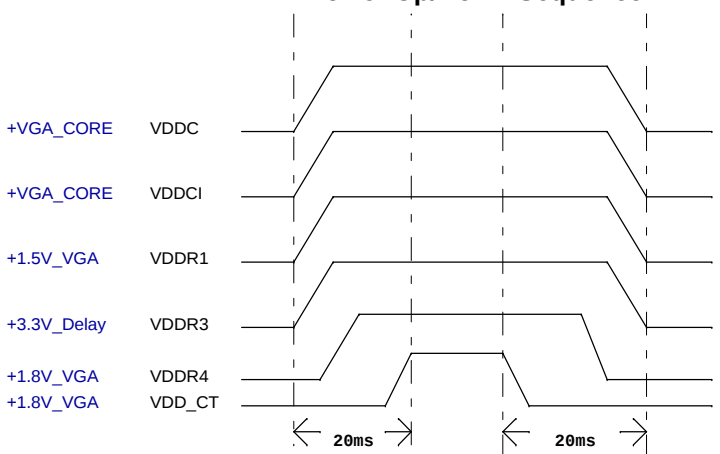
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYS	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2
--------	--------	----------	-------	-------

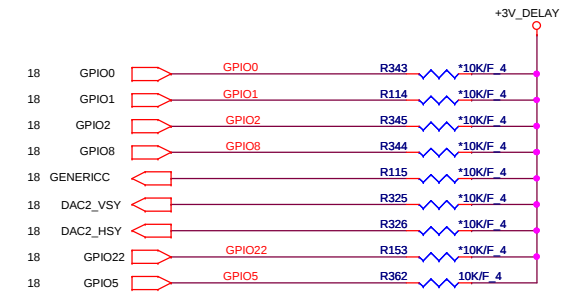
Power Up/Down Sequence



Memory Aperture size

GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	0
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : R22
Quantia Computer Inc.

Size Custom

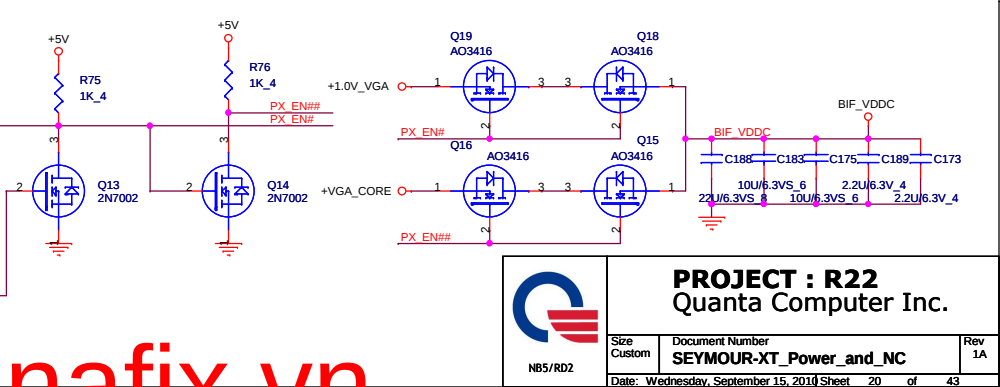
Document Number

SEYMOUR-XT GND / LVDS/ Straps

Rev 1A

Date: Wednesday, September 15, 2014

Sheet 19 of 43



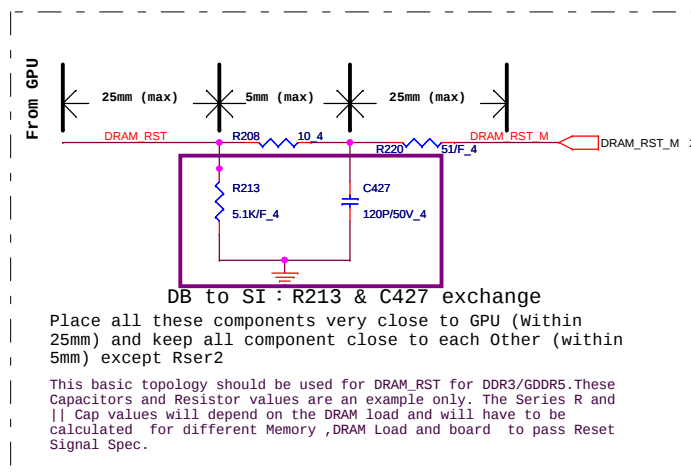
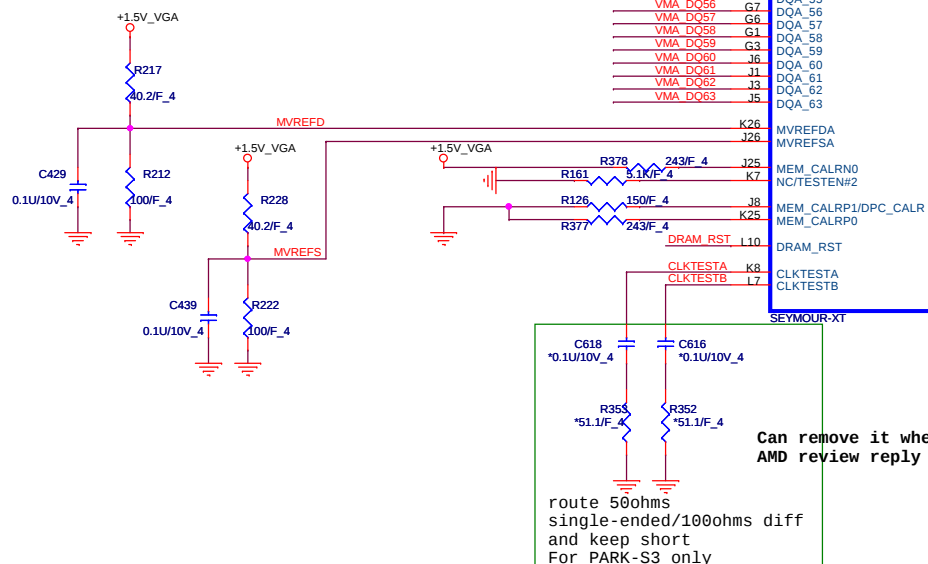
22	VMA_ODT0	VMA_ODT0
22	VMA_ODT1	VMA_ODT1
22	VMA_RAS0#	VMA_RAS0#
22	VMA_RAS1#	VMA_RAS1#
22	VMA_CAS0#	VMA_CAS0#
22	VMA_CAS1#	VMA_CAS1#
22	VMA_WE0#	VMA_WE0#
22	VMA_WE1#	VMA_WE1#
22	VMA_CS0#	VMA_CS0#
22	VMA_CS1#	VMA_CS1#
22	VMA_CKE0	VMA_CKE0
22	VMA_CKE1	VMA_CKE1
22	VMA_CLK0	VMA_CLK0
22	VMA_CLK0#	VMA_CLK0#
22	VMA_CLK1	VMA_CLK1
22	VMA_CLK1#	VMA_CLK1#
22	VMA_WDQS[7..0]	VMA_WDQS[7..0]
22	VMA_RDQS[7..0]	VMA_RDQS[7..0]
22	VMA_DM[7..0]	VMA_DM[7..0]
22	VMA_DQ[63..0]	VMA_DQ[63..0]
22	VMA_MA[13..0]	VMA_MA[13..0]
22	VMA_BA0	VMA_BA0
22	VMA_BA1	VMA_BA1
22	VMA_BA2	VMA_BA2

support 16bit
VRAM (64M X 16)

VMA_DQ0	K27	DQA_0
VMA_DQ1	J29	DQA_1
VMA_DQ2	H30	DQA_2
VMA_DQ3	H32	DQA_3
VMA_DQ4	G29	DQA_4
VMA_DQ5	F28	DQA_5
VMA_DQ6	F32	DQA_6
VMA_DQ7	F30	DQA_7
VMA_DQ8	C30	DQA_8
VMA_DQ9	F27	DQA_9
VMA_DQ10	A28	DQA_10
VMA_DQ11	C28	DQA_11
VMA_DQ12	E27	DQA_12
VMA_DQ13	D24	DQA_13
VMA_DQ14	G26	DQA_14
VMA_DQ15	F25	DQA_15
VMA_DQ16	A25	DQA_16
VMA_DQ17	C25	DQA_17
VMA_DQ18	E25	DQA_18
VMA_DQ19	D24	DQA_19
VMA_DQ20	E23	DQA_20
VMA_DQ21	E23	DQA_21
VMA_DQ22	D22	DQA_22
VMA_DQ23	F21	DQA_23
VMA_DQ24	E21	DQA_24
VMA_DQ25	D20	DQA_25
VMA_DQ26	F19	DQA_26
VMA_DQ27	A19	DQA_27
VMA_DQ28	D18	DQA_28
VMA_DQ29	F17	DQA_29
VMA_DQ30	A17	DQA_30
VMA_DQ31	C17	DQA_31
VMA_DQ32	E17	DQA_32
VMA_DQ33	D16	DQA_33
VMA_DQ34	F15	DQA_34
VMA_DQ35	A15	DQA_35
VMA_DQ36	D14	DQA_36
VMA_DQ37	F13	DQA_37
VMA_DQ38	A13	DQA_38
VMA_DQ39	C13	DQA_39
VMA_DQ40	E11	DQA_40
VMA_DQ41	A11	DQA_41
VMA_DQ42	C11	DQA_42
VMA_DQ43	F11	DQA_43
VMA_DQ44	A9	DQA_44
VMA_DQ45	C9	DQA_45
VMA_DQ46	F9	DQA_46
VMA_DQ47	D8	DQA_47
VMA_DQ48	A7	DQA_48
VMA_DQ49	C7	DQA_49
VMA_DQ50	F7	DQA_50
VMA_DQ51	A5	DQA_51
VMA_DQ52	C5	DQA_52
VMA_DQ53	F5	DQA_53
VMA_DQ54	D3	DQA_54
VMA_DQ55	E1	DQA_55
VMA_DQ56	G7	DQA_56
VMA_DQ57	G6	DQA_57
VMA_DQ58	G1	DQA_58
VMA_DQ59	G3	DQA_59
VMA_DQ60	J6	DQA_60
VMA_DQ61	J1	DQA_61
VMA_DQ62	J3	DQA_62
VMA_DQ63	J5	DQA_63

MEMORY INTERFACE

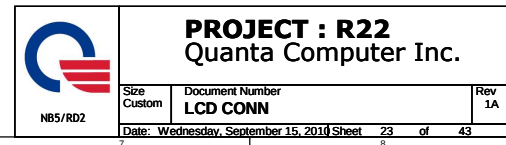
MAA_0	K17	VMA_MA0
MAA_1	J20	VMA_MA1
MAA_2	H23	VMA_MA2
MAA_3	G23	VMA_MA3
MAA_4	G24	VMA_MA4
MAA_5	H24	VMA_MA5
MAA_6	J19	VMA_MA6
MAA_7	K19	VMA_MA7
MAA_8	K14	VMA_MA8
MAA_9	J11	VMA_MA9
MAA_10	J13	VMA_MA10
MAA_11	H11	VMA_MA11
MAA_12	G11	VMA_MA12
MAA_13/BA2	J16	VMA_BA0
MAA_14/BA0	L15	VMA_BA1
MAA_15/BA1		
DQMA_0	E32	VMA_DM0
DQMA_1	E30	VMA_DM1
DQMA_2	A21	VMA_DM2
DQMA_3	C21	VMA_DM3
DQMA_4	E13	VMA_DM4
DQMA_5	D12	VMA_DM5
DQMA_6	E3	VMA_DM6
DQMA_7	F4	VMA_DM7
RDQSA_0	H28	VMA_RDQS0
RDQSA_1	C27	VMA_RDQS1
RDQSA_2	A23	VMA_RDQS2
RDQSA_3	E19	VMA_RDQS3
RDQSA_4	E15	VMA_RDQS4
RDQSA_5	D10	VMA_RDQS5
RDQSA_6	D6	VMA_RDQS6
RDQSA_7	G5	VMA_RDQS7
WDQSA_0	H27	VMA_WDQS0
WDQSA_1	A27	VMA_WDQS1
WDQSA_2	C23	VMA_WDQS2
WDQSA_3	C19	VMA_WDQS3
WDQSA_4	C15	VMA_WDQS4
WDQSA_5	E9	VMA_WDQS5
WDQSA_6	C5	VMA_WDQS6
WDQSA_7	H4	VMA_WDQS7
ODTA0	L18	VMA_ODT0
ODTA1	K16	VMA_ODT1
CLKA0	H26	VMA_CLK0
CLKA0B	H25	VMA_CLK0#
CLKA1	G9	VMA_CLK1
CLKA1B	H9	VMA_CLK1#
RASA0B	G22	VMA_RAS0#
RASA1B	G17	VMA_RAS1#
CASA0B	G19	VMA_CAS0#
CASA1B	G16	VMA_CAS1#
CSA0B_0	H22	VMA_CS0#
CSA0B_1	J22	
CSA1B_0	G13	VMA_CS1#
CSA1B_1	K13	
CKEA0	K20	VMA_CKE0
CKEA1	J17	VMA_CKE1
WEA0B	G25	VMA_WE0#
WEA1B	H10	VMA_WE1#
PX_EN	AB16	
RSVD#2	G14	VMA_MA13
RSVD#3	G20	



PROJECT : R22
Quanta Computer Inc.

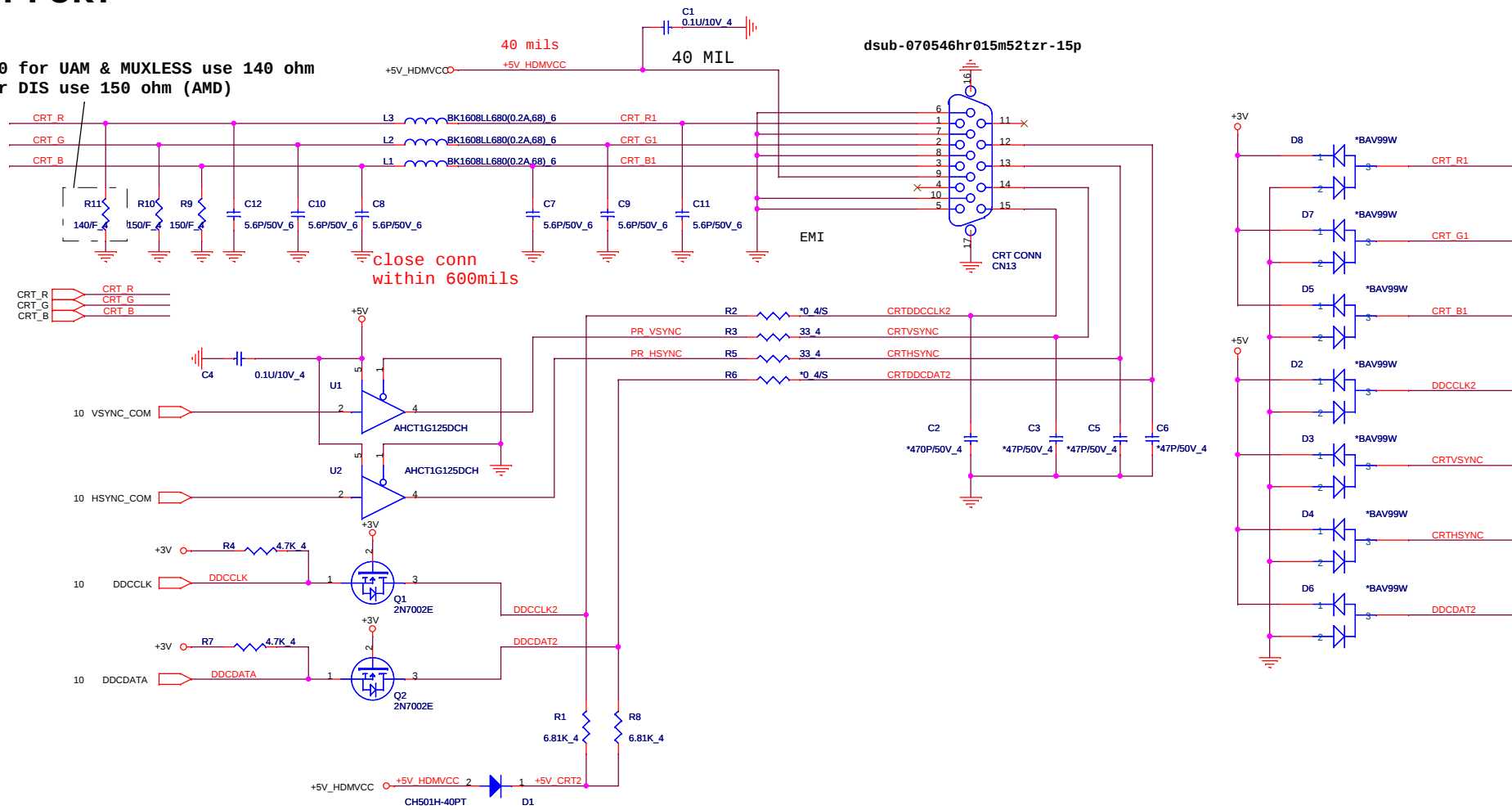
Size Custom	Document Number SEYMOUR-XT MEM Interface	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 21	of 43





CRT PORT

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)

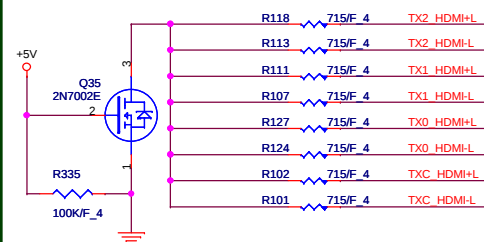


UMA/DISCRETE select for HDMI

From RS880M

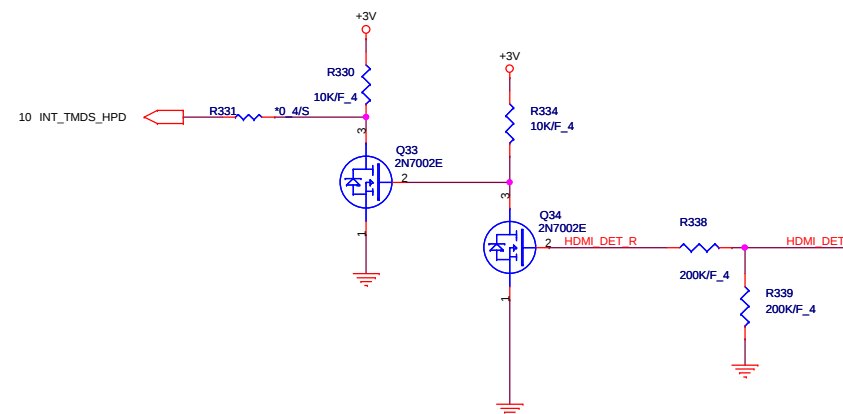
for Layout
concern
,placement close
north bridge

9	C_PEG_TX15	C_PEG_TX15	C625	0.1U/10V_4	TX2 HDMI-L
9	C_PEG_TX#15	C_PEG_TX#15	C626	0.1U/10V_4	TX2 HDMI+L
9	C_PEG_TX14	C_PEG_TX14	C623	0.1U/10V_4	TX1 HDMI-L
9	C_PEG_TX#14	C_PEG_TX#14	C624	0.1U/10V_4	TX1 HDMI+L
9	C_PEG_TX#13	C_PEG_TX#13	C620	0.1U/10V_4	TX0 HDMI-L
9	C_PEG_TX13	C_PEG_TX13	C622	0.1U/10V_4	TX0 HDMI+L
9	C_PEG_TX#12	C_PEG_TX#12	C615	0.1U/10V_4	TXC HDMI-L
9	C_PEG_TX12	C_PEG_TX12	C617	0.1U/10V_4	TXC HDMI+L

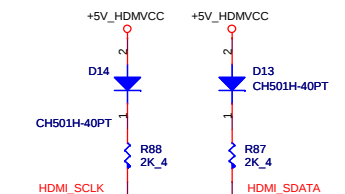


Close to HDMI Connector

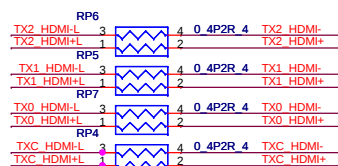
HDMI HPD SENSE



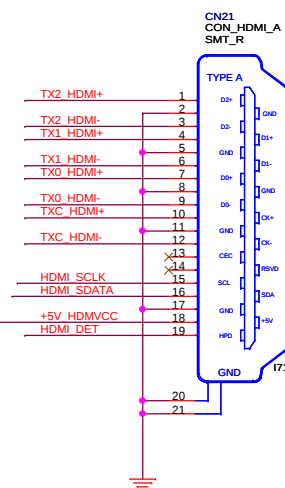
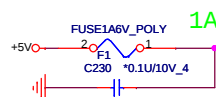
HDMI Connector



Add for EMI debug



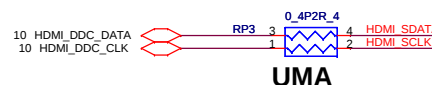
Need add nearby HDMI CONN



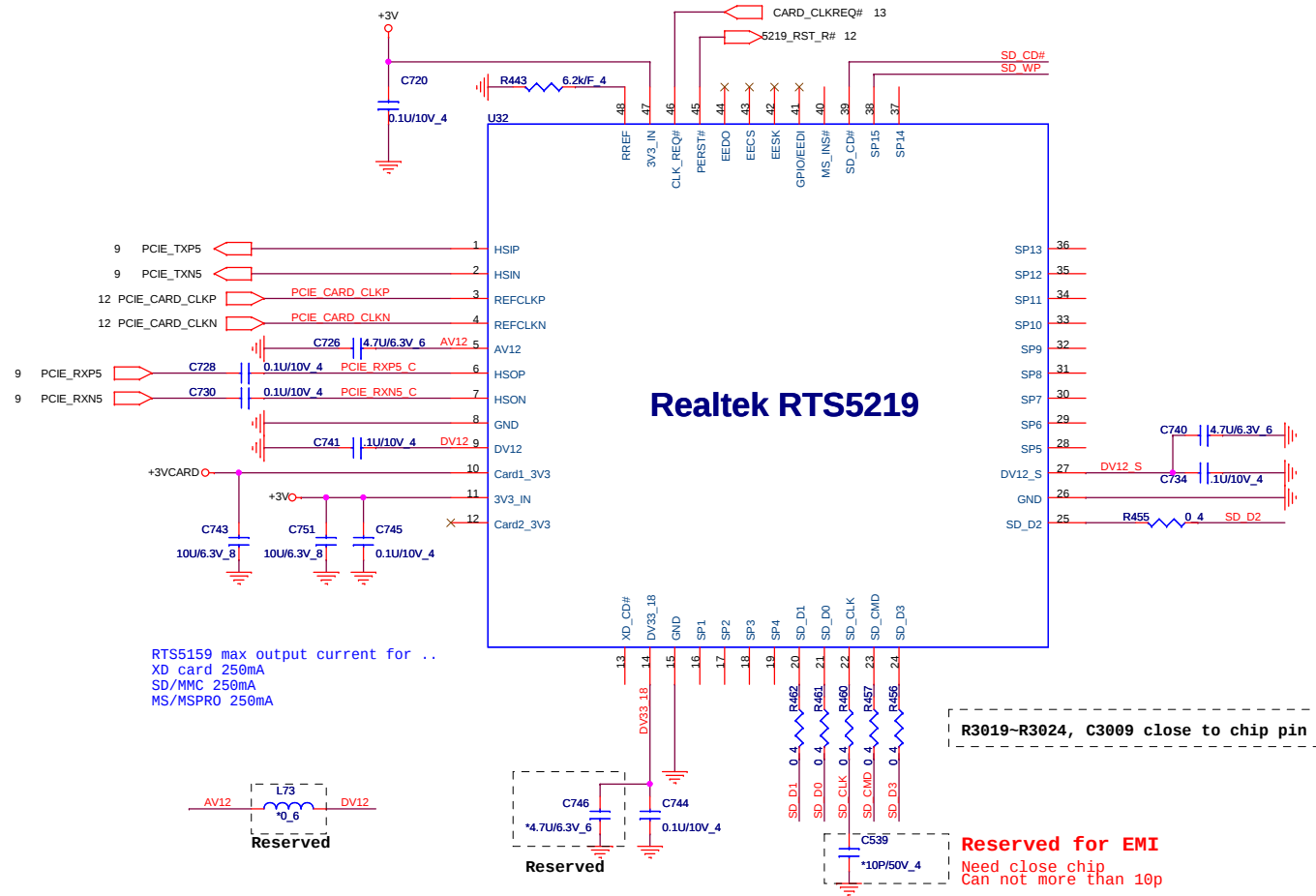
hdmi-100042mr019s172z1-19p-v

UMA HDMI I2C SELECT

Close to HDMI Connector

PROJECT : R22
Quanta Computer Inc.

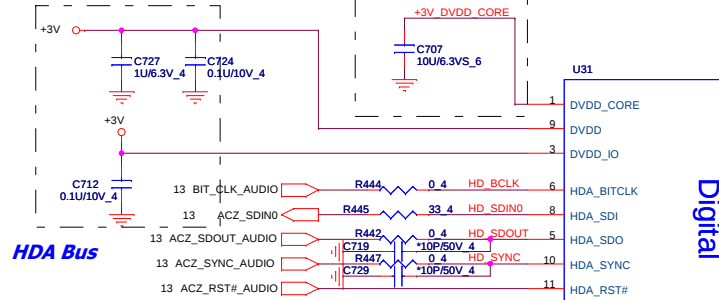
Size Custom	Document Number HDMI	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 25	of 43



3,5,6,7,10,11,12,13,14,15,16,20,23,24,25,26,28,29,30,31,32,33,38,39 +3V
+4.75VAVDD
5,20,23,24,25,28,29,31,33,39 +5V

Close to CODEC

Close to CODEC

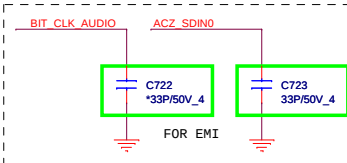
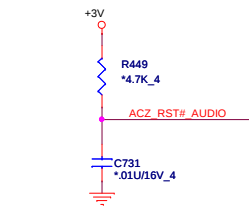


TO Digital MIC

Digital

Close to CODEC

Analog



SI, check BIT_CLK_AUDIO
double pull low

>40mils trace

Close to CODEC

Close to CODEC

TO Headphone jack

TO Audio Jack MIC

TO Internal Speakers

C10625 close C10629, and C10625
close chip

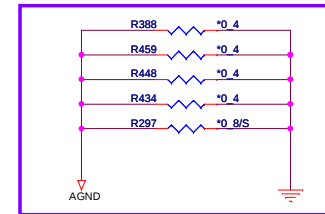
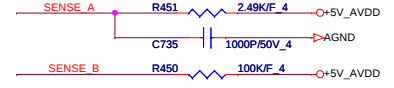
Check layout
mount location

EMI Request

INT. SPEAKER



DB to SI : 9/14 for IDT recommend



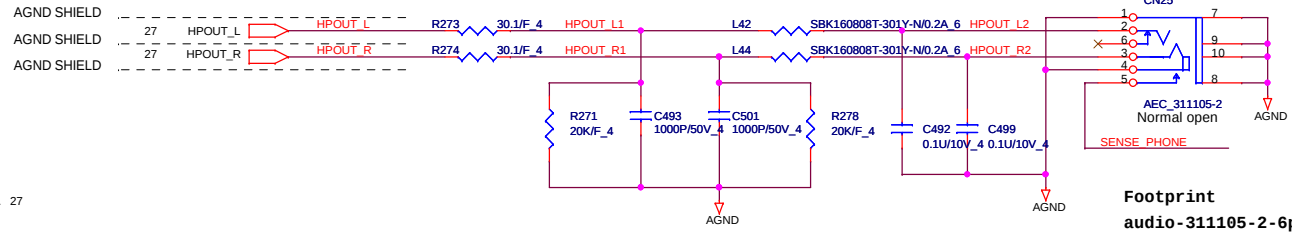
DB to SI : Reverse For EMI & ESD



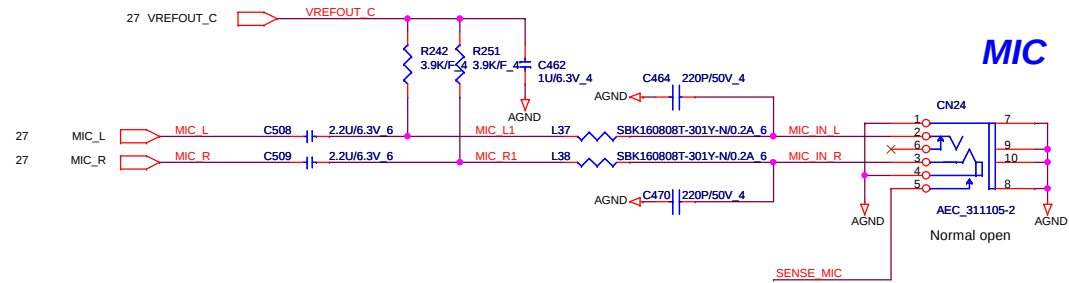
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number Azalia 92HD80	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 27 of 43		

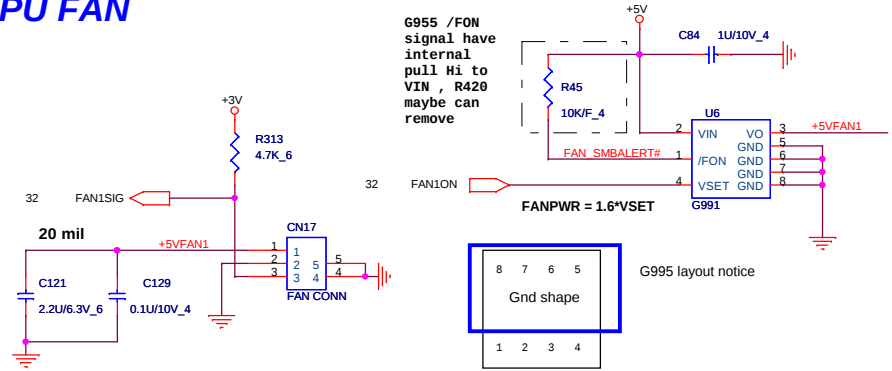
Line out



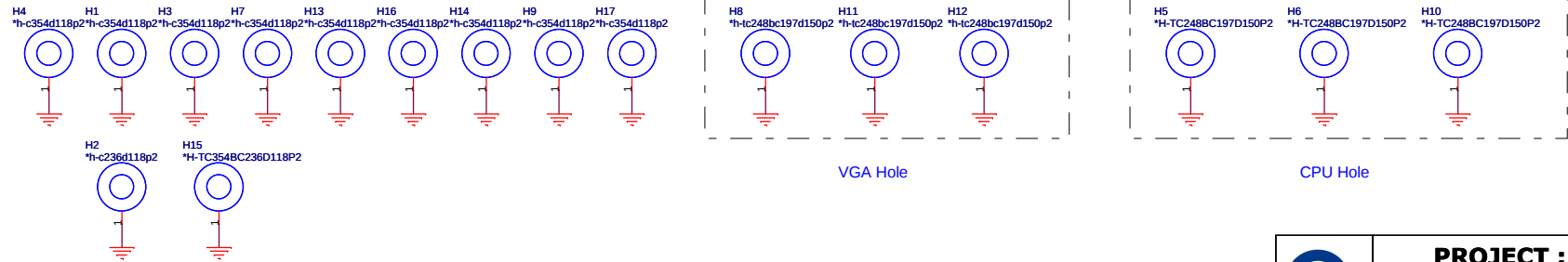
MIC



CPU FAN



HOLE



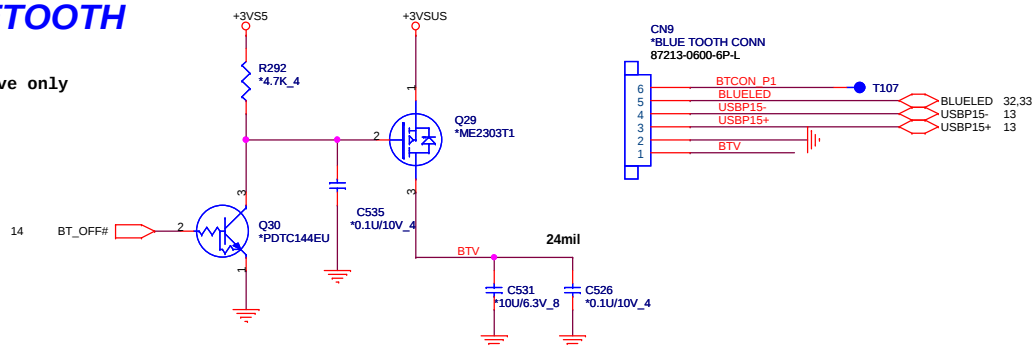
PROJECT : R22
Quanta Computer Inc.

Size Custom Document Number AMP_TPA6017/CPU FAN/HOLE Rev 1A

Date: Wednesday, September 15, 2010 Sheet 28 of 43

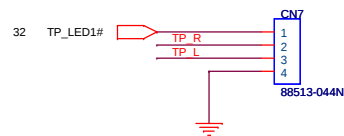
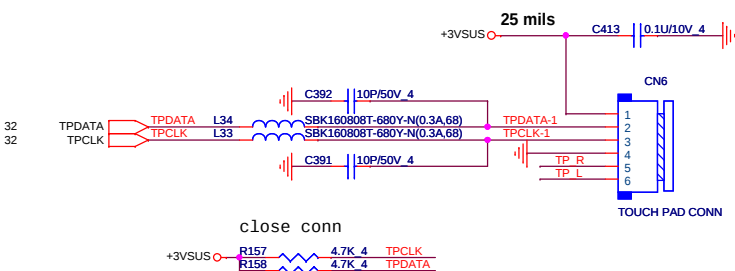
BLUETOOTH

Reserve only

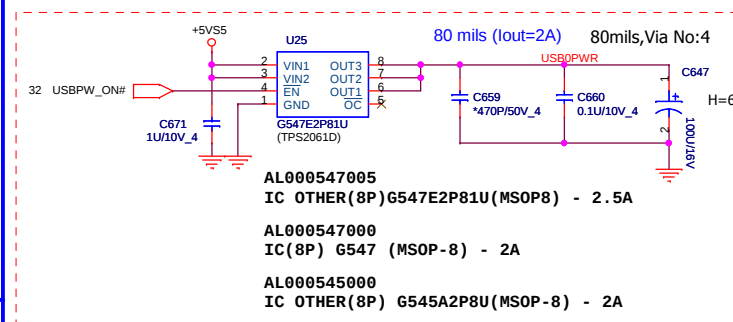


TOUCH PAD CONN

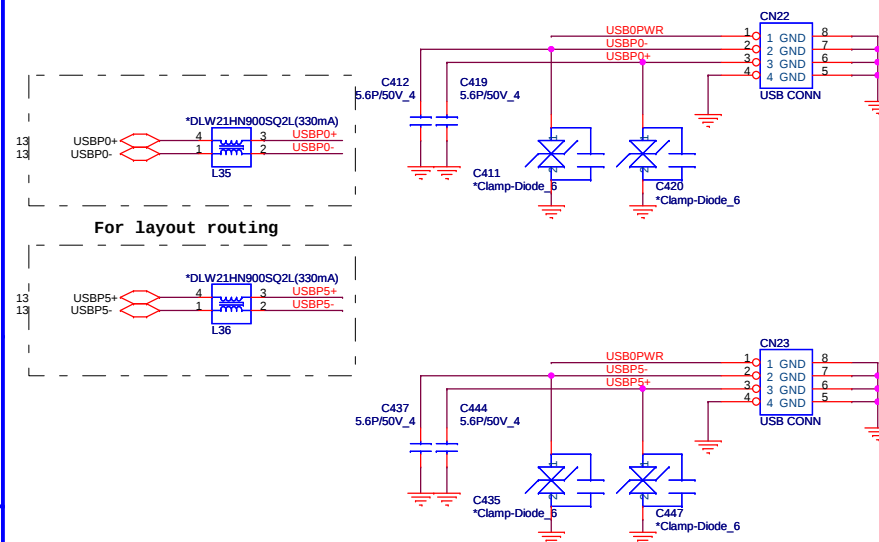
To TOUCH
PAD SW board



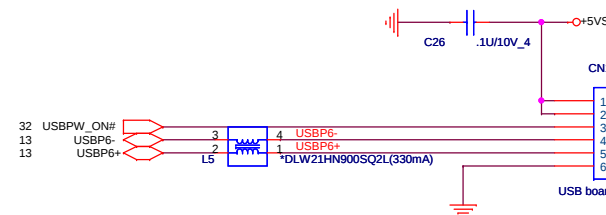
LEFT SIDE USBX2



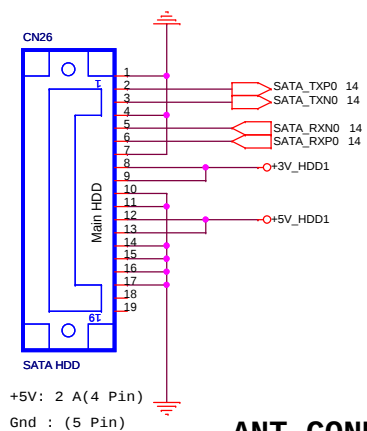
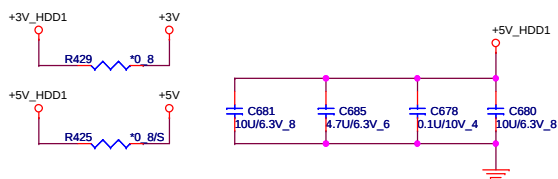
AL000547005
IC OTHER(8P)G547E2P81U(MSOP8) - 2.5A
AL000547000
IC(8P) G547 (MSOP-8) - 2A
AL000545000
IC OTHER(8P) G545A2P8U(MSOP-8) - 2A



Right SIDE USBX1



SATA HDD CONNECTOR

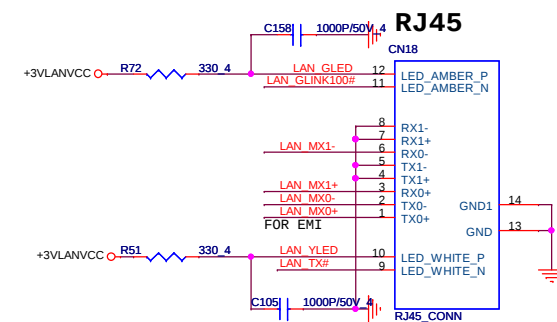
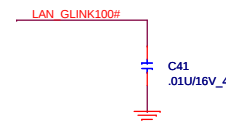
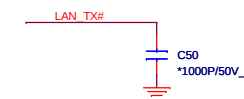
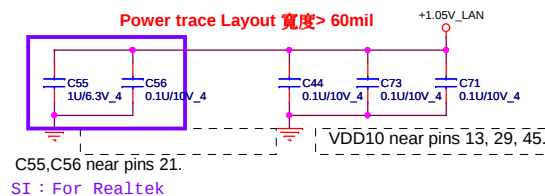


ANT CONN

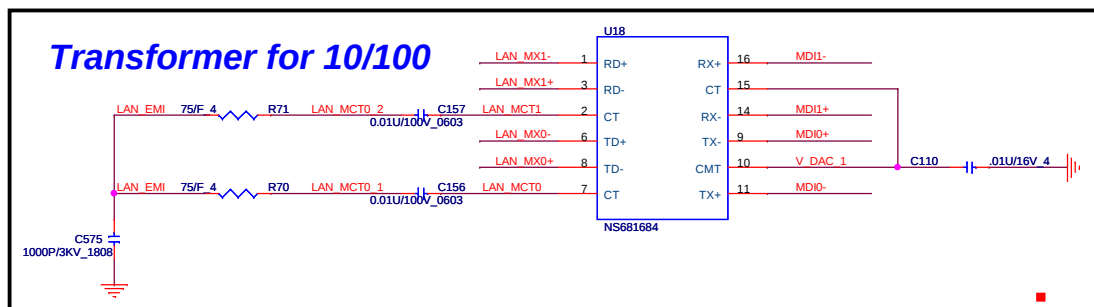


PROJECT : R22
Quanta Computer Inc.

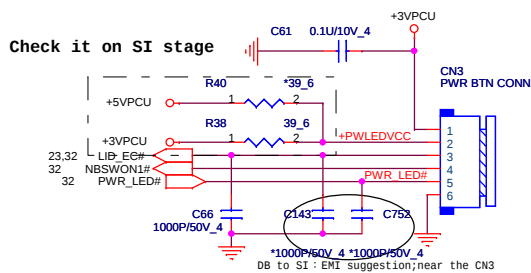
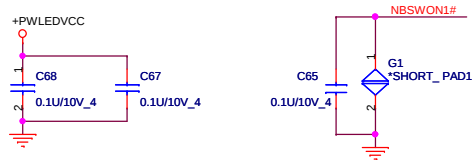
Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 29 of 43		



Footprint : rj45-130452-u4-12p

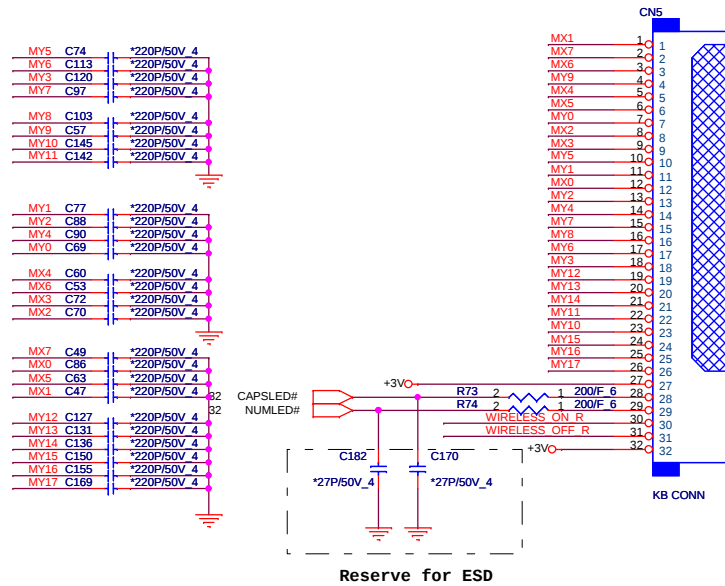


POWER BUTTON CONNECTOR

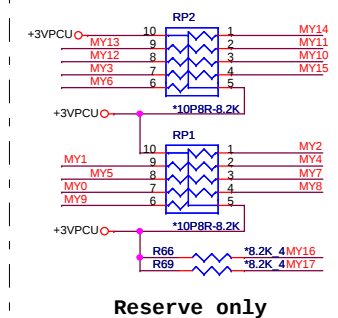


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD CONN

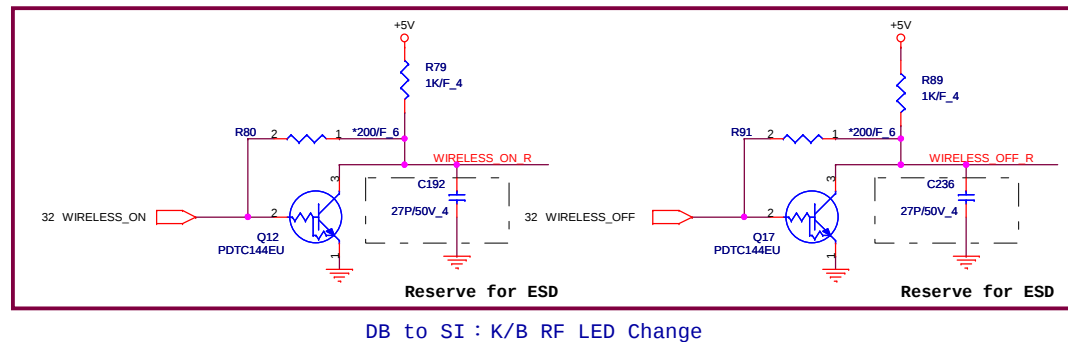
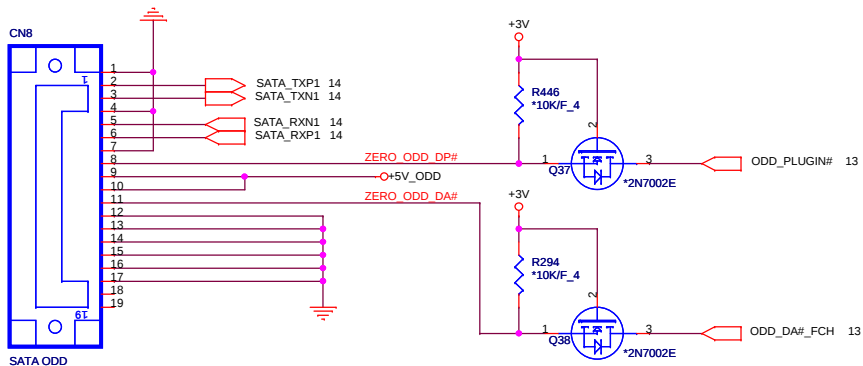


KEYBOARD PULL-UP



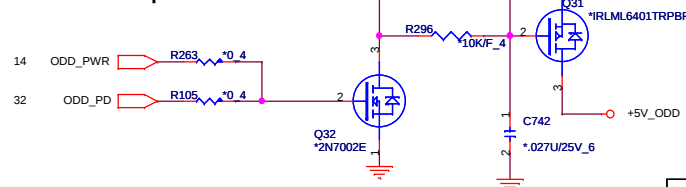
SATA CD-ROM

ANT CONN



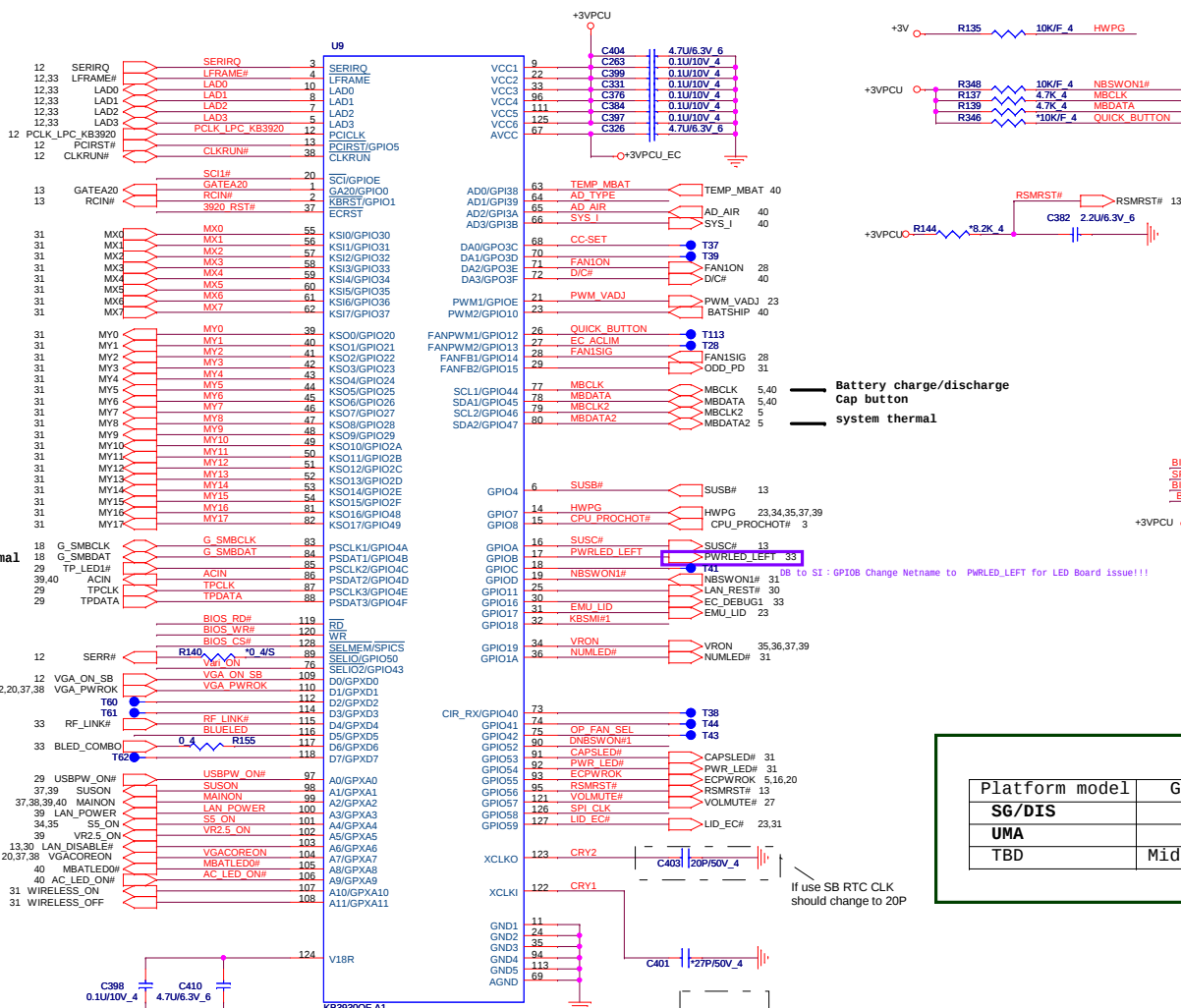
Zero Power ODD circuit

High : ODD power on
Low : ODD power down

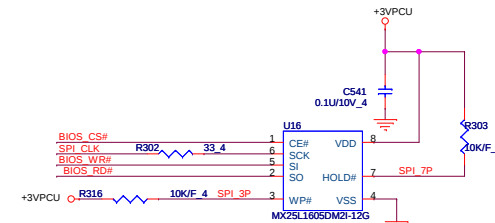


PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KEYBOARD/SW_BOARD/ODD	1A
Date: Wednesday, September 15, 2010	Sheet 31	of 43

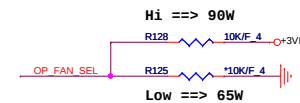


Battery charge/discharge
Cap button
system thermal



MAX AKE38FP0Z00 2M byte
WINBOND AKE38FP0N01 SPI
EON AKE38ZA0Q00 BIOS
SOCKET DFHS08FS023

Platform model	GPIO42
SG/DIS	High
UMA	Low
TBD	Middle (1.5V)



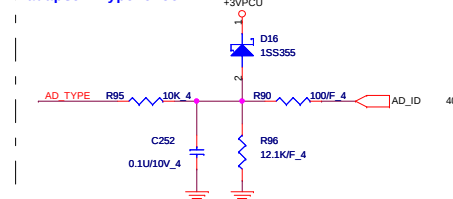
Hi ==> 90W

Low ==> 65W

If use SB RTC CLK
should change to 20P

Put close to EC side

adapter Type check

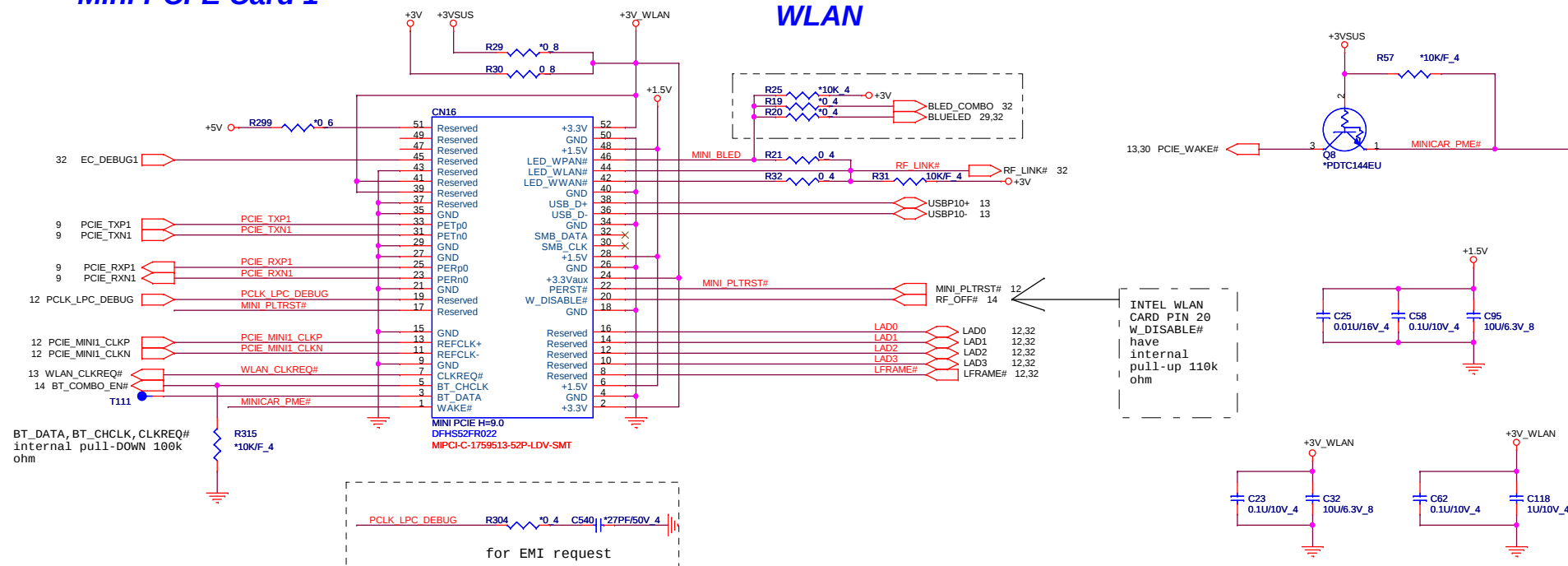


PROJECT : R22
Quanta Computer Inc.

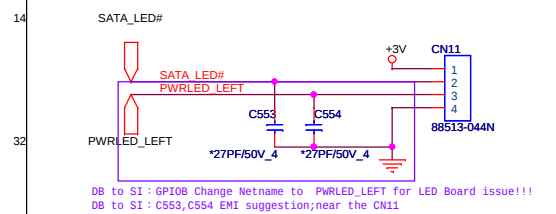
Document Number
KB3926/ROM/TP

Date: Wednesday, September 15, 2010 | Sheet 32 of 43

Mini PCI-E Card 1

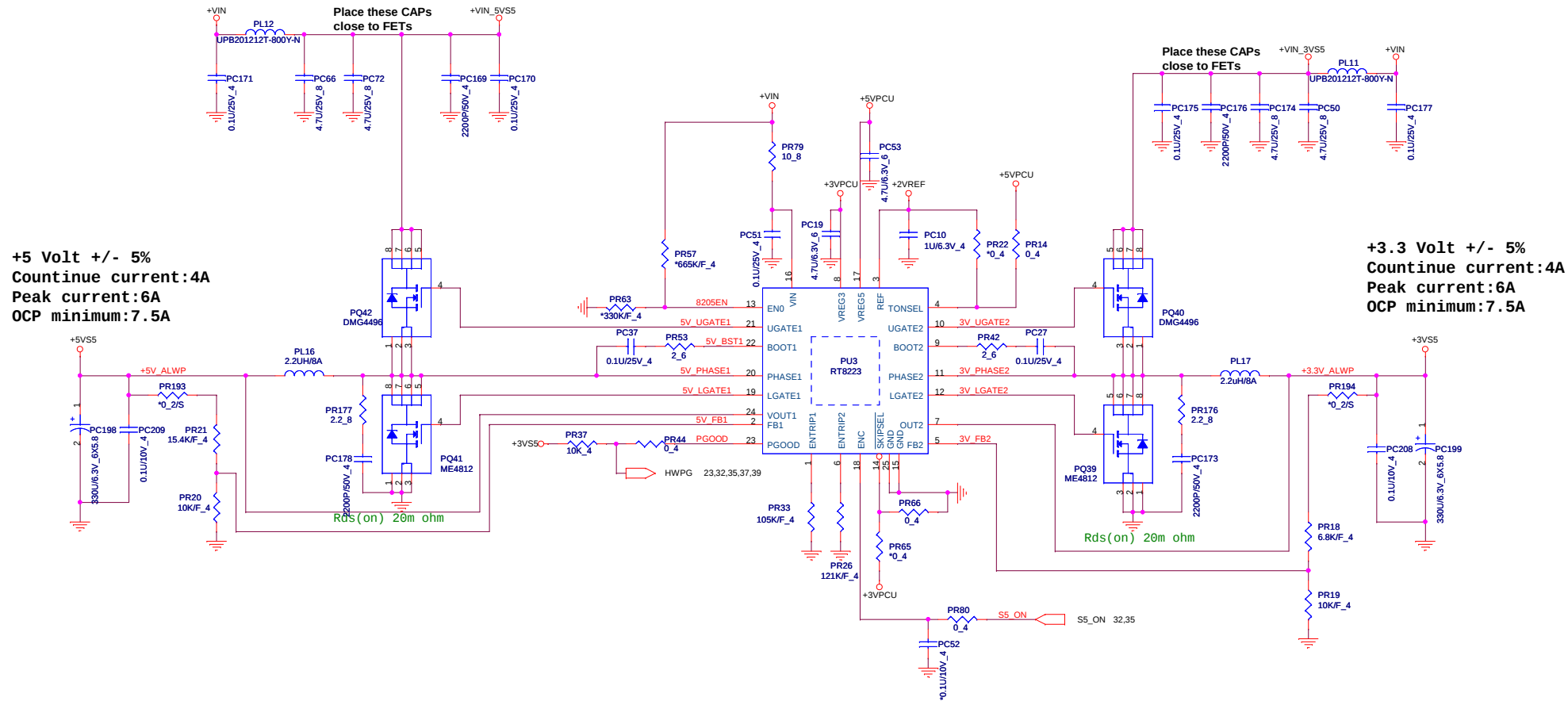


LED board CONN



PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number Mini CARD/LED CONN	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 33	of 43



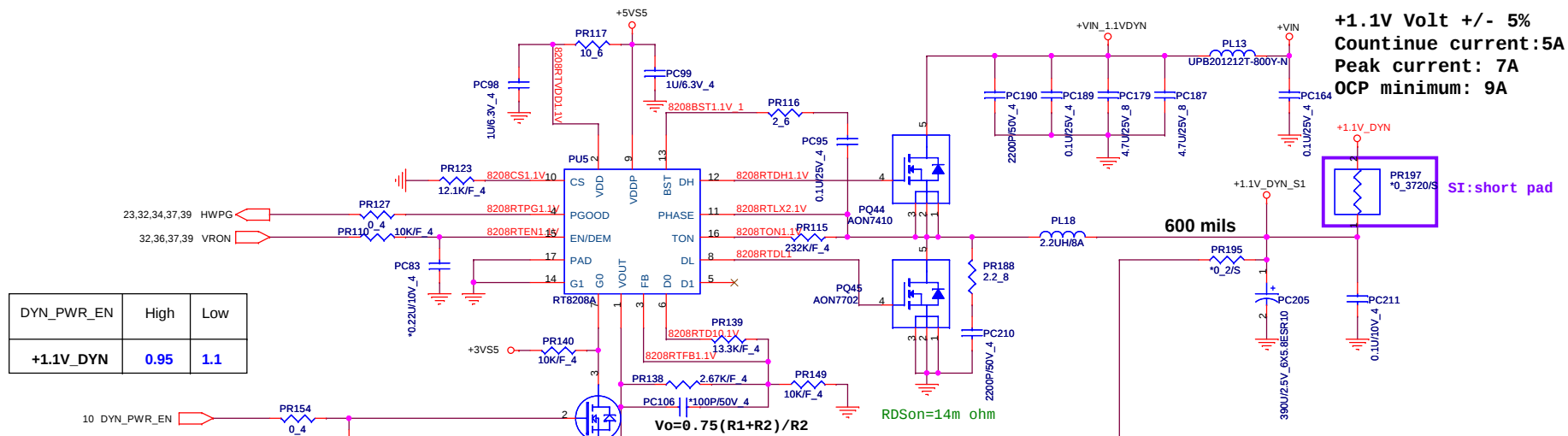


NBS/RD2

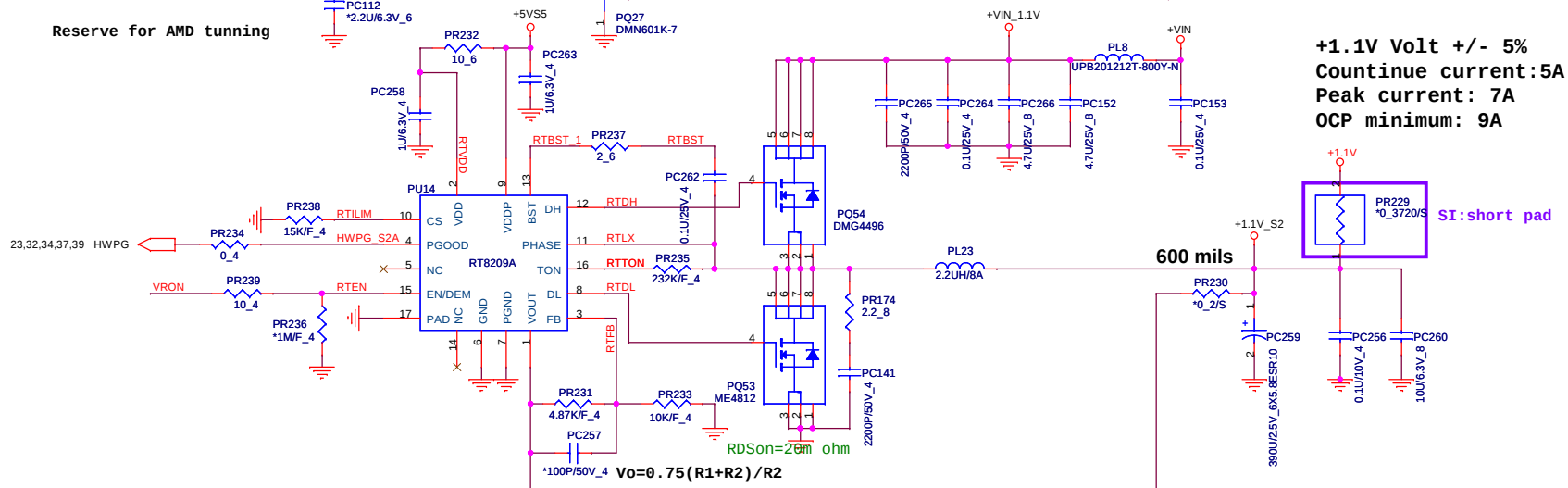
PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

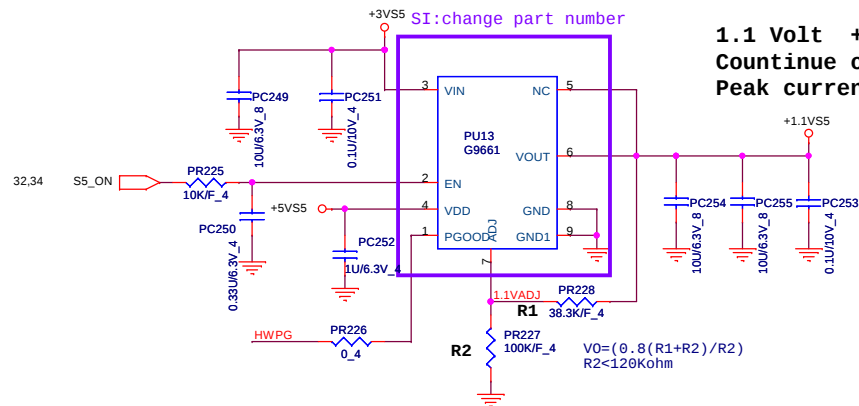
Date: Wednesday, September 15, 2010 Sheet 34 of 43



Reserve for AMD tunning



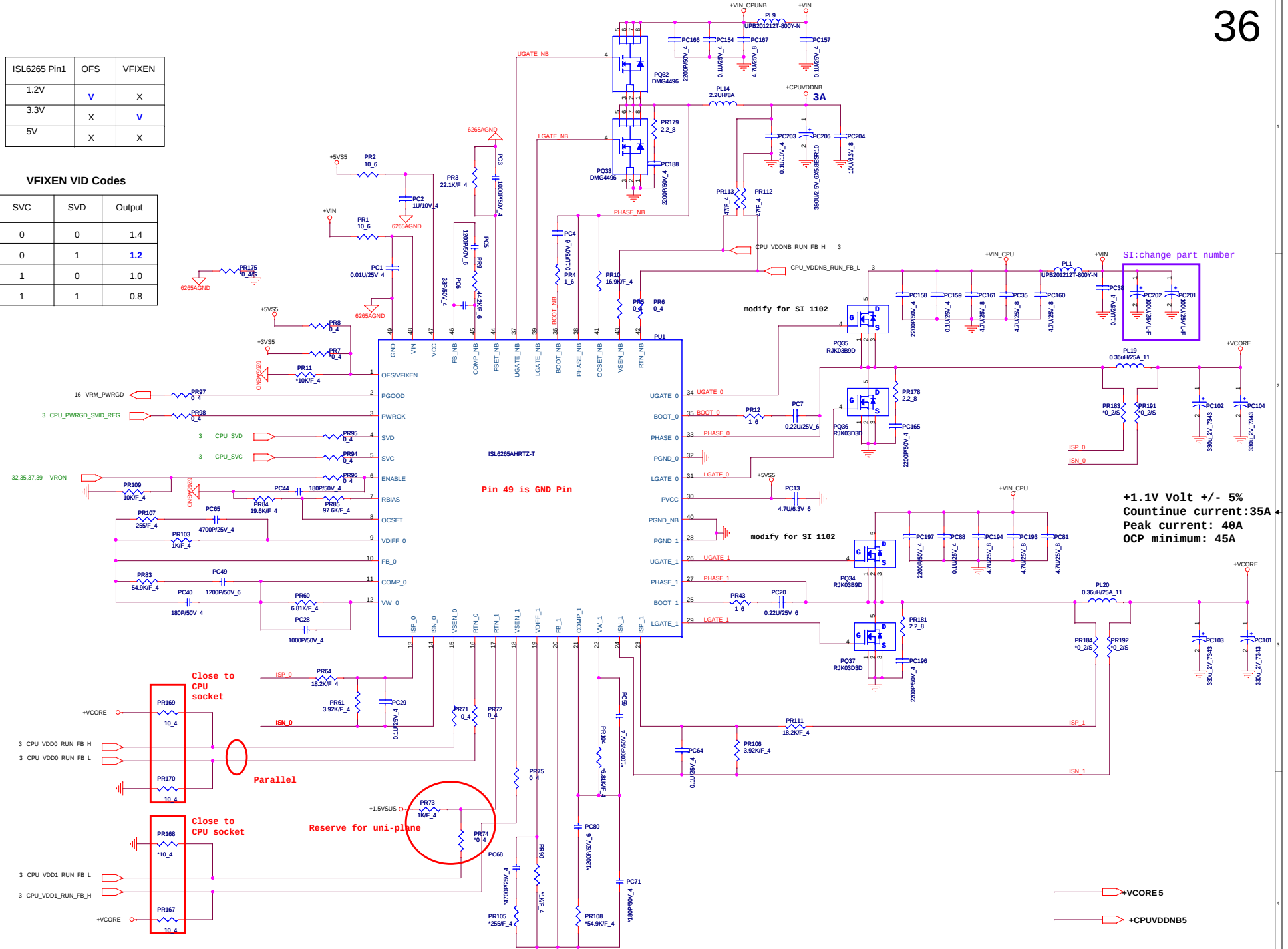
1.1 Volt +/- 5%
Continue current:0.2A
Peak current:0.5A



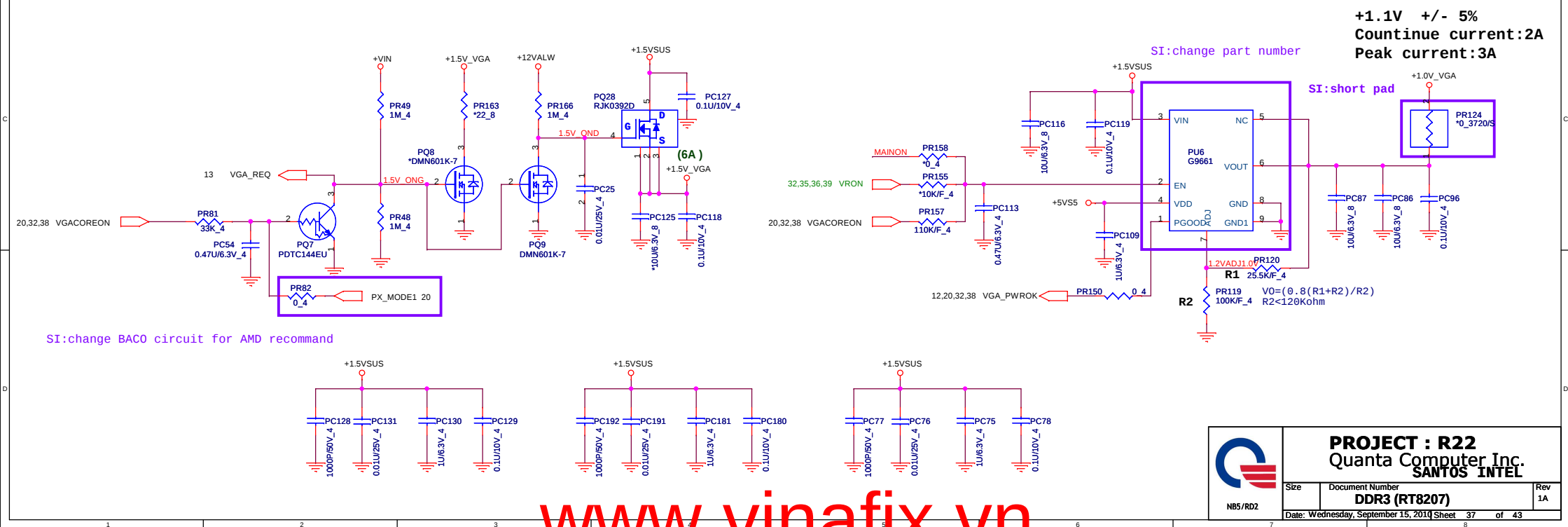
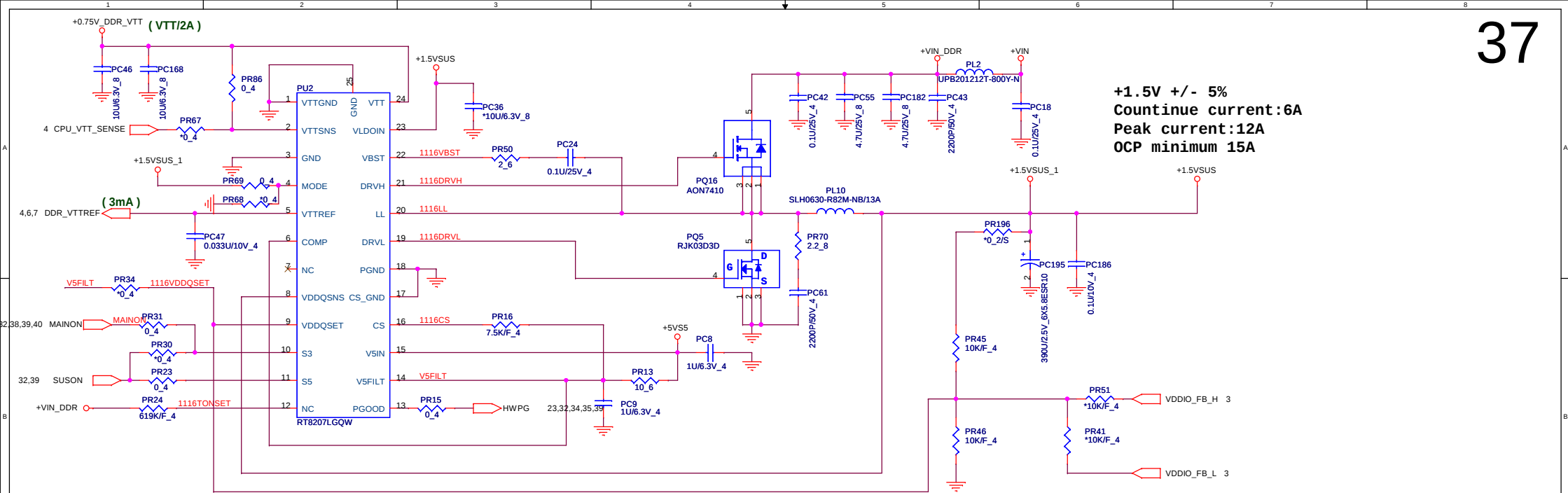
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

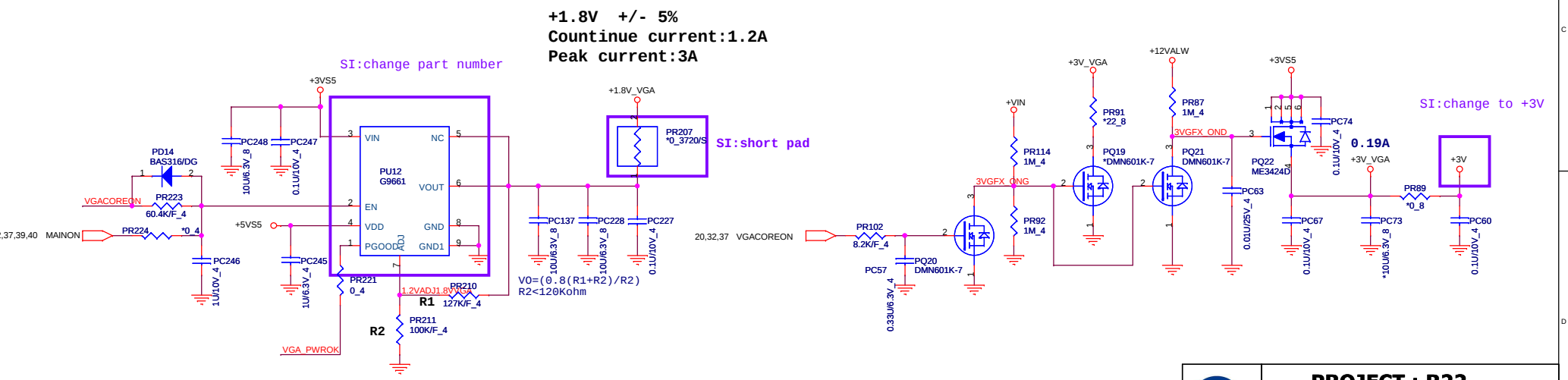
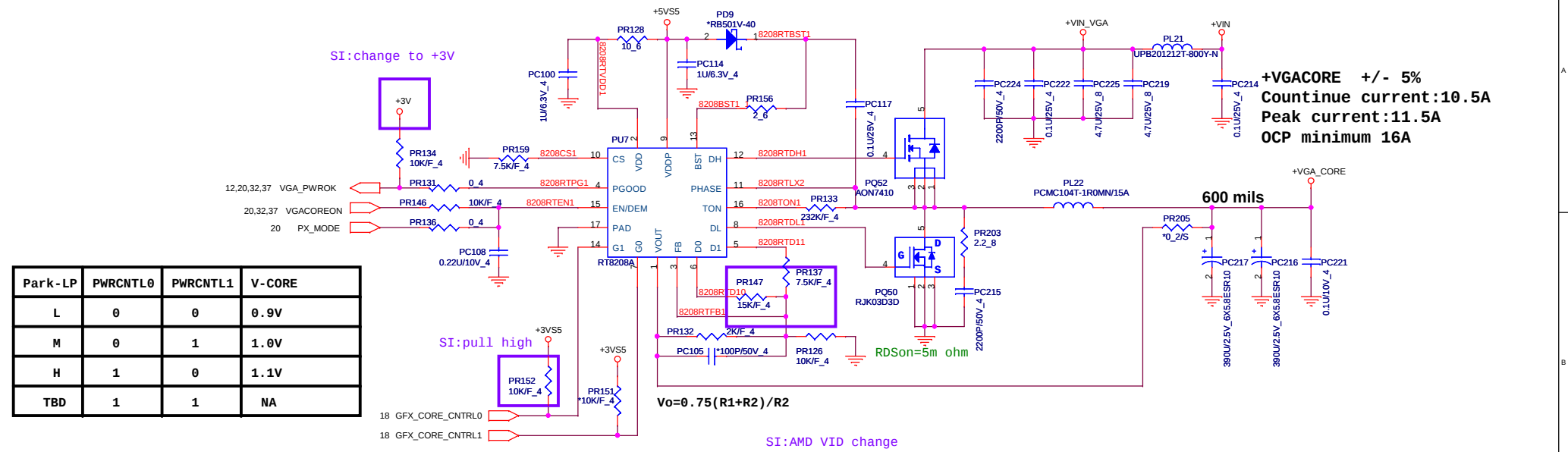
VFIXEN VID Codes

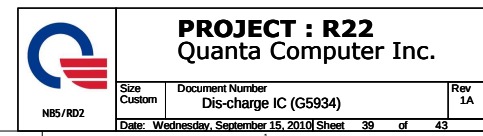
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



+1.1V Volt +/- 5%
 Countinue current:35A
 Peak current: 40A
 OCP minimum: 45A



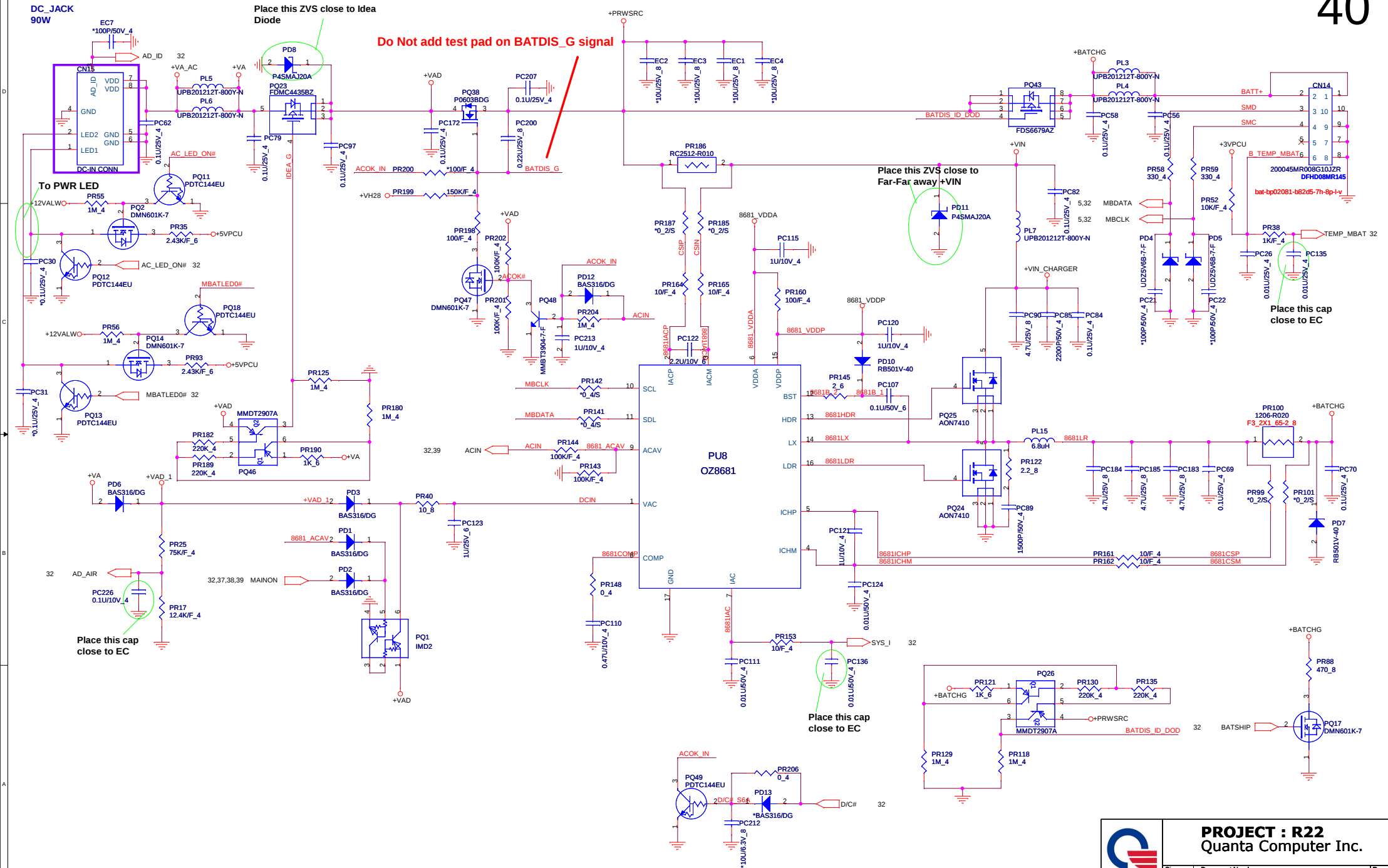




SI:change part number & footprint

DC_JACK
90WPlace this ZVS close to Idea
Diode

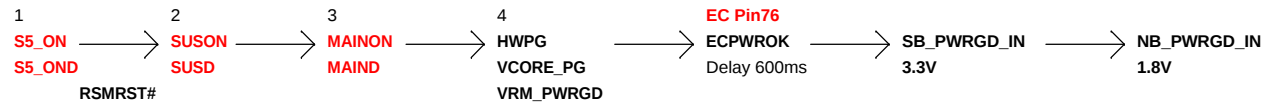
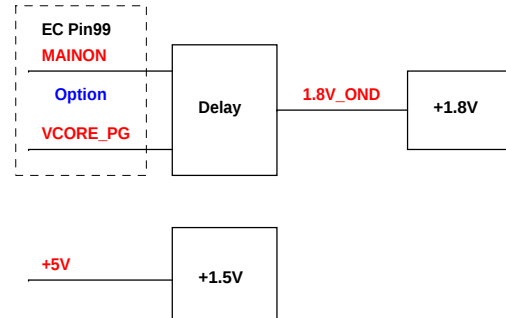
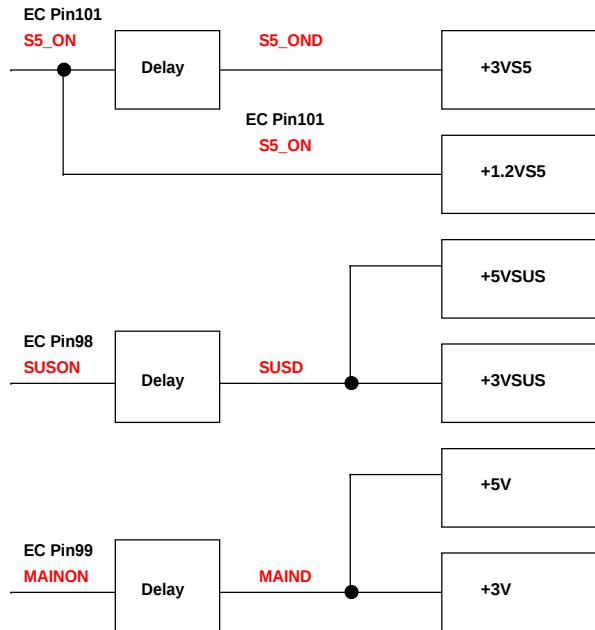
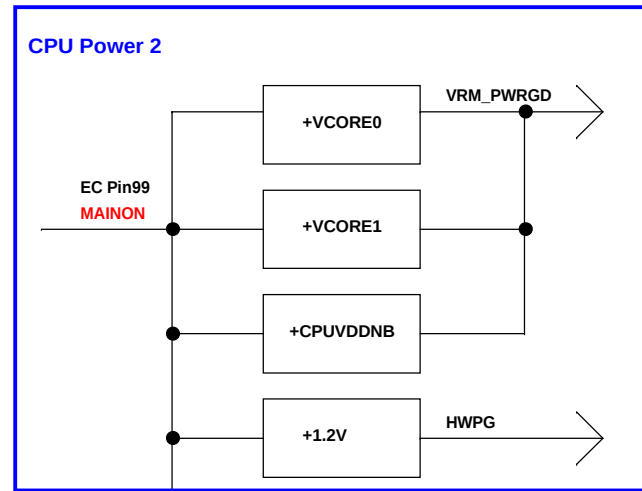
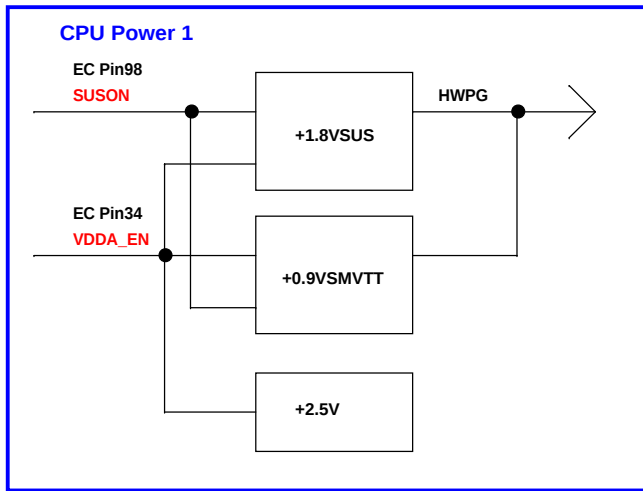
Do Not add test pad on BATDIS_G signal

Place this ZVS close to
Far-Far away +VINPlace this cap
close to ECPlace this cap
close to ECPlace this cap
close to EC

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251)	1A

Date: Wednesday, September 15, 2010 Sheet 40 of 43



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 42 of 43	