COMPAL CONFIDENTIAL

MODEL NAME : AAZ50

PCB NO : DAA0009W000

BOM P/N :

GPIO MAP: Gen7 GPIO Master_1127

Beaver Creek 12" UMA

Skylake U

2015-09-23

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

TCM@ : TPM & China TPM select

MB PCB

Part Number	Description
DAZ1DK00100	PCB AAZ50 LA-C451P LS-C451P 02

Layout Dell logo

REV: A00
PWB:

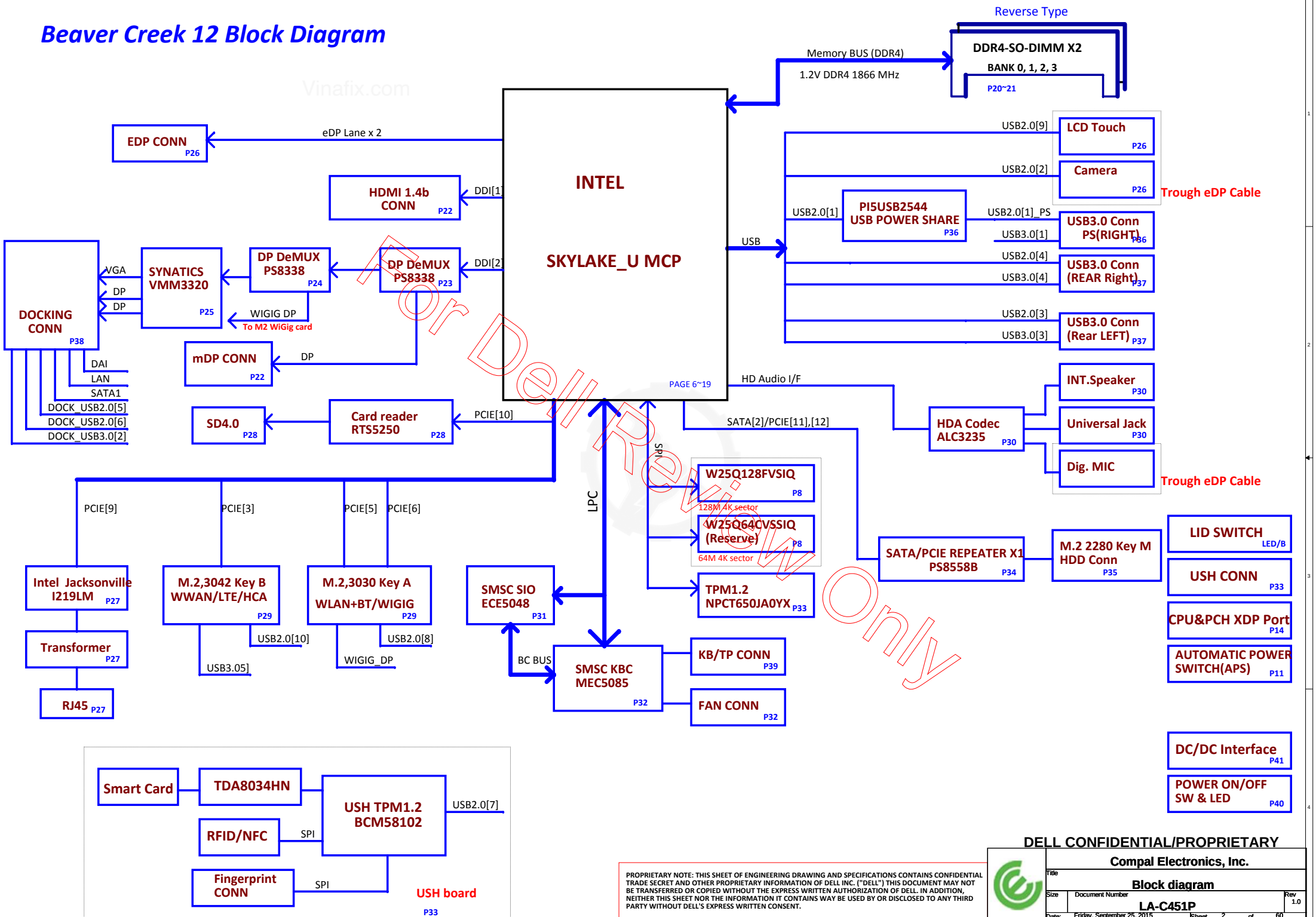
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 1 of 60

Beaver Creek 12 Block Diagram



Compal Electronics, Inc.

Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

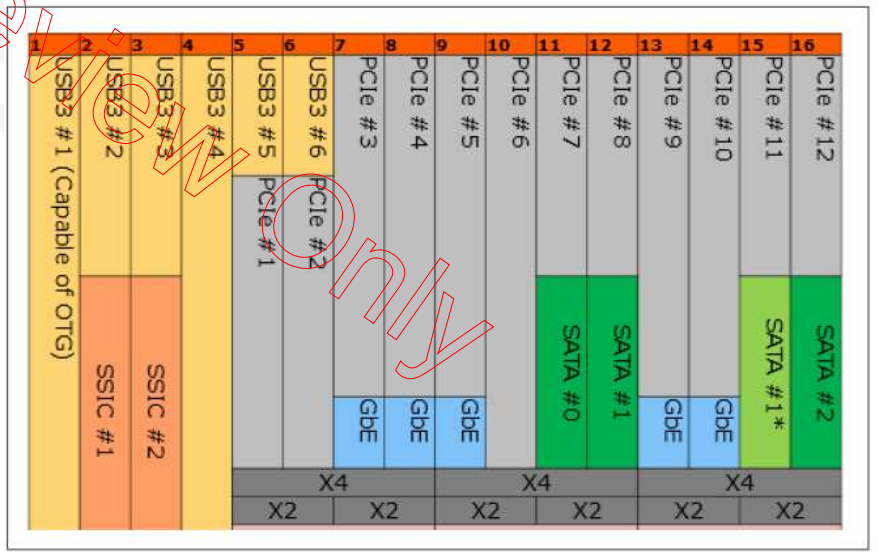
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	NP-155F	0.50
			Add Plating		
1	Top		Copper foil	0.5+plating	1.80
		3.7	Prepreg	1080	2.65
2	GND/PWR		Copper foil	0.5oz	0.65
		3.8	Core	4mil	4.00
3	IN 1		Copper foil	0.5oz	0.65
		3.7	Prepreg	2112	3.35
4	GND/PWR		Copper foil	0.5oz	0.65
		3.8	Core	4mil	4.00
5	IN 2		Copper foil	0.5 oz	0.65
		3.7	Prepreg	2112	3.01
6	IN 3		Copper foil	0.5 oz	0.65
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Prepreg	2112	3.35
8	IN 4		Copper foil	0.5oz	0.65
		3.8	Core	4mil	4.00
9	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.65
10	Bottom		Copper foil	0.5+plating	1.80
			Add Plating		
			SolderMask		0.50
Overall Thickness (1.0mm ± 10%)			39.37		40.81000
					1.036574

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right
USB3.0-2	SSIC-1			EDOCK PORT1
USB3.0-3	SSIC-2			JUSB1-->Rear Left
USB3.0-4				JUSB2-->Rear Right
USB3.0-5		PCIE-1		M2 3042(WWAN)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3042(HCA or QCA LTE)
		PCIE-4		NA
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	EDOCK E-SATA
		PCIE-9		LOM
		PCIE-10		Card Reader
		PCIE-11	SATA-1*	M.2 2280 SSD(Reverse) (PCIex2 or SATA)
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	Camera
3	JUSB2-->Rear Left
4	JUSB3-->Rear Right
5	EDOCK PORT1
6	EDOCK PORT2
7	USH
8	M.2 304230(BT)
9	Touch Screen
10	M2 3042(WWAN)

USH	H	BIO

High Speed I/O (HSIO) Lane Multiplexing in SKL U



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Title: Port assignment

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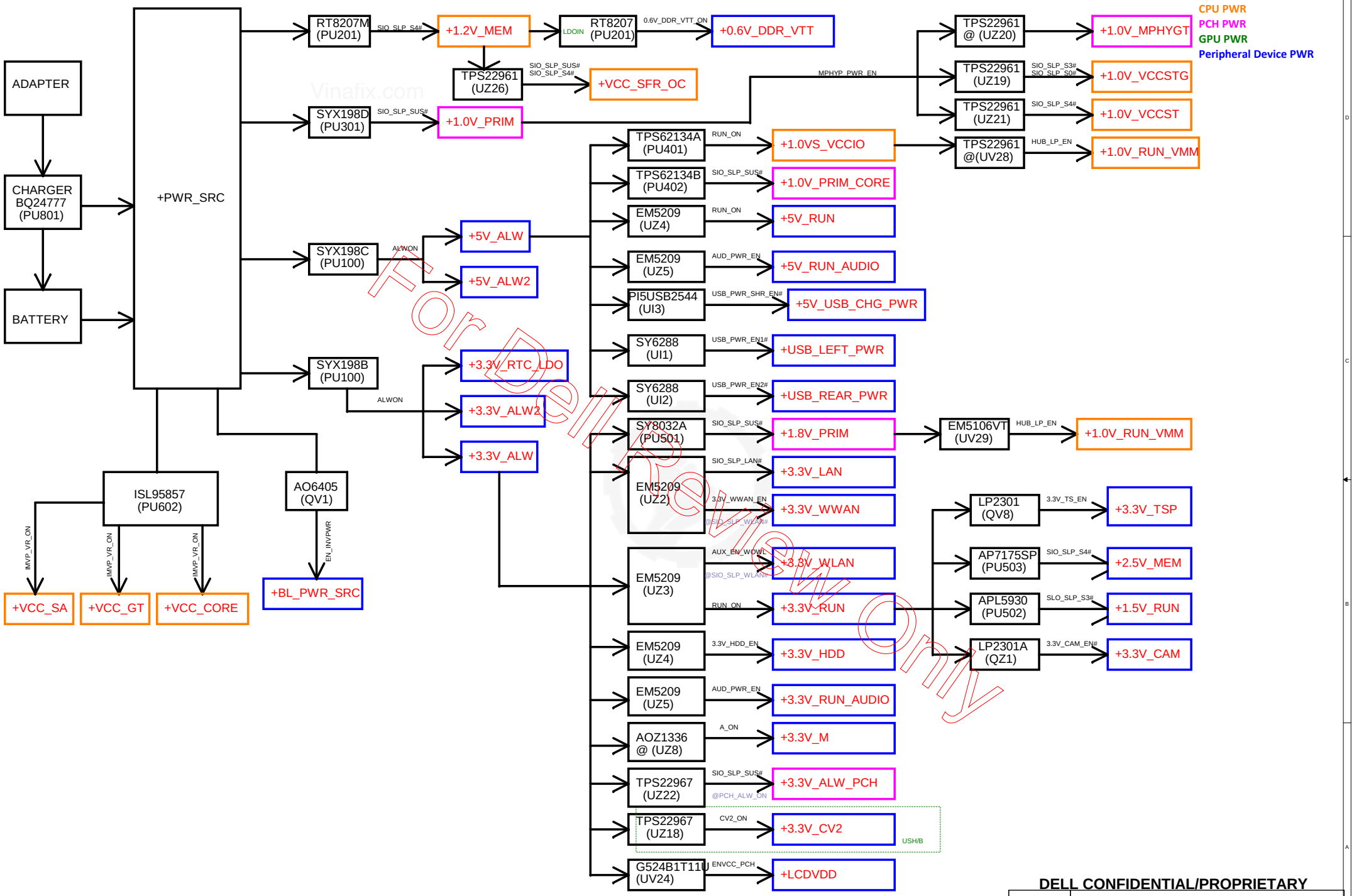
Date: Friday, September 25, 2015 | Sheet 3 of 60



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Title: Power rails

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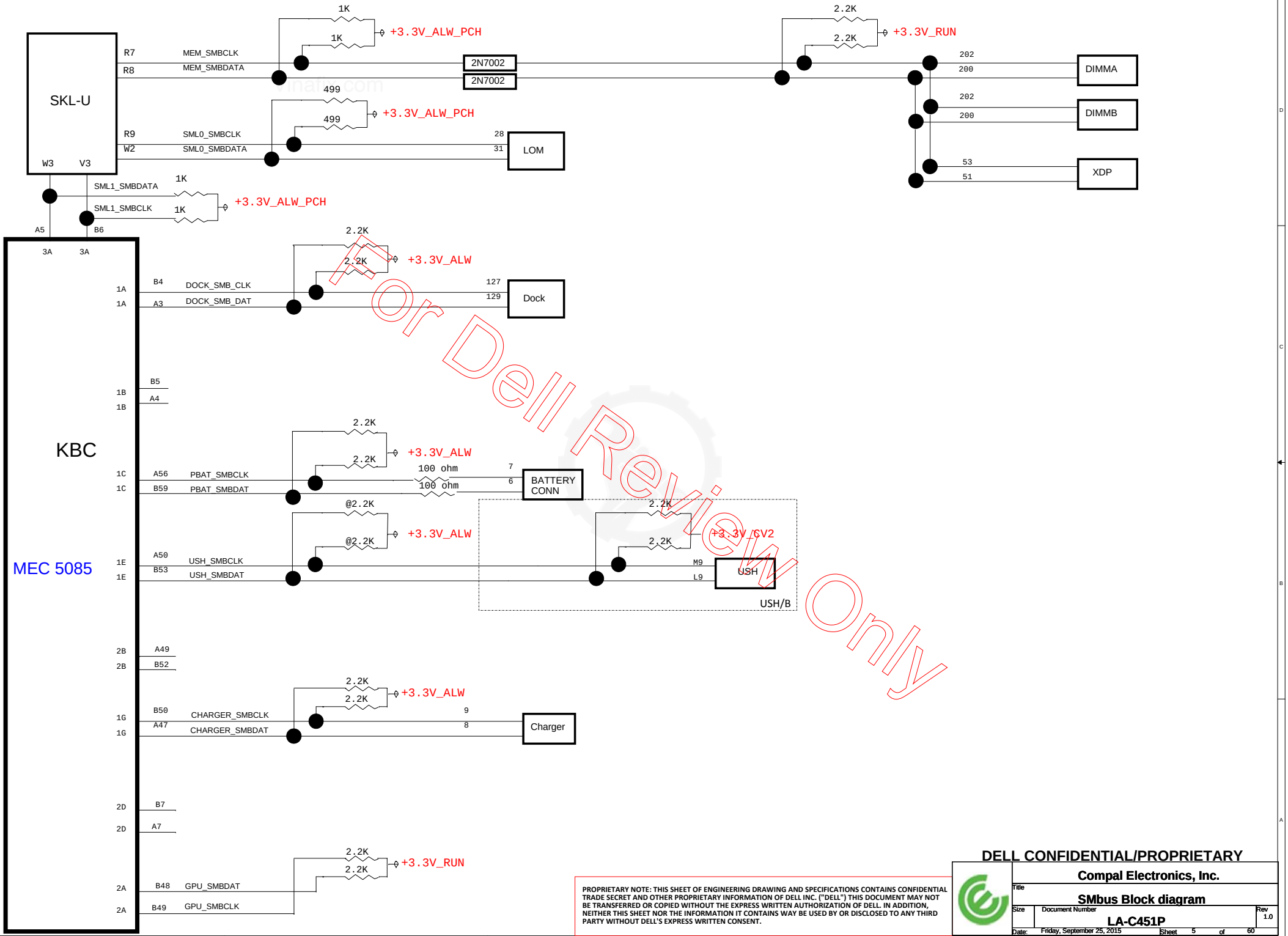
Date: Friday, September 25, 2015 | Sheet 4 of 60



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Title: SMbus Block diagram

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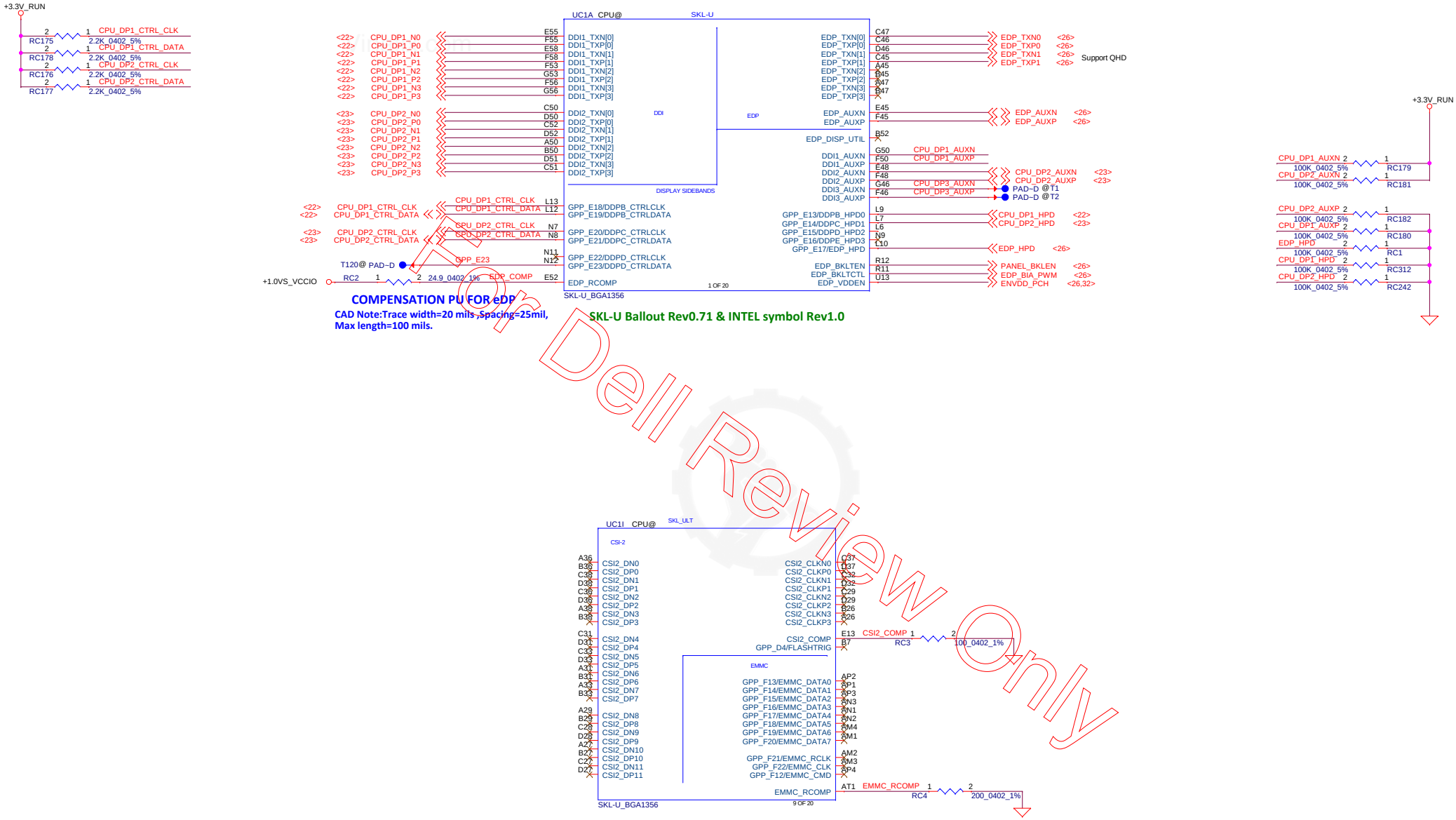
Date: Friday, September 25, 2015 | Sheet 5 of 60



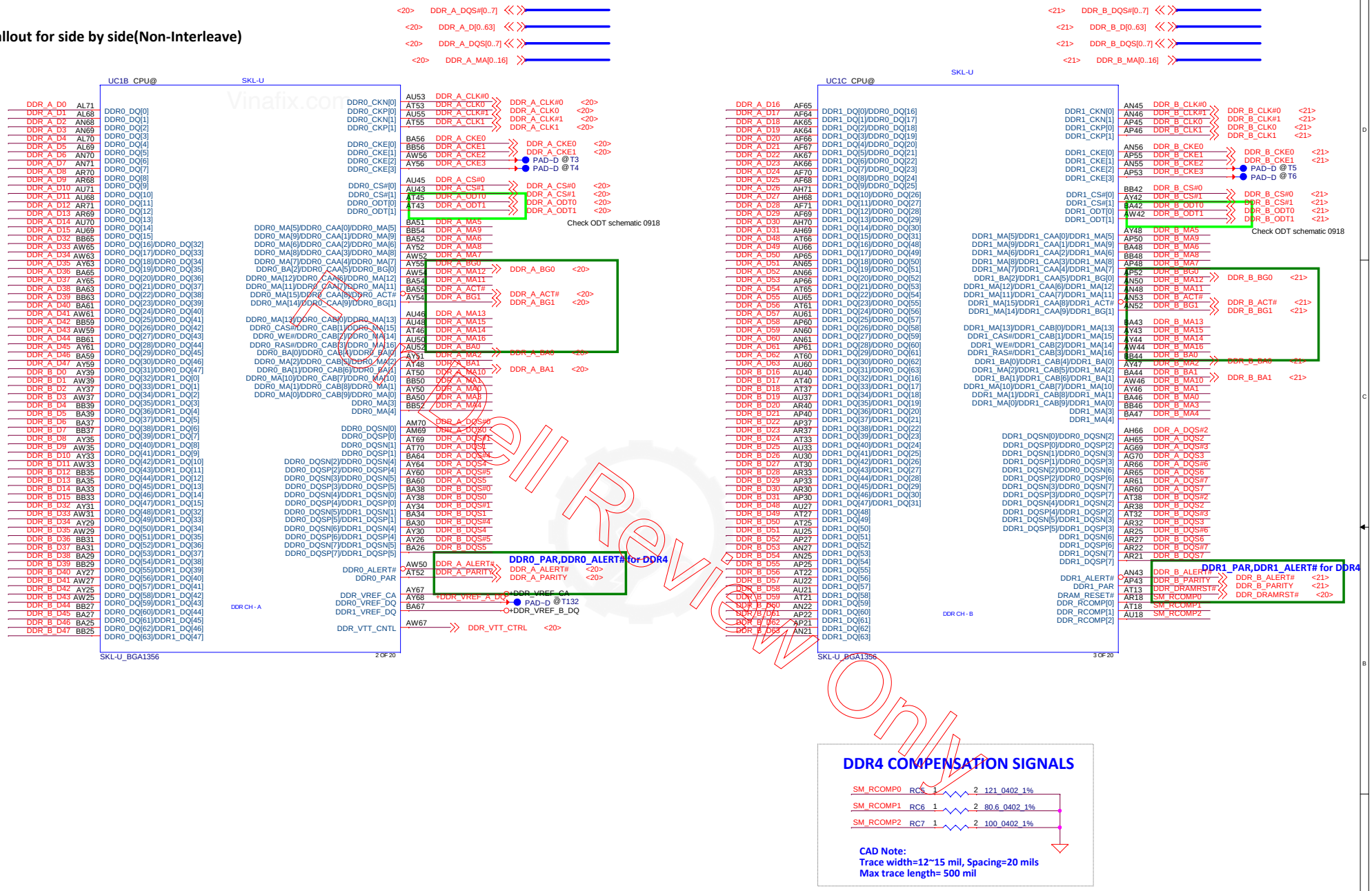
Compal Electronics, Inc.

Title: CPU (1/14)

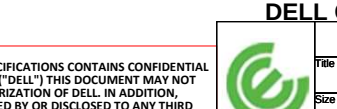
Size | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 6 of 60

DDR4, Ballot for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Compal Electronics, Inc.

Title	CPU (2/14)	
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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E CPU@ SKL-U

SPI - FLASH
PCH_SPI_CLK AV2 — SPI0_CLK
PCH_SPI_D1 AW3 — SPI0_MISO
PCH_SPI_D0 AV3 — SPI0_MOSI
PCH_SPI_D2 AW2 — SPI0_IO2
PCH_SPI_D3 AU4 — SPI0_IO3
PCH_SPI_CS#0 AU3 — SPI0_CS0#
PCH_SPI_CS#1 AU2 — SPI0_CS1#
PCH_SPI_CS#2 AU1 — SPI0_CS2#

<14> PCH_SPI_DO_XDP — RC10 1 2 1K_0402_1%
<14> PCH_SPI_DO2_XDP — RC11 1 2 1K_0402_1%
<33> PCH_SPI_CS#2

SPI - TOUCH
ONE_DIMM# M2 — GPP_D1/SPI1_CLK
<33> TPM_PIRQ# M3 — GPP_D2/SPI1_MISO
J4 — GPP_D3/SPI1_MOSI
V1 — GPP_D21/SPI1_IO2
V2 — GPP_D22/SPI1_IO3
<28> MEDIACARD_IRQ# M1 — GPP_D0/SPI1_CS#

C LINK
<29> PCH_CL_CLK1 G3 — CL_CLK
<29> PCH_CL_DATA1 G2 — CL_DATA
<29> PCH_CL_RST1# G1 — CL_RST#

AW13 — GPP_A9/RCIN#
<32> SIO_RCIN#
AY11 — GPP_A6/SERIRQ
<31,32> IRQ_SERIRQ
RC21 1 2 10K_0402_1%

SKL-U_BGA1356
5 OF 20

SMBUS, SMLINK
GPP_C0/SMBCLK R7 MEM_SMBCLK
GPP_C1/SMBDATA R8 MEM_SMBDATA
GPP_C2/SMBALERT# R10 PCH_SMB_ALERT#
GPP_C3/SML0CLK R9 SML0_SMBCLK — SML0_SMBCLK <27>
GPP_C4/SML0DATA W2 SML0_SMBDATA — SML0_SMBDATA <27>
GPP_C5/SML0ALERT# W1 GPP_C5
GPP_C6/SML1CLK W3 SML1_SMBCLK — SML1_SMBCLK <32>
GPP_C7/SML1DATA V3 SML1_SMBDATA — SML1_SMBDATA <32>
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 — LPC_AD0 <31,32>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 — LPC_AD1 <31,32>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 — LPC_AD2 <31,32>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 — LPC_AD3 <31,32>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# — LPC_FRAME# <31,32>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT#
Reserve

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 PCI_CLK_LPC0 — EMC@ RC16 1 2 22_0402_5% — CLK_PCI_5048 <31>
GPP_A10/CLKOUT_LPC1 AY9 PCI_CLK_LPC1 — EMC@ RC18 1 2 22_0402_5% — CLK_PCI_MEC <32>
GPP_A8/CLKRUN# AW11 — EMC@ RC22 1 2 22_0402_5% — CLK_PCI_LPDEBUG <32>
CLKRUN# <31,32> — EMC@ RC24 1 2 22_0402_5% — CLK_PCI_DOCK <38>

DIMM Detect

HIGH	1 DIMM
LOW	2 DIMM

+3.3V_RUN
MEM_SMBCLK — QC2A DMN65D8LDW-7_SOT363-6 — DDR_XDP_WAN_SMBCLK <14,20,21>
MEM_SMBDATA — QC2B DMN65D8LDW-7_SOT363-6 — DDR_XDP_WAN_SMBDAT <14,20,21>

DDR_XDP_WAN_SMBDAT 2.2K_0402_5% RC318
DDR_XDP_WAN_SMBCLK 2.2K_0402_5% RC319

+3.3V_ALW_PCH
MEM_SMBCLK RC12 1K_0402_5%
MEM_SMBDATA RC14 1K_0402_5%
SML1_SMBCLK RC15 1K_0402_5%
SML1_SMBDATA RC17 1K_0402_5%
SML0_SMBCLK RC347 499_0402_1%
SML0_SMBDATA RC348 499_0402_1%
SUS_STAT# Reserve @RC26 10K_0402_5%

11/20 INTEL REVIEW
+3.3V_LAN
SML0_SMBCLK @RC19 499_0402_1%
SML0_SMBDATA @RC20 499_0402_1%

+3.3V_RUN
8/5 CKLT0.9
CLKRUN# RC27 8.2K_0402_5%

SOFTWARE TAA

CLK_PCI_5048 27P_0402_50V8J EMC@ CC3
CLK_PCI_MEC 27P_0402_50V8J @EMC@ CC4
CLK_PCI_LPDEBUG 27P_0402_50V8J EMC@ CC5
CLK_PCI_DOCK 27P_0402_50V8J EMC@ CC6
Reserve for RF

PCH_SPI_CLK_1_R — 33_0402_5% @EMC@ RC28 — 33P_0402_50V8J @EMC@ CC7
PCH_SPI_CLK_0_R — 33_0402_5% @EMC@ RC29 — 33P_0402_50V8J @EMC@ CC8

+3.3V_SPI
@RC30 PCH_SPI_D2_R1 1K_0402_5%
@RC31 PCH_SPI_D3_R1 1K_0402_5%
@RC316 PCH_SPI_D3_R1 1K_0402_5%
03/02:follow Intel MOW_2015WW06

<33> PCH_SPI_D1_R1
<33> PCH_SPI_D0_R1
<33> PCH_SPI_CLK_R1
RPC1 33_0804_8P4R_5%
PCH_SPI_D1_R1 — PCH_SPI_D1_0_R
PCH_SPI_D0_R1 — PCH_SPI_D0_0_R
PCH_SPI_CLK_R1 — PCH_SPI_CLK_0_R
PCH_SPI_D3_R1 — PCH_SPI_D3_0_R

@RPC2 33_0804_8P4R_5%
PCH_SPI_D3_R1 — PCH_SPI_D3_1_R
PCH_SPI_CLK_R1 — PCH_SPI_CLK_1_R
PCH_SPI_D0_R1 — PCH_SPI_D0_1_R
PCH_SPI_D1_R1 — PCH_SPI_D1_1_R

+3.3V_ALW_PCH
PCH_SMB_ALERT# RC23 2.2K_0402_5%

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

+3.3V_ALW_PCH
GPP_C5 @RC25 10K_0402_5%

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

128Mb Flash ROM
UC5 W25Q128FVSIQ_SO8
+3.3V_SPI — CC9 0.1U_0201_10V6K
PCH_SPI_CS#0_R1 — RC37 0_0402_5% — PCH_SPI_CS#0_R2
PCH_SPI_D2_R1 — RC39 33_0402_5% — PCH_SPI_D2_0_R
/CS — PCH_SPI_CS#0_R2
IO1 — PCH_SPI_D1_0_R
IO2 — PCH_SPI_D2_0_R
GND
VCC — +3.3V_SPI
IO3 — PCH_SPI_D3_0_R
CLK — PCH_SPI_CLK_0_R
IO0 — PCH_SPI_D0_0_R

64Mb Flash ROM
UC6@ W25Q64FVSSIQ_SO8
+3.3V_SPI — @ CC10 0.1U_0201_10V6K
PCH_SPI_CS#1_R1 — @RC42 0_0402_5% — PCH_SPI_CS#1_R2
PCH_SPI_D2_R1 — @RC43 33_0402_5% — PCH_SPI_D2_1_R
/CS — PCH_SPI_CS#1_R2
DO(IO1) — PCH_SPI_D1_1_R
/WP(IO2)
GND
VCC — +3.3V_SPI
/HOLD(IO3) — PCH_SPI_D3_1_R
CLK — PCH_SPI_CLK_1_R
DI(IO0) — PCH_SPI_D0_1_R

E_T_6705K-Y20N-00L
@RC32 PCH_SPI_CS#1_R1 — PCH_SPI_CS#1
RC33 PCH_SPI_D0_R1 — PCH_SPI_D0
RC34 PCH_SPI_D1_R1 — PCH_SPI_D1
RC35 PCH_SPI_CLK_R1 — PCH_SPI_CLK
RC36 PCH_SPI_CS#0_R1 — PCH_SPI_CS#0
RC38 PCH_SPI_D2_R1 — PCH_SPI_D2
RC40 PCH_SPI_D3_R1 — PCH_SPI_D3
+3.3V_SPI
+3.3V_ALW_PCH — @RC289 8/27 sch review 0_0402_5%
+3.3V_M — @RC276 0_0402_5%
RC41 0_0402_5% — +3.3V_SPI_R
JSPI1 CONN@ <11,18,32,41,45,46,47>
<11,32>

+3.3V_RUN — 11/29 MOW for DCI — 150K_0402_5% @RC326
+3.3V_ALW_PCH — 02/25 INTEL mail for DCI — 150K_0402_5% RC317
@RC327 0_0402_5%
GPP_B23 — GPP_B23_Q — @QC3 L2N7002WT1G_SC-70-3
SIO_SLP_A# — @RC339 0_0402_5%
SIO_SLP_SUS# — @RC340 0_0402_5%

EXI BOOT STALL BYPASS	
HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

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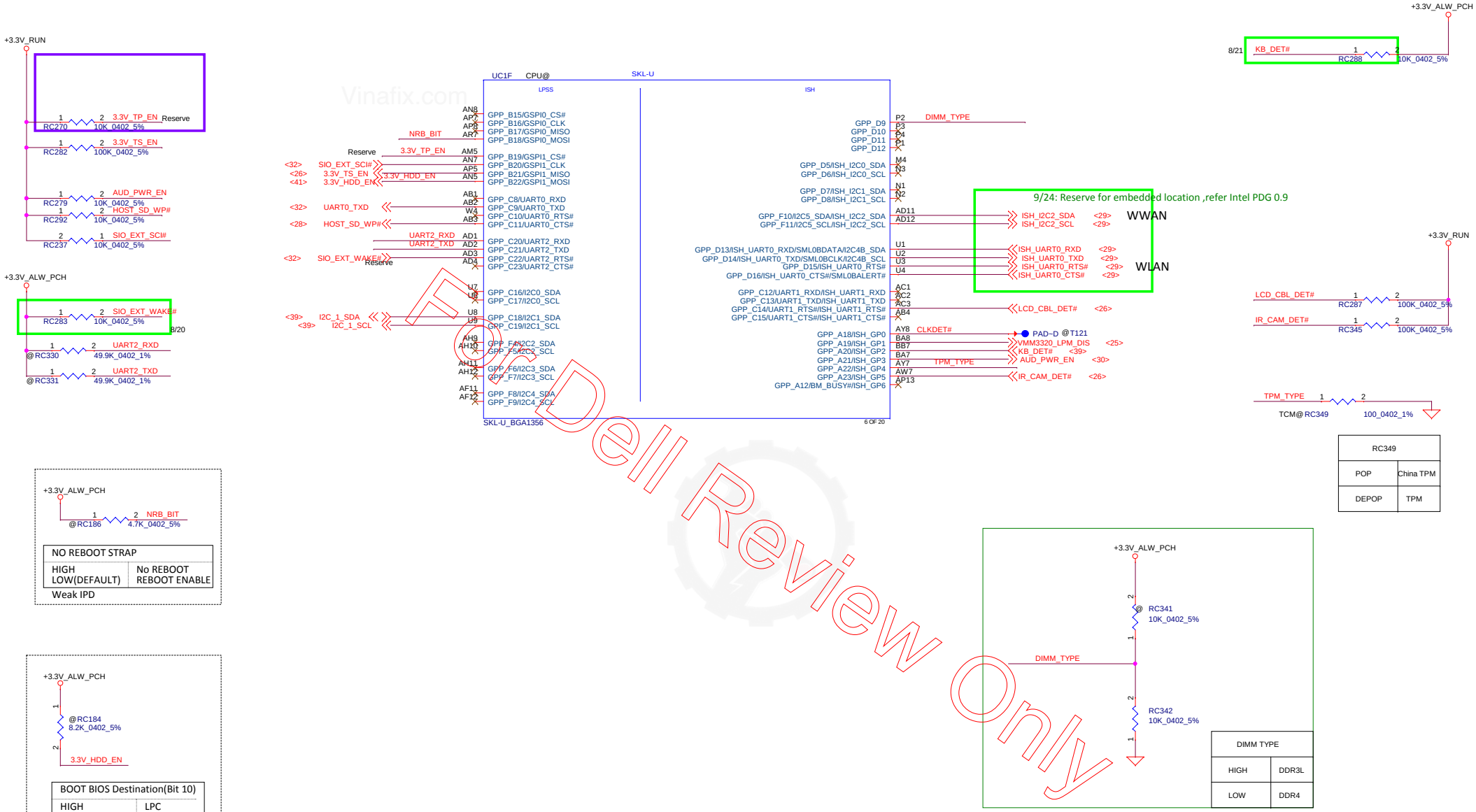
Title: CPU (3/14)
Size: — Document Number: LA-C451P — Rev: 1.0
Date: Friday, September 25, 2015 — Sheet 8 of 60



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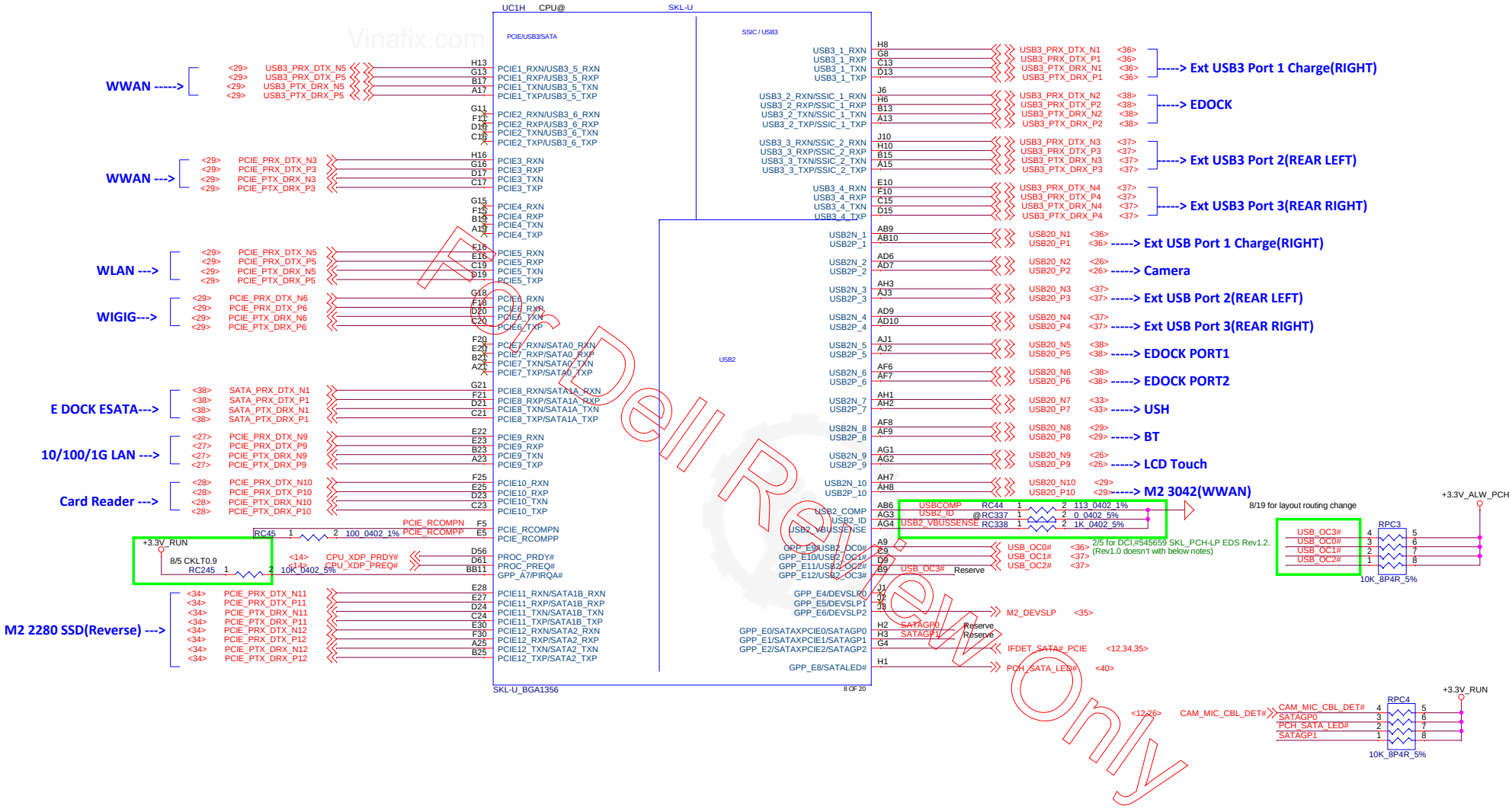
Title	CPU (4/14)	
Size	Document Number: LA-C451P	Rev: 1.0
Date: Friday, September 25, 2015	Sheet 9 of 60	



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Compal Electronics, Inc.

Title: CPU (5/14)

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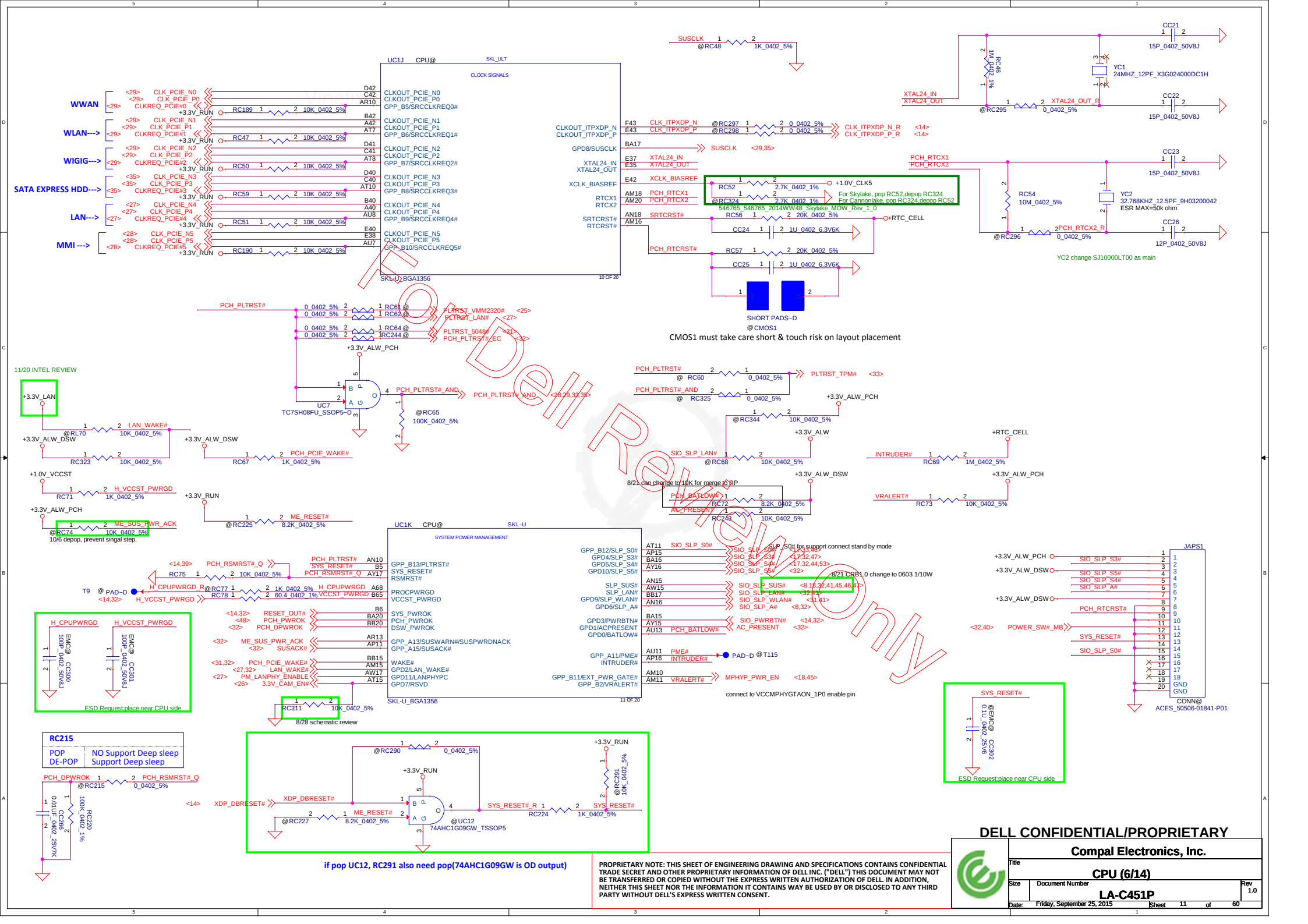
Date: Friday, September 25, 2015 | Sheet 10 of 60


UC1J CPU@ SKL_ULT
CLOCK SIGNALS
WWAN
WLAN--->
WIGIG--->
SATA EXPRESS HDD--->
LAN--->
MMI --->
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RTCX1
RTCX2
SRTCRST#
RTCRST#
SKL-U_BGA1356
10 OF 20
SUSCLK
PCH_RTCX1
PCH_RTCX2
PCH_RTCRST#
SRTCRST#
PCH_PLTRST#
PLTRST_VMM2320#
PLTRST_LAN#
PLTRST_5048#
PCH_PLTRST#_EC
+3.3V_ALW_PCH
UC7
TC7SH08FU_SSOP5-D
PCH_PLTRST#_AND
SHORT PADS-D
@CMOS1
CMOS1 must take care short & touch risk on layout placement
11/20 INTEL REVIEW
+3.3V_LAN
+3.3V_ALW_DSW
+3.3V_RUN
+1.0V_VCCST
+3.3V_ALW
+RTC_CELL
8/21 can change to 10K for merge to RP
10/6 depop, prevent singal step.
UC1K CPU@ SKL-U
SYSTEM POWER MANAGEMENT
SLP_S0# for support connect stand by mode
8/21 CRB1.0 change to 0603 1/10W
JAPS1
CONN@
ACES_50506-01841-P01
ESD Request:place near CPU side
8/28 schematic review
RC215
POP NO Support Deep sleep
DE-POP Support Deep sleep
74AHC1G09GW_TSSOP5
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)
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Compal Electronics, Inc.
CPU (6/14)
LA-C451P
Rev 1.0
Friday, September 25, 2015
Sheet 11 of 60
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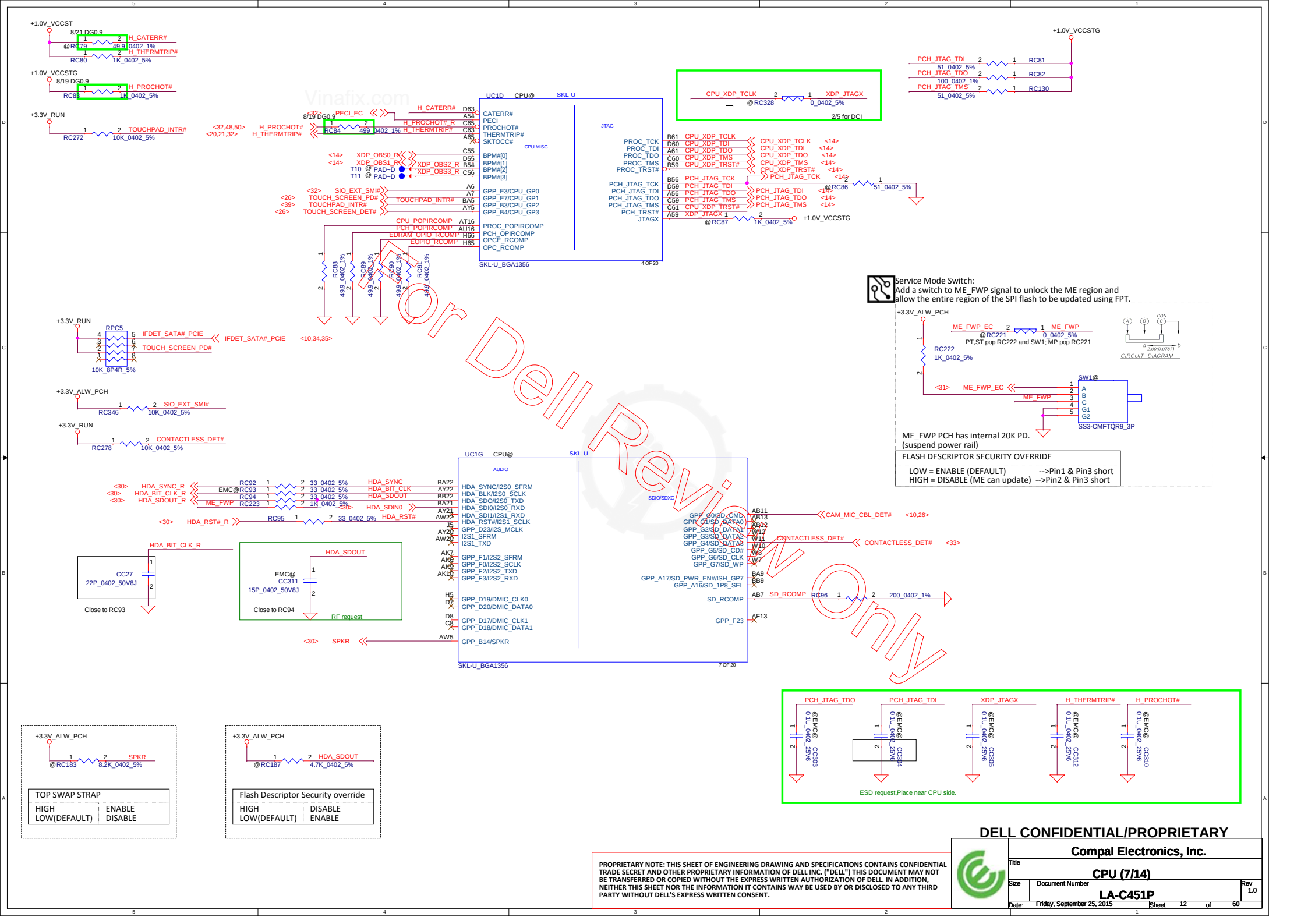
+1.0V_VCCST
8/21 DG0.9
H_CATERR#
@RC79 49.9_0402_1%
H_THERMTRIP#
RC80 1K_0402_5%
+1.0V_VCCSTG
8/19 DG0.9
H_PROCHOT#
RC83 1K_0402_5%
+3.3V_RUN
TOUCHPAD_INTR#
RC272 10K_0402_5%
+1.0V_VCCSTG
PCH_JTAG_TDI RC81 51_0402_5%
PCH_JTAG_TDO RC82 100_0402_1%
PCH_JTAG_TMS RC130 51_0402_5%
CPU_XDP_TCLK @RC328 XDP_JTAGX 0_0402_5%
2/5 for DCI
UC1D CPU@ SKL-U
JTAG
CPU MISC
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
SKL-U_BGA1356
4 OF 20
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX
CPU_XDP_TCLK
CPU_XDP_TDI
CPU_XDP_TDO
CPU_XDP_TMS
CPU_XDP_TRST#
XDP_JTAGX
@RC86 51_0402_5%
@RC87 1K_0402_5%
+1.0V_VCCSTG
RC88 RC89 RC90 RC91 49.9_0402_1%
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.
+3.3V_ALW_PCH
ME_FWP_EC @RC221 ME_FWP 0_0402_5%
PT,ST pop RC222 and SW1; MP pop RC221
RC222 1K_0402_5%
CIRCUIT DIAGRAM
SW1@
SS3-CMFTQR9_3P
ME_FWP PCH has internal 20K PD.
(suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
+3.3V_RUN
RPC5 10K_8P4R_5%
IFDET_SATA#_PCIE
TOUCH_SCREEN_PD#
+3.3V_ALW_PCH
SIO_EXT_SMI# RC346 10K_0402_5%
+3.3V_RUN
CONTACTLESS_DET# RC278 10K_0402_5%
UC1G CPU@ SKL-U
AUDIO
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR
SKL-U_BGA1356
7 OF 20
SDIO/SDXC
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_RCOMP
GPP_F23
CAM_MIC_CBL_DET#
CONTACTLESS_DET#
HDA_SYNC_R
HDA_BIT_CLK_R
HDA_SDOUT_R
HDA_SDIN0
HDA_RST#_R
RC92 RC93 RC94 RC223 RC95 33_0402_5%
HDA_SYNC
HDA_BIT_CLK
HDA_SDOUT
HDA_RST#
CC27 22P_0402_50V8J
Close to RC93
EMC@ CC311 15P_0402_50V8J
Close to RC94
RF request
SPKR
RC96 200_0402_1%
PCH_JTAG_TDO
PCH_JTAG_TDI
XDP_JTAGX
H_THERMTRIP#
H_PROCHOT#
@EMC@ 0.1U_0402_25V6
CC303 CC304 CC305 CC312 CC310
ESD request,Place near CPU side.
+3.3V_ALW_PCH
@RC183 SPKR 8.2K_0402_5%
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
+3.3V_ALW_PCH
@RC187 HDA_SDOUT 4.7K_0402_5%
Flash Descriptor Security override
HIGH DISABLE
LOW(DEFAULT) ENABLE
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Compal Electronics, Inc.
Title
CPU (7/14)
Size
Document Number
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1.0
Date: Friday, September 25, 2015
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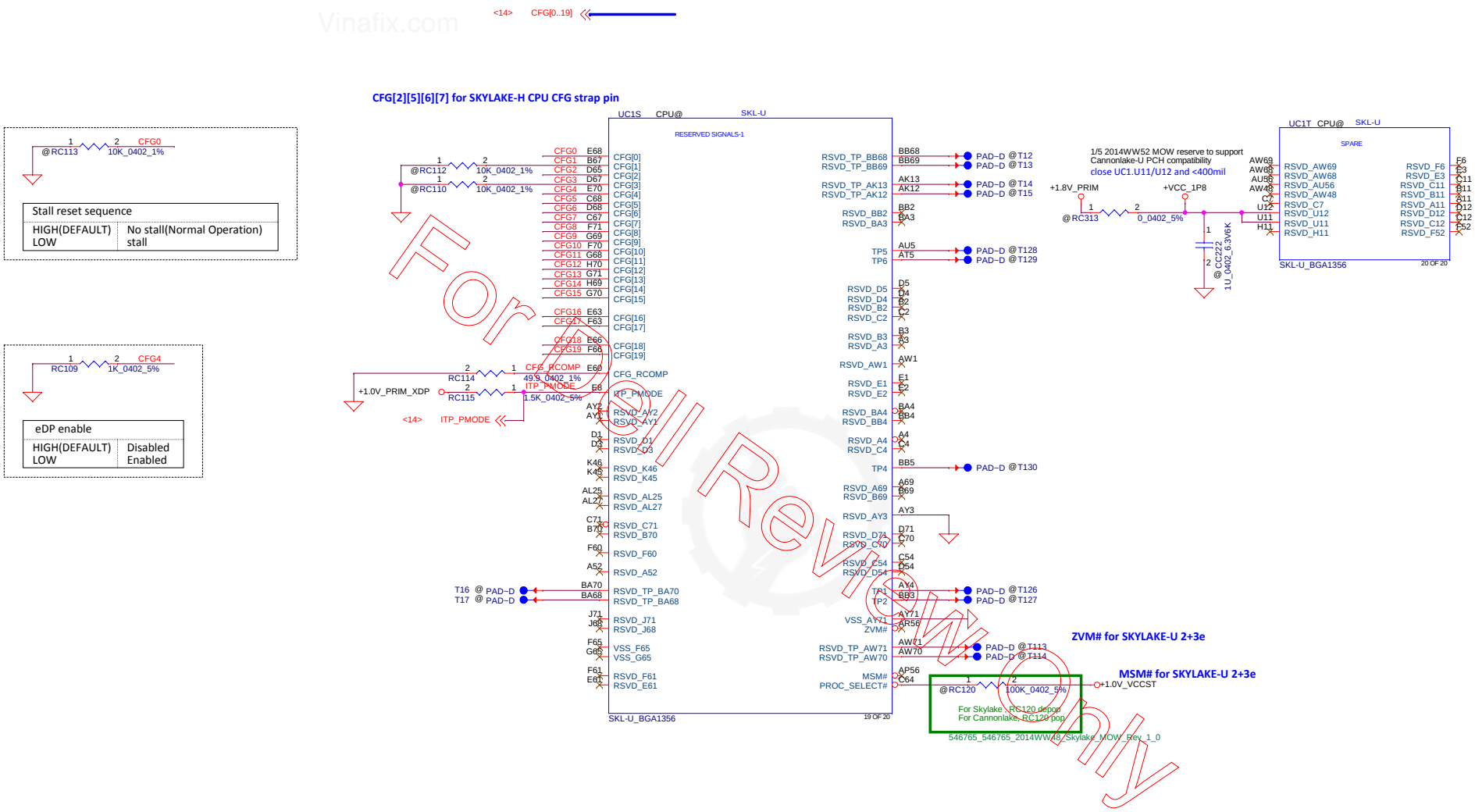

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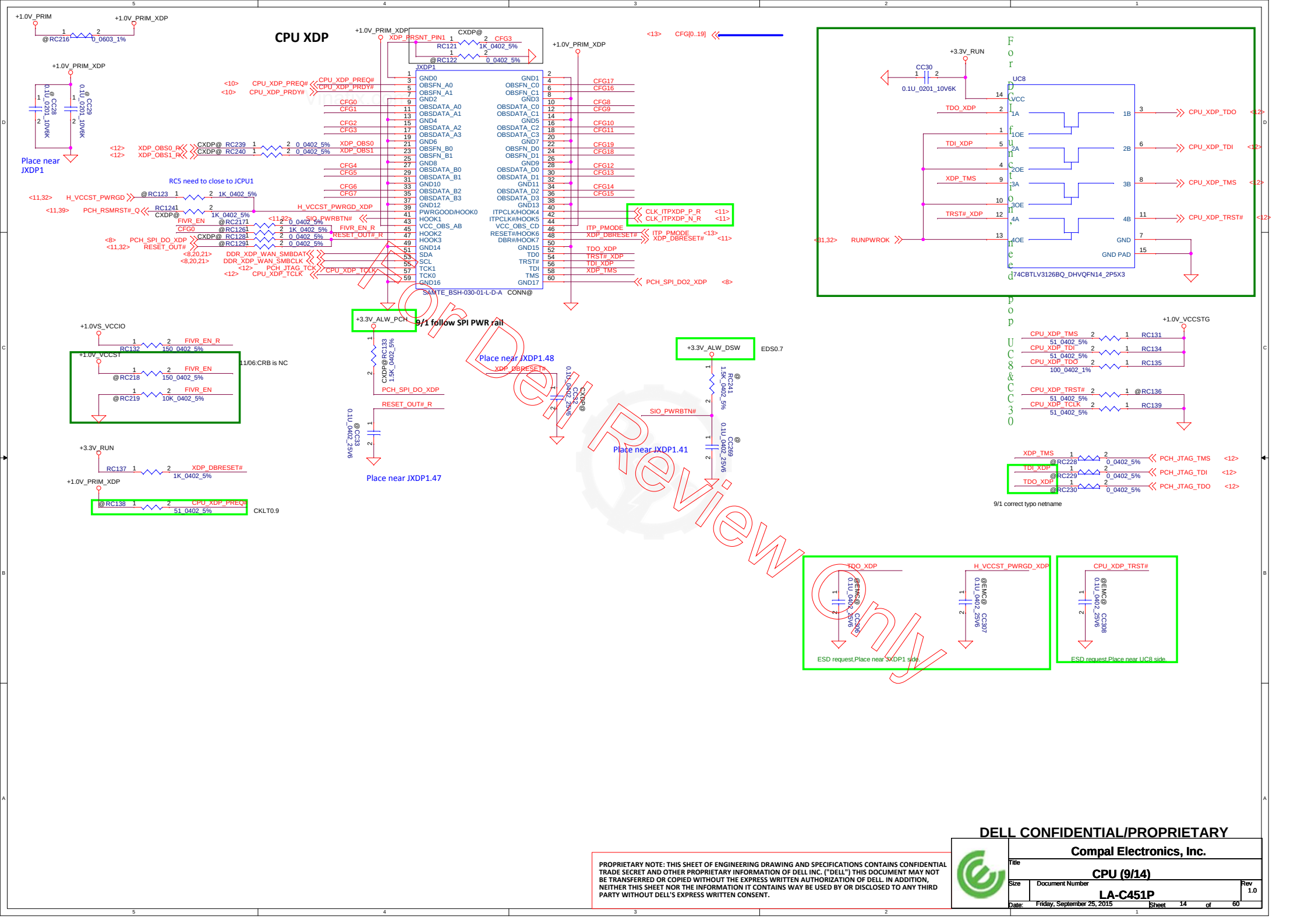
CPU XDP



Compal Electronics, Inc.

Title: CPU (9/14)

Size: | Document Number: LA-C451P | Rev: 1.0

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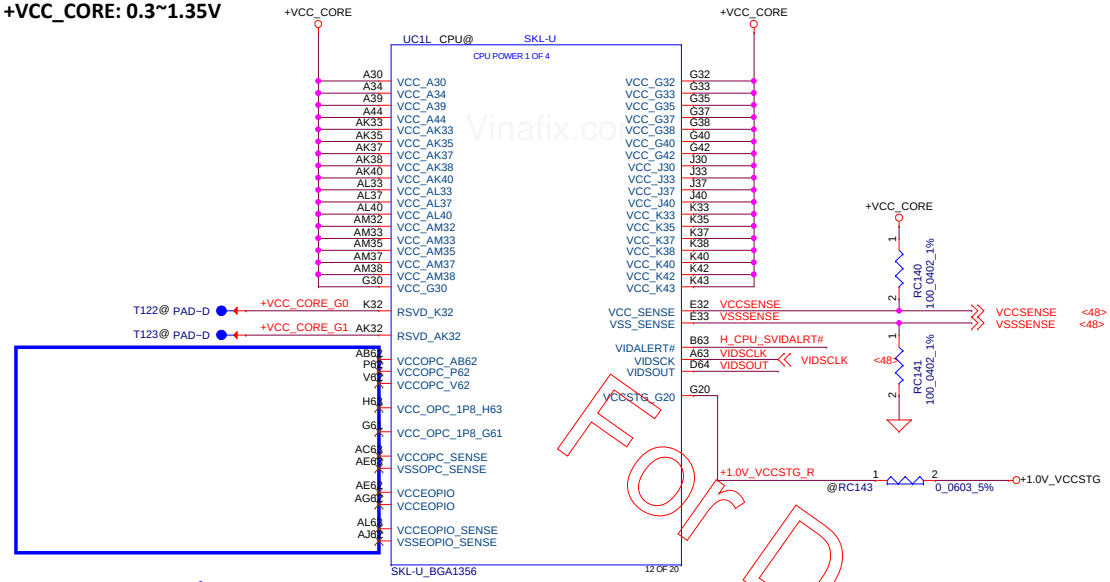
+VCC_CORE: 0.3~1.35V

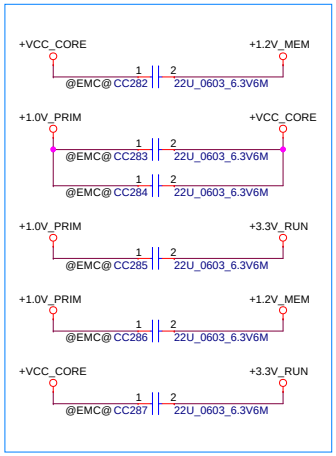


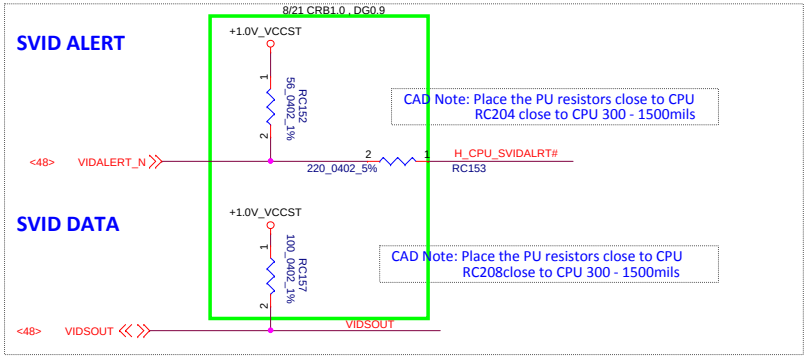
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

ESD Request





Compal Electronics, Inc.

Title: CPU (10/14)

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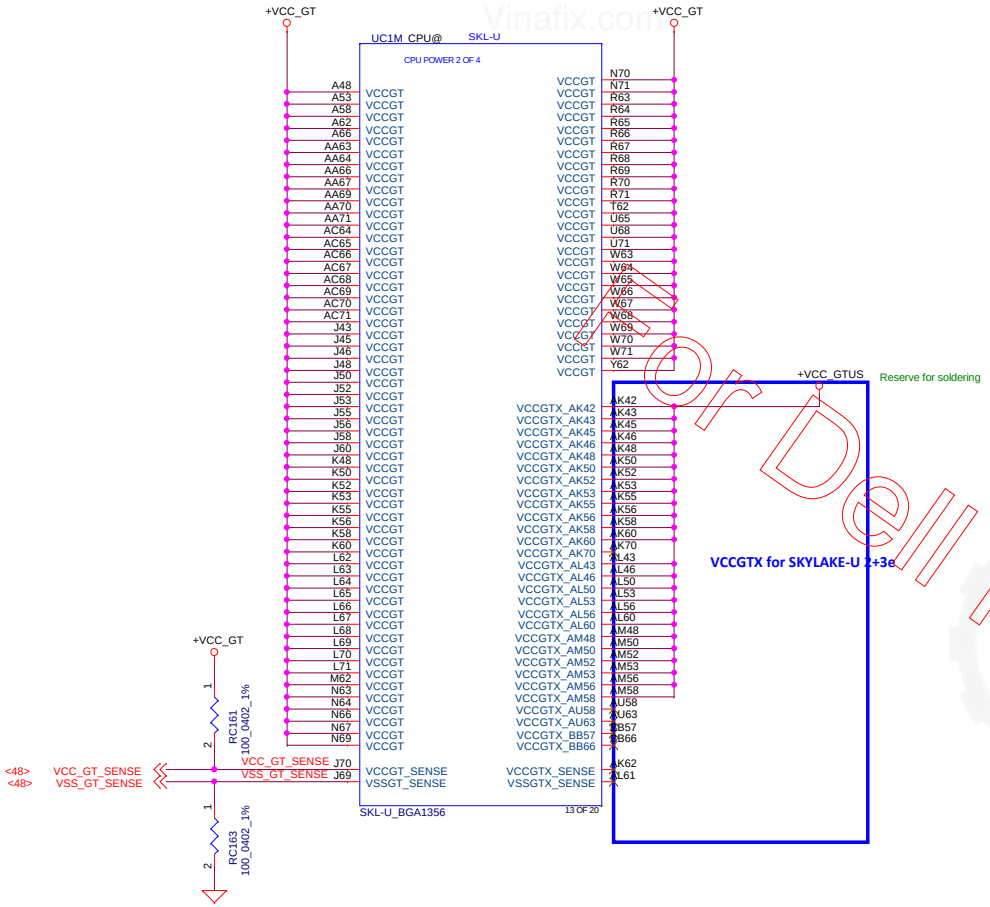
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



Compal Electronics, Inc.

Title: CPU (11/14)

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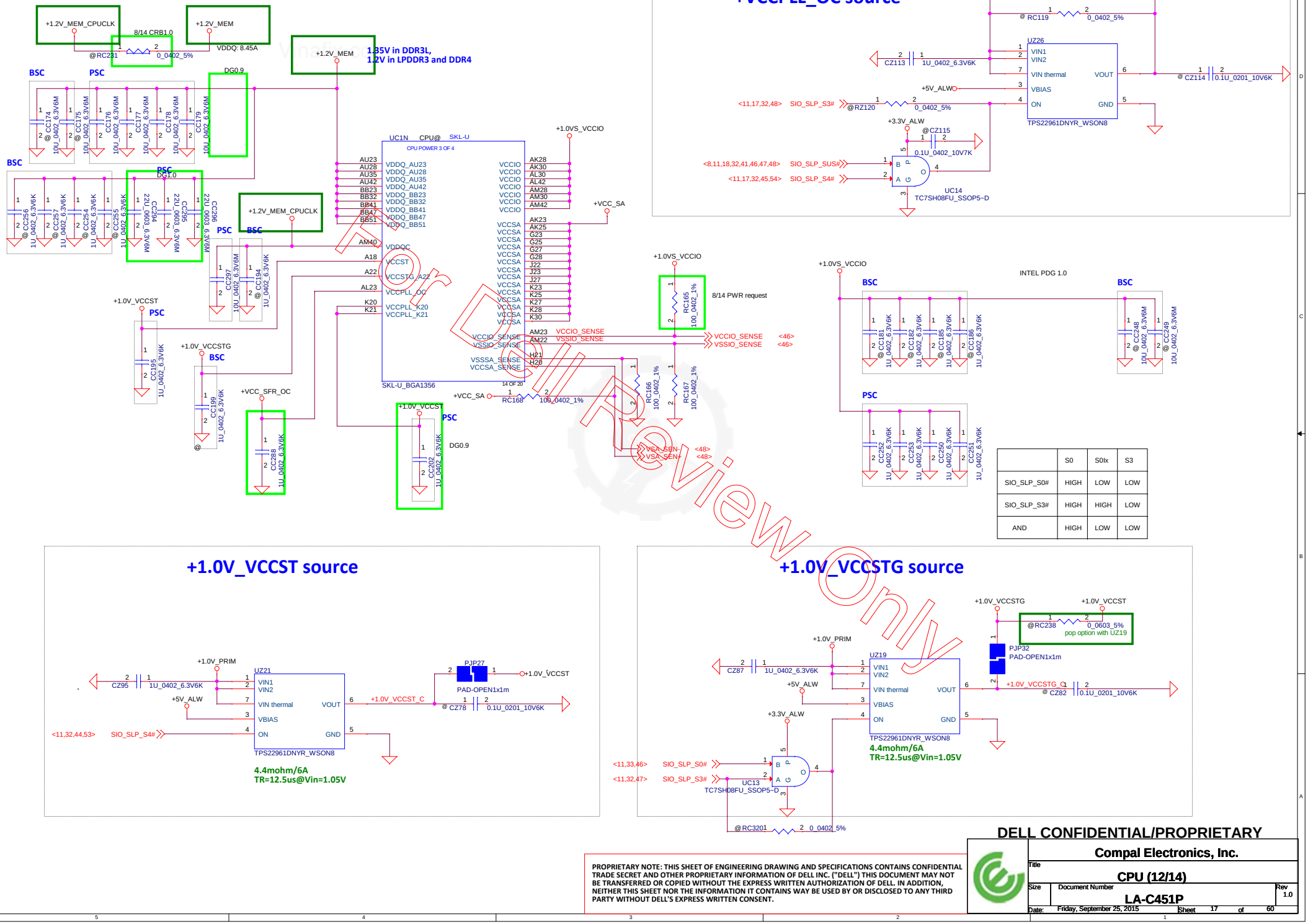
Date: Friday, September 25, 2015 | Sheet 16 of 60



	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

Compal Electronics, Inc.

Title: CPU (12/14)

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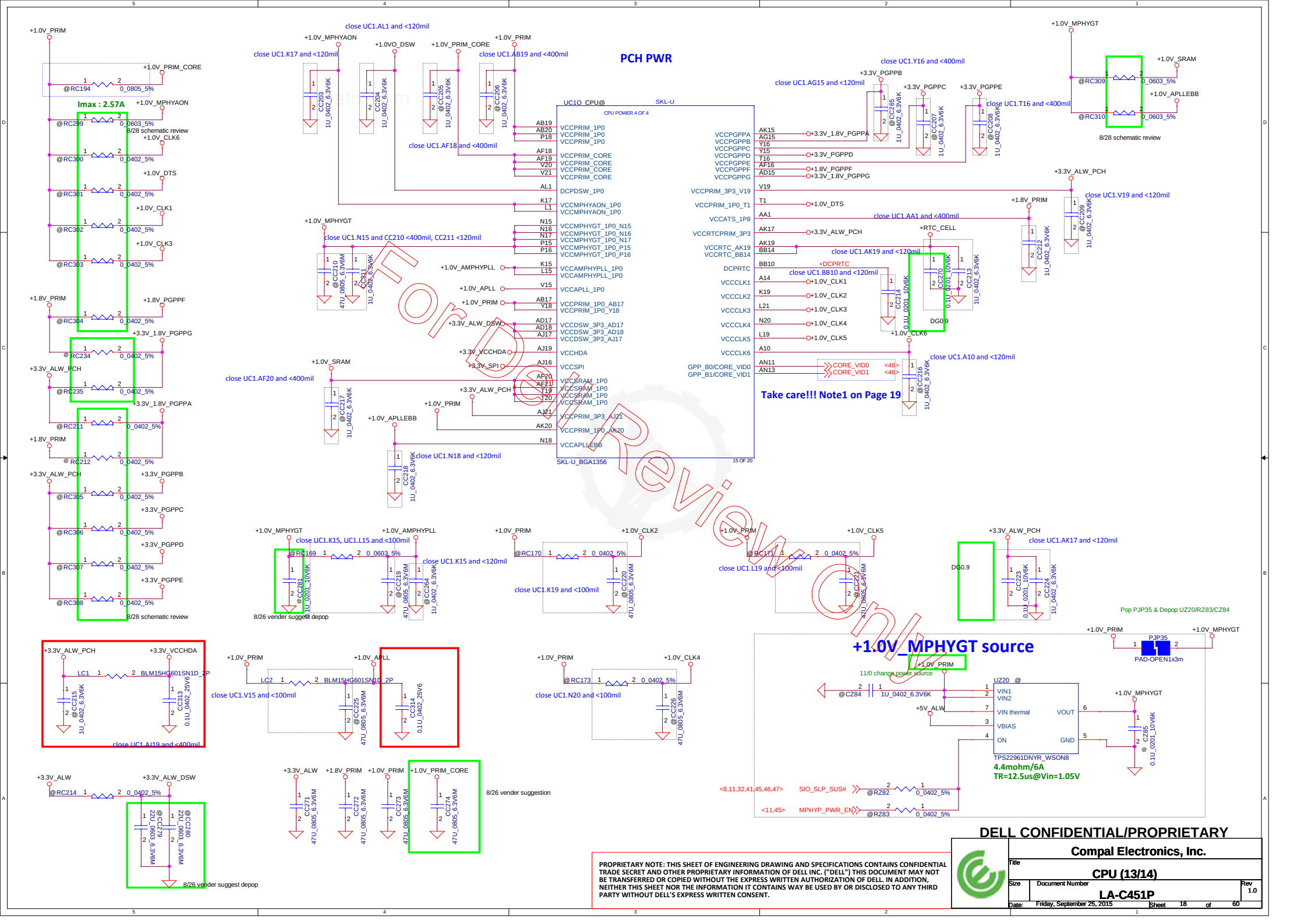
PCH PWR
Imax : 2.57A
UC1O_CPU@
SKL-U
CPU POWER 4 OF 4
SKL-U_BGA1356
15 OF 20
Take care!!! Note1 on Page 19
+1.0V_MPHYGT source
11/0 change power source
TPS22961DNYR_WSON8
4.4mohm/6A
TR=12.5us@Vin=1.05V
8/28 schematic review
8/26 vender suggest depop
8/26 vender suggestion
Pop PJP35 & Depop UZ20/RZ83/CZ84
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CPU (13/14)
LA-C451P
Friday, September 25, 2015
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CPU@ UC1P SKL-U

GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58

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CPU@ UC1Q SKL-U

GND 2 OF 3

AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
	VSS	VSS	BA41

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CPU@ UC1R SKL-U

GND 3 OF 3

F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21
	VSS	VSS	

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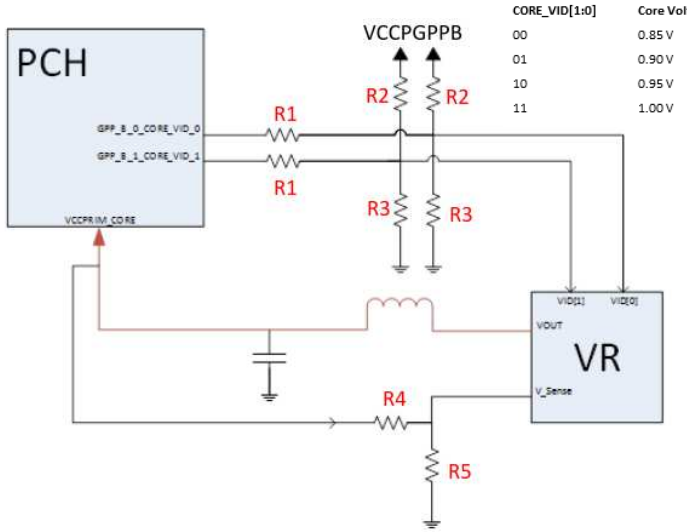
Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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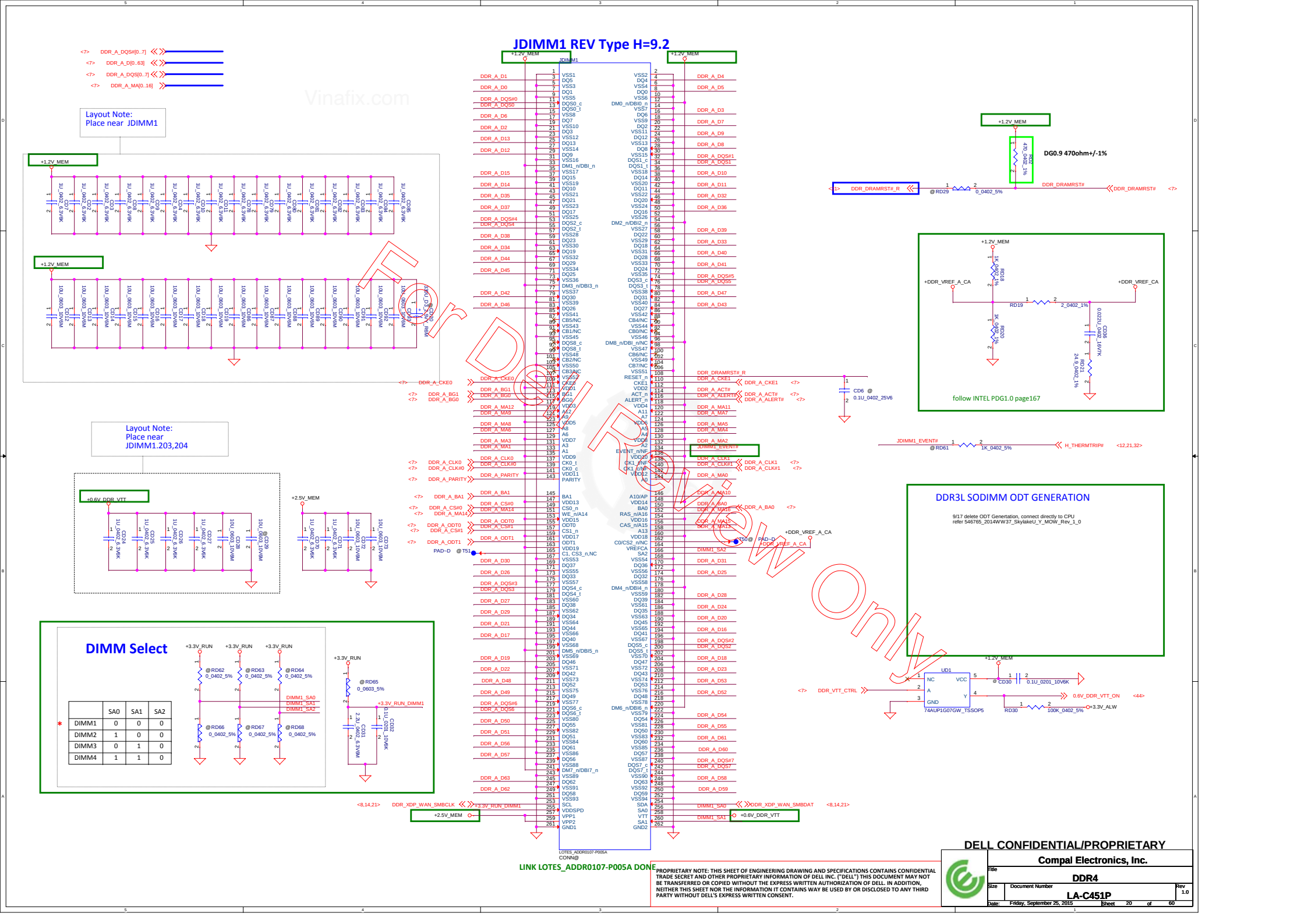
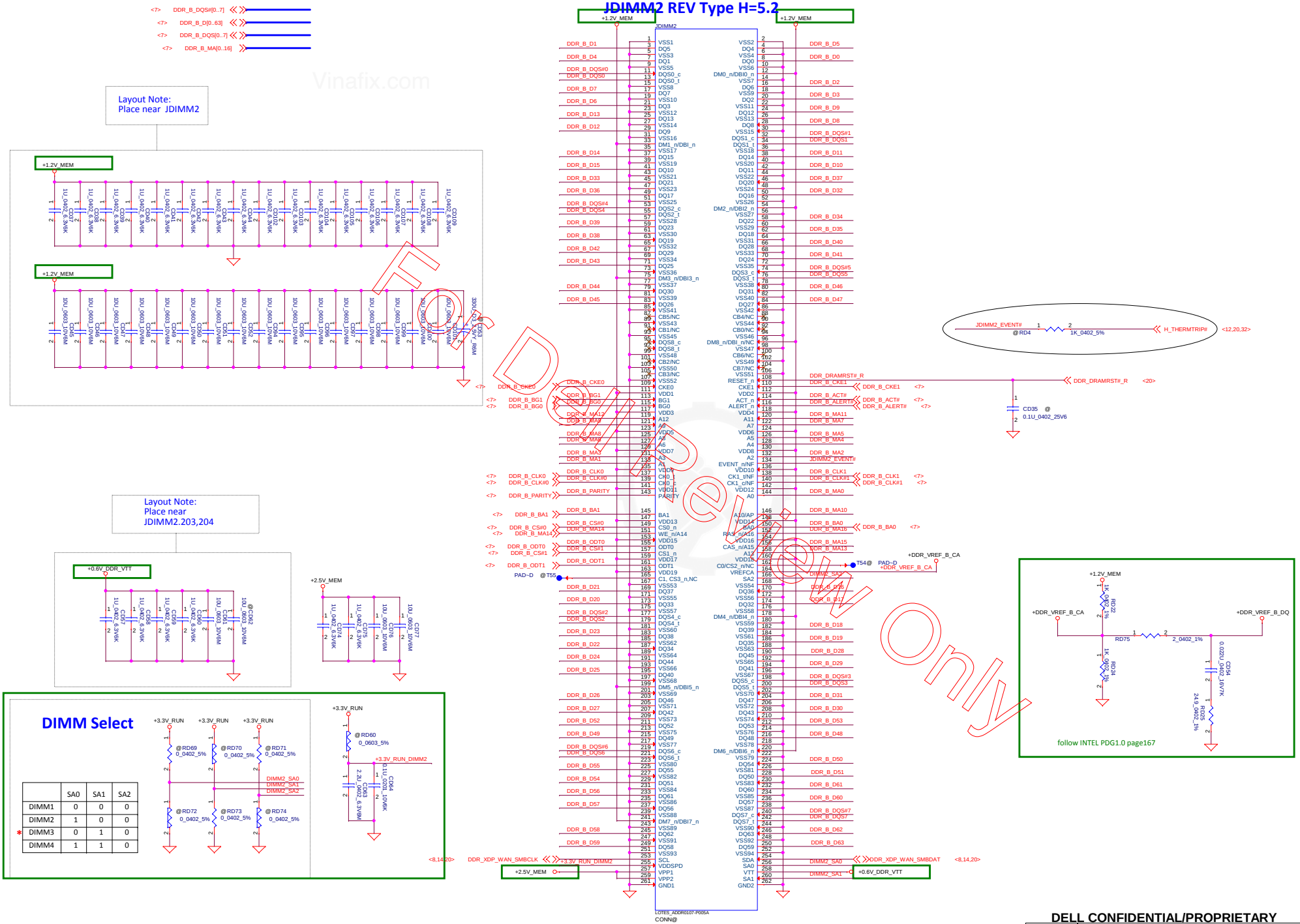
JDIMM1 REV Type H=9.2



JDIMM2 REV Type H=5.2



LINK LOTES_ADDR0107-P005A DONE

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Title	DDR4
Size	Document Number: LA-C451P
Rev	1.0
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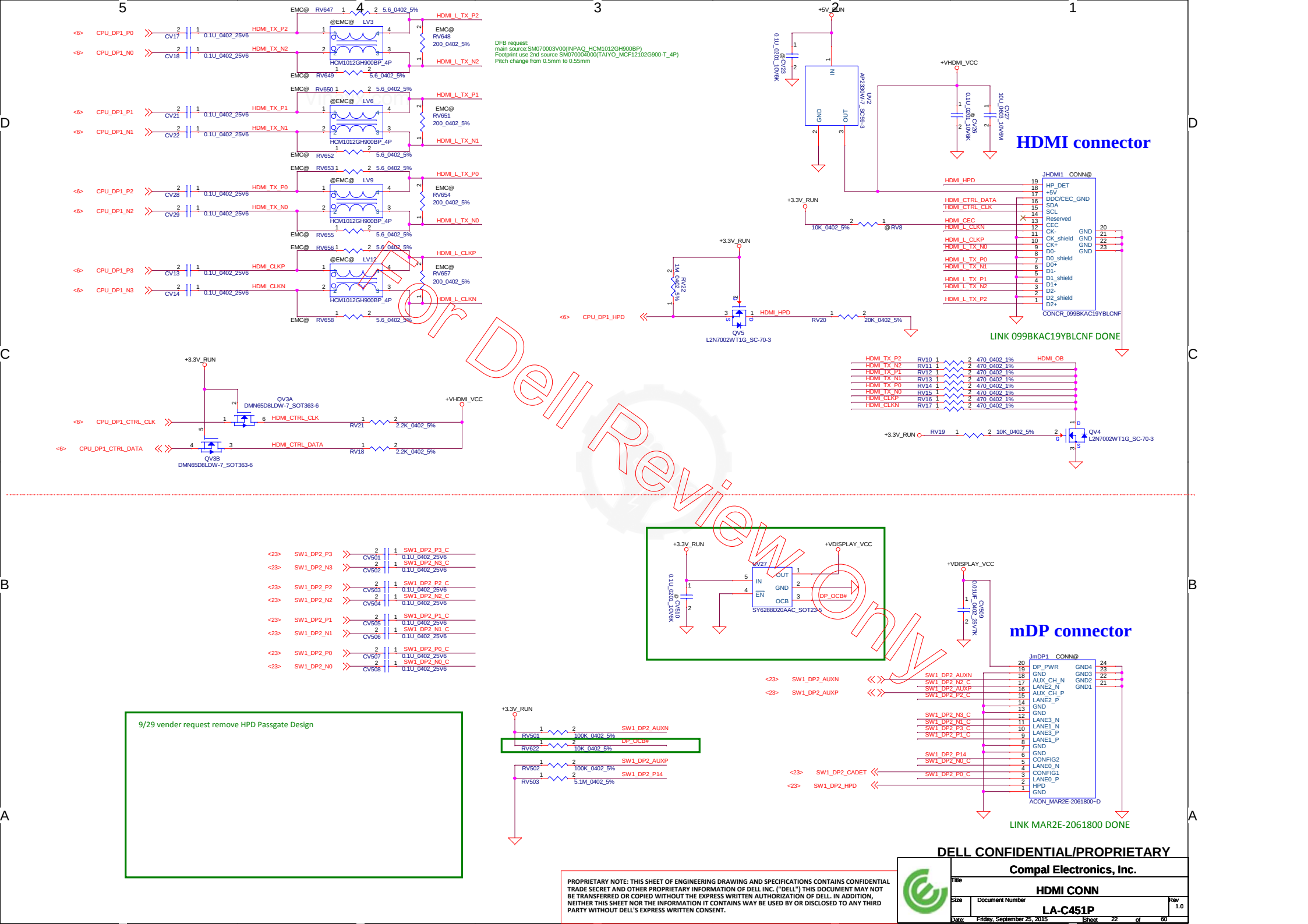
HDMI connector
mDP connector
DFB request:
main source:SM070003V00(INPAQ_HCM1012GH900BP)
Footprint use 2nd source SM070004000(TAIYO_MCF12102G900-T_4P)
Pitch change from 0.5mm to 0.55mm
HCM1012GH900BP_4P
JHDMI1 CONN@
CONCR_099BKAC19YBLCNF
LINK 099BKAC19YBLCNF DONE
JmDP1 CONN@
ACON_MAR2E-2061800-D
LINK MAR2E-2061800 DONE
DMN65D8LDW-7_SOT363-6
L2N7002WT1G_SC-70-3
SY6288D20AAC_SOT23-5
AP2330W-7_SC59-3
9/29 vender request remove HPD Passgate Design
For Dell Review Only
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HDMI CONN
LA-C451P
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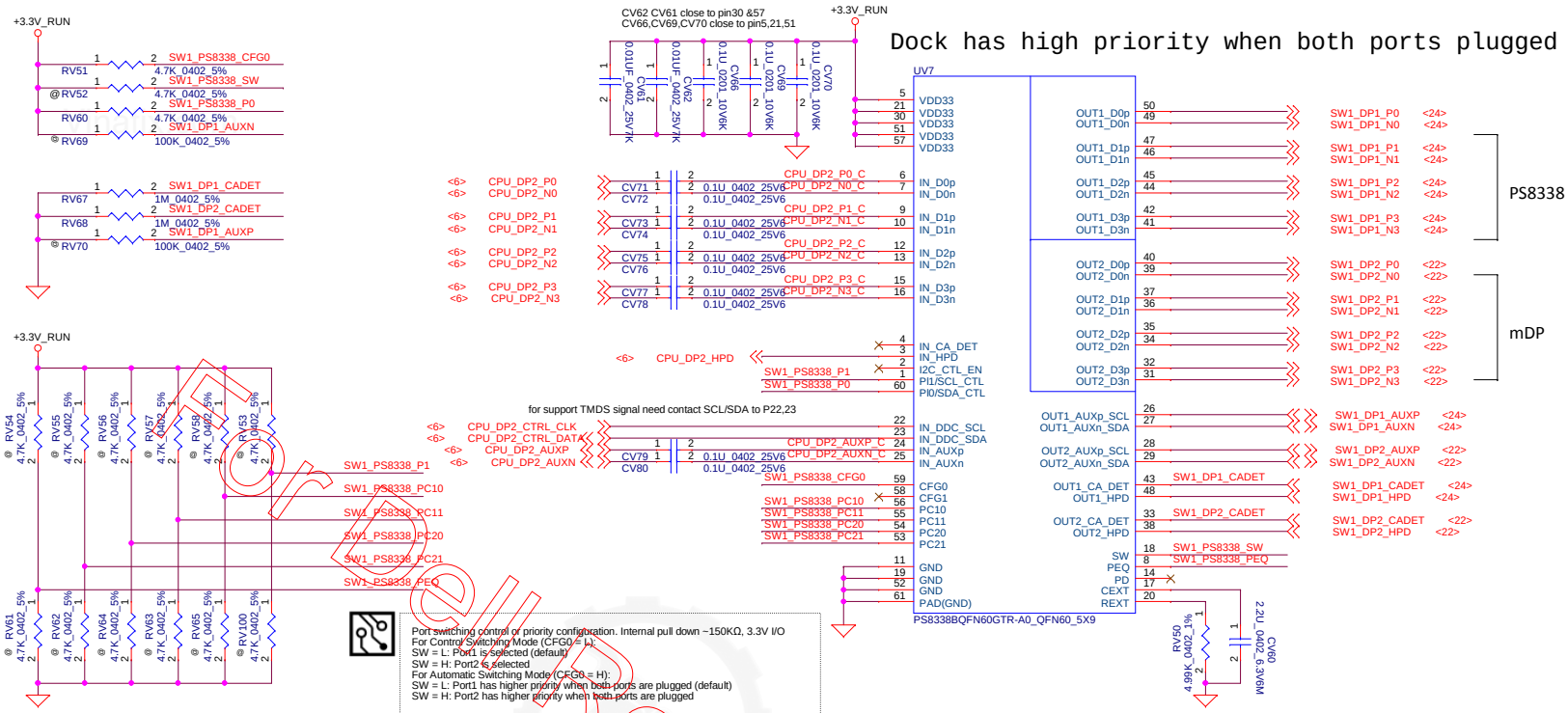

Compal Electronics, Inc.

Title: DP SW

Size | Document Number: LA-C451P | Rev: 1.0

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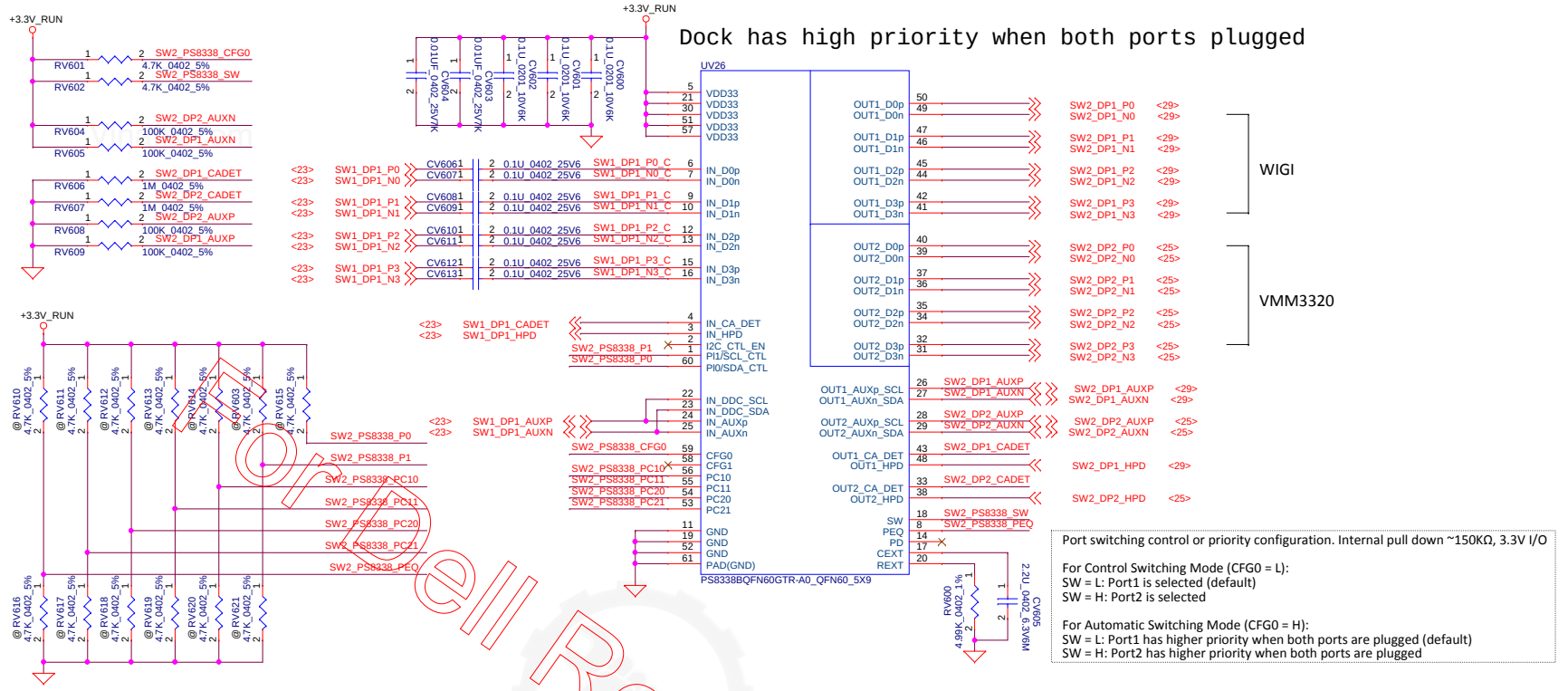

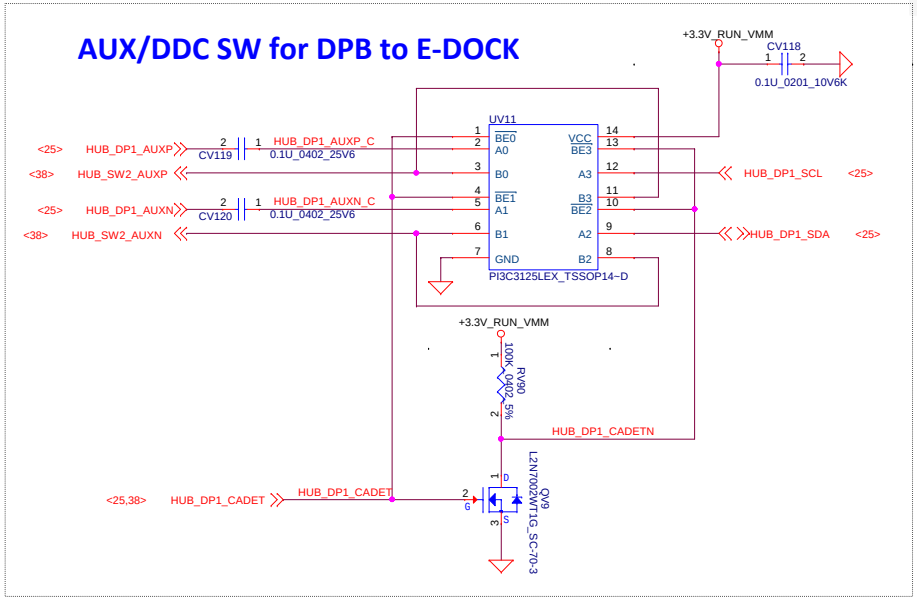

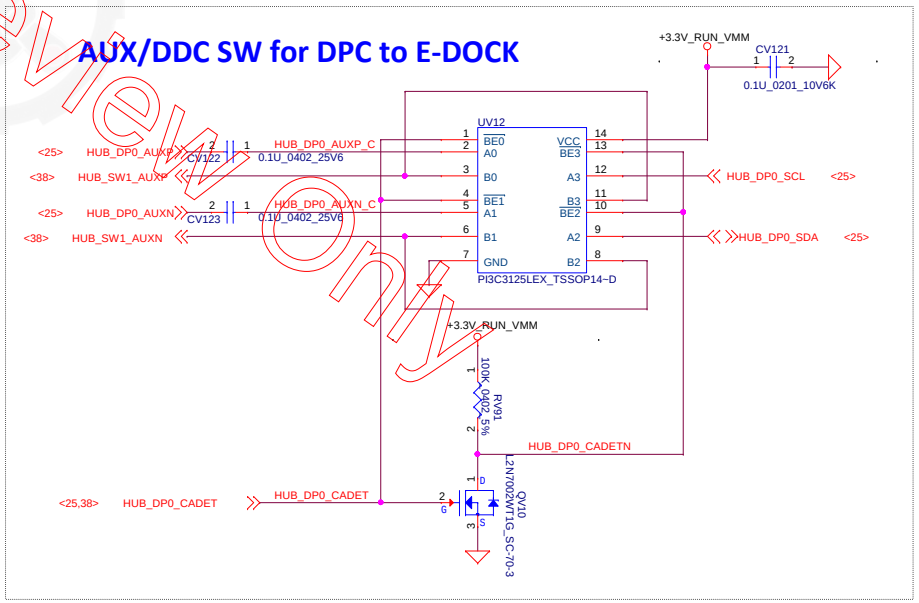

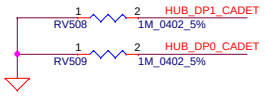

	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

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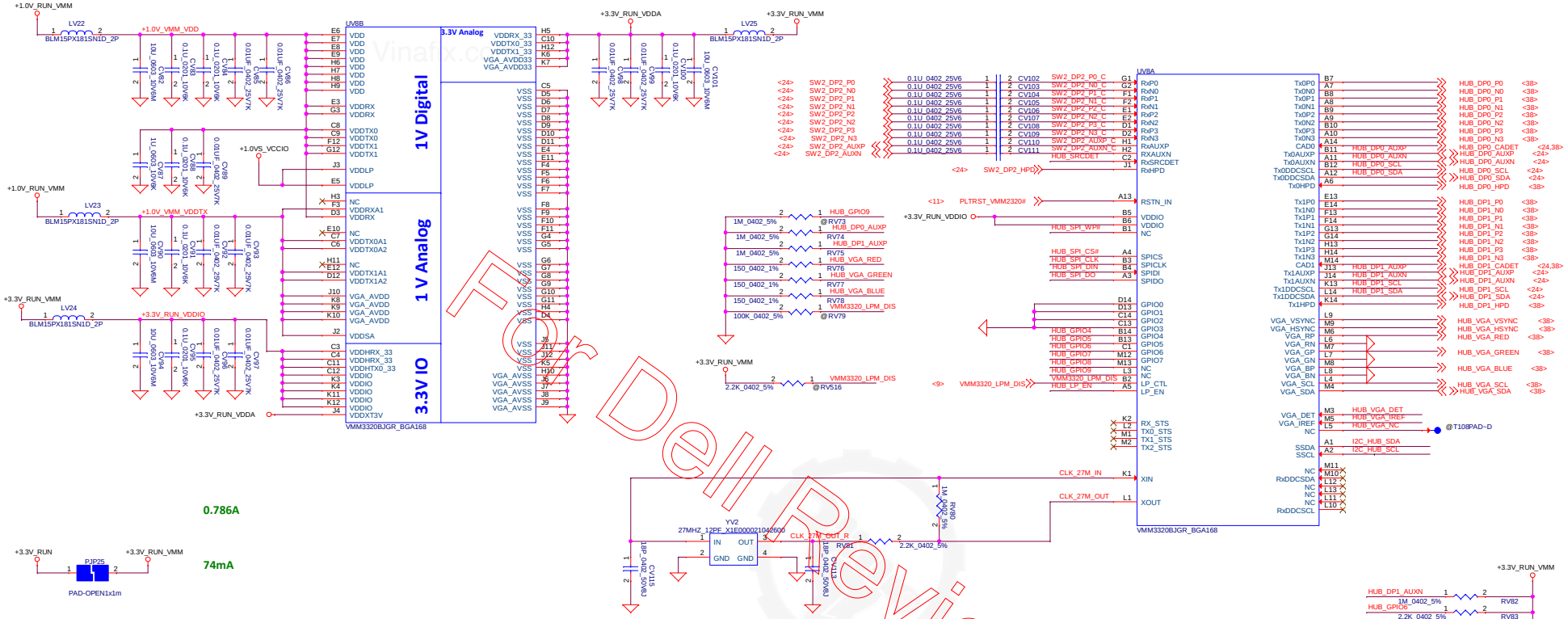
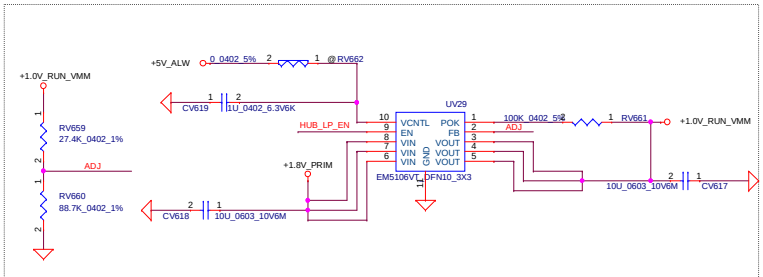
Compal Electronics, Inc.

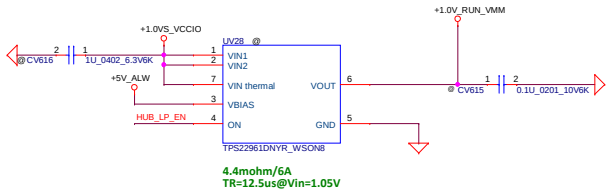
Title	DP SW	
Size	Document Number: LA-C451P	Rev: 1.0
Date: Friday, September 25, 2015	Sheet 24 of 60	





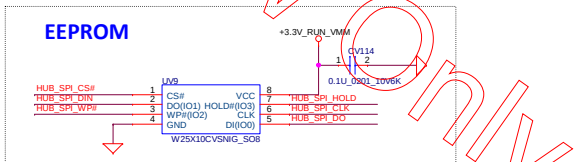
Low Power Mode by external Load switch

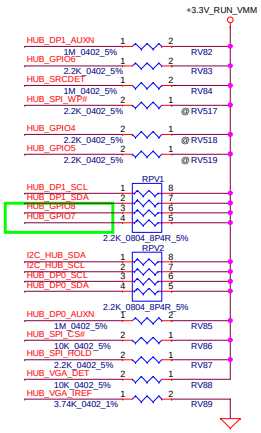
Pop UV29 &PJP37, depop PJP24&UV28 &PJP33



4.4mohm/6A
TR=12.5us@Vin=1.05V

VMM2320 Operation power consumption for 1.0V=1.464A (Max)





PRODUCT SUMMARY (SI3456DDV)			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[d]	Q_g (Typ.)
30	0.040 at V_{GS} = 10 V	6.3	2.8 nC
	0.050 at V_{GS} = 4.5 V	5.7	

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	DP 1.2 MST HUB
Size	Document Number: LA-C451P
Rev	1.0
Date:	Friday, September 25, 2015
Sheet	25 of 60

LINK 50398-04041-001 DONE

JEDP1 — ACES_50398-04041-001 CONN@

+3.3V_TSP

TOUCH_SCREEN_PD# <12>
DMIC0 <30>
DMIC_CLK0 <30>
+3.3V_RUN
+3.3V_CAM
USB20_N2_R
USB20_P2_R
CAM_MIC_CBL_DET# <10,12>
Pin15: LOOP_BACK
+BL_PWR_SRC
EMC@LV1 BLM15BB221SN1D_2P
BIA_PWM
DISP_ON
EDP_HPD <6>
LCD_TST <31>
+LCDVDD
TOUCH_SCREEN_DET#
EDP_AUXN_C CV1 0.1U_0402_25V6 EDP_AUXN <6>
EDP_AUXP_C CV2 0.1U_0402_25V6 EDP_AUXP <6>
EDP_TXP0_C CV3 0.1U_0402_25V6 EDP_TXP0 <6>
EDP_TXN0_C CV4 0.1U_0402_25V6 EDP_TXN0 <6>
EDP_TXP1_C CV5 0.1U_0402_25V6 EDP_TXP1 <6>
EDP_TXN1_C CV6 0.1U_0402_25V6 EDP_TXN1 <6>
TOUCH_SCREEN_DET# <12>
LCD_CBL_DET# <9>
@EMC@ CA5 100P_0402_50V8J
@EMC@ CA6 100P_0402_50V8J

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events
USB20_N9_R
USB20_P9_R
EXC24CQ900U_4P LV27 EMC@
USB20_N9 <10>
USB20_P9 <10>

@EMC@ DV4 AZC199-02SPR7G_SOT23-3
ESD depop location

+3.3V_RUN
10K_0402_5% RV623
TOUCH_SCREEN_DET#

Due to BC12/14, PC12 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table

CONN@ JIR1 E-T_4251K-F06N-40L
+PWR_SRC
IR_CAM_DET# <9>

Link SP01001YO00 done

+BL_PWR_SRC — 0.1U_0603_50V7K @CV7 — Close to JEDP1.17~19
+LCDVDD — 0.1U_0201_10V6K @CV8 — Close to JEDP1.30~31
+3.3V_CAM — 0.1U_0201_10V6K @CZ1 — Close to JEDP1.11
+3.3V_TSP — 0.1U_0201_10V6K @CZ2 — Close to JEDP1.1
+3.3V_RUN — 0.1U_0201_10V6K @CA7 — Close to JEDP1.10

DV1 BAT54CW_SOT323-3
BIA_PWM — RV1 4.7K_0402_5% — EDP_BIA_PWM <6> — BIA_PWM_EC <32>

DV2 BAT54CW_SOT323-3
DISP_ON — RV2 4.7K_0402_5% — PANEL_BKLEN <6> — PANEL_BKEN_EC <31>

For Touchscreen

+3.3V_RUN — 10K_0402_5% RV6 — QV8 LP2301ALT1G_SOT23-3 — +3.3V_TSP / +3.3V_RUN
<9> 3.3V_TS_EN — QV7 L2N7002WT1G_SC-70-3

WebCAM

+3.3V_CAM / +3.3V_RUN — QZ1 LP2301ALT1G_SOT23-3
<11> 3.3V_CAM_EN#

EXC24CQ900U_4P LZ1 EMC@
<10> USB20_P2 — USB20_P2_R
<10> USB20_N2 — USB20_N2_R

Backlight POWER

+PWR_SRC — QV1 AO6405_TSOP6 — +BL_PWR_SRC
CV11 1000P_0402_50V7K
RV4 270K_0402_5%
CV12 0.1U_0603_50V7K
BL_PWR_SRC_ON
QV2 L2N7002WT1G_SC-70-3
RV5 47K_0402_5%
CV374 0.01U_0402_50V7K
<32> EN_INVPWR

LCDVDD POWER

+LCDVDD — @CV9 10U_0603_10V6M — PJP29 PAD-OPEN1x1m — +EDP_VDD
UV24 G524B1T11U_SOT23-5 (VOUT / VIN / GND / EN / /OC)
+3.3V_ALW — @CV10 0.01UF_0402_25V7K
<31> LCD_VCC_TEST_EN
<6,32> ENVDD_PCH
DV3 BAT54CW_SOT323-3
EN_LCDPWR
RV3 100K_0402_5%

Compal Electronics, Inc.

Title: eDP CONN & Touch screen
Size: Document Number: LA-C451P
Rev: 1.0
Date: Friday, September 25, 2015
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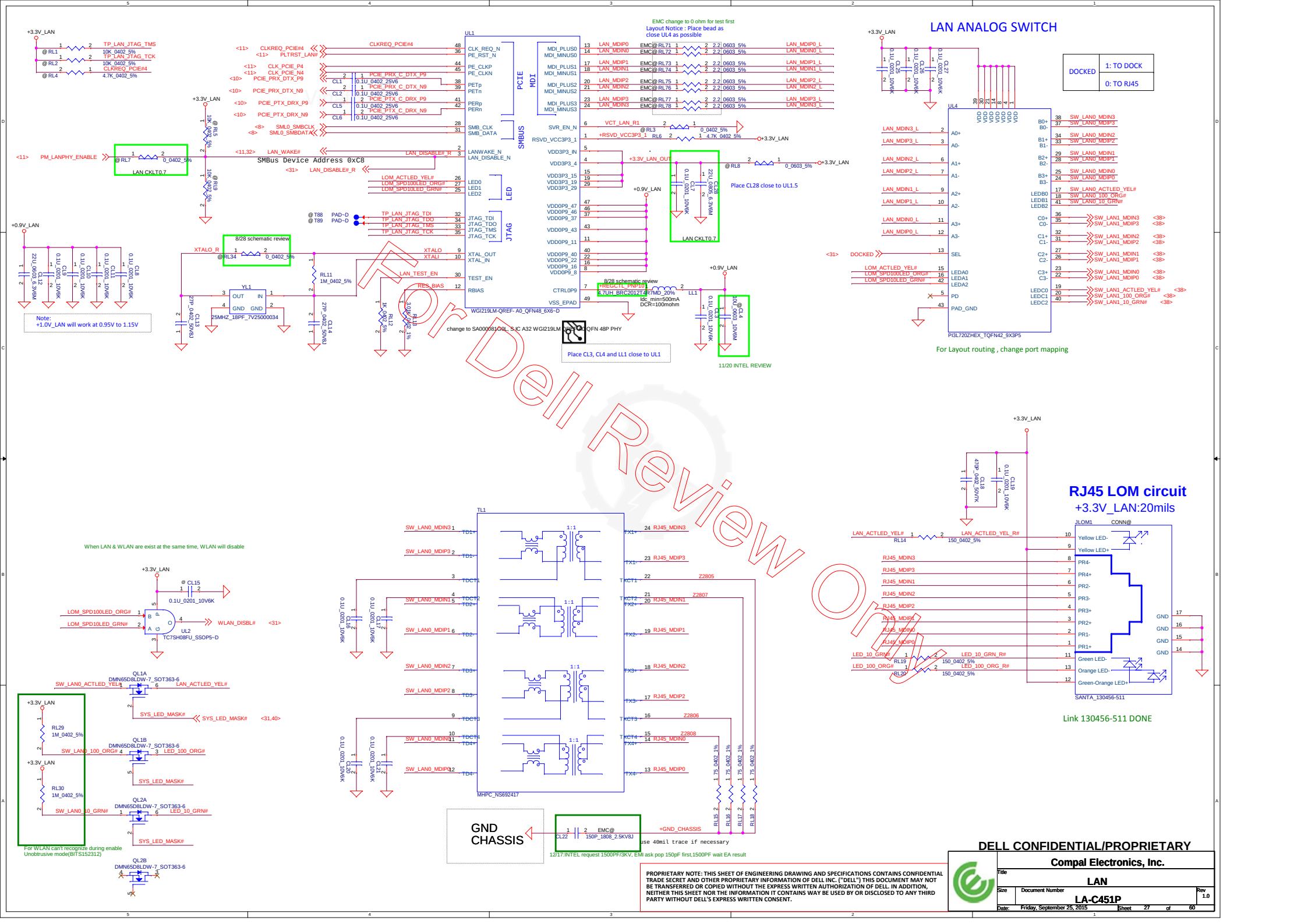


DOCKED	1: TO DOCK
	0: TO RJ45

EMC change to 0 ohm for test first
Layout Notice : Place bead as close UL4 as possible

SMBus Device Address 0xC8

Note: +1.0V_LAN will work at 0.95V to 1.15V

When LAN & WLAN are exist at the same time, WLAN will disable

For WLAN can't recognize during enable Unobtrusive mode(BIT5152312)

GND CHASSIS

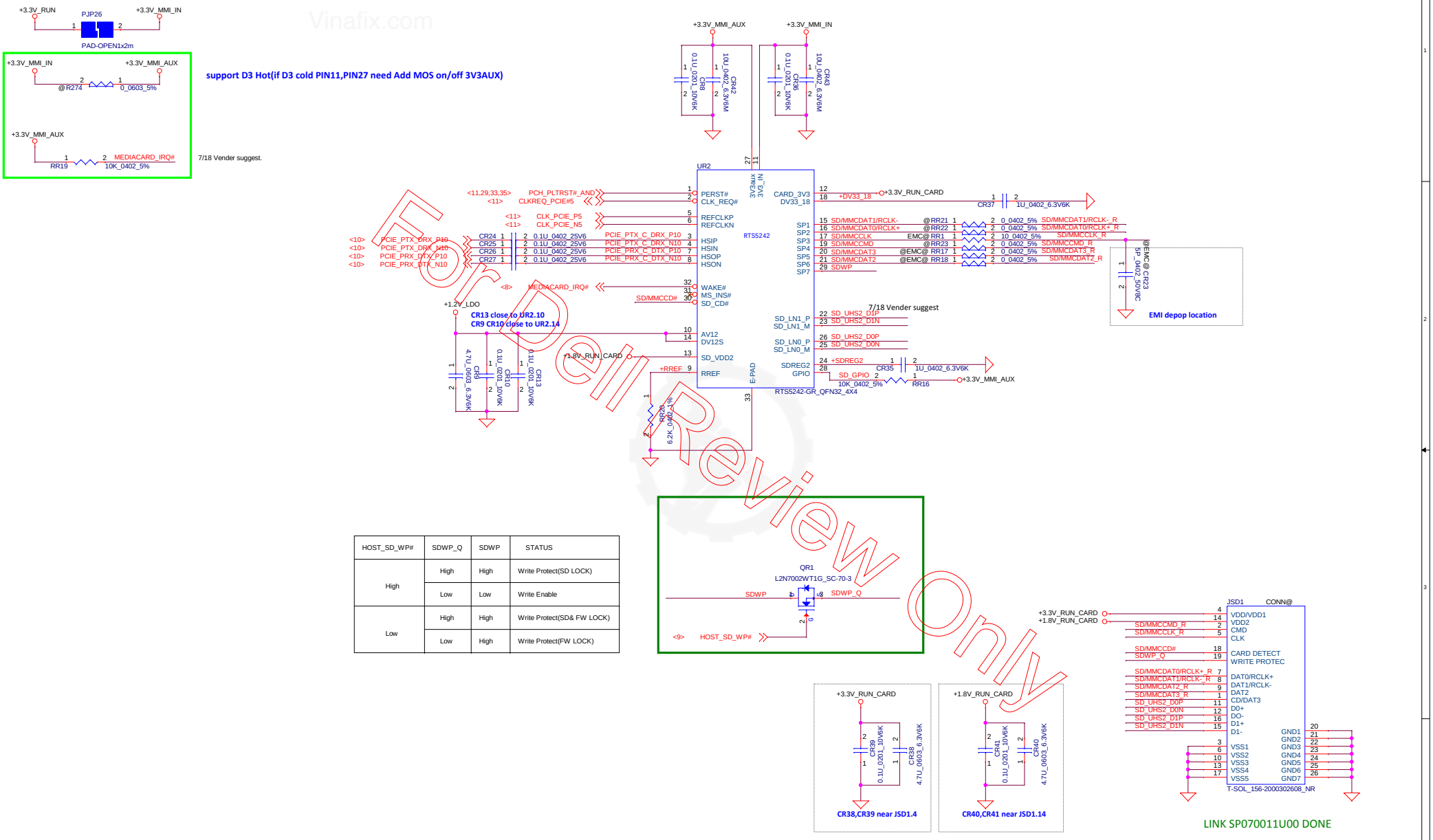
Use 40mil trace if necessary

Place CL28 close to UL1.5

Place CL3, CL4 and LL1 close to UL1

change to SA000081G9L, S IC A32 WGI219LM QFN 48P QFN 48P PHY

Compal Electronics, Inc.			
Title: LAN			
Size	Document Number: LA-C451P		Rev: 1.0
Date: Friday, September 25, 2015	Sheet 27 of 60		



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

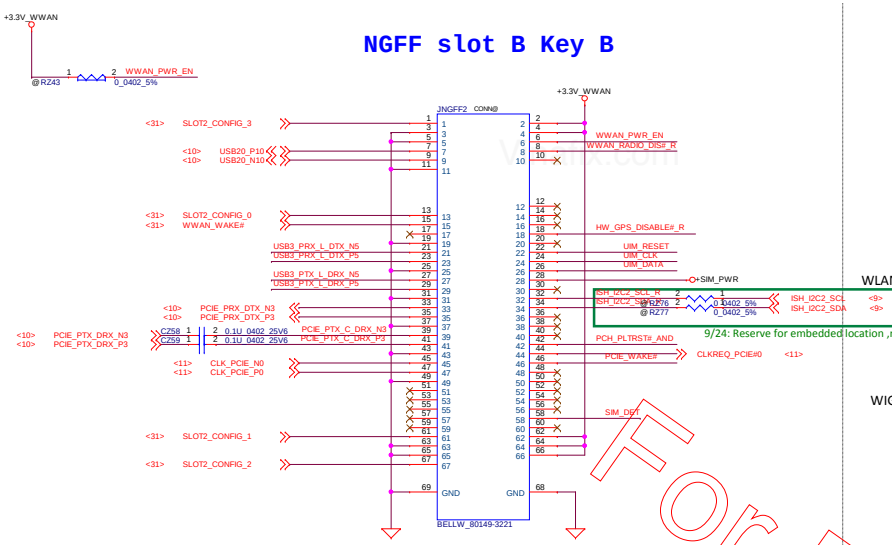
Compal Electronics, Inc.

Title: Card Reader

Size: | Document Number: LA-C451P | Rev: 1.0

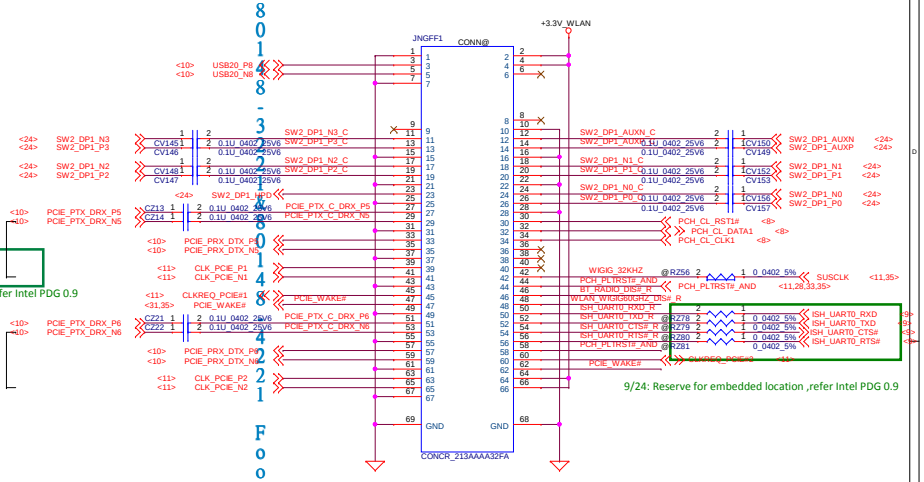
Date: Friday, September 25, 2015 | Sheet 28 of 60

NGFF slot B Key B



9/24: Reserve for embedded location ,refer Intel PDG 0.9

NGFF slot A Key A

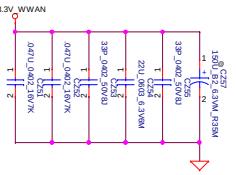


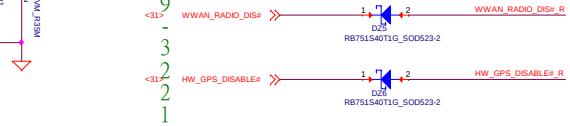
9/24: Reserve for embedded location ,refer Intel PDG 0.9

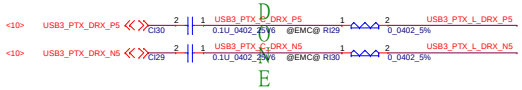
WLAN

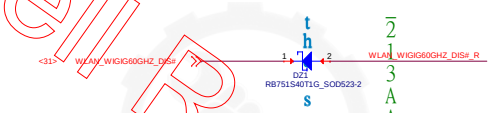
WIGI

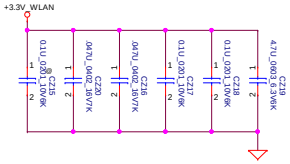
8014983221 Footprint same as CONCR_213AAAA32FA LINK DONE







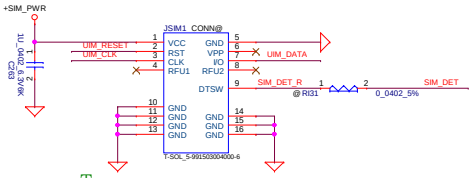




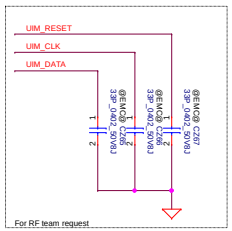
Power Rating TBD

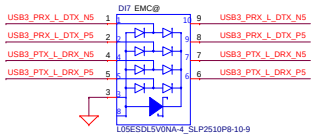
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

SIM Card Push-Push



T-SOL_5-9915030040000-6





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Compal Electronics, Inc.

Title	NGFF Card	
Size	Document Number	Rev
	LA-C451P	1.0
Date: Friday, September 25, 2015	Sheet 29 of 60	

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Link 50279-0040N-001 DONE

Close to UA1

Close to UA1 pin6

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

1A

5mA

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place RA9 close to codec

Place RA32 close to codec

Place CA29 close to Codec

place at AGND and DGND plane

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

Global Headset
Universal Jack

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

Normal
Open

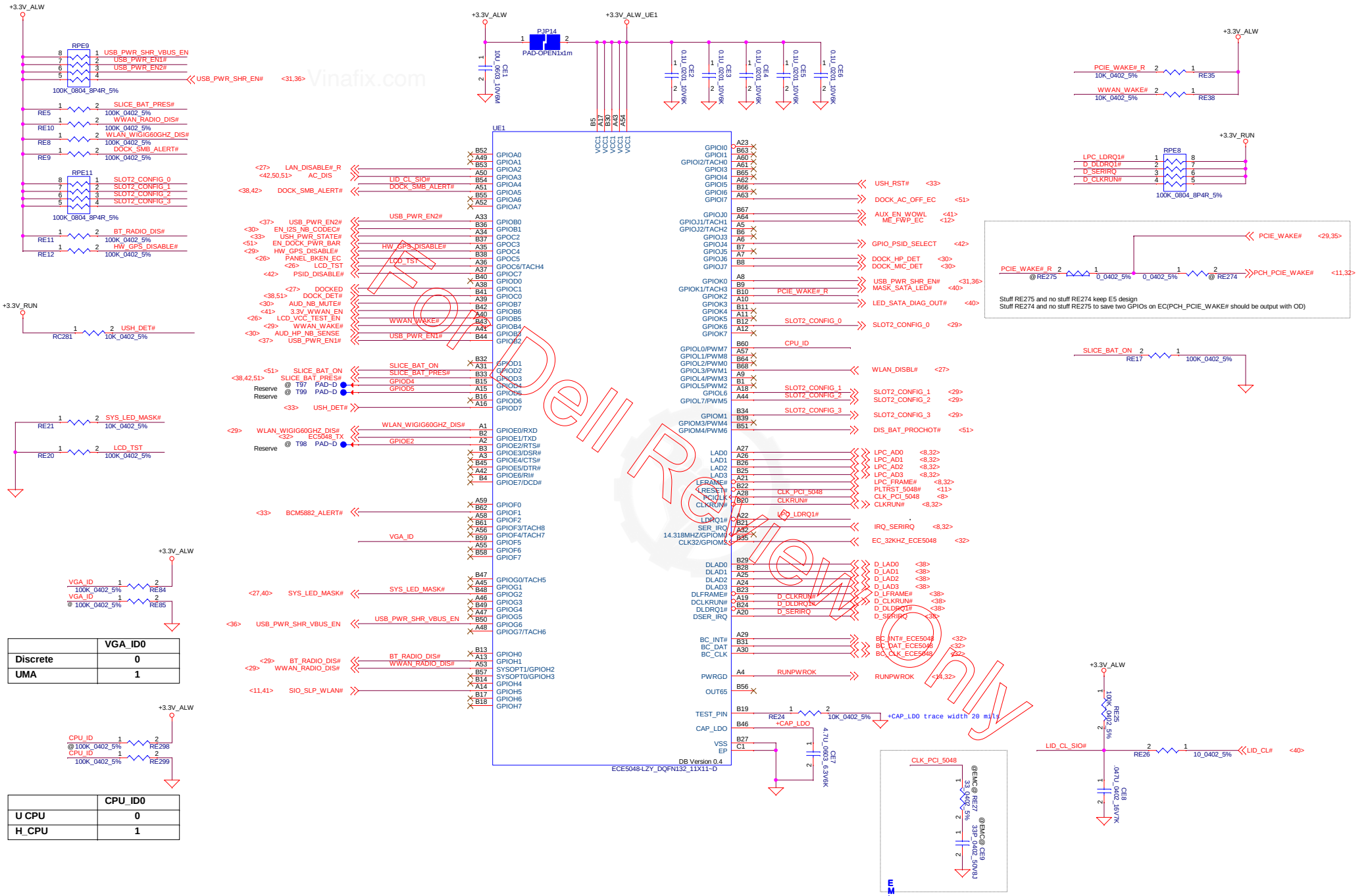
Link 2SJ3095-022111F DONE

Compal Electronics, Inc.

Title: Codec ALC3235

Size: | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 30 of 60



	VGA_ID0
Discrete	0
UMA	1

	CPU_ID0
U CPU	0
H_CPU	1

Compal Electronics, Inc.	
Title	ECE5048
Size	Document Number: LA-C451P
Rev	1.0
Date:	Friday, September 25, 2015
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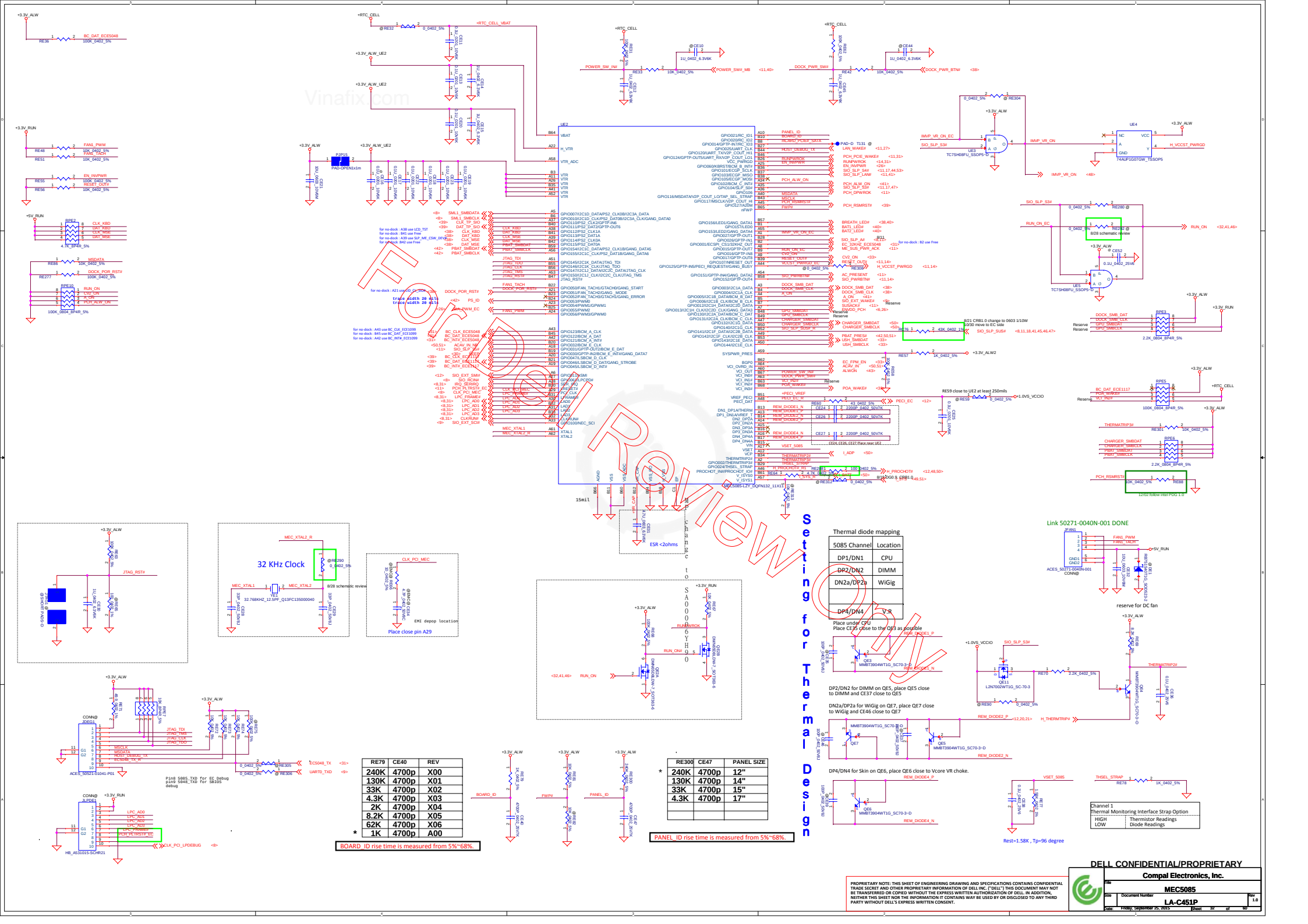
Vinafix.com
For Review Only
MEC5085
ESR <2ohms
32 KHz Clock
EMI depop location
Place close pin A29
Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | DIMM
DN2a/DP2a | WiGig
DP4/DN4 | V.R
Place under CPU
Place CE35 close to the QE3 as possible
DP2/DN2 for DIMM on QE5, place QE5 close to DIMM and CE37 close to QE5
DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig and CE46 close to QE7
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
Rest=1.58K , Tp=96 degree
Link 50271-0040N-001 DONE
reserve for DC fan
Channel 1
Thermal Monitoring Interface Strap Option
HIGH | Thermistor Readings
LOW | Diode Readings
RE79 | CE40 | REV
240K | 4700p | X00
130K | 4700p | X01
33K | 4700p | X02
4.3K | 4700p | X03
2K | 4700p | X04
8.2K | 4700p | X05
62K | 4700p | X06
1K | 4700p | A00
BOARD_ID rise time is measured from 5%~68%.
RE300 | CE47 | PANEL SIZE
240K | 4700p | 12"
130K | 4700p | 14"
33K | 4700p | 15"
4.3K | 4700p | 17"
PANEL_ID rise time is measured from 5%~68%.
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Compal Electronics, Inc.
MEC5085
LA-C451P
Rev 1.0
Friday, September 25, 2015
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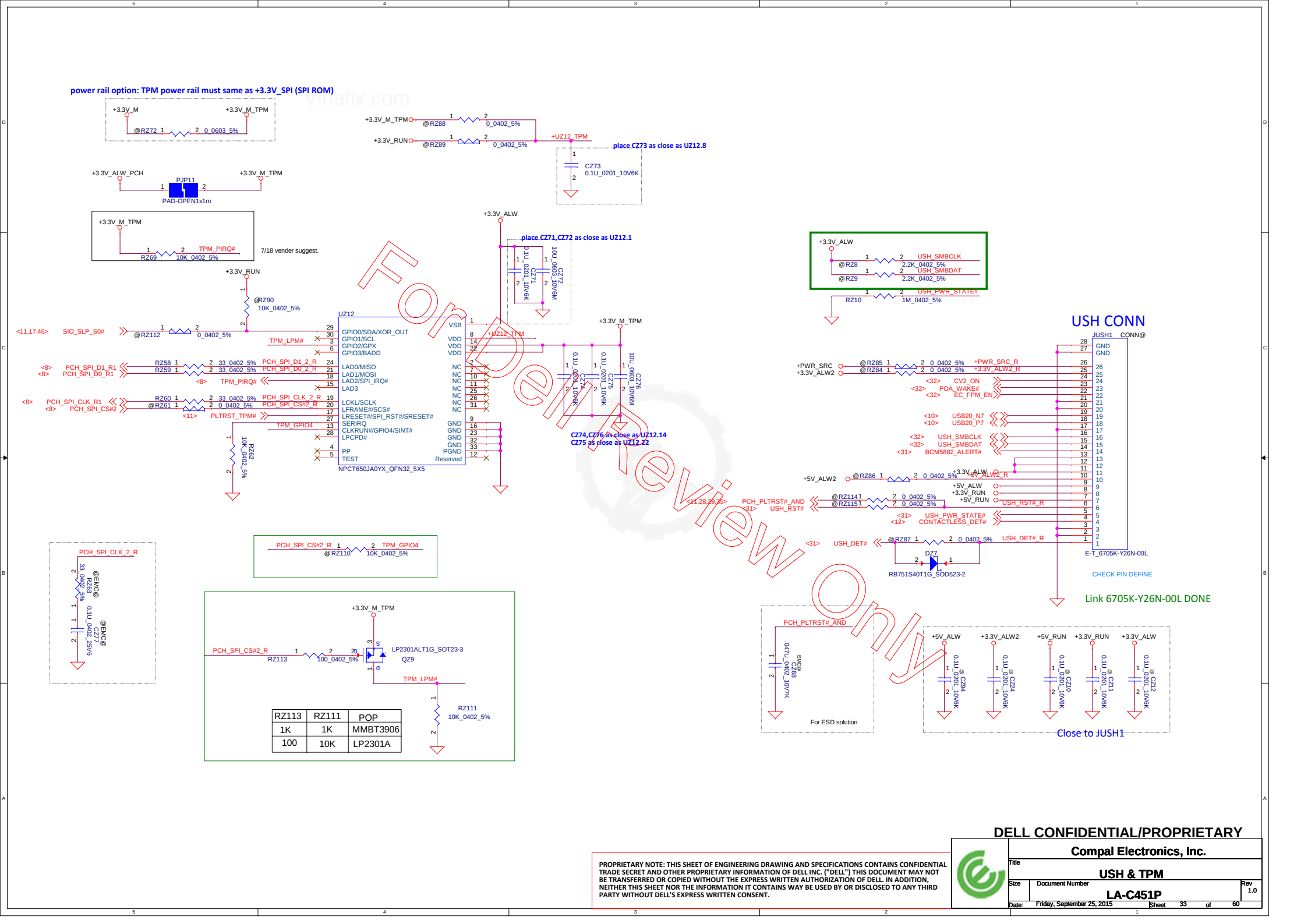
power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)
+3.3V_M
+3.3V_M_TPM
@RZ72 1
2 0 0603 5%
+3.3V_M_TPM
@RZ88 1
2 0_0402_5%
+3.3V_RUN
@RZ89 1
2 0_0402_5%
+UZ12_TPM
place CZ73 as close as UZ12.8
CZ73
0.1U_0201_10V6K
+3.3V_ALW_PCH
PJP11
PAD-OPEN1x1m
+3.3V_M_TPM
+3.3V_M_TPM
TPM_PIRQ#
RZ69
10K_0402_5%
7/18 vender suggest.
+3.3V_ALW
place CZ71,CZ72 as close as UZ12.1
CZ71
0.1U_0201_10V6K
CZ72
10U_0603_10V6M
+3.3V_RUN
@RZ90
10K_0402_5%
UZ12
<11,17,46> SIO_SLP_S0#
@RZ112 1
2 0_0402_5%
GPIO0/SDA/XOR_OUT
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD
TPM_LPM#
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3
<8> PCH_SPI_D1_R1
<8> PCH_SPI_D0_R1
RZ58 1
RZ59 1
2 33_0402_5%
PCH_SPI_D1_2_R
PCH_SPI_D0_2_R
<8> TPM_PIRQ#
<8> PCH_SPI_CLK_R1
<8> PCH_SPI_CS#2
RZ60 1
@RZ61 1
2 33_0402_5%
2 0_0402_5%
PCH_SPI_CLK_2_R
PCH_SPI_CS#2_R
<11> PLTRST_TPM#
LCKL/SCLK
LFRAME#/SCS#
LRESET#/SPI_RST#/SRESET#
SERIRQ
CLKRUN#/GPIO4/SINT#
LPCPD#
TPM_GPIO4
PP
TEST
NPCT650JA0YX_QFN32_5X5
VSB
VDD
VDD
VDD
NC
NC
NC
NC
NC
NC
NC
GND
GND
GND
GND
PGND
Reserved
+UZ12_TPM
+3.3V_M_TPM
CZ74
CZ75
CZ76
0.1U_0201_10V6K
0.1U_0201_10V6K
10U_0603_10V6M
CZ74,CZ76 as close as UZ12.14
CZ75 as close as UZ12.22
RZ62
10K_0402_5%
+3.3V_ALW
USH_SMBCLK
USH_SMBDAT
@RZ8
@RZ9
2.2K_0402_5%
USH_PWR_STATE#
RZ10
1M_0402_5%
USH CONN
JUSH1 CONN@
+PWR_SRC
+3.3V_ALW2
@RZ85 1
@RZ84 1
2 0_0402_5%
+PWR_SRC_R
+3.3V_ALW2_R
<32> CV2_ON
<32> POA_WAKE#
<32> EC_FPM_EN
<10> USB20_N7
<10> USB20_P7
<32> USH_SMBCLK
<32> USH_SMBDAT
<31> BCM5882_ALERT#
+5V_ALW2
@RZ86 1
+3.3V_ALW
+5V_ALW
+3.3V_RUN
+5V_RUN
<11,28,29,35> PCH_PLTRST#_AND
<31> USH_RST#
@RZ114 1
@RZ115 1
USH_RST#_R
<31> USH_PWR_STATE#
<12> CONTACTLESS_DET#
<31> USH_DET#
@RZ87 1
USH_DET#_R
DZ7
RB751S40T1G_SOD523-2
E-T_6705K-Y26N-00L
CHECK PIN DEFINE
Link 6705K-Y26N-00L DONE
PCH_SPI_CS#2_R
@RZ110 1
2 TPM_GPIO4
10K_0402_5%
PCH_SPI_CLK_2_R
RZ255
33_0402_5%
@EMC@
CZ77
0.1U_0402_25V6
@EMC@
+3.3V_M_TPM
PCH_SPI_CS#2_R
RZ113
100_0402_5%
LP2301ALT1G_SOT23-3
QZ9
TPM_LPM#
RZ111
10K_0402_5%
RZ113 | RZ111 | POP
1K | 1K | MMBT3906
100 | 10K | LP2301A
PCH_PLTRST#_AND
.047U_0402_16V7K
EMC@
CZ78
For ESD solution
+5V_ALW
+3.3V_ALW2
+5V_RUN
+3.3V_RUN
+3.3V_ALW
0.1U_0201_10V6K
CZ94
CZ24
CZ10
CZ11
CZ12
Close to JUSH1
For Dell Review Only
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
USH & TPM
Size
Document Number
LA-C451P
Rev
1.0
Date: Friday, September 25, 2015
Sheet 33 of 60
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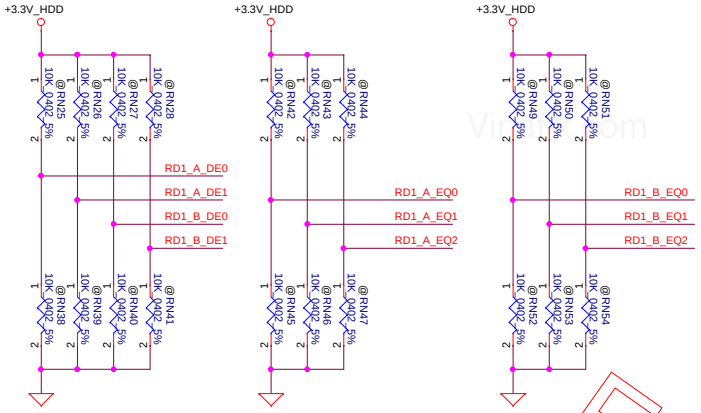


Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

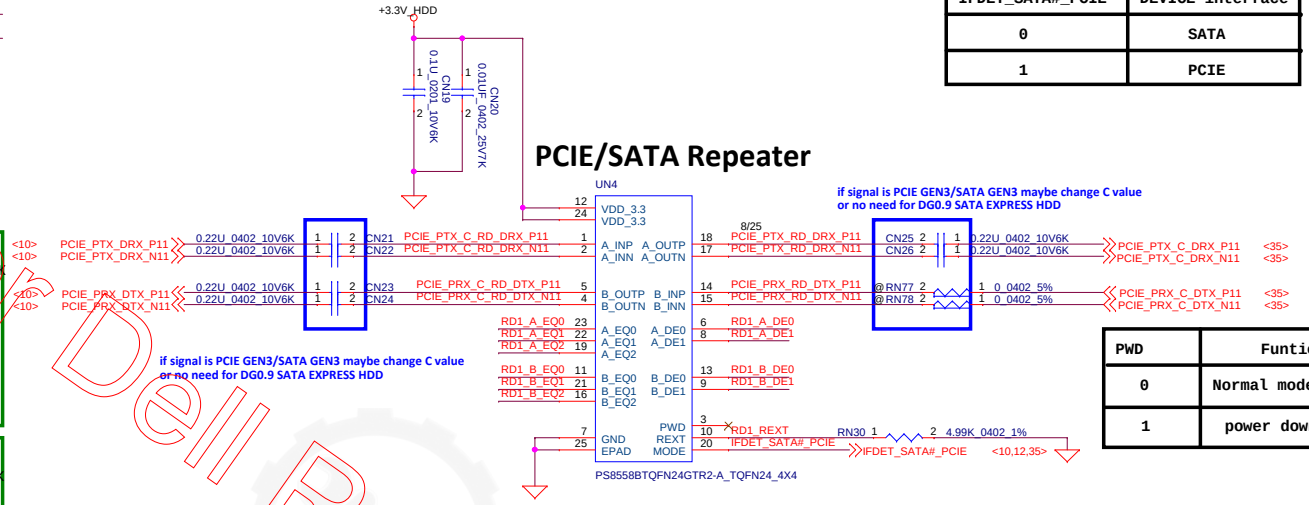
[B_DE1,B_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB

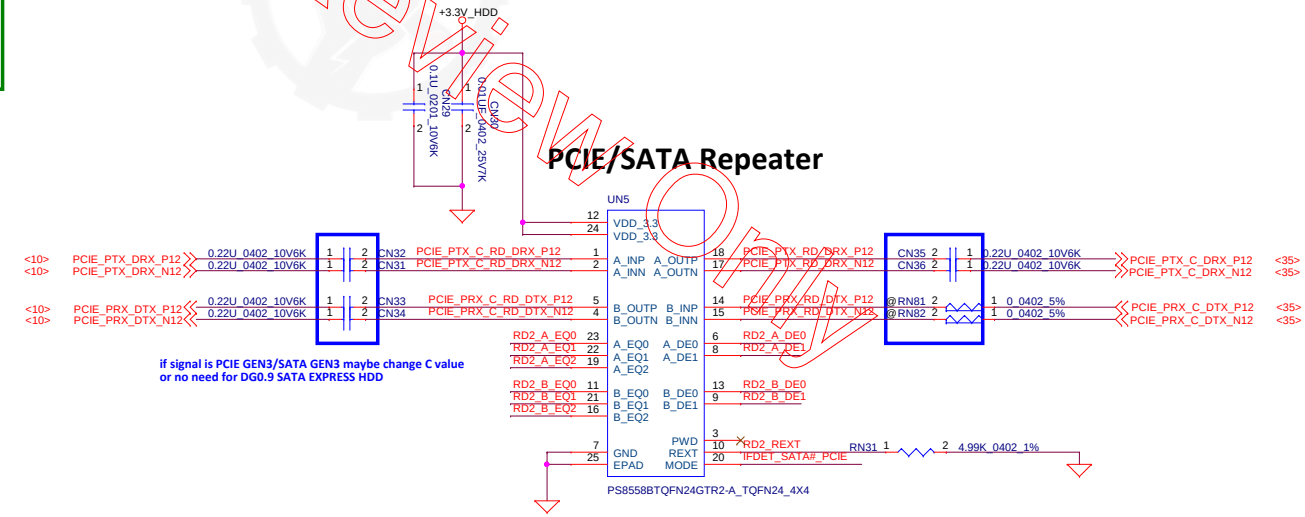
IFDET_SATA#_PCIE	DEVICE interface
0	SATA
1	PCIE

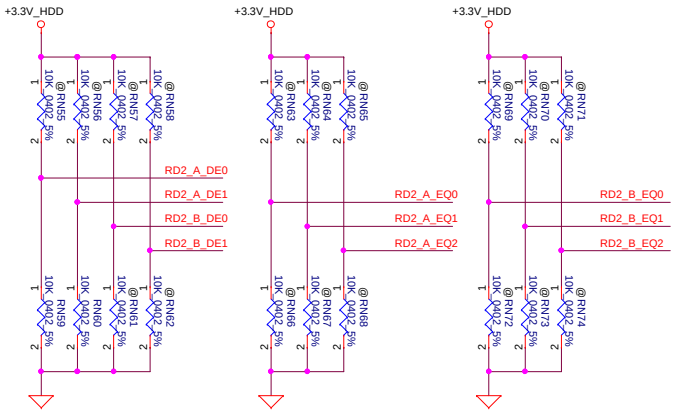
PCIE/SATA Repeater



PWD	Funtion
0	Normal mode(default)
1	power down mode

PCIE/SATA Repeater





SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Compal Electronics, Inc.

Title: Mini Card-2/2

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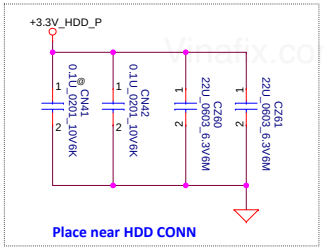
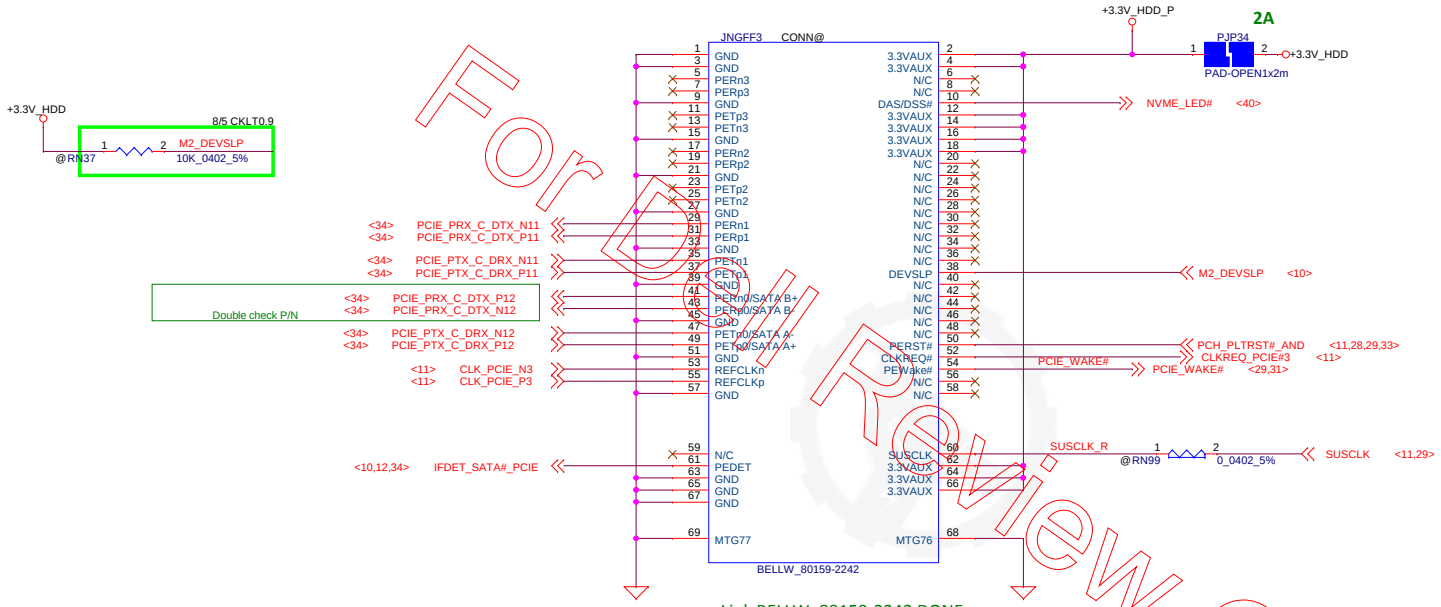


2280 SSD

NGFF slot C Key M



Link BELLW_80159-2242 DONE

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: HDD CONN

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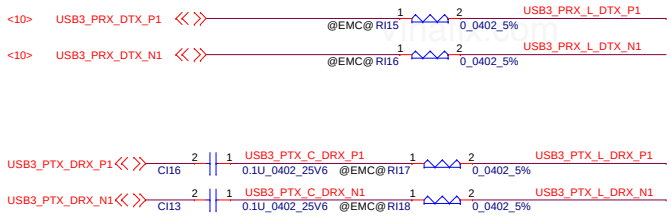
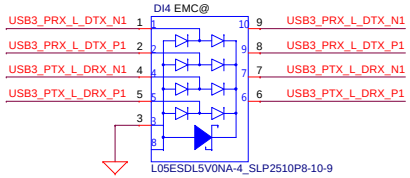
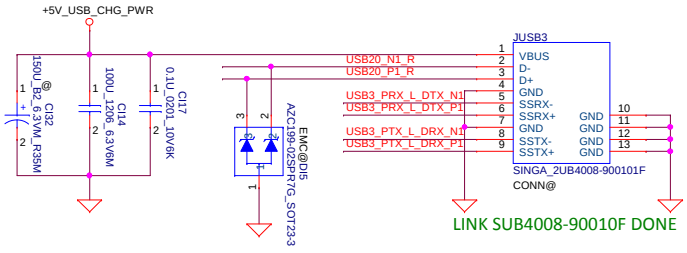
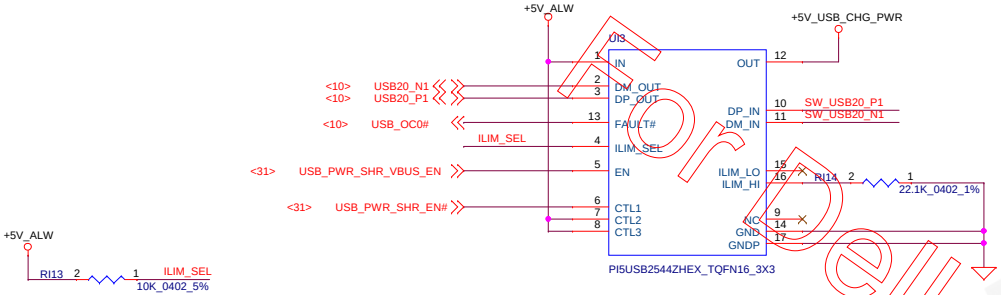
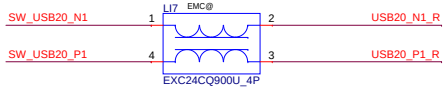
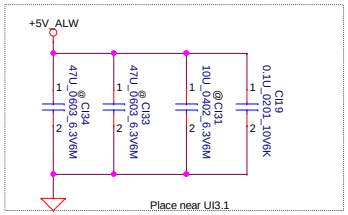










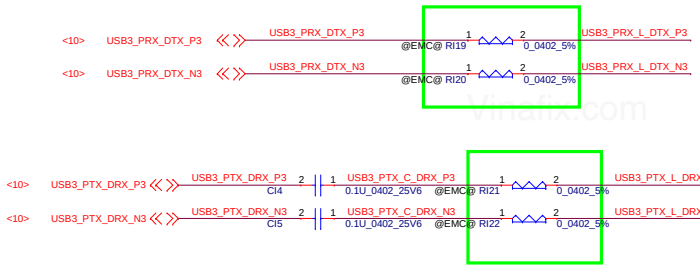


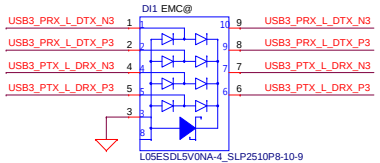
Compal Electronics, Inc.

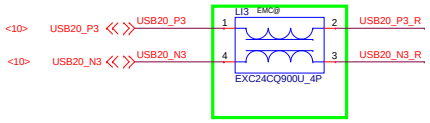
Title: USB SW

Size | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 36 of 60

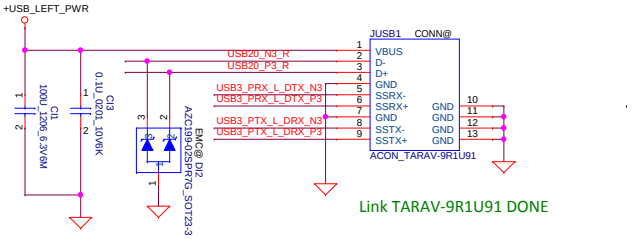




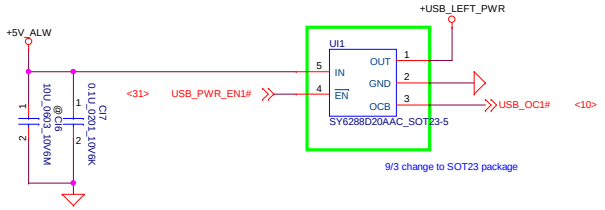


8/19 for layout routing change

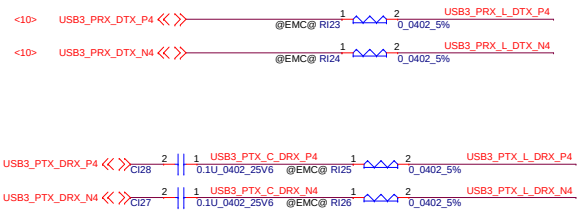
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

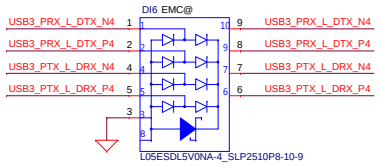


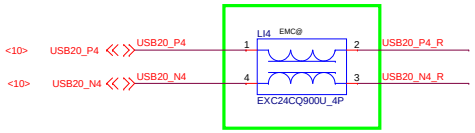
Link TARAV-9R1U91 DONE



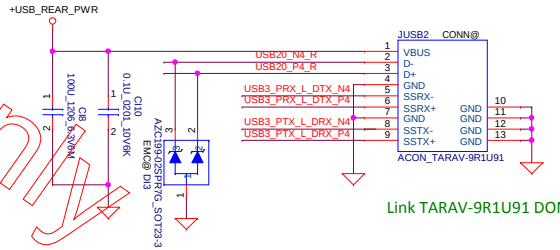
9/3 change to SOT23 package



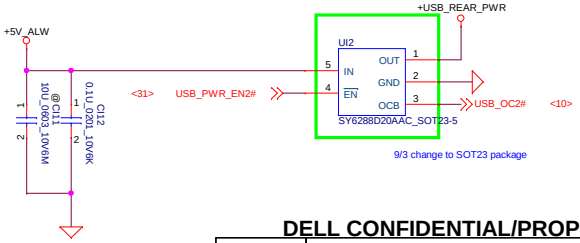




8/19 for layout routing change



Link TARAV-9R1U91 DONE



9/3 change to SOT23 package

Compal Electronics, Inc.

Title: USB3.0

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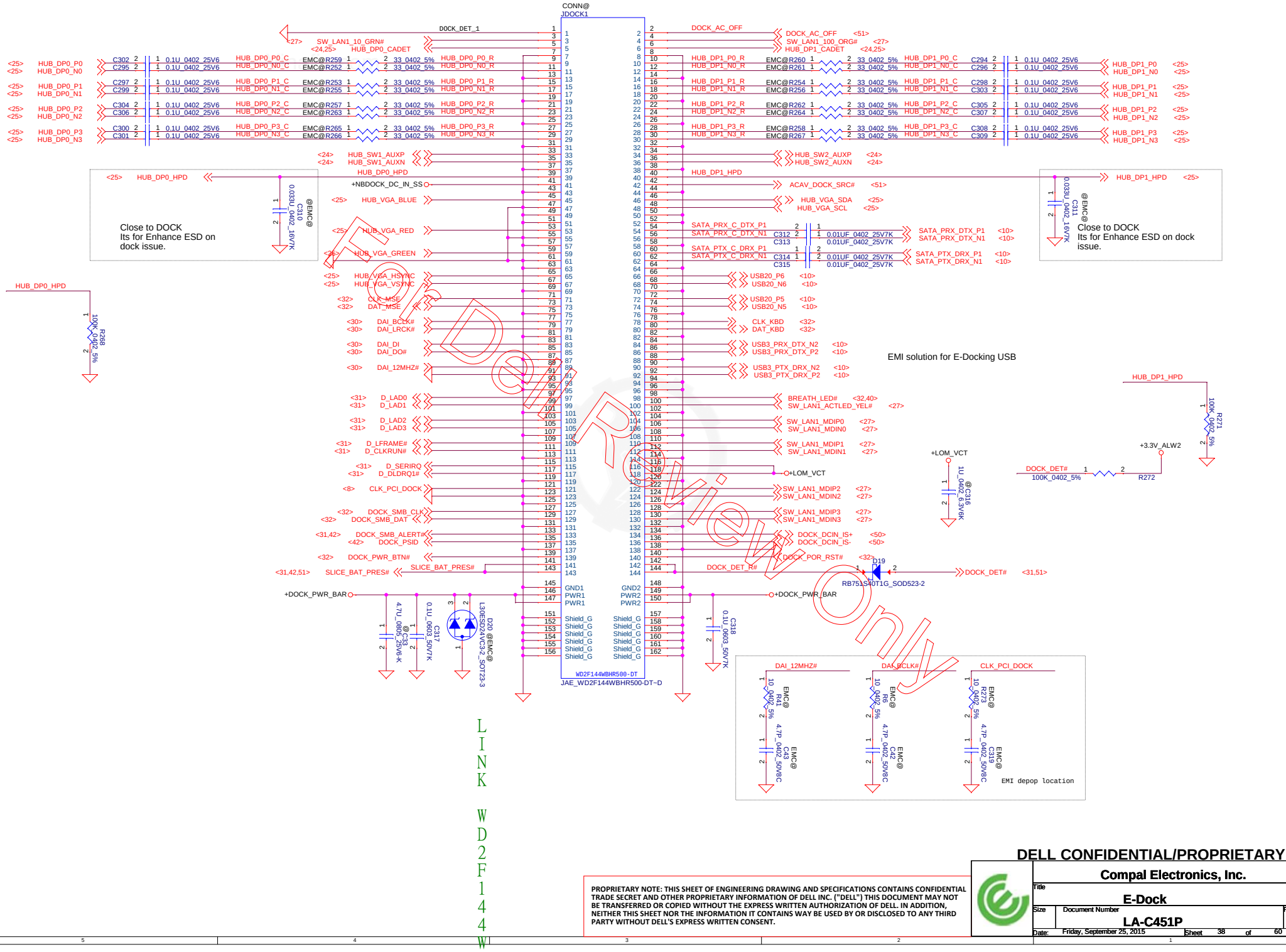

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Title	E-Dock
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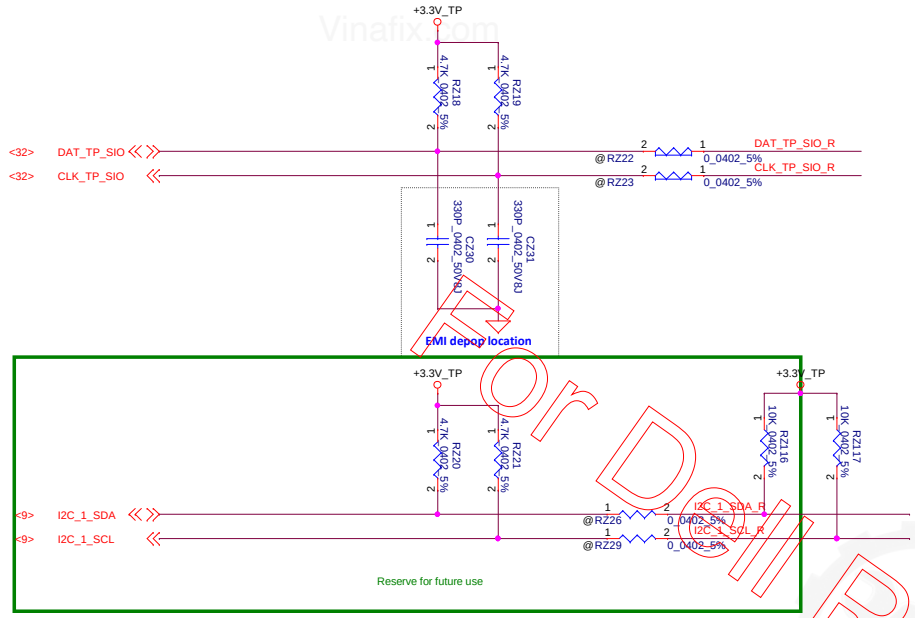
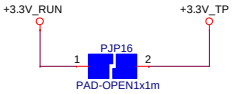
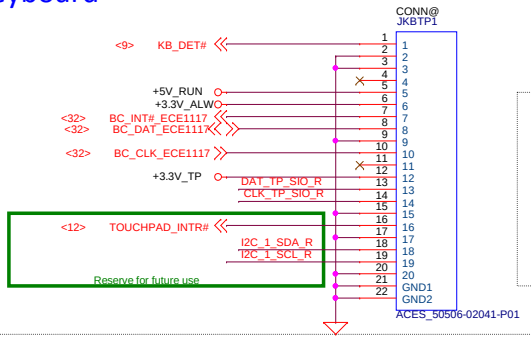
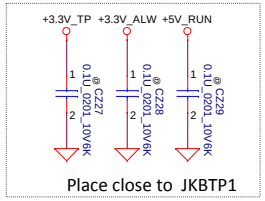
Touch Pad





Keyboard





Link 50506-02041-P0 DONE

@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-SATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

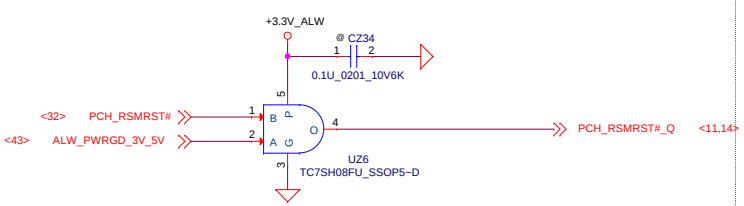
@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

RSMRST circuit



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Compal Electronics, Inc.

Title: Keyboard

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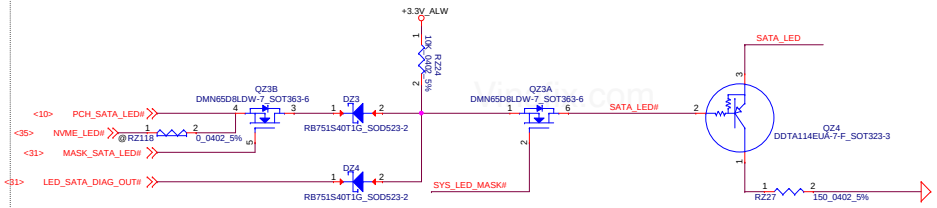
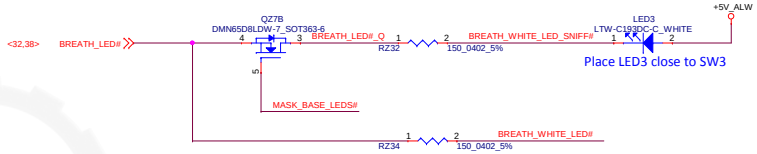
HDD LED solution for White LED

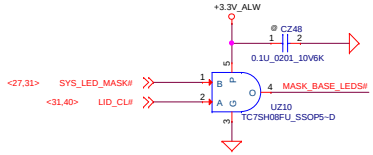


Battery LED

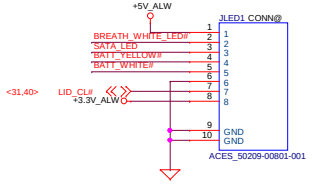
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

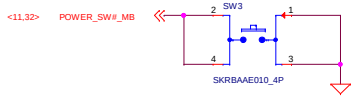




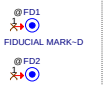
LED board CONN



POWER & INSTANT ON SWITCH

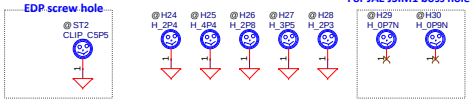


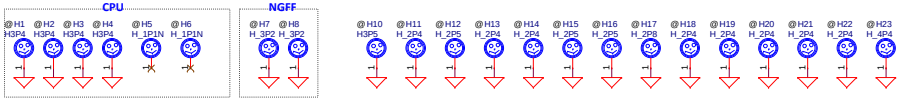
Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PAD, LED
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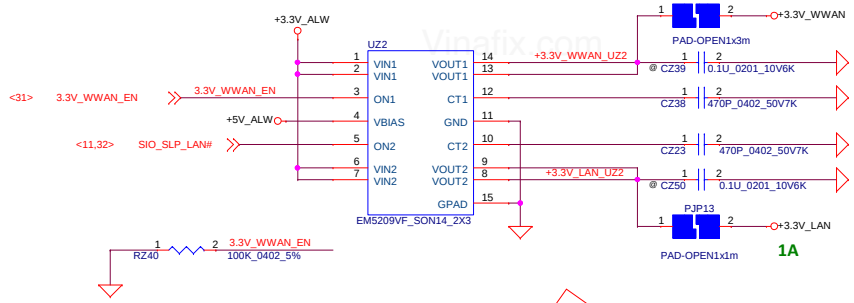
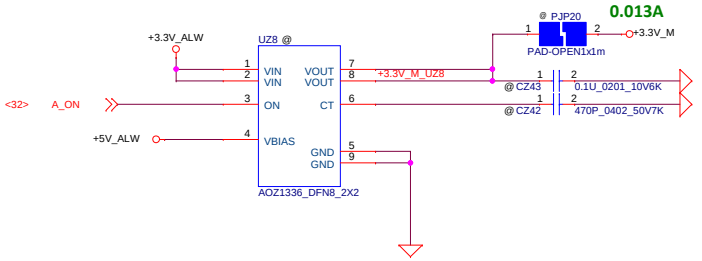
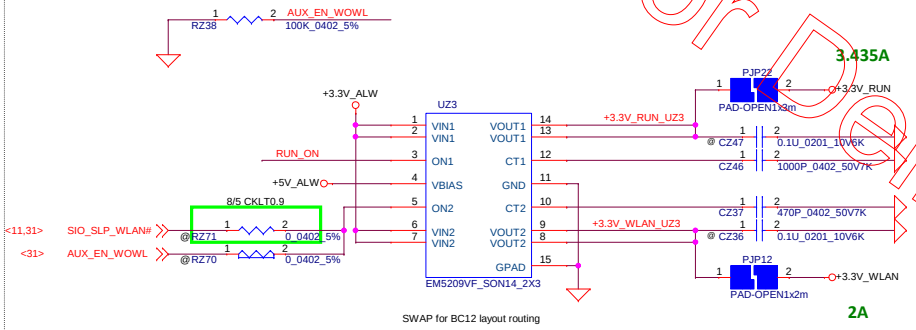
+3.3V_WWAN/+3.3V_LAN source



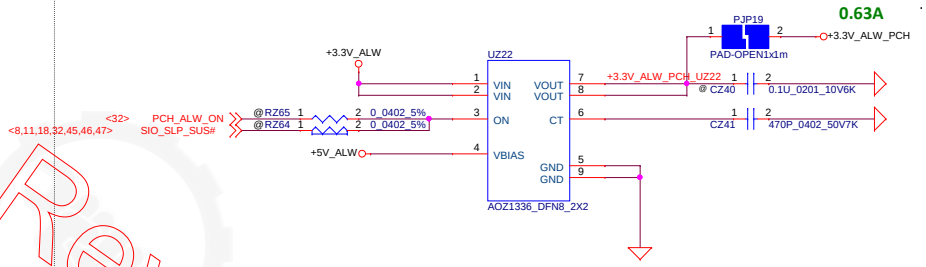
+3.3V_M source



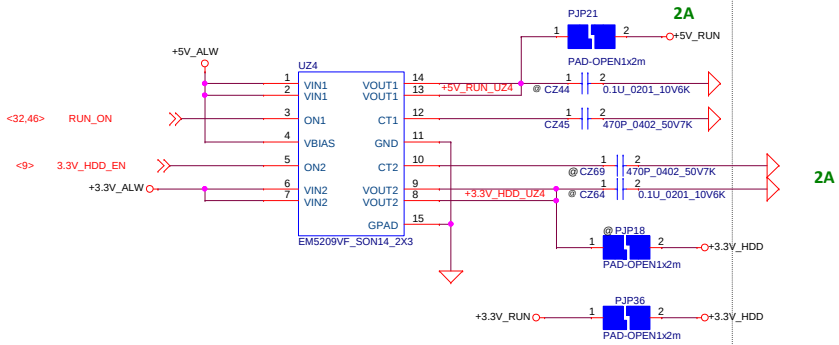
+3.3V_WLAN/+3.3V_RUN source



+3.3V_ALW_PCH source



+5V_RUN/+3.3V_HDD source



+3.3V_SUS source

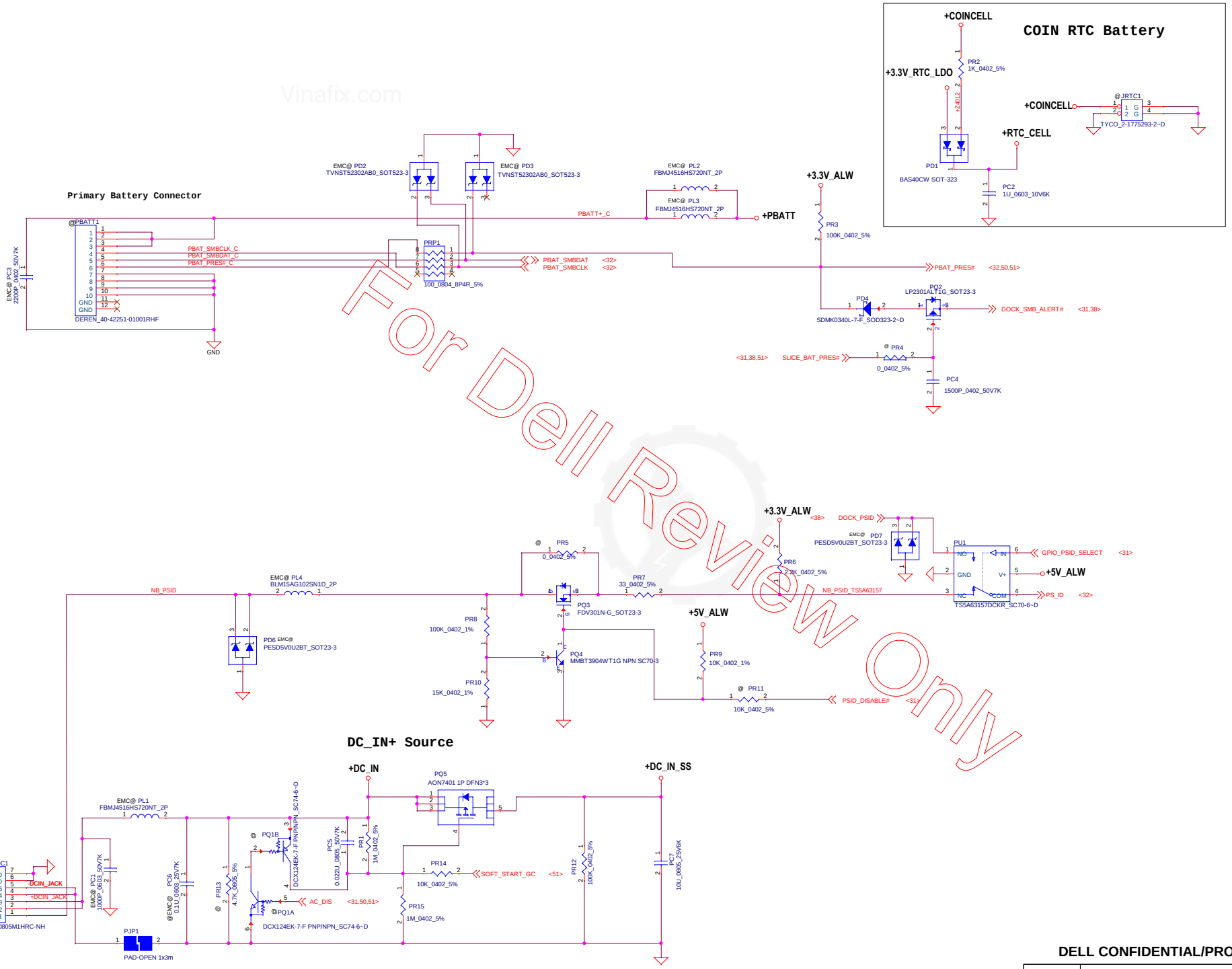
Move to USH/B

Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 41 of 60



Compal Electronics, Inc.	
Title	+DCIN
Size	Document Number: LA-C451P
Rev	1.0
Date:	Friday, September 25, 2015
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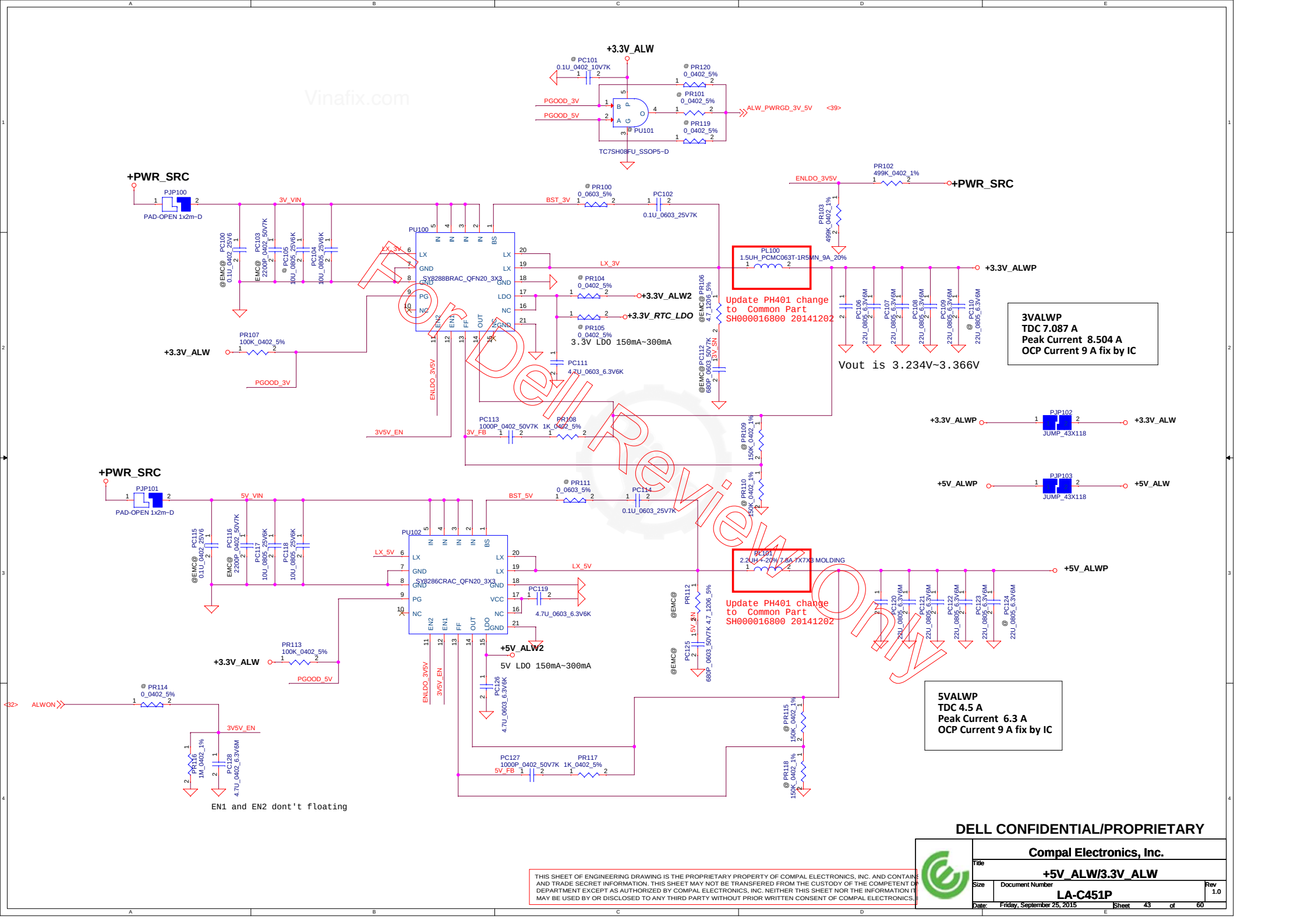

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-C451P
Rev	1.0
Date:	Friday, September 25, 2015
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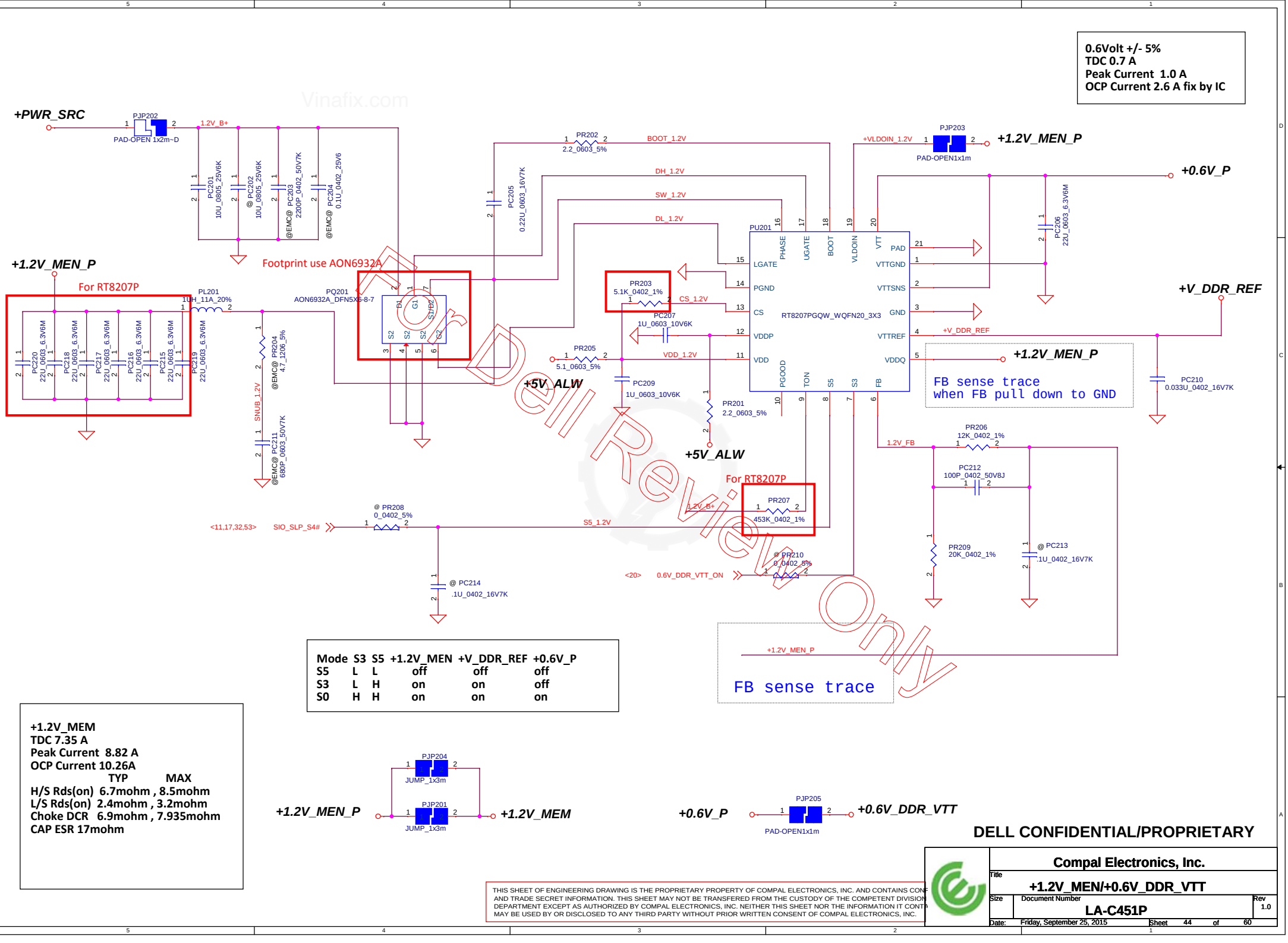

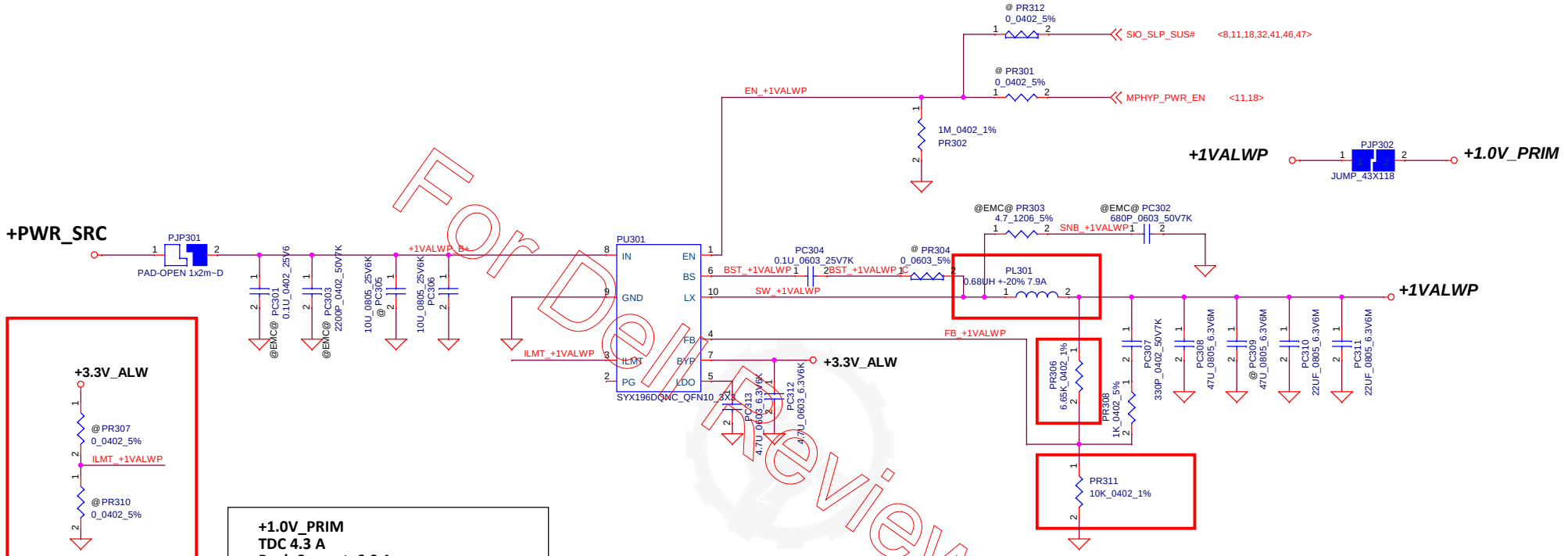

Compal Electronics, Inc.	
Title	+1VALWP
Size	Document Number: LA-C451P
Rev	1.0
Date:	Friday, September 25, 2015
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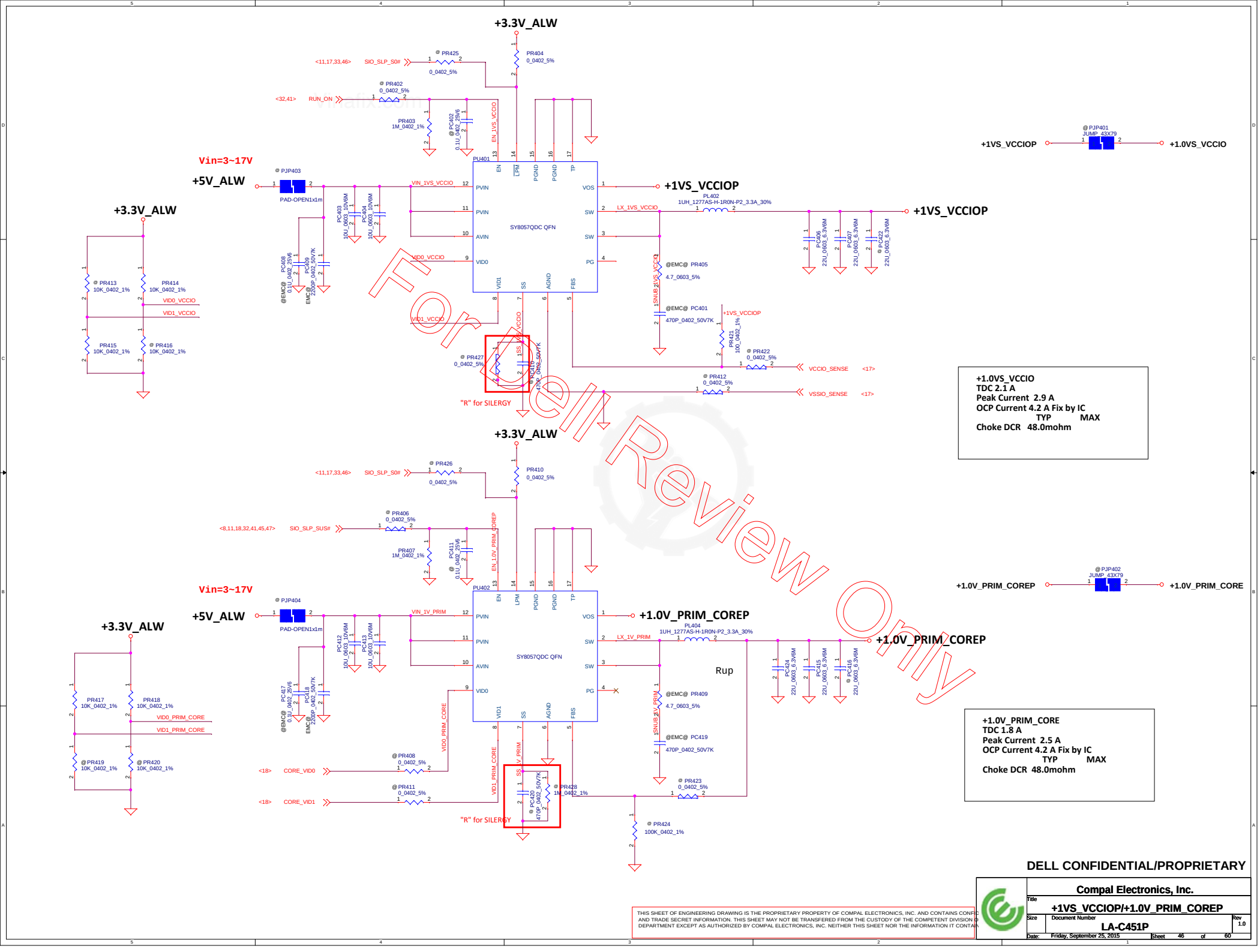

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Title	+1VS_VCCIOP/+1.0V_PRIM_COREP	
Size	Document Number LA-C451P	Rev 1.0
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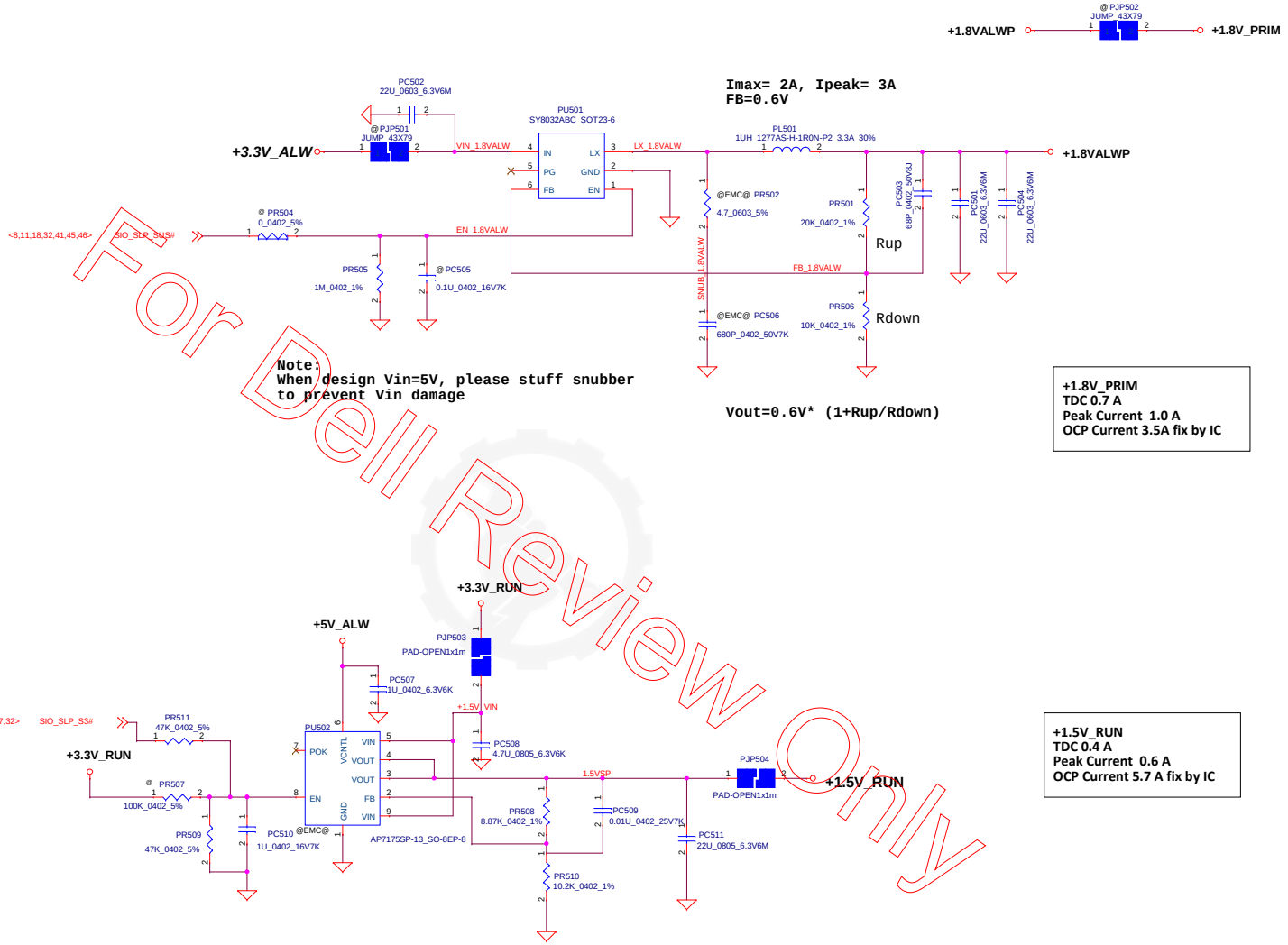

Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: *+1.8VALWP/+1.5V_RUN*

Size	Document Number	Rev
C		1.0

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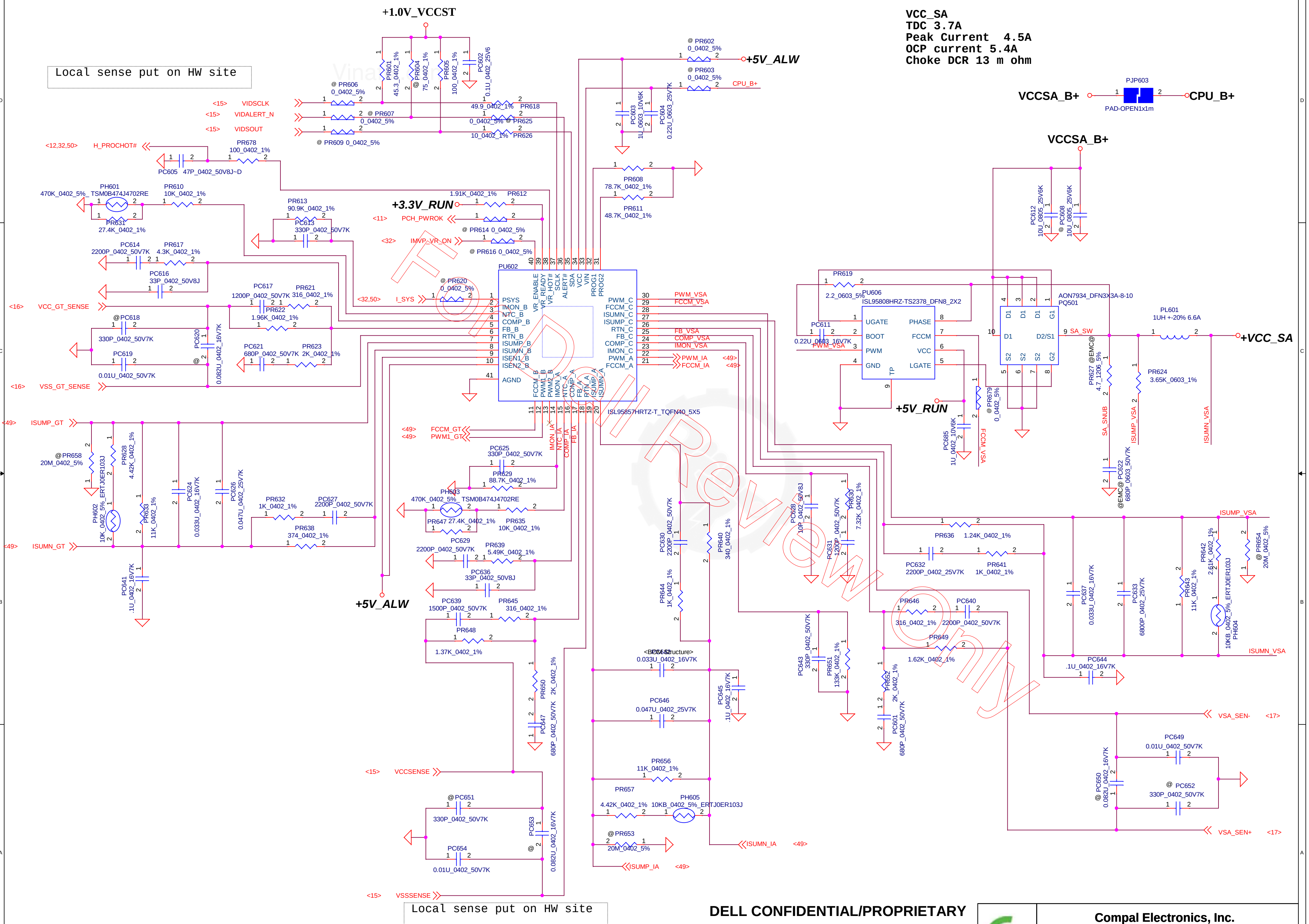

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Compal Electronics, Inc.	
Title	PWR_VCORE_ISL95812 for QC
Size / Document Number	LA-C451P
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Date:	Friday, September 25, 2015
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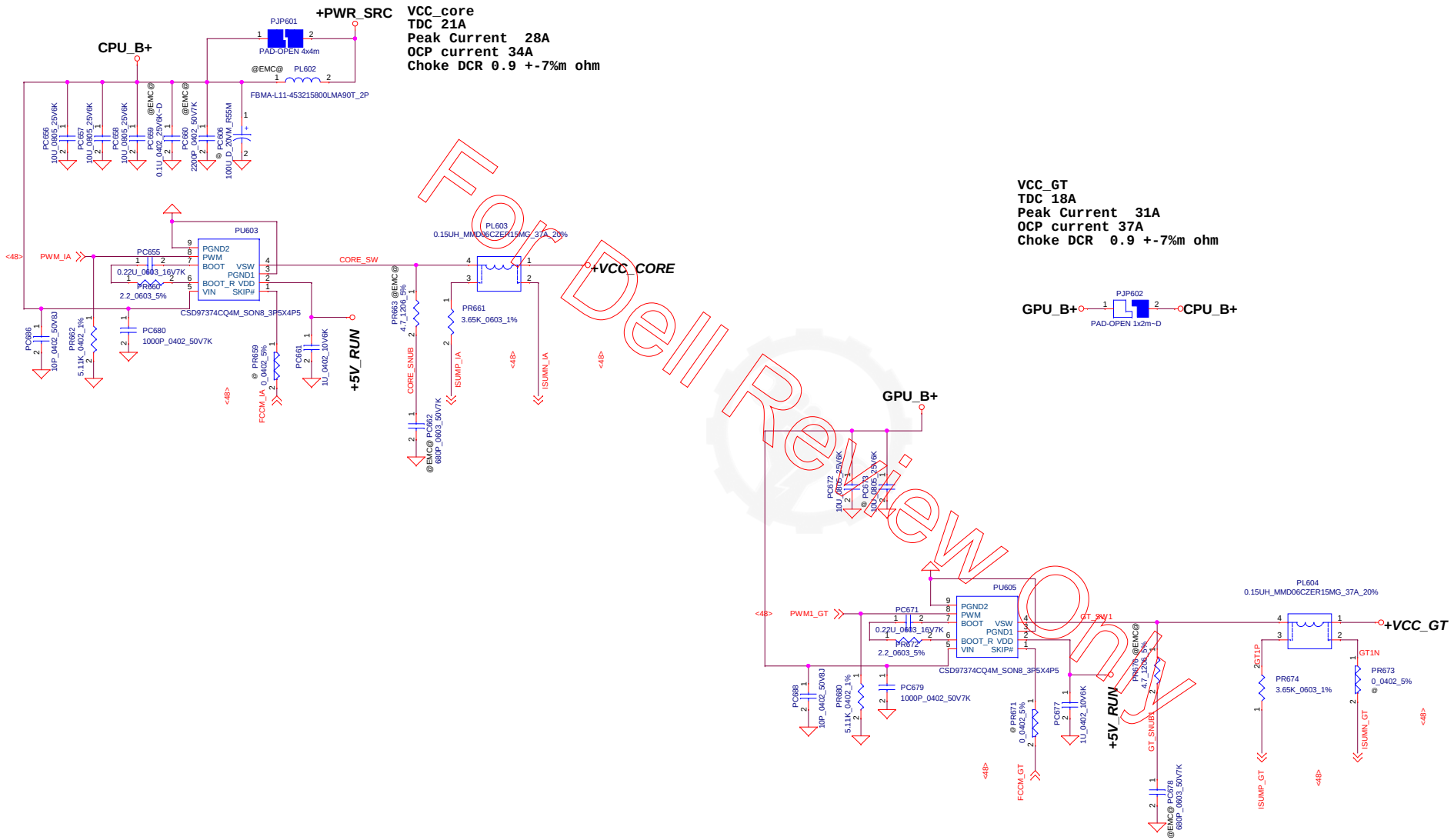

Compal Electronics, Inc.

Title: PWR_VCORE_ISL95812 for QC

Size | Document Number: LA-C451P | Rev: 1.0

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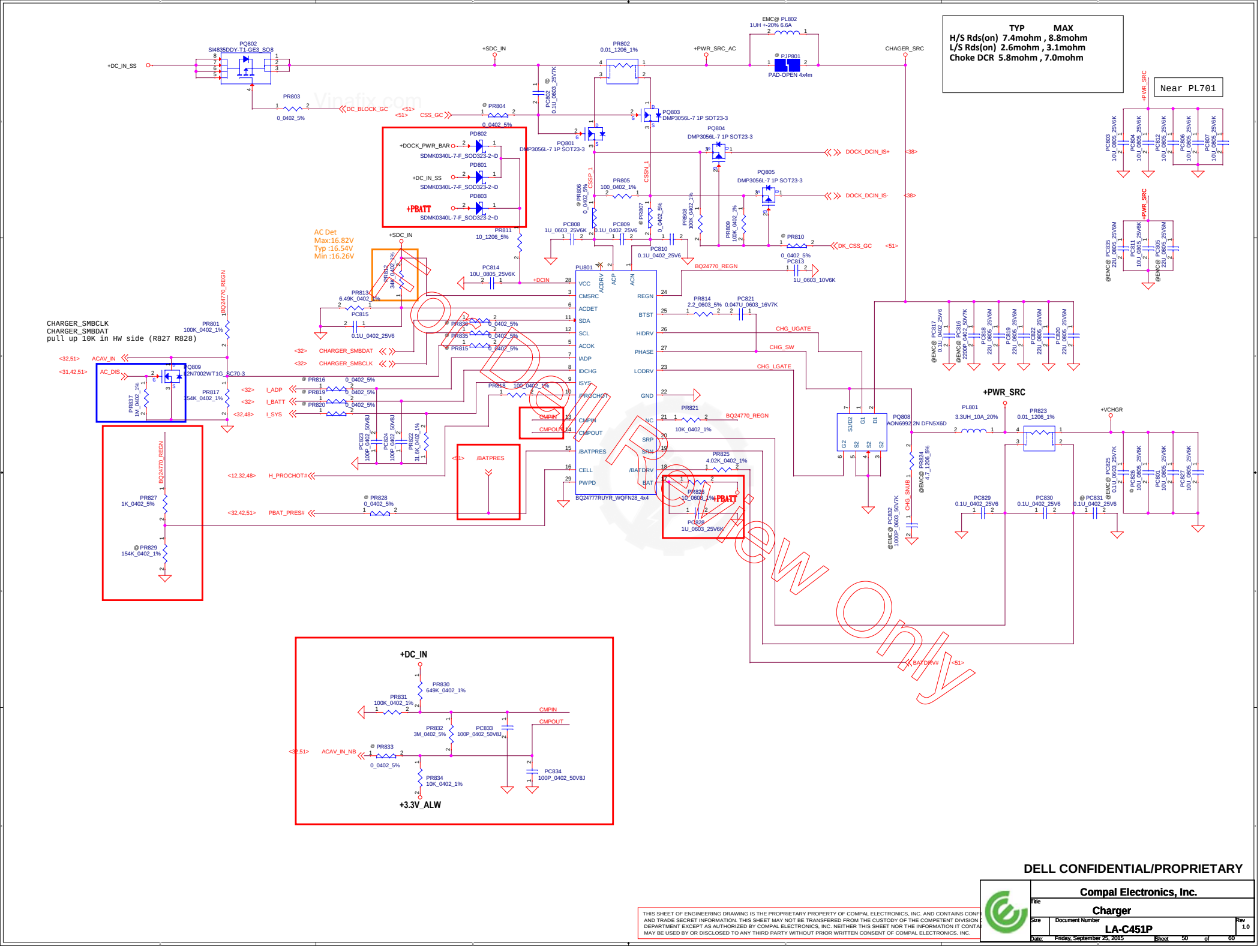

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Compal Electronics, Inc.	
Title: Charger	
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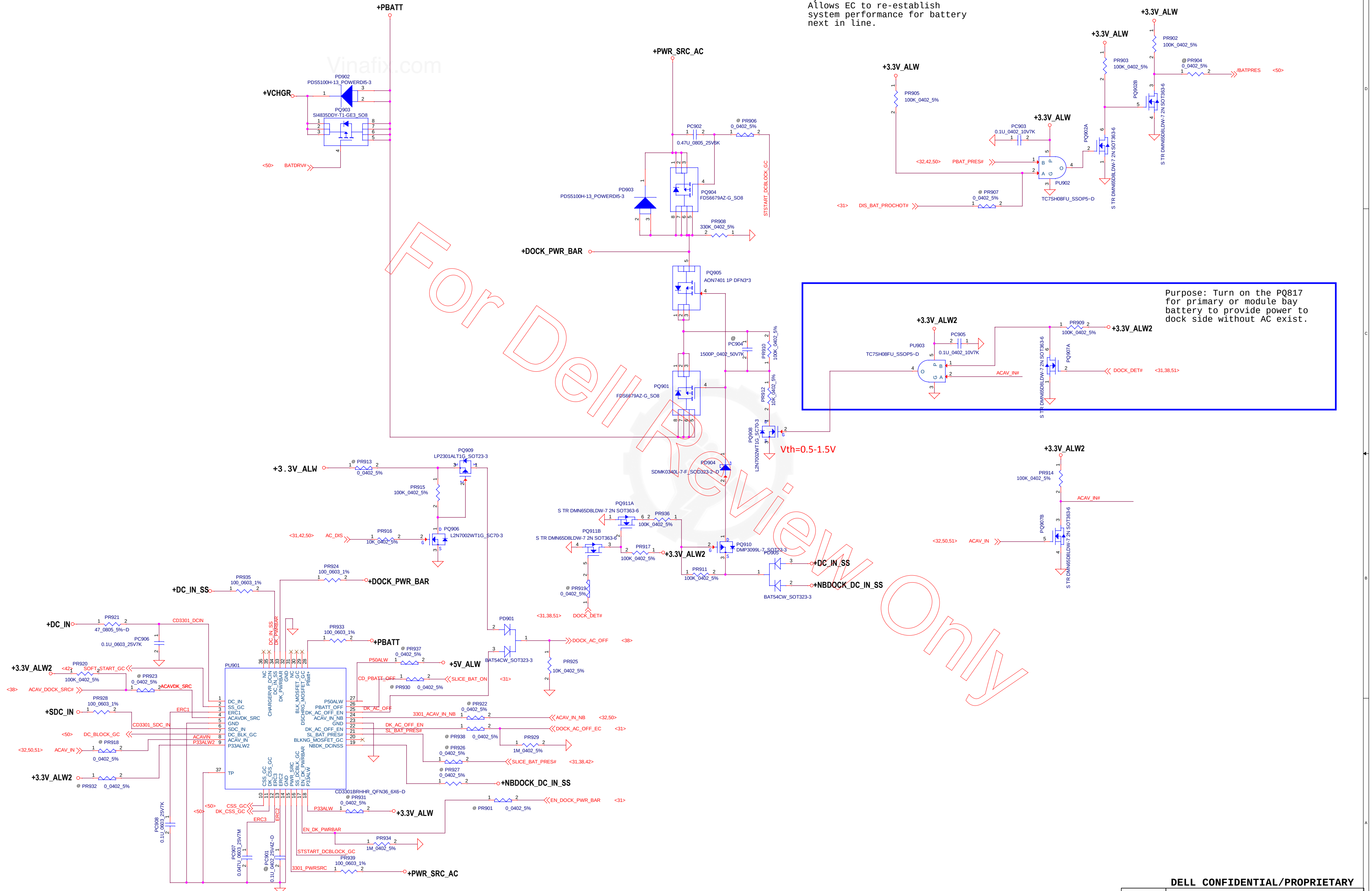
Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.



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VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+330u_D2*2 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +330u_D2*2 pcs

+VCC_CORE

+VCC_GT

+VCC_SA

VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs

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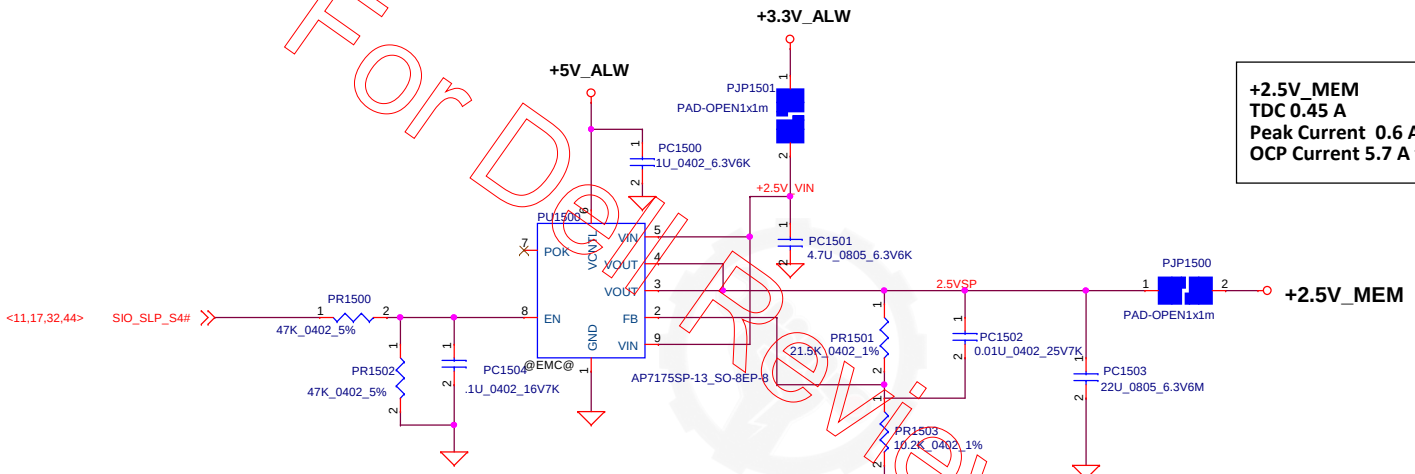
Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size: | Document Number: LA-C451P | Rev: 1.0

Date: Friday, September 25, 2015 | Sheet 52 of 60



+2.5V_MEM
TDC 0.45 A
Peak Current 0.6 A
OCP Current 5.7 A fix by IC

Compal Electronics, Inc.		
Title: +2.5V_MEM		
Size	Document Number: LA-C451P	Rev: 1.0
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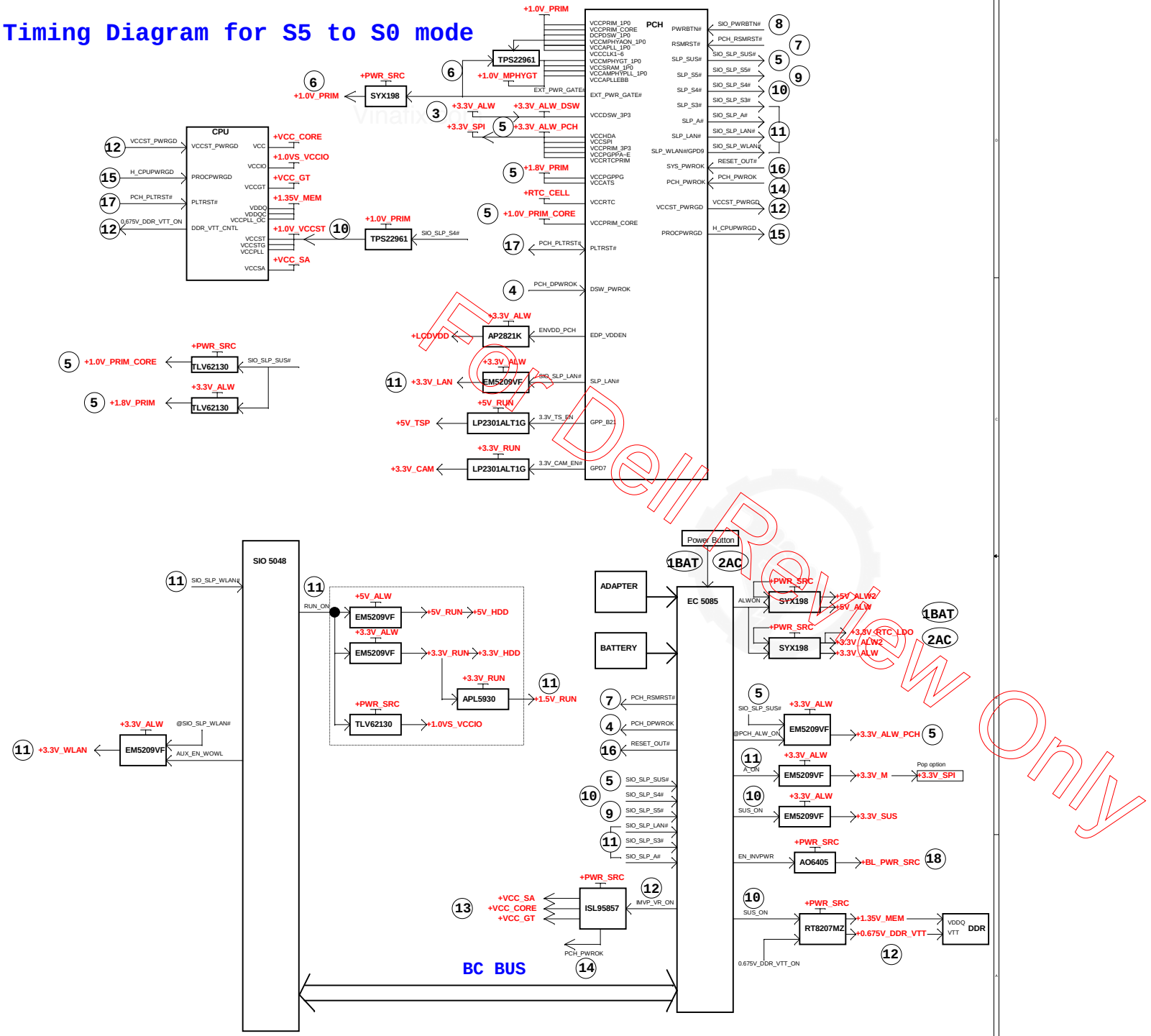
Timing Diagram for S5 to S0 mode



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Power Sequence

Document Number: LA-C451P

Rev: 1.0

Date: Friday, September 25, 2015

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev. 0.1
1	43	+5V/+3.3V	12/29	Compal	change PWR IC for 3V and 5v power rail 5V and 3V change form TPS51285B to SY8286CRAC and SY8286BRAC.	Remove PQ100, PQ101, PQ102, PQ103 (H-L side Mosfet) PC113, PC115 (Polymar) Change PL100 to 1.5UH_PCMC063T-1R5MN_9A_20% PL101 to 2.2UH +-20% 7.8A 7X7X3 MOLDING Add PU100 SY8286BRAC_QFN20_3X3 PU102 SY8286CRAC_QFN20_3X3	X01
2	48	+VCCSA	12/29	Compal	change VCC_GT to one phase.	Remove PC635 PC638 PU602 Pin9 and Pin10 contect to +5V_ALW	X01
3	49	+VCC_CORE/GT	12/29	Compal	change VCC_GT to one phase.	Remove PC663, PC664, PC665, PC669, PC670, PC681, PC687 PL605, PR664, PR665, PR666, PR667, PR668, PR669, PR670, PR681, PU604 Change PL604 to 0.15UH_MMD06CZER15MG_37A_20%	X01
4	47	+1.5V_RUN	05/25	Compal	+1.5V_RUN enable chnage to SIO_SLP_S3#	Turn PR507 to de-pop Add PR511 47k_0402 to contact SIO_SLP_S3#	
5	46	VCCIO	09/07	Compal	VCCIO change to 0.95V	remove PR413 PR416 add PR414 PR415	X06
6							
7							
8							
9							
10							

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7,17,20,21	HW	2014/11/17	COMPAL	Change DDR3L to DDR4 schematic	1. JDIMM1&JDIMM2 change from DDR3L to DDR4 connector 2. change +1.35V_MEM to +1.2V_MEM 3. change +0.675V_DDR_VTT to +0.6V_DDR_VTT 4. add +2.5V_MEM	0.2(X01)
~~2~~	~~10,32,34~~	~~HW~~	~~2014/11/17~~	~~COMPAL~~	~~EC MCARD_PCIE#_SATA pin is for WWAN slot, not KEY M SSD slot~~	~~1. QN2.1&UC1.H2&RC174.1 change from MCARD_PCIE#_SATA to IFDET_SATA_PCIE#~~	~~0.2(X01)~~
3	9	HW	2014/11/17	COMPAL	For reduce power comsupition	RC287 change from 10k to 100k ohm	0.2(X01)
4	34	HW	2014/11/19	COMPAL	For key M slot PCIE/SATA Detect	Delete QN2/RN48/RN24, IFDET_SATA#_PCIE connect to PCH directly (BIOS need setup SATA=0;PCIE=1 by PSCPSP_Px_STRP bit=1)	0.2(X01)
5	8,11,27	HW	2014/11/20	COMPAL	Follow Intel LAN Review result	1.RC19&RC20 PH change from +3.3V_ALW_PCH to +3.3V_LAN 2.CL7 change from 1uF to 0.1uF 3.CL4 add @ 4.CL16&CL17&CL20&CL21 change from 0.47uF to 0.1uF 5.RC70 PH change from +3.3V_ALW_DSW to +3.3V_LAN	0.2(X01)
6	36	HW	2014/11/20	COMPAL	Follow Pericom Review result	Reserve CI31	0.2(X01)
7	31,32	HW	2014/11/21	COMPAL	Follow Gen7 GPIO Master_1122	1.AC_DIS change from UE2.A10 to UE1.A50 2.Add PANEL_ID at UE2.A10 and RE300&CE47 3.Delete RE291 & RE281,and change SUS_ON to CV2_ON	0.2(X01)
8	27	HW	2014/11/25	COMPAL	Follow Intel LAN Review result	1.CL22 change from 150P to 1500P 2KV(SE00000WQ00)	0.2(X01)
9	30	HW	2014/11/25	COMPAL	Follow Intel WOV(Wake on Voice) suggest	1.Delete RA15/RA41/RA42	0.2(X01)
10	34	HW	2014/11/25	COMPAL	Remove co-lay schematic with PS8558B	1.Delete CN43~CN46,RN85,RN86,UN89~RN98	0.2(X01)
11	32	HW	2014/11/25	COMPAL	For separate +1.2V_MEM&+3.3V_CV2 enable pin	1.Delete RE291&RE281	0.2(X01)
12	11,12,14	HW	2014/11/25	COMPAL	For ESD request	1.Add CC300 100P at H_VCCST_PWRGD 2.Add CC301 100P at H_CPUPWRGD 3.Reserve CC302 0.1u at SYS_RESET# 4.Reserve CC303 0.1u at PCH_JTAG_TDO 5.Reserve CC304 0.1u at PCH_JTAG_TDI 6.Reserve CC305 0.1u at XDP_JTAGX 7.Reserve CC306 0.1u at TDO_XDP 8.Reserve CC307 0.1u at H_VCCST_PWRGD_XDP 9.Reserve CC308 0.1u at CPU_XDP_TRST#	0.2(X01)
13	20,21	HW	2014/11/25	COMPAL	Follow Intel DDR4 Review result	1.CD24~CD27,CD57~CD60 change from 0.1uF to 1uF 2.CD29,CD62 add @ 3.+2.5V_MEM add CD70,CD71,CD74,CD75(1UF) & CD72,CD73,CD76,CD77(10UF) 3.+1.2V_MEM add CD78~CD85,CD102~CD109(1UF)&CD86~CD101(10UF)	0.2(X01)
14	38	HW	2014/12/01	COMPAL	For sync up with PARK CITY DSC port mapping	Swap USB2.0 port5 & port6 at JDOCK1	0.2(X01)
15	32	HW	2014/12/01	COMPAL	Board ID for X01	RE79 change from 240k ohm to 130k ohm	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	31,32	HW	2014/12/01	COMPAL	Follow Gen7 GPIO Master_1127	1.Delete RE294/RE295/RE296/RE297 2.5085 GPIO116 change from PCH_PCIE_WAKE# to MSDATA 3.5085 GPIO124 change from ME_FWP_EC to PCH_PCIE_WAKE# 4.5048 GPIOJ1 add ME_FWP_EC 5.5085 GPIO117 change from USB_PWR_SHR_EN# to MSCLK 6.5048 GPIOK0 add USB_PWR_SHR_EN#	0.2(X01)
17	32	HW	2014/12/02	COMPAL	Follow INTEL PDG 1.0	Charger SMBUS PU resistor change from 10k to 2.2k	0.2(X01)
18	32	HW	2014/12/02	COMPAL	Follow INTEL PDG 1.0	RE88 change from 47k to 10k	0.2(X01)
19	39	HW	2014/12/05	COMPAL	Follow Dell ARD Rev1.3	1.Reserve RZ26/RZ29 for I2C_1_SDA/I2C_1_SCL 2.Add RZ22/RZ23 for DAT_TP_SIO/CLK_TP_SIO	0.2(X01)
20	13	HW	2014/12/05	COMPAL	Follow 546765_546765_2014WW48_Skylake_MOW_Rev_1_0	RC120 add @	0.2(X01)
21	32	HW	2014/12/09	COMPAL	For Port Mapping update	1.For USB2, Camera change from port 10 to port 2 WWAN change form port 2 to port 10 2.For USB3, EDOCK change from port 5 to port 2 WWAN change from port 2 to port 5 3.For SATA, EDOCK change from SATA1B to SATA1A 4.For PCIE/SATA, M2 SSD PCIE lane 0 change from port 7 to port 12, M2 SSD PCIE lane 1 change from port 8 to port 11	0.2(X01)
22	11	HW	2014/12/27	COMPAL	For PLTRST glitch issue	1.UC7.5 change from +3.3V_RUN to +3.3V_ALW_PCH 2.Pop RC325,depop RC60	0.3(X02)
23	11	HW	2014/12/29	COMPAL	For DIMM Select Issue	Pop RD63 ;Depop RD67	0.3(X02)
24	22	HW	2014/12/29	COMPAL	For HDMI EMI solution	1.add RV647~RV658	0.3(X02)
25	32	HW	2014/12/30	COMPAL	For Layou routing	1.Swap LV3,LV6,LV9,LV12	0.3(X02)
26	32	HW	2014/12/29	COMPAL	For Power down sequence	1.add QE8,UE4,RE304,RE305	0.3(X02)
27	8	HW	2014/12/31	COMPAL	For Support DCI	1.Reserve RC326,QC3, Add RC327	0.3(X02)
28	13	HW	2014/12/31	COMPAL	Follow 546765_546765_2014WW52_Skylake_MOW_Rev_1_0	1.Reserve CC222 and RC313	0.3(X02)
29	33	HW	2015/02/06	COMPAL	For TPM issue	1.UZ12.29 reserve RZ90(10K) PU to +3.3V_RUN 2.UZ12.3 add TPM_LPM# signal & QZ9,RZ111 3.UZ12.13 add TPM_GPIO4 signal &Reserve RZ110 4.Add RZ88(+3.3V_M_TPM), Reserve RZ89(+3.3V_RUN)	0.4(X03)
30	12	HW	2015/02/06	COMPAL	For support DCI	1.add RC328 between CPU_XDP_TCLK & XDP_JTAG 2.add RC329,Reserve RC340 3.Pop QC3,depop RC327	0.4(X03)
31	10	HW	2015/02/06	COMPAL	For fix DCI warmboot hang up issue	1.USB2_ID add RC337(10K) to GND 2.USB2_VBUSSENSE add RC338(10K) to GND	0.4(X03)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
32	32	HW	2015/02/06	COMPAL	For Power down sequence	Depop RE304,RE305,pop UE3	0.4(X03)
33	11	HW	2015/02/06	COMPAL	For auto power on issue	Depop RC70, depop RC323	0.4(X03)
34	26	HW	2015/02/06	COMPAL	BOM changed,follow PC	UV24 from SA00006EE00(AP2821KTR-G1) to SA00006Y800(G524B1T114)	0.4(X03)
35	8	HW	2015/03/02	COMPAL	Intel MOW_2015WW06:Intel recommendation for DCI tool consulting,	RC317 change from 4.7k to 150k ohm	0.4(X03)
36	32	HW	2015/03/02	COMPAL	For X03 Board ID	RE79 change from 130k to 4.3k	0.4(X03)
37	8	HW	2015/03/02	COMPAL	Intel MOW_2015WW06:Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update	de-pop RC30, RC316	0.4(X03)
38	33	HW	2015/03/02	COMPAL	for allow further reducing power in TPM 2.0 F/W,when system is in S3/4/5 and main power is off.	Pop RZ90	0.4(X03)
39	34	HW	2015/03/02	COMPAL	Follow SATA EA result	pop RN59 &RN60	0.4(X03)
40	20,21	HW	2015/03/02	COMPAL	Intel MOW_2015WW02	Depop CD6,CD35	0.4(X03)
41	35,12	HW	2015/03/02	COMPAL	For ESD request	1.H_THERMTRIP# reserve CC309 0.1uF to GND 2.H_PROCHOT# reserve CC310 0.1uF to GND	0.4(X03)
42	12	HW	2015/03/02	COMPAL	For RF request	1.CC3~CC6 change from 12pF to 27pF & pop 2.HDA_SDOUT add CC311 15pF to GND	0.4(X03)
43	26	HW	2015/03/02	COMPAL	Reserve for IR camera	Reserve JIR1	0.4(X03)
44	33	HW	2015/03/04	COMPAL	For TPM vender review result	UZ12.29 reserve RZ112 to SIO_SLP_S0#	0.4(X03)
45	9	HW	2015/03/04	COMPAL	For support DDR3L & DDR4	UC1.P2 add DIMM_TYPE signal,Low(RC342)=DDR4,High(RC341)=DDR3L	0.4(X03)
~~46~~	~~36~~	~~HW~~	~~2015/03/04~~	~~COMPAL~~	~~For USB charger issue~~	~~UI3 change from SA00007TJ00(Pericom) to SA00008DH00(Selegro)~~	~~0.4(X03)~~
47	11,32	HW	2015/03/06	COMPAL	For Crystal EA	CC21/CC22 change to 15pF CE28/CE29 change to 33pF	0.4(X03)
48	8	HW	2015/03/06	COMPAL	Follow INTEL CRB	RC23 change from 8.2k to 2.2k	0.4(X03)
49	33	HW	2015/04/17	NUVOTON	For support modern standby	1. Pop RZ112(0 ohm) & Depop RZ90(10k ohm)	0.5(X04)
50	33	HW	2015/04/17	NUVOTON	For TPM schematic review	1. Pop RZ89(0 ohm) & Depop RZ88(0 ohm) 2. Add RZ113(100 ohm)	0.5(X04)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
51	9,11	HW	2015/04/17	COMPAL	For backdrive issue	1. DIMM_TYPE PU change from +3.3V_ALW to +3.3V_ALW_PCH 2. VRALERT# PU change from +3.3V_ALW to +3.3V_ALW_PCH	0.5(X04)
52	9,26	HW	2015/04/17	COMPAL	For IR camera design	1. add IR_CAM_DET# connect between GPP_A23(UC1.AW7) & JIR1.6 2. JIR1.3 change from +PWR_SRC to NC	0.5(X04)
53	31,33	HW	2015/04/17	Broadcom	Reserve for USH RESET	UE1.A62 add USH_RST#, and reserve RZ114&RZ115 on JUSH1.21	0.5(X04)
54	12	HW	2015/04/17	COMPAL	For wake up system when non-deep S3	SIO_EXT_SMI# PU change from +3.3V_RUN to +3.3V_ALW_PCH	0.5(X04)
55	10	HW	2015/04/17	INTEL	For DCI function	RC337 change from 1k to 0 ohm	0.5(X04)
56	29	HW	2015/04/17	COMPAL	SIM detect	Add RI31 connecting with JSIM1.9 and NGFF2.58	0.5(X04)
57	29	HW	2015/04/17	COMPAL	ME request	JSIM1 change from JAE_SF51S006V4B to T-SOL_5-991503004000-6	0.5(X04)
58	41	HW	2015/04/17	COMPAL	For +3.3V_HDD power solution	Depop PJP18,CZ69; Pop PJP36	0.5(X04)
59	39	HW	2015/04/17	COMPAL	For new U1 TP module	Add RZ116 and RZ117 PU on I2C._1_SDA_R/I2C_1_SCL_R	0.5(X04)
60	8	HW	2015/04/21	COMPAL	For LAN backdrive	1. Add RC347 and RC348 PU to +3.3V_ALW_PCH 2. Depop RC19,RC20	0.5(X04)
61	32	HW	2015/04/21	COMPAL	For Board ID	RE79 change from 4.3k to 2k	0.5(X04)
62	14	HW	2015/04/23	COMPAL	For DCI function	UC8 & CC30 remove CXDP@	0.5(X04)
63	22	HW	2015/04/24	COMPAL	Base on HDMI EE/EMI measure result	Pop LV3/LV6/LV9/LV12 Depop RV647~RV658	0.5(X04)
64	40	HW	2015/04/29	COMPAL	ME request	Add H28 H_2P3	0.5(X04)
65	40	HW	2015/04/29	COMPAL	For JAE JSIM1 boss hole	Add H29 H_0P7N & H30 H_0P9N	0.5(X04)
66	36	HW	2015/05/04	COMPAL	For 儲存巴士 shut down issue	Add CZ32 (150U_B2_6.3VM_R35M)	0.5(X04)
67	39	HW	2015/05/06	COMPAL	For TP sometimes can't work in BIOS or OS	Pop CZ30/CZ31 330pF	0.5(X04)
68	29,40	HW	2015/05/12	COMPAL	For NVME SSD LED issue	JNGFF3.10 add NVME_LED#, thought RZ118(0 ohm) connect to PCH_SATA_LED#	0.5(X04)
69	36	HW	2015/05/12	COMPAL	For USB charger issue	UI3 main source change from SA00008DH00(Selegro) to SA00007TJ00(Pericom)	0.5(X04)
70	40	HW	2015/05/12	COMPAL	Base on LED EA result	RZ25/RZ27/RZ34 change from 220 to 150 ohm	0.5(X04)
71	18	HW	2015/05/28	INTEL	For RF 5.76GHz noise issue	1. add RC349,CC313,CC314 2. change 0603 to 0402	0.5(X04)
72	27	HW	2015/06/02	COMPAL	For LAN EA result	Change LL2~LL9(12nH) to RL71~RL78(2.2ohm)	0.5(X04)
73	22	HW	2015/06/02	COMPAL	For HDMI EA result	1.RV647/RV649/RV650/RV652/RV653/RV655/RV656/RV658 change from 8.2ohm to 5.6 ohm 2.RV648/RV651/RV653/RV657 change from 150 ohm to 200 ohm 3.Depop LV3/LV6/LV9/LV12;Pop RV647~RV658	0.5(X04)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
74	25	HW	2015/06/03	COMPAL	For DP hub display flicker issue	1.Add UV29,CV617,CV618,CV619,PJP37,RV659,RV650,RV661 2.Depop UV28,PJP33	0.5(X04)
75	9	HW	2015/06/04	COMPAL	Sink up with Park City	Reserve RC330,RC331	0.5(X04)
76	33	HW	2015/07/13	DELL	IC change from TPM2.0 to TPM1.2	UZ12 change from SA000082D00(TPM2.0) to SA000082D20(TPM1.2)	0.6(X05)
77	33	HW	2015/07/13	NUVOTON	For TPM Deep S3 issue	UZ12.1 change from +3.3V_ALW_PCH to +3.3V_ALW	0.6(X05)
78	32	HW	2015/07/13	COMPAL	For Global Reset issue	1.Add UE5,QE11 & Reserve CE52,RE90 2.RE292 footprint change from 0ohm-short to 0 ohm(@)	0.6(X05)
79	32	HW	2015/07/13	COMPAL	For Board ID	RE79 change from 2k to 8.2k	0.6(X05)
80	18	HW	2015/07/17	COMPAL	For RF request	1.Change RC349/RC172(0 ohm) to LC1/LC2(BLM15HG601SN1D) 2.Pop CC313/CC314	0.6(X05)
81	36	HW	2015/07/17	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	0.6(X05)
82	17	HW	2015/08/17	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control to +VCCPLL_OC power rail	0.7(X06)
83	17	HW	2015/08/17	COMPAL	Follow Park City for DC mode CPU trubo issue	Reserved RE313 pull down path on I_SYS	0.7(X06)
84	17	HW	2015/08/17	COMPAL	Change design soluiton for prevent thermal too high	UV29 change from APL5930QBI-TRG_TDFN10_3X3 to G9661-25ADJRE1U_TDFN10_3X3 & VIN change from +3.3V_RUN to +1.8V_PRIM	0.7(X06)
85	32	HW	2015/08/19	COMPAL	For Board ID	RE79 change from 8.2k to 62k	0.7(X06)
86	36	HW	2015/08/27	COMPAL	For 儲存巴士 & Dell USB HDD issue at Low battery on 3 cell battery	1.Pop CI14; depop CI32 2.UI3 change from SA00007TJ00 to SA000097E00 3.Reserve CI33,CI34	0.7(X06)
87	9	HW	2015/09/09	COMPAL	Add GPIO for China TPM & TPM option	add TPM_TYPE signal &RC349	1.0(A00)
88	8	HW	2015/09/09	COMPAL	For TP issue	Depop CC4	1.0(A00)
89	32	HW	2015/09/09	COMPAL	For Board ID	RE79 change from 62k to 1k	1.0(A00)
90	12,28,32,27	HW	2015/09/09	COMPAL	For MP	1.Depop SW1, RC221 change to 0 ohm short pad 2.UR2 change from SA000089Q00 to SA000089Q10 3.UE2 change from SA00006YH30 to SA00006YH90 4.UL1 change from SA000081G0L to SA000081G1L	1.0(A00)